Semester Long Internship Spring 2026

On

Designing Integrated Circuit in eSim

Submitted by

Sufiyan Shaikh
Pune Institute of Computer Technology, Pune

Under the guidance of

Prof. Prabhu Ramachandran
Principal Investigator
Department of Aerospace Engineering
Indian Institute of Technology Bombay

June 8, 2026

Acknowledgment

I express my sincere gratitude to Prof. Prabhu Ramachandran for providing me with the opportunity to be part of the FOSSEE internship program and for his continued efforts in promoting open-source engineering tool development. His leadership and vision have been instrumental in fostering meaningful student participation in the open-source ecosystem.

I also acknowledge Prof. Kannan M. Moudgalya for his foundational role in establishing and strengthening the FOSSEE initiative. His contributions to open-source education and the development of the FOSSEE fellowship framework have been pivotal in creating the academic and organisational platform through which this internship was undertaken.

My sincere appreciation extends to my mentor, Sumanto Kar, for his continual support, technical guidance, and encouragement throughout the duration of this project. His insights and feedback played a key role in refining ideas, overcoming challenges, and ensuring timely completion of the tasks assigned to me.

I would also like to thank my internal mentors, Mr. Varad Patil and Ms. Shanthi Priya K for their valuable guidance, coordination, and technical inputs during the internship. Their mentorship contributed significantly to the clarity, progress, and successful execution of the work.

This internship has been an enriching learning experience, allowing me to work closely with open-source EDA tools, develop IC subcircuits in eSim, and gain exposure to realworld circuit modeling and simulation workflows. The knowledge acquired during this period will undoubtedly support my future academic and professional pursuits.

I would also like to thank the entire FOSSEE team for their coordination, assistance, and timely interactions at various stages of this work. Their collective efforts ensured smooth workflow, resource accessibility, and effective project execution.

Contents

Chapter 1

Introduction

The FOSSEE (Free/Libre and Open Source Software for Education) project is a nationwide initiative dedicated to promoting the use of open-source software in order to improve the quality of education in India. The central aim of the project is to minimize dependence on proprietary software in academic institutions by encouraging the adoption of free and open-source alternatives. Through various programs and activities, FOSSEE facilitates the transition from commercial software to reliable, freely accessible open-source tools. Additionally, the project focuses on developing new FLOSS tools and enhancing existing ones to meet the continuously evolving requirements of education and research. FOSSEE functions under the National Mission on Education through Information and Communication Technology (NME-ICT), an initiative launched by the Ministry of Education (formerly the Ministry of Human Resource Development), Government of India. The project offers a comprehensive support framework that includes extensive documentation, interactive learning resources, hands-on training programs, and workshops. These efforts are aimed at enabling students, educators, and professionals to effectively incorporate open-source tools into their academic and research activities. By fostering a culture of collaboration, inclusivity, and innovation, FOSSEE has played a significant role in making technology more accessible and has created new avenues for learning and experimentation across a wide range of disciplines.

1.1 Background

Electronic Design Automation (EDA) tools play a crucial role in the design, simulation, analysis, and verification of modern electronic circuits and systems. These tools assist engineers in developing analog, digital, and mixed-signal circuits while reducing design complexity, development time, and manufacturing costs. Traditionally, advanced EDA software has been dominated by proprietary solutions such as OrCAD, PSpice, HSPICE, and Xpedition, which often require expensive licenses and infrastructure.

To address the growing need for accessible and affordable design tools in academia and industry, several open-source EDA initiatives have emerged. These platforms provide students, researchers, educators, and small-scale industries with powerful design capabilities without licensing restrictions. Open-source EDA tools promote collaborative development, transparency, customization, and wider adoption of electronic design methodologies.

Among such initiatives, eSim has emerged as a significant open-source EDA platform developed under the FOSSEE (Free/Libre and Open Source Software for Education) project at the Indian Institute of Technology Bombay. The tool aims to provide a comprehensive environment for circuit design, simulation, analysis, and PCB development while encouraging the use of free and open-source software in engineering education and research.

1.2 Overview of eSim

eSim (previously known as Oscad/FreeEDA) is a free and open-source Electronic Design Automation (EDA) software developed by the FOSSEE team at the Indian Institute of Technology Bombay. It provides an integrated environment for schematic capture, circuit simulation, analysis, and PCB design using various open-source technologies. eSim is released under the GNU General Public License (GPL) and serves as an alternative to several commercial EDA tools.

The software combines multiple open-source components, including KiCad for schematic capture and PCB design, Ngspice for circuit simulation, GHDL and Verilator for digital design verification, OpenModelica for system-level modeling, and SkyWater SKY130 Process Design Kit (PDK) support for integrated circuit design. Through this integration, eSim enables users to perform analog, digital, and mixed-signal circuit development within a unified platform.

One of the key strengths of eSim is its ability to provide professional-grade design and simulation capabilities without requiring expensive software licenses. It supports SPICE model integration, custom subcircuit development, waveform analysis, PCB layout generation, and various simulation workflows. These features make it particularly suitable for engineering education, academic research, open-source hardware development, and industrial prototyping.

In this internship, eSim was utilized for the development, implementation, and verification of various integrated circuit subcircuits. The work involved studying device datasheets, constructing equivalent circuit models, implementing subcircuits within the eSim environment, and validating their behavior through simulation-based analysis.

1.3 Objectives of the Project

The primary objective of this work was to study, implement, and verify the functional behavior of various analog and digital integrated circuits using the eSim environment. The project aimed to understand the internal operation of different devices through a detailed analysis of manufacturer datasheets and to reproduce their functionality using the circuit elements and device models available within the eSim framework.

Another important objective was to contribute towards the enhancement of the eSim ecosystem by developing reusable models and schematic symbols wherever possible. In addition to complete subcircuit development, emphasis was also placed on behavioral modeling and simulation-based verification of devices whose subcircuits were not fully realized. This approach helped in studying a broader range of integrated circuits and understanding their operating principles.

The project also sought to design suitable test circuits and analyze the corresponding simulation results in order to validate the implemented models. Particular importance was given to ensuring that the observed characteristics agreed with the functional specifications provided by the manufacturers. Through this process, an effort was made to maintain consistency between theoretical device operation and simulation behavior.

Furthermore, the work aimed to provide practical exposure to open-source Electronic Design Automation (EDA) tools and simulation methodologies. The project facilitated hands-on experience with eSim, KiCad, and NgSpice, thereby strengthening the understanding of circuit modeling, simulation workflows, and component development. The knowledge and experience gained through this work are expected to be beneficial for future studies and applications involving analog and digital circuit design.

1.4 Methodology

The implementation process began with a detailed study of datasheets obtained from semiconductor manufacturers such as Texas Instruments and Analog Devices. The datasheets were examined to understand the internal architecture, electrical characteristics, truth tables, pin configurations, and operating conditions of the selected devices. This analysis served as the foundation for determining the most appropriate approach for reproducing the functionality of each integrated circuit.

After understanding the device specifications, the internal circuitry was implemented using the components and device models already available within the eSim environment. Depending on the complexity and feasibility of the device, either a complete subcircuit was developed or a behavioral model was constructed to reproduce the essential functionality of the integrated circuit. Special attention was given to ensuring that the implemented circuits accurately reflected the behavior described in the corresponding datasheets.

For devices intended to be represented within the eSim library, schematic symbols were created based on the package information and pin assignments specified by the manufacturers. Proper pin mapping and terminal arrangements were incorporated to ensure compatibility between the symbol representation and the implemented circuit model. This facilitated the integration of the devices into larger circuit designs and improved the usability of the developed models.

Following the implementation stage, appropriate test circuits were designed to evaluate the operation of the devices under different input conditions. These test configurations were developed with the objective of verifying the logical functionality, switching characteristics, and overall response of the implemented circuits. Simulation studies were performed using the KiCad-to-NgSpice interface provided by eSim, and the generated waveforms were analyzed to study the behavior of the circuits.

Whenever discrepancies were observed between the simulated results and the expected characteristics described in the datasheets, the circuit implementation was revisited and necessary modifications were carried out. This iterative process of implementation, testing, analysis, and refinement continued until satisfactory agreement with the expected device behavior was achieved. The final results were then documented through schematics, symbols, test circuits, and simulation plots to provide a comprehensive record of the work carried out.

Chapter 2

Literature Survey

2.1 Open-Source Electronic Design Automation Tools

Open-source Electronic Design Automation (EDA) tools have become increasingly important in academic and research environments owing to their accessibility and flexibility. Among these tools, eSim provides an integrated platform for schematic capture, simulation, and circuit analysis by combining KiCad and NgSpice. Such tools enable users to design and verify analog and digital circuits without relying on proprietary software and promote the adoption of open-source methodologies in electronics education and research.

2.2 eSim Framework

eSim, developed under the FOSSEE project at the Indian Institute of Technology Bombay, is an open-source EDA tool designed for circuit design and simulation. It integrates schematic capture capabilities provided by KiCad with the simulation features of NgSpice. In addition to supporting analog and digital circuit analysis, eSim provides facilities for component modeling, subcircuit development, and library management, making it suitable for educational as well as research-oriented applications.

2.3 Circuit Simulation using NgSpice

NgSpice is a widely used open-source circuit simulator capable of performing DC, AC, transient, and mixed-signal analyses. It provides a flexible environment for verifying the behavior of electronic circuits before hardware implementation. In the present work, NgSpice was employed through the eSim interface to analyze the performance of the developed circuits and validate their functionality under different operating conditions.

2.4 Datasheet-Based Circuit Modeling

Datasheets published by semiconductor manufacturers serve as the primary source of information regarding the electrical characteristics and internal operation of integrated circuits. Parameters such as truth tables, recommended operating conditions, internal block diagrams, and timing characteristics provide valuable insights for circuit implementation. Accurate interpretation of these specifications is essential for reproducing the behavior of devices within simulation environments.

2.5 Subcircuit Development and Symbol Creation

The development of reusable subcircuits and schematic symbols plays an important role in extending the capabilities of circuit simulation platforms. Subcircuits simplify the representation of complex devices and facilitate their integration into larger designs, while schematic symbols provide a standardized interface for circuit development. Proper mapping between symbol pins and subcircuit terminals ensures consistency and improves the usability of component libraries.

Chapter 3

Problem Statement

3.1 Problem Statement

To design and develop various analog and digital integrated circuit models in the form of sub-circuits using device model files already present in the eSim library. These IC models should be useful for future circuit design purposes by developers and users once they are successfully integrated into the eSim sub-circuit library.

3.2 Approach

The implementation process followed a systematic workflow consisting of datasheet analysis, subcircuit development, symbol creation, simulation testing, and validation. The primary objective was to develop accurate and reusable IC subcircuits for integration into the eSim library. Each device was implemented based on manufacturer specifications and verified through simulation to ensure correct functionality. The overall methodology adopted during the internship is described below.

3.2.1 Datasheet Analysis

The first stage involved studying the datasheets of various analog and digital integrated circuits from reputed semiconductor manufacturers. The internal architecture, functional description, electrical characteristics, truth tables, and application circuits were carefully examined to understand the operating behavior of each device. Based on this analysis, suitable ICs were selected for implementation in eSim.

3.2.2 Subcircuit Development

After understanding the device operation, an equivalent circuit model was developed using the components and simulation models available within the eSim environment. The implementation was carried out according to the specifications provided in the datasheet while ensuring compatibility with the eSim simulation framework. The developed circuit was then converted into a reusable subcircuit.

3.2.3 Symbol and Pin Configuration

For each implemented device, an appropriate schematic symbol was created based on the package information and pin configuration specified in the datasheet. Input, output, power, and control pins were mapped correctly to ensure seamless integration of the subcircuit into user designs.

3.2.4 Test Circuit Design

To verify the correctness of the developed subcircuit, dedicated test circuits were designed based on recommended application circuits and operating conditions described in the datasheet. Various input combinations and operating scenarios were considered to evaluate the functional behavior of the device.

3.2.5 Simulation and Validation

The developed subcircuits and their corresponding test circuits were simulated using eSim's NgSpice-based simulation environment. Output waveforms, logic states, and electrical characteristics were analyzed and compared with expected datasheet behavior. Any discrepancies observed during testing were investigated and corrected through iterative modifications to the circuit model. The validation process was repeated until satisfactory agreement with the device specifications was achieved.

Chapter 4

IC Sub-circuit creation

4.1 CD4585B

4.1.1 Overview

The CD4585B is a 4-bit magnitude comparator designed to compare two 4-bit binary numbers and determine their relative magnitudes. The device provides three output signals indicating whether one binary number is greater than, less than, or equal to the other. In addition to basic comparison functionality, the IC supports cascading, allowing multiple comparators to be connected together for the comparison of larger binary words.

The CD4585B is commonly used in digital systems requiring numerical comparison operations, including arithmetic logic units (ALUs), digital control systems, microprocessor-based applications, and data processing circuits. Its cascading capability makes it suitable for applications involving multi-bit data comparison while maintaining simple circuit implementation.

As part of this internship, the CD4585B was implemented as a reusable subcircuit within the eSim environment. The objective was to accurately reproduce the functional behavior of the device according to its datasheet specifications and validate its operation through simulation.

4.1.2 Internal Circuit Analysis

The CD4585B operates by comparing corresponding bits of two 4-bit binary inputs, designated as A3–A0 and B3–B0. The comparison process begins with the most significant bits and proceeds toward the least significant bits. At each stage, the internal logic evaluates the equality condition between corresponding bits before propagating the result to subsequent stages. This hierarchical comparison mechanism ensures that the magnitude relationship is determined correctly even when differences exist only in lower-order bits. The internal logic network evaluates the relationship between corresponding bit pairs and generates one of three output conditions: A¿B, A¡B, or A=B.

The device also includes cascade input terminals that enable multiple CD4585B comparators to be connected together for higher-bit comparisons. These cascade inputs allow the comparison result from a lower-order stage to influence the final output, ensuring correct operation when comparing binary numbers wider than four bits. The hierarchical comparison mechanism employed by the device ensures that the magnitude relationship between the two binary numbers is correctly established even when differences occur only in the lower-order bits. This arrangement enables efficient comparison while minimizing the amount of additional logic required in practical implementations.

4.1.3 Subcircuit Implementation

The CD4585B subcircuit was developed in eSim by implementing the comparator logic described in the manufacturer datasheet. The design was constructed using logic gates available within the simulation environment and organized into a reusable hierarchical subcircuit.

Special attention was given to the implementation of the greater-than, less-than, and equality detection logic, as well as the cascading functionality required for multi-stage comparisons. The completed schematic was verified to ensure that the generated outputs matched the expected truth table for all input combinations. The circuit was organized in a hierarchical manner to improve readability and simplify future modifications. Throughout the implementation process, emphasis was placed on maintaining consistency between the simulated behavior and the functional characteristics described in the manufacturer datasheet.

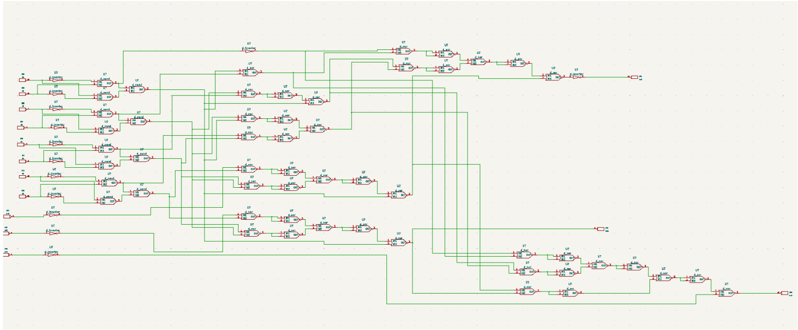


Figure 4.1

4.1.4 Symbol Creation

4.1.5 Test Circuit

A dedicated test circuit was developed to validate the functionality of the implemented CD4585B subcircuit. Various combinations of binary inputs were applied to the A and B terminals to verify the greater-than, less-than, and equality outputs.

The test cases included equal input values, conditions where A exceeded B, and conditions where B exceeded A. Additional verification was performed to ensure proper operation of the comparison logic under different input combinations.

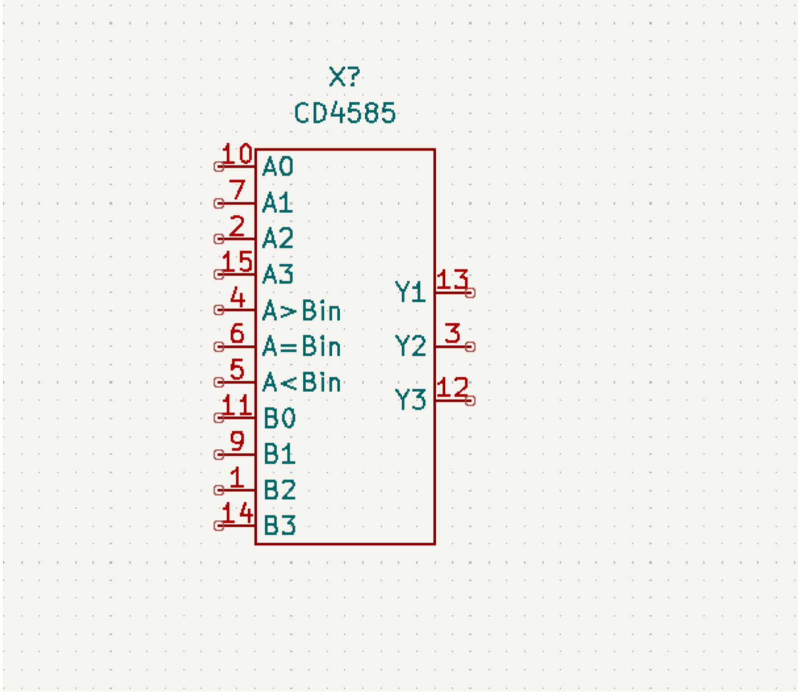


Figure 4.2

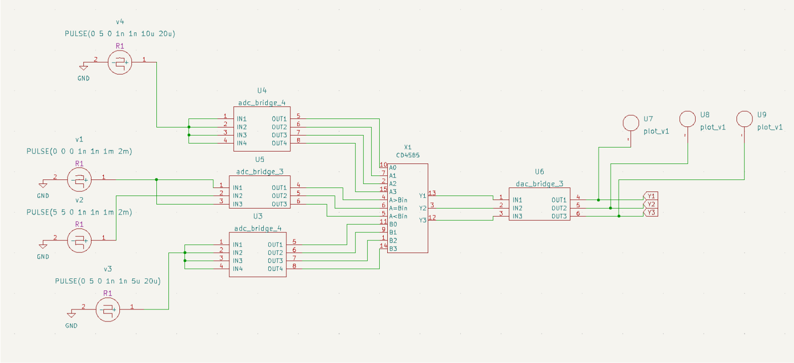


Figure 4.3

4.1.6 Simulation Results

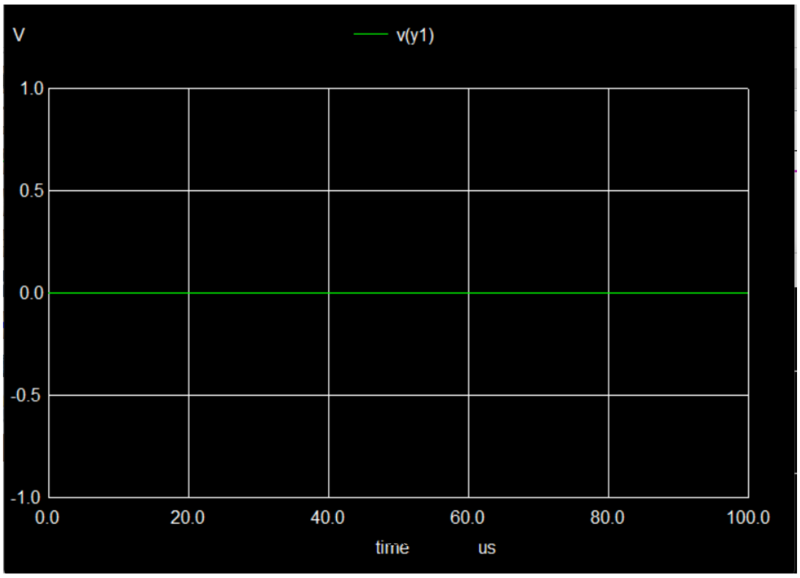


Figure 4.4

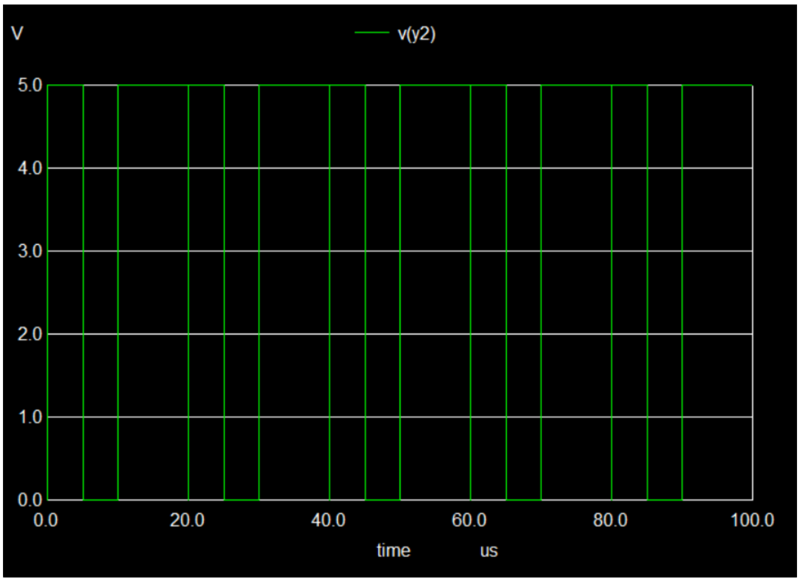


Figure 4.5

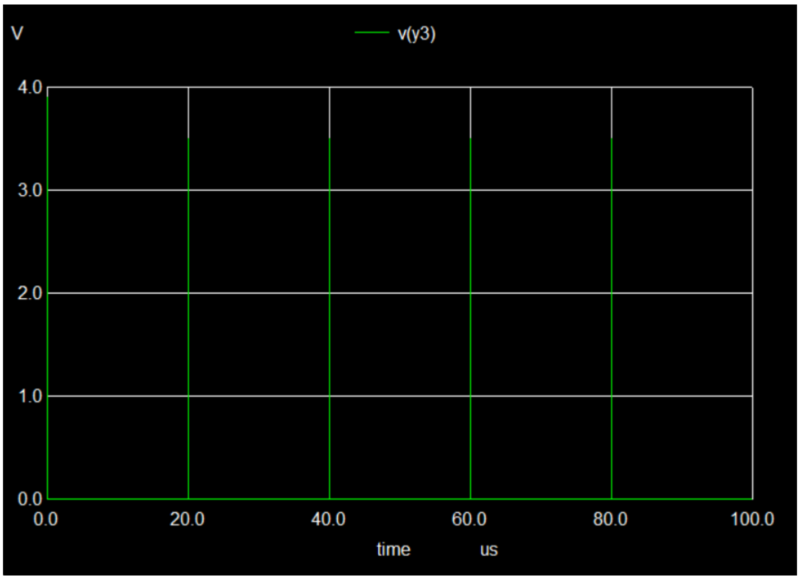


Figure 4.6

The generated waveforms were analyzed and compared with the expected truth table specified in the device documentation. The obtained results demonstrated correct operation of the greater-than, less-than, and equality outputs under different input conditions. The successful verification of the circuit confirms that the developed subcircuit accurately reproduces the functional characteristics of the CD4585B.

4.2 SN74ALS156 Dual 2-Line to 4-Line Decoder/Demultiple

4.2.1 Overview

The SN74ALS156 is a dual 2-line to 4-line decoder/demultiplexer fabricated using Advanced Low-Power Schottky (ALS) technology. The device contains two independent decoder sections with common address inputs and separate enable controls. Depending on the binary state of the address lines, one of the four outputs corresponding to the selected decoder section is activated. The outputs are active-low and employ open-collector transistor stages, enabling interfacing with a variety of external circuits through pull-up resistors.

Due to its decoding capability and compatibility with TTL logic families, the SN74ALS156 finds applications in memory addressing, data routing, code conversion, and digital control systems. Its open-collector outputs provide flexibility for wired logic applications and allow multiple devices to share common output lines when required.

4.2.2 Internal Circuit Analysis

The internal architecture of the SN74ALS156 consists of two decoder sections that share a common pair of address inputs while maintaining separate enable terminals. The decoder logic translates the binary information present at the address inputs into one of four output lines. Since the outputs are active-low, the selected output is driven to a low state while the remaining outputs remain in the high-impedance state through external pull-up resistors.

The output stage is implemented using open-collector transistor configurations, which distinguish the device from conventional totem-pole output logic circuits. This arrangement enables greater flexibility in interfacing and allows external loads operating at different voltage levels to be controlled. The use of ALS technology provides reduced power consumption and improved switching characteristics while maintaining compatibility with standard TTL systems.

4.2.3 Circuit Implementation

The functional behavior of the SN74ALS156 was reproduced within the eSim environment by implementing the decoder logic and the open-collector output stages using available simulation components. Particular attention was given to accurately modeling the active-low characteristics and the enable functionality of the device.

The implementation was carried out with the objective of reproducing the truth table and switching characteristics specified in the manufacturer datasheet. Appropriate pull-up arrangements were incorporated to realize the open-collector behavior of the outputs. The resulting circuit was subsequently analyzed under different combinations of address and enable inputs to verify its operation.

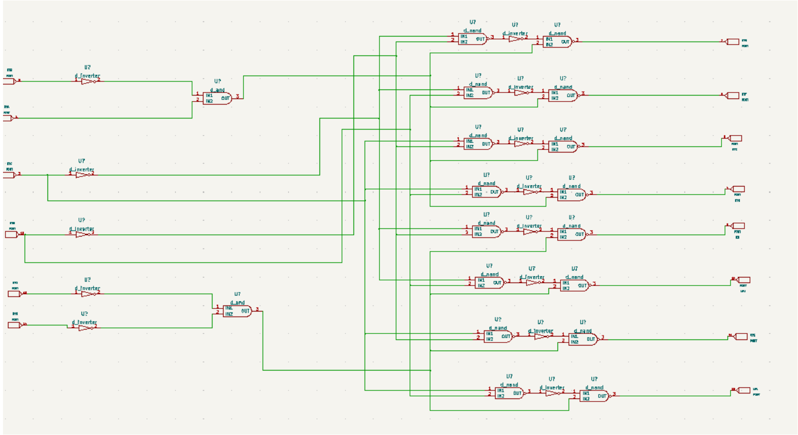


Figure 4.7

4.2.4 Symbol Creation

A schematic symbol corresponding to the SN74ALS156 was created based on the package configuration and pin assignments provided in the datasheet. The symbol includes the common address inputs, individual enable inputs, output terminals, and power connections required for device operation.

Proper pin mapping was carried out to ensure consistency between the symbol and the implemented circuit model. The developed symbol facilitates convenient integration of the device into larger digital systems and improves the readability of circuit schematics.

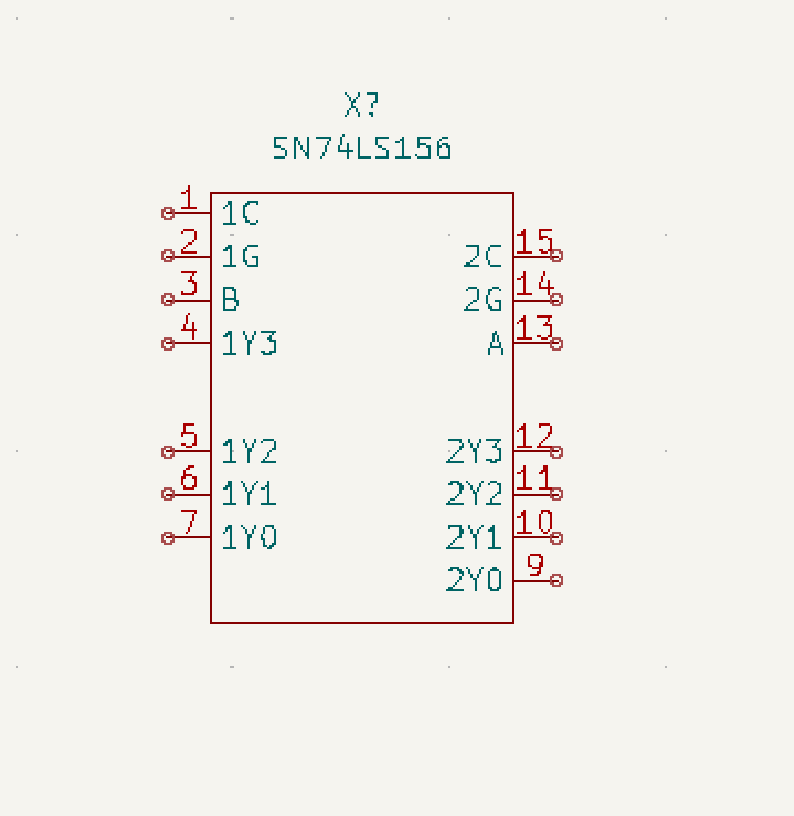


Figure 4.8

4.2.5 Test circuit

A suitable test circuit was developed to evaluate the operation of the implemented model under various input conditions. The test setup was designed to exercise the decoding functionality of the device and to observe the corresponding output response.

Different combinations of control and input signals were applied during simulation to verify the expected behavior of the circuit.

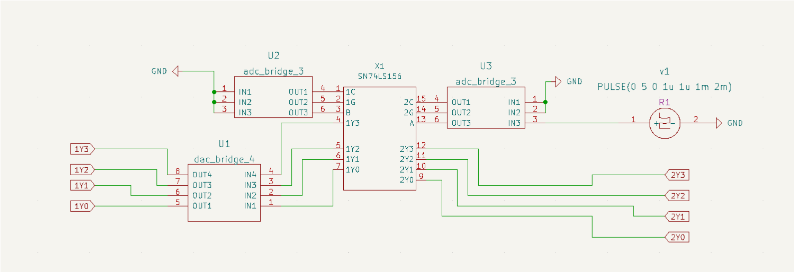


Figure 4.9

4.2.6 Simulation Results

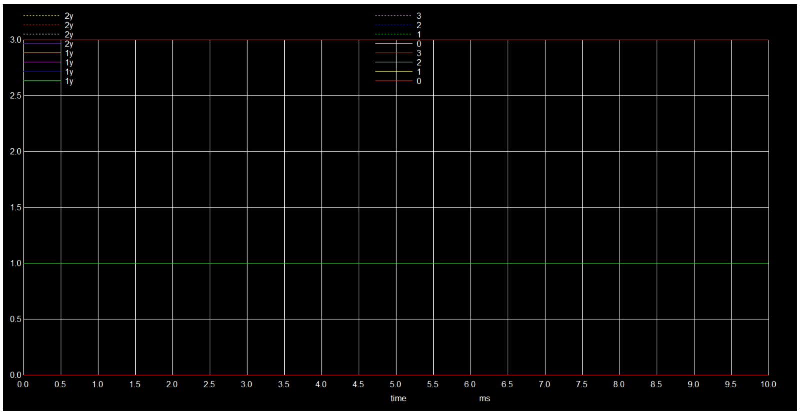


Figure 4.10

4.3 SNx5452B Dual Peripheral Driver

4.3.1 Overview

The SNx5452B is a dual peripheral driver designed to provide high-current output capability for interfacing logic circuits with external loads. It consists of two independent driver channels that enable low-power digital signals to control devices requiring higher current levels.

The device is commonly employed in switching and interfacing applications involving relays, indicators, lamps, and other peripheral components. Its high current gain and compatibility with digital logic families make it suitable for industrial control systems and digital electronics applications.

The device is intended for applications requiring higher current drive capability than that available from standard logic circuits. Typical applications include relay drivers, lamp drivers, solenoid control circuits, and various interfacing applications in digital systems.

4.3.2 Internal Circuit Analysis

The SNx5452B consists of two identical driver channels, each containing input circuitry and a high-current transistor output stage. The input stage accepts logic-level signals and controls the output transistor arrangement responsible for driving external loads.

The internal transistor configuration provides current amplification and switching capability while maintaining compatibility with standard digital logic levels. The two channels operate independently, allowing simultaneous control of separate loads. The device architecture is designed to provide reliable operation in applications requiring higher output current than that available directly from conventional logic circuits.

4.3.3 Circuit Implementation

The circuit was implemented by recreating the functional blocks of the SNx5452B using components available within the eSim environment. Particular attention was given to the transistor output stage and the associated current-driving characteristics to ensure behavior consistent with the device specifications.

The implemented model was simulated under different input conditions to verify the switching behavior of both driver channels and to observe the corresponding output response.

Particular emphasis was placed on reproducing the switching characteristics and current-driving capability of the output stages. The developed model was evaluated under different input conditions to verify its operation.

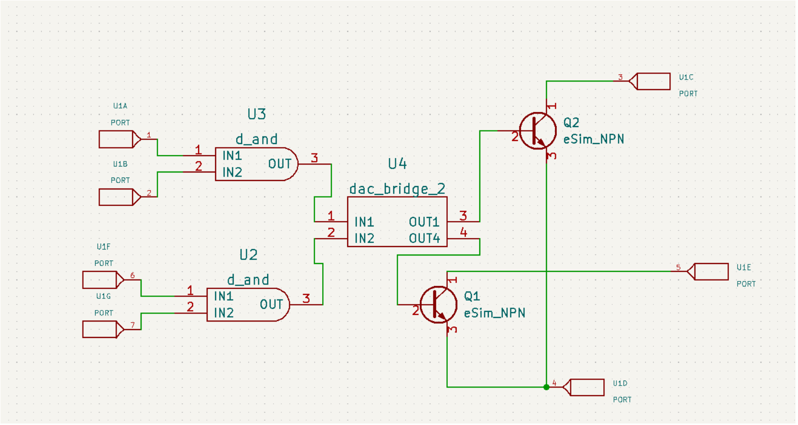


Figure 4.11

4.3.4 Symbol Creation

After the successful implementation of the SNx5452B subcircuit, a custom schematic symbol was created to facilitate its use in higher-level circuit designs. The symbol was designed in accordance with the standard 8-pin package configuration of the device. Pins 1 and 2 correspond to the inputs of Channel 1 (1A and 1B), while pin 3 represents the open-collector output 1Y. Pin 4 serves as the common ground terminal. Similarly, pins 6 and 7 correspond to the inputs of Channel 2 (2A and 2B), and pin 5 represents the output 2Y.

Appropriate electrical types were assigned to all pins to ensure proper ERC validation. The input pins were defined as input pins, the output pins were designated as open-collector outputs, and the ground pin was configured as a power input. The symbol was then associated with the developed subcircuit model, enabling the SNx5452B to be used as a reusable component in subsequent simulations. This approach closely emulates the behavior and pin configuration of the actual integrated circuit and allows the device to be incorporated easily into larger electronic systems.

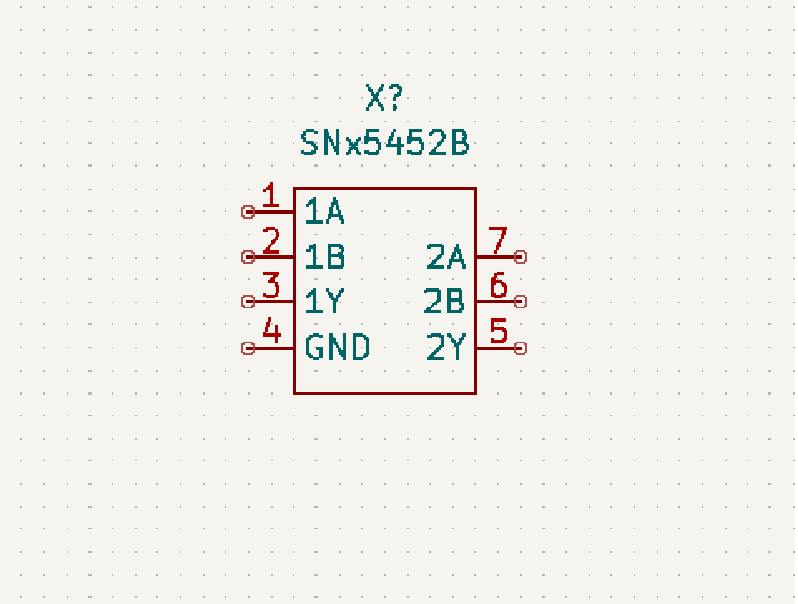


Figure 4.12

4.3.5 Test Circuit

A test circuit was constructed to verify the functionality of the developed SNx5452B model. The device outputs were configured as open-collector outputs and were connected to external pull-up resistors of 4.7 kΩ tied to a +5 V supply. Pulse voltage sources were applied to the input terminals in order to generate varying combinations of logic levels during transient analysis.

The input signals were selected such that all four possible input combinations were obtained over the simulation interval. This allowed the output behavior to be observed and compared with the expected NAND truth table. Whenever both inputs of a particular channel were at logic HIGH, the corresponding transistor switched ON and pulled the output to ground, resulting in a logic LOW. For all other input combinations, the transistor remained OFF and the pull-up resistor maintained the output at logic HIGH.

Transient analysis was carried out to observe the switching characteristics of the device and to verify its operation over time. The resulting waveforms demonstrated that the developed model accurately reproduced the open-collector NAND functionality of the SNx5452B, thereby confirming the correctness of the implemented subcircuit.

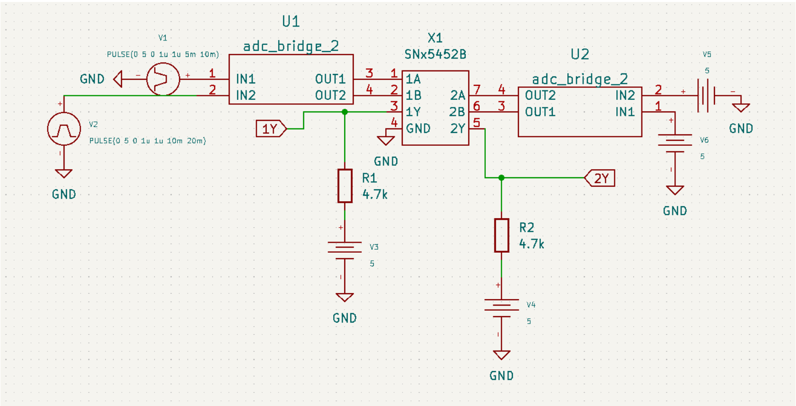


Figure 4.13

4.3.6 Simulation Results

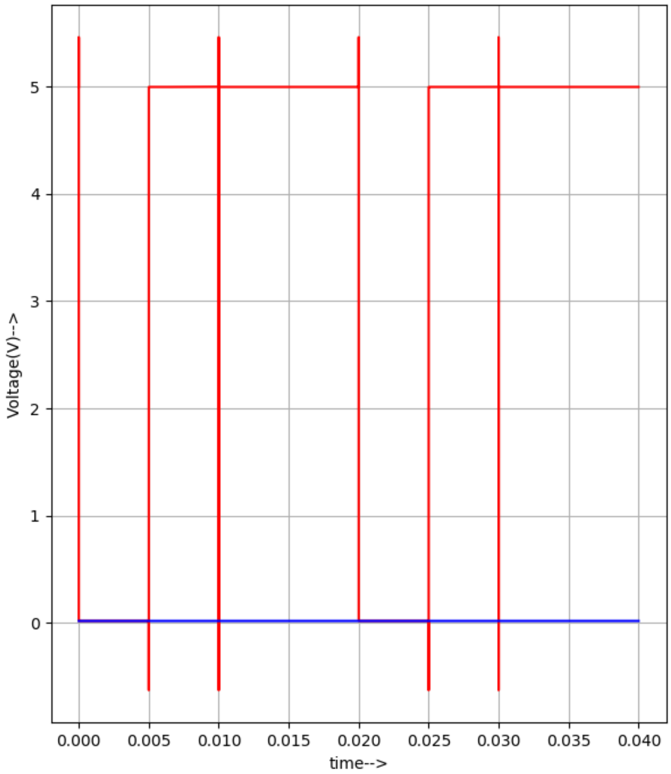


Figure 4.14

A transient analysis was performed by applying pulse inputs to the SN75452B model. The output waveform was observed at pin 1Y. During the intervals when both input signals were simultaneously at logic HIGH, the corresponding output transistor conducted and pulled the output to ground. Consequently, the output voltage remained close to 0 V, confirming the open-collector NAND behavior of the SN75452B. The obtained waveform agrees with the expected truth table of the device, thereby validating the correctness of the implemented subcircuit model.

4.4 SN74HC03 Quad 2-Input NAND Gate with Open-Drain Outputs

4.4.1 Overview

The SN74HC03 is a high-speed CMOS device consisting of four independent two-input NAND gates with open-drain outputs. The open-drain configuration allows the outputs to be connected together through an external pull-up resistor, making the device suitable for wired-AND logic and interfacing applications involving multiple voltage levels.

The device combines the low power consumption of CMOS technology with high noise immunity and fast switching characteristics. Owing to its open-drain outputs, the SN74HC03 is widely used in digital logic systems, bus-oriented architectures, signal interfacing circuits, and applications requiring external load driving capability.

The combination of CMOS technology and open-drain outputs provides high noise immunity, low static power dissipation, and flexibility in interfacing with external circuits. These characteristics make the device suitable for bus-oriented systems and digital control applications.

4.4.2 Internal Circuit Analysis

The SN74HC03 contains four independent two-input NAND gates implemented using CMOS transistor technology. Each gate performs the NAND operation on its corresponding input signals and drives an open-drain output stage.

Unlike conventional totem-pole outputs, the open-drain configuration can actively pull the output low but requires an external pull-up resistor to produce a logic-high level. This arrangement provides flexibility in interfacing and allows multiple outputs to share a common line. The internal transistor network ensures high-speed operation while maintaining low static power dissipation.

4.4.3 Subcircuit Implementation

The SN74HC03 was implemented in eSim by constructing the logic and output stages according to the device specifications. Particular emphasis was placed on accurately reproducing the open-drain output behavior, which distinguishes the device from standard NAND gate implementations.

The completed design was organized as a reusable subcircuit, allowing the device to be readily integrated into larger digital systems. The functionality of each gate and the operation of the output stage were verified through simulation.

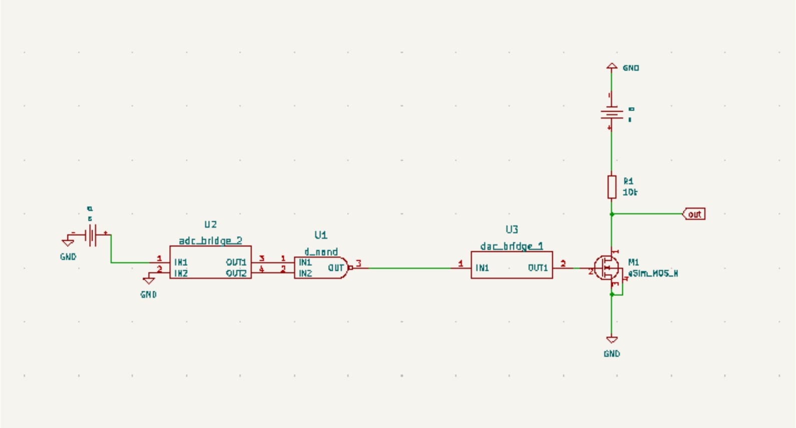


Figure 4.15

4.4.4 Symbol Creation

After completing the implementation of the internal subcircuit of the SN74HC03, a custom symbol was generated to represent the integrated circuit as a single functional component. The symbol was created to match the pin configuration of the actual 14-pin device specified in the datasheet. The eight input terminals corresponding to the four independent NAND gates were assigned to pins 1, 2, 4, 5, 9, 10, 12, and 13, while the four open-drain outputs were assigned to pins 3, 6, 8, and 11. Pins 7 was designated as GND.

The symbol creation process enables the complex internal circuitry consisting of NAND gates, digital-to-analog bridges, and NMOS output stages to be represented as a compact block. This significantly improves circuit readability and facilitates its use in higher-level designs without repeatedly exposing the internal implementation.

The generated symbol accurately reproduces the functionality of the SN74HC03 and provides an interface identical to the physical IC package. This approach simplifies the construction of application circuits and allows the device to be reused conveniently in future simulations.

Special attention was given to preserving the original pin arrangement of the device so that the symbol remains compatible with standard schematics and datasheet documentation. Consequently, the custom component behaves similarly to the commercially available SN74HC03 integrated circuit and can be incorporated into larger digital systems with ease.

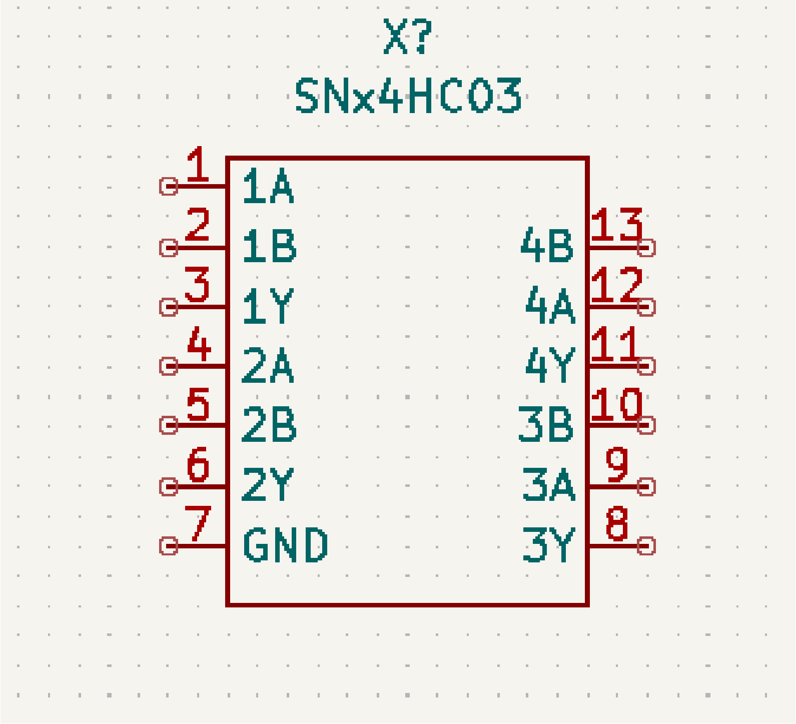


Figure 4.16

4.4.5 Test Circuit

A test circuit was constructed to verify the functional behavior of the developed SN74HC03 model. The supply voltage of +5 V was applied to pin 14, while pin 7 was connected to ground. Since the outputs of the SN74HC03 are open-drain, external pull-up resistors of 10 kΩ were connected between each output pin and the supply voltage. These resistors provide the logic HIGH state whenever the internal NMOS transistor is turned off.

For verification purposes, one NAND gate section was tested initially. Logic levels were applied to pins 1 and 2, corresponding to inputs 1A and 1B, while the output was observed at pin 3. The remaining unused inputs were connected to ground to avoid undefined logic conditions. Different combinations of logic HIGH and logic LOW were applied to the input terminals and the corresponding output voltage was monitored.

The simulation was performed using transient analysis. Input signals were generated using pulse sources to automatically cycle through all possible input combinations. The output waveform obtained from the simulation was compared with the theoretical truth table of the SN74HC03. The results confirmed that the output remained LOW whenever either input was LOW and became HIGH only when both inputs were HIGH, thereby validating the correct operation of the open-drain NAND gate.

The successful verification of one channel demonstrates the correctness of the overall four-channel implementation, since all four sections of the SN74HC03 are identical and operate independently. The developed model therefore accurately reproduces the behavior of the original integrated circuit and can be used for further digital circuit simulations and applications.

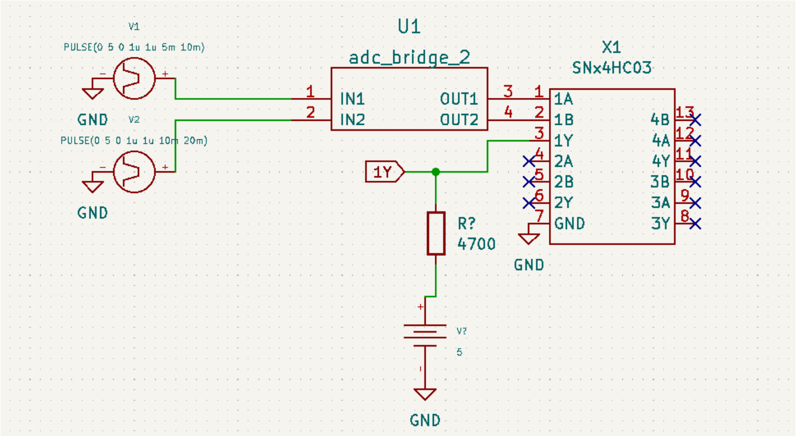


Figure 4.17

4.4.6 Simulation Results

The simulation results confirmed the correct operation of the NAND gates and demonstrated the characteristic behavior of the open-drain outputs. The generated waveforms were found to be in agreement with the functional specifications provided in the datasheet.

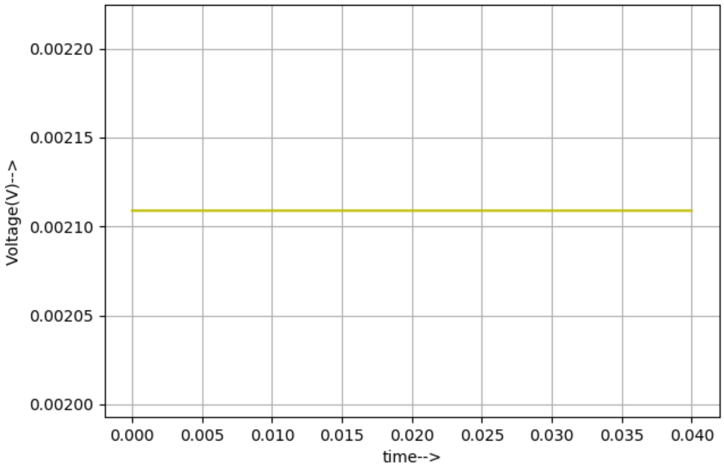


Figure 4.18

4.5 CD4073B Triple 3-Input AND Gate

4.5.1 Overview

The CD4073B is a CMOS integrated circuit consisting of three independent 3-input AND gates. Each gate performs the logical AND operation on three input signals and produces a HIGH output only when all the inputs are simultaneously HIGH. The device belongs to the CD4000 series of CMOS logic ICs and offers the advantages of low power consumption, high noise immunity, and a wide operating voltage range. Due to these characteristics, the CD4073B finds applications in digital control systems, combinational logic circuits, timing circuits, data processing systems, and various embedded and industrial applications.

The IC contains three identical gates, allowing multiple logic operations to be performed simultaneously within a single package. The device operates over a supply voltage range typically extending from 3 V to 18 V and is available in standard dual-in-line and surface-mount packages.

4.5.2 Internal Circuit Analysis

Although the external function of the CD4073B is that of a 3-input AND gate, the internal realization is based on CMOS logic optimization techniques. Instead of implementing the AND operation directly, the circuit utilizes input inverters followed by NOR structures and a final inverter stage. This arrangement is derived from De Morgan's theorem and provides a more efficient transistor-level implementation.

Initially, each input signal is inverted to obtain the complemented signals. These inverted signals are then combined through NOR networks. Finally, the output of the NOR structure is inverted to obtain the desired AND operation.

The CMOS implementation provides excellent noise immunity and low static power dissipation. The actual IC also includes additional output buffering stages and protection circuitry to improve drive capability and protect the device from electrostatic discharge and overvoltage conditions. Since the IC contains three identical logic sections, the same internal architecture is repeated three times within the device.

4.5.3 Subcircuit Implementation

The subcircuit for the CD4073B was developed using basic digital logic components available in eSim. Since a direct 3-input NOR gate was not available, the required functionality was obtained using cascaded 2-input NOR gates together with inverter blocks.

For each gate, three inverter blocks were employed to generate the complemented input signals. The outputs of these inverters were combined through two cascaded NOR gates to realize the equivalent of a 3-input NOR function. A final inverter stage was used to convert the resulting logic expression into the desired 3-input AND operation.

This approach allowed the functional behavior of the actual IC to be reproduced accurately without requiring transistor-level implementation. Three identical sections were constructed to represent the three independent gates present in the CD4073B package. The completed subcircuit was then converted into a reusable hierarchical block for further simulations.

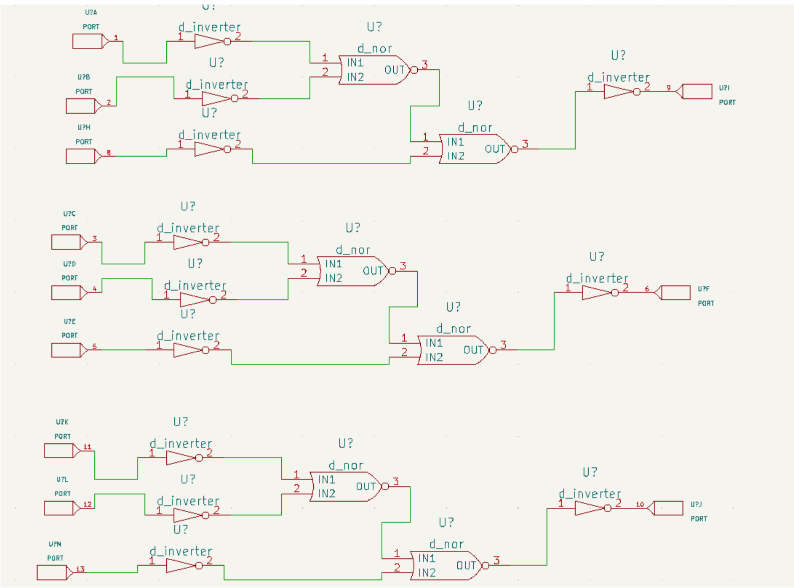


Figure 4.19

4.5.4 Symbol Creation

After the successful development of the subcircuit, a custom symbol corresponding to the CD4073B package was created. The symbol was designed according to the standard 14-pin package configuration specified in the datasheet.

Pins 1, 2, and 8 correspond to inputs A, B, and C respectively, while pin 9 represents output J. Similarly, pins 3, 4, and 5 serve as inputs D, E, and F with output K available at pin 6. The third gate utilizes pins 13, 12, and 11 as inputs G, H, and I respectively, with output L available at pin 10. Pin 14 is connected to the positive supply voltage VDD and pin 7 is connected to ground (VSS).

The custom symbol enabled the IC to be used in schematic diagrams exactly like a commercially available integrated circuit. This hierarchical approach improved modularity and simplified testing and verification procedures.

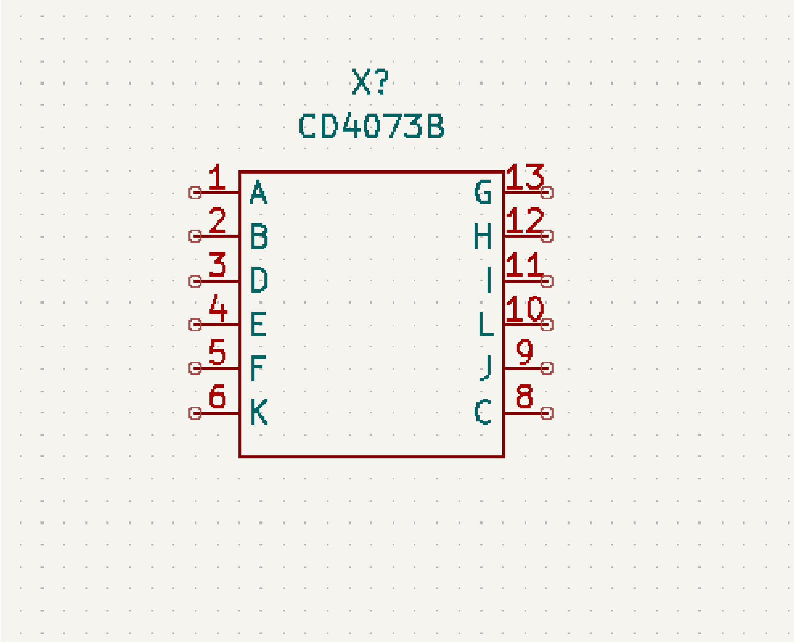


Figure 4.20

4.5.5 Test Circuit

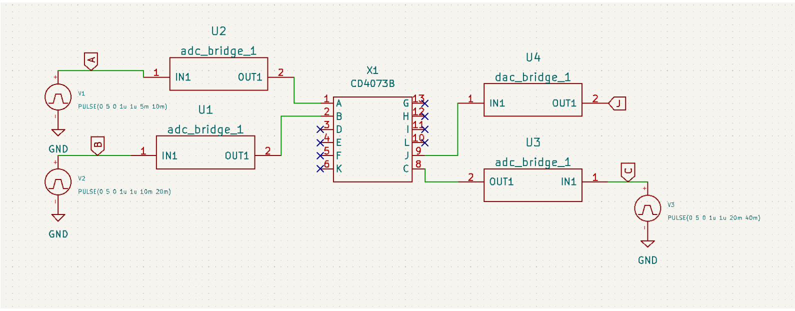


Figure 4.21

To verify the operation of the designed IC, a transient analysis test circuit was constructed. Three pulse voltage sources were applied to inputs A, B, and C of one of the AND gates. The pulse signals were selected with different periods so that all possible input combinations could be generated automatically during the simulation interval.

Input A was assigned the highest switching frequency, followed by input B and input C. This arrangement produced all eight possible combinations of the three input variables over one complete cycle. The output node J was monitored using voltage probes and waveform analysis tools.

Transient analysis was performed with a start time of 0 s, a stop time of 40 ms, and a suitable time step to accurately observe the transitions. The same methodology can be applied to the remaining two gates since all three sections of the IC are identical in construction and operation.

4.5.6 Simulation Results

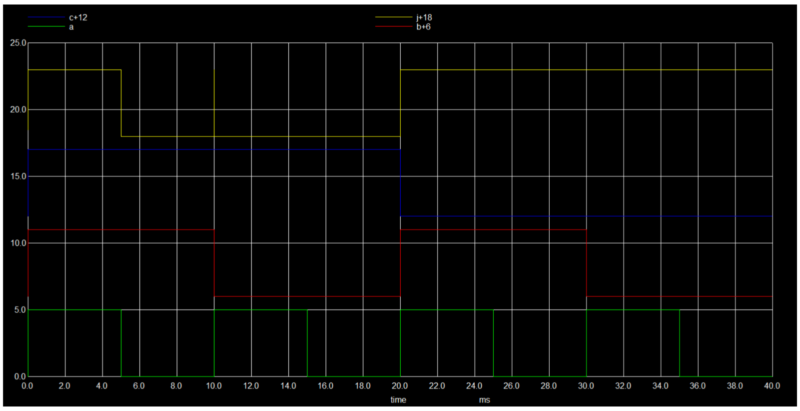


Figure 4.22

The transient response obtained from the simulation verified the correct operation of the CD4073B. The input waveforms generated all possible combinations of logic states over the specified time interval. Analysis of the output waveform demonstrated that the output remained LOW whenever one or more input signals were LOW.

A HIGH output was observed only during the interval in which all three input signals were simultaneously HIGH. This behavior is consistent with the truth table of a 3-input AND gate and confirms the successful realization of the logic function.

The obtained waveforms also showed proper switching characteristics and correct timing relationships between the input and output signals. The simulation results validated the accuracy of the developed subcircuit and confirmed that the custom IC model faithfully reproduces the behavior of the actual CD4073B integrated circuit. Therefore, the designed model can be effectively employed in larger digital systems and hierarchical circuit simulations requiring multiple 3-input AND operations.

4.6 CD74HCT241 Octal Buffer and Line Driver

4.6.1 Overview

The CD74HCT241 is an octal non-inverting buffer and line driver belonging to the High-Speed CMOS family with TTL-compatible input thresholds. The device is specifically designed to provide increased current driving capability and improved signal integrity in digital systems. It contains eight independent non-inverting buffers arranged into two groups of four outputs, with each group controlled by a separate active-low output enable input. The outputs of the device are three-state, allowing them to assume a logic HIGH, logic LOW, or high-impedance condition.

The high-impedance capability makes the CD74HCT241 particularly suitable for bus-oriented systems and applications where multiple devices share common signal lines. By placing unused outputs into the high-impedance state, bus contention can be avoided and efficient signal management can be achieved. The device is widely employed in microprocessor systems, memory interfaces, digital communication circuits, industrial control applications, and embedded electronic systems where reliable signal transmission and buffering are required.

The TTL-compatible characteristics of the CD74HCT241 enable seamless interfacing between CMOS and TTL logic families while maintaining low power dissipation and high noise immunity. Owing to its high-speed operation and enhanced output drive capability, the device serves as an effective interface element between low-current logic circuits and external loads requiring greater drive strength.

4.6.2 Internal Circuit Analysis

Internally, the CD74HCT241 consists of eight independent non-inverting buffer stages organized into two groups. Each group is associated with an active-low output enable signal, namely 1OE and 2OE. The enable inputs control the output stages of the corresponding four buffers simultaneously. When the output enable input is LOW, the outputs become active and each output follows the logic state present at its corresponding input. Conversely, when the output enable input is HIGH, the outputs enter the high-impedance state and are effectively disconnected from the external circuitry.

Each buffer stage incorporates CMOS transistor networks designed to provide high current drive capability and low propagation delay. The internal architecture ensures that the input signals are reproduced at the output without inversion. Since the outputs are isolated when disabled, multiple devices may share common buses without causing electrical conflicts.

The internal output structure provides improved fan-out capability, allowing the device to drive several digital inputs simultaneously. Furthermore, the CMOS implementation contributes to low static power consumption and high noise margins, making the device suitable for high-speed digital applications.

The functional organization of the IC enables flexible control over groups of outputs, thereby simplifying signal routing and bus management. This feature makes the CD74HCT241 highly advantageous in systems involving multiplexed data lines, address buses, and communication interfaces.

4.6.3 Subcircuit Implementation

The SPICE subcircuit model of the CD74HCT241 was developed to emulate the behavior of the actual integrated circuit within the eSim environment. The implementation included all eight non-inverting buffer channels together with their corresponding three-state output characteristics. Two enable inputs were incorporated to control the operation of the output groups in accordance with the functional specifications of the device.

The subcircuit accurately reproduces the logic functionality of the physical IC by ensuring that each output follows its respective input whenever the corresponding enable signal is active. When the enable input is deactivated, the associated outputs are placed in the high-impedance state, thereby simulating the bus isolation capability of the device.

Special consideration was given to maintaining compatibility with NGSpice simulation requirements. The resulting subcircuit model provides a realistic representation of the device and facilitates functional verification prior to hardware implementation. The modular structure of the subcircuit also improves reusability and simplifies integration into larger digital systems.

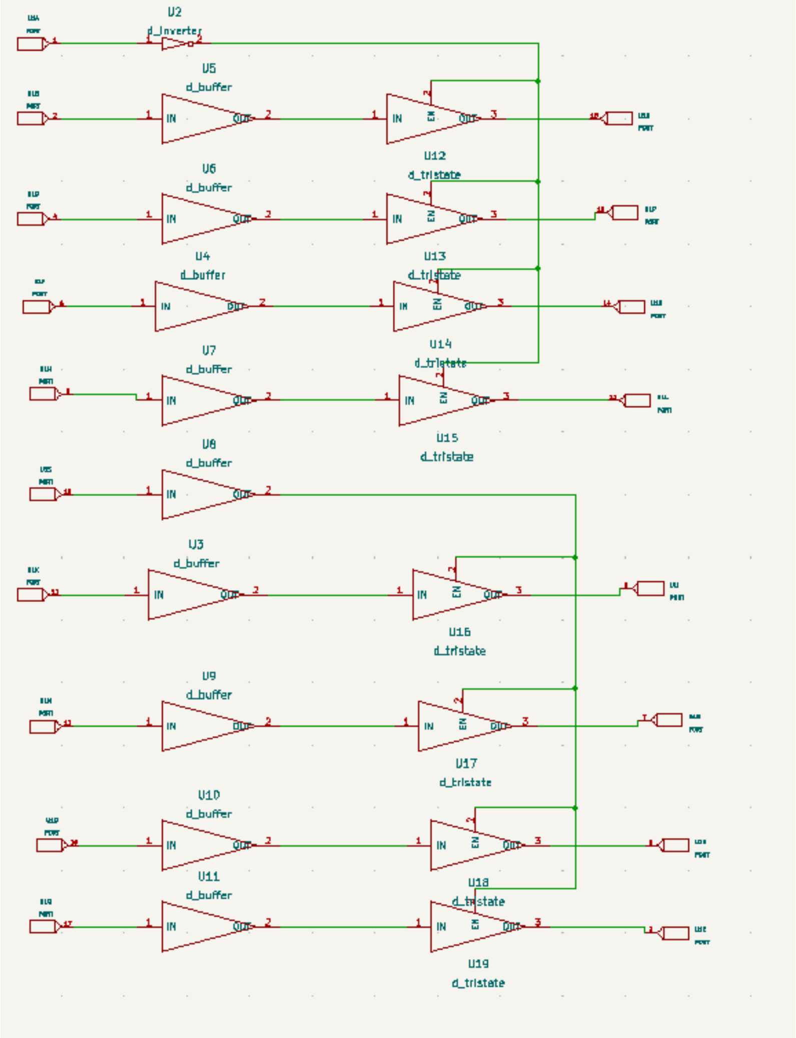


Figure 4.23

4.6.4 Symbol Creation

A custom schematic symbol for the CD74HCT241 was created to enable convenient use of the device within the eSim schematic editor. The symbol was designed in accordance with the pin configuration of the actual integrated circuit and includes all input, output, and enable terminals.

The symbol contains eight input pins designated as 1A0 through 1A3 and 2A0 through 2A3, along with eight corresponding outputs labelled 1Y0 through 1Y3 and 2Y0 through 2Y3. Two active-low enable inputs, namely 1OE and 2OE, were incorporated to provide control over the output groups. The arrangement of the pins was selected to closely resemble the physical package configuration and to facilitate intuitive schematic development.

The custom symbol simplifies circuit design and enhances readability by providing a clear representation of the device structure. Moreover, the availability of a dedicated symbol improves design efficiency and promotes modular implementation practices.

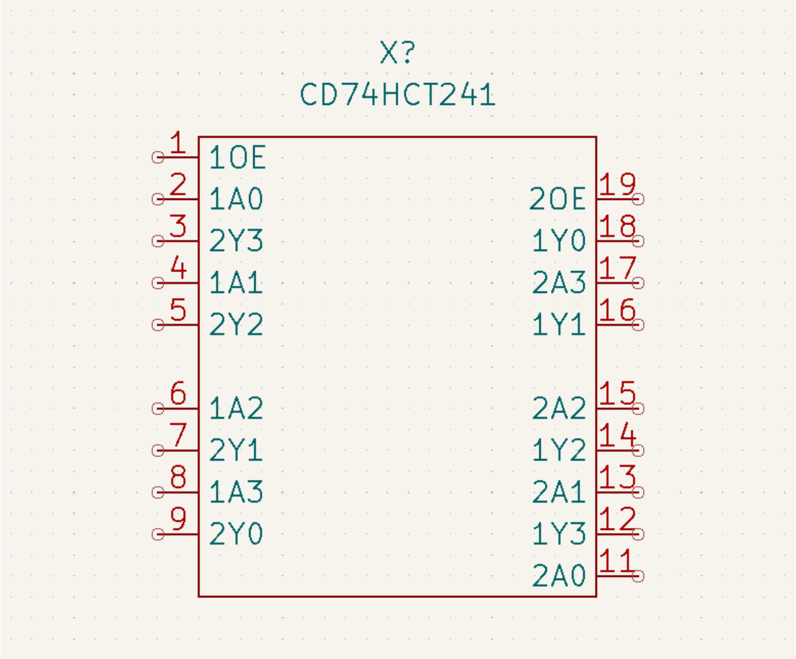


Figure 4.24

4.6.5 Test Circuit

A test circuit was constructed to verify the functional operation of the CD74HCT241. The output enable inputs were connected to logic LOW in order to activate both groups of outputs. Various combinations of digital signals were applied to the input terminals to examine the behavior of the corresponding outputs.

Input voltage sources representing logic HIGH and logic LOW levels were employed to stimulate the circuit. The outputs were monitored to determine whether they correctly reproduced the input signals. Additional tests were performed by driving the enable inputs HIGH so that the three-state functionality of the device could be examined.

Transient analysis was carried out using NGSpice to observe the time-domain response of the circuit. Different pulse waveforms were applied to the input terminals, and the resulting output waveforms were analyzed to verify the non-inverting characteristics and proper operation of the enable control circuitry.

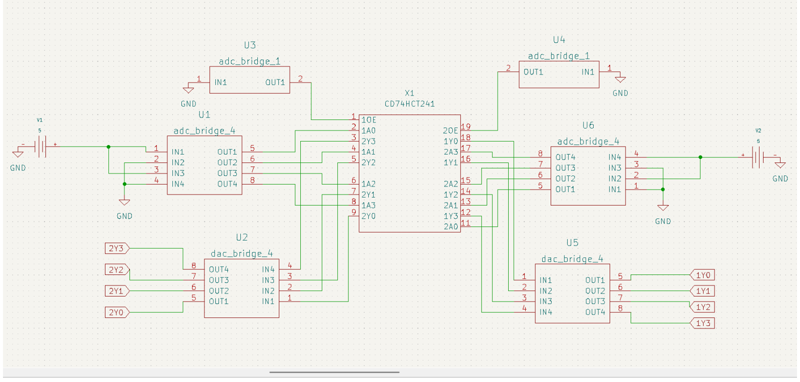


Figure 4.25

4.6.6 Simulation Results

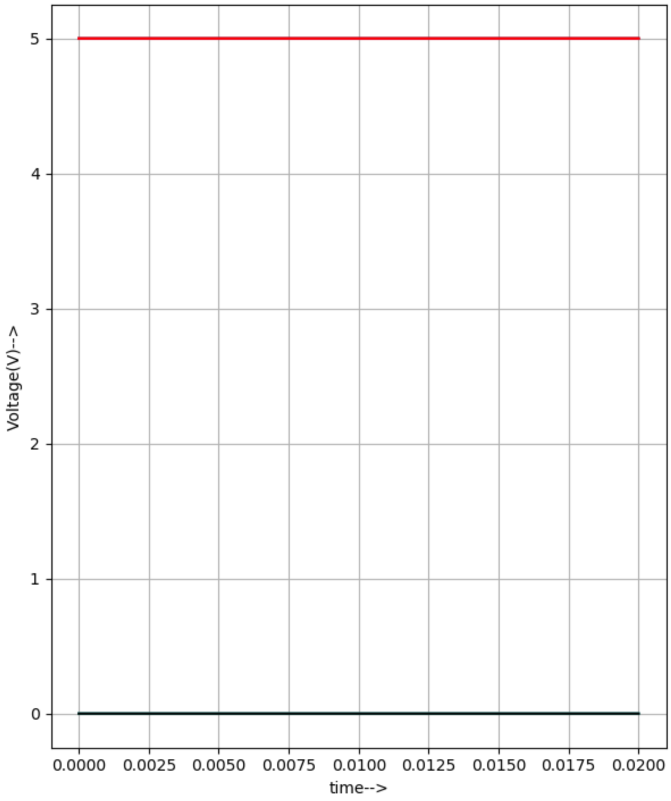
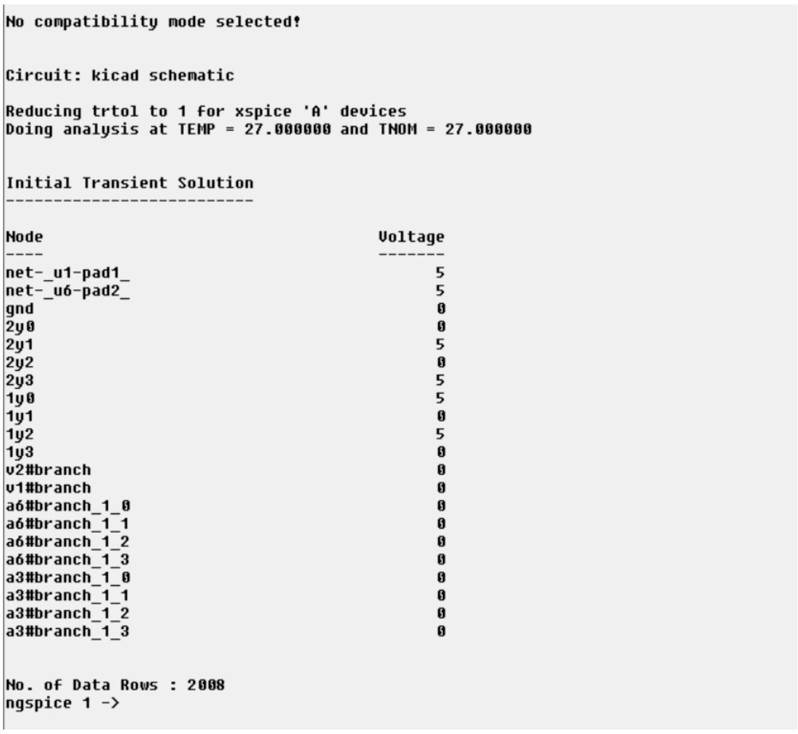


Figure 4.26



```
No compatibility mode selected!


Circuit: kicad schematic

Reducing trtol to 1 for xspice 'A' devices
Doing analysis at TEMP = 27.000000 and TNOM = 27.000000


Initial Transient Solution
--------------------------

Node                                   Voltage
----                                   -------
net-_u1-pad1_                                5
net-_u6-pad2_                                5
gnd                                          0
2y0                                          0
2y1                                          5
2y2                                          0
2y3                                          5
1y0                                          5
1y1                                          0
1y2                                          5
1y3                                          0
v2#branch                                    0
v1#branch                                    0
a6#branch_1_0                                0
a6#branch_1_1                                0
a6#branch_1_2                                0
a6#branch_1_3                                0
a3#branch_1_0                                0
a3#branch_1_1                                0
a3#branch_1_2                                0
a3#branch_1_3                                0


No. of Data Rows : 2008
ngspice 1 ->
```

Figure 4.27

Simulation of the CD74HCT241 was performed using eSim and NGSpice to validate the functionality of the developed model. During the analysis, digital input signals were applied to the buffer inputs while the output enable pins were maintained in the active state. The observed waveforms demonstrated that each output accurately followed its corresponding input, thereby confirming the non-inverting behavior of the device.

Further analysis was conducted by changing the states of the enable inputs. When the enable inputs were asserted HIGH, the outputs entered the high-impedance state as expected. This behavior verified the proper implementation of the three-state output mechanism and demonstrated the suitability of the device for bus-oriented applications.

The simulation results confirmed that the developed subcircuit model successfully reproduces the characteristics of the actual CD74HCT241 integrated circuit. The obtained waveforms and output responses were found to be consistent with the functional specifications provided in the manufacturer's datasheet. Consequently, the model can be reliably utilized in the design and analysis of complex digital systems requiring signal buffering and controlled output isolation.

4.7 CD74HC563 Octal D-Type Transparent Latch with Three-State Outputs

4.7.1 Overview

The CD74HC563 is an octal transparent D-type latch with three-state outputs belonging to the high-speed CMOS logic family. It consists of eight individual D latches sharing a common latch enable input and a common output enable input. The device is capable of storing eight bits of digital data and presenting the stored information at the outputs whenever the output stage is enabled.

The latch enable input, denoted by ($\overline{LE}$), controls the data storage operation. When ($\overline{LE}$) is LOW, the latch operates in transparent mode and the outputs follow the input signals. When ($\overline{LE}$) is HIGH, the data present immediately before the transition is retained and stored internally. The output enable input, denoted by ($\overline{OE}$), controls the tri-state output buffers. When ($\overline{OE}$) is HIGH, all outputs enter the high-impedance state, thereby isolating the device from the external bus.

The CD74HC563 is widely used in digital systems for temporary data storage, bus interfacing, signal synchronization, and memory buffering applications.

4.7.2 Internal Circuit Analysis

Internally, the CD74HC563 consists of eight identical D-type transparent latches connected to a common control network. Each latch receives one data input and stores one bit of information. The latch section is followed by an output stage consisting of tri-state buffers controlled by the output enable signal.

The latch enable signal is internally inverted before being applied to the active-low gate input of each D latch. Consequently, when ($\overline{LE}$) is LOW, the latch becomes transparent and the output follows the input. When ($\overline{LE}$) transitions HIGH, the last logic state present at the input is stored and maintained until the latch is enabled again.

The output section is controlled by the active-low output enable input. When ($\overline{OE}$) is LOW, the stored data is available at the outputs. When ($\overline{OE}$) is HIGH, the outputs are disconnected from the external circuit and enter the high-impedance state. This feature allows several devices to share a common bus without causing contention.

The device therefore performs three important operations:

- Transparent operation when ($\overline{LE} = 0$)
- Data storage when ($\overline{LE} = 1$)
- High-impedance output mode when ($\overline{OE} = 1$)

4.7.3 Subcircuit Implementation

The behavioral model of the CD74HC563 was constructed using eight D-latch elements and eight tri-state output buffers. Each latch receives one of the eight input signals (D_0) to (D_7), while a common latch enable signal controls all storage elements simultaneously.

The outputs of the latch stages are connected to tri-state buffers whose enable terminals are driven by the output enable signal. Since both control inputs are active LOW, the model accurately reproduces the functionality specified in the manufacturer datasheet.

The implementation provides support for the following operating modes:

1. Transparent mode in which the outputs follow the corresponding inputs.
2. Latch mode in which previously stored data is retained even after changes in the input signals.
3. High-impedance mode in which the outputs are electrically isolated from the external circuitry.

The resulting subcircuit accurately reproduces the behavior of the original integrated circuit and can therefore be used in larger digital system simulations.

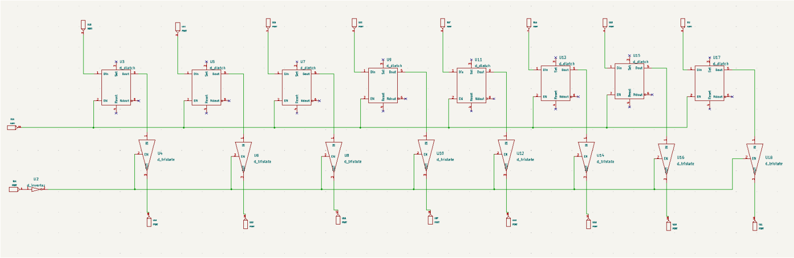


Figure 4.28

4.7.4 Symbol Creation

A custom schematic symbol for the CD74HC563 was developed to facilitate its use within the eSim environment. The symbol contains eight data input pins (($D_0 - D_7$)), eight output pins (($Q_0 - Q_7$)), and two control pins corresponding to the latch enable and output enable signals.

The pin numbering and arrangement were selected according to the device datasheet to ensure compatibility with the implemented subcircuit. The symbol provides a compact and user-friendly representation of the device, thereby simplifying the design and simulation of digital systems employing octal latches.

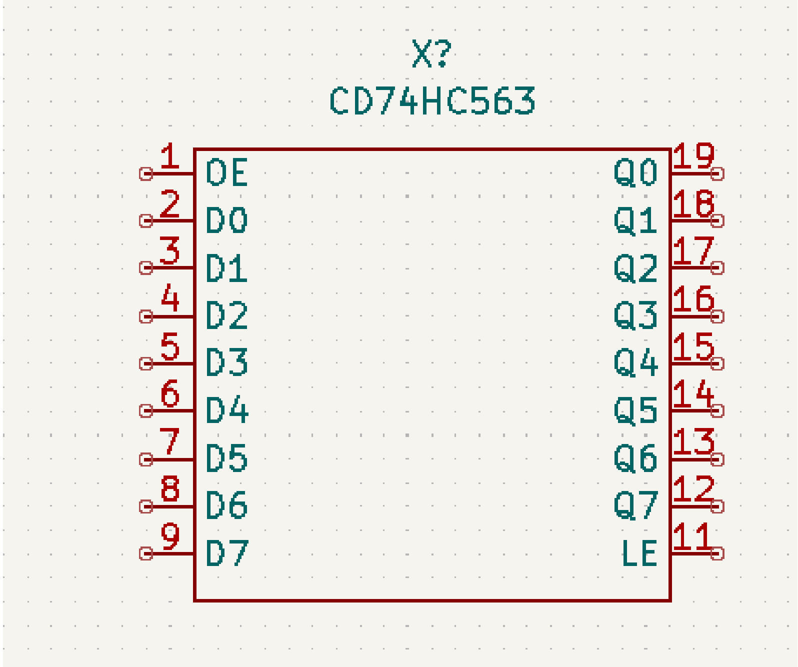


Figure 4.29

4.7.5 Test Circuit

A test circuit was designed to verify the functional correctness of the developed subcircuit. Pulse voltage sources were applied to the data inputs and control signals in order to exercise different operating conditions.

Initially, both ($\overline{LE}$) and ($\overline{OE}$) were maintained LOW, placing the device in transparent mode. Under these conditions, the outputs continuously tracked the corresponding input signals. Subsequently, the latch enable signal was driven HIGH, causing the values present at the inputs to be stored internally. Further changes in the input signals did not affect the outputs, thereby confirming proper latch operation.

Finally, the output enable signal was driven HIGH to place the output buffers in the high-impedance state. This operation verified the correct functioning of the tri-state output stage and demonstrated the suitability of the device for bus-oriented applications.

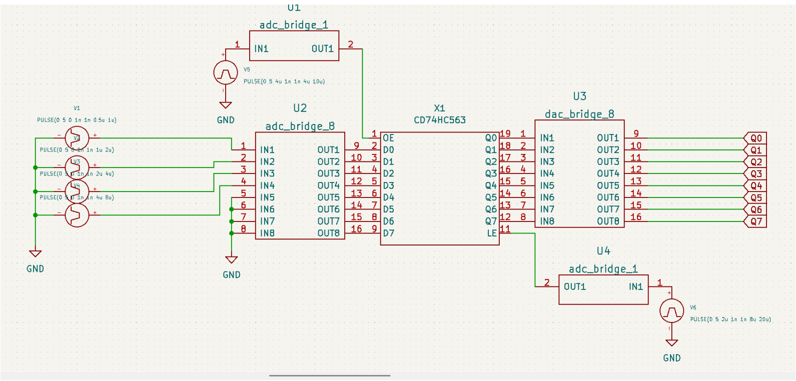

U1
adc_bridge_1
IN1
OUT1
V5
PULSE(0 5 4u 1n 1n 4u 10u)
GND
V1
PULSE(0 5 0 1n 1n 0.5u 1u)
V2
PULSE(0 5 0 1n 1n 1u 2u)
V3
PULSE(0 5 0 1n 1n 2u 4u)
V4
PULSE(0 5 0 1n 1n 4u 8u)
GND
U2
adc_bridge_8
IN1
IN2
IN3
IN4
IN5
IN6
IN7
IN8
OUT1
OUT2
OUT3
OUT4
OUT5
OUT6
OUT7
OUT8
GND
X1
CD74HC563
OE
D0
D1
D2
D3
D4
D5
D6
D7
Q0
Q1
Q2
Q3
Q4
Q5
Q6
Q7
LE
U3
dac_bridge_8
IN1
IN2
IN3
IN4
IN5
IN6
IN7
IN8
OUT1
OUT2
OUT3
OUT4
OUT5
OUT6
OUT7
OUT8
Q0
Q1
Q2
Q3
Q4
Q5
Q6
Q7
U4
adc_bridge_1
OUT1
IN1
V6
PULSE(0 5 2u 1n 1n 8u 20u)
GND

Figure 4.30

4.7.6 Simulation Results

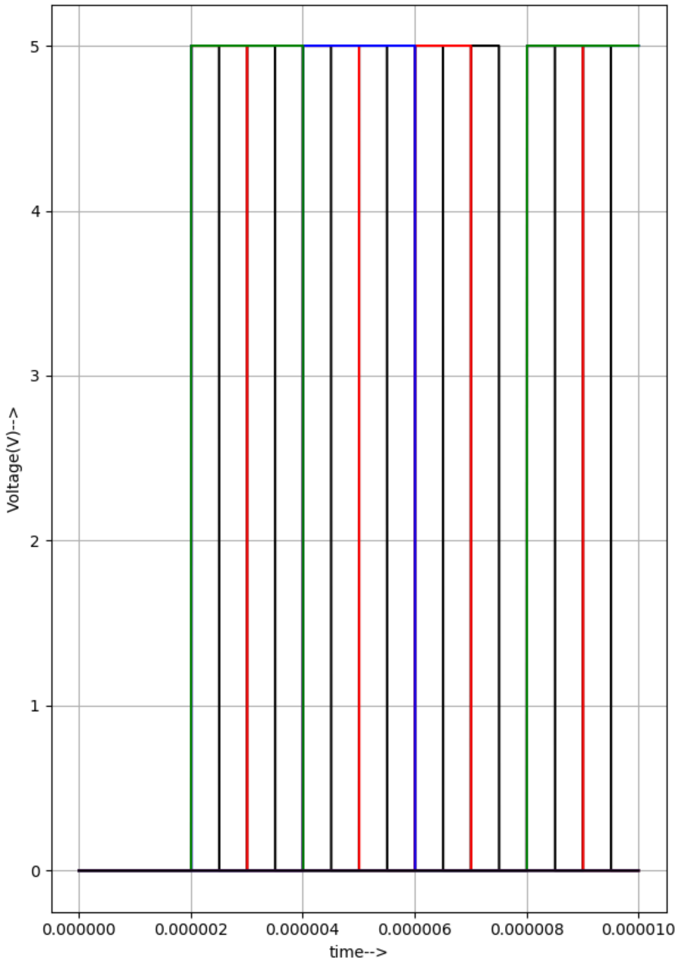


Figure 4.31

Transient analysis was performed to validate the operation of the developed model. The output waveforms confirmed that the circuit behaved in accordance with the expected characteristics of the CD74HC563.

During the interval in which the latch enable signal was LOW, the outputs followed the input waveforms, demonstrating transparent operation. When the latch enable signal transitioned HIGH, the output states remained constant even though the input signals continued to change. This behavior confirmed that the previously sampled data had been successfully stored by the internal latches.

The output enable control further demonstrated the tri-state capability of the device. Upon re-enabling the outputs, the previously stored values reappeared without any loss of information, verifying the integrity of the storage mechanism.

The obtained simulation results closely matched the functional specifications provided in the datasheet, thereby confirming the correctness of the developed behavioral model and validating its suitability for use in digital system simulations.

4.8 LM760 High-Speed Differential Comparator

4.8.1 Overview

The LM760 is a high-speed differential voltage comparator developed by National Semiconductor for applications requiring rapid signal comparison and high sensitivity. The device is designed to operate from symmetrical supply voltages and provides complementary TTL-compatible outputs. Owing to its fast response characteristics, the LM760 finds application in zero-crossing detectors, high-speed analog-to-digital converters, peak detectors, line receivers, and pulse detection circuits.

The comparator operates by continuously comparing two input voltages and producing complementary output states depending upon the polarity of the differential input. Due to its high gain and low propagation delay, the device is capable of detecting very small variations between the input signals. Typical applications include pulse shaping, threshold detection, and signal conditioning in communication and measurement systems.

Internally, the LM760 consists of multiple transistor stages, current mirrors, active loads, biasing networks, and complementary output driver circuits. The architecture enables high-speed operation while maintaining stable and reliable performance over a wide operating range. The equivalent circuit demonstrates the analog design philosophy used in early integrated comparators and highlights the extensive use of transistor-level circuit techniques.

4.8.2 Internal Circuit Analysis

The internal architecture of the LM760 consists of twenty-four bipolar junction transistors, twenty-two resistors, and six diodes interconnected to realize a high-speed differential comparator. The input stage is formed by a differential transistor pair which senses the voltage difference between the two input terminals. This stage provides excellent sensitivity and serves as the primary signal amplification block.

Following the input section, intermediate transistor stages provide voltage amplification and establish the required current distribution within the circuit. Current mirrors and active loads are employed to improve gain and ensure balanced operation. Biasing networks composed of resistors and diode-connected elements maintain proper operating conditions for the various transistor stages.

The output section contains complementary transistor arrangements that provide two output terminals, namely OUT1 and OUT2. These outputs exhibit complementary characteristics, allowing the device to be employed in high-speed switching and signal detection applications. The transistor arrangement also enhances the driving capability and contributes to the overall response speed of the comparator.

The equivalent circuit illustrates the complexity involved in analog integrated circuit design, where numerous transistors cooperate to achieve high gain, stability, and rapid switching performance. The LM760 represents an excellent example of transistor-level implementation of a precision analog comparator.

4.8.3 Subcircuit Implementation

The LM760 equivalent circuit was implemented in eSim using the transistor-level schematic provided in the National Semiconductor datasheet. Individual NPN and PNP transistor models were utilized to recreate the internal architecture of the device. The implementation included all transistor stages, resistive networks, and diode structures present in the equivalent circuit.

Special attention was given to preserving the interconnections between the input differential stage, intermediate amplification stage, current mirror section, and output driver circuits. The resistor values and diode arrangements were incorporated according to the equivalent circuit specifications in order to maintain the intended bias conditions and signal flow.

The resulting subcircuit successfully reproduced the structural organization of the original LM760 comparator and enabled detailed analysis of the internal operation. Through the use of hierarchical design techniques, the complex transistor network was organized into a single reusable component suitable for simulation and testing.

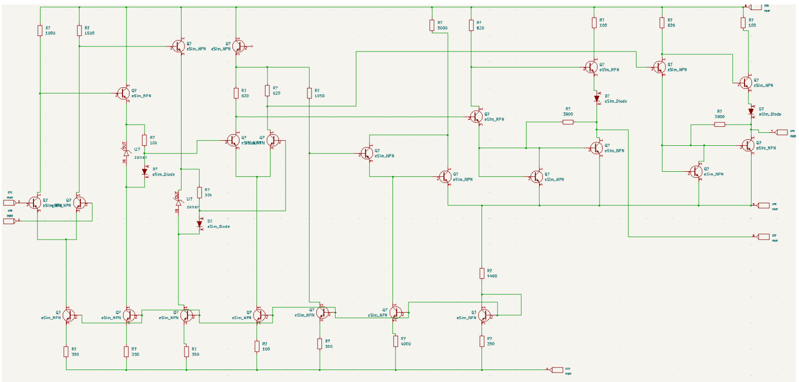


Figure 4.32

4.8.4 Symbol Creation

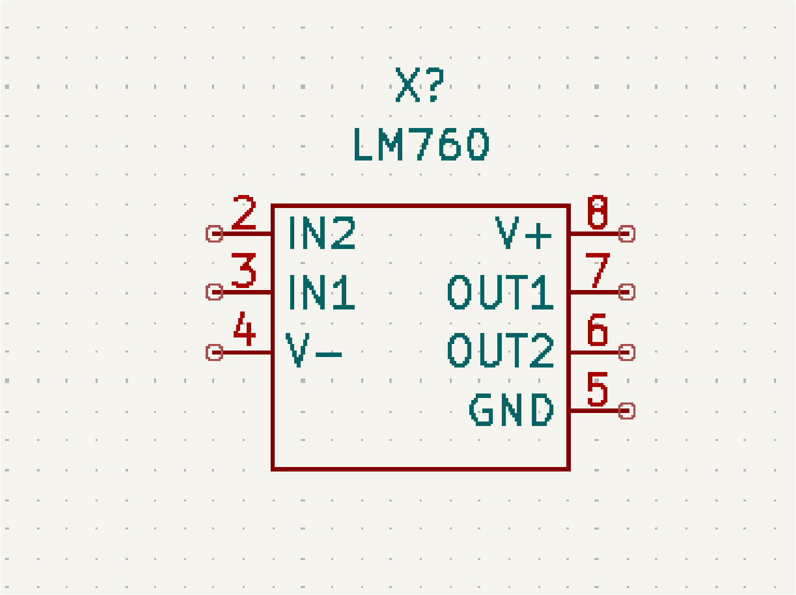


Figure 4.33

After successful implementation of the transistor-level subcircuit, a custom symbol for the LM760 was created to facilitate its use in higher-level circuit designs. The symbol was designed to represent the functional behavior of the comparator while providing a simplified interface to the user.

The symbol consists of seven terminals corresponding to the input, output, and power connections of the device. These terminals include IN1, IN2, V+, V-, GND, OUT1, and OUT2. The arrangement of pins was chosen to resemble the standard package configuration and to simplify circuit construction.

The creation of the custom symbol enabled the complex internal transistor network to be encapsulated within a single functional block. This approach improves readability, simplifies schematic development, and allows the device to be reused conveniently in different applications.

4.8.5 Test Circuit

To verify the operation of the implemented comparator, a transient analysis test circuit was constructed. A pulse waveform was applied to input terminal IN1, while the second input terminal IN2 was maintained at a reference potential. Appropriate supply voltages were provided through the V+, V-, and GND terminals.

The test configuration was selected to evaluate the response of the comparator to changing input conditions. The pulse source generated alternating voltage levels which produced differential input signals at the comparator terminals. Observation of the output waveforms enabled analysis of the switching characteristics and dynamic behavior of the circuit.

Transient simulations were carried out using suitable time-step and stop-time parameters to capture the fast response characteristics of the comparator. The complementary outputs were monitored throughout the simulation interval in order to study the signal transitions and verify the operation of the implemented architecture.

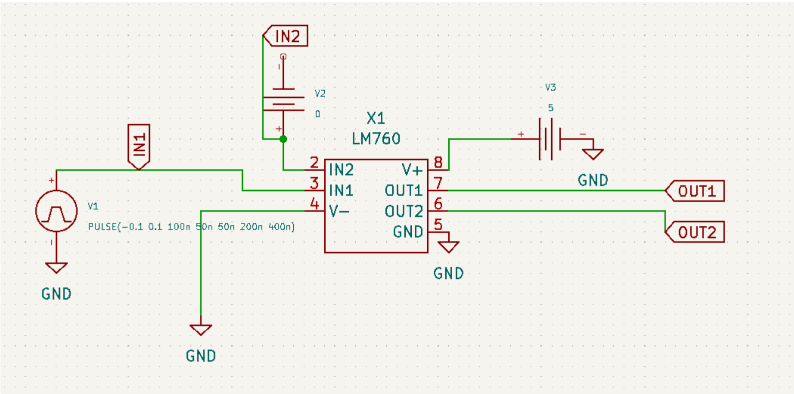


Figure 4.34

4.8.6 Simulation Results

Transient analysis of the implemented LM760 comparator demonstrated the expected dynamic response of the circuit under varying input conditions. The input pulse waveform produced corresponding changes within the internal transistor stages, resulting in observable output transitions at the complementary output terminals.

The simulated waveforms indicated proper propagation of signals through the differential amplifier stage and subsequent output driver circuitry. The outputs exhibited complementary behavior and responded consistently to changes in the input voltage, confirming the successful operation of the comparator structure.

Minor variations in output levels and waveform characteristics were observed due to the practical limitations associated with transistor-level modeling and the use of generalized device parameters. Nevertheless, the simulation results verified the functionality of the implemented equivalent circuit and demonstrated the ability of the LM760 architecture to perform high-speed differential voltage comparison.

Overall, the transistor-level realization successfully reproduced the essential operating characteristics of the LM760 high-speed differential comparator. The project provided valuable insight into analog integrated circuit design and illustrated the interaction between differential amplifier stages, current mirrors, and complementary output structures in achieving fast and reliable comparator performance.

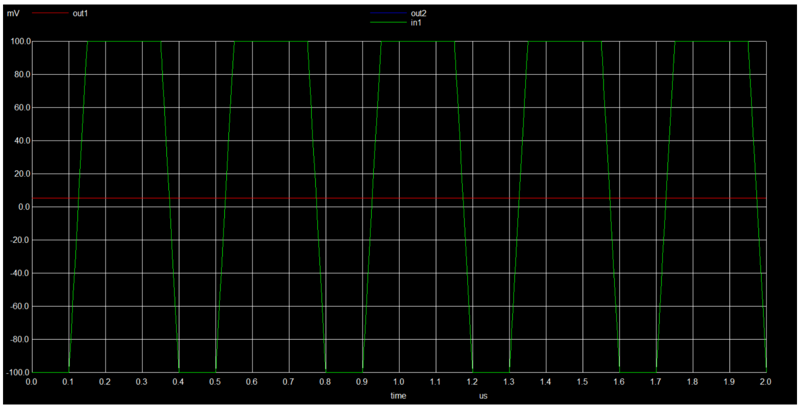


Figure 4.35

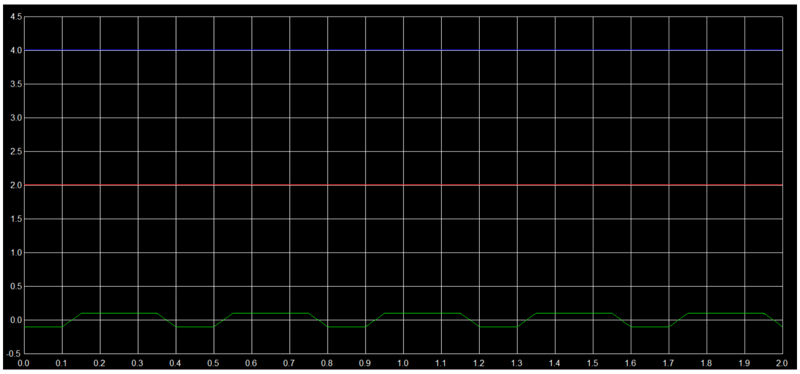


Figure 4.36

4.9 SN74HC623 Octal Bus Transceiver

4.9.1 Overview

The SN74HC623 is an octal bidirectional bus transceiver designed for high-speed data communication between two separate buses. It consists of eight identical transceiver channels that provide bidirectional data transfer with three-state outputs. The device is fabricated using high-speed CMOS technology and is compatible with standard CMOS and TTL logic levels. The three-state outputs allow multiple devices to share a common bus without causing contention when the outputs are disabled.

Unlike ordinary buffers, the SN74HC623 permits data transfer in both directions. The A and B terminals are bidirectional ports and neither side is permanently assigned as an input or output. The direction of data transfer is controlled by two independent active-low output enable inputs, namely OEAB and OEBA. By appropriately controlling these enable signals, information can be transferred from the A bus to the B bus or from the B bus to the A bus.

The device contains eight identical transceiver sections, making it suitable for interfacing microprocessors, memory devices, communication systems, and parallel data buses. Its low power consumption and high noise immunity make it suitable for modern digital systems where reliable data transfer is required.

4.9.2 Internal Circuit Analysis

The SN74HC623 consists of eight identical bidirectional transceiver stages. Each stage contains two non-inverting tri-state buffers connected in opposite directions. One buffer transfers information from the A side to the B side, while the second buffer transfers information from the B side to the A side. The outputs of these buffers are controlled by active-low enable inputs.

When OEAB is asserted low, the A-to-B transmission path becomes active and the corresponding signal appearing at terminal A is transferred to terminal B. Simultaneously, the B-to-A transmission path remains disabled. Similarly, when OEBA is asserted low, data is transferred from the B side to the A side while the opposite direction remains disabled.

Since the outputs are tri-state, both transmission paths can be disabled by keeping both enable inputs inactive. In this condition, the outputs enter a high-impedance state, thereby electrically isolating the buses. This feature allows multiple devices to share the same communication lines.

Internally, the complete integrated circuit contains eight identical channels, designated as A1-B1 through A8-B8. All channels share common control signals while operating independently with respect to the transmitted data. This architecture enables simultaneous transfer of eight bits of information and significantly improves data throughput in digital systems.

The use of CMOS technology provides high switching speed, low static power dissipation, and excellent noise immunity. Consequently, the device can be employed in a wide range of digital applications requiring efficient bus interfacing.

4.9.3 Subcircuit Implementation

To model the operation of the SN74HC623 in eSim, a hierarchical subcircuit approach was adopted. The complete IC was constructed by replicating the internal transceiver stage eight times. Each stage was composed of two tri-state buffers connected in opposite directions to achieve bidirectional signal flow.

For every channel, one tri-state buffer was responsible for transferring data from terminal A to terminal B, whereas another tri-state buffer transferred data from terminal B to terminal A. These buffers were controlled using the OEAB and OEBA inputs, thereby reproducing the actual operating principle of the integrated circuit.

The channels A1-B1, A2-B2, A3-B3, A4-B4, A5-B5, A6-B6, A7-B7, and A8-B8 were implemented in an identical manner. Since all channels possess identical characteristics, the complete octal transceiver could be realized by repeating the same internal structure eight times.

The hierarchical implementation simplified circuit construction and provided a close representation of the functional behavior of the original integrated circuit. Such modular construction also improves readability and facilitates future modifications or debugging.

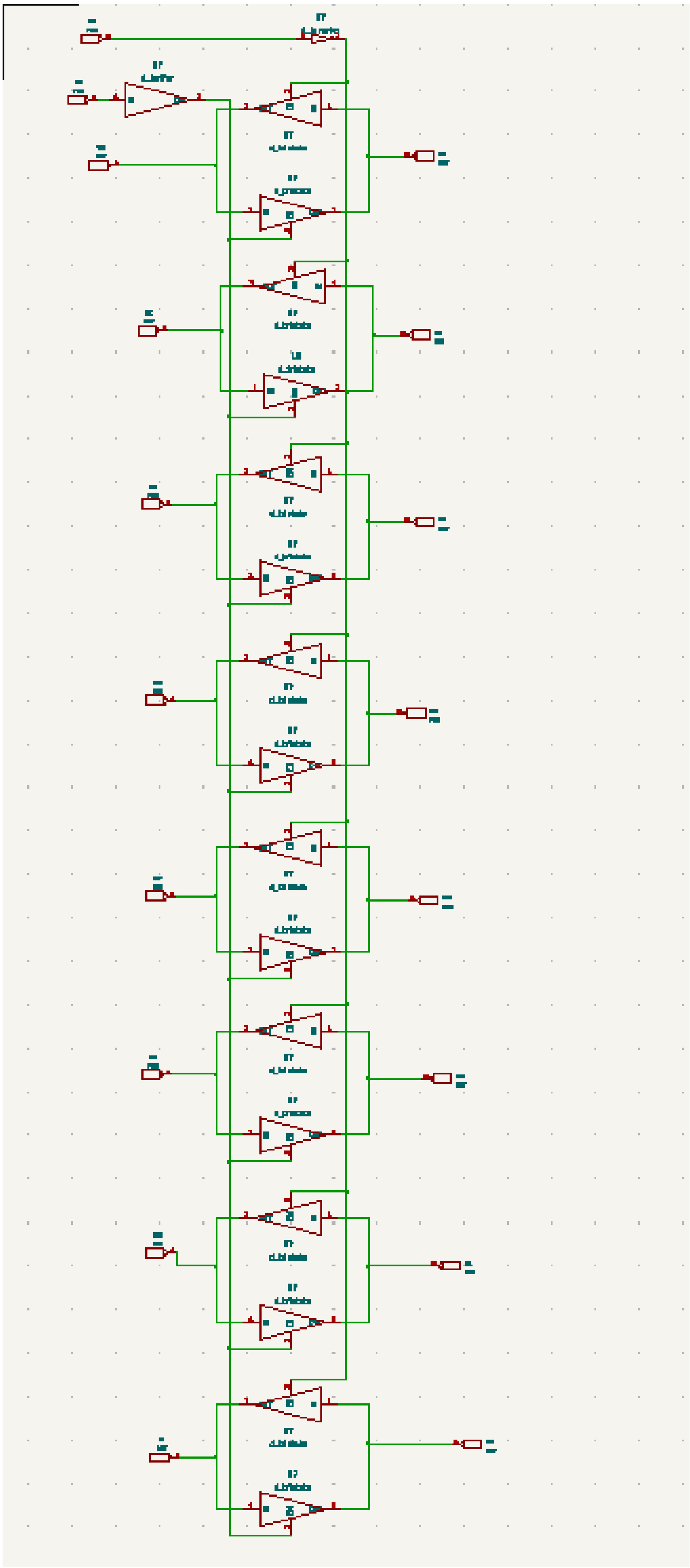


Figure 4.37

4.9.4 Symbol Creation

A custom schematic symbol for the SN74HC623 was created in KiCad to provide a convenient interface for circuit design and simulation. The symbol was designed according to the standard 20-pin package configuration of the device.

Pin 1 was assigned to OEAB, while pin 19 was assigned to OEBA. Pins A1 through A8 were placed on the left side of the symbol, and pins B1 through B8 were placed on the right side. Since these terminals can act as both inputs and outputs depending on the selected direction of data transfer, they were assigned the bidirectional pin type.

The enable pins OEAB and OEBA were assigned as input pins because they control the operating mode of the transceiver. Power and ground connections were incorporated as hidden power pins to maintain a clean and organized symbol appearance.

Proper classification of the pin types ensured accurate electrical rule checking and improved the usability of the symbol during schematic design. The resulting symbol closely resembles the manufacturer's pin configuration and provides an intuitive representation of the device.

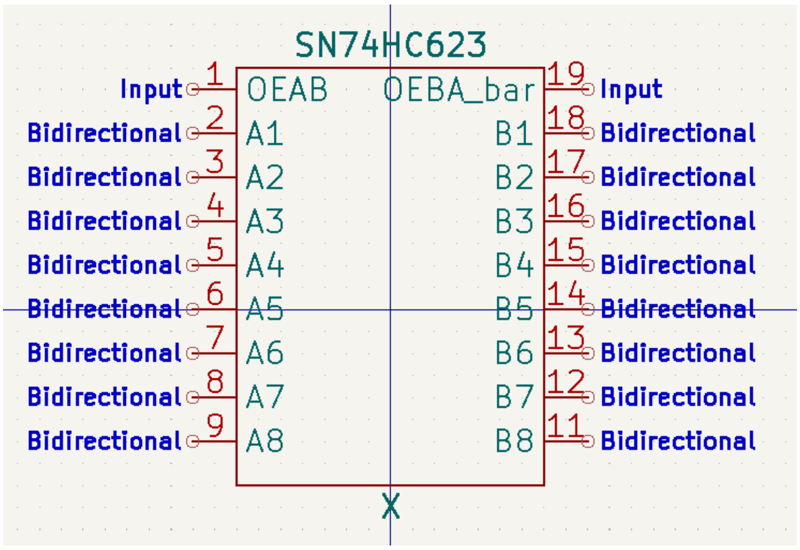


Figure 4.38

4.9.5 Test Circuit

A test circuit was developed to verify the functionality of the implemented SN74HC623 model. For simplicity, only one transceiver channel was utilized during simulation. The A1 terminal was selected as the input node, while B1 served as the output node.

The output enable input OEAB was connected to logic low, thereby enabling the A-to-B transmission path. Simultaneously, OEBA was maintained at logic high so that the B-to-A transmission path remained disabled. Under these conditions, the device operates as a non-inverting buffer transferring data from A1 to B1.

A pulse voltage source with an amplitude varying between 0 V and 5 V was connected to the A1 terminal. The pulse signal used for simulation had a rise time and fall time of 1 ns, pulse width of 5 μs, and a period of 10 μs. A transient analysis was carried out over a duration of 50 μs with a simulation step size of 100 ns.

The waveforms at terminals A1 and B1 were observed using the waveform viewer. To improve visualization, the output waveform corresponding to B1 was vertically shifted by 6 V so that both signals could be compared without overlap.

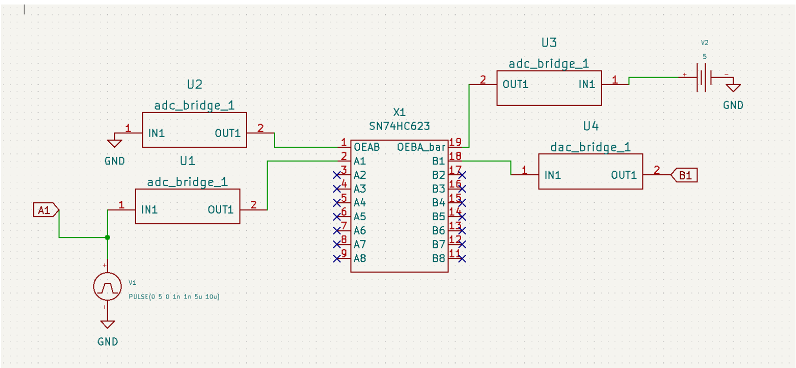


Figure 4.39

4.9.6 Simulation Results

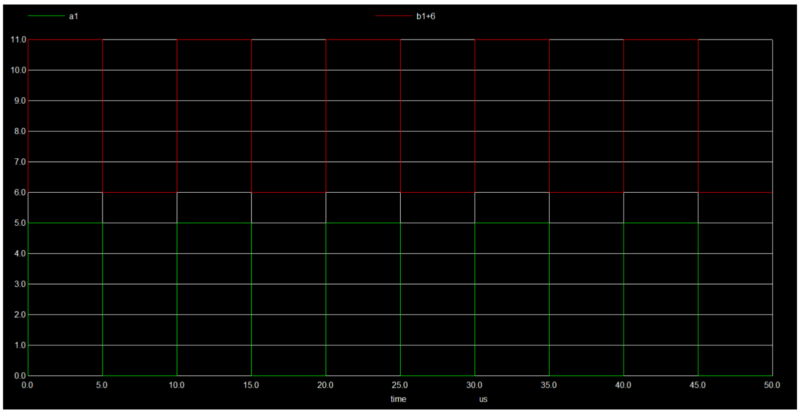


Figure 4.40

Transient simulation confirmed the correct operation of the SN74HC623 subcircuit. The waveform obtained at terminal B1 was found to be identical to the pulse signal applied at terminal A1. The output reproduced the input signal without distortion, exhibiting identical amplitude, frequency, and pulse width characteristics.

The rising and falling transitions of both signals occurred simultaneously, indicating negligible propagation delay within the digital model. In the waveform display, the B1 output signal was shifted vertically by 6 V to distinguish it from the input waveform. Despite this offset, both signals possessed identical timing characteristics and demonstrated complete correspondence.

The simulation results verify that the implemented subcircuit accurately reproduces the behavior of the SN74HC623 octal bus transceiver. Successful signal transfer from A1 to B1 confirms the correctness of the internal architecture, enable control arrangement, and custom symbol implementation. Consequently, the developed model can be employed reliably in larger digital systems requiring bidirectional bus communication and three-state operation.

Chapter 5

Conclusion and Future Scope

The work carried out during this internship focused on the study, implementation, and verification of various analog and digital integrated circuits within the eSim environment. Through the development of circuit models and simulation-based validation, valuable contributions were made towards expanding the capabilities of the eSim library. The activities undertaken provided practical exposure to circuit modeling, device analysis, and the use of open-source Electronic Design Automation (EDA) tools.

These IC models serve as essential building blocks for designing and simulating complex electronic systems, making them valuable resources for students, educators, and researchers using eSim. By integrating verified models into the eSim library and studying the behavior of additional devices, the work has contributed to strengthening the platform's ability to support practical circuit design and experimentation.

This initiative not only reinforces the importance of open-source EDA tools in academic and research settings but also lays the foundation for future developments. As the eSim device model library continues to expand, it is expected to encourage wider adoption among the engineering community and facilitate the development of increasingly sophisticated circuits. The outcomes of this work therefore represent a meaningful contribution towards strengthening the ecosystem of accessible and open-source circuit simulation tools.

Bibliography

[1] eSim Documentation, FOSSEE Project, Indian Institute of Technology Bombay. https://esim.fossee.in/

[2] Texas Instruments, ”CD4585B CMOS 4-Bit Magnitude Comparator Datasheet”. https://www.ti.com/lit/ds/symlink/cd4585b.pdf

[3] Texas Instruments, ”SN74HC03 Quad 2-Input NAND Gates with Open-Drain Outputs Datasheet”. https://www.ti.com/lit/ds/symlink/sn74hc03.pdf

[4] Texas Instruments, ”CD4073B CMOS Triple 3-Input AND Gate Datasheet”. https://www.ti.com/lit/ds/symlink/cd4073b.pdf

[5] Texas Instruments, ”SN75452B Dual Peripheral Drivers Datasheet”. https://www.ti.com/lit/ds/symlink/sn75452b.pdf

[6] Analog Devices, ”AD623 Low Cost Instrumentation Amplifier Datasheet”. https://www.analog.com/media/en/technical-documentation/data-sheets/ad623.pdf

[7] Texas Instruments, ”OPT101 Monolithic Photodiode and Single-Supply Transimpedance Amplifier Datasheet”. https://www.ti.com/lit/ds/symlink/opt101.pdf

[8] Ngspice User’s Manual. https://ngspice.sourceforge.io/docs.html

[9] KiCad Documentation. https://docs.kicad.org/

[10] FOSSEE Project, Indian Institute of Technology Bombay. https://fossee.in/