Semester-Long Internship Autumn 2025

On

Designing Integrated Circuit in eSim

Submitted by

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Under the guidance of

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Acknowledgment

I would like to express my deepest gratitude to Prof. Prabhu Ramachandran for providing me the opportunity to be a part of the FOSSEE internship program and for supporting open-source engineering tool development at IIT Bombay. His guidance and vision have encouraged students and researchers to actively contribute to the open-source ecosystem.

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My sincere appreciation extends to my mentor, Mr. Sumanto Kar, for his continual support, technical guidance, and encouragement throughout the duration of this project. His insights and feedback played a key role in refining ideas, overcoming challenges, and ensuring timely completion of the tasks assigned to me.

I would also like to thank my internal mentors, Mr. Varad Patil, Ms. Shanthi Priya K, for their valuable guidance, coordination, and technical inputs during the internship. Their mentorship contributed significantly to the clarity, progress, and successful execution of the work.

This internship has been an enriching learning experience, allowing me to work closely with open-source EDA tools, develop IC subcircuits in eSim, and gain exposure to real-world circuit modeling and simulation workflows. The knowledge acquired during this period will undoubtedly support my future academic and professional pursuits.

I would also like to thank the entire FOSSEE team for their coordination, assistance, and timely interactions at various stages of this work. Their collective efforts ensured smooth workflow, resource accessibility, and effective project execution.

Contents

Chapter 1

Introduction

FOSSEE (Free/Libre and Open Source Software for Education) project promotes the use of FLOSS tools to improve the quality of education in our country. It aims to reduce dependency on proprietary software in educational institutions. It encourages the use of FLOSS tools through various activities to ensure commercial software is replaced by equivalent FLOSS tools. It also develops new FLOSS tools and upgrade existing tools to meet requirements in academia and research.

The FOSSEE project is part of the National Mission on Education through Information and Communication Technology (ICT), Ministry of Human Resource Development (MHRD), Government of India.

1.1 eSim

eSim is a CAD tool that helps electronic system designers to design, test, and analyze their circuits. The important feature of this tool is that it is open source, allowing users to modify the source as per their needs. The software provides a generic, modular, and extensible platform for experimenting with electronic circuits. eSim is built using various free/libre and open-source software components including:

1.1.1 Kicad

Integrated software where all functions of circuit drawing, control, layout, library management, and access to the PCB design software are carried out.

1.1.2 Ngspice

Ngspice is a general-purpose circuit simulation program for nonlinear dc, nonlinear transient, and linear ac analysis.

1.1.3 KiCad to Ngspice converter

Analysis parameters, source details are provided through this module. It allows us to add and edit the device models and subcircuits included in the circuit schematic.

1.1.4 Subcircuit Builder

This module allows the user to create a subcircuit for a component. Once the subcircuit for a component is created, the user can use it in other circuits.

1.1.5 NGHDL

A module for mixed signal circuit simulation, is also integrated with eSim. It makes use of VHDL code.

1.1.6 NgVeri

NgVeri, a module for mixed signal circuit simulation, is also integrated with eSim. It makes use of Verilog/System Verilog/Transaction-Level Verilog code.

1.1.7 Makerchip

Makerchip is a cloud-based browser application developed by Redwood EDA to do digital circuit design. One can simulate Verilog/SystemVerilog/Transaction-Level Verilog code in Makerchip.

Chapter 2

Abstract

The objective of this internship was to design and develop various integrated circuits using the Subcircuit Builder Method in eSim. This involved modeling the ICs with eSim library files and subsequently simulating them with different circuits. The goal was to expand the eSim Subcircuit Library for future use, enhancing its utility and application in educational and practical scenarios.

2.1 Approach

- Identify and research an integrated circuit (IC) that is not currently available in the eSim library.
- Obtain and study the datasheet of the selected IC thoroughly.
- Carefully examine the schematic provided in the datasheet.
- Accurately recreate the schematic in eSim using the Subcircuit Builder Method.
- Model the IC in eSim, ensuring all parameters and configurations match those in the datasheet.
- Simulate the integrated circuit within eSim, testing it with various circuits to verify its functionality.
- Document the process and results to contribute to the future use and expansion of the eSim Subcircuit Library.

Chapter 3

Integrated Circuit Design

3.1 74HCT540

3.1.1 Description

The 74HC/HCT540 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A. The 74HC/HCT540 are octal inverting buffer/line drivers with 3-state outputs. The 3-state outputs are controlled by the output enable inputs OE1 and OE2. A HIGH on OEn causes the outputs to assume a high impedance OFF-state.

Features Of 74HCT540

- **Operating Voltage Range:** Supports a wide supply voltage (V_{CC}) range, typically from 2.0V to 6.0V.
- **Low Power Consumption:** Being a CMOS device, it draws very little quiescent current of 80 μA maximum at room temperature.
- **High Noise Immunity:** Inherits the standard CMOS characteristic of high noise margin.
- **Drive Capability:** Capable of driving up to 15 standard LS-TTL loads.

3.1.2 Pin Diagram

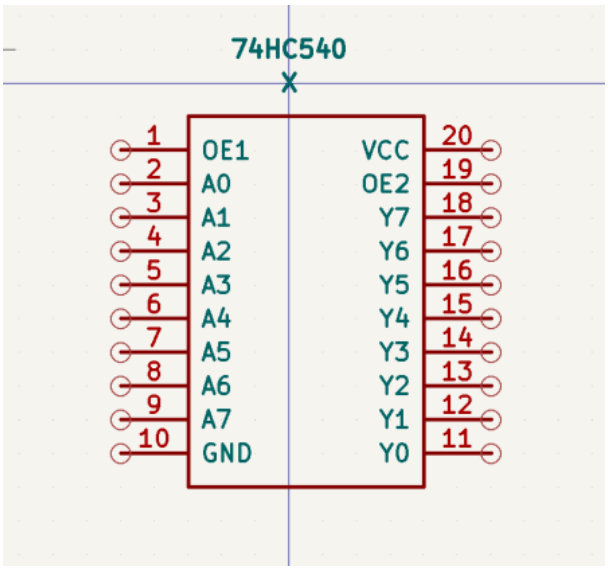

Figure 3.1: Pin Diagram of 74HCT540

3.1.3 Sub-Circuit Diagram

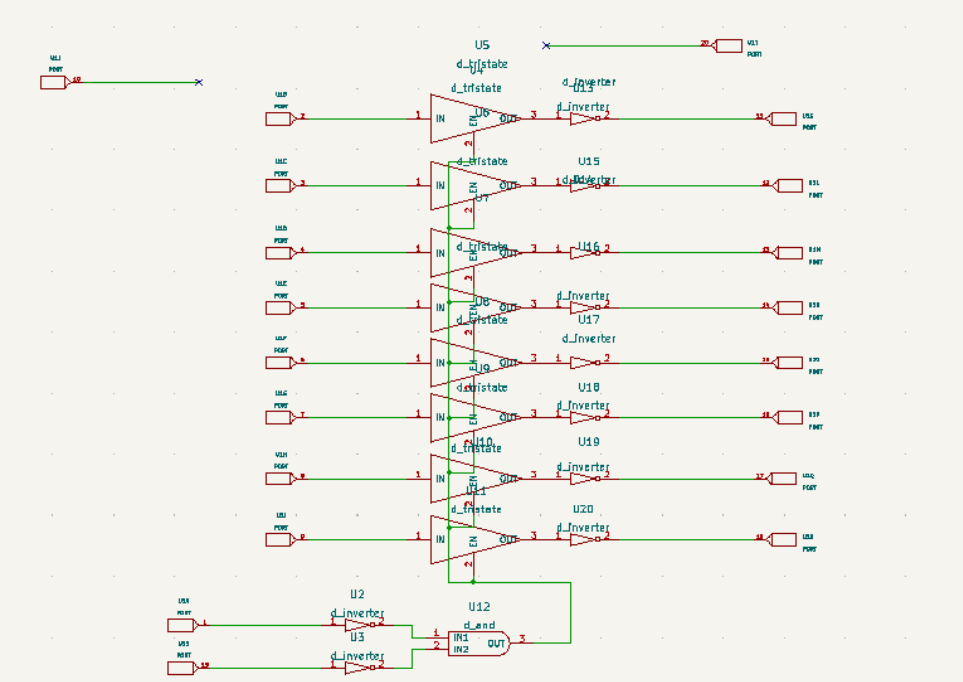

Figure 3.2: Sub-Circuit of 74HCT540

3.1.4 Test-Circuit Diagram

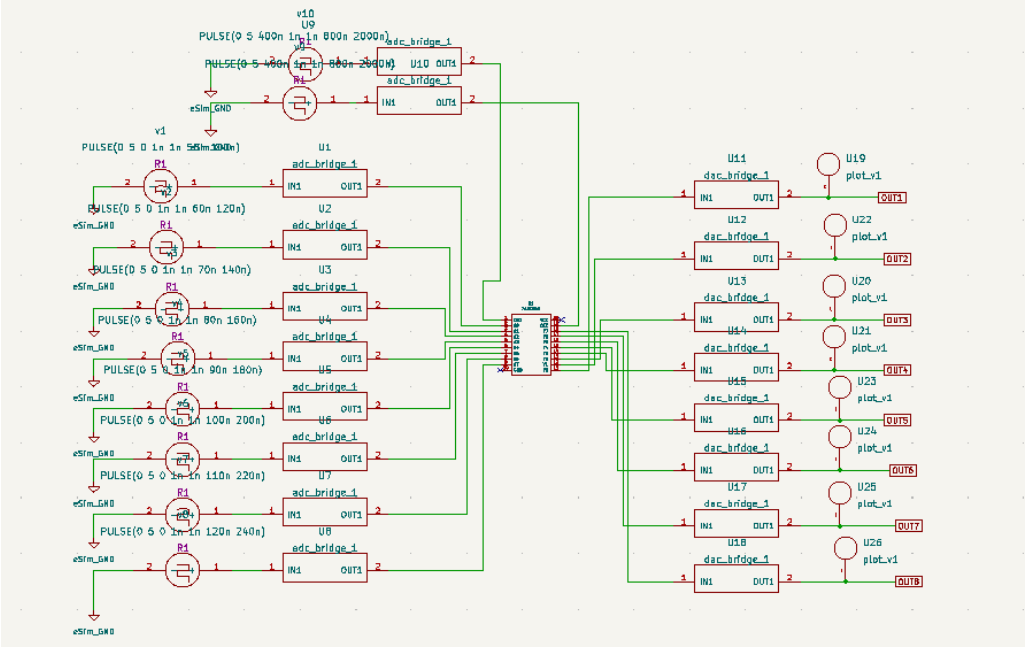

Figure 3.3: Test Circuit of 74HCT540

3.1.5 NgSpice Plot

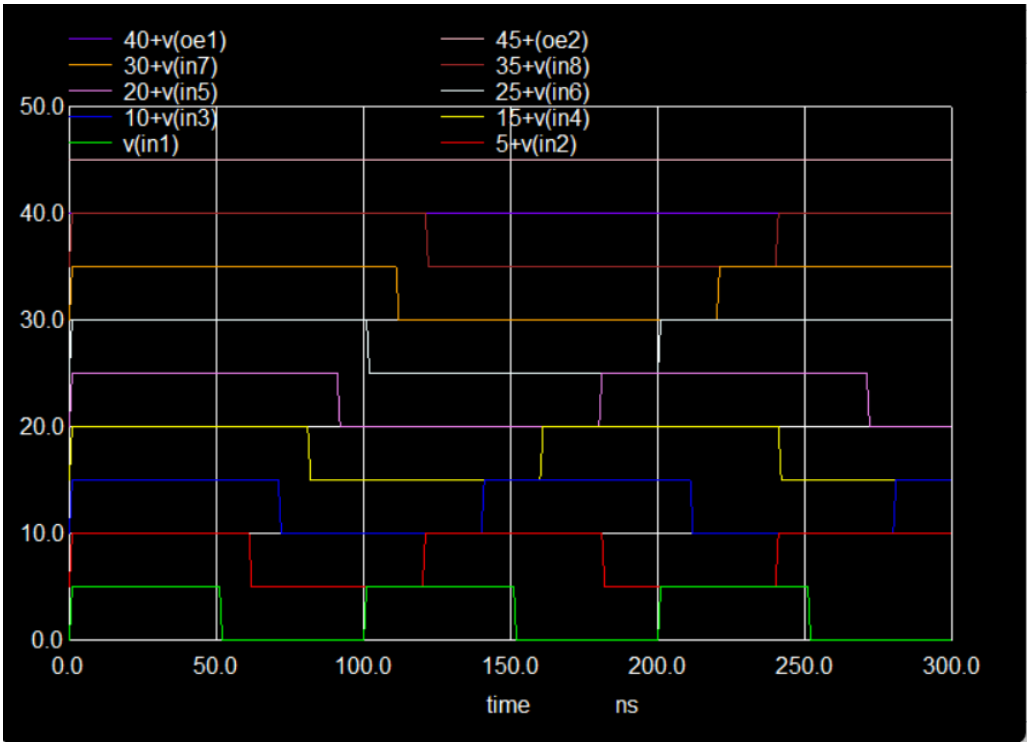

Figure 3.4: Input Graph of 74HCT540

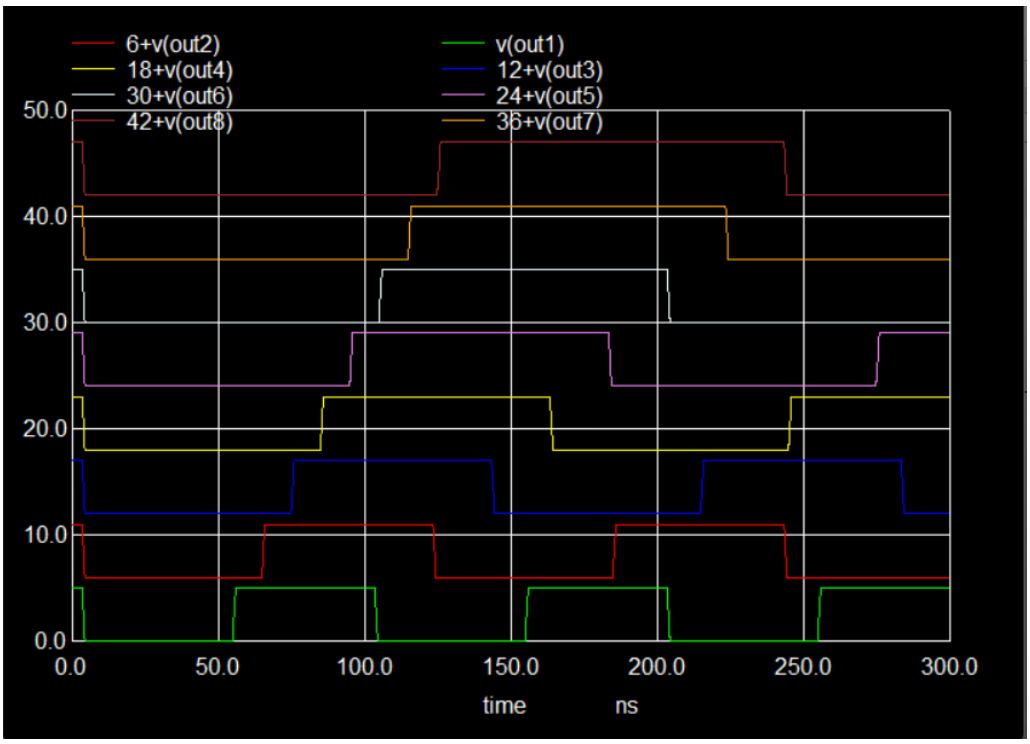

Figure 3.5: Output Graph of 74HCT540

3.2 SN74HC138

3.2.1 Description

The SN74HC138 devices are designed to be used in high-performance memory-decoding or data-routing applications requiring very short propagation delay times. In high-performance memory systems, these decoders can be used to minimize the effects of system decoding. When employed with high-speed memories utilizing a fast enable circuit, the delay times of these decoders and the enable time of the memory are usually less than the typical access time of the memory. This means that the effective system delay introduced by the decoders is negligible.

Features Of SN74HC138

- **Active-Low Outputs:** The outputs are inverted. When an output is selected by the input binary code, that specific output goes LOW, while the other seven unselected outputs remain HIGH.
- **Operating Voltage Range:** Like most chips in the 74HC family, it supports a wide supply voltage range, typically from 2.0V to 6.0V.
- **Low Power Consumption:** It utilizes CMOS technology, resulting in very low static power dissipation compared to older TTL logic families.

3.2.2 Pin Diagram

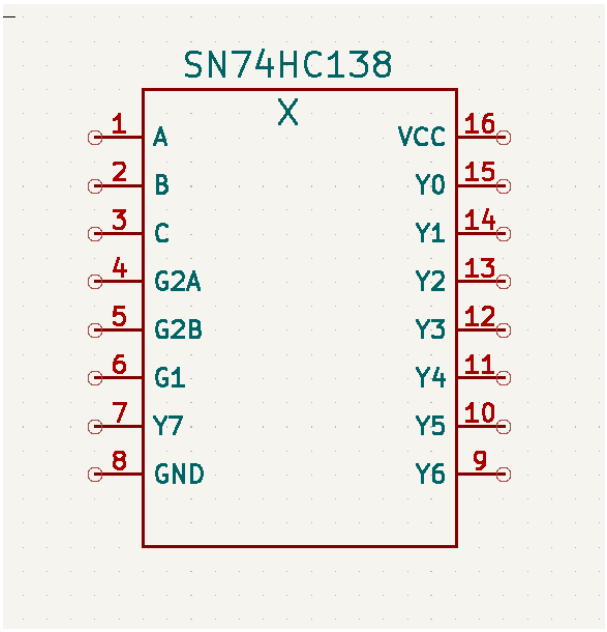

Figure 3.6: Pin Diagram of SN74HC138

3.2.3 Sub-Circuit Diagram

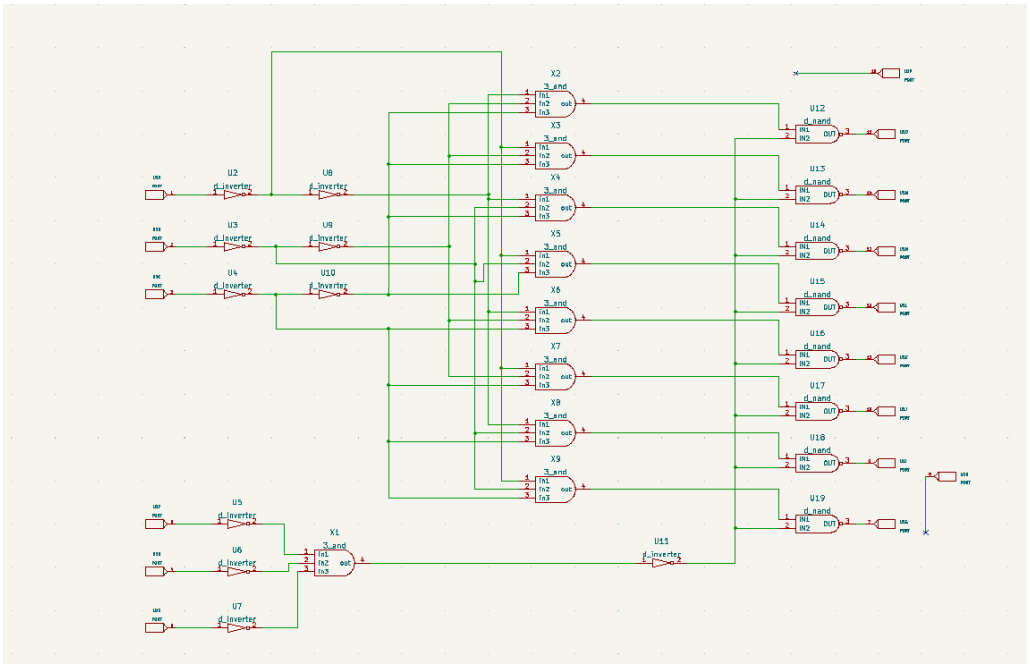

Figure 3.7: Sub-Circuit of SN74HC138

3.2.4 Test-Circuit Diagram

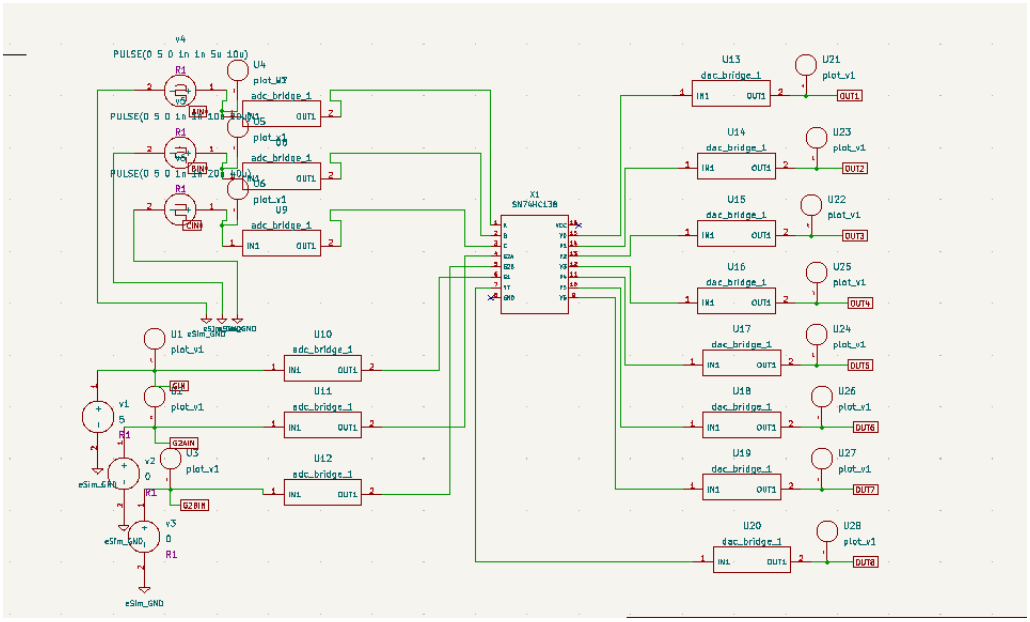

Figure 3.8: Test Circuit of SN74HC138

3.2.5 NgSpice Plot

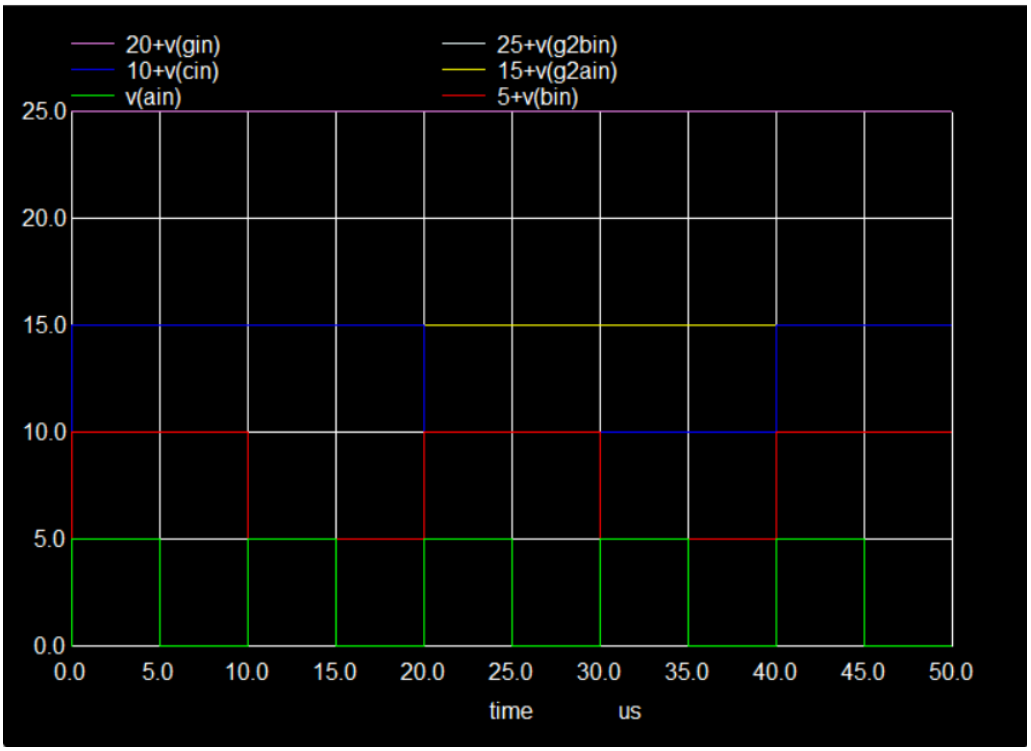

Figure 3.9: Input Graph of SN74HC138

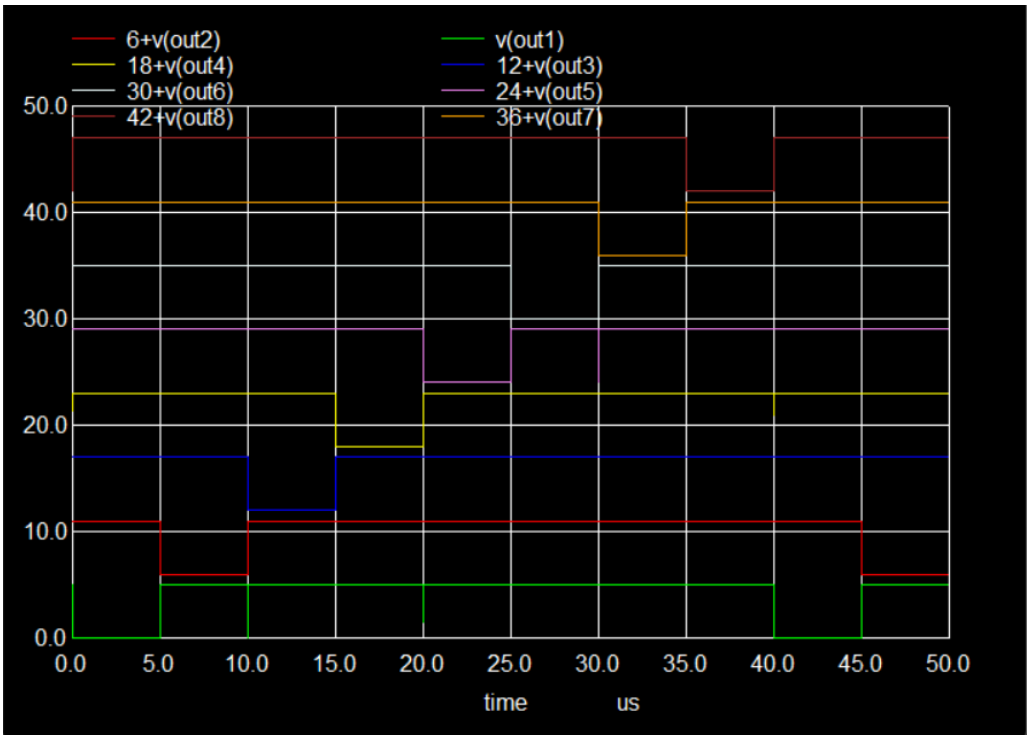

Figure 3.10: Output Graph of SN74HC138

3.3 IN74LV574

3.3.1 Description

The 74LV574 is an octal D-type flip-flop featuring separate D-type inputs for each flip-flop and non-inverting 3-state outputs for oriented applications. A clock (CP) and an output enable (OE) input are common to all flip-flops. The eight flip-flops will store the state of their individual D-inputs that meet the set-up and hold times requirements on the LOW-to-HIGH CP transition. When OE is LOW, the contents of the eight flip-flops are available at the outputs. When OE is HIGH, the outputs go to the high impedance OFF-state. Operation of the OE input does not affect the state of the flip-flops.

Features Of IN74LV574

- **8-Bit Storage:** Contains eight individual D-type flip-flops that share a common clock and output enable.
- **Positive Edge-Triggered:** Data on the D inputs is latched and stored in the flip-flops on the LOW-to-HIGH transition of the clock pulse (CP).
- **3-State Outputs:** The non-inverting Q outputs can be placed in a high-impedance (High-Z) OFF-state. This prevents bus contention, making the IC ideal for implementing buffer registers, bidirectional bus drivers, and I/O ports.

3.3.2 Pin Diagram

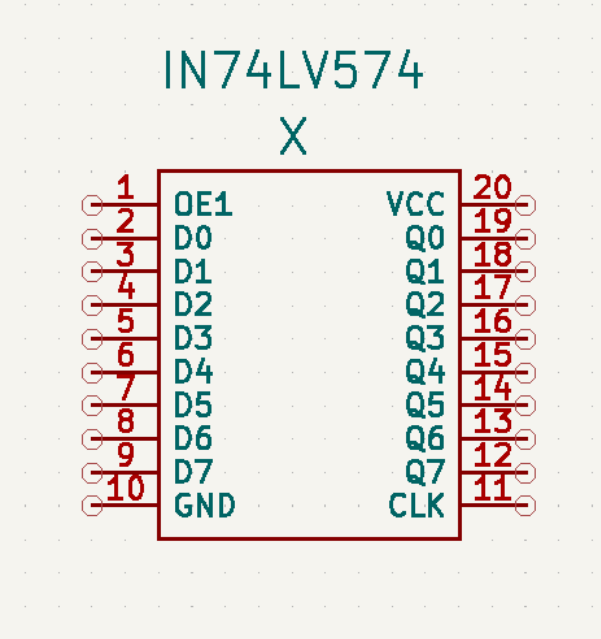

Figure 3.11: Pin Diagram of IN74LV574

3.3.3 Sub-Circuit Diagram

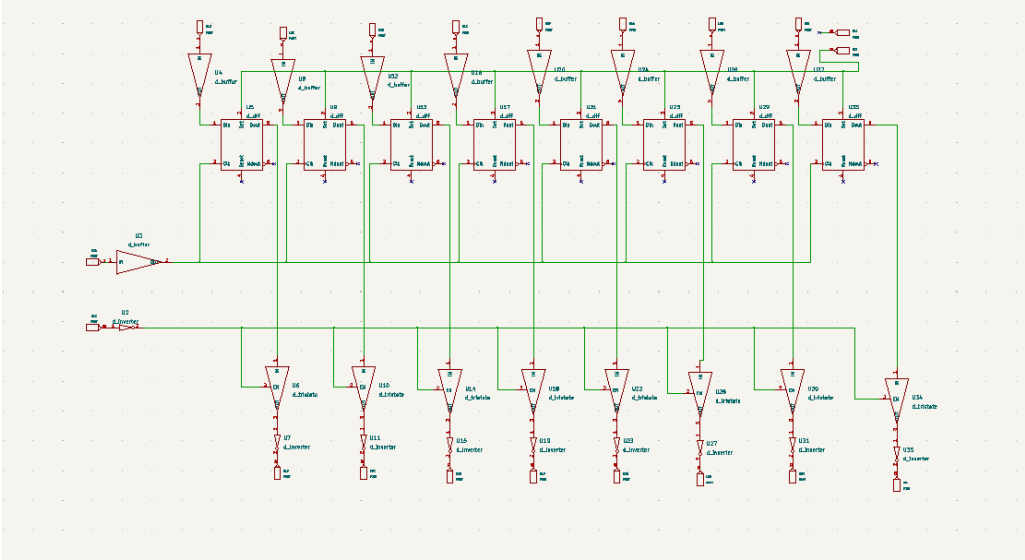

Figure 3.12: Sub-Circuit of IN74LV574

3.3.4 Test-Circuit Diagram

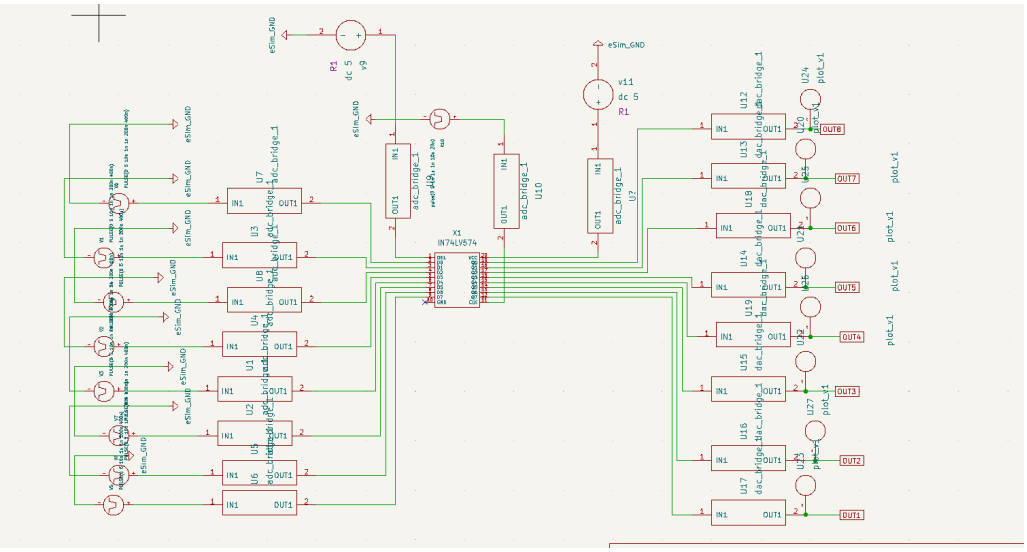

Figure 3.13: Test Circuit of IN74LV574

3.3.5 NgSpice Plot

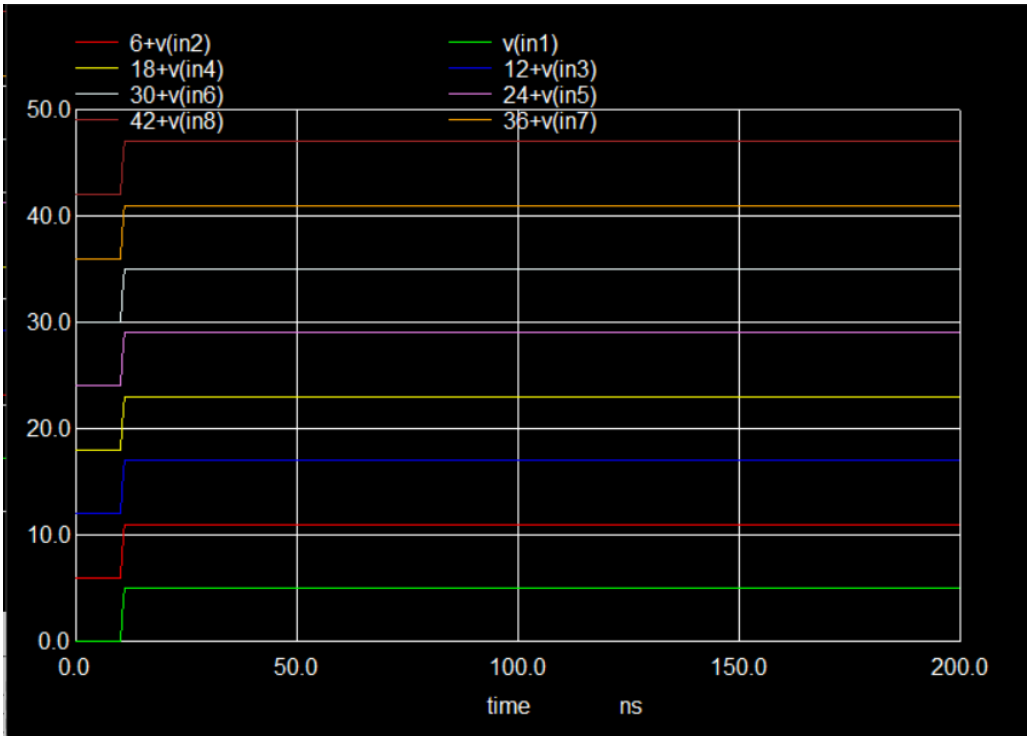

Figure 3.14: Input Graph of IN74LV574

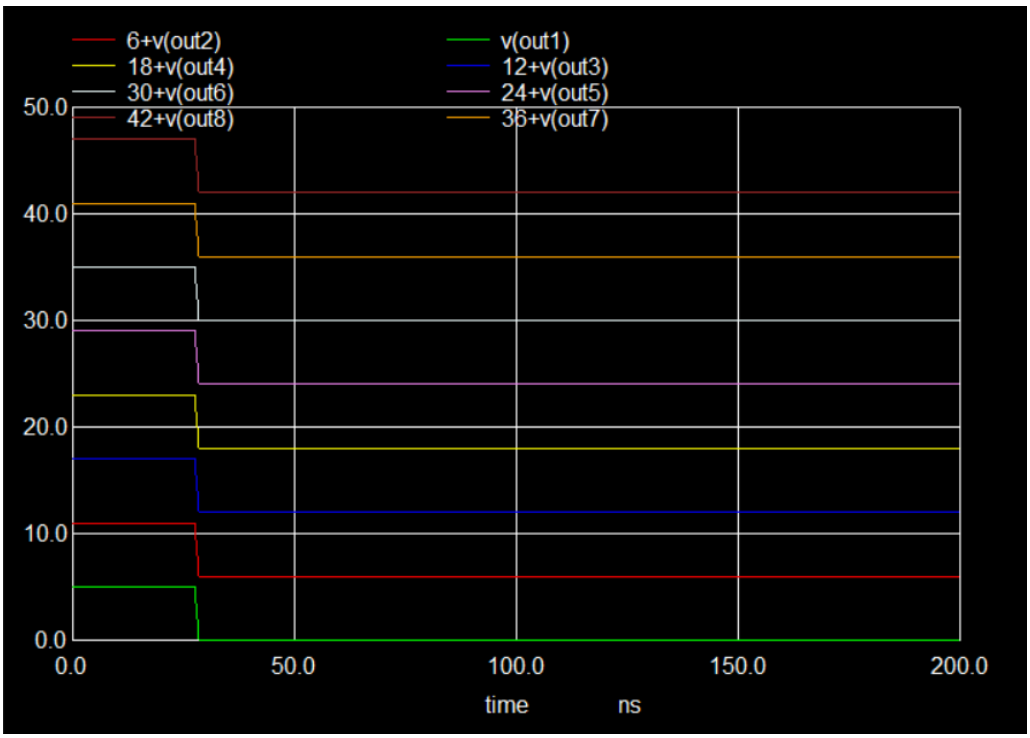

Figure 3.15: Output Graph of IN74LV574

3.4 74HCT164

3.4.1 Description

The 74HC164; 74HCT164 are 8-bit edge-triggered shift registers with serial data entry and an output from each of the eight stages. Data is entered serially through one of two inputs (DSA or DSB); either input can be used as an active HIGH enable for data entry through the other input. Both inputs must be connected together or an unused input must be tied HIGH.

Features Of 74HCT164

- **SIPO Architecture:** Takes a single serial data stream and clocks it out across eight parallel output pins (Q0–Q7 or QA–QH), making it highly useful for I/O pin expansion on microcontrollers.
- **Gated Serial Inputs (A & B):** Features two serial data inputs connected via an internal AND gate. This allows one pin to be used as an active-HIGH enable for data entry on the other pin. If both are tied together, it acts as a single serial input.
- **Positive Edge-Triggered Clock:** Data shifts one position to the right (from Q0 toward Q7) on every LOW-to-HIGH transition of the clock (CP or CLK) pin.

3.4.2 Pin Diagram

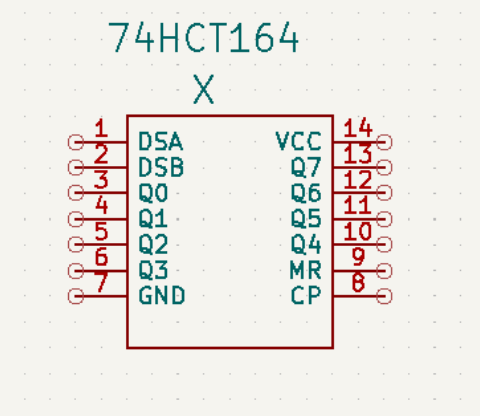

Figure 3.16: Pin Diagram of 74HCT164

3.4.3 Sub-Circuit Diagram

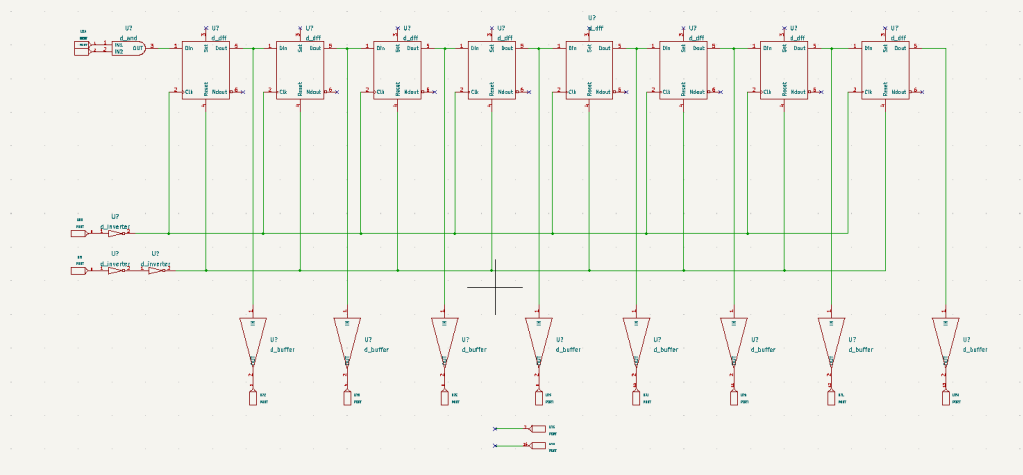

Figure 3.17: Sub-Circuit of 74HCT164

3.4.4 Test-Circuit Diagram

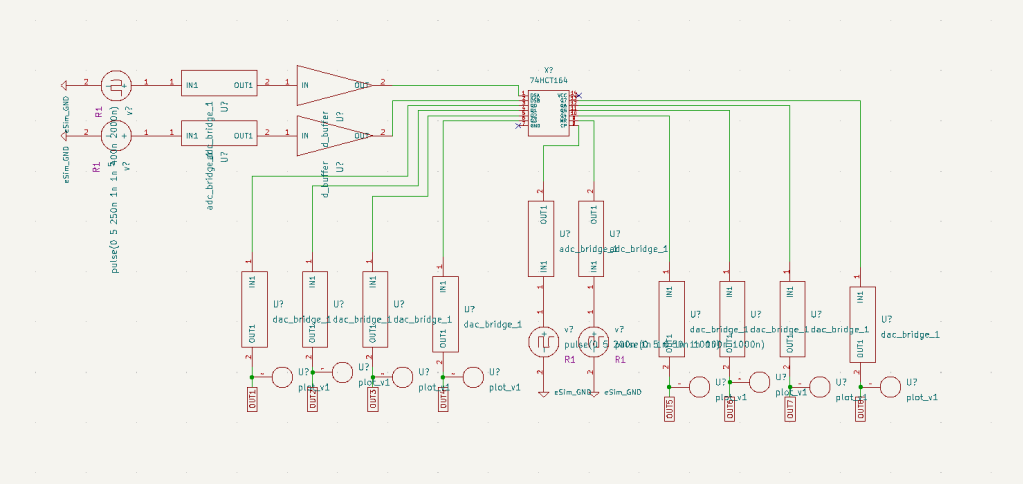

Figure 3.18: Test Circuit of 74HCT164

3.4.5 NgSpice Plot

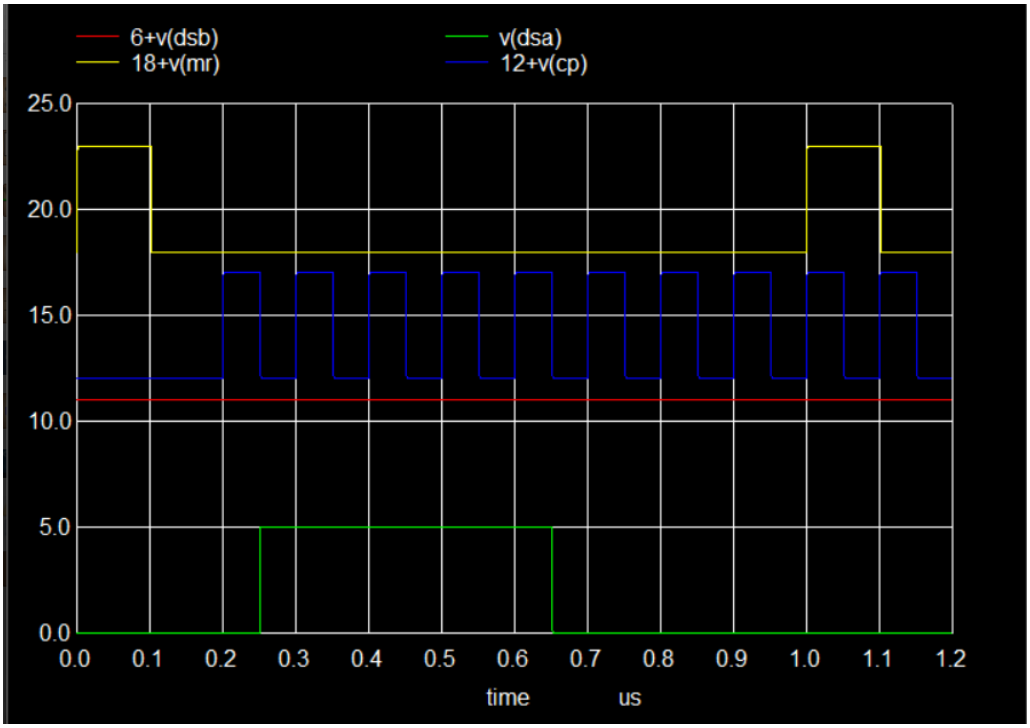

Figure 3.19: Input Graph of 74HCT164

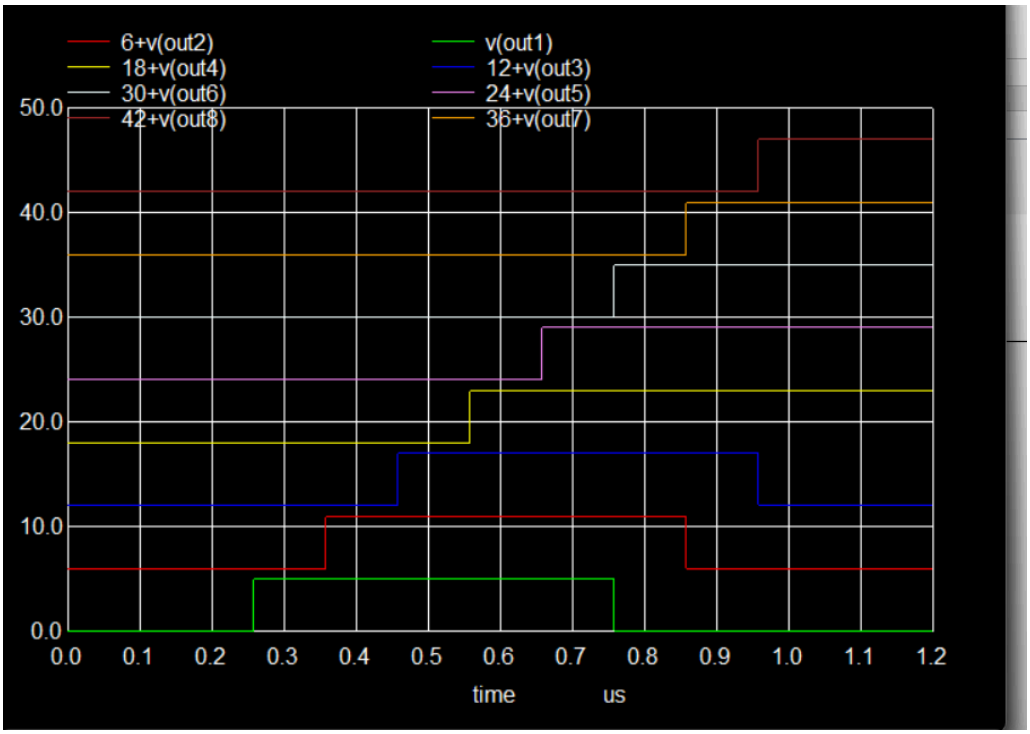

Figure 3.20: Output Graph of 74HCT164

3.5 CD4002

3.5.1 Description

These NOR and NAND gates are monolithic complementary MOS (CMOS) integrated circuits. The N- and P-channel enhancement mode transistors provide a symmetrical circuit with output swings essentially equal to the supply voltage. This results in high noise immunity over a wide supply voltage range. No DC power other than that caused by leakage current is consumed during static conditions. All inputs are protected against static discharge and latching conditions.

Features Of CD4002

- **Dual 4-Input NOR Logic:** Provides two separate logic gates. A HIGH on any of the four inputs (or any combination thereof) will force the respective output LOW. The output is HIGH only when all four inputs are LOW.
- **Buffered Outputs:** The outputs are buffered, which improves the transfer characteristics (sharper transitions) and provides consistent output drive capability regardless of the input logic combination.
- **High Noise Immunity:** Characteristic of the CD4000 series, it offers excellent noise margins, making it ideal for electrically noisy industrial environments.

3.5.2 Pin Diagram

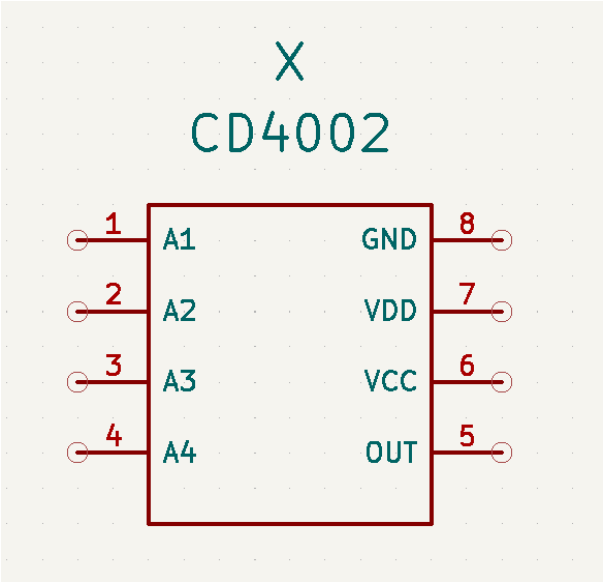

Figure 3.21: Pin Diagram of CD4002

3.5.3 Sub-Circuit Diagram

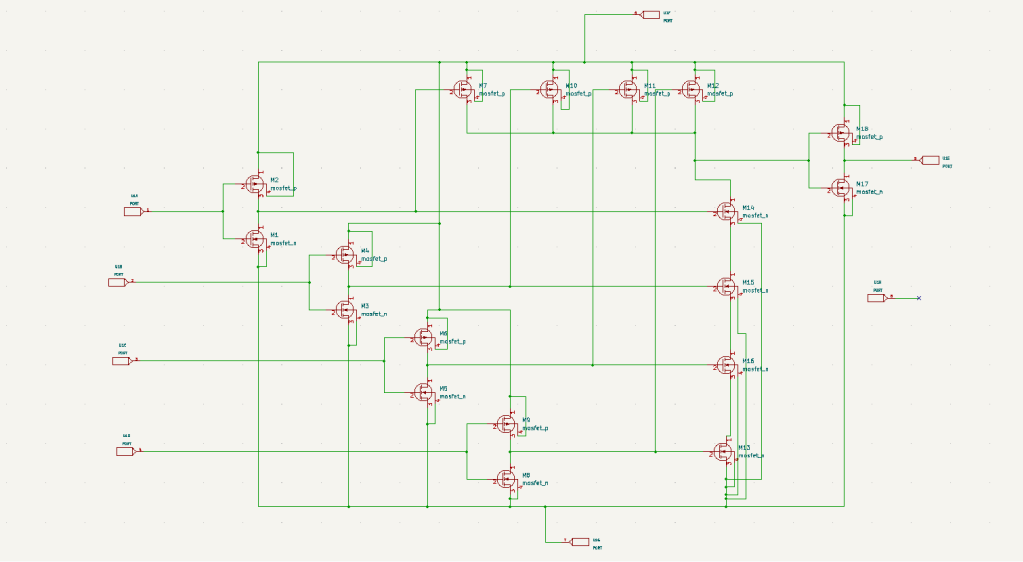

Figure 3.22: Sub-Circuit of CD4002

3.5.4 Test-Circuit Diagram

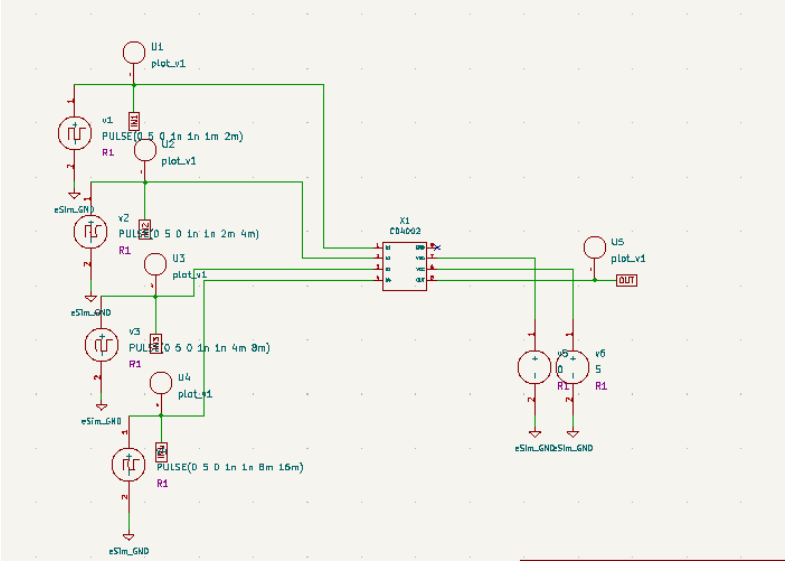

Figure 3.23: Test Circuit of CD4002

3.5.5 NgSpice Plot

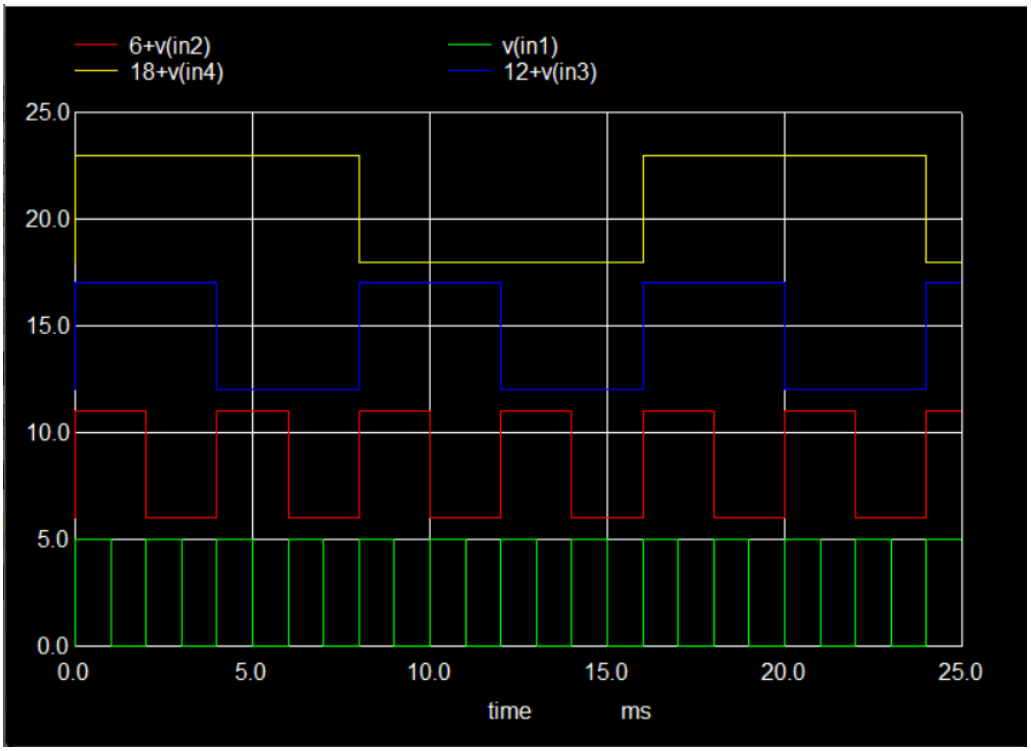

Figure 3.24: Input Graph of CD4002

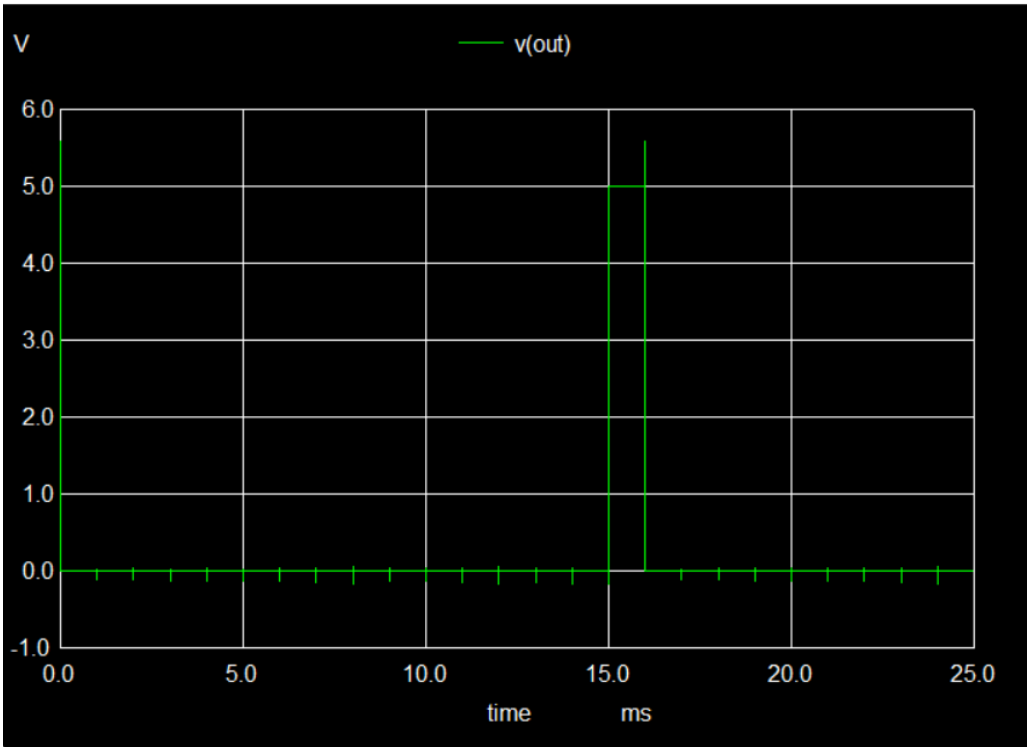

Figure 3.25: Output Graph of CD4002

3.6 SN74HC139

3.6.1 Description

The SN74HC139 devices are designed for high-performance memory-decoding or data-routing applications requiring very short propagation delay times. In high-performance memory systems, these decoders can minimize the effects of system decoding. When employed with high-speed memories utilizing a fast enable circuit, the delay time of these decoders and the enable time of the memory usually are less than the typical access time of the memory. This means that the effective system delay introduced by the decoders is negligible.

Features Of SN74HC139

- **Dual Independent Circuits:** The IC contains two completely separate 2-to-4 line decoders. They share only the power and ground pins.
- **Active-LOW Outputs:** The selected output pin goes LOW, while all other unselected outputs remain HIGH. This is extremely common for driving "Chip Select" (CS) or "Output Enable" (OE) lines on memory chips and peripherals.
- **Active-LOW Enable:** Each decoder has its own enable pin (often labeled G or EN). When this pin is HIGH, all four outputs of that decoder are forced HIGH, regardless of the address inputs.

3.6.2 Pin Diagram

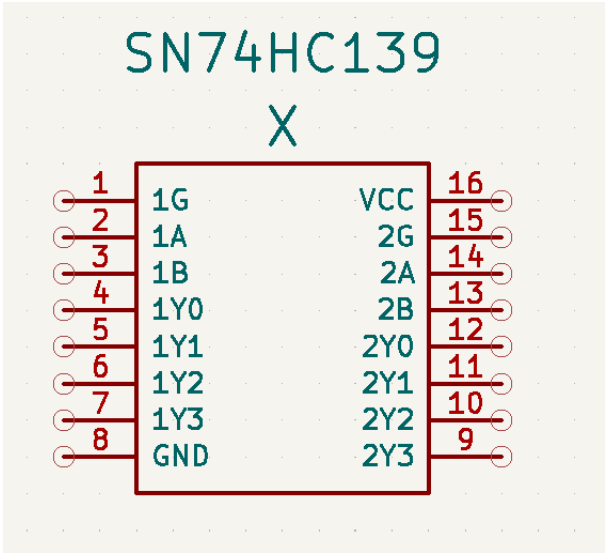

Figure 3.26: Pin Diagram of SN74HC139

3.6.3 Sub-Circuit Diagram

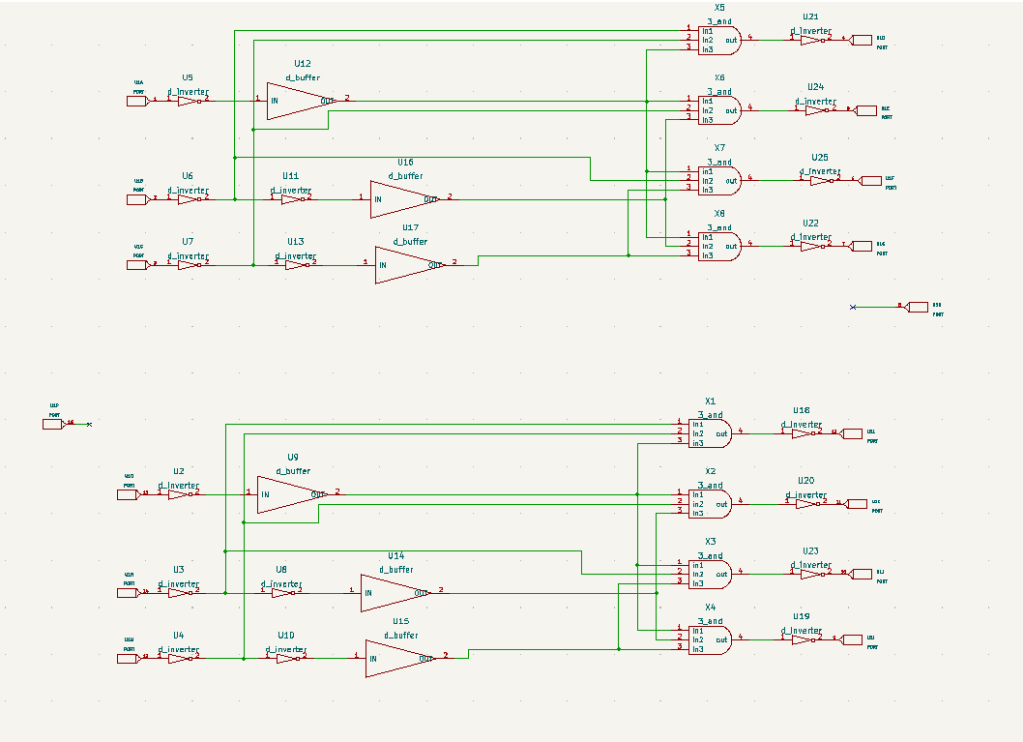

Figure 3.27: Sub-Circuit of SN74HC139

3.6.4 Test-Circuit Diagram

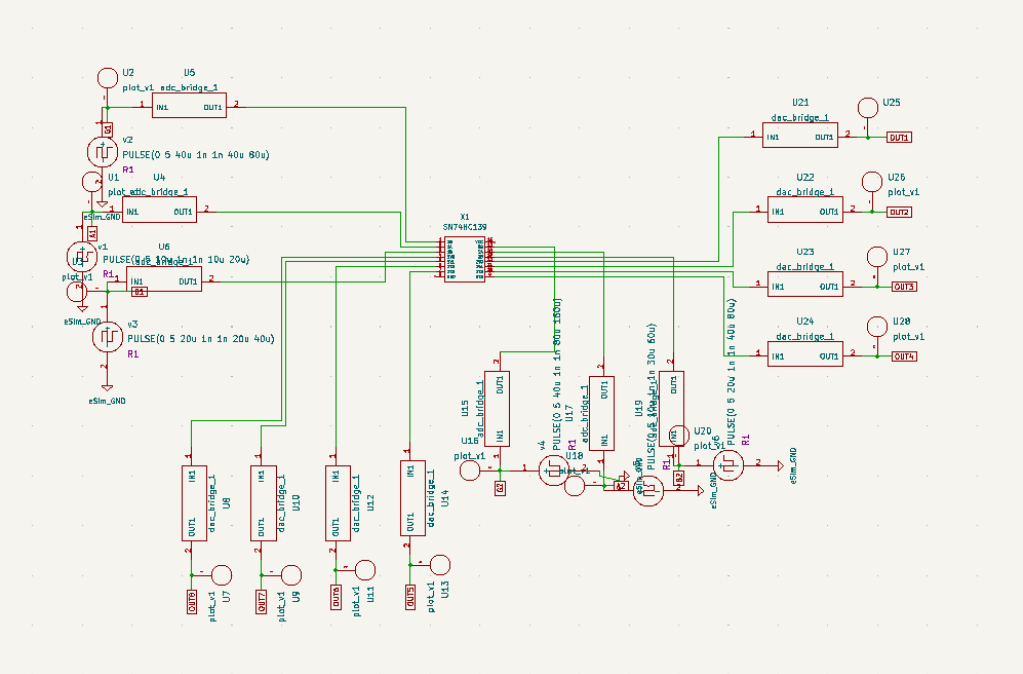

Figure 3.28: Test Circuit of SN74HC139

3.6.5 NgSpice Plot

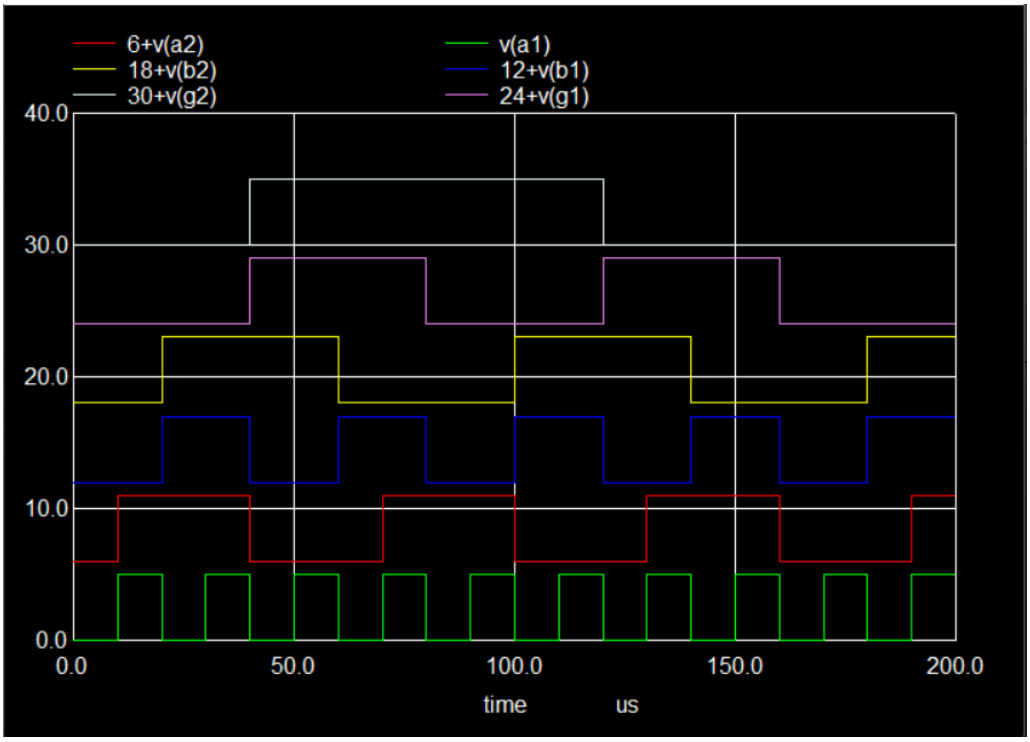

Figure 3.29: Input Graph of SN74HC139

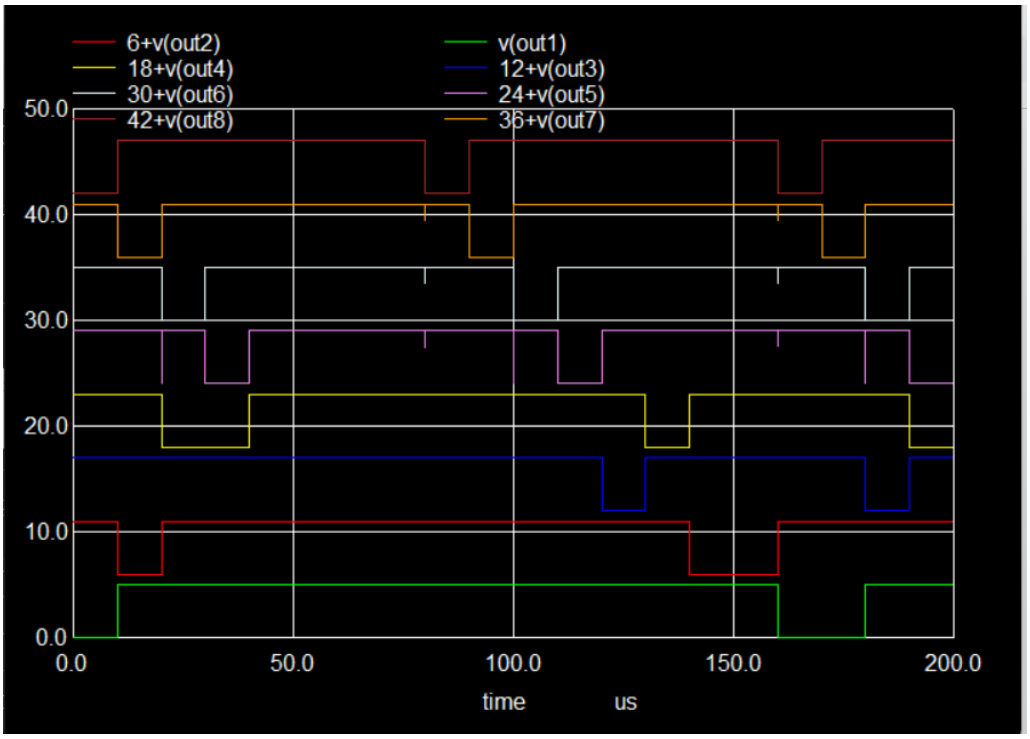

Figure 3.30: Output Graph of SN74HC139

3.7 SN74LVC2G100

3.7.1 Description

The SN74LVC2G100 is a dual, sequential, configurable multiple function device with Schmitt Trigger inputs. Sixteen patterns of a 4-bit input determines the output state. The output state serves as the input to a D-Flip Flop, which is transferred to the Q output on the positive going CLK edge. The user can choose the logic functions MUX, AND, OR, NAND, NOR, inverter, and non-inverter.

Features Of SN74LVC2G100

- **Integrated D-Flip Flop:** The output state computed by the configured logic gate does not go straight to the output pin. Instead, it serves as the D input to an internal D-type flip-flop.
- **Positive Edge-Triggered:** The evaluated logic state is latched and transferred to the Q output on the LOW-to-HIGH transition of the clock (CLK) pulse.
- **Schmitt-Trigger Inputs:** All inputs feature Schmitt-trigger action. This provides excellent noise immunity and allows the chip to reliably handle slow or noisy input signals without output oscillation.

3.7.2 Pin Diagram

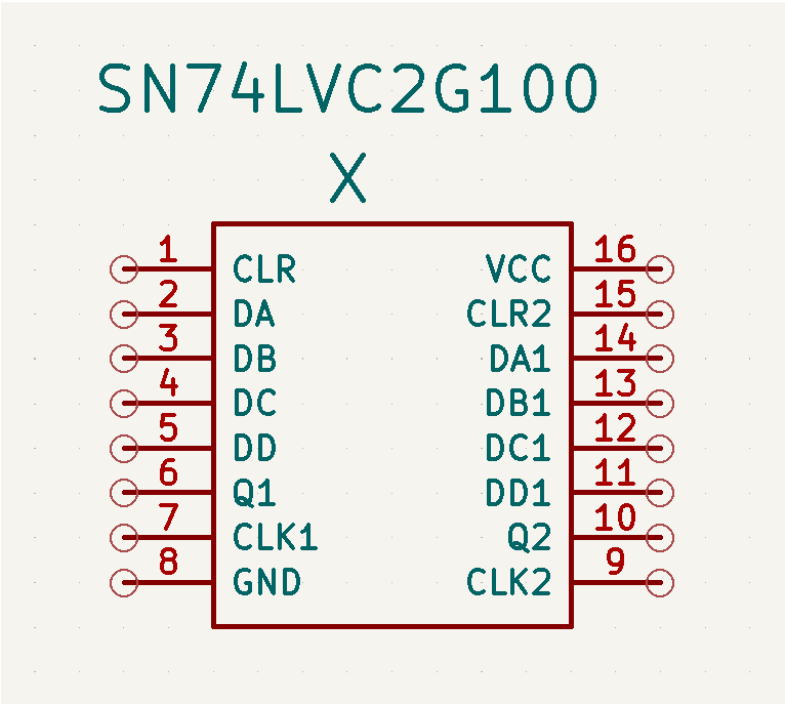

Figure 3.31: Pin Diagram of SN74LVC2G100

3.7.3 Sub-Circuit Diagram

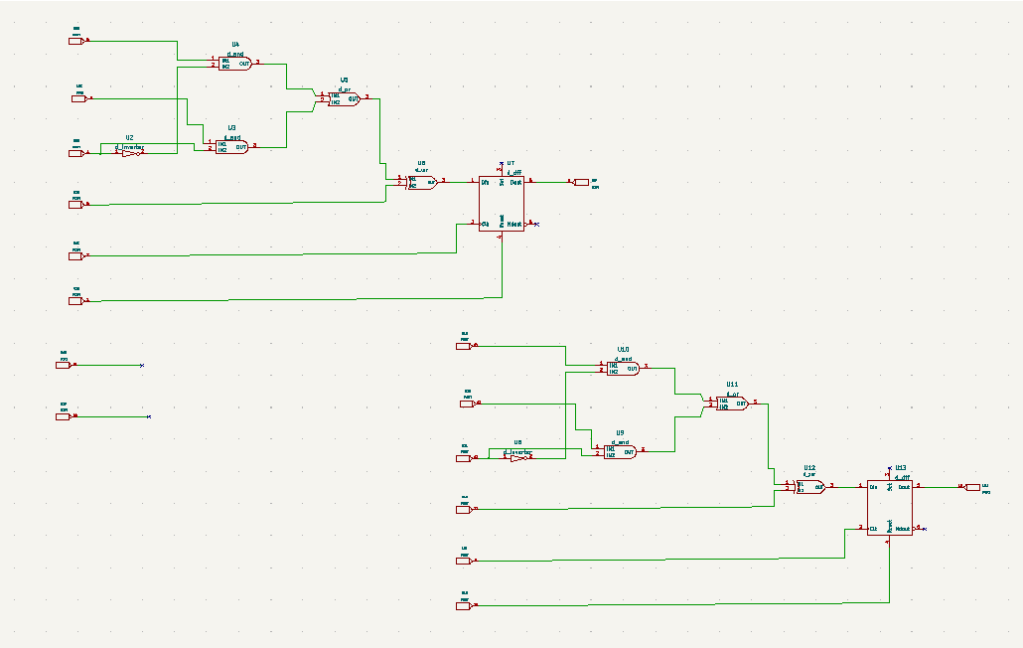

Figure 3.32: Sub-Circuit of SN74LVC2G100

3.7.4 Test-Circuit Diagram

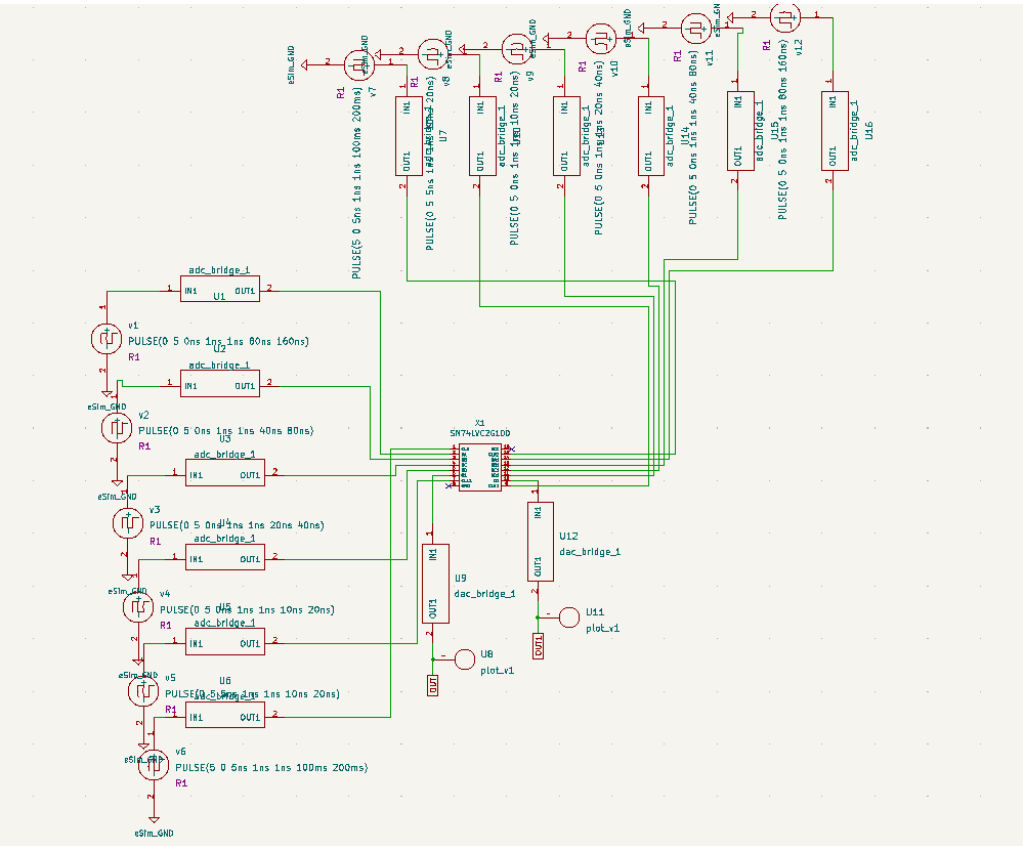

Figure 3.33: Test Circuit of SN74LVC2G100

3.7.5 NgSpice Plot

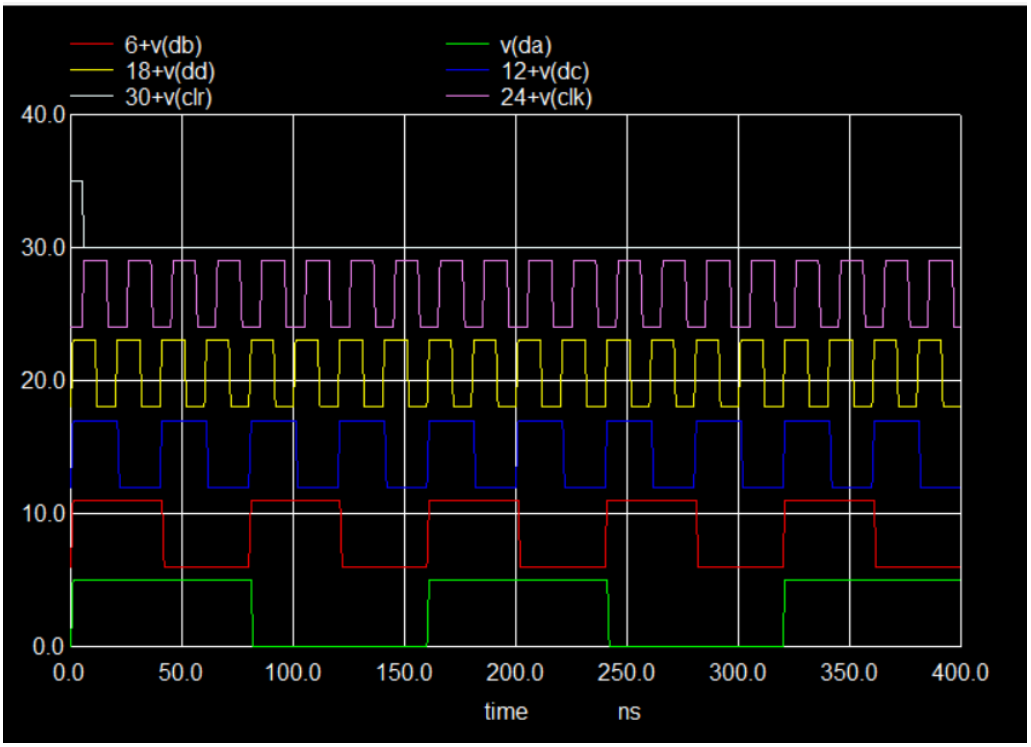

Figure 3.34: Input Graph of SN74LVC2G100

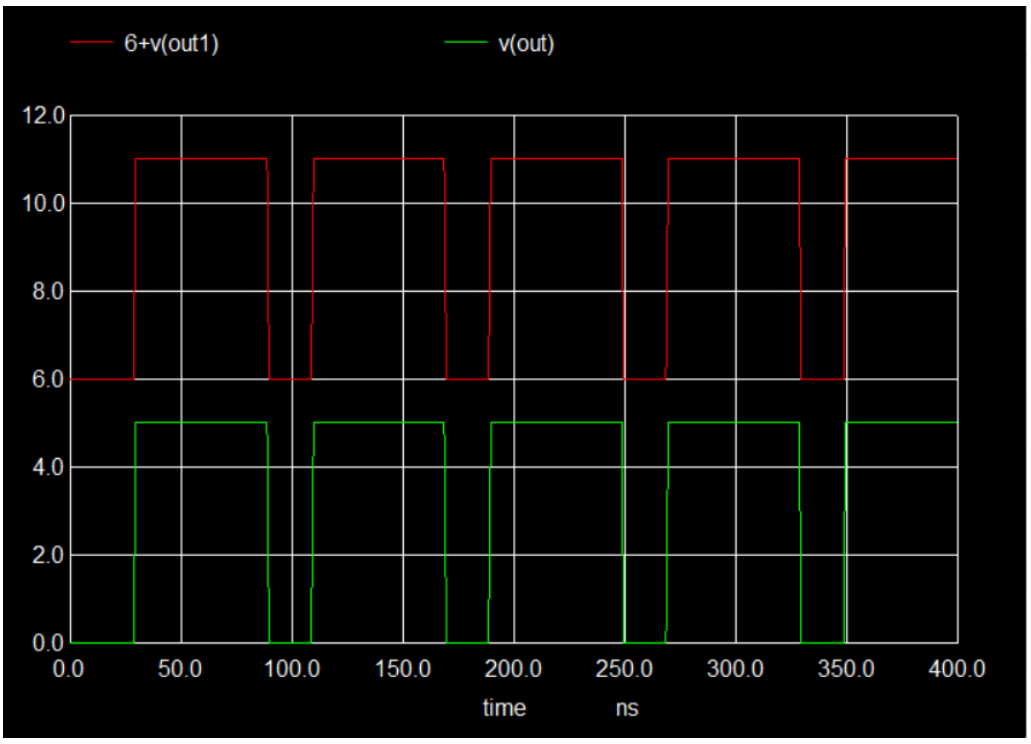

Figure 3.35: Output Graph of SN74LVC2G100

3.8 CD4078BE

3.8.1 Description

The CD4078B types are supplied in 14-lead hermetic dual-in-line ceramic packages (F3A suffix), 14-lead dual-in-line plastic packages (E suffix), 14-lead small-outline packages (M, MT, M96, and NSR suffixes), and 14-lead thin shrink small-outline packages (PW and PWR suffixes).

Features Of CD4078BE

- **Wide Input Cascading:** It allows you to check if any of eight separate signal lines are active using a single chip, making it highly useful for creating large address decoders, interrupt handlers, or parity checking networks.
- **Fully Buffered:** All inputs and outputs are buffered. This ensures that the output impedance and switching speeds remain consistent regardless of how many input pins are being driven or changed simultaneously.
- **Symmetrical Characteristics:** The buffered outputs provide standardized, symmetrical output voltage transitions, meaning the rise time and fall time are closely matched.

3.8.2 Pin Diagram

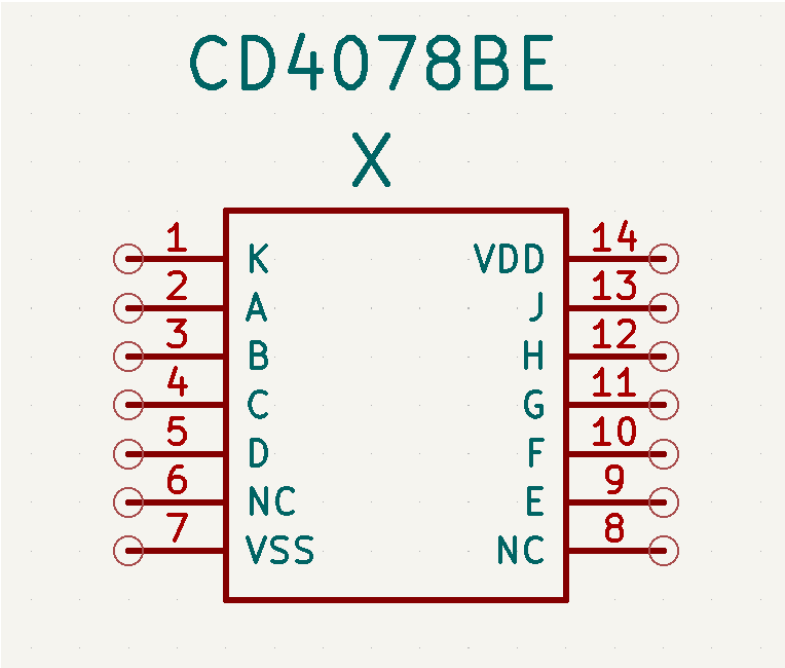

Figure 3.36: Pin Diagram of CD4078BE

3.8.3 Sub-Circuit Diagram

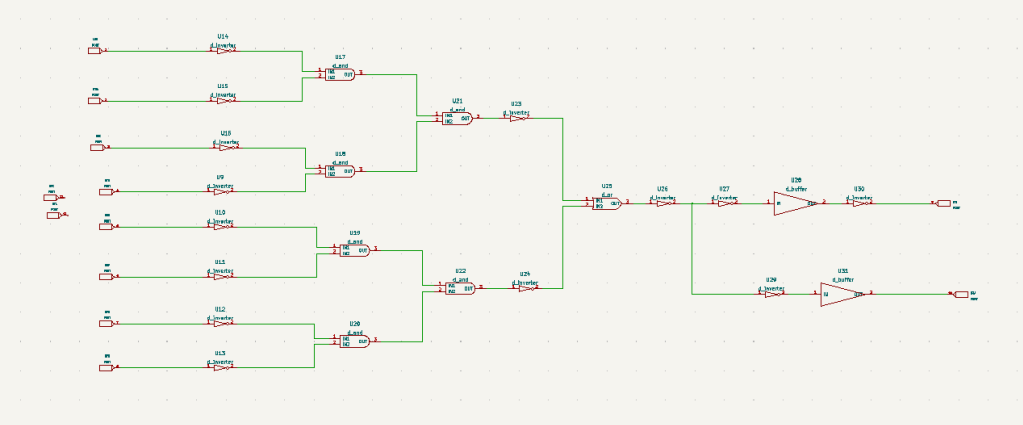

Figure 3.37: Sub-Circuit of CD4078BE

3.8.4 Test-Circuit Diagram

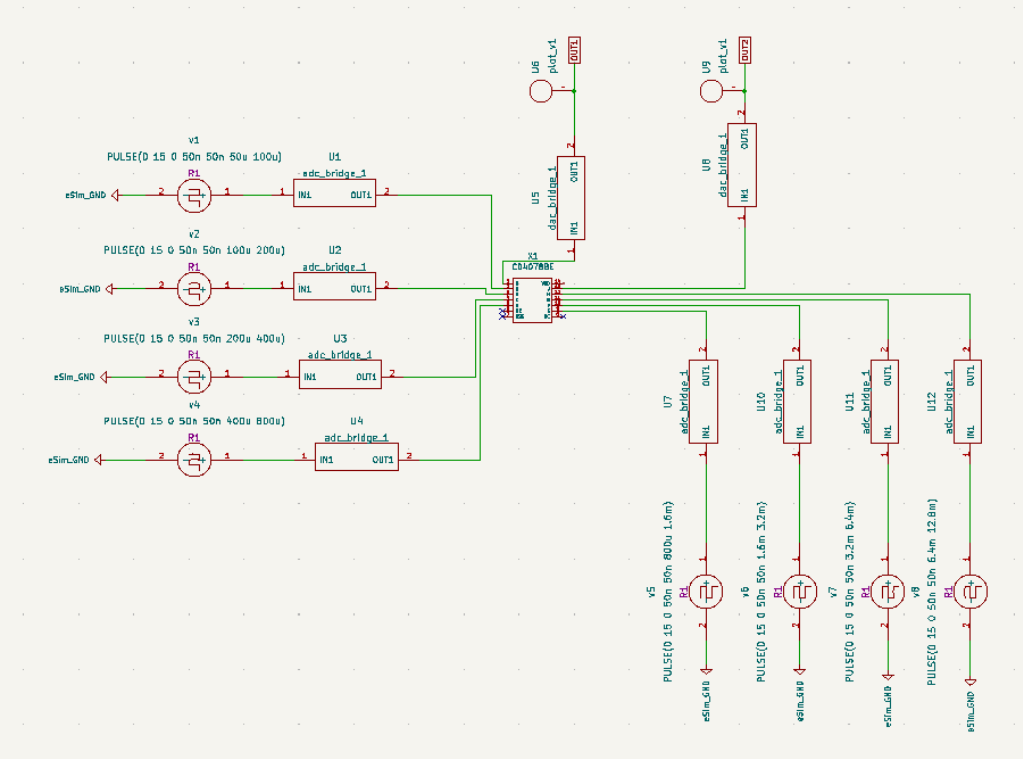

Figure 3.38: Test Circuit of CD4078BE

3.8.5 NgSpice Plot

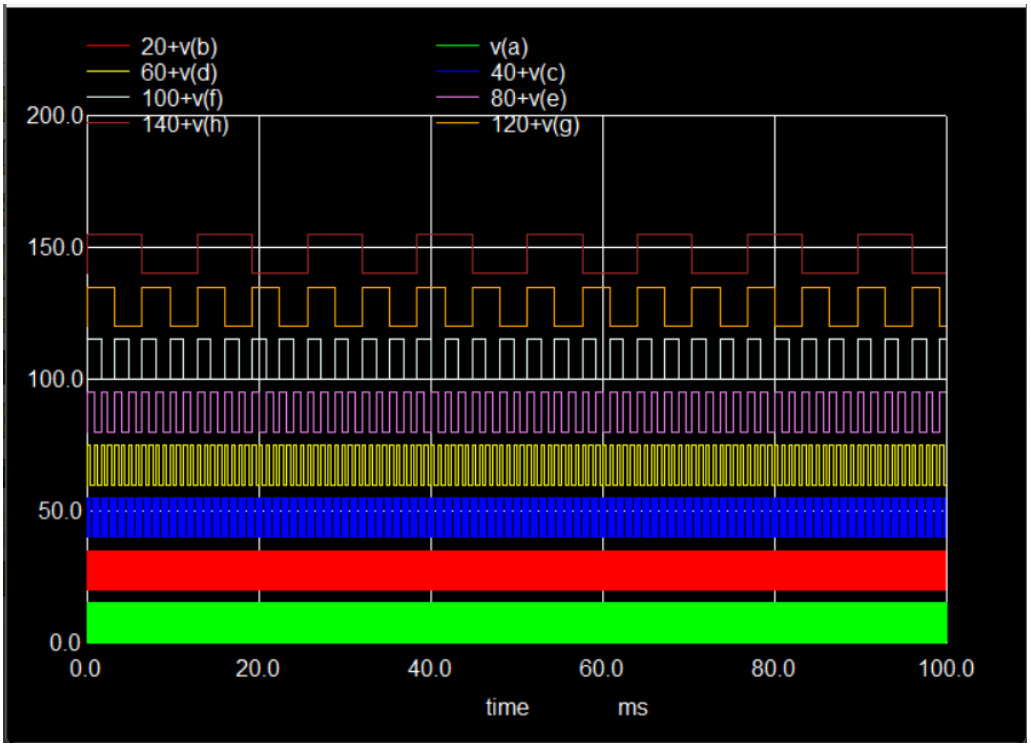

Figure 3.39: Input Graph of CD4078BE

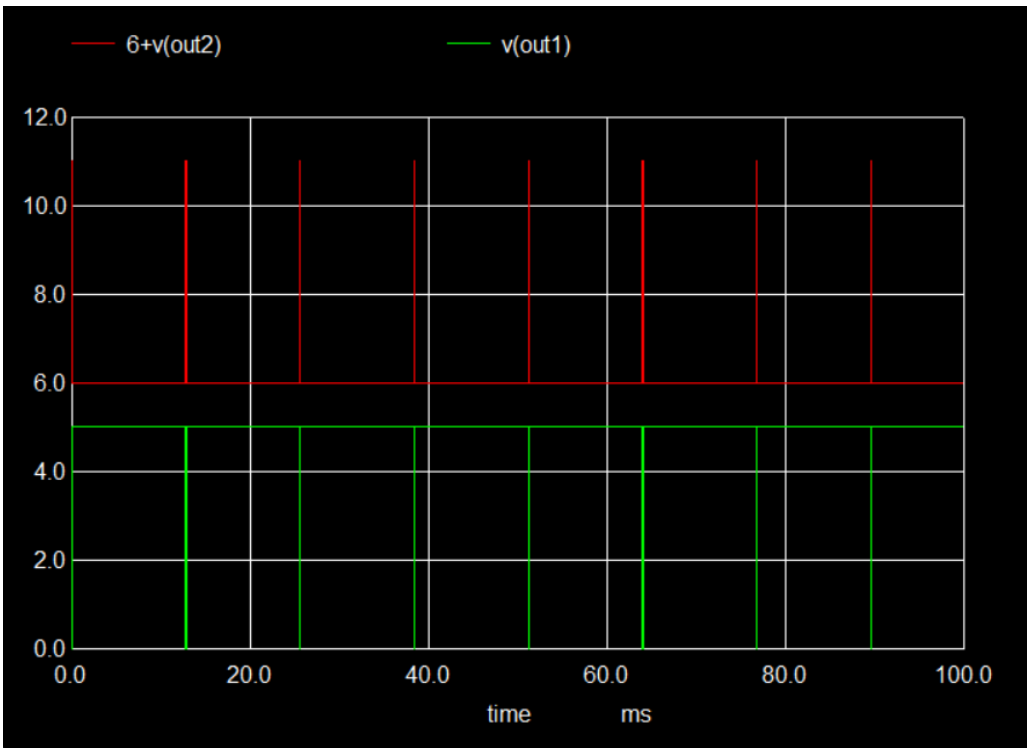

Figure 3.40: Output Graph of CD4078BE

3.9 TPIC6C595

3.9.1 Description

The TPIC6C595 is supplied in 14-lead hermetic dual-in-line ceramic packages (F3A suffix), 14-lead dual-in-line plastic packages (E suffix), 14-lead small-outline packages (M, MT, M96, and NSR suffixes), and 14-lead thin shrink small-outline packages (PW and PWR suffixes).

Features Of TPIC6C595

- **8-Bit SIPO Architecture:** Features an 8-bit serial-in, parallel-out (SIPO) shift register that feeds into an 8-bit D-type storage register (latch).
- **Open-Drain DMOS Outputs:** The outputs (DRAIN0–DRAIN7) are low-side, open-drain DMOS transistors. When the output state is HIGH, the transistor turns on and sinks current to ground. When LOW, the output is off (high impedance).
- **Built-in Transient Protection:** It contains integrated voltage clamps (rated to 33V) on the outputs. This provides inductive transient protection, making it highly suitable for directly driving inductive loads like relays, solenoids, and stepper motors without requiring external flyback diodes.

3.9.2 Pin Diagram

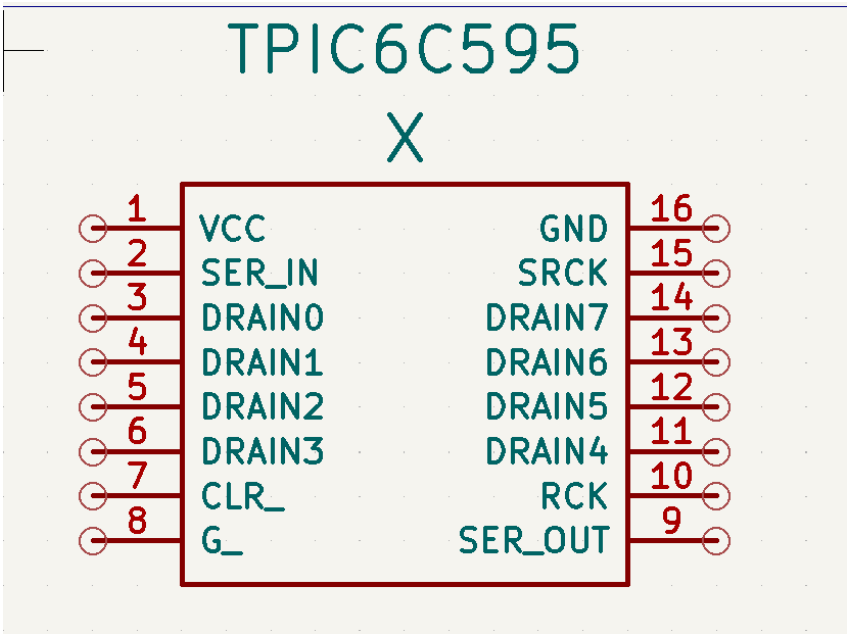

Figure 3.41: Pin Diagram of TPIC6C595

3.9.3 Sub-Circuit Diagram

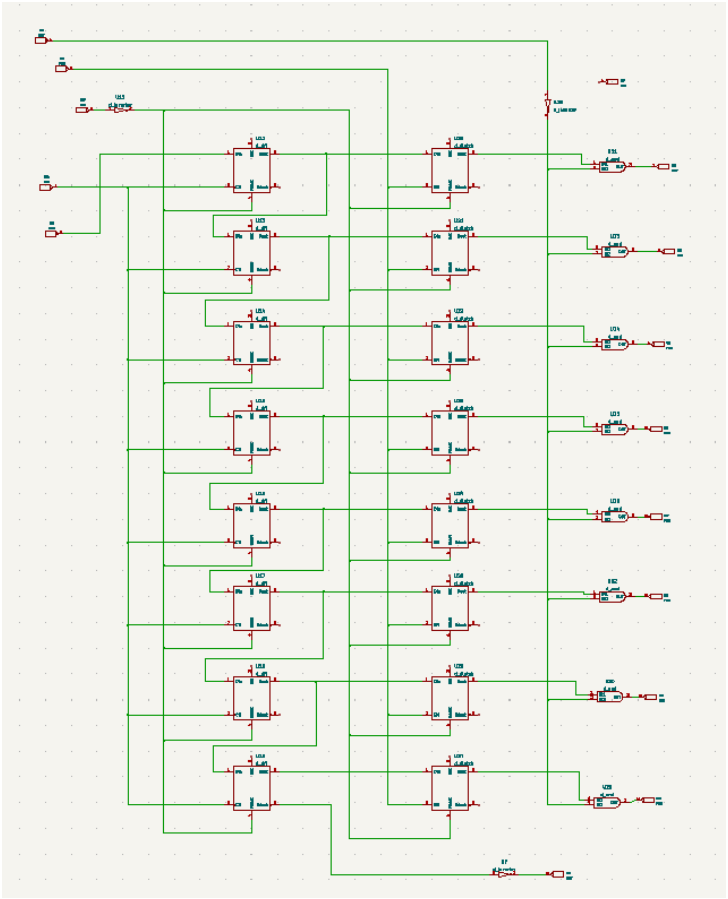

Figure 3.42: Sub-Circuit of TPIC6C595

3.9.4 Test-Circuit Diagram

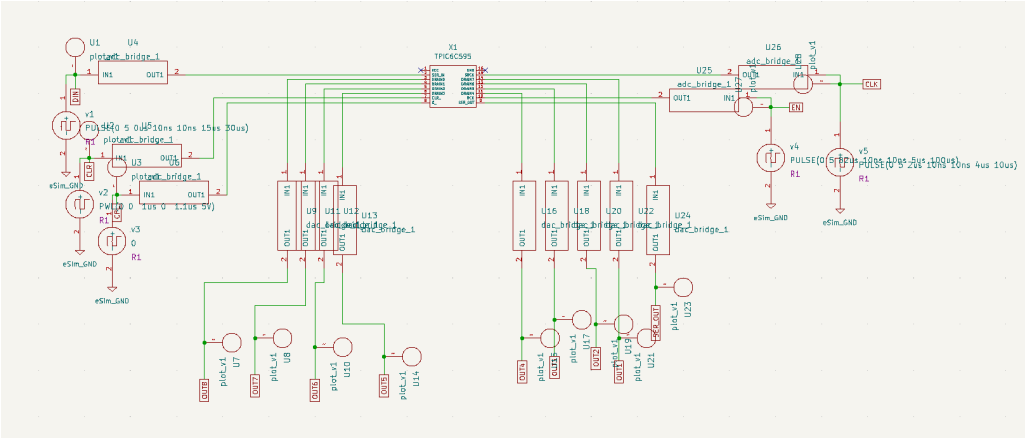

Figure 3.43: Test Circuit of TPIC6C595

3.9.5 NgSpice Plot

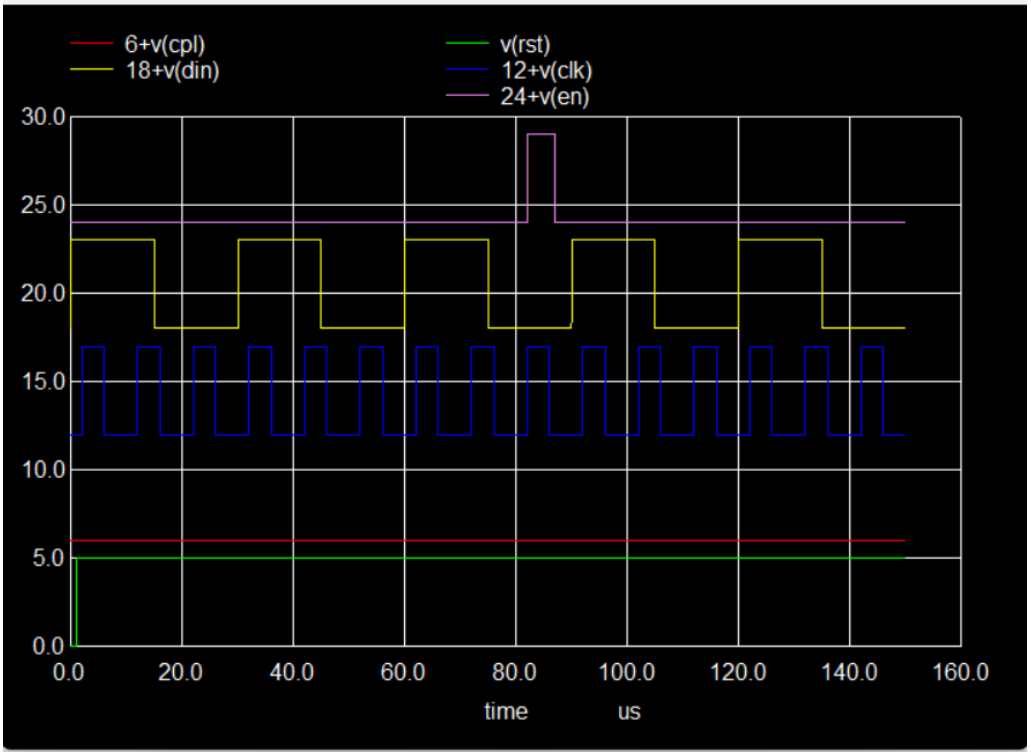

Figure 3.44: Input Graph of TPIC6C595

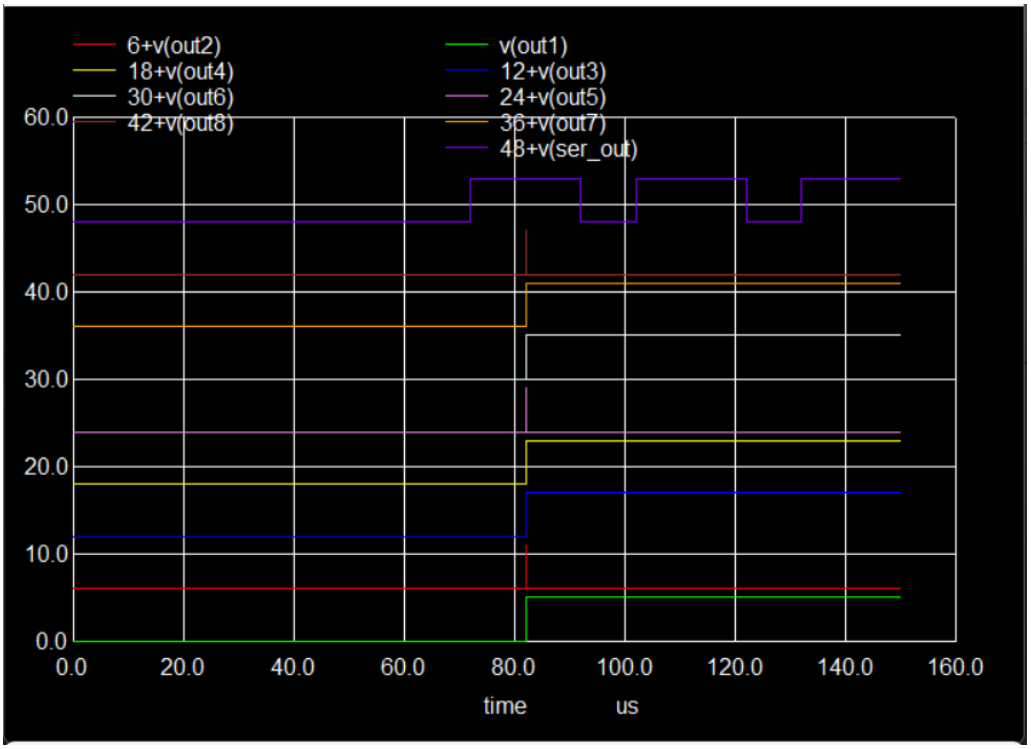

Figure 3.45: Output Graph of TPIC6C595

3.10 74HCT93

3.10.1 Description

The 74HC/HCT93 are 4-bit binary ripple counters. The devices consist of four master-slave flip-flops internally connected to provide a divide-by-two section and a divide-by-eight section. Each section has a separate clock input (CP0 and CP1) to initiate state changes of the counter on the HIGH-to-LOW clock transition. State changes of the outputs do not occur simultaneously because of internal ripple delays. Therefore, decoded output signals are subject to decoding spikes and should not be used for clocks or strobes.

Features Of 74HCT93

- **Two-Section Architecture:** The chip is internally divided into two independent counters: a 1-bit (divide-by-2) counter and a 3-bit (divide-by-8) counter.
- **External Cascading:** To function as a full 4-bit (divide-by-16) binary counter, the output of the first stage (Q0) must be externally wired to the clock input of the second stage (CP1). If left unconnected, you can use the two sections completely independently.
- **Negative Edge-Triggered:** The internal flip-flops change state on the HIGH-to-LOW transition of the clock pulses.

3.10.2 Pin Diagram

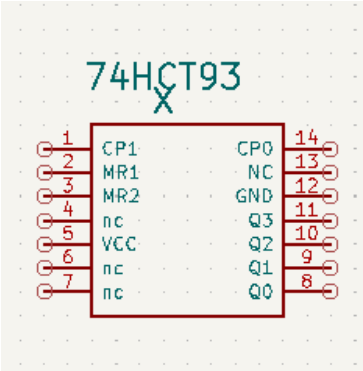

Figure 3.46: Pin Diagram of 74HCT93

3.10.3 Sub-Circuit Diagram

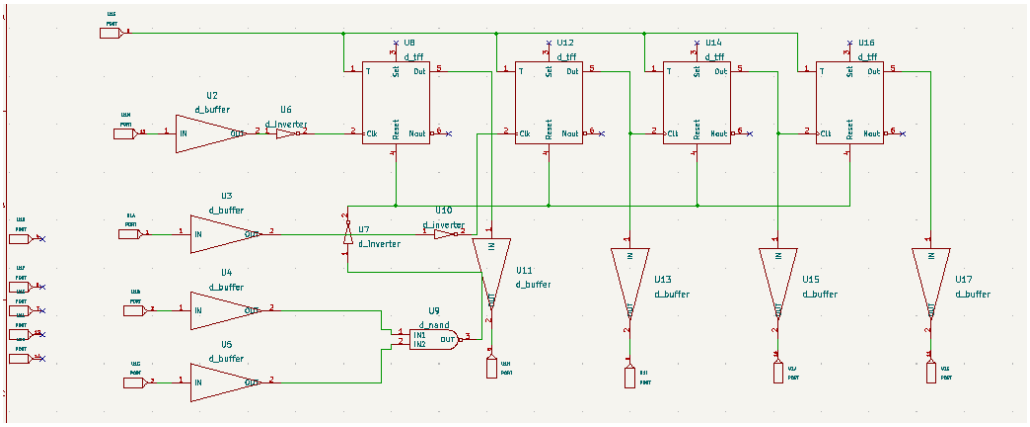

Figure 3.47: Sub-Circuit of 74HCT93

3.10.4 Test-Circuit Diagram

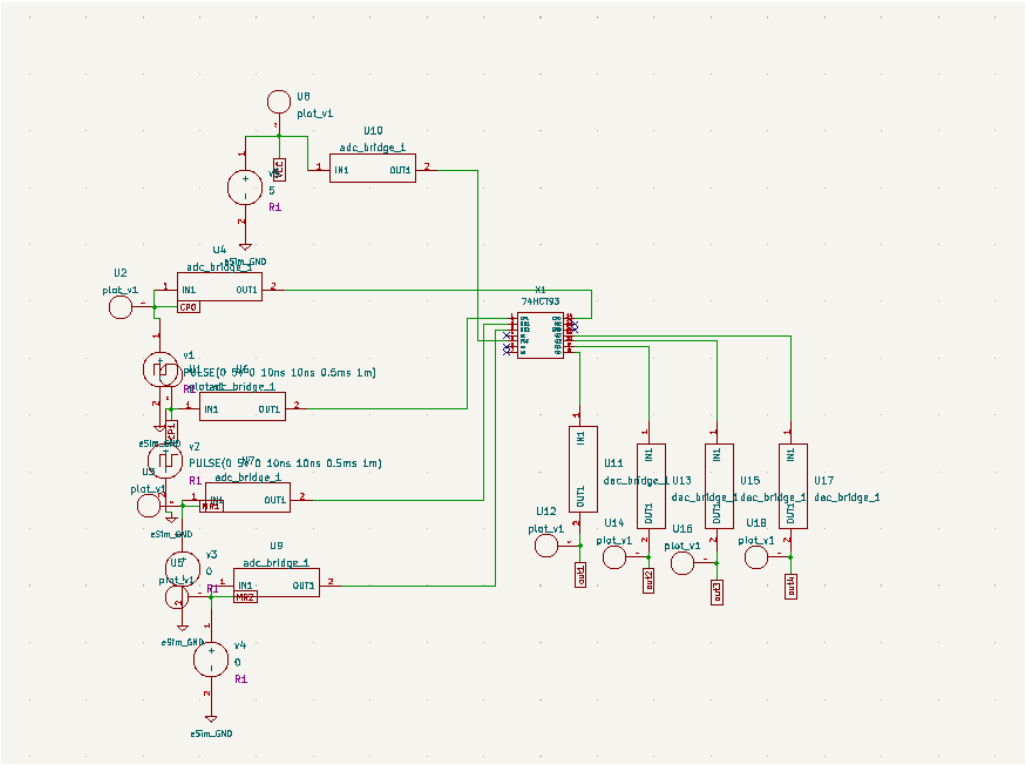

Figure 3.48: Test Circuit of 74HCT93

3.10.5 NgSpice Plot

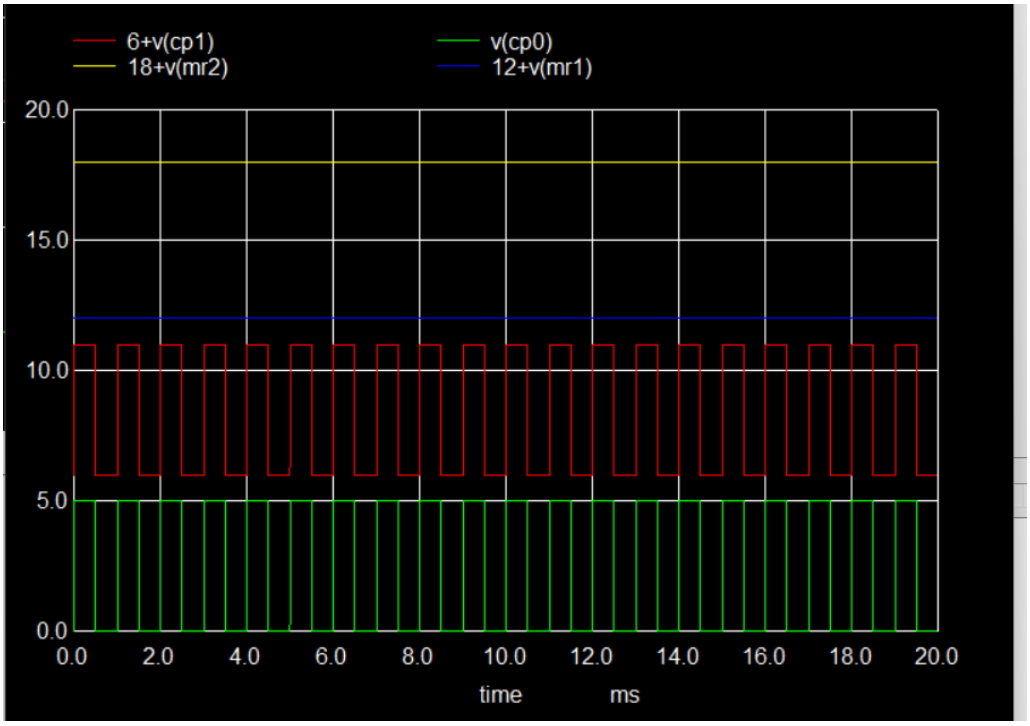

Figure 3.49: Input Graph of 74HCT93

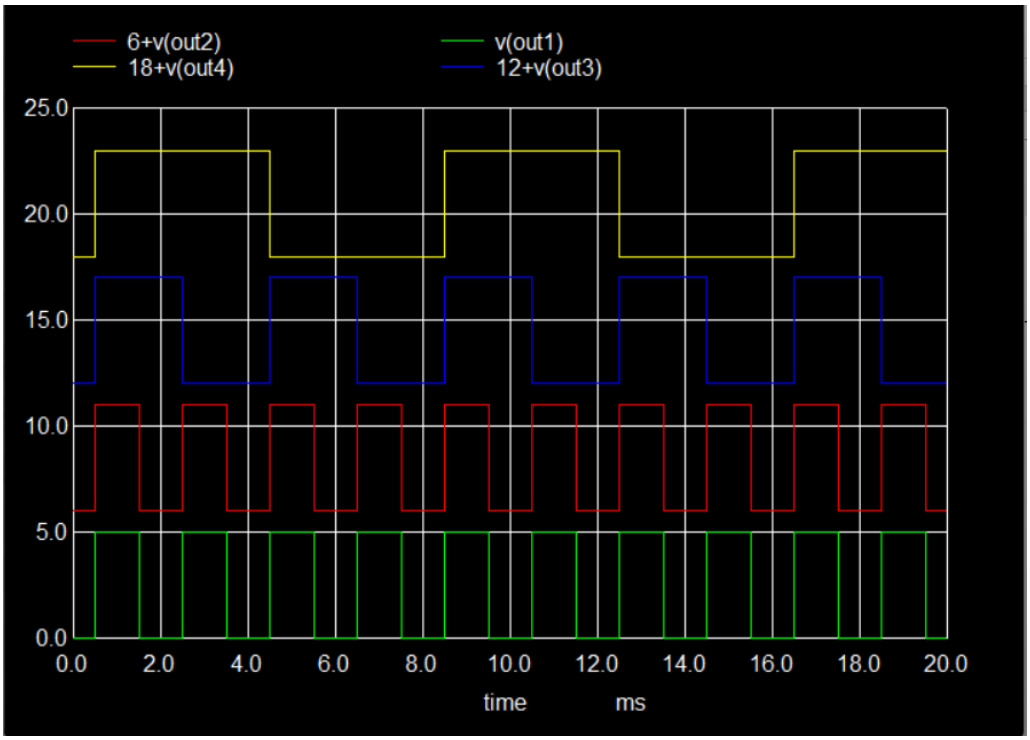

Figure 3.50: Output Graph of 74HCT93

3.11 74HCT151

3.11.1 Description

The 74HC/HCT151 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

Features Of 74HCT151

- **Multiplexing Capability:** Acts as an 8-to-1 multiplexer, selecting one of eight inputs (I_0 to I_7) based on a 3-bit binary address (S_0, S_1, S_2).
- **Output Configuration:** Provides both True (Y) and Complementary ($\overline{Y}$) outputs.
- **Enable Input:** Features an active-LOW enable input $\overline{E}$. When $\overline{E}$ is HIGH, the Y output is forced LOW and the $\overline{E}$ output is forced HIGH, regardless of the other inputs.
- **TTL Compatibility:** The "HCT" designation indicates that the device has TTL-compatible input levels, making it easy to interface with systems operating at 5V logic levels.

3.11.2 Pin Diagram

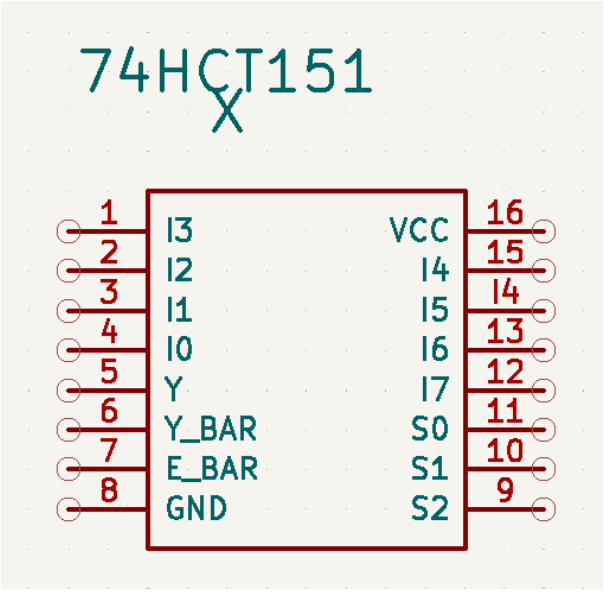

Figure 3.51: Pin Diagram of 74HCT151

3.11.3 Sub-Circuit Diagram

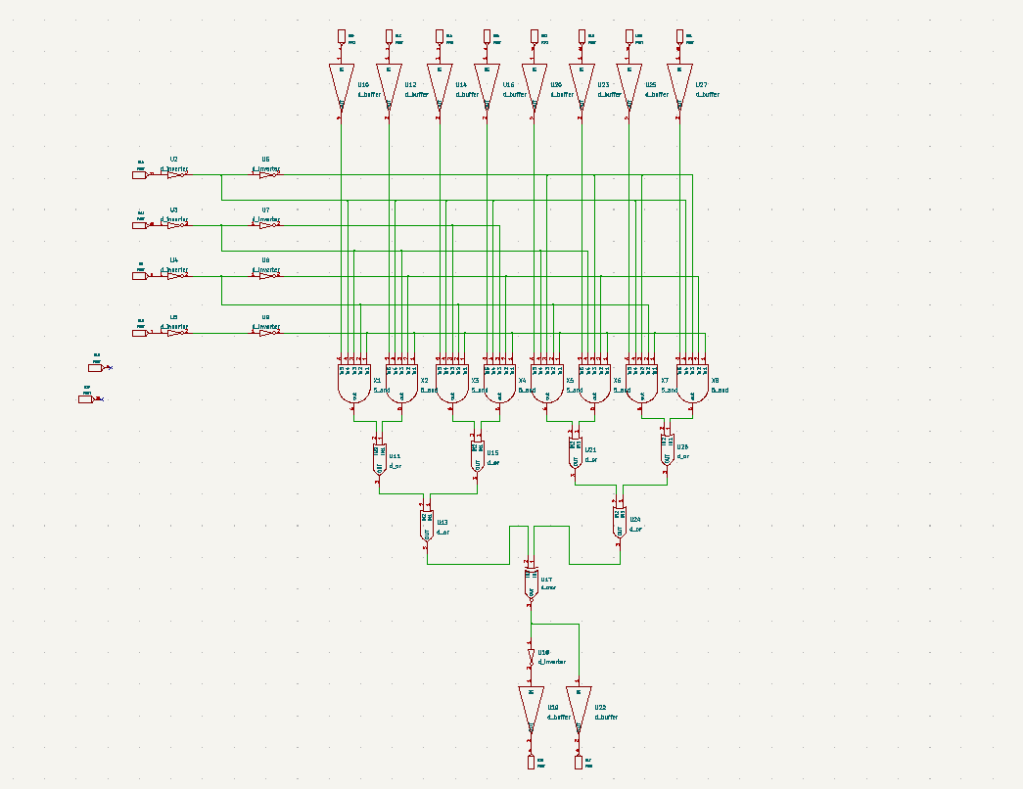

Figure 3.52: Sub-Circuit of 74HCT151

3.11.4 Test-Circuit Diagram

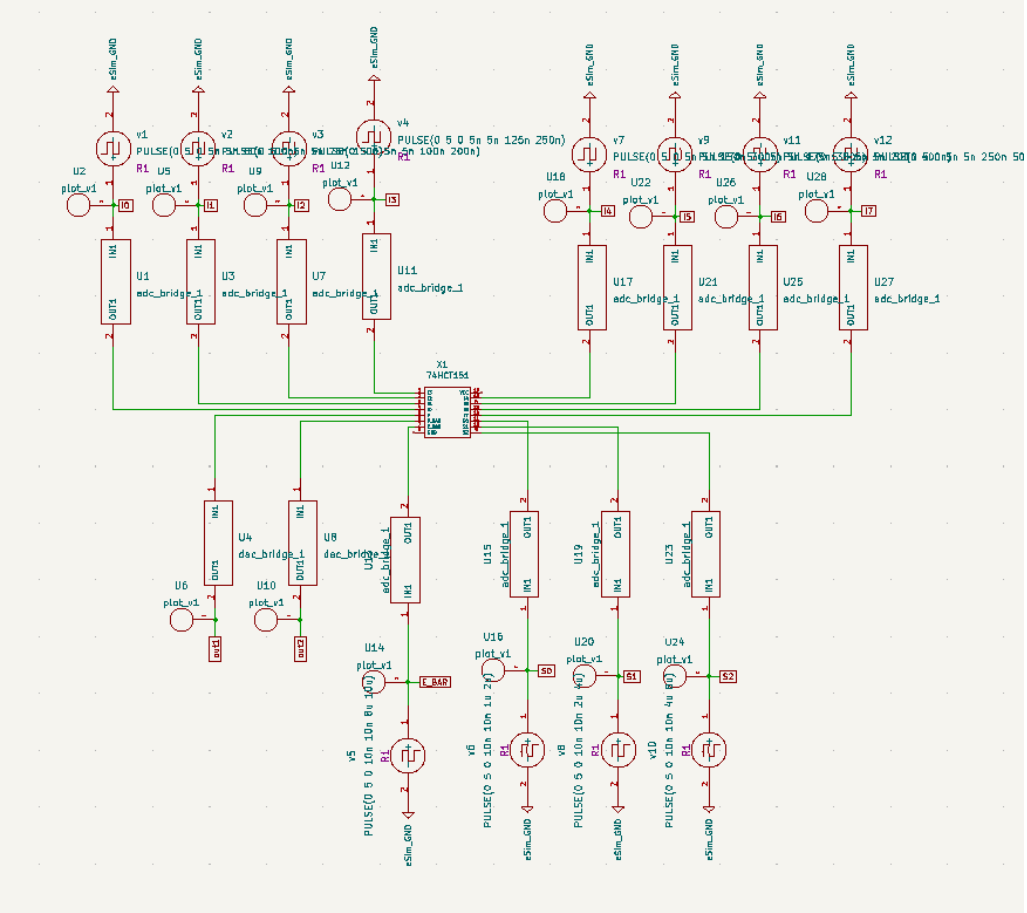

Figure 3.53: Test Circuit of 74HCT151

3.11.5 NgSpice Plot

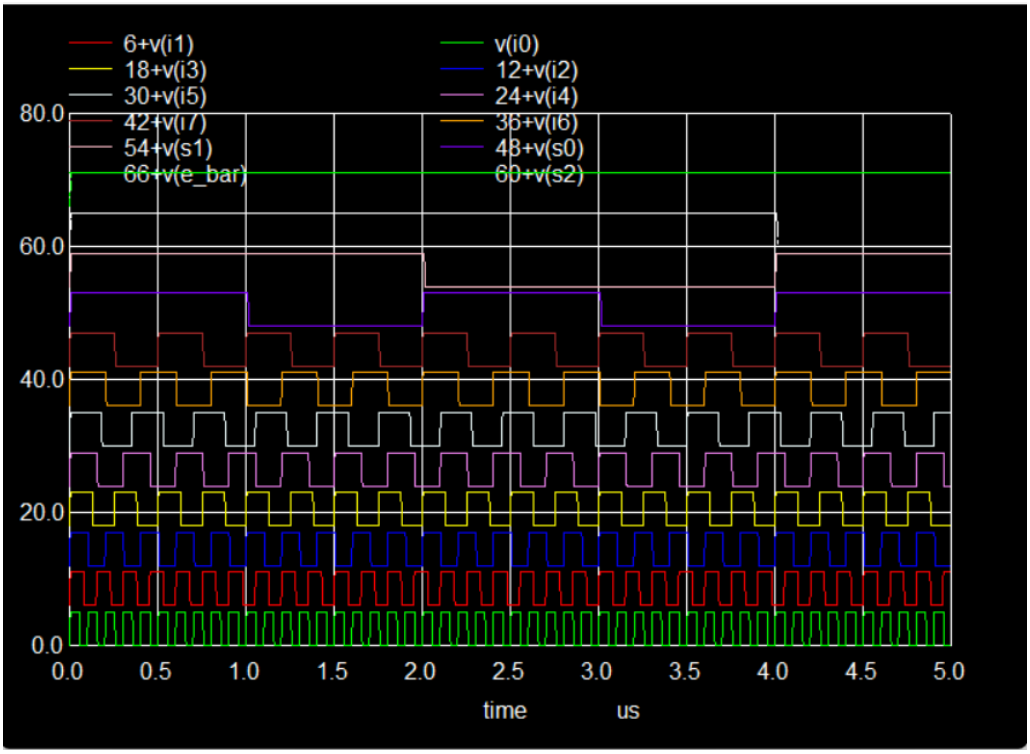

Figure 3.54: Input Graph of 74HCT151

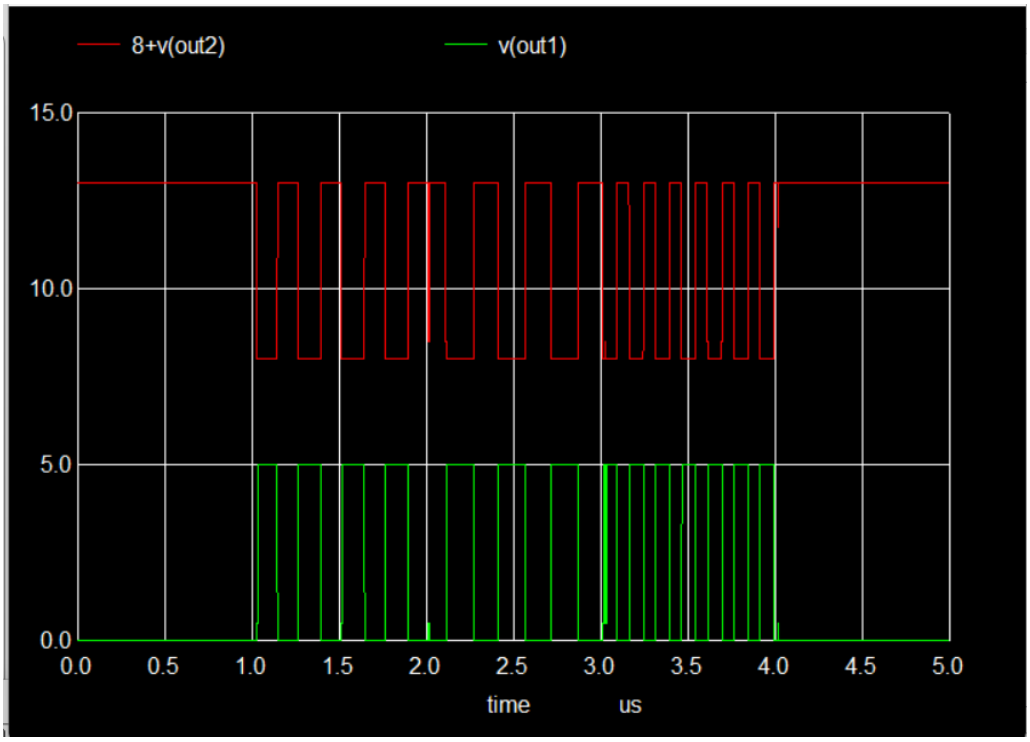

Figure 3.55: Output Graph of 74HCT151

Chapter 4

Conclusion and Future Scope

This project successfully demonstrates the comprehensive design and simulation of integrated circuits utilizing the eSim platform. The process encompassed schematic development, component interconnection, and rigorous simulation, culminating in the validation of the circuit's intended functionality. Through this endeavor, a deeper understanding of digital circuit principles and practical experience with an open-source EDA tool were achieved. The project not only reinforces foundational concepts in design but also highlights the significance of accessible simulation environments in fostering innovation and skill development in electronic design automation.

This project highlights the growing importance of open-source EDA tools like eSim, which can be further developed to support more complex designs and automated verification processes, thereby contributing significantly to both educational and industrial domains.

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