Semester-Long Internship Spring 2026

On

Designing Integrated Circuit in eSim

Submitted by

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Chapter 1

Introduction

FOSSEE (Free/Libre and Open Source Software for Education) project promotes the use of FLOSS tools to improve the quality of education in our country. It aims to reduce dependency on proprietary software in educational institutions. It encourages the use of FLOSS tools through various activities to ensure commercial software is replaced by equivalent FLOSS tools. It also develops new FLOSS tools and upgrade existing tools to meet requirements in academia and research.

The FOSSEE project is part of the National Mission on Education through Information and Communication Technology (ICT), Ministry of Human Resource Development (MHRD), Government of India.

1.1 eSim

eSim is a CAD tool that helps electronic system designers to design, test, and analyze their circuits. The important feature of this tool is that it is open source, allowing users to modify the source as per their needs. The software provides a generic, modular, and extensible platform for experimenting with electronic circuits. eSim is built using various free/libre and open-source software components including:

1.1.1 Kicad

Integrated software where all functions of circuit drawing, control, layout, library management, and access to the PCB design software are carried out.

1.1.2 Ngspice

Ngspice is a general-purpose circuit simulation program for nonlinear dc, nonlinear transient, and linear ac analysis.

1.1.3 KiCad to Ngspice converter

Analysis parameters, source details are provided through this module. It allows us to add and edit the device models and subcircuits included in the circuit schematic.

1.1.4 Subcircuit Builder

This module allows the user to create a subcircuit for a component. Once the subcircuit for a component is created, the user can use it in other circuits.

1.1.5 NGHDL

A module for mixed signal circuit simulation, is also integrated with eSim. It makes use of VHDL code.

1.1.6 NgVeri

NgVeri, a module for mixed signal circuit simulation, is also integrated with eSim. It makes use of Verilog/System Verilog/Transaction-Level Verilog code.

1.1.7 Makerchip

Makerchip is a cloud-based browser application developed by Redwood EDA to do digital circuit design. One can simulate Verilog/SystemVerilog/Transaction-Level Verilog code in Makerchip.

Chapter 2

Abstract

The objective of this internship was to design and develop various integrated circuits using the Subcircuit Builder Method in eSim. This involved modeling the ICs with eSim library files and subsequently simulating them with different circuits. The goal was to expand the eSim Subcircuit Library for future use, enhancing its utility and application in educational and practical scenarios.

2.1 Approach

- Identify and research an integrated circuit (IC) that is not currently available in the eSim library.
- Obtain and study the datasheet of the selected IC thoroughly.
- Carefully examine the schematic provided in the datasheet.
- Accurately recreate the schematic in eSim using the Subcircuit Builder Method.
- Model the IC in eSim, ensuring all parameters and configurations match those in the datasheet.
- Simulate the integrated circuit within eSim, testing it with various circuits to verify its functionality.
- Document the process and results to contribute to the future use and expansion of the eSim Subcircuit Library.

Chapter 3

Integrated Circuit Design

3.1 μA107

3.1.1 Description

The μA107 is a general-purpose operational amplifier developed using the Fairchild Planar epitaxial process technology. These ICs are designed to provide improved accuracy, low noise, low offset voltage, and very low input current compared to earlier operational amplifiers such as the μA709 and μA741. The devices are internally compensated for stable operation and are suitable for high impedance applications. They can be used in integrators, sample-and-hold circuits, slow ramp generators, voltage followers, and amplifier circuits. The μA107 series also offers excellent temperature stability and reliable performance over a wide operating temperature range.

Features Of μA107

- **Low Input Current:** Suitable for high impedance applications and precision circuits.
- **Low Offset Voltage:** Provides better accuracy and stable amplifier operation.
- **Internal Frequency Compensation:** Ensures stable performance without requiring external compensation components.

3.1.2 Pin Diagram

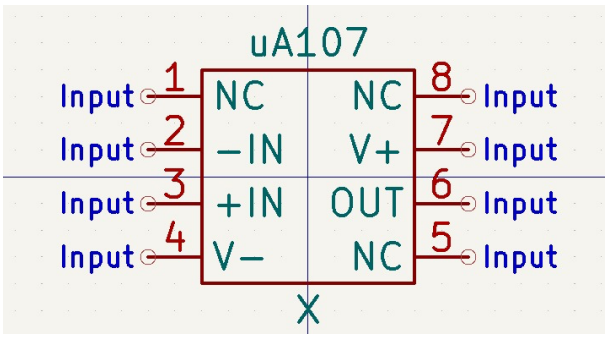

Figure 3.1: Pin Diagram of μA107

3.1.3 Sub-Circuit Diagram

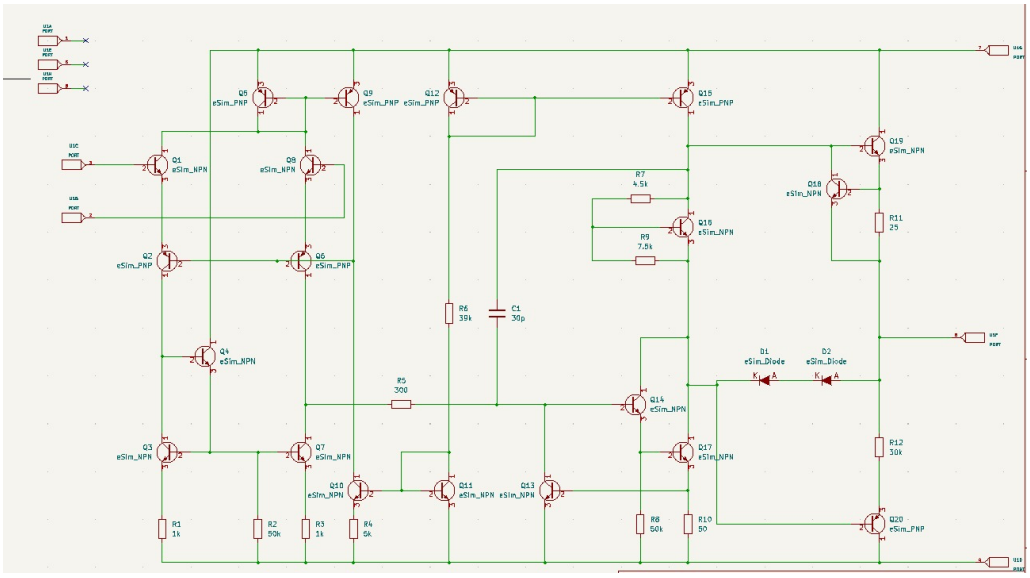

Figure 3.2: Sub-Circuit of μA107

3.1.4 Test-Circuit Diagram

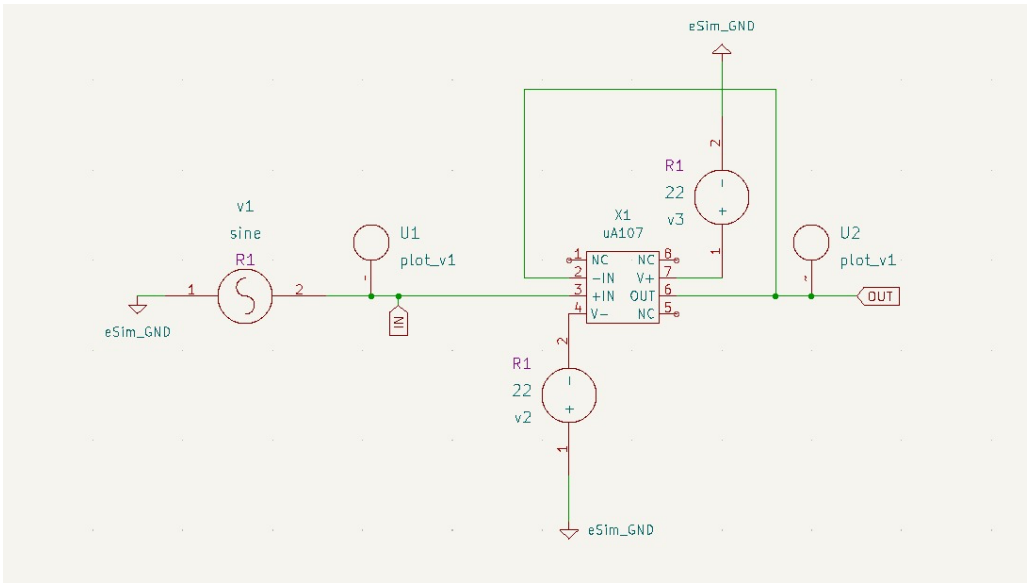

Figure 3.3: Test Circuit of μA107

3.1.5 NgSpice Plot

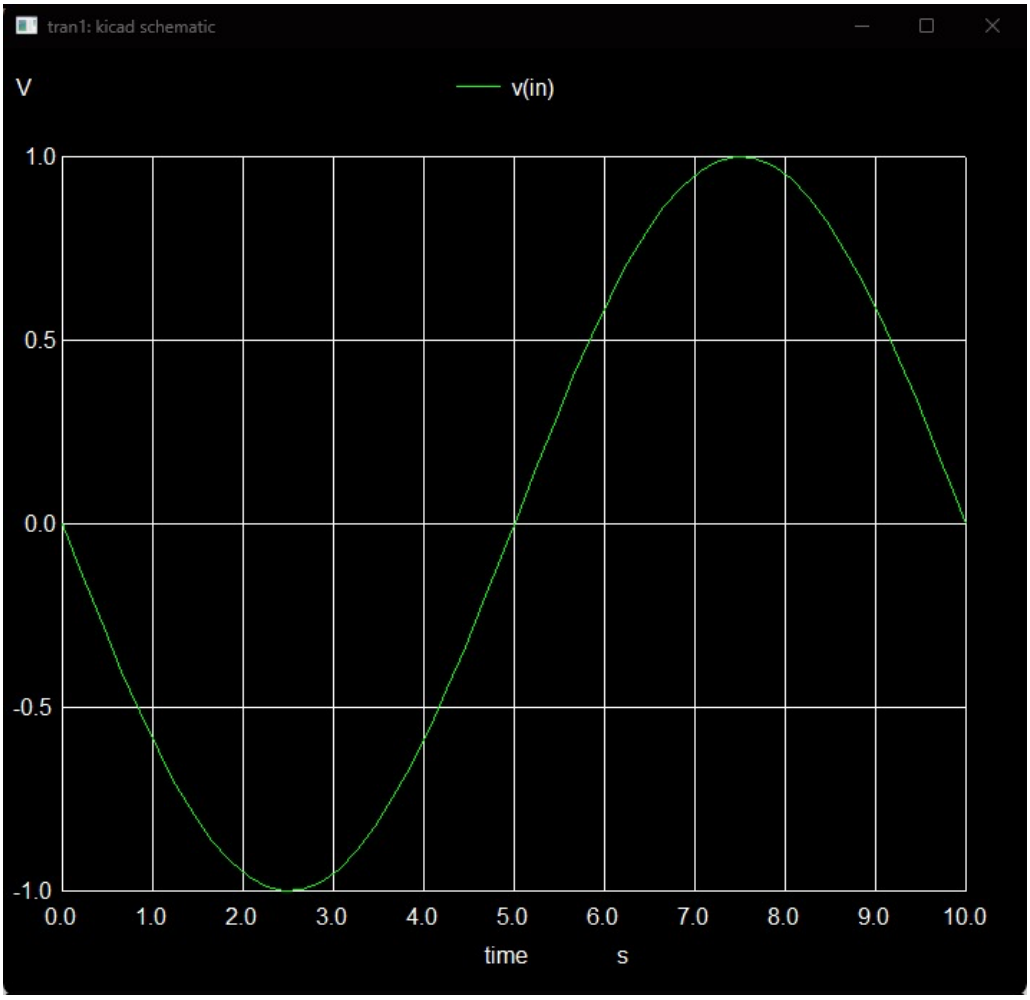

Figure 3.4: Input Graph of μA107

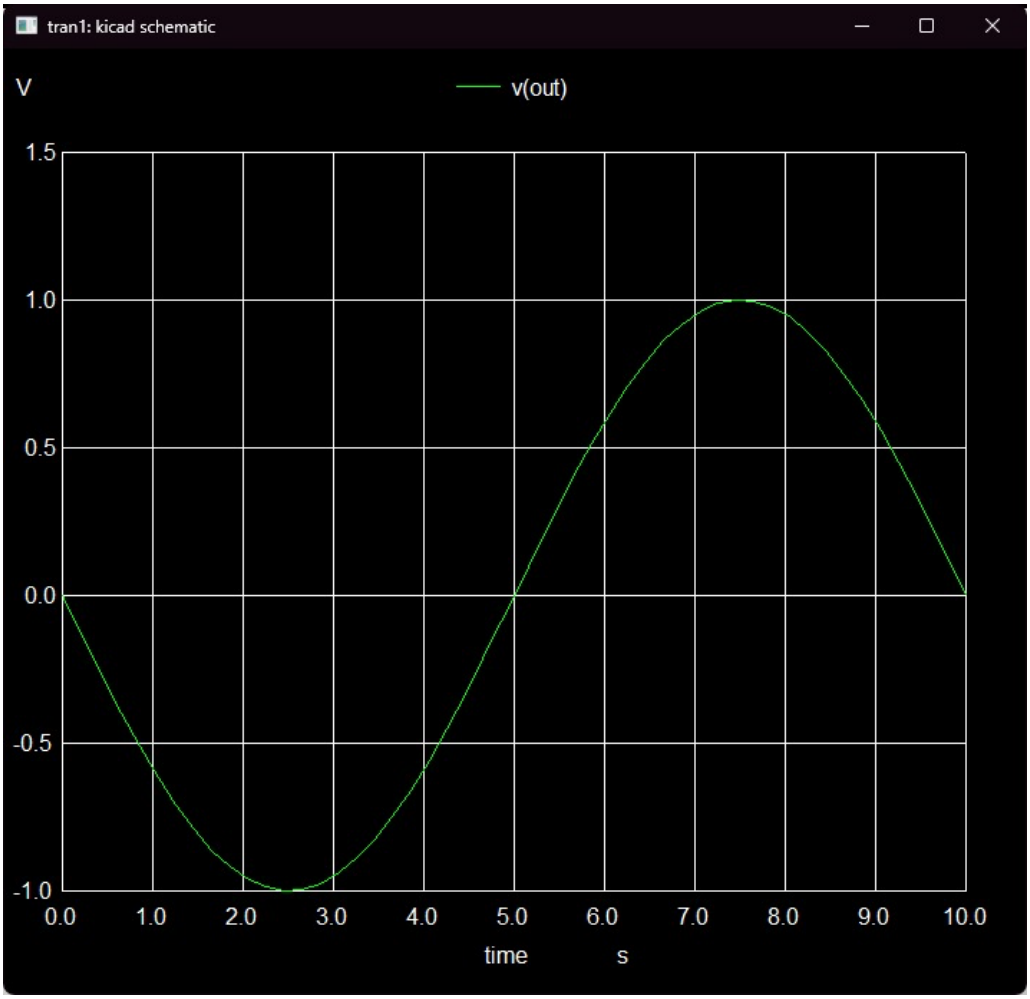

Figure 3.5: Output Graph of μA107

3.2 μA799

3.2.1 Description

The μA799 is a monolithic operational amplifier designed for general-purpose analog applications. It is internally frequency compensated for stable operation over a wide range of supply voltages. The device offers high gain, low power consumption, and a wide common mode input range that includes ground or negative supply voltage. It is suitable for amplifiers, filters, oscillators, comparators, and signal processing circuits.

Features Of μA799

- **Wide Operating Voltage Range:** Supports single supply operation from 3V to 36V and dual supply operation up to $\pm$18V.
- **Internally Compensated:** Provides stable operation without requiring external compensation components.
- **Low Power Consumption:** Consumes very low supply current for efficient circuit operation.

3.2.2 Pin Diagram

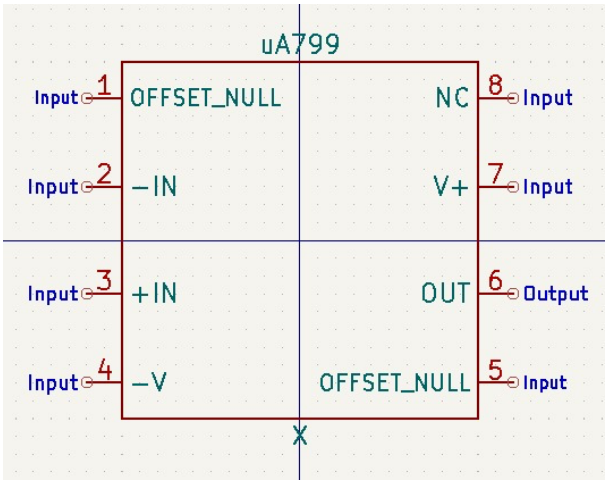

Figure 3.6: Pin Diagram of μA799

3.2.3 Sub-Circuit Diagram

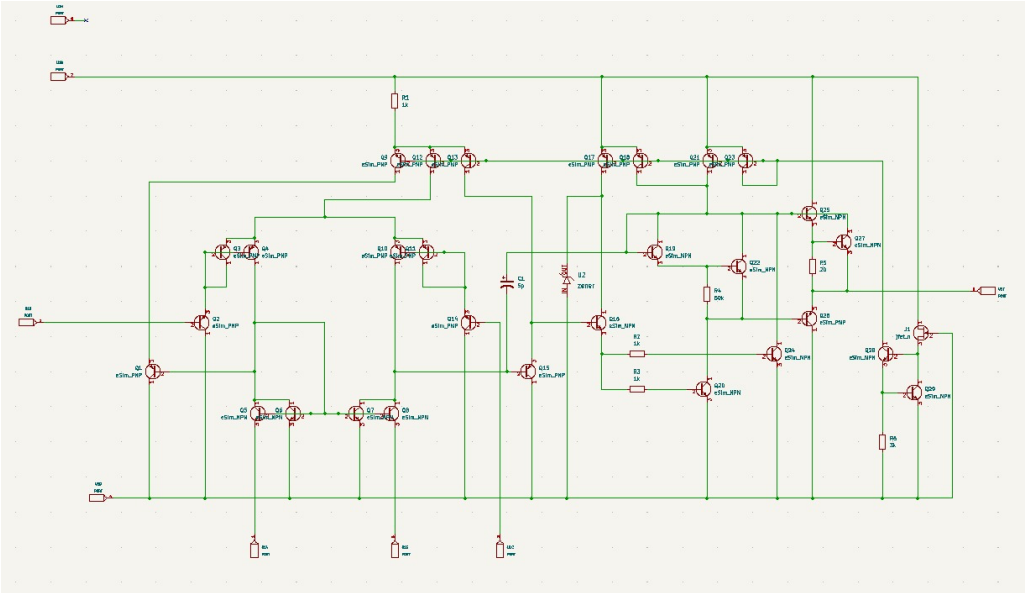

Figure 3.7: Sub-Circuit of μA799

3.2.4 Test-Circuit Diagram

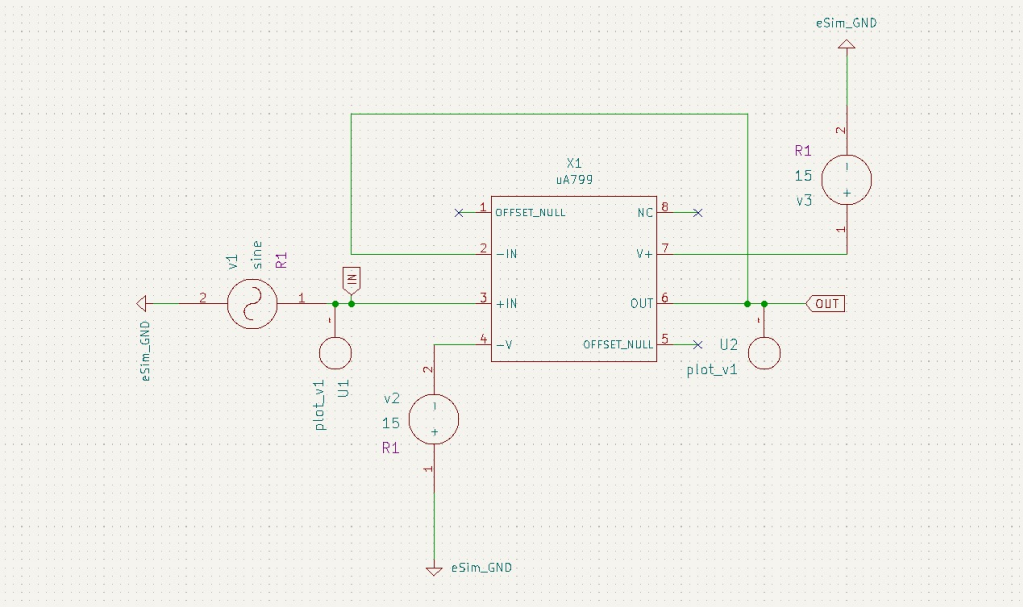

Figure 3.8: Test Circuit of μA799

3.2.5 NgSpice Plot

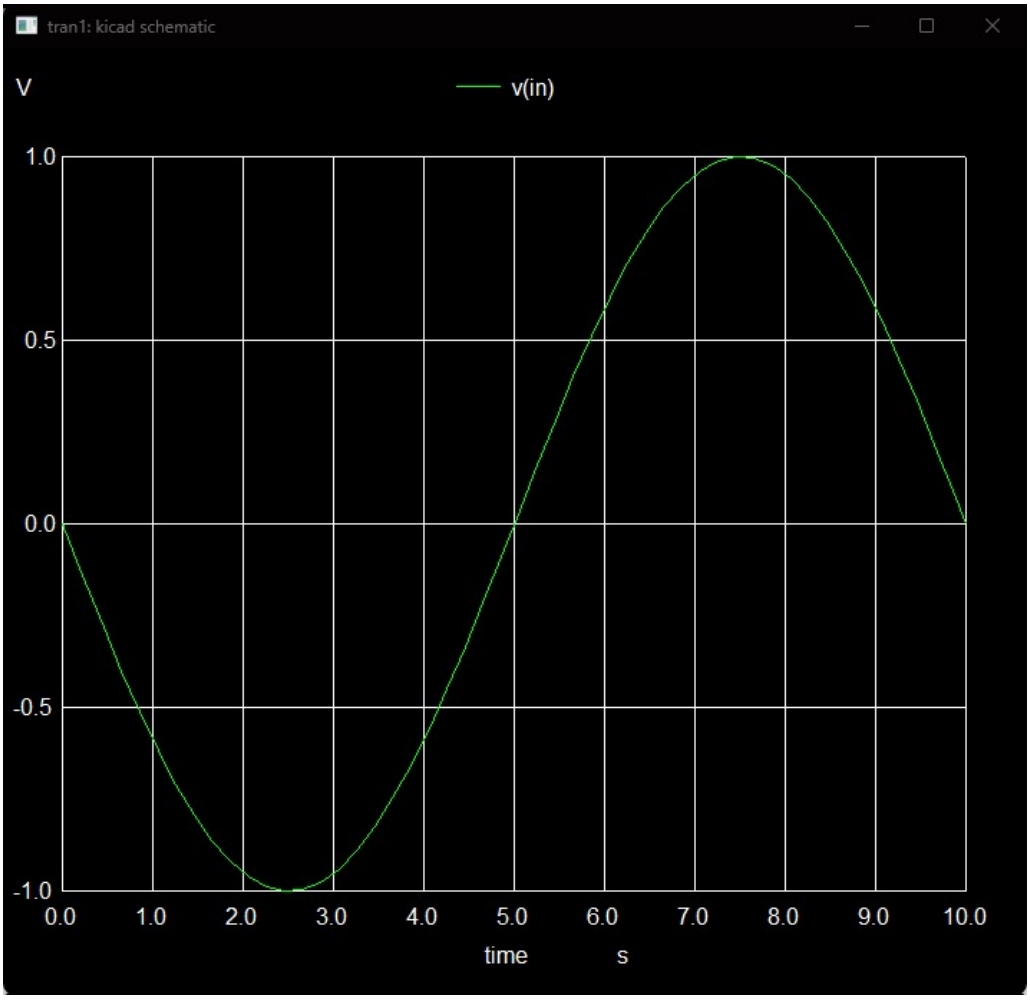

Figure 3.9: Input Graph of μA799

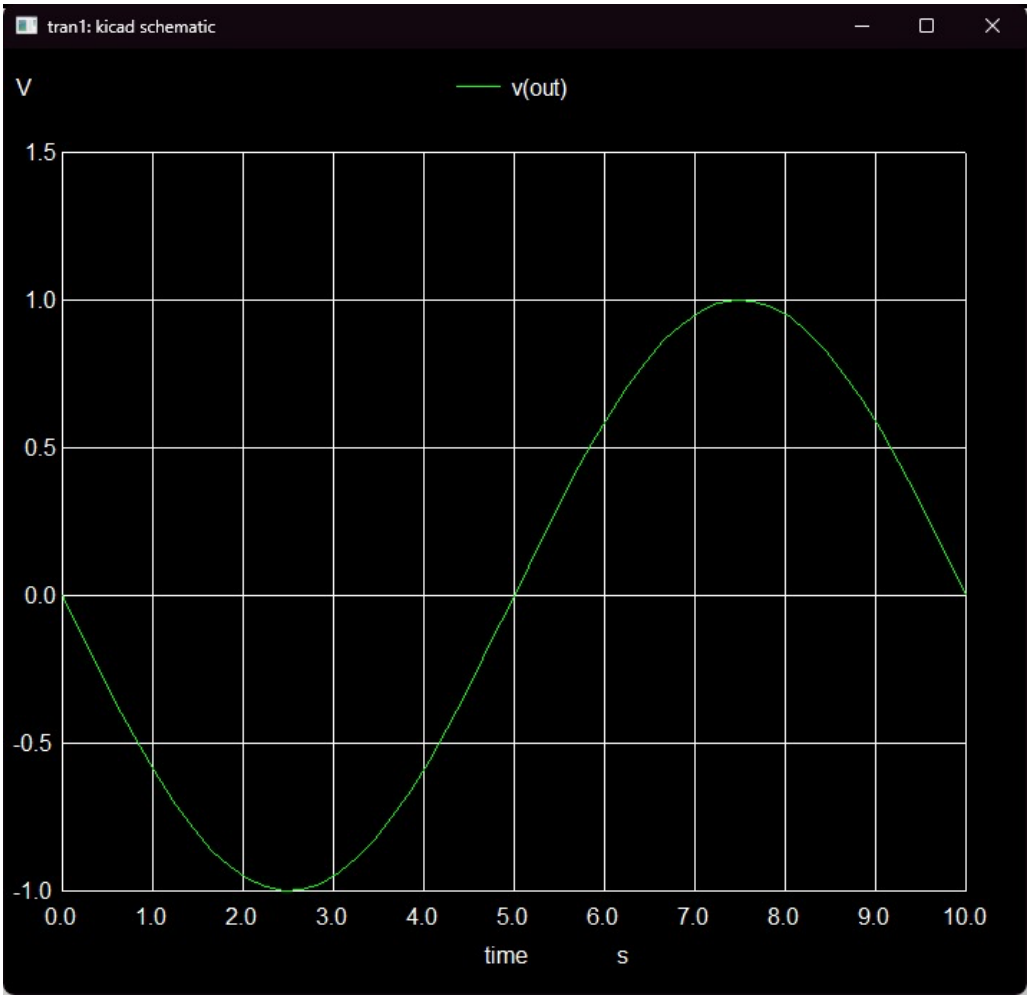

Figure 3.10: Output Graph of μA799

3.3 μA740

3.3.1 Description

The μA740 is a high performance FET input operational amplifier designed for analog applications requiring very high input impedance and low input bias current. It provides high slew rate, wide operating voltage range, and stable operation without external frequency compensation. The device is suitable for voltage followers, active filters, integrators, sample-and-hold circuits, and general amplifier applications.

Features Of μA740

- **High Input Impedance:** Very high input impedance of about 1,000,000 MΩ makes it suitable for high impedance circuits.
- **No Frequency Compensation Required:** Internally compensated for stable closed-loop operation without external components.
- **Short Circuit Protection:** Output is protected against short circuit conditions for reliable operation.

3.3.2 Pin Diagram

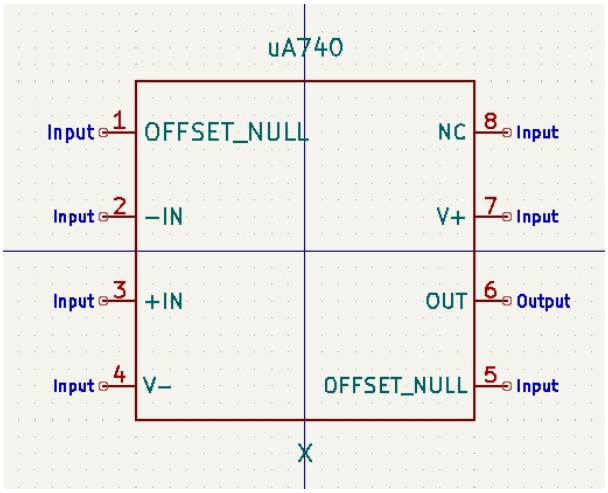

Figure 3.11: Pin Diagram of μA740

3.3.3 Sub-Circuit Diagram

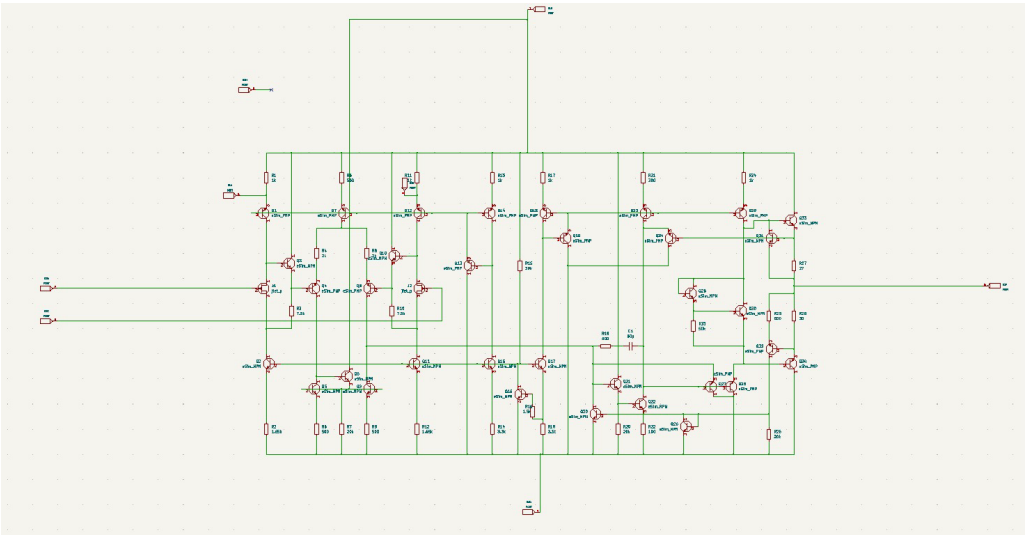

Figure 3.12: Sub-Circuit of μA740

3.3.4 Test-Circuit Diagram

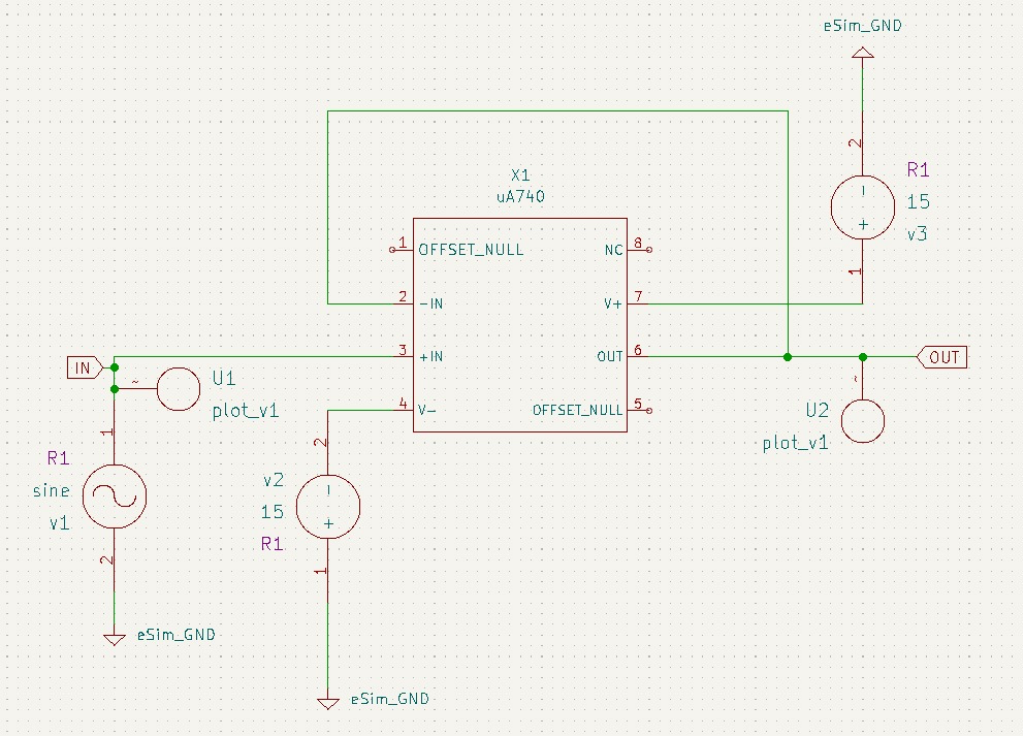

Figure 3.13: Test Circuit of μA740

3.3.5 NgSpice Plot

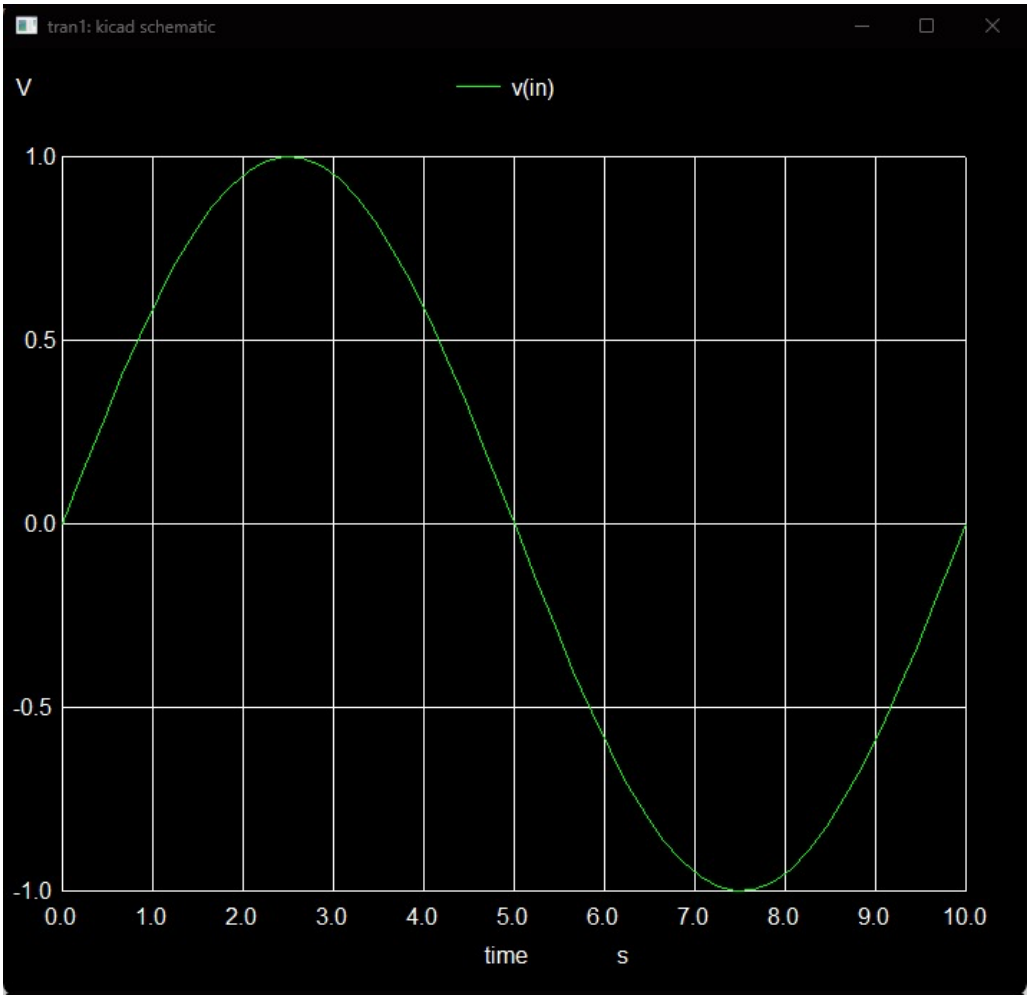

Figure 3.14: Input Graph of μA740

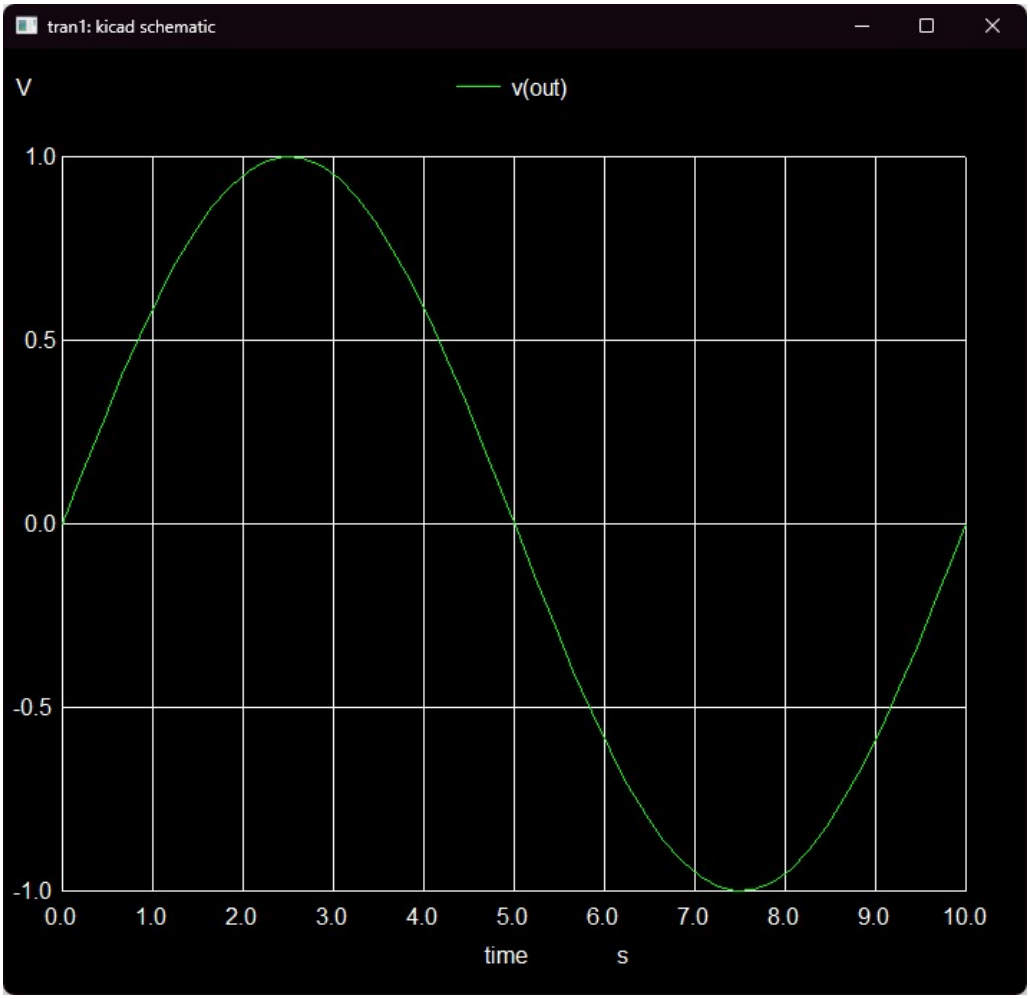

Figure 3.15: Output Graph of μA740

3.4 μA798

3.4.1 Description

The μA798 is a dual operational amplifier containing two independent high gain internally frequency compensated operational amplifiers in a single package. It is designed for operation with single or dual power supplies and provides wide operating voltage range, high gain, and low power consumption. The device is suitable for filters, oscillators, comparators, and general analog applications.

Features Of μA798

- **Dual Operational Amplifiers:** Contains two independent op-amps in a single IC package.
- **Wide Supply Voltage Range:** Supports single supply from 3V to 36V and dual supply up to ±18V.
- **Internally Compensated:** Provides stable operation without external frequency compensation.

3.4.2 Pin Diagram

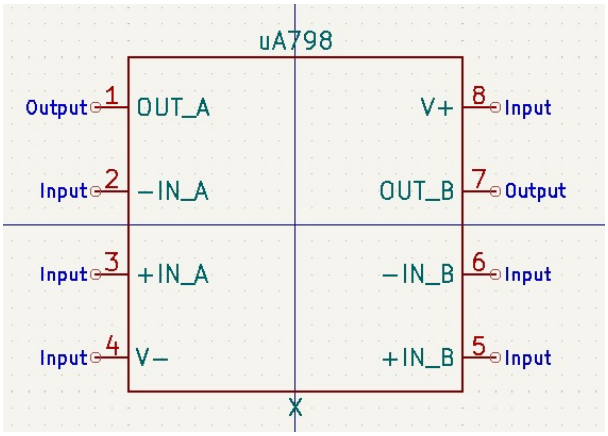

Figure 3.16: Pin Diagram of μA798

3.4.3 Sub-Circuit Diagram

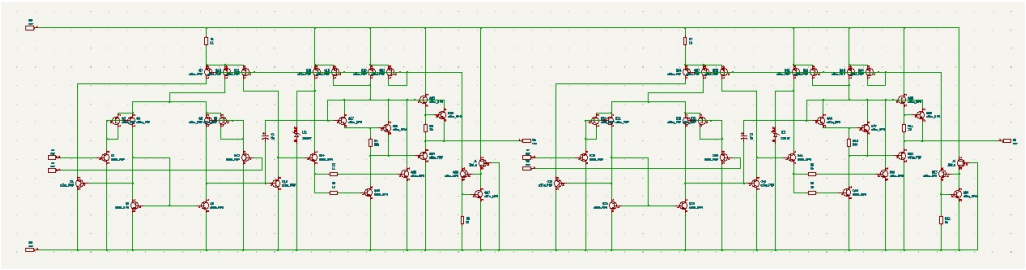

Figure 3.17: Sub-Circuit of μA798

3.4.4 Test-Circuit Diagram

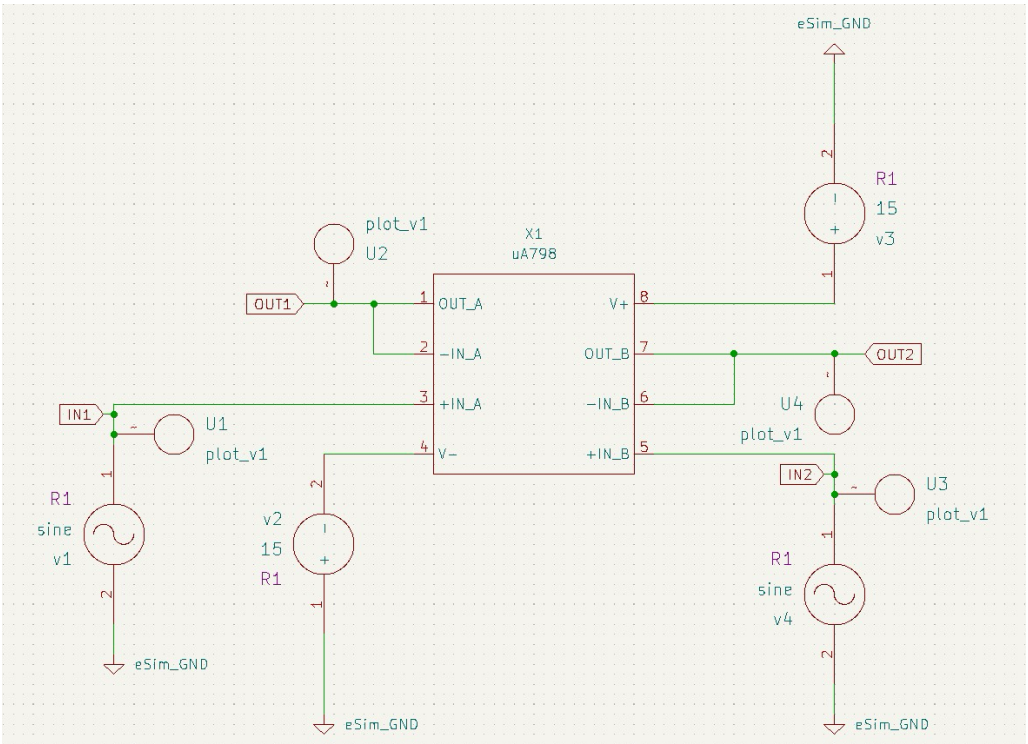

Figure 3.18: Test Circuit of μA798

3.4.5 NgSpice Plot

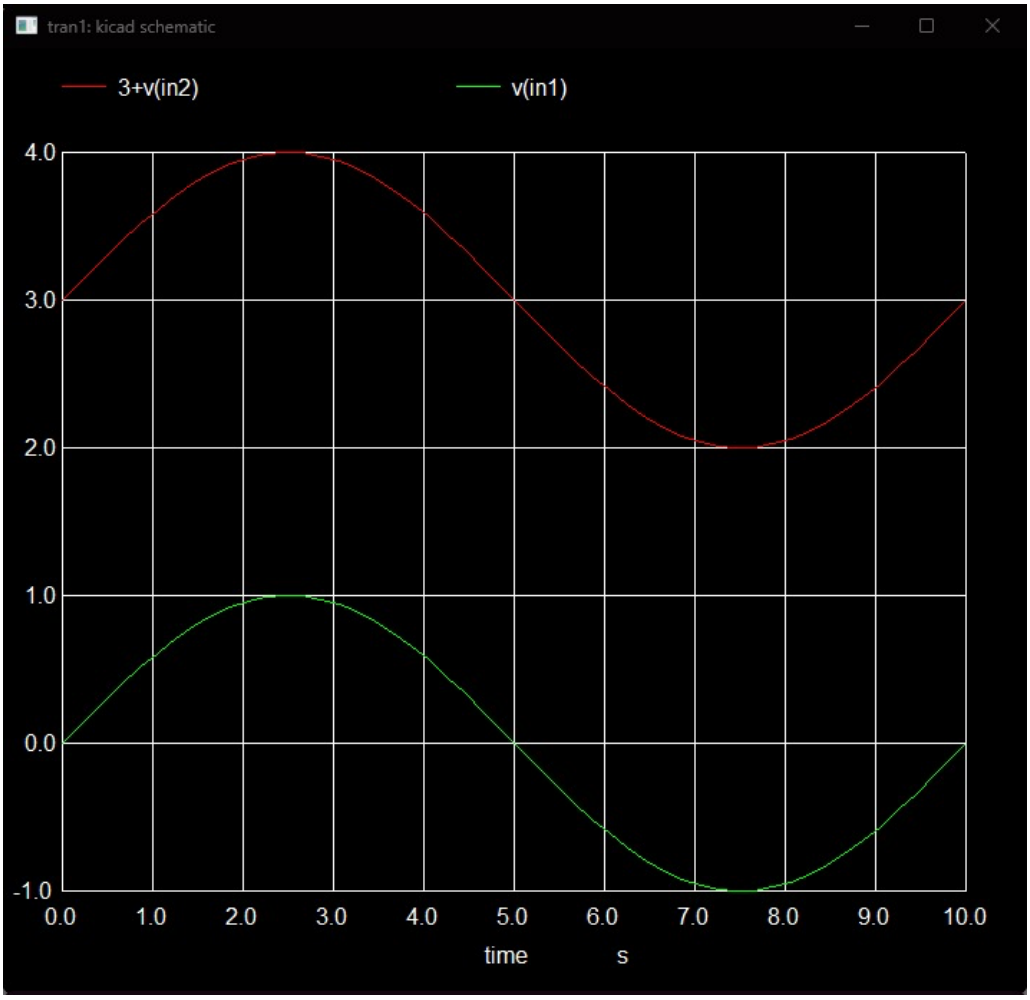

Figure 3.19: Input Graph of μA798

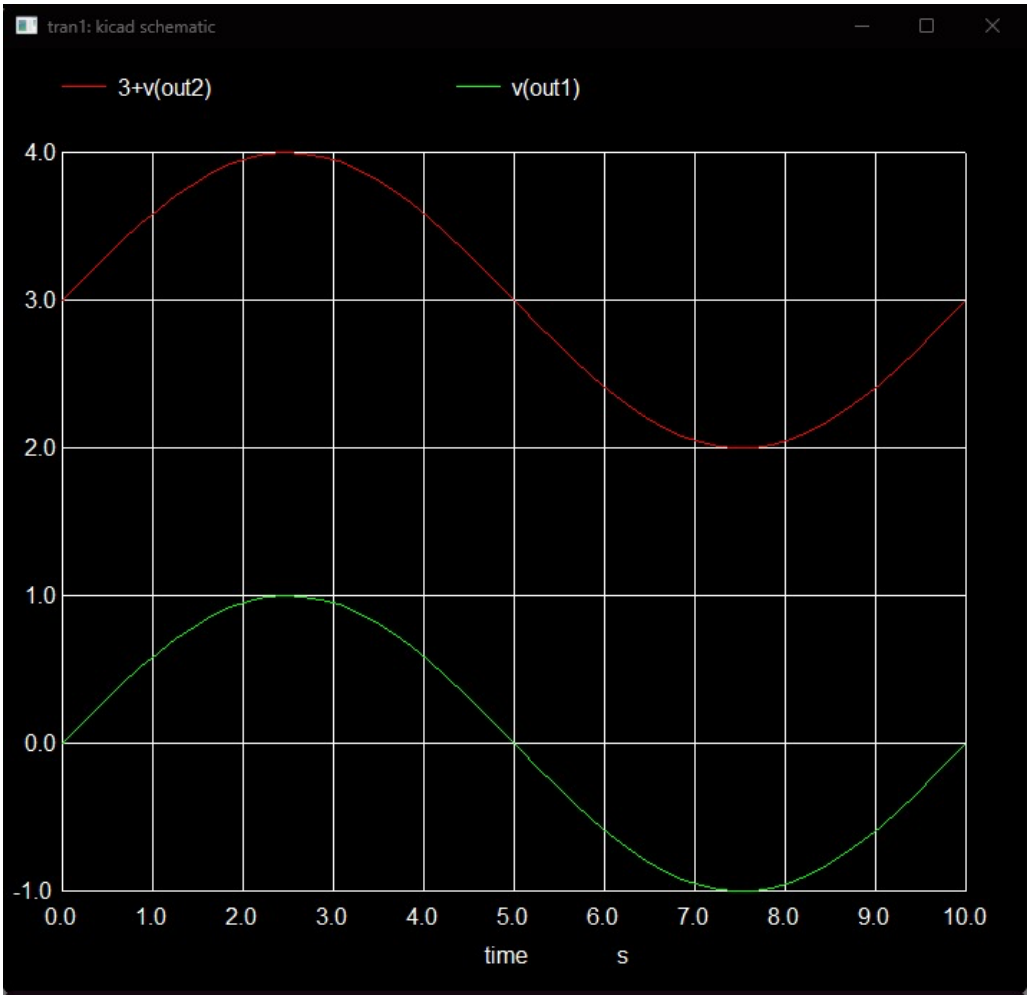

Figure 3.20: Output Graph of μA798

3.5 μA747

3.5.1 Description

The μA747 is a dual frequency-compensated operational amplifier containing two high performance operational amplifiers in a single package. It is designed for analog applications where compact size, high gain, and stable operation are required. The device provides wide operating voltage range, short circuit protection, and requires no external frequency compensation components.

Features Of μA747

- **Dual Operational Amplifiers:** Contains two independent operational amplifiers in one IC package.
- **No Frequency Compensation Required:** Internally frequency compensated for stable closed-loop operation.
- **Short Circuit Protection:** Output is protected against short circuit conditions for reliable performance.

3.5.2 Pin Diagram

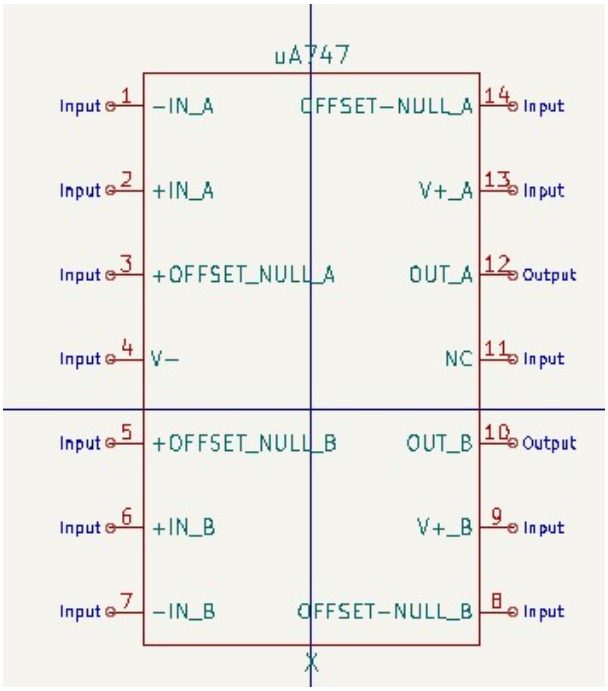

Figure 3.21: Pin Diagram of μA747

3.5.3 Sub-Circuit Diagram

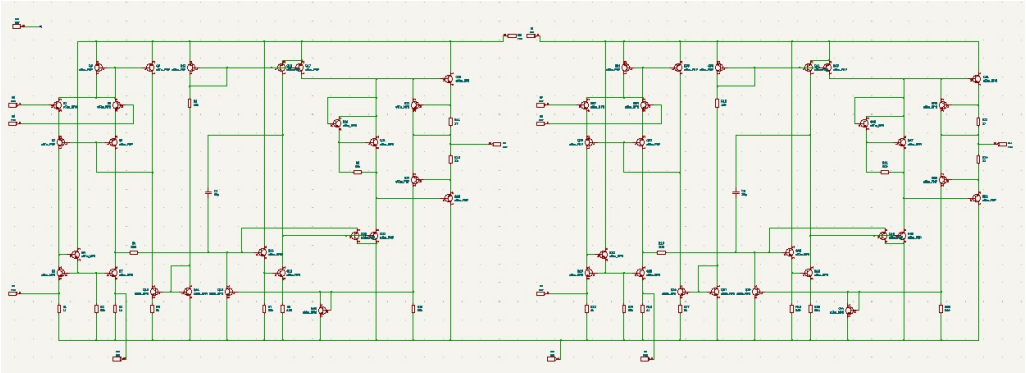

Figure 3.22: Sub-Circuit of μA747

3.5.4 Test-Circuit Diagram

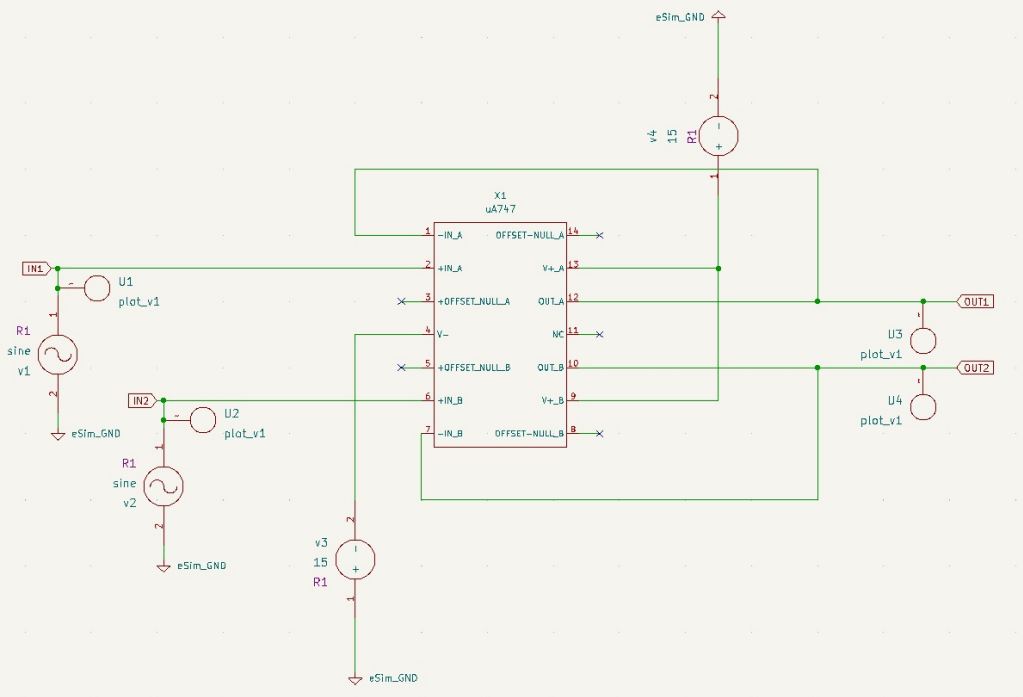

Figure 3.23: Test Circuit of μA747

3.5.5 NgSpice Plot

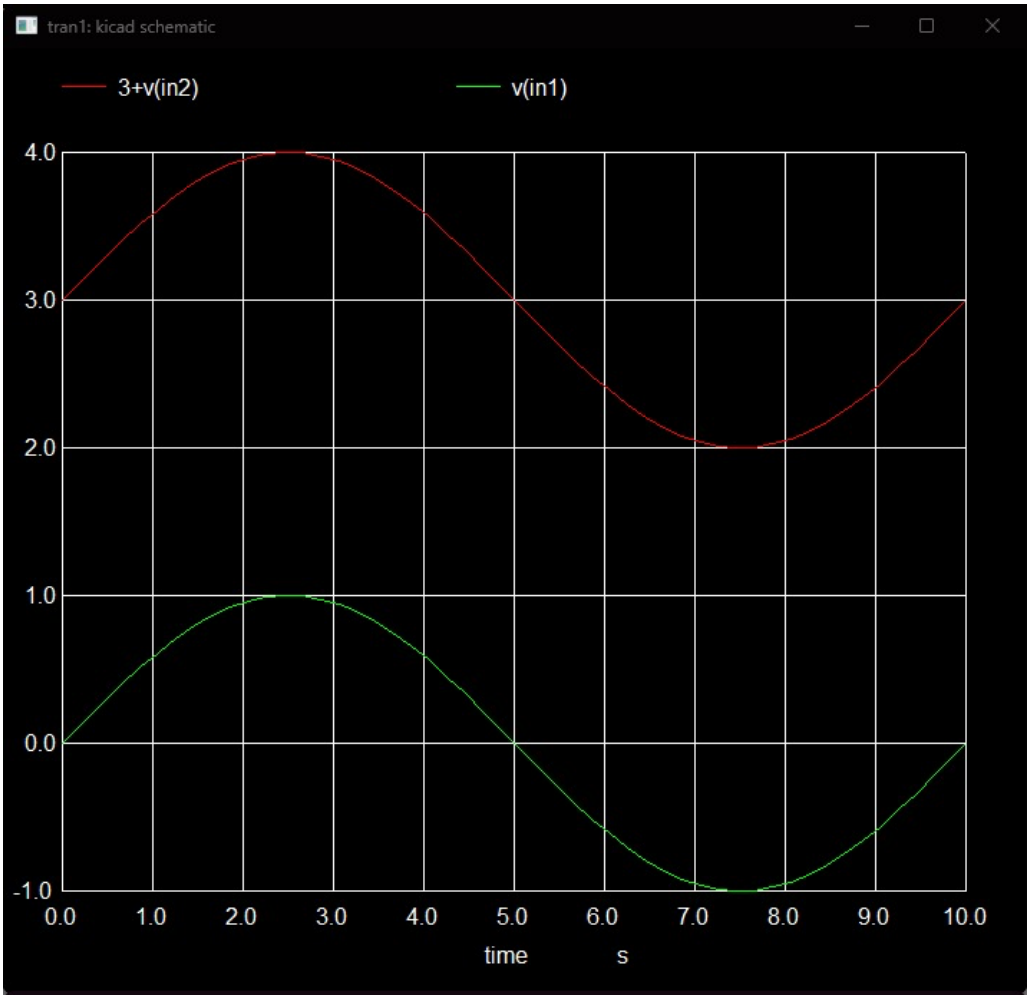

Figure 3.24: Input Graph of μA747

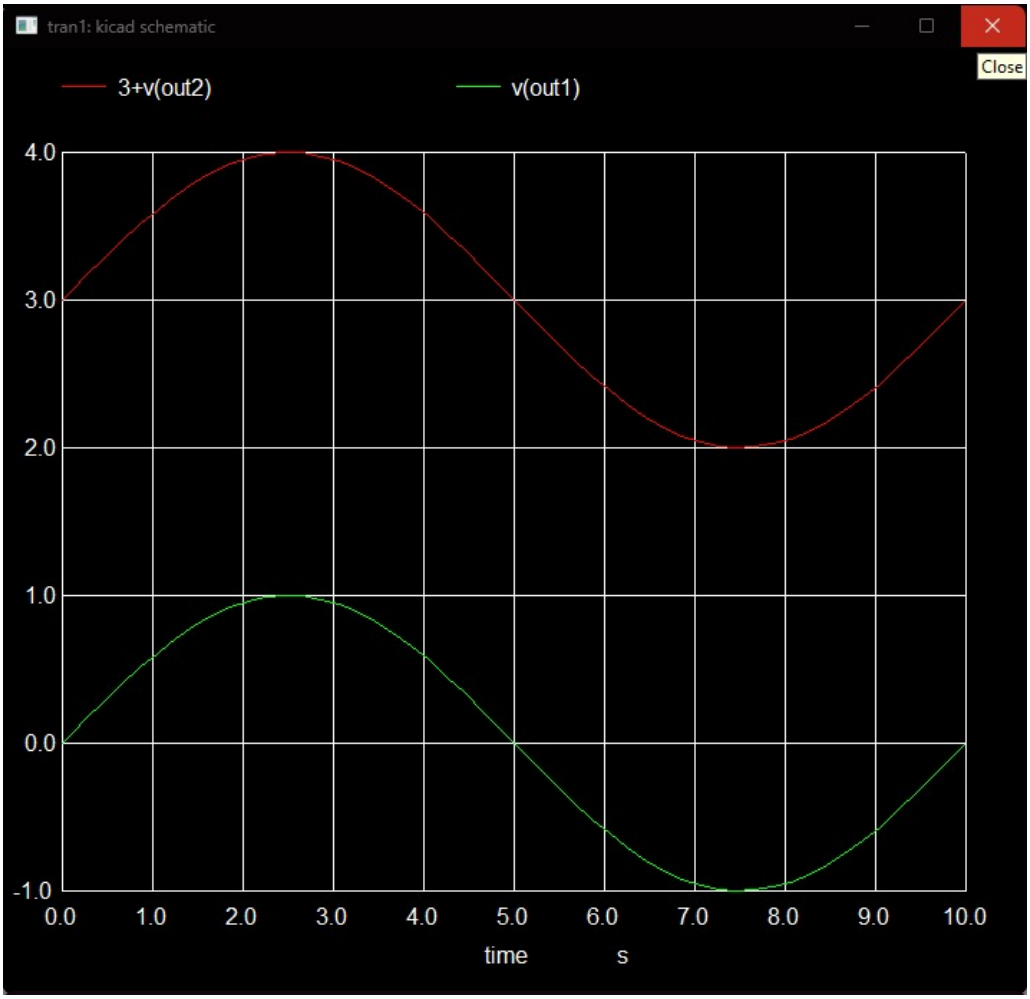

Figure 3.25: Output Graph of μA747

3.6 μA748

3.6.1 Description

The μA748 is a precision single operational amplifier designed for general purpose analog applications. It provides low offset voltage, low power consumption, and stable operation with frequency compensation. The device offers short circuit protection, wide common mode voltage range, and reliable performance in amplifier and comparator applications.

Features Of μA748

- **Low Offset Voltage:** Maximum input offset voltage of 3 mV over temperature range.
- **Frequency Compensation:** Stable operation using a single 30 pF compensation capacitor.
- **Short Circuit Protection:** Continuous output short circuit protection for reliable operation.

3.6.2 Pin Diagram

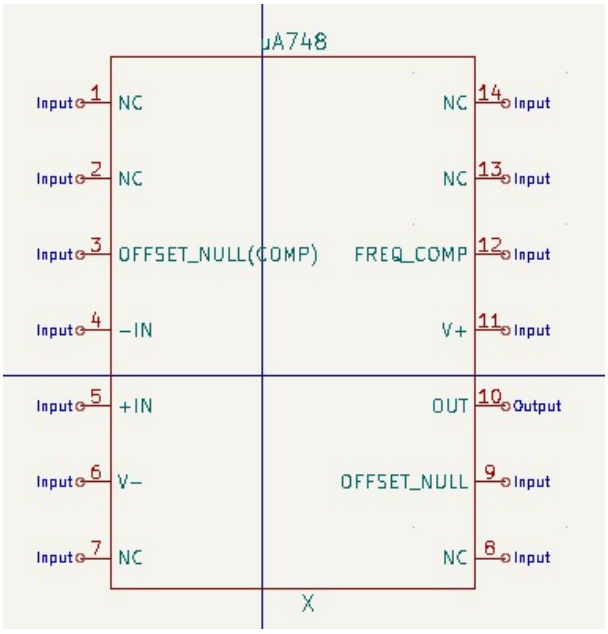

Figure 3.26: Pin Diagram of μA748

3.6.3 Sub-Circuit Diagram

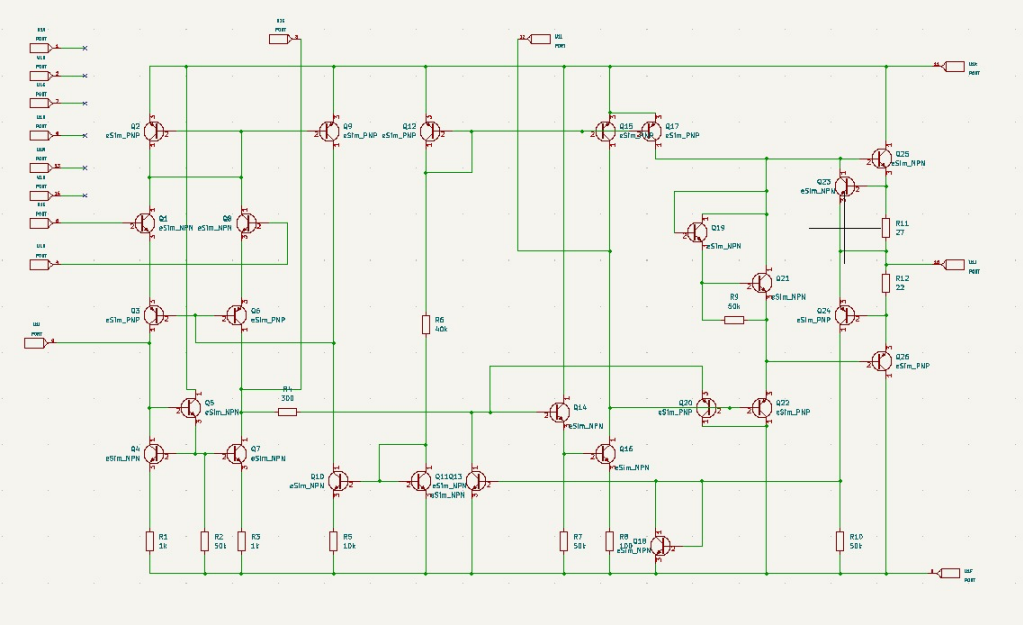

Figure 3.27: Sub-Circuit of μA748

3.6.4 Test-Circuit Diagram

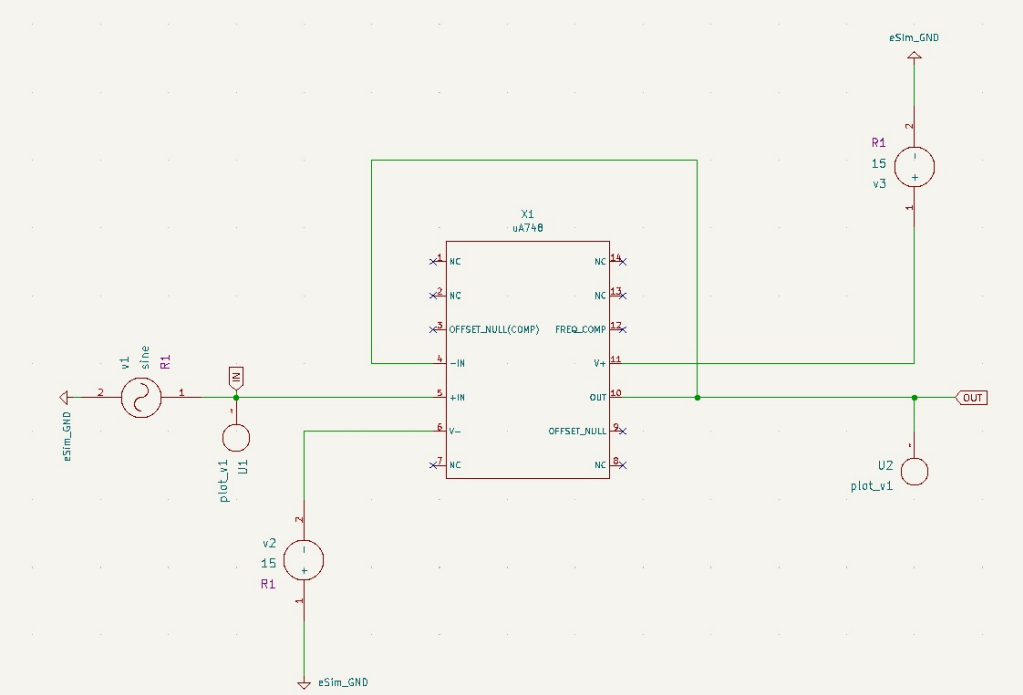

Figure 3.28: Test Circuit of μA748

3.6.5 NgSpice Plot

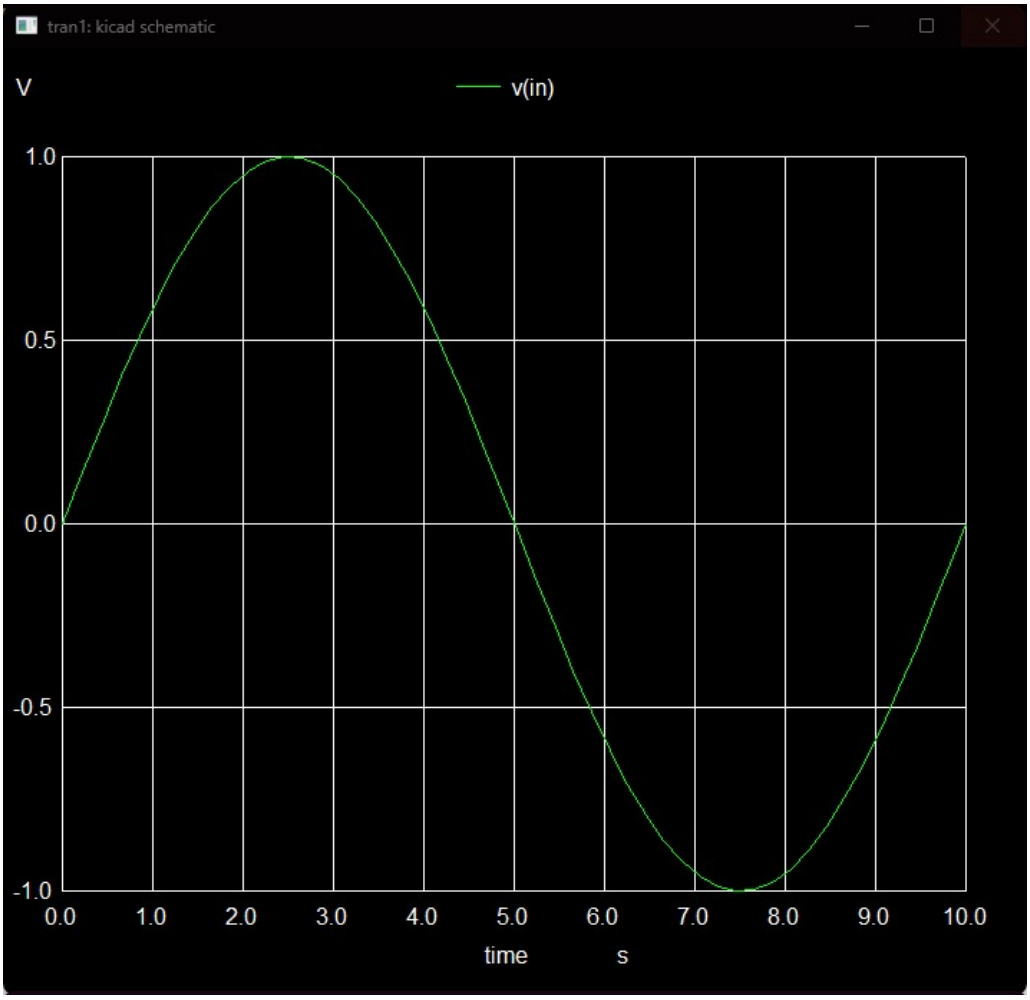

Figure 3.29: Input Graph of μA748

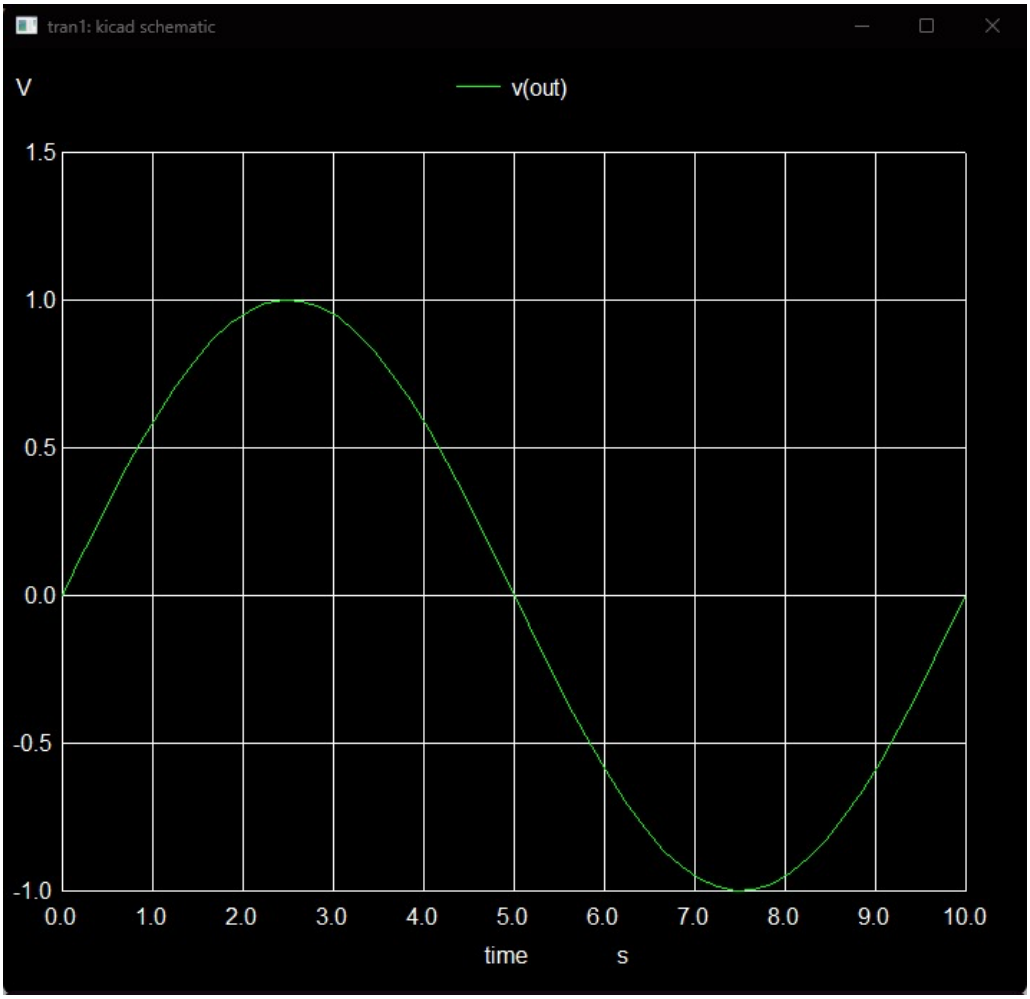

Figure 3.30: Output Graph of μA748

3.7 CD4072B

3.7.1 Description

The CD4072B is a CMOS Triple 3-Input OR Gate IC designed for implementing positive logic OR functions in digital electronic circuits. It contains three independent 3-input OR gates in a single package and provides high noise immunity, low power consumption, and reliable CMOS performance over a wide operating voltage range.

Features Of CD4072B

- **Triple 3-Input OR Gates:** Contains three independent 3-input OR gates in a single IC package.
- **Wide Operating Voltage Range:** Operates with supply voltages from 3V to 18V.
- **Low Power Consumption:** CMOS design provides very low quiescent power dissipation.

3.7.2 Pin Diagram

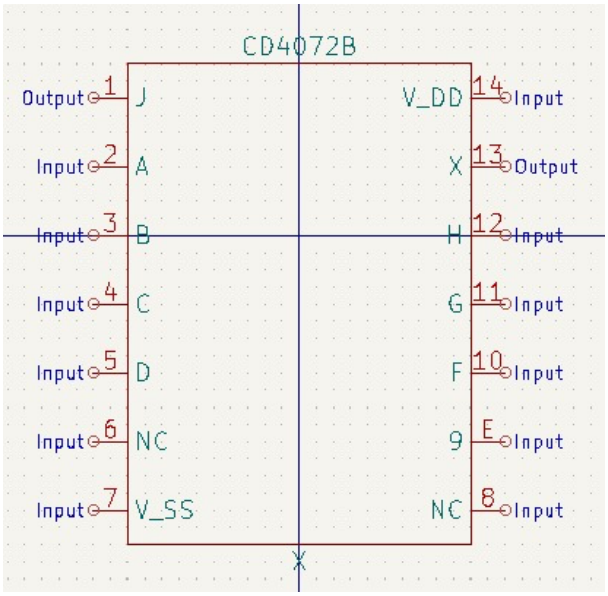

Figure 3.31: Pin Diagram of CD4072B

3.7.3 Sub-Circuit Diagram

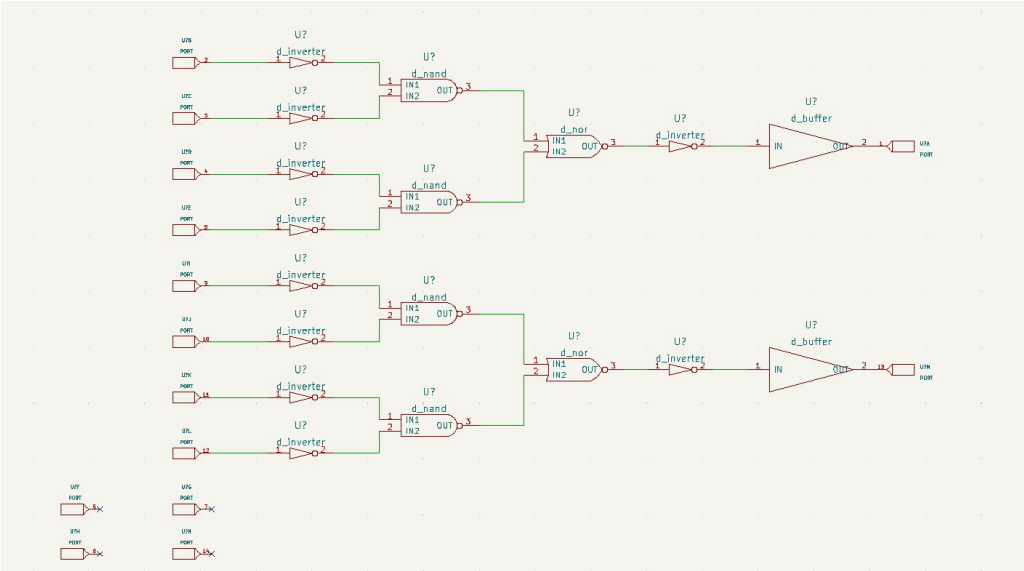

Figure 3.32: Sub-Circuit of CD4072B

3.7.4 Test-Circuit Diagram

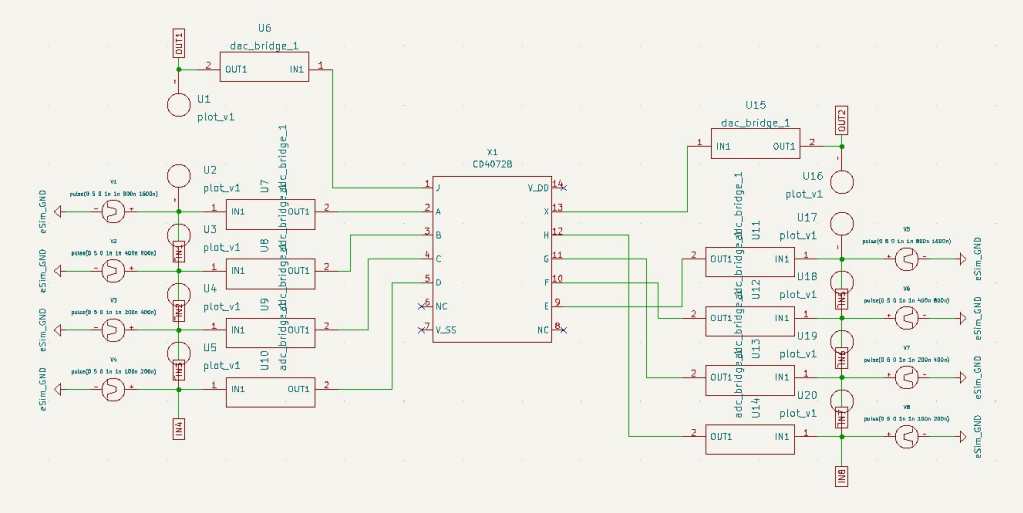

Figure 3.33: Test Circuit of CD4072B

3.7.5 NgSpice Plot

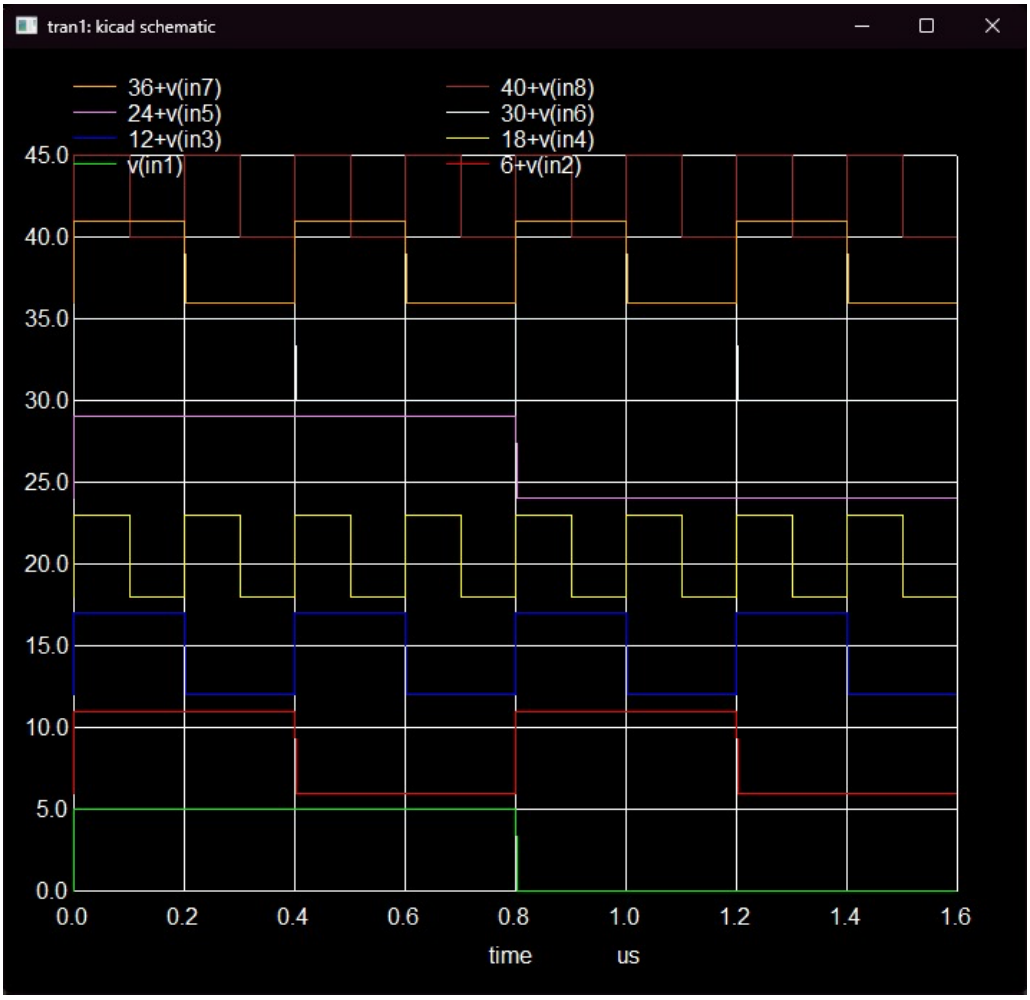

Figure 3.34: Input Graph of CD4072B

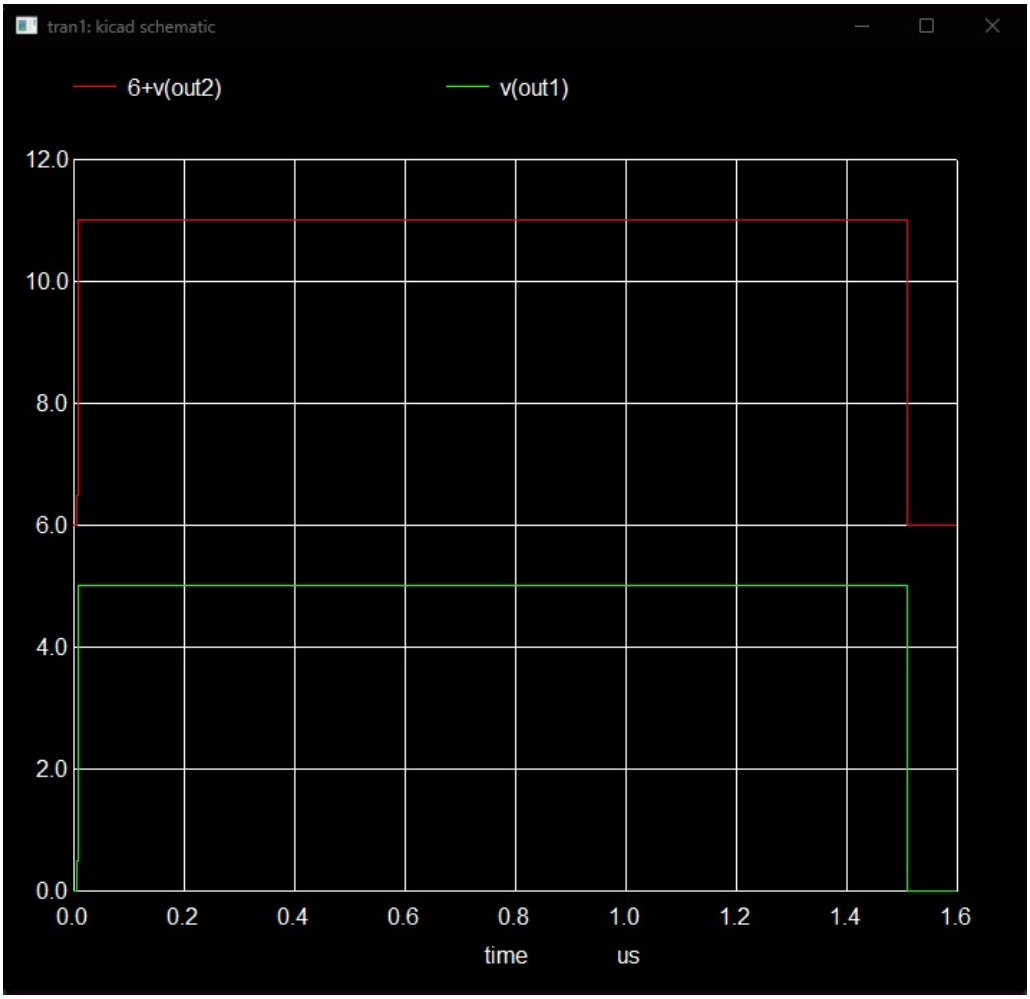

Figure 3.35: Output Graph of CD4072B

3.8 CD4042A

3.8.1 Description

The CD4042A is a CMOS Quad Clocked "D" Latch IC that contains four latch circuits controlled by a common clock signal. It provides complementary Q and $\overline{Q}$ outputs for each latch and supports polarity control for clock operation. The device offers low power consumption, high noise immunity, and reliable CMOS performance for data storage and digital logic applications.

Features Of CD4042A

- **Quad D Latch:** Contains four independent clocked D latch circuits in a single IC.
- **Complementary Outputs:** Provides both Q and $\overline{Q}$ outputs for each latch.
- **Low Power Consumption:** CMOS technology ensures very low quiescent power dissipation.

3.8.2 Pin Diagram

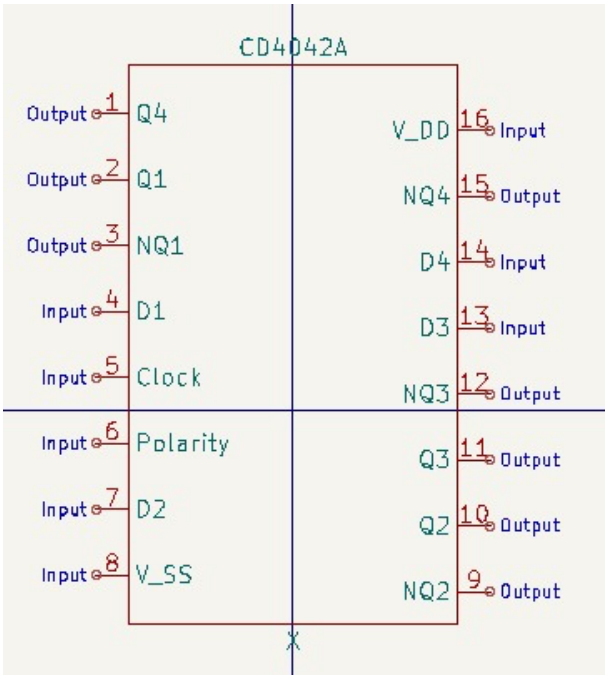

Figure 3.36: Pin Diagram of CD4042A

3.8.3 Sub-Circuit Diagram

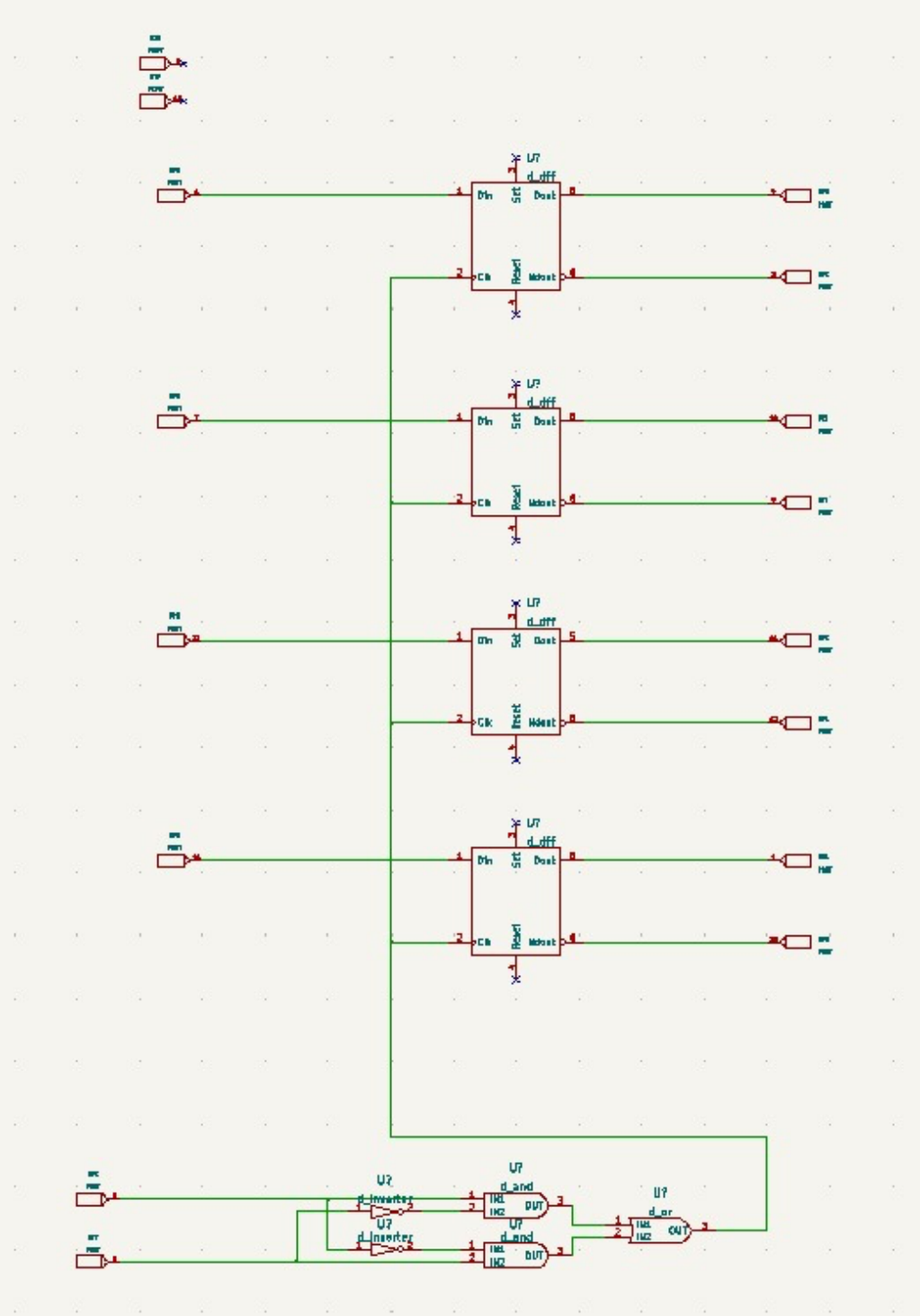

Figure 3.37: Sub-Circuit of CD4042A

3.8.4 Test-Circuit Diagram

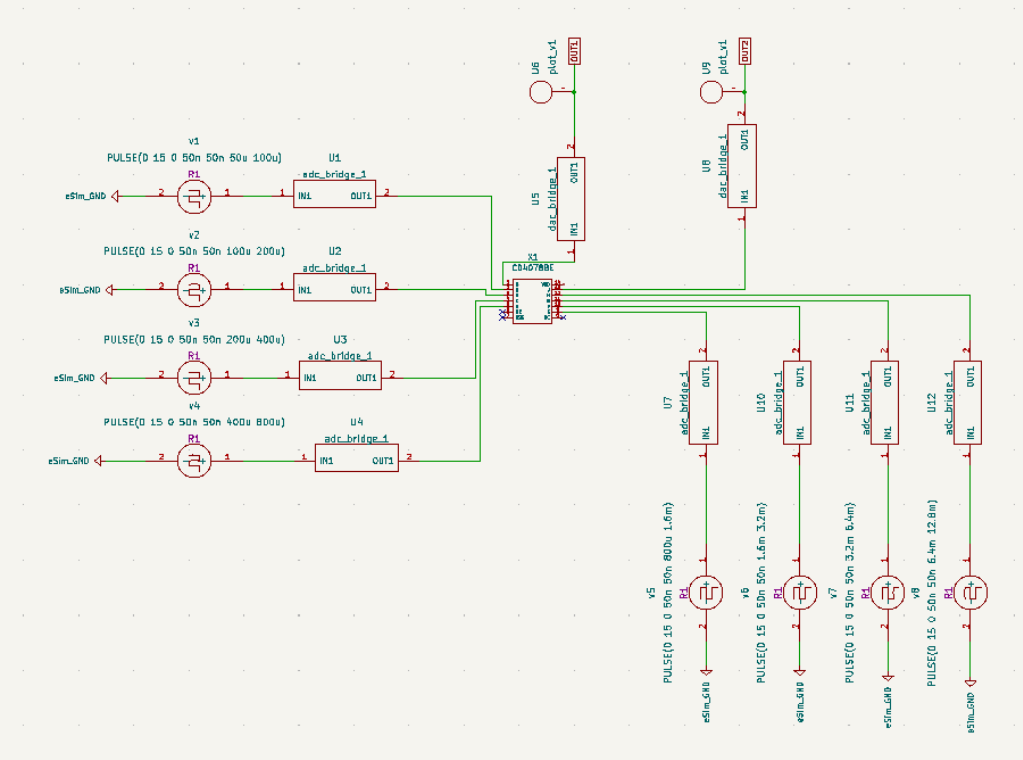

Figure 3.38: Test Circuit of CD4042A

3.8.5 NgSpice Plot

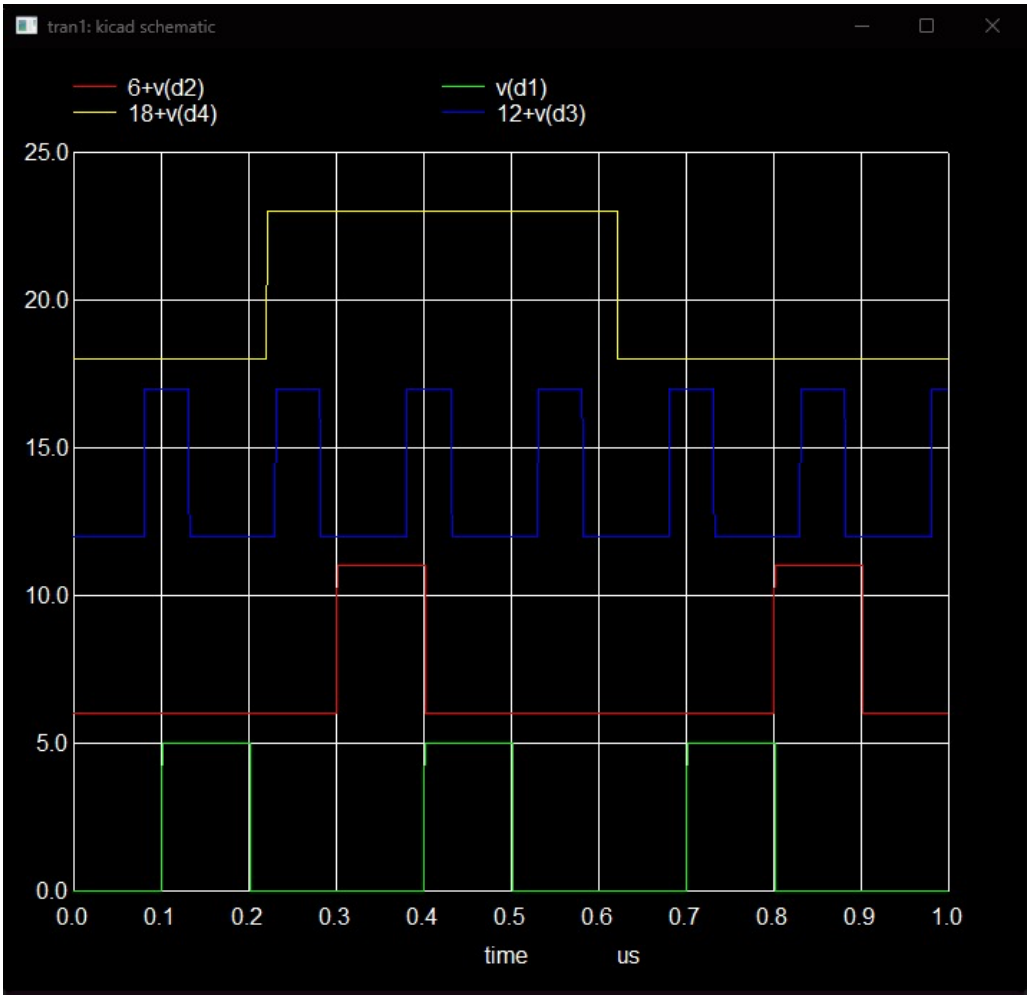

Figure 3.39: Input Graph of CD4042A

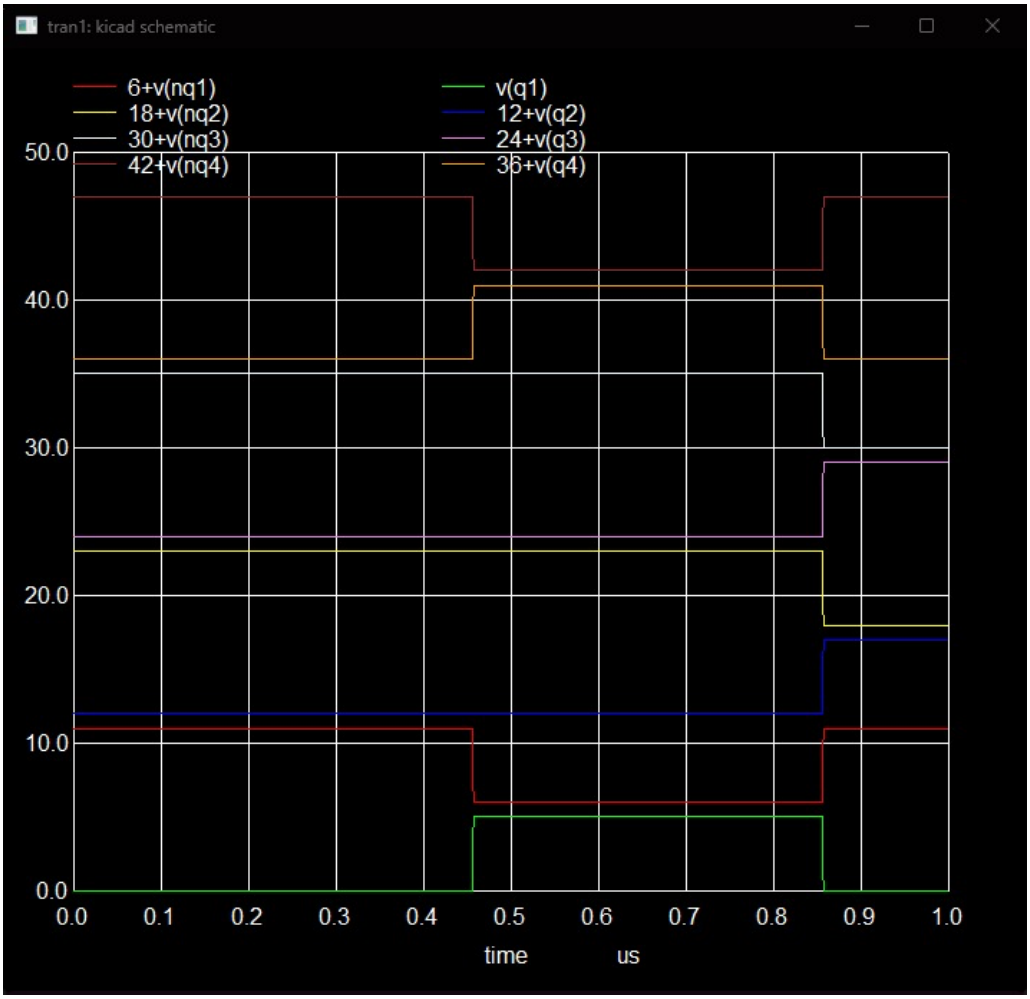

Figure 3.40: Output Graph of CD4042A

Chapter 4

Conclusion and Future Scope

This project successfully demonstrates the comprehensive design and simulation of integrated circuits utilizing the eSim platform. The process encompassed schematic development, component interconnection, and rigorous simulation, culminating in the validation of the circuit's intended functionality. Through this endeavor, a deeper understanding of digital circuit principles and practical experience with an open-source EDA tool were achieved. The project not only reinforces foundational concepts in design but also highlights the significance of accessible simulation environments in fostering innovation and skill development in electronic design automation.

This project highlights the growing importance of open-source EDA tools like eSim, which can be further developed to support more complex designs and automated verification processes, thereby contributing significantly to both educational and industrial domains.

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