



Semester-Long Internship Autumn 2025

On

Designing Integrated Circuit in eSim

Submitted by

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This internship has been an enriching learning experience, allowing me to work closely with open-source EDA tools, develop IC subcircuits in eSim, and gain exposure to real-world circuit modeling and simulation workflows. The knowledge acquired during this period will undoubtedly support my future academic and professional pursuits.

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Chapter 1

Introduction

FOSSEE (Free/Libre and Open Source Software for Education) project promotes the use of FLOSS tools to improve the quality of education in our country. The aim of the project is to reduce dependency on proprietary software in educational institutions. FOSSEE encourages the use of FLOSS tools through various activities to ensure commercial software is replaced by equivalent FLOSS tools. FOSSEE uses FLOSS tools for its activities wherever possible.

The FOSSEE project is part of the National Mission on Education through Information and Communication Technology (ICT), Ministry of Human Resource Development (MHRD), Government of India.

1.1 eSim

eSim is a CAD tool that helps electronic system designers to design, test, and analyze their circuits. The important features of eSim are listed below:

1.1.1 Kicad

Integrated software where all functions of circuit drawing, control, layout, library management, and access to the PCB design software are carried out.

1.1.2 Ngspice

Ngspice is a general-purpose circuit simulation program for nonlinear dc, nonlinear transient, and linear ac analysis.

1.1.3 KiCad to Ngspice converter

Analysis parameters, source details are provided through this module. It allows us to add and edit the device models and subcircuit models.

1.1.4 Subcircuit Builder

This module allows the user to create a subcircuit for a component. Once the subcircuit for a component is created, the subcircuit can be used in other circuits.

1.1.5 NGHDL

A module for mixed signal circuit simulation, is also integrated with eSim. It makes use of VHDL code.

1.1.6 NgVeri

NgVeri, a module for mixed signal circuit simulation, is also integrated with eSim. It makes use of Verilog/System Verilog code.

1.1.7 Makerchip

Makerchip is a cloud-based browser application developed by Redwood EDA to do digital circuit design. One can simulate Verilog, TL-Verilog, and SystemVerilog designs in Makerchip.

Chapter 2

Abstract

The objective of this internship was to design and develop various integrated circuits using the Subcircuit Builder Method within eSim. The primary focus was on implementing analog and digital ICs that are currently not available in the eSim subcircuit library, thereby expanding its functionality and utility for circuit designers and students.

2.1 Approach

- Identify and research an integrated circuit (IC) that is not currently available in the eSim library.
- Obtain and study the datasheet of the selected IC thoroughly.
- Carefully examine the schematic provided in the datasheet.
- Accurately recreate the schematic in eSim using the Subcircuit Builder Method.
- Model the IC in eSim, ensuring all parameters and configurations match those in the datasheet.
- Simulate the integrated circuit within eSim, testing it with various circuits to verify its functionality.
- Document the process and results to contribute to the future use and expansion of the eSim Subcircuit Library.

Chapter 3

Integrated Circuit Design

3.1 $\mu\text{A}107$

3.1.1 Description

The $\mu\text{A}107$ is a general-purpose operational amplifier developed using the Fairchild Planar epitaxial process technology. It provides high gain, low input current, and internal frequency compensation, making it ideal for a wide range of analog circuit applications.

Features Of $\mu\text{A}107$

- Low Input Current: Suitable for high impedance applications and precision circuits.
- Low Offset Voltage: Provides better accuracy and stable amplifier operation.
- Internal Frequency Compensation: Ensures stable performance without requiring external compensation components.

3.1.2 Pin Diagram

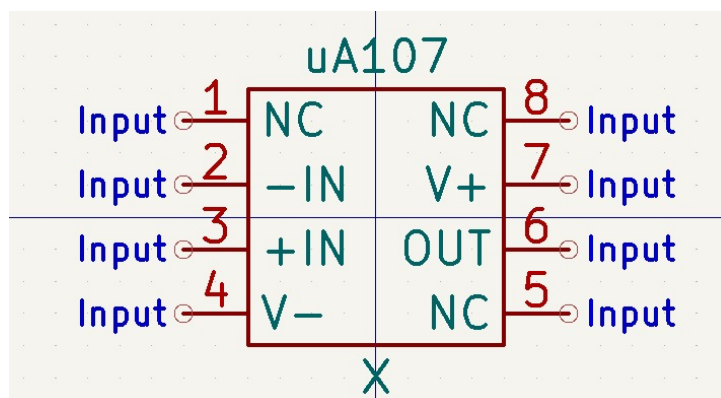


Figure 3.1: Pin Diagram of $\mu\text{A}107$

3.1.3 Sub-Circuit Diagram

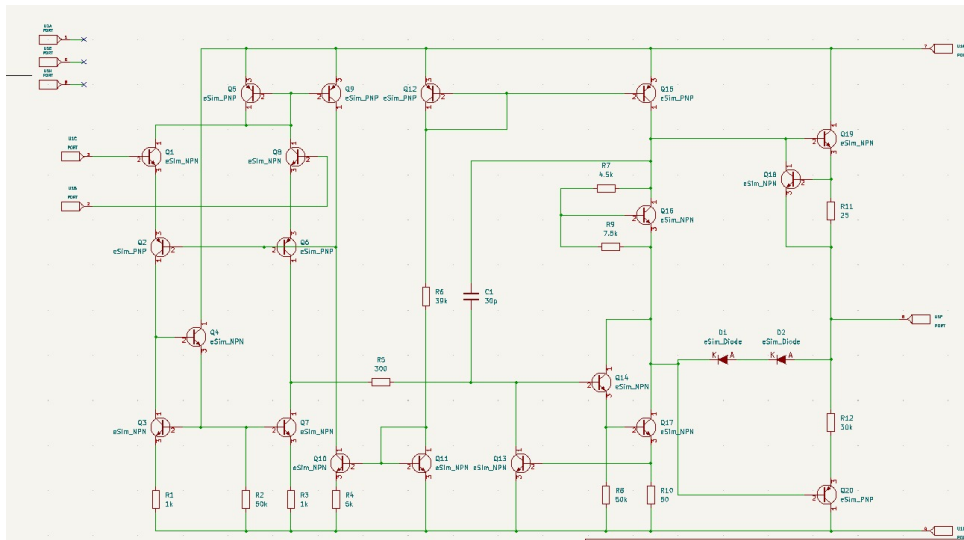


Figure 3.2: Sub-Circuit of $\mu A107$

3.1.4 Test-Circuit Diagram

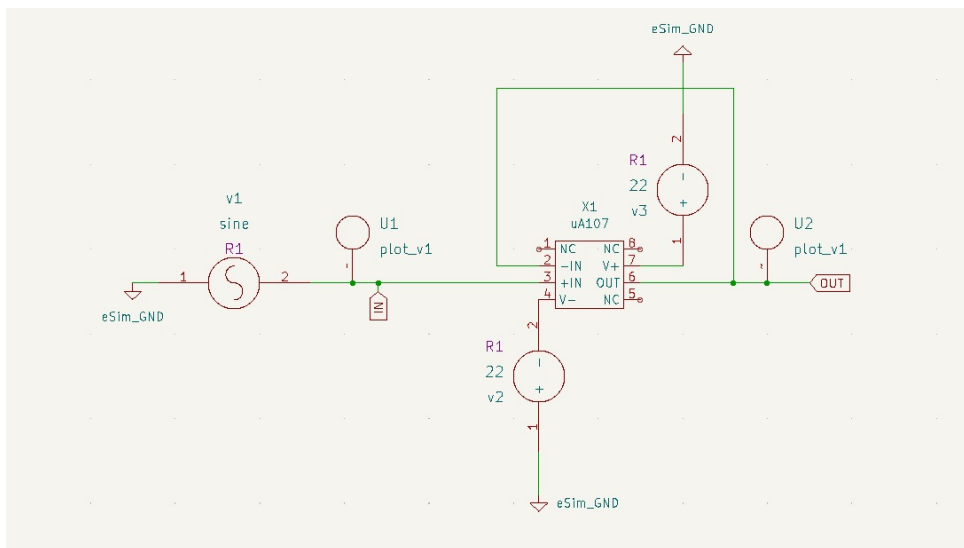


Figure 3.3: Test Circuit of $\mu A107$

3.1.5 NgSpice Plot

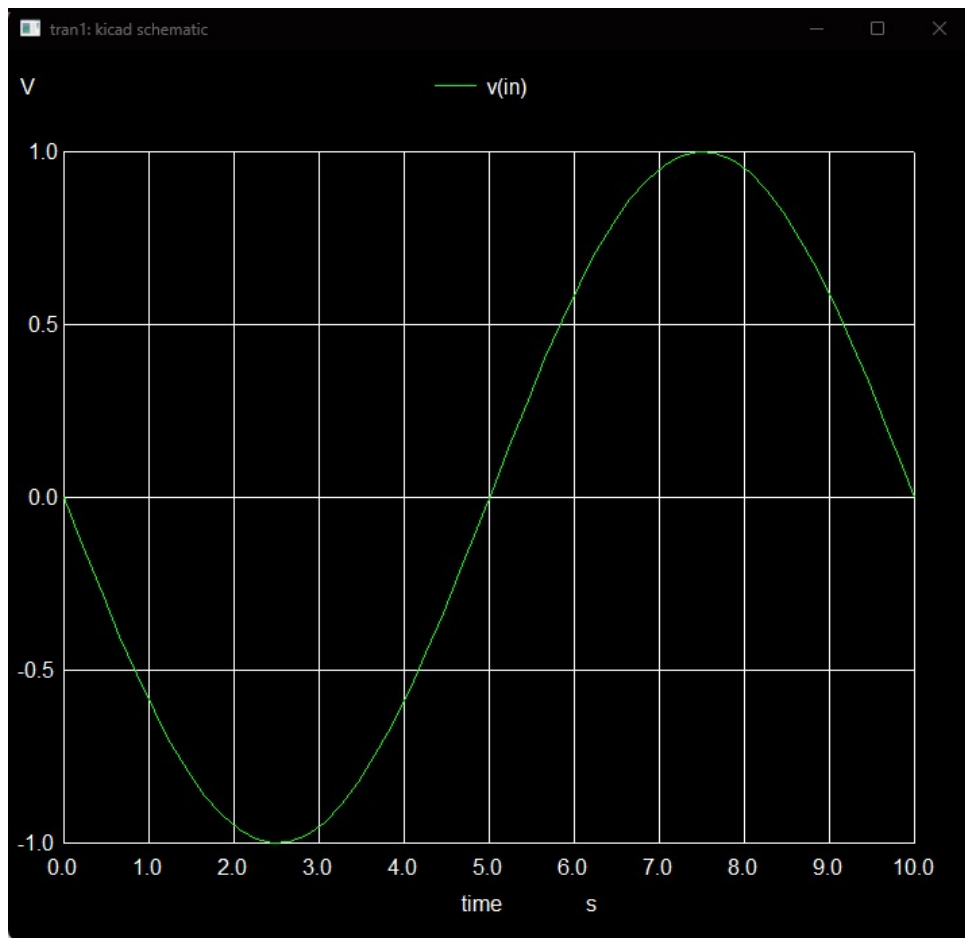


Figure 3.4: Input Graph of $\mu A107$

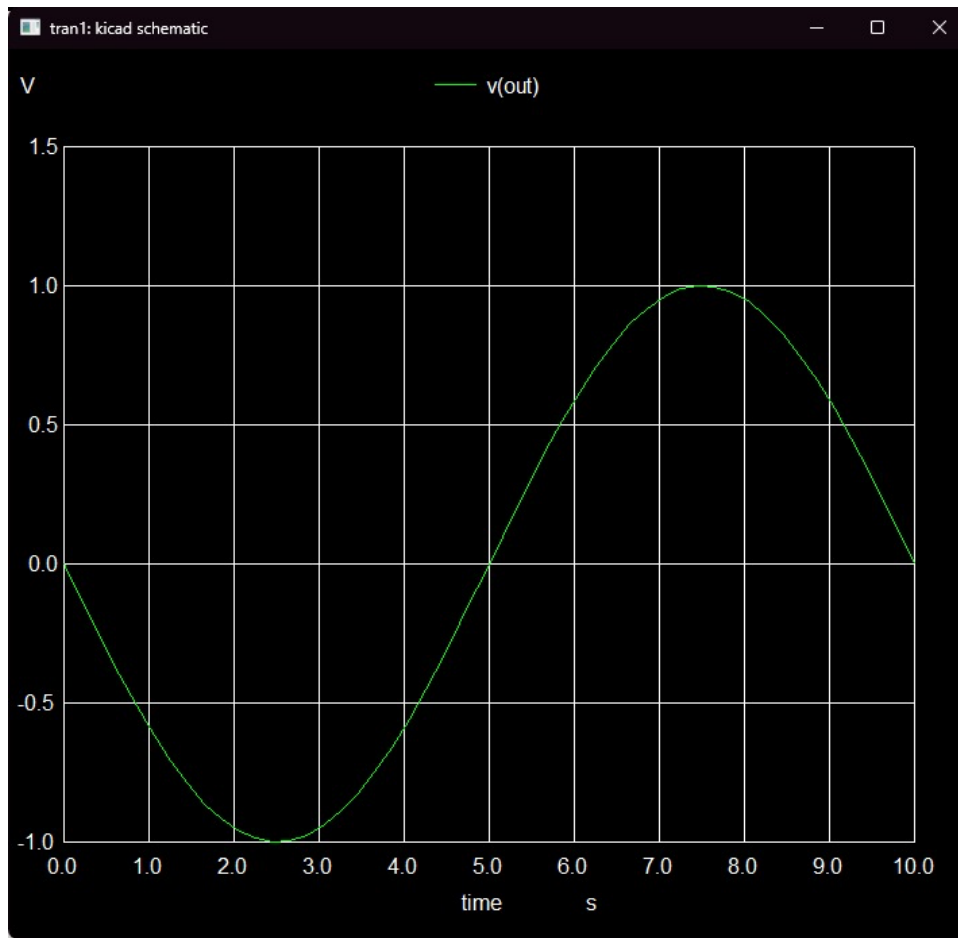


Figure 3.5: Output Graph of $\mu A107$

3.2 $\mu A799$

3.2.1 Description

The $\mu A799$ is a monolithic operational amplifier designed for general-purpose analog applications. It is internally frequency compensated for stable operation across a wide range of configurations.

Features Of $\mu A799$

- **Wide Operating Voltage Range:** Supports single supply operation from 3V to 36V and dual supply operation up to $\pm 18V$.
- **Internally Compensated:** Provides stable operation without requiring external compensation components.
- **Low Power Consumption:** Consumes very low supply current for efficient circuit operation.

3.2.2 Pin Diagram

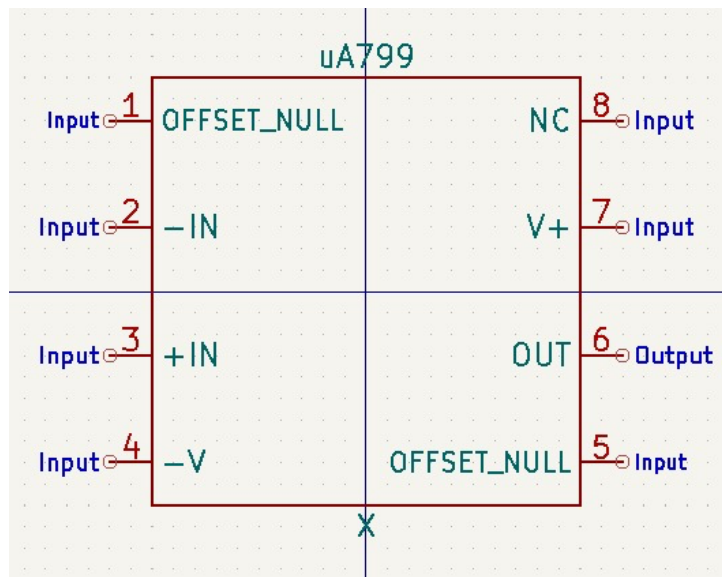
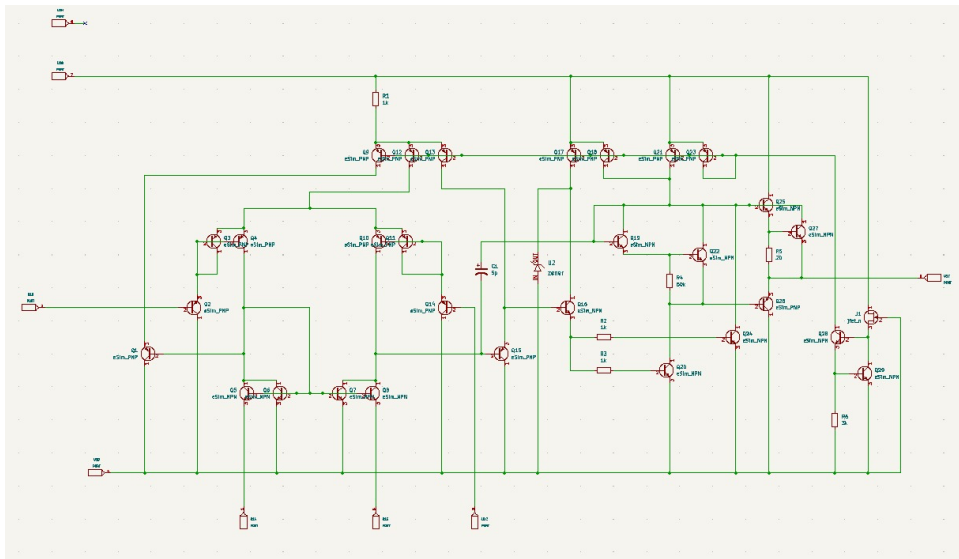


Figure 3.6: Pin Diagram of $\mu A799$

3.2.3 Sub-Circuit Diagram



3.2.4 Test-Circuit Diagram

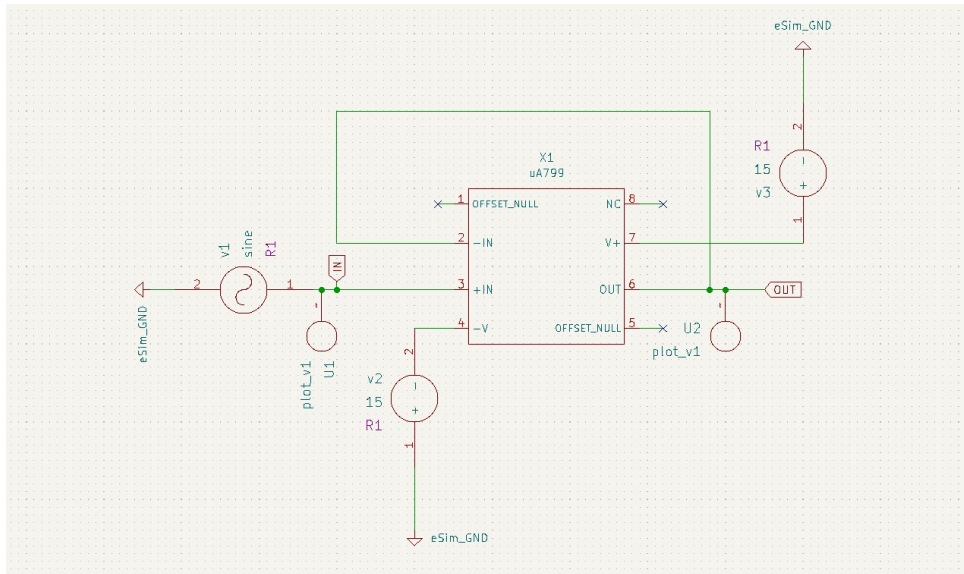


Figure 3.8: Test Circuit of $\mu A799$

3.2.5 NgSpice Plot

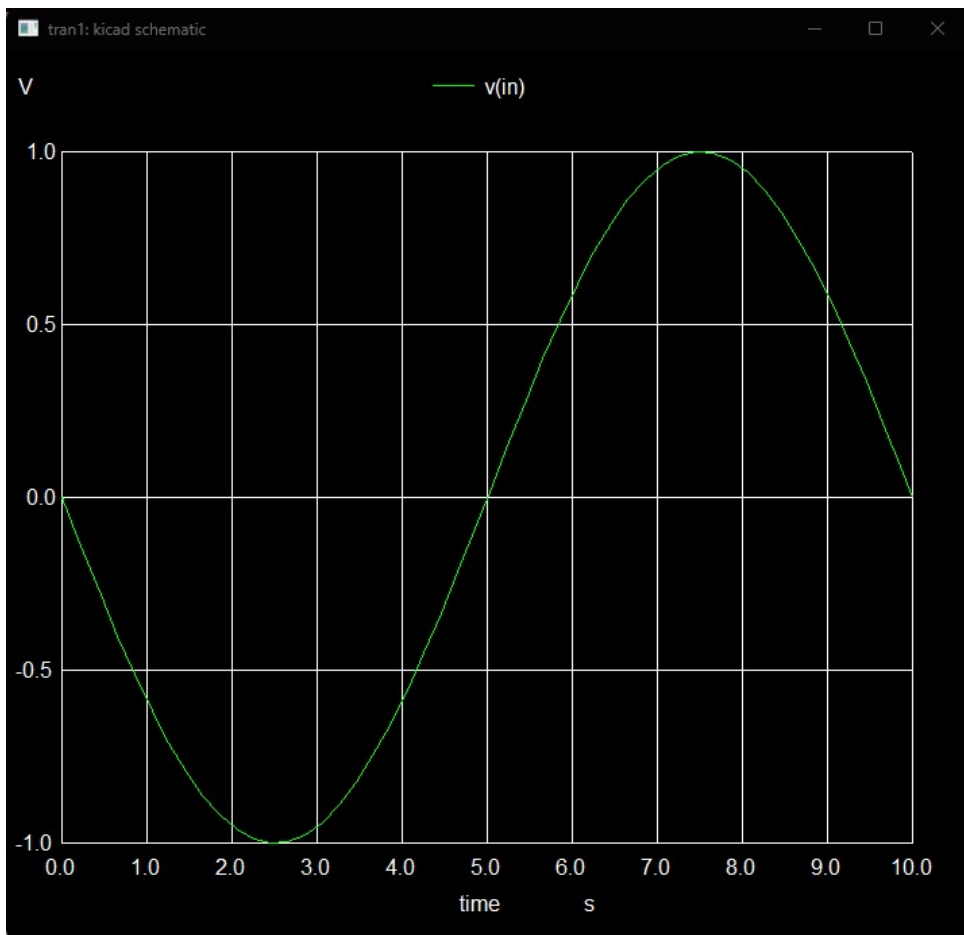


Figure 3.9: Input Graph of $\mu A799$

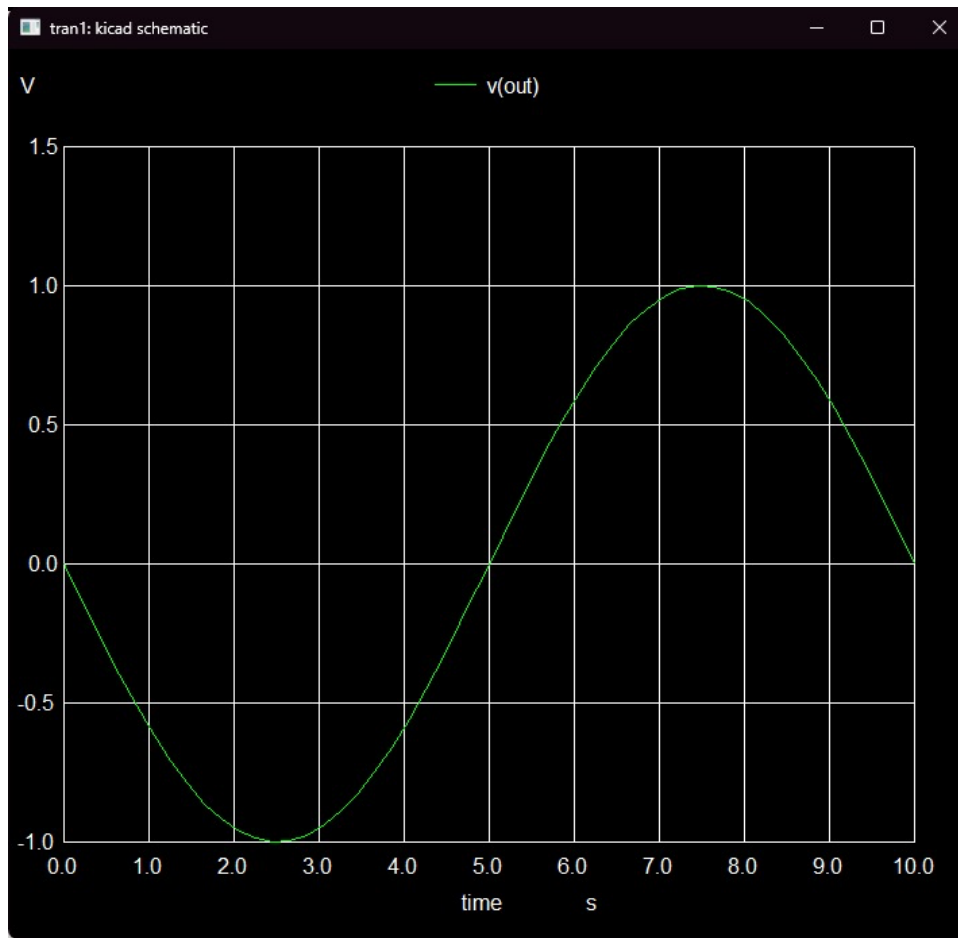


Figure 3.10: Output Graph of $\mu\text{A}799$

3.3 $\mu\text{A}740$

3.3.1 Description

The $\mu\text{A}740$ is a high performance FET input operational amplifier designed for analog applications requiring very high input impedance and low bias current.

Features Of $\mu\text{A}740$

- High Input Impedance: Very high input impedance of about 1,000,000 $\text{M}\Omega$ makes it suitable for high impedance circuits.
- No Frequency Compensation Required: Internally compensated for stable closed-loop operation without external components.
- Short Circuit Protection: Output is protected against short circuit conditions for reliable operation.

3.3.2 Pin Diagram

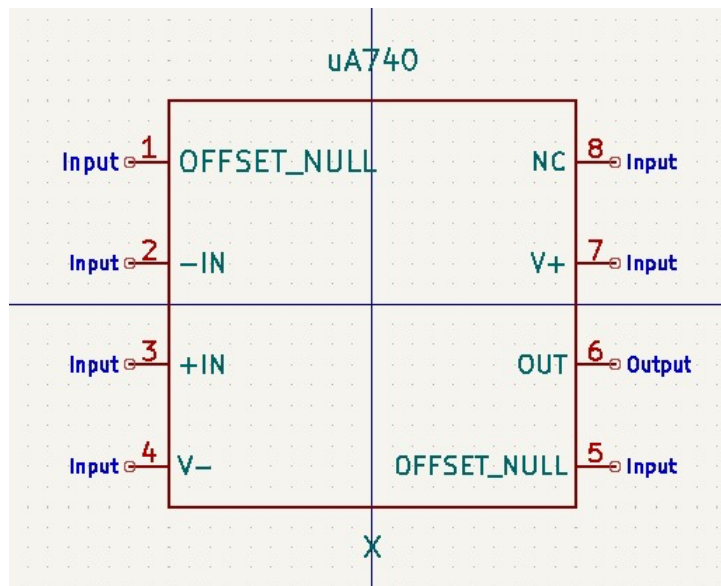


Figure 3.11: Pin Diagram of $\mu A740$

3.3.3 Sub-Circuit Diagram

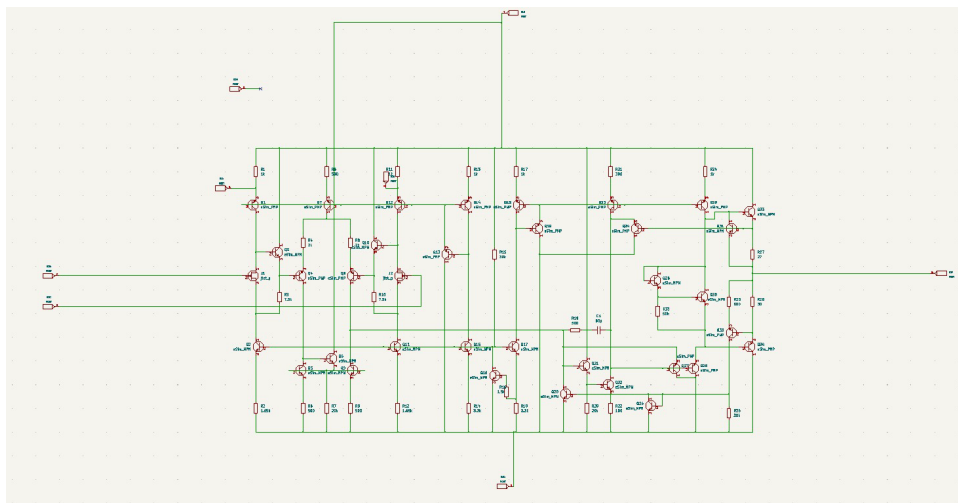


Figure 3.12: Sub-Circuit of $\mu A740$

3.3.4 Test-Circuit Diagram

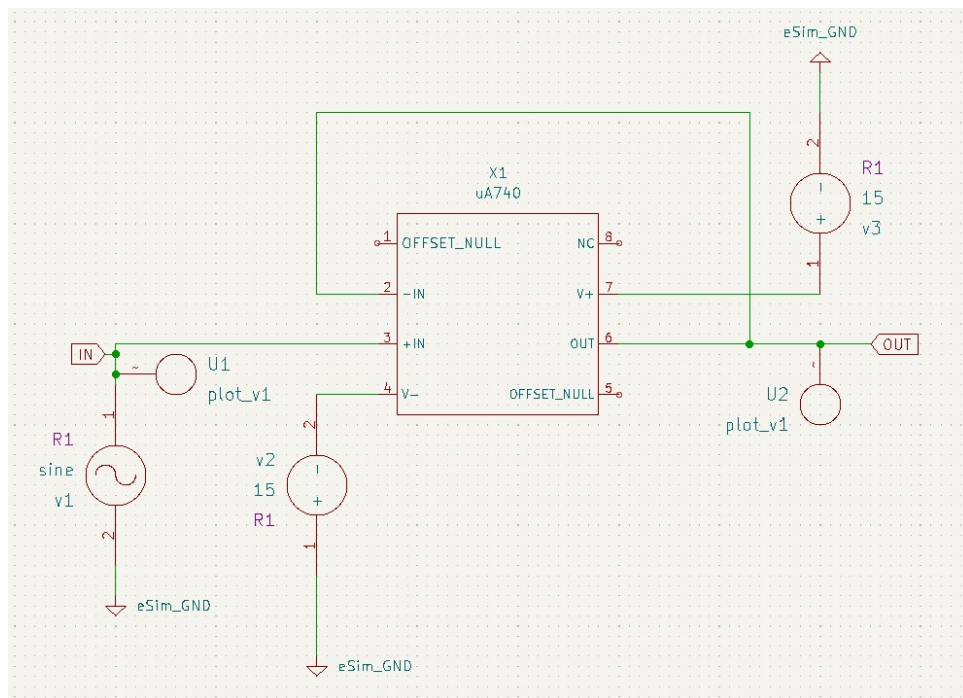


Figure 3.13: Test Circuit of $\mu A740$

3.3.5 NgSpice Plot

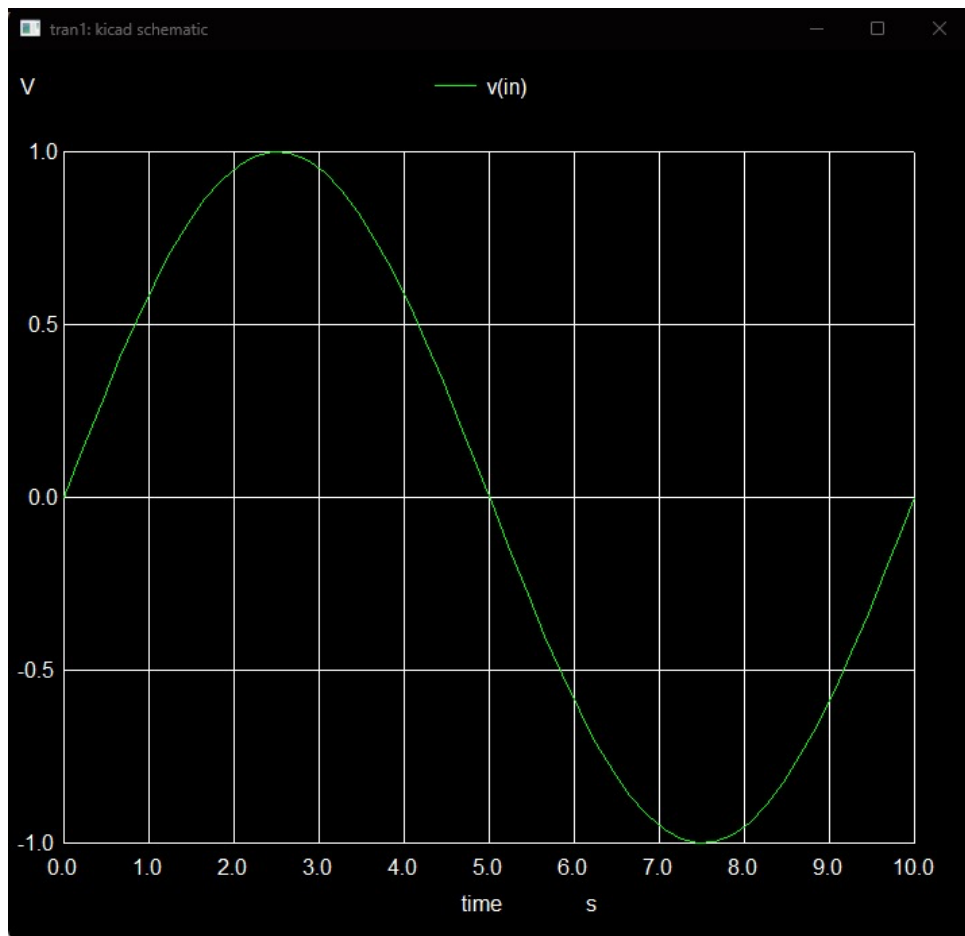


Figure 3.14: Input Graph of $\mu A740$

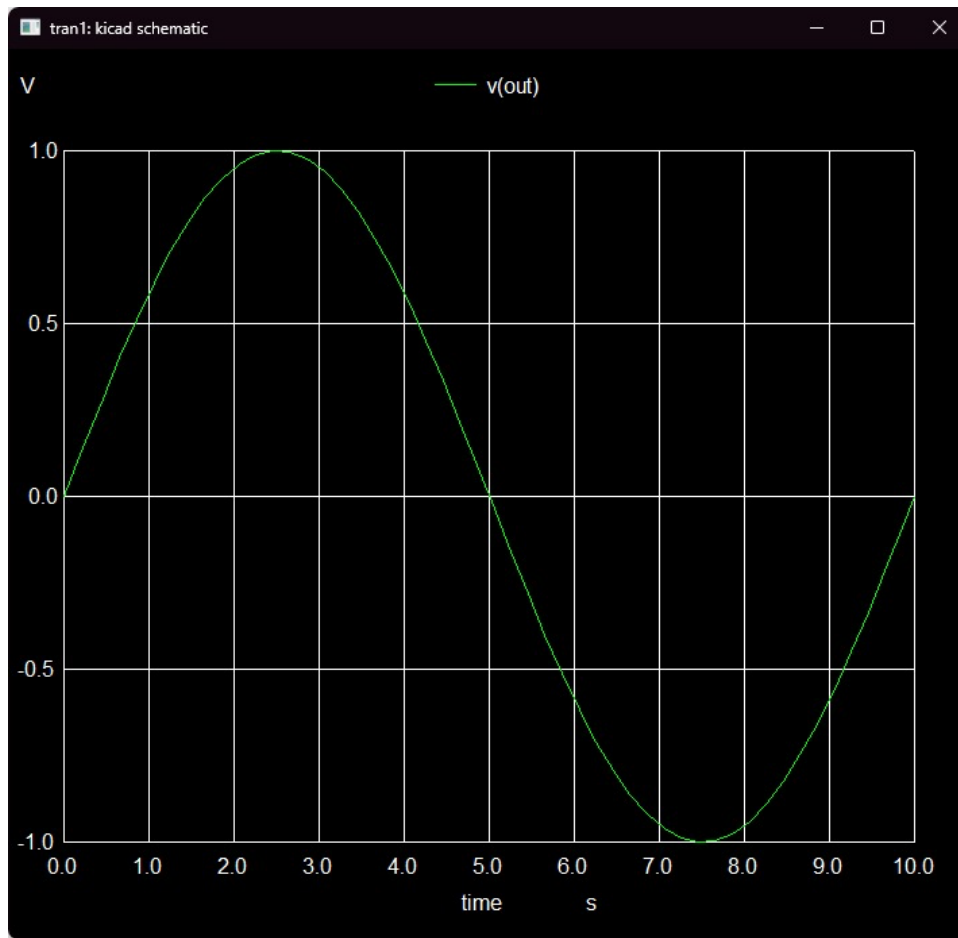


Figure 3.15: Output Graph of $\mu\text{A}740$

3.4 $\mu\text{A}798$

3.4.1 Description

The $\mu\text{A}798$ is a dual operational amplifier containing two independent high gain internally frequency compensated operational amplifiers designed for a wide range of analog applications.

Features Of $\mu\text{A}798$

- Dual Operational Amplifiers: Contains two independent op-amps in a single IC package.
- Wide Supply Voltage Range: Supports single supply from 3V to 36V and dual supply up to $\pm 18\text{V}$.
- Internally Compensated: Provides stable operation without external frequency compensation.

3.4.2 Pin Diagram

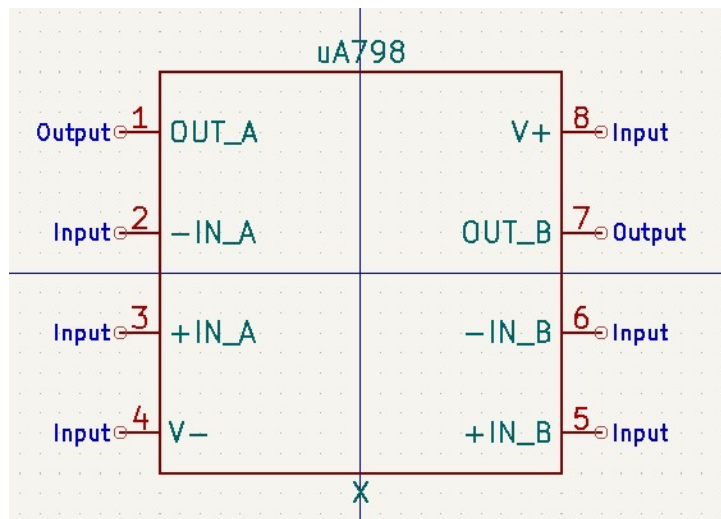


Figure 3.16: Pin Diagram of $\mu A798$

3.4.3 Sub-Circuit Diagram

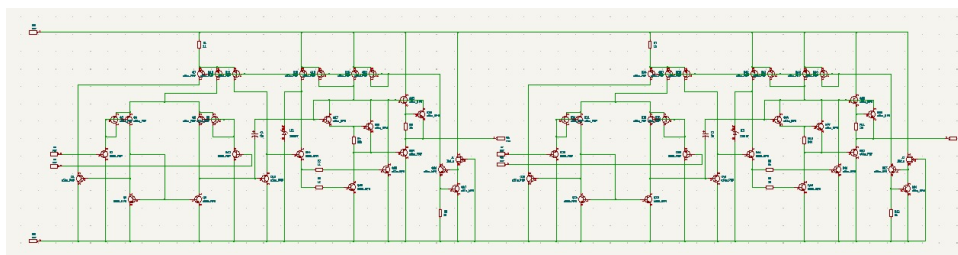


Figure 3.17: Sub-Circuit of $\mu A798$

3.4.4 Test-Circuit Diagram

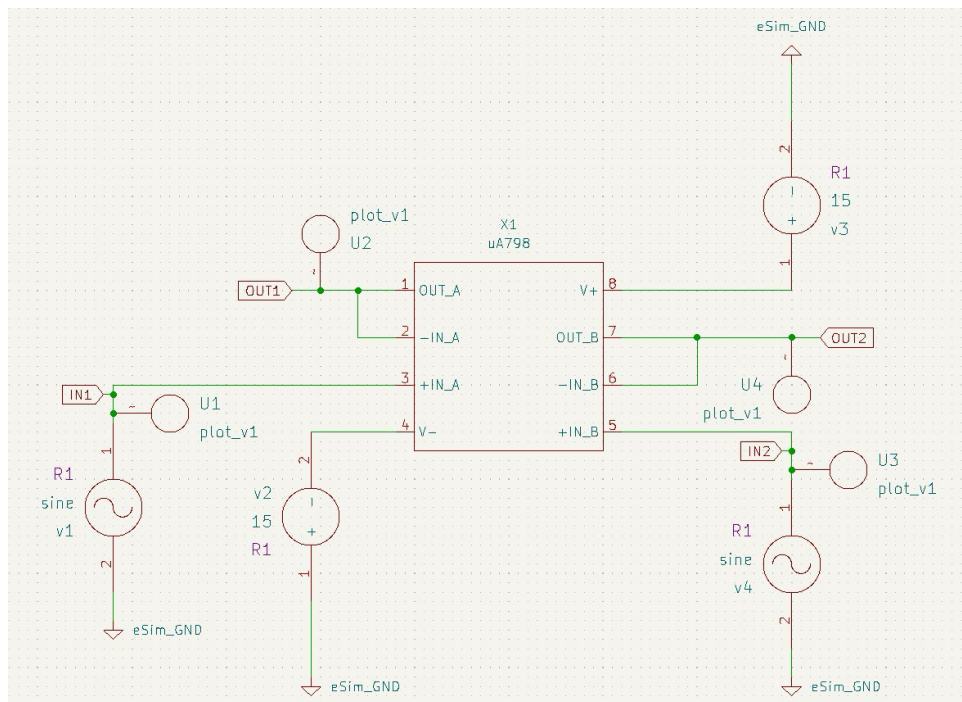


Figure 3.18: Test Circuit of $\mu A798$

3.4.5 NgSpice Plot

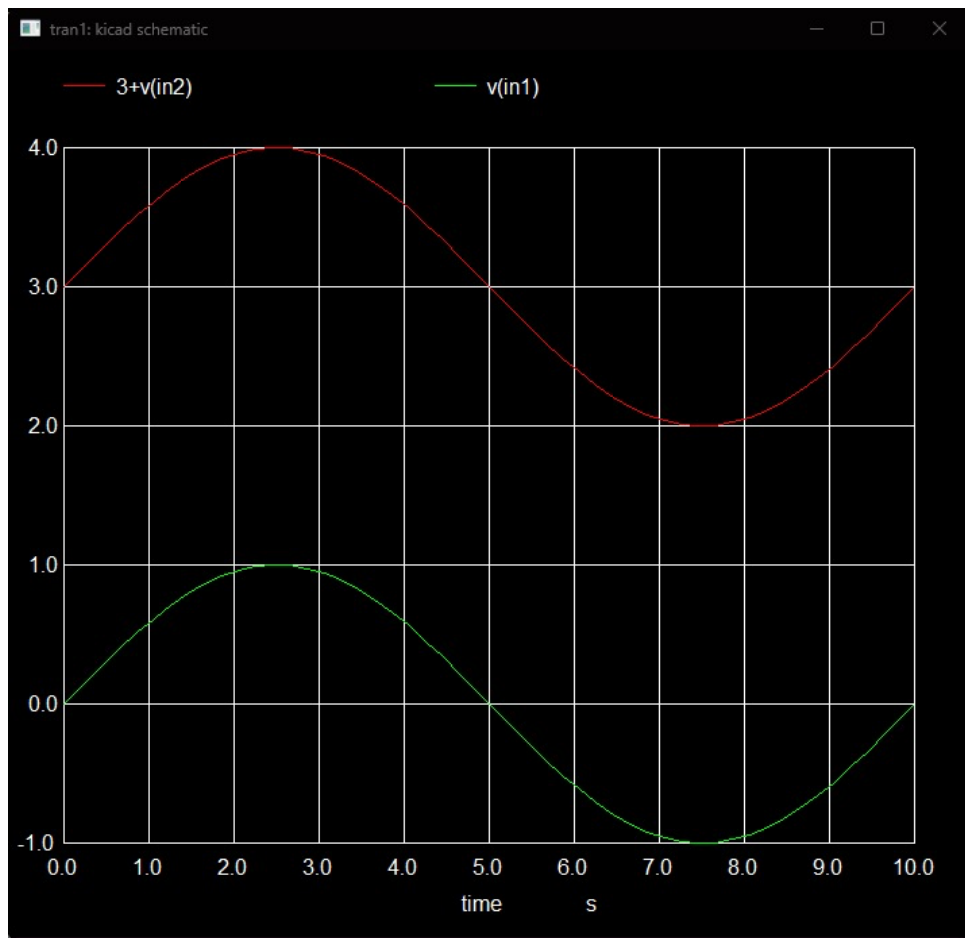


Figure 3.19: Input Graph of $\mu A798$

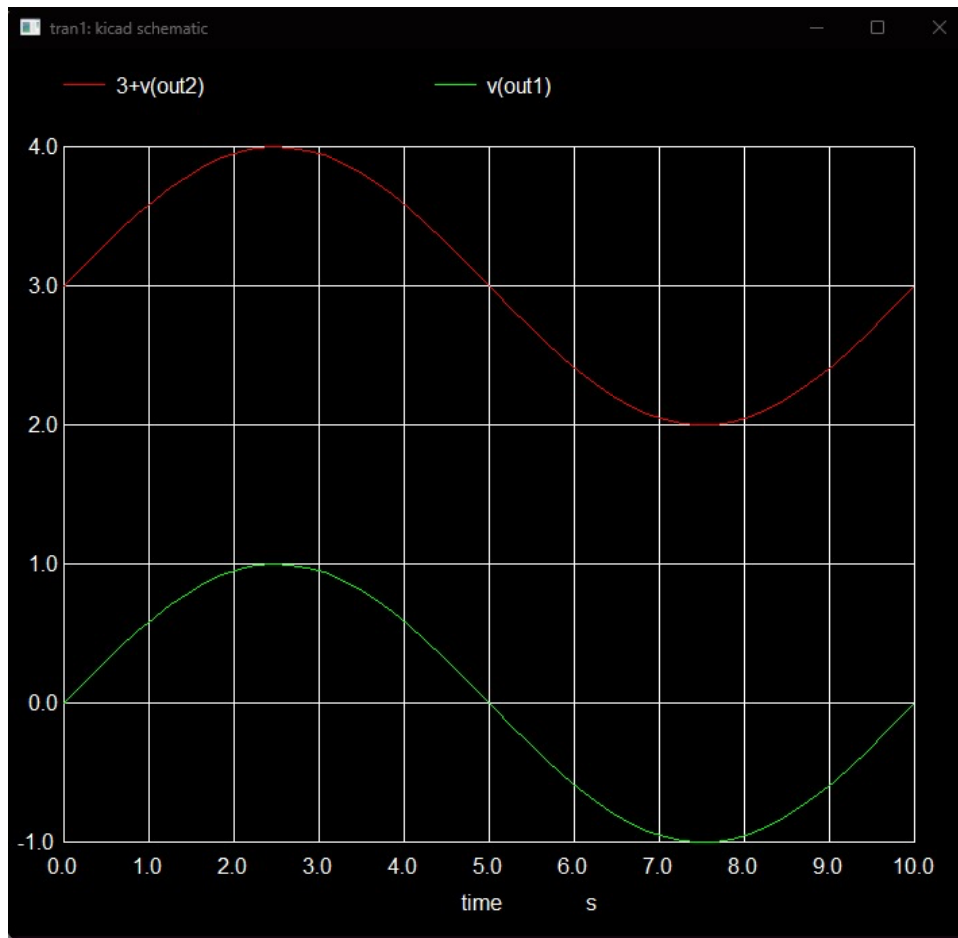


Figure 3.20: Output Graph of $\mu\text{A}798$

3.5 $\mu\text{A}747$

3.5.1 Description

The $\mu\text{A}747$ is a dual frequency-compensated operational amplifier containing two high performance operational amplifiers in a single package for space-critical applications.

Features Of $\mu\text{A}747$

- Dual Operational Amplifiers: Contains two independent operational amplifiers in one IC package.
- No Frequency Compensation Required: Internally frequency compensated for stable closed-loop operation.
- Short Circuit Protection: Output is protected against short circuit conditions for reliable performance.

3.5.2 Pin Diagram

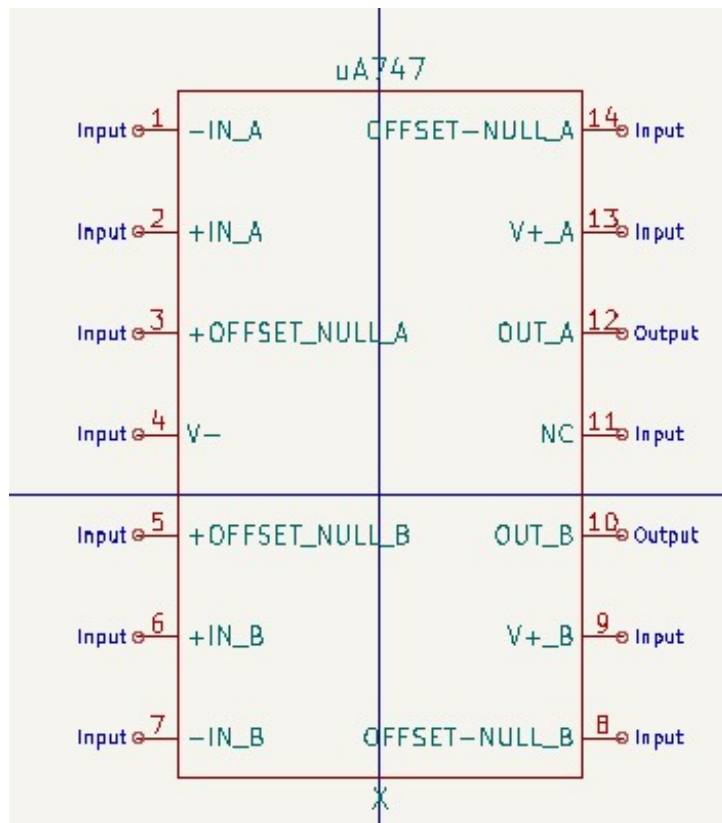


Figure 3.21: Pin Diagram of $\mu A747$

3.5.3 Sub-Circuit Diagram

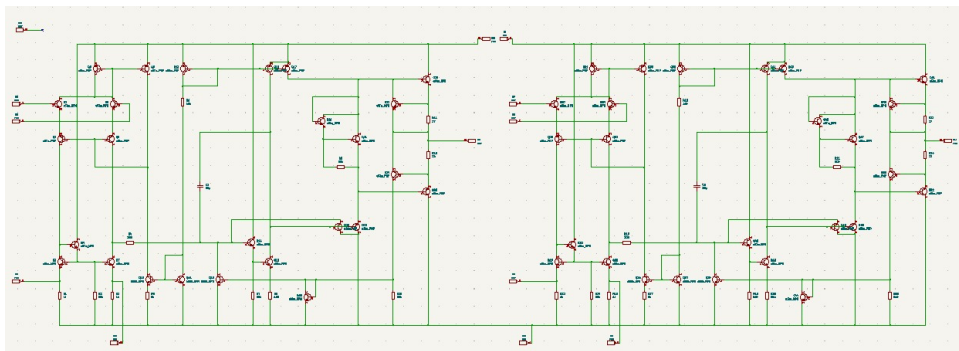


Figure 3.22: Sub-Circuit of $\mu A747$

3.5.4 Test-Circuit Diagram

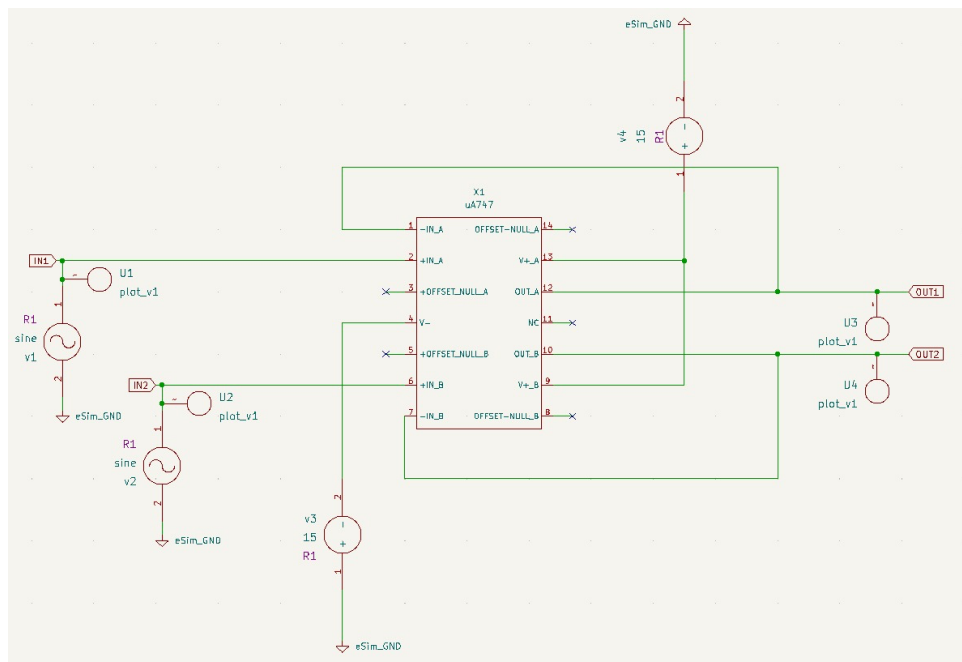


Figure 3.23: Test Circuit of $\mu A747$

3.5.5 NgSpice Plot

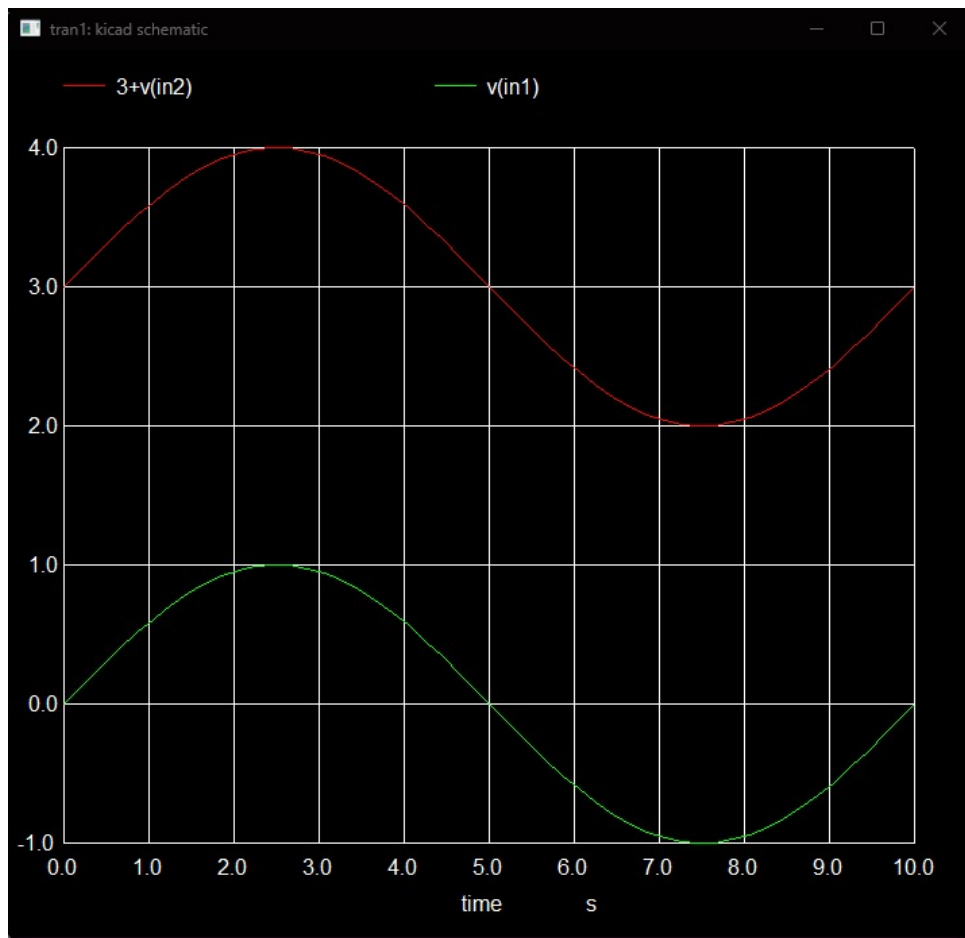


Figure 3.24: Input Graph of $\mu A747$

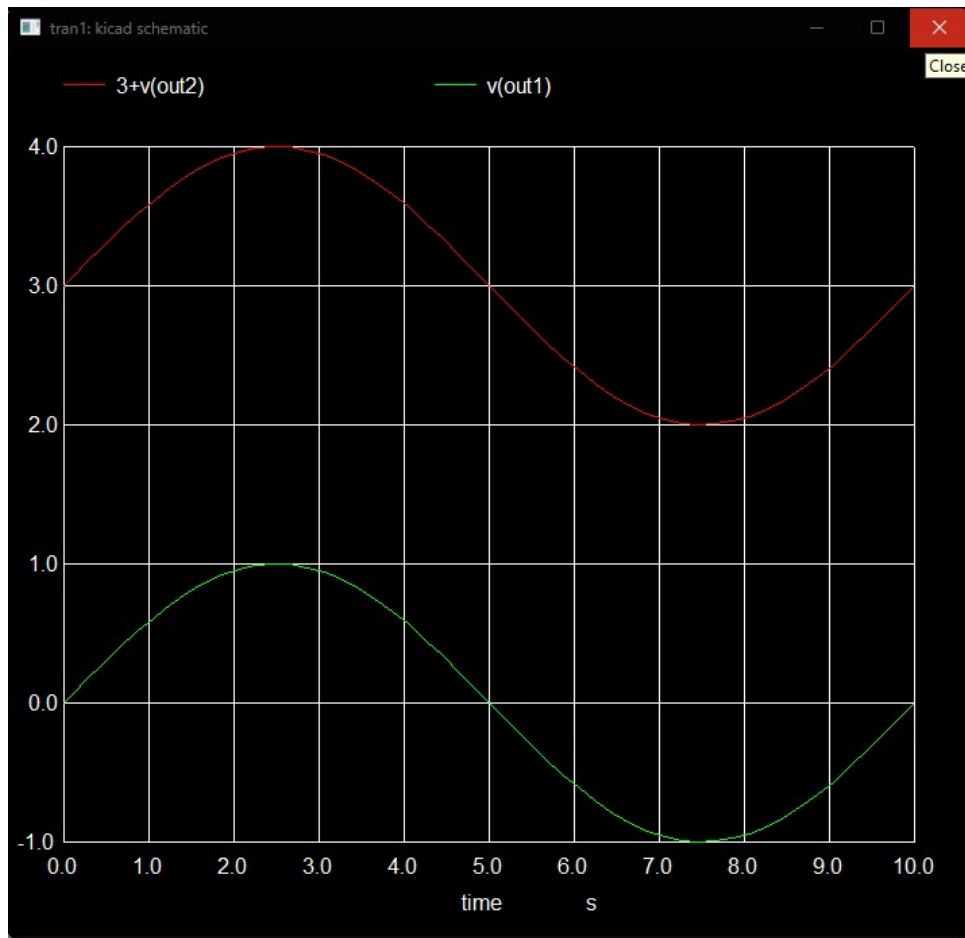


Figure 3.25: Output Graph of $\mu A747$

3.6 $\mu A748$

3.6.1 Description

The $\mu A748$ is a precision single operational amplifier designed for general purpose analog applications. It provides low offset voltage and external frequency compensation capability for optimized performance.

Features Of $\mu A748$

- Low Offset Voltage: Maximum input offset voltage of 3 mV over temperature range.
- Frequency Compensation: Stable operation using a single 30 pF compensation capacitor.
- Short Circuit Protection: Continuous output short circuit protection for reliable operation.

3.6.2 Pin Diagram

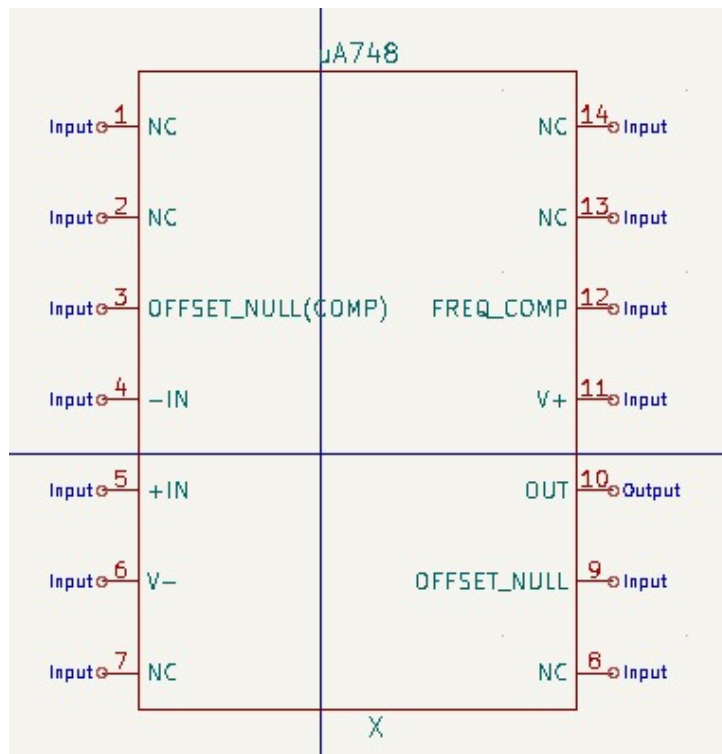


Figure 3.26: Pin Diagram of UA748

3.6.3 Sub-Circuit Diagram

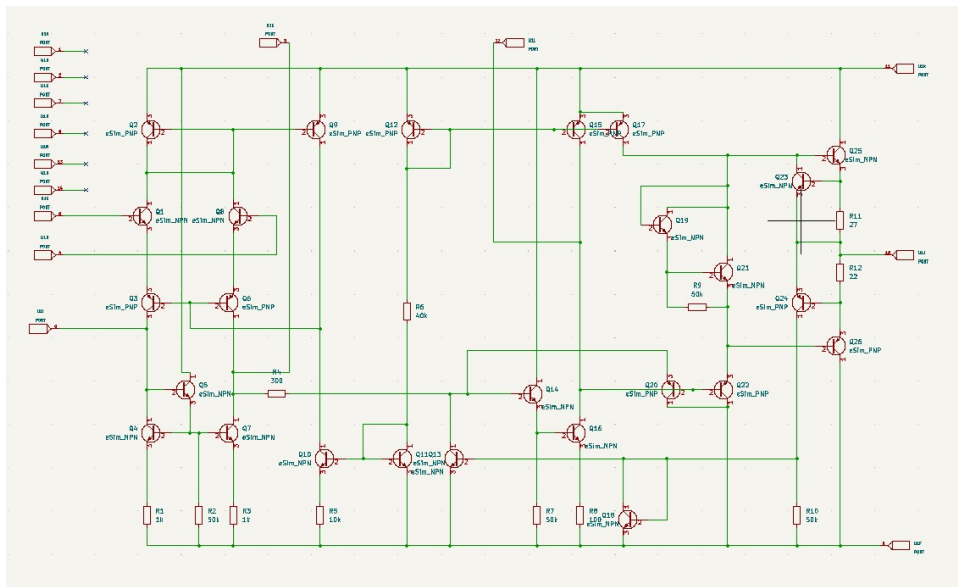


Figure 3.27: Sub-Circuit of $\mu A748$

3.6.4 Test-Circuit Diagram

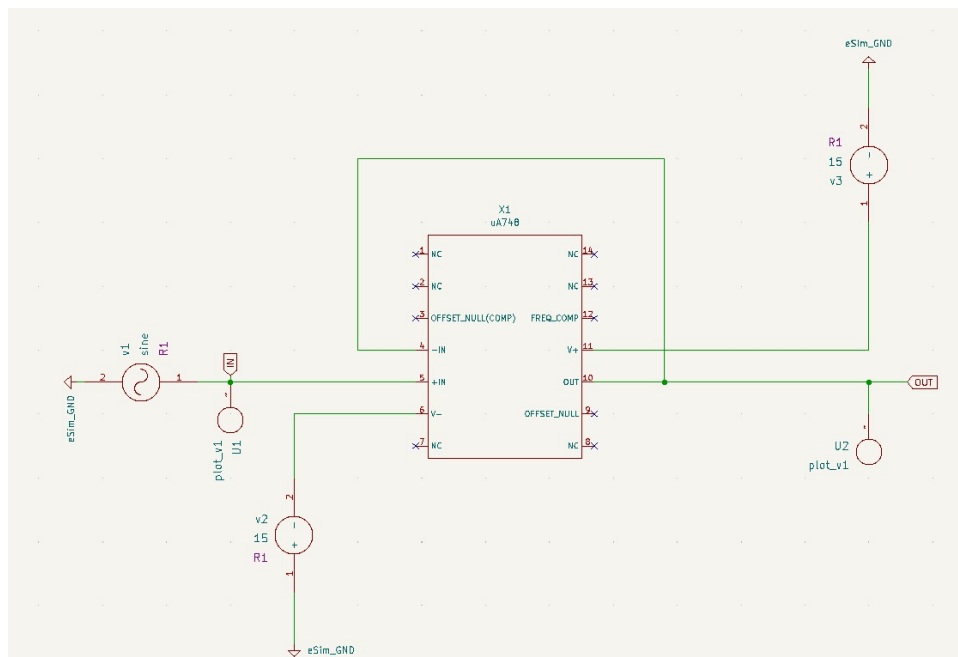


Figure 3.28: Test Circuit of $\mu A748$

3.6.5 NgSpice Plot

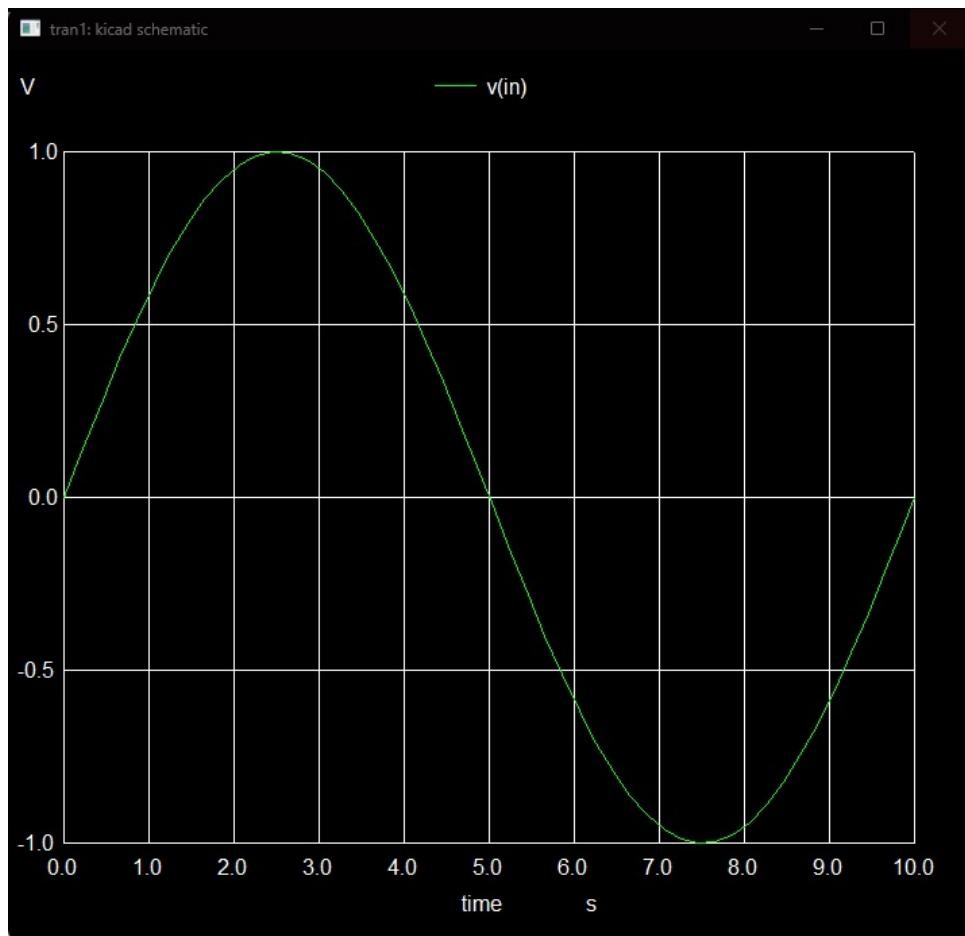


Figure 3.29: Input Graph of $\mu A748$

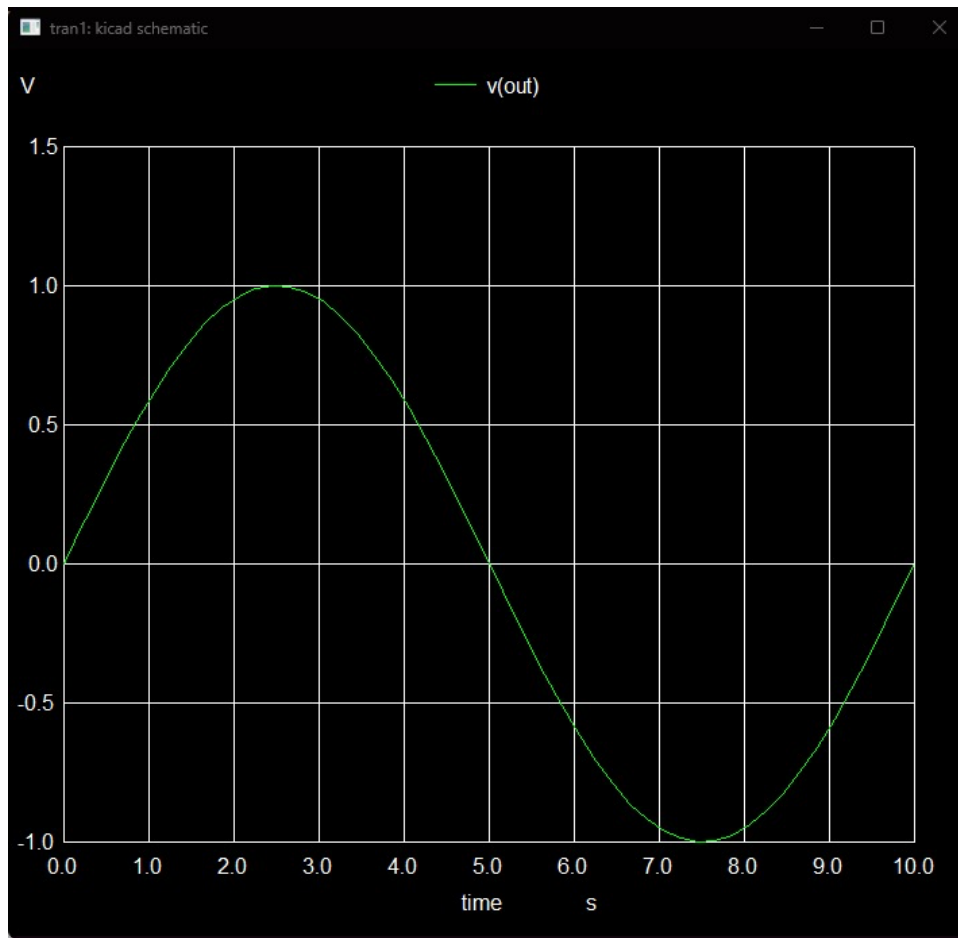


Figure 3.30: Output Graph of $\mu A748$

3.7 CD4072B

3.7.1 Description

The CD4075B is a CMOS Triple 3-Input OR Gate IC designed for implementing positive logic OR functions in digital electronic circuits. It is built using complementary MOS technology for high noise immunity and low power consumption.

Features Of CD4072B

- Triple 3-Input OR Gates: Contains three independent 3-input OR gates in a single IC package.
- Wide Operating Voltage Range: Operates with supply voltages from 3V to 18V.
- Low Power Consumption: CMOS design provides very low quiescent power dissipation.

3.7.2 Pin Diagram

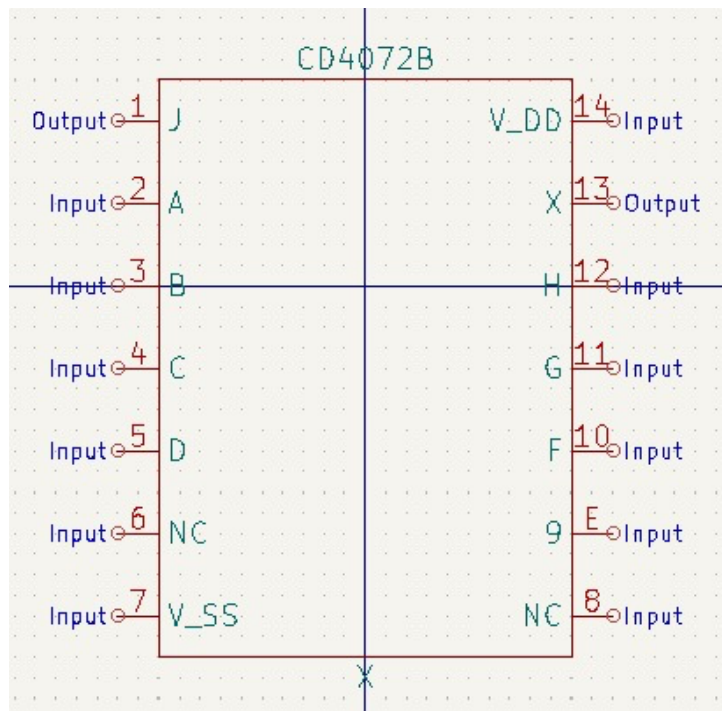


Figure 3.31: Pin Diagram of CD4072B

3.7.3 Sub-Circuit Diagram

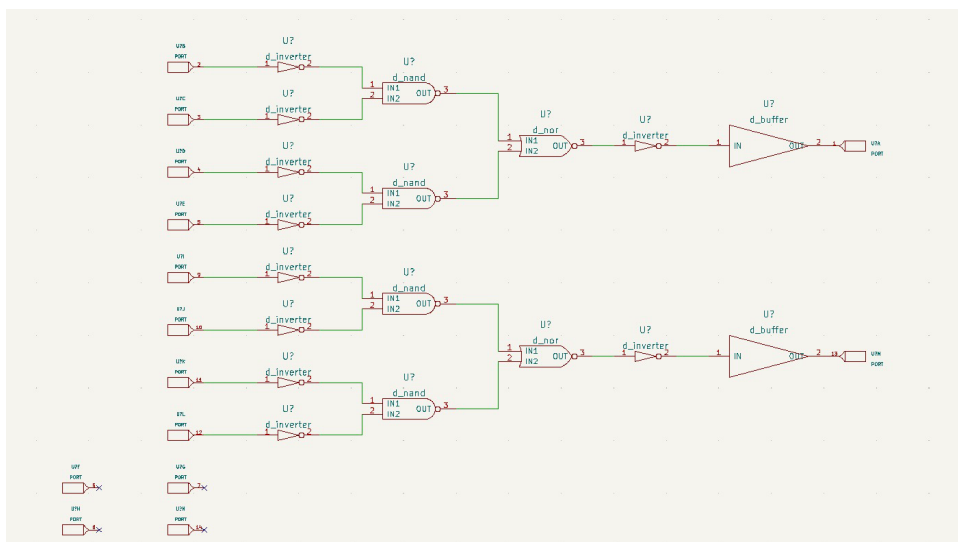


Figure 3.32: Sub-Circuit of CD4072B

3.7.4 Test-Circuit Diagram

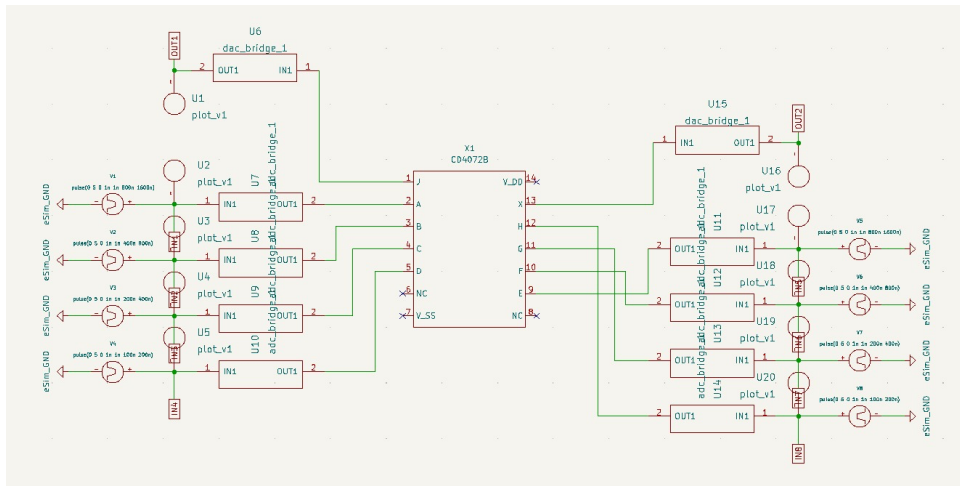


Figure 3.33: Test Circuit of CD4072B

3.7.5 NgSpice Plot

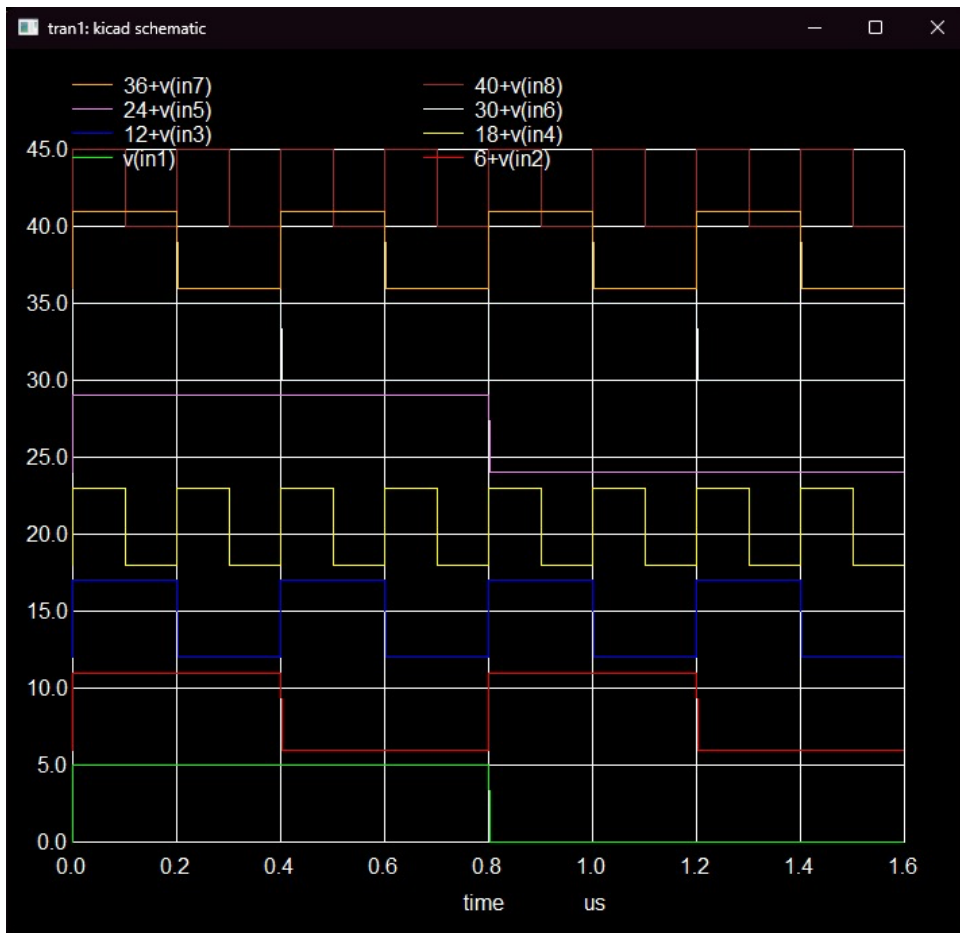


Figure 3.34: Input Graph of CD4072B

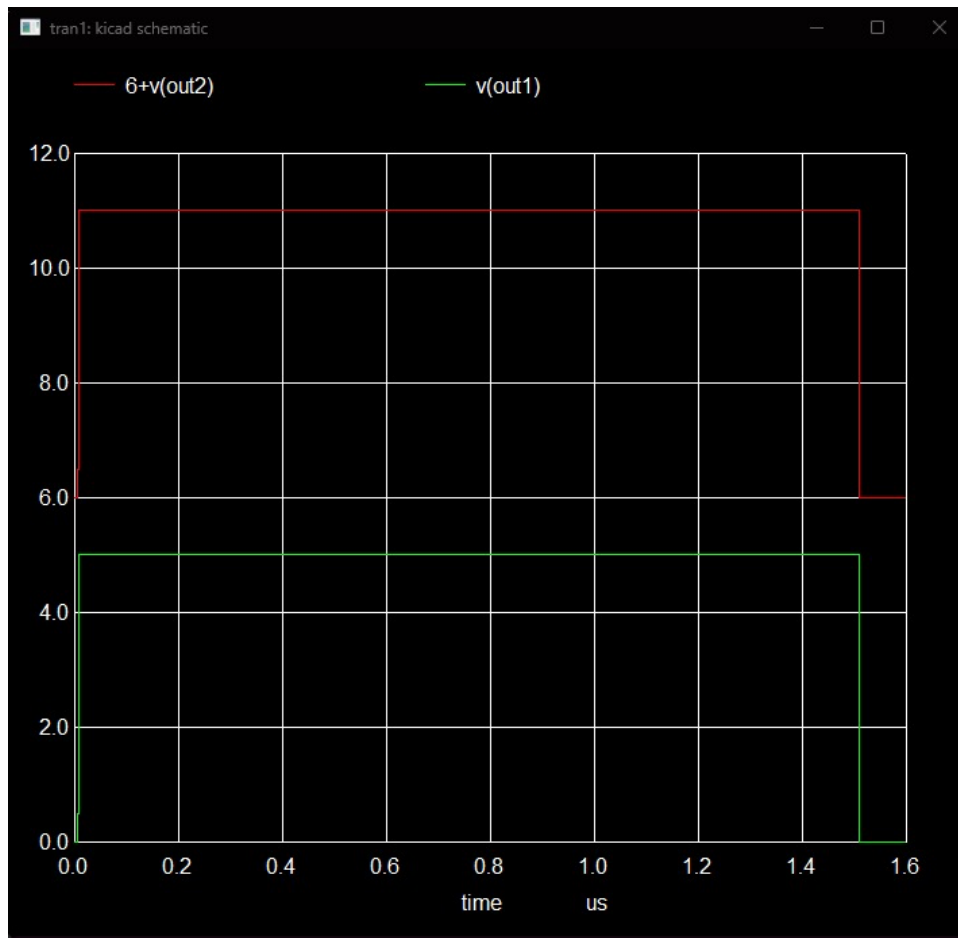


Figure 3.35: Output Graph of CD4072B

3.8 CD4042A

3.8.1 Description

The CD4042A is a CMOS Quad Clocked “D” Latch IC that contains four latch circuits controlled by a common clock signal. It is designed for data storage and transfer applications in digital systems.

Features Of CD4042A

- Quad D Latch: Contains four independent clocked D latch circuits in a single IC.
- Complementary Outputs: Provides both Q and \bar{Q} outputs for each latch.
- Low Power Consumption: CMOS technology ensures very low quiescent power dissipation.

3.8.2 Pin Diagram

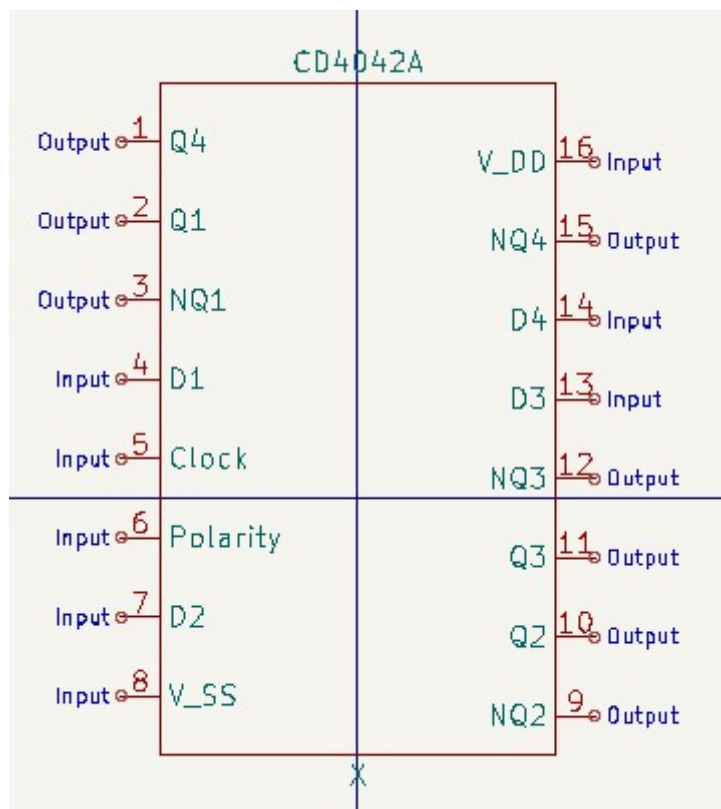


Figure 3.36: Pin Diagram of CD4042A

3.8.3 Sub-Circuit Diagram

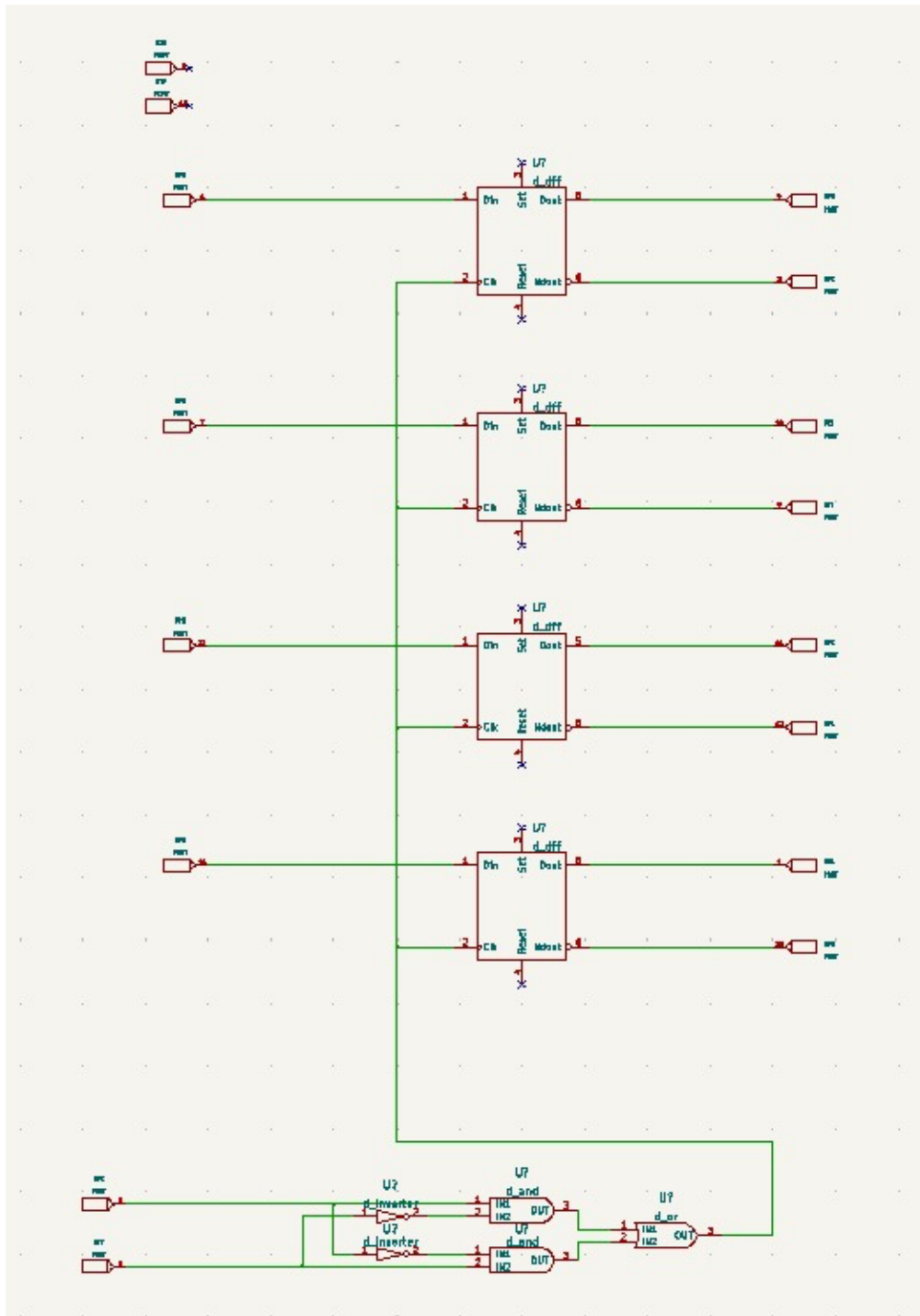


Figure 3.37: Sub-Circuit of CD4042A

3.8.4 Test-Circuit Diagram

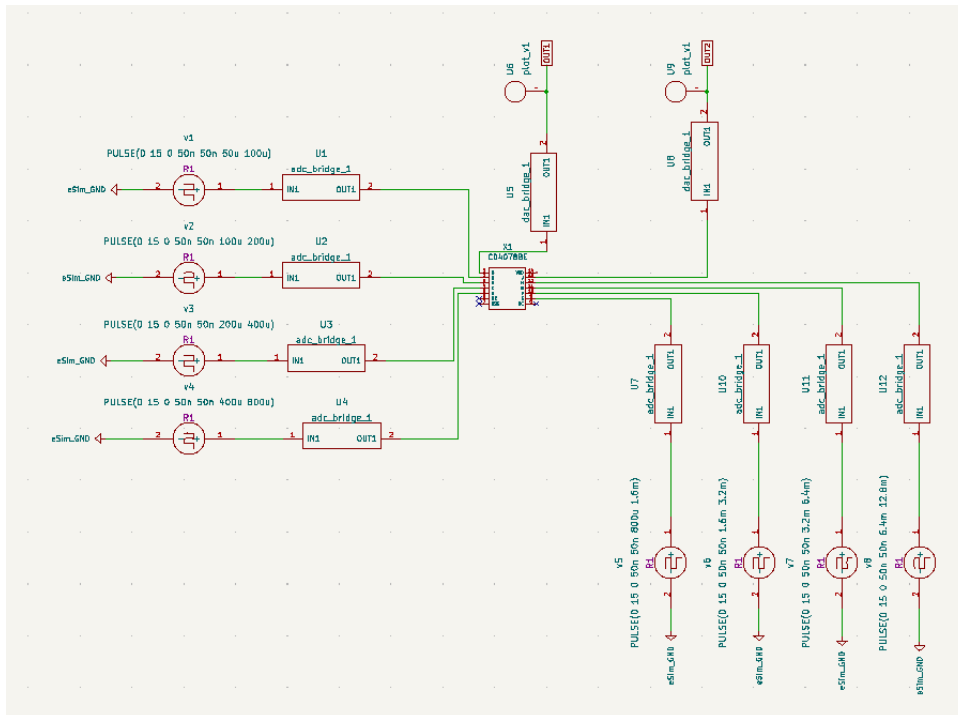


Figure 3.38: Test Circuit of CD4042A

3.8.5 NgSpice Plot

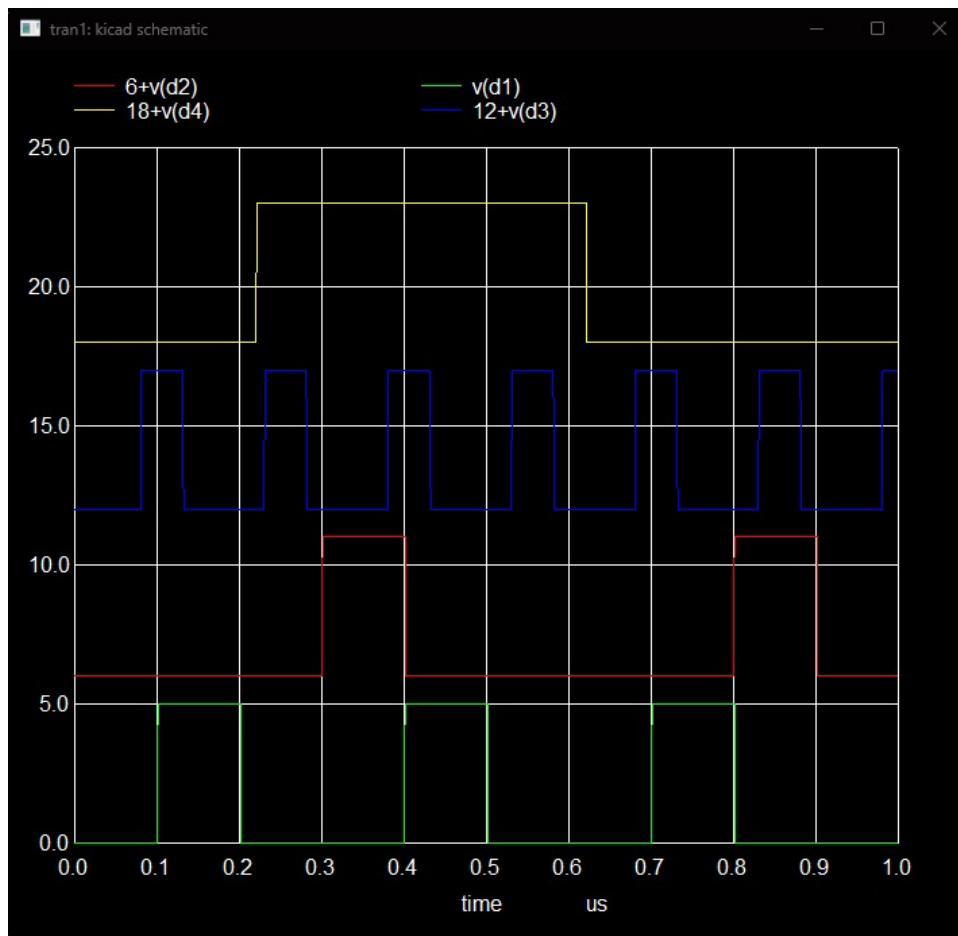


Figure 3.39: Input Graph of CD4042A

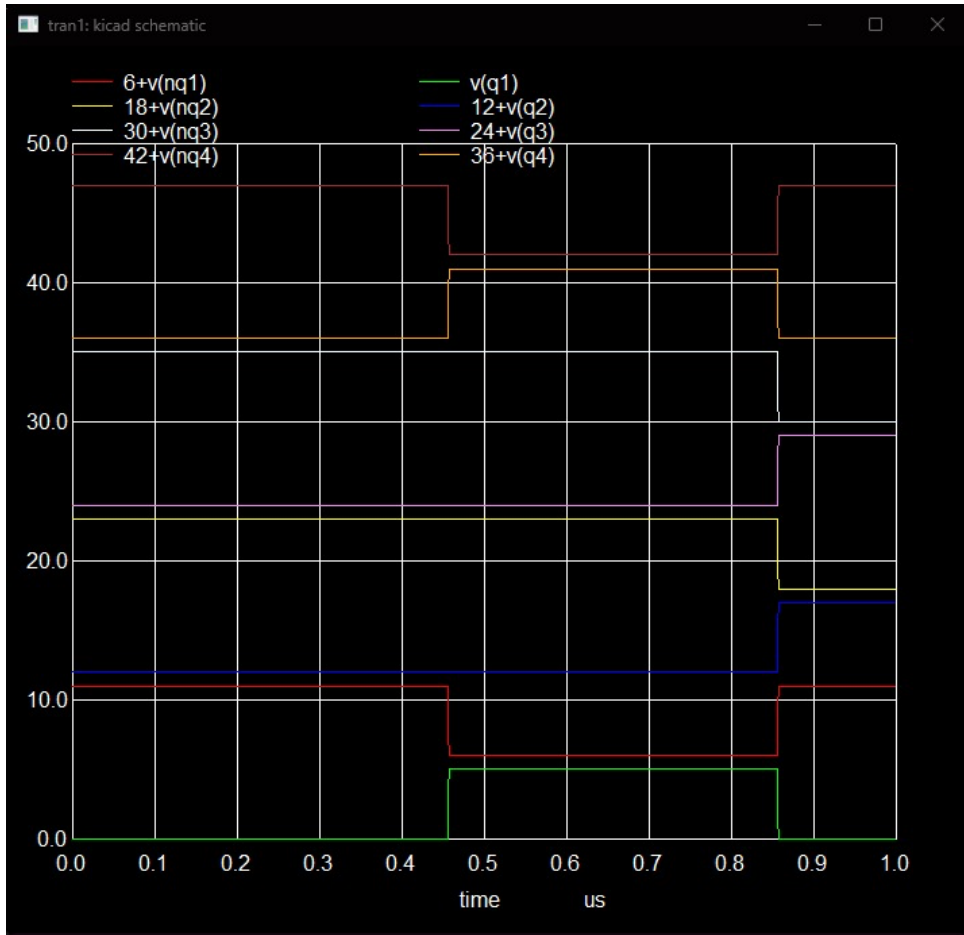


Figure 3.40: Output Graph of CD4042A

Chapter 4

Conclusion and Future Scope

This project successfully demonstrates the comprehensive design and simulation of integrated circuits utilizing the eSim Subcircuit Builder Method. Through the systematic approach of studying datasheets, recreating schematics, and verifying through simulation, multiple ICs have been added to the eSim subcircuit library.

This project highlights the growing importance of open-source EDA tools like eSim, which can be further developed to support a wider range of electronic components and simulation capabilities.

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3. μ A740
URL: <https://datasheet4u.com/datasheets/Fairchild/UA740/1305446>
4. μ A798
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