Semester Long Internship Spring 2026

On

Designing Integrated Circuits in eSim

Submitted by

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Acknowledgment

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This internship has been an enriching learning experience, allowing me to work closely with open-source EDA tools, develop IC subcircuits in eSim, and gain exposure to real-world circuit modeling and simulation workflows. The knowledge acquired during this period will undoubtedly support my future academic and professional pursuits.

I would also like to thank the entire FOSSEE team for their coordination, assistance, and timely interactions at various stages of this work. Their collective efforts ensured smooth workflow, resource accessibility, and effective project execution.

Contents

Chapter 1

Introduction

1.1 FOSSEE

FOSSEE, which stands for Free/Libre and Open Source Software for Education, is an organization based at IIT Bombay [1]. It is a remarkable initiative aimed at promoting the use of open-source software in education and research. It was established with the mission to reduce dependency on proprietary software and to encourage the adoption of open-source alternatives. FOSSEE offers a wide range of tools and resources that cater to various academic and professional needs.

It provides comprehensive documentation, tutorials, workshops, and hands-on training sessions to empower students, educators, and professionals to leverage open-source software for their projects and coursework. The organization's commitment to fostering a collaborative and inclusive environment has significantly contributed to the democratization of technology and has opened up new avenues for innovation and learning.

1.2 eSim

eSim, created by the FOSSEE project at IIT Bombay [2], is a versatile open-source software tool for circuit design and simulation. It combines various open-source software packages into one cohesive platform, making it easier to design, simulate, and analyze electronic circuits. This tool is particularly useful for students, educators, and professionals who need an affordable and accessible alternative to proprietary software.

eSim offers features for schematic creation, circuit simulation, and PCB design, and includes an extensive library of components. The Subcircuit feature is a significant enhancement, enabling users to design complex circuits by integrating simpler subcircuits. Through eSim, FOSSEE promotes the use of open-source solutions in engineering education and professional fields, encouraging innovation and collaboration.

1.3 NgSpice

NgSpice is an open-source SPICE simulator for electric and electronic circuits. It can simulate various circuit elements, including JFETs, bipolar and MOS transistors, passive elements (R, L, C), diodes and other devices, all interconnected in a netlist.

Digital circuits are also simulated, ranging from single gates to complex circuits, including combinations of analog, digital, and mixed-signal circuits. NgSpice offers a wealth of device models for active, passive, analog, and digital elements. Users input their circuits as netlists, and the output is one or more graphs of currents, voltages, and other electrical quantities, or saved in a data file.

1.4 Makechip

Makechip is a platform that offers convenient and accessible tools for digital circuit design. It provides both browser-based and desktop-based environments for coding, compiling, simulating, and debugging Verilog designs. Makechip supports a combination of open-source and proprietary tools, ensuring a comprehensive range of capabilities.

Users can simulate Verilog/SystemVerilog/Transaction-Level Verilog code in Makechip. eSim is interfaced with Makechip using a Python-based application called Makechip-App, which launches the Makechip IDE. Makechip aims to make circuit design easy and enjoyable for users of all skill levels. The platform provides a userfriendly interface, intuitive workflows, and a range of helpful features that simplify the design process and enhance the overall user experience.

The main drawback of these open-source tools is that they are not comprehensive. While some are capable of PCB design (e.g., KiCad), others focus on simulations (e.g., gEDA). To the best of our knowledge, there is no open-source software that combines circuit design, simulation, and layout design in one platform. eSim addresses this gap by integrating all these capabilities.

Chapter 2

Features of eSim

The objective behind the development of eSim is to provide an open-source EDA solution for electronics and electrical engineers. The software is capable of performing schematic creation, PCB design, and circuit simulation (analog, digital, and mixedsignal). It also provides facilities to create new models and components. Thus, eSim offers the following features:

1. Schematic Creation: eSim provides an easy-to-use graphical interface for drawing circuit schematics, making it accessible for users of all levels. Users can drag and drop components from the library onto the schematic, simplifying the design process. Comprehensive editing tools allow for easy modification of schematics, including moving, rotating, and labeling components.

2. Circuit Simulation: eSim supports SPICE (Simulation Program with Integrated Circuit Emphasis), a standard for simulating analog and digital circuits. Users can perform various types of analysis such as transient, AC, and DC, providing insights into circuit behavior over time and frequency. An integrated waveform viewer helps visualize simulation results, aiding in the analysis and debugging of circuit designs.

3. PCB Design: The PCB layout editor allows users to place components and route traces with precision. eSim includes DRC (Design Rule Check) capabilities to ensure that the PCB design adheres to manufacturing constraints and electrical rules. Users can generate Gerber files, which are standard for PCB fabrication, directly from their designs.

4. Subcircuit Feature: This feature enables users to create complex circuits by integrating smaller, simpler subcircuits, promoting modular and hierarchical design approaches. Subcircuits can be reused in different projects, saving time and effort in redesigning common circuit elements.

5. Open Source Integration: eSim integrates several open-source tools like KiCad, NgSpice, and GHDL, providing a comprehensive suite for electronic design automation. Being open-source, eSim is free to use, making advanced circuit design tools accessible without the need for expensive licenses.

Chapter 3

Problem Statement

To design and develop various analog and digital integrated circuit models in the form of sub-circuits using device model files already present in the eSim library. These IC models should be useful for future circuit design purposes by developers and users once they are successfully integrated into the eSim sub-circuit library.

3.1 Approach

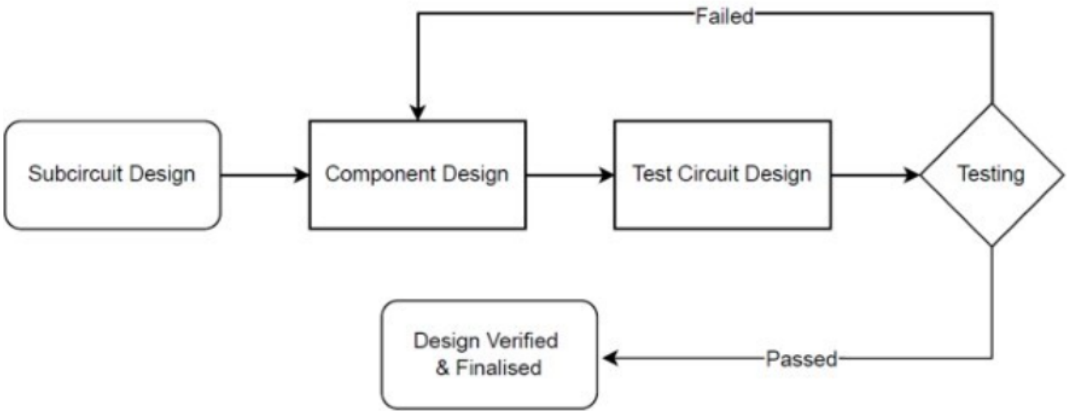

Figure 3.1: Flowchart of IC Design Approach Followed

Our approach to implementing the problem statement involved a systematic process, leveraging datasheets from leading Integrated Circuit (IC) manufacturers such as Texas Instruments, Analog Devices, and NXP Semiconductors. We focused on selecting ICs with diverse functionalities, including precision amplifiers, comparators, encoders, and audio amplifiers. The process is outlined in the following steps:

1. Analyzing Datasheets: The first step involved an in-depth review of datasheets for various analog and digital ICs. We aimed to identify circuits suitable for implementation in eSim that were not already present in the eSim library. This process included scrutinizing the detailed schematics of each IC, evaluating component values, and under-

standing truth tables. The goal was to select ICs that offered unique functionalities or enhancements not yet covered.

2. Subcircuit Creation: After selecting appropriate ICs, we proceeded to model these as sub-circuits within eSim. We utilized the model files available in the eSim device model library and ensured that our designs adhered strictly to the specifications outlined in the official datasheets. This phase also involved creating accurate symbol and pin diagrams for each IC, in accordance with the packaging and pin descriptions provided in the datasheets. This step was crucial for ensuring the fidelity of the subcircuit models.

3. Test Circuit Design: With the sub-circuits created, we then designed and built test circuits based on the datasheets. This step was essential for verifying the functionality of each sub-circuit. We developed a series of test cases and constructed corresponding test circuits to evaluate the performance and accuracy of the implemented IC models.

4. Schematic Testing: Following the construction of test circuits, we conducted simulations to analyze the outputs. This involved generating waveforms and plots to assess the behavior of the circuits. We employed KiCad for converting designs to NgSpice netlists and utilized eSim's simulation features to perform comprehensive testing.

If the simulated outputs deviated from expected results, it signaled potential errors in the schematic. In such instances, we revisited the design phase to identify and correct discrepancies. The iterative process of debugging and re-testing continued until the test cases produced satisfactory results. Once the IC models met the desired performance criteria, they were deemed successful, marking the completion of the design process.

Chapter 4

74LS31

4.1 General Description

The 74LS31 is a Hex Delay Element belonging to the Low-Power Schottky TTL logic family. It contains six independent delay elements designed to introduce controlled propagation delays in digital circuits. The device is commonly used for timing adjustments, pulse shaping, and synchronization applications. Its low-power Schottky technology ensures fast switching performance with reduced power consumption. The IC is TTL compatible and suitable for a wide range of digital systems.

4.2 Key Features

- Contains six independent delay elements.
- Low-Power Schottky TTL technology.
- Provides controlled signal propagation delay.
- High-speed switching performance.
- TTL-compatible inputs and outputs.

4.3 Applications

- Digital timing circuits.
- Pulse shaping applications.
- Clock synchronization systems.
- Delay generation networks.
- Signal conditioning circuits.

4.4 Subcircuit

The 74LS31 Hex Delay Element was implemented as a subcircuit in eSim using logic elements that introduce a fixed propagation delay. The subcircuit accurately replicates the timing behavior specified in the datasheet.

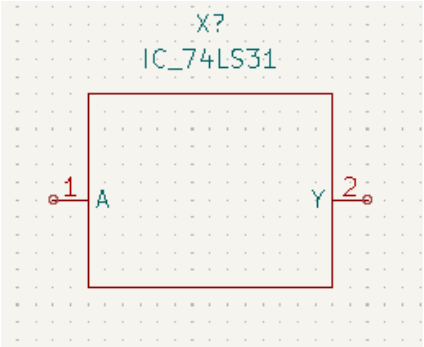

Figure 4.1: Subcircuit of 74LS31

4.5 Subcircuit Schematic Diagram

The schematic diagram illustrates the internal arrangement of the six delay elements. Each section provides a controlled delay to the input signal before producing the corresponding output.

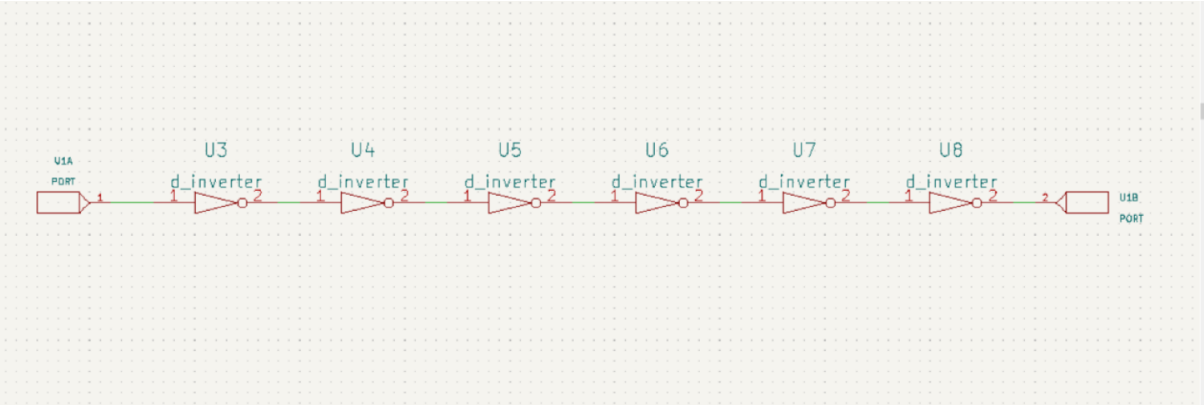

Figure 4.2: Subcircuit Schematic of 74LS31

4.6 Test Circuit

A test circuit was designed to verify the delay characteristics of the device. Pulse inputs were applied and the delayed outputs were observed through simulation.

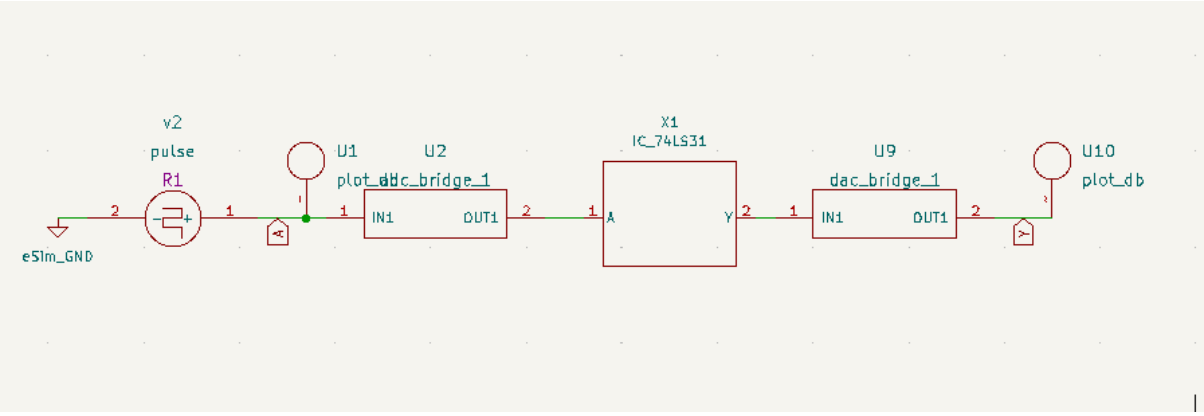

Figure 4.3: Test Circuit of 74LS31

4.7 Function Table

INPUT A_n	OUTPUT Y_n	FUNCTION
L	L (after t_{PLH})	If A_n is LOW, Y_n becomes LOW after propagation delay (t_{PLH})
H	H (after t_{PHL})	If A_n is HIGH, Y_n becomes HIGH after propagation delay (t_{PHL})
X	X (after t_{PZ})	If A_n changes from HIGH to LOW, Y_n changes to LOW after t_{PZL}
X	X (after t_{PZL})	If A_n changes from LOW to HIGH, Y_n changes to HIGH after t_{PZLL}

Figure 4.4: Function Table of 74LS31

4.8 Output Plot

The output waveform confirms the expected propagation delay between input and output signals. The results match the functional behavior described in the datasheet.

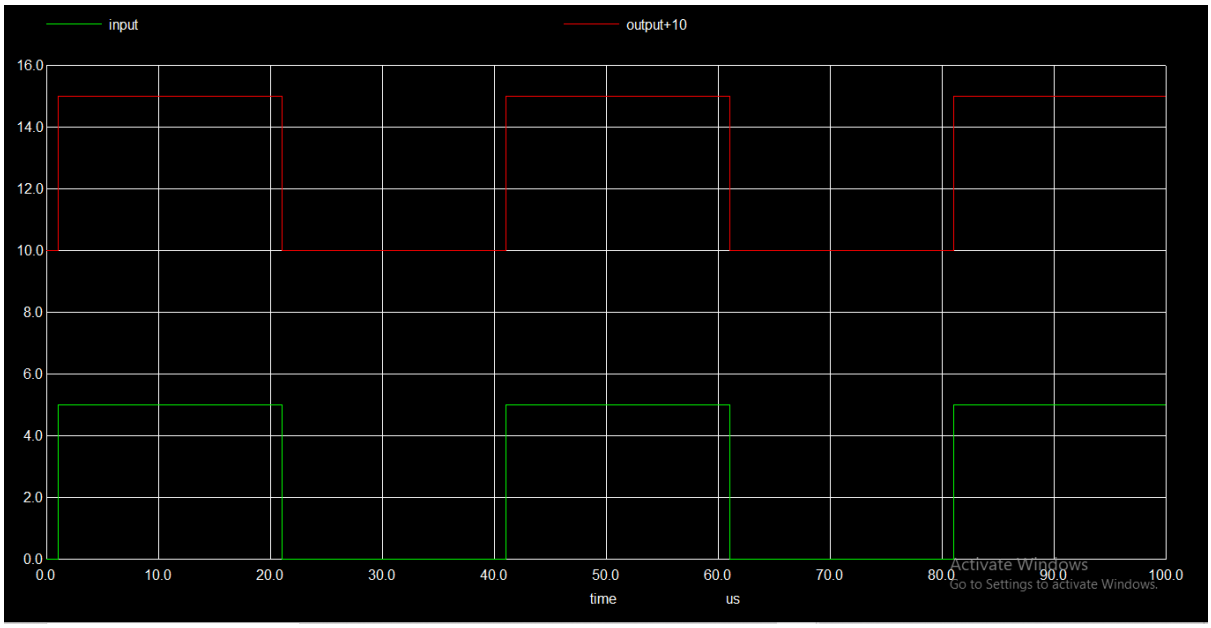

Figure 4.5: Output Plot of 74LS31

Chapter 5

NA53

5.1 General Description

The NA53 is a 5-input NAND gate integrated circuit designed for implementing wide-input digital logic functions. The device performs the NAND operation on five independent input signals and generates a single output. It is useful in combinational logic applications where multiple conditions must be evaluated simultaneously. The IC offers reliable switching performance and compatibility with standard digital logic families. Its compact implementation reduces component count in digital systems.

5.2 Key Features

- Five independent logic inputs.
- Performs NAND logic operation.
- High-speed digital switching.
- TTL-compatible operation.
- Compact hardware implementation.

5.3 Applications

- Combinational logic circuits.
- Control logic implementation.
- Digital processing systems.
- Embedded system applications.
- Logic function generation.

5.4 Subcircuit

The NA53 5-input NAND gate was modeled as an eSim subcircuit using CMOS logic gates. The design performs the NAND operation on five independent inputs.

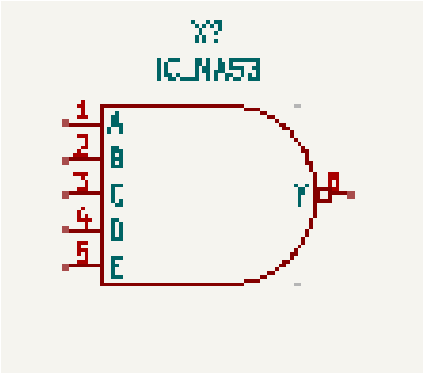

Figure 5.1: Subcircuit of NA53

5.5 Subcircuit Schematic Diagram

The schematic diagram shows the implementation of the five-input NAND function. The arrangement ensures correct logical operation for all possible input combinations.

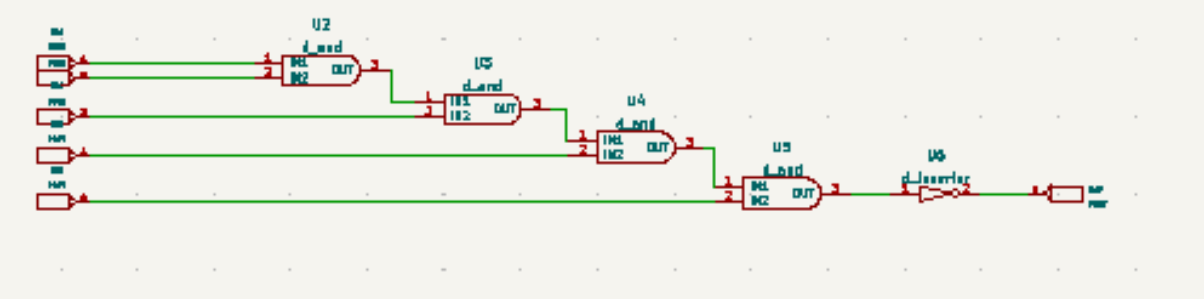

Figure 5.2: Subcircuit Schematic of NA53

5.6 Test Circuit

The test circuit applies different combinations of logic inputs to validate the NAND functionality. Simulation results were monitored to verify correctness.

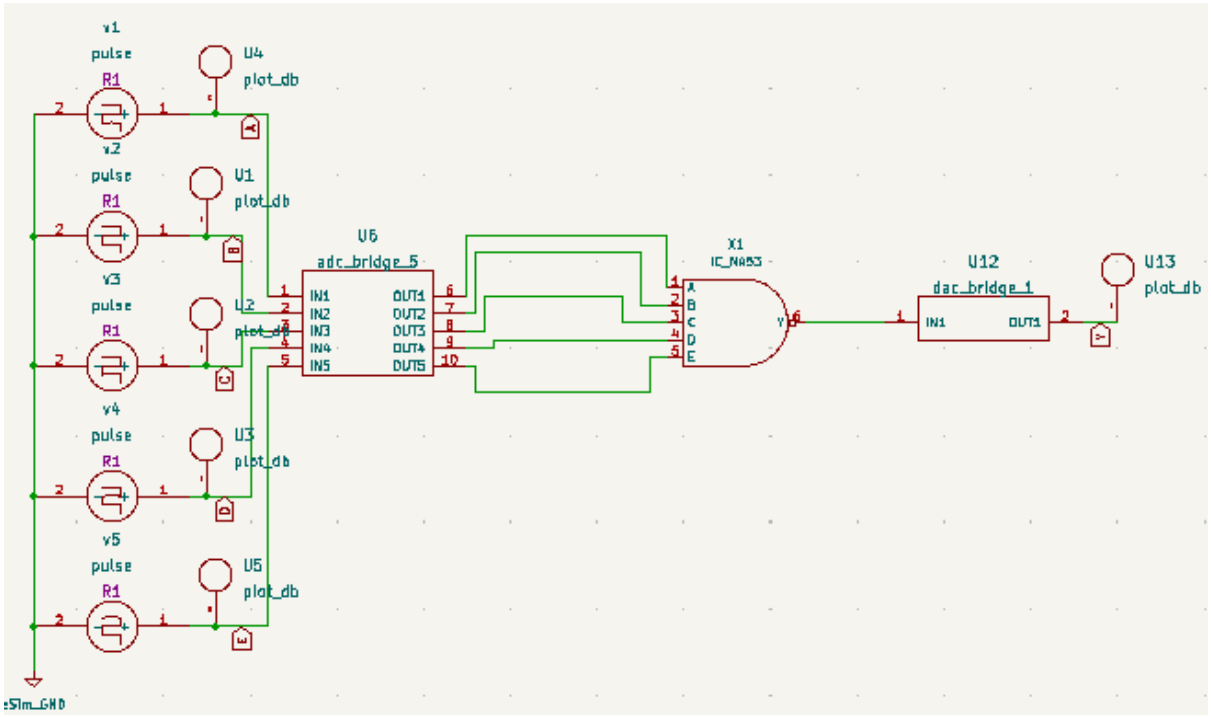

Figure 5.3: Test Circuit of NA53

5.7 Function Table

A	B	C	D	E	Q
L	X	X	X	X	H
X	L	X	X	X	H
X	X	L	X	X	H
X	X	X	L	X	H
X	X	X	X	L	H
H	H	H	H	H	L

Figure 5.4: Function Table of NA53

5.8 Output Plot

The output waveform demonstrates proper NAND gate operation. The output remains LOW only when all five inputs are HIGH.

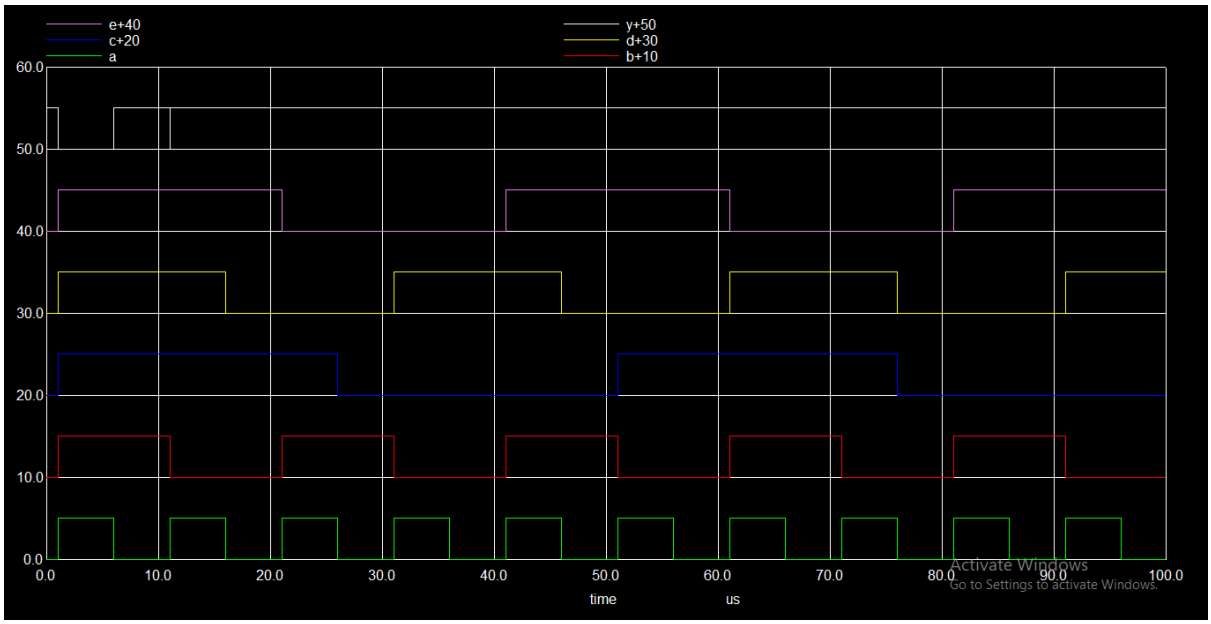

Figure 5.5: Output Plot of NA53

Chapter 6

OR73

6.1 General Description

The OR73 is a 7-input OR gate featuring enhanced drive capability. It performs logical OR operations on seven independent input signals and provides a single output. The device is designed for applications requiring high fan-out capability and reliable signal driving. Its increased drive strength allows direct interfacing with multiple digital loads. The IC is suitable for high-performance digital logic systems.

6.2 Key Features

- Seven independent input lines.
- Performs OR logic operation.
- 3x output drive capability.
- High fan-out support.
- Fast switching characteristics.

6.3 Applications

- Logic combination circuits.
- Digital control systems.
- Signal aggregation networks.
- High fan-out applications.
- Embedded systems.
- Industrial digital controllers.

6.4 Subcircuit

The OR73 device was implemented as a seven-input OR gate with enhanced drive capability. The subcircuit combines seven logic inputs into a single output signal.

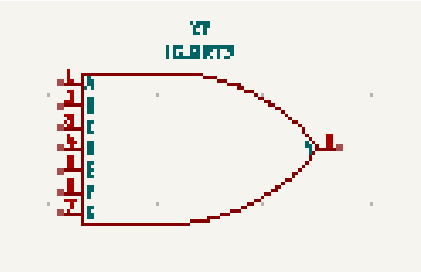

Figure 6.1: Subcircuit of OR73

6.5 Subcircuit Schematic Diagram

The schematic illustrates the internal OR gate structure used to realize the seven-input logic function. The design supports reliable digital operation.

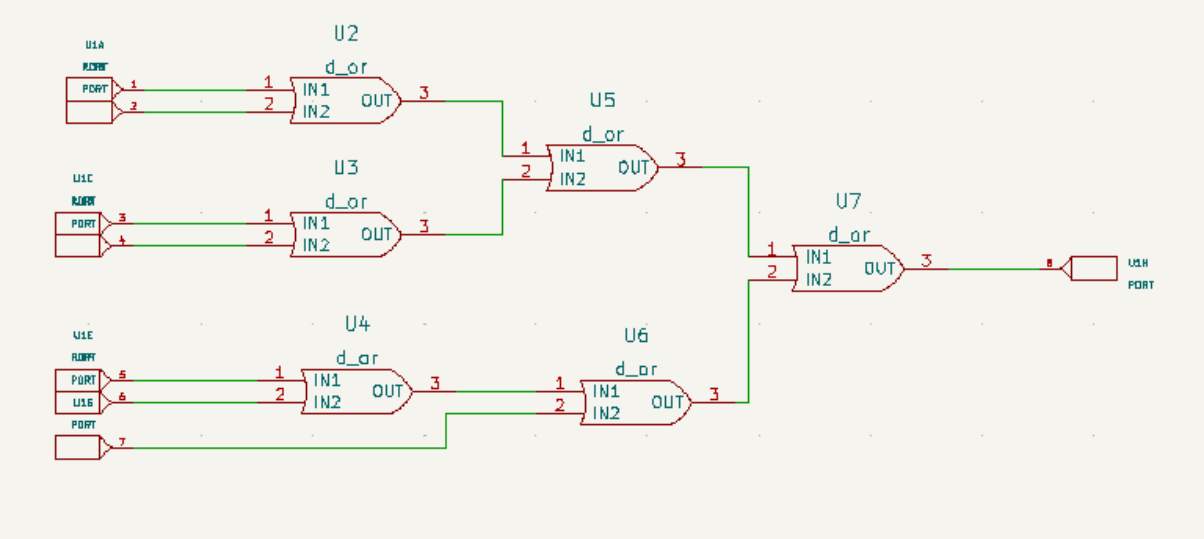

Figure 6.2: Subcircuit Schematic of OR73

6.6 Test Circuit

A dedicated test circuit was developed to evaluate all major input combinations. Various logic patterns were applied to verify correct operation.

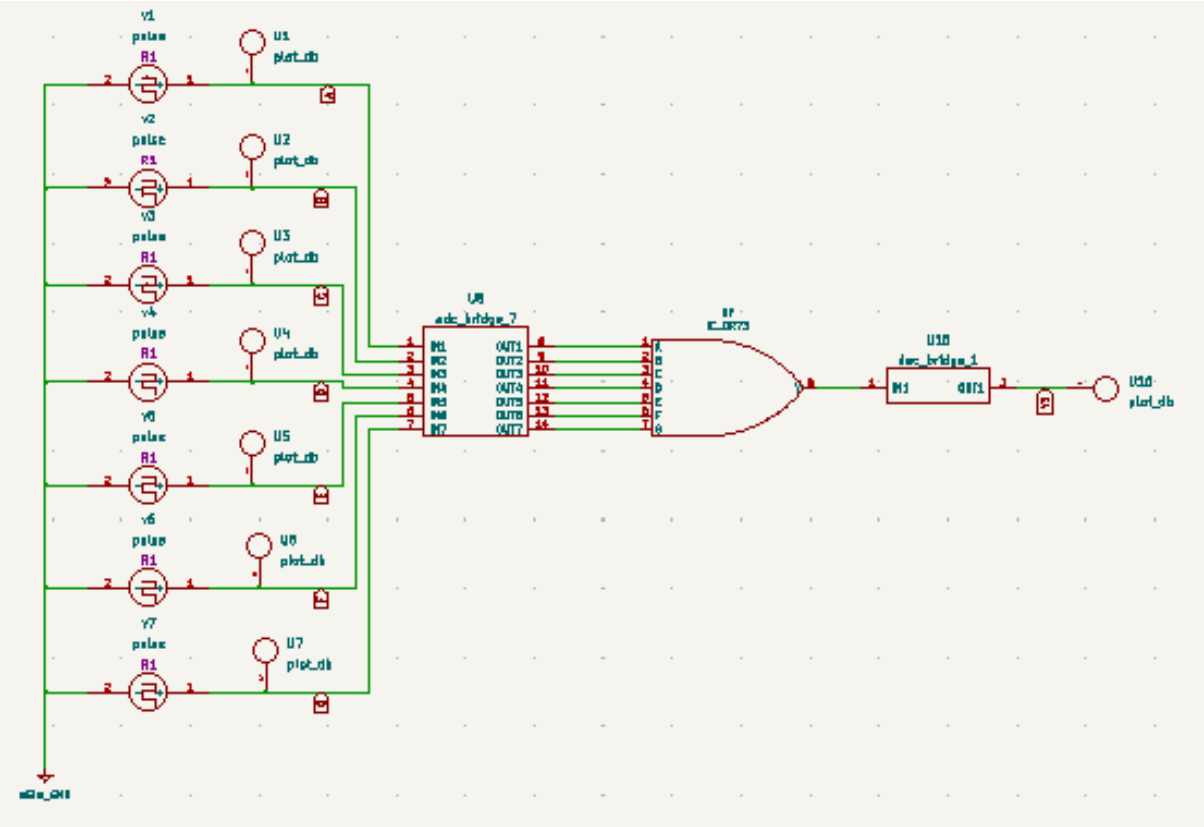

Figure 6.3: Test Circuit of OR73

6.7 Function Table

A	B	C	D	E	F	G	Q
L	L	L	L	L	L	L	L
H	X	X	X	X	X	X	H
X	H	X	X	X	X	X	H
X	X	H	X	X	X	X	H
X	X	X	H	X	X	X	H
X	X	X	X	H	X	X	H
X	X	X	X	X	H	X	H
X	X	X	X	X	X	H	H

Figure 6.4: Function Table of OR73

6.8 Output Plot

The output waveform confirms that the output becomes HIGH whenever any input is HIGH. The simulated results match the expected truth table.

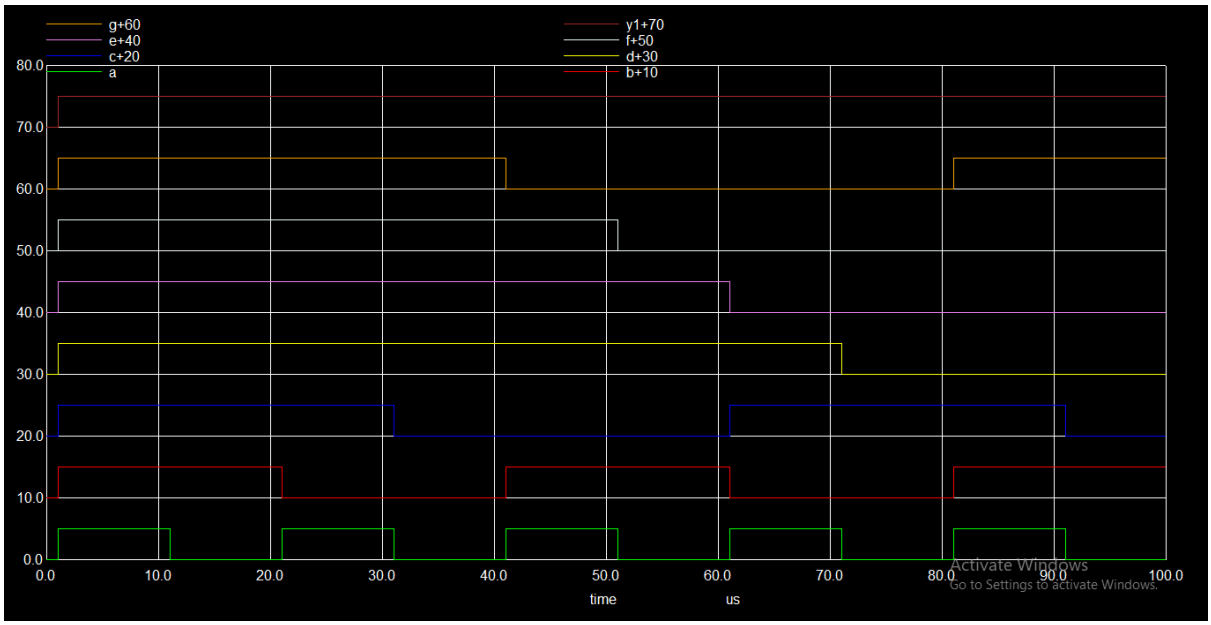

Figure 6.5: Output Plot of OR73

Chapter 7

GD74HCT58

7.1 General Description

The GD74HCT58 is a dual AND-OR gate integrated circuit from the HCT logic family. It combines multiple AND gates followed by OR gate stages to implement complex combinational logic functions. The device provides TTL-compatible input thresholds while operating with CMOS technology. It offers low power consumption and high noise immunity. The IC is widely used in logic control and decision-making circuits.

7.2 Key Features

- Dual AND-OR gate configuration.
- CMOS implementation.
- TTL-compatible inputs.
- High noise immunity.
- Low power consumption.
- High-speed operation.

7.3 Applications

- Logic control circuits.
- Digital decision-making systems.
- Embedded applications.
- Industrial automation.
- Data processing circuits.

7.4 Subcircuit

The GD74HCT58 dual AND-OR gate was implemented as an eSim subcircuit. The design combines multiple AND stages followed by OR logic to achieve the required function.

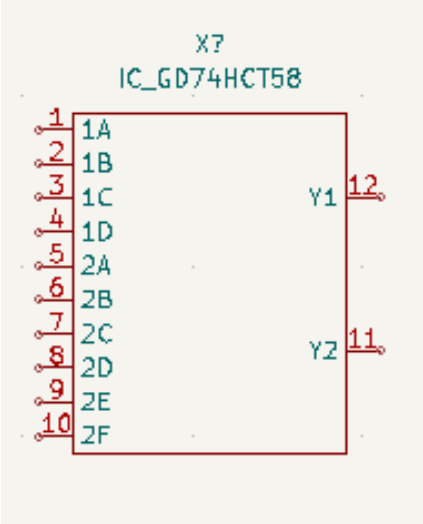

Figure 7.1: Subcircuit of GD74HCT58

7.5 Subcircuit Schematic Diagram

The schematic diagram presents the arrangement of the AND and OR gates within the circuit. The structure accurately reproduces the device functionality.

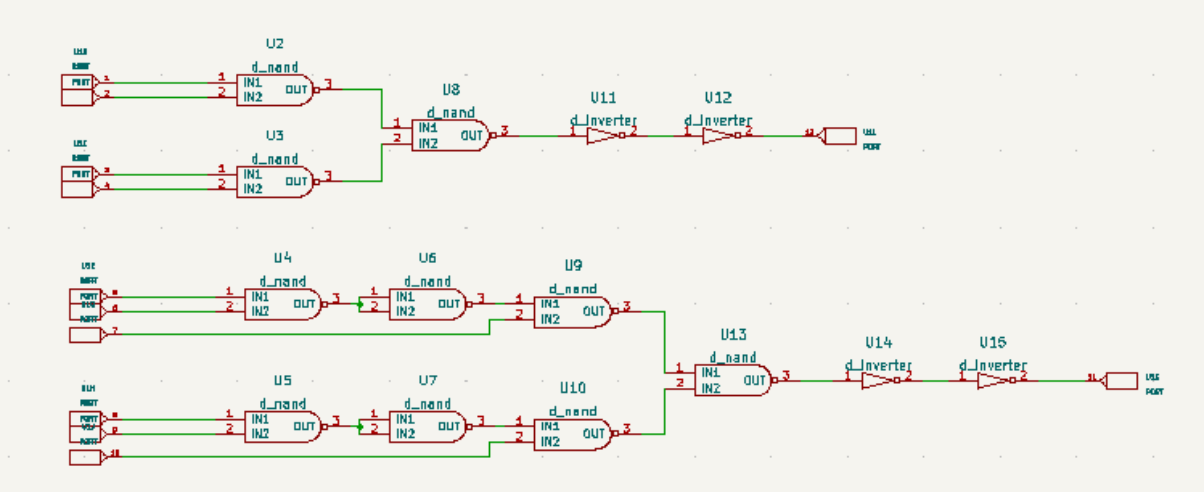

Figure 7.2: Subcircuit Schematic of GD74HCT58

7.6 Test Circuit

A test circuit was created to validate the AND-OR logic operations. Different input combinations were applied to verify the output response.

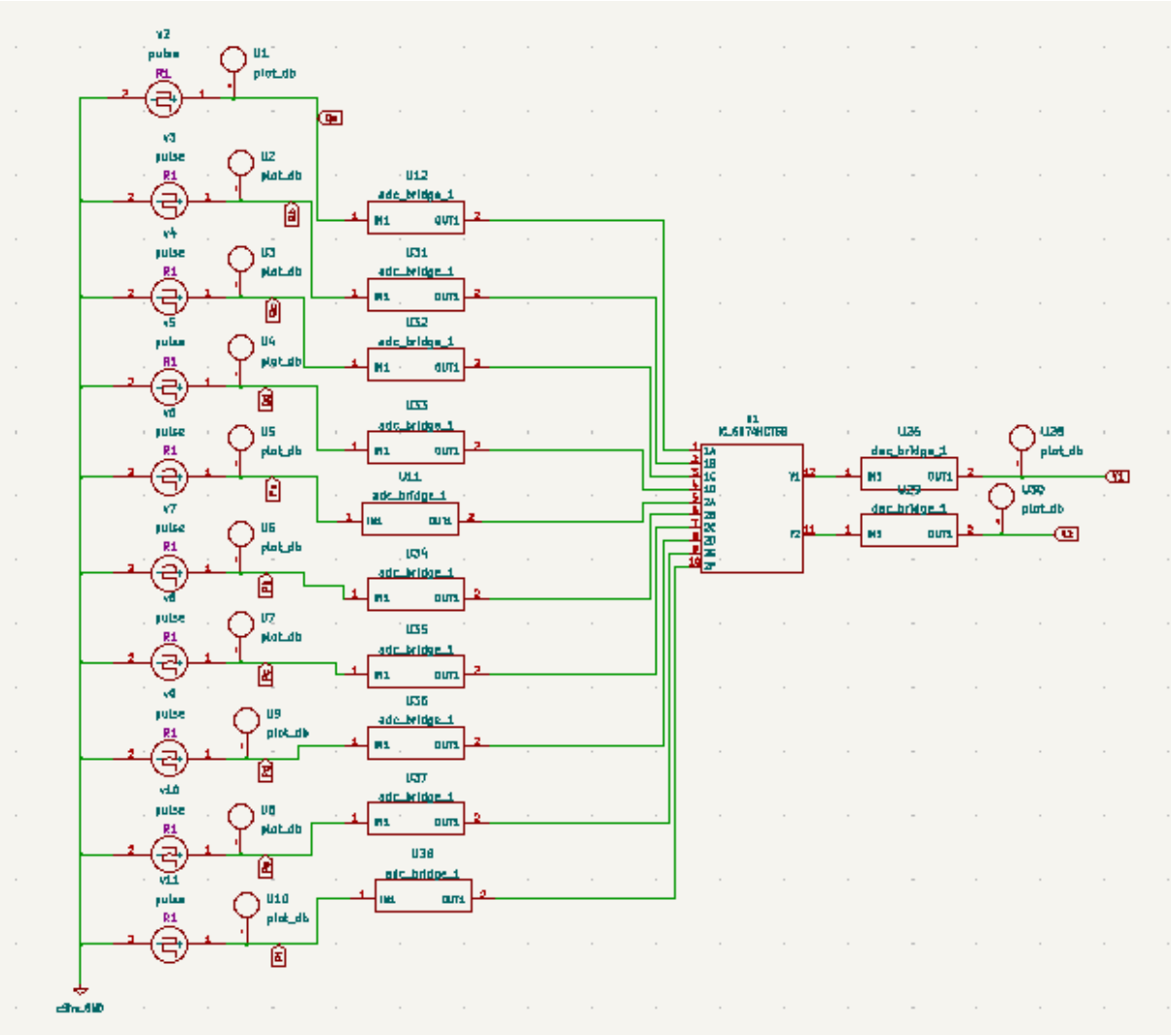

Figure 7.3: Test Circuit of GD74HCT58

7.7 Function Table

INPUTS		OUTPUT
N*	M*	nY
L	L	L
H	L	H
L	H	H
H	H	H

Figure 7.4: Function Table of GD74HCT58

7.8 Output Plot

The output waveform demonstrates correct logical behavior for all tested input conditions. The results are consistent with the datasheet specifications.

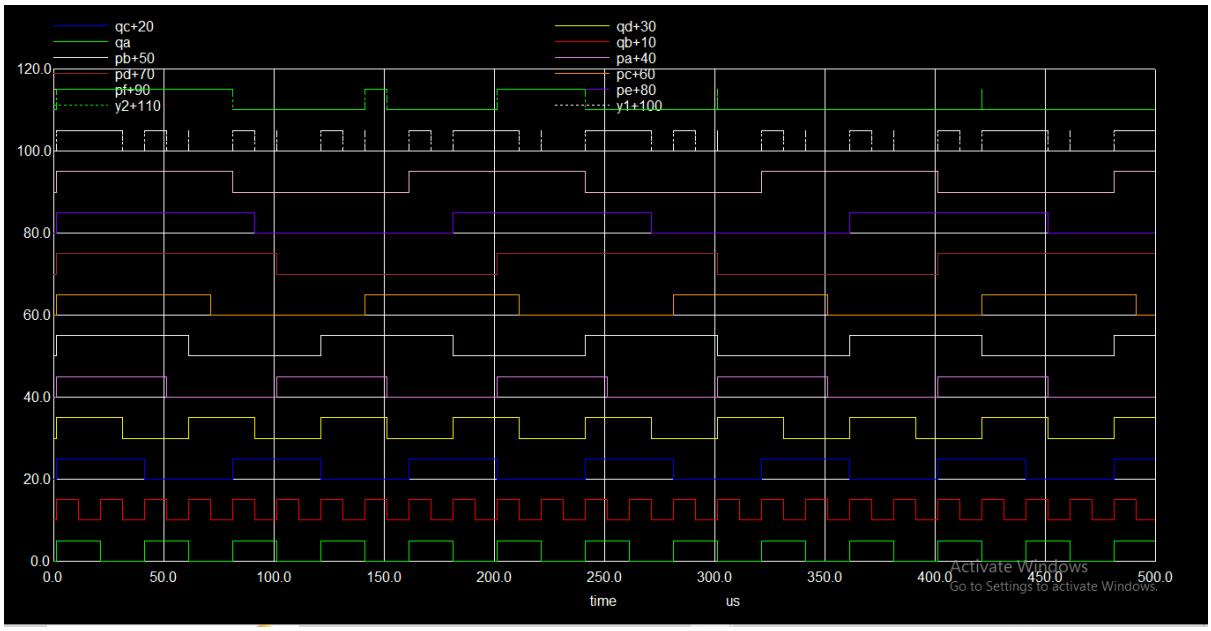

Figure 7.5: Output Plot of GD74HCT58

Chapter 8

DM8098

8.1 General Description

The DM8098 is a tristate hex inverting buffer designed for digital bus interfacing applications. It contains six independent inverting buffers with tristate outputs. The device allows outputs to be enabled or placed in a high-impedance state for bus sharing applications. It improves signal integrity and reduces loading effects in digital systems. The IC is widely used in microprocessor and memory interfacing circuits.

8.2 Key Features

- Six independent inverting buffers.
- Tristate output capability.
- Bus isolation functionality.
- High-speed switching operation.
- TTL-compatible inputs and outputs.

8.3 Applications

- Bus-oriented systems.
- Memory interfacing circuits.
- Microprocessor applications.
- Signal buffering networks.
- Data transmission systems.
- Digital communication interfaces.

8.4 Subcircuit

The DM8098 tristate hex inverting buffer was developed as an eSim subcircuit. The design includes six inverting buffers with tristate output control.

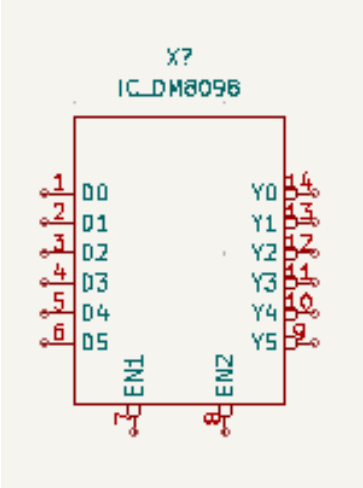

Figure 8.1: Subcircuit of DM8098

8.5 Subcircuit Schematic Diagram

The schematic diagram shows the implementation of the inverting buffers and output-enable circuitry. This arrangement allows normal and high-impedance operation.

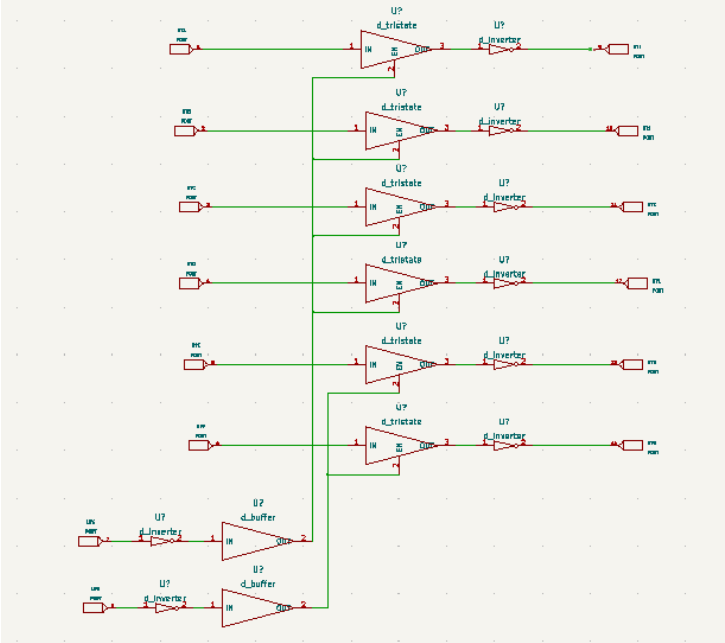

Figure 8.2: Subcircuit Schematic of DM8098

8.6 Test Circuit

The test circuit verifies both inversion and tristate functionality. Input signals and enable controls were varied during simulation.

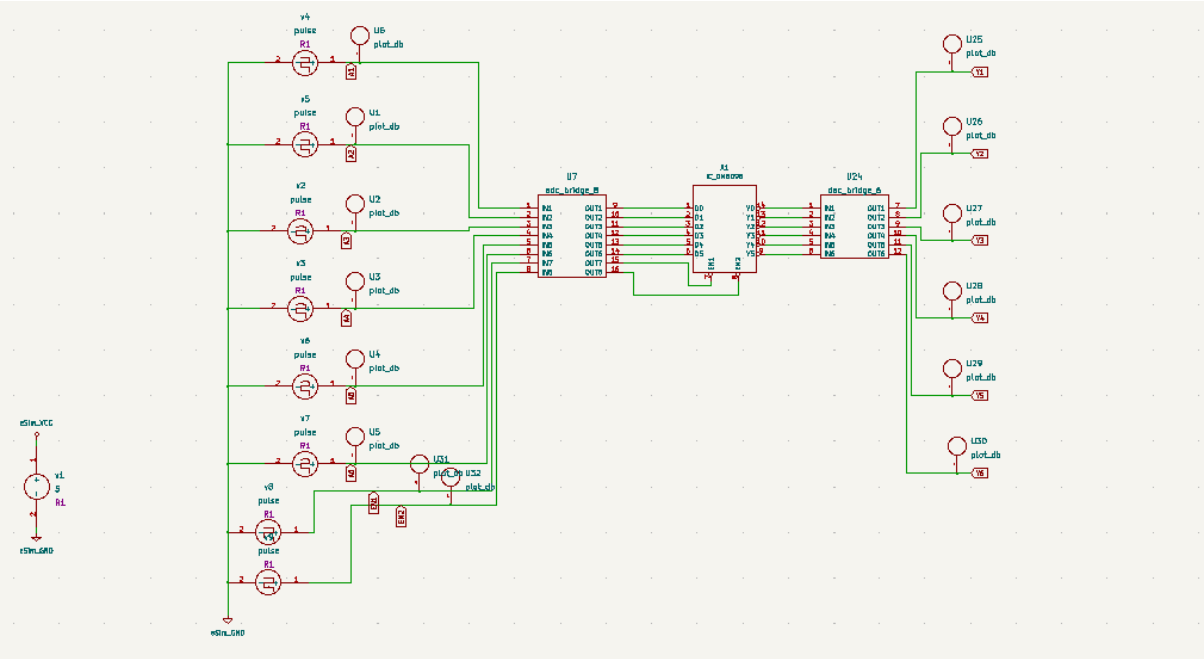

Figure 8.3: Test Circuit of DM8098

8.7 Function Table

98, L98

Inputs		Outputs
$\overline{G}$	A	Y
H	X	Hi-Z
L	H	L
L	L	H

Figure 8.4: Function Table of DM8098

8.8 Output Plot

The output waveform confirms proper inversion of input signals and correct tristate behavior. High-impedance states are observed when outputs are disabled.

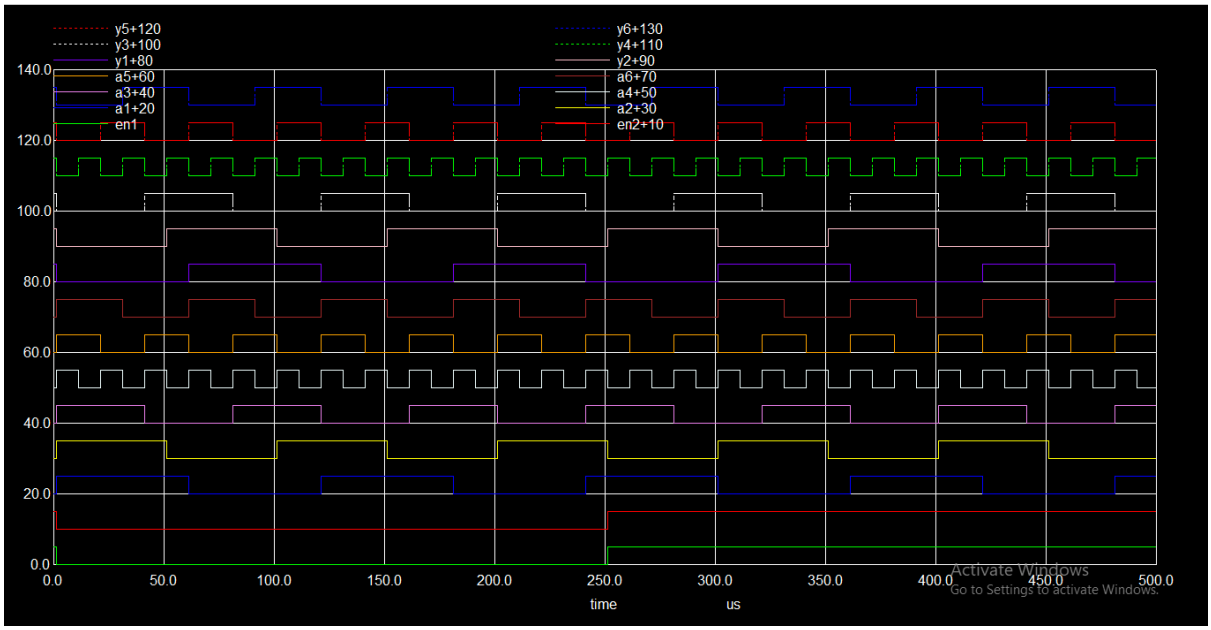

Figure 8.5: Output Plot of DM8098

Chapter 9

CD74AC174

9.1 General Description

The CD74AC174 is a hex D-type flip-flop featuring six edge-triggered storage elements. Each flip-flop stores one bit of data and transfers the input value to the output on the active clock edge. The device includes a common clock and master reset functionality. Advanced CMOS technology provides high-speed performance with low power consumption. It is widely used in registers and digital storage applications.

9.2 Key Features

- Six D-type flip-flops.
- Positive-edge-triggered operation.
- Common clock input.
- Master reset function.
- High-speed performance.
- Low power consumption.

9.3 Applications

- Data storage registers.
- Shift register systems.
- Digital counters.
- Timing control circuits.
- Embedded systems.

9.4 Subcircuit

The CD74AC174 hex D-type flip-flop was implemented using edge-triggered storage elements. The subcircuit provides six independent data storage channels.

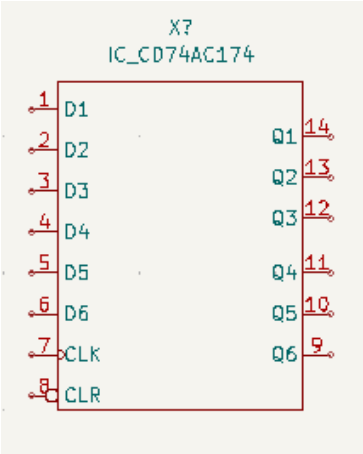

Figure 9.1: Subcircuit of CD74AC174

9.5 Subcircuit Schematic Diagram

The schematic illustrates the internal flip-flop arrangement and common clock structure. The design follows the functional organization of the actual device.

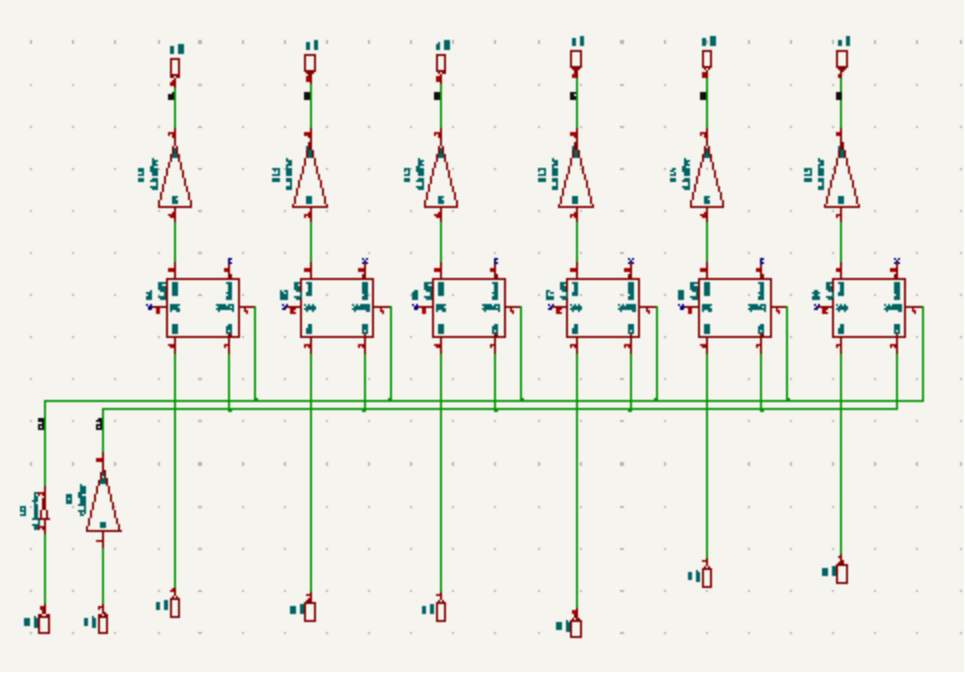

Figure 9.2: Subcircuit Schematic of CD74AC174

9.6 Test Circuit

A test circuit was designed to verify data storage and clock-triggered operation. Various input patterns were applied during simulation.

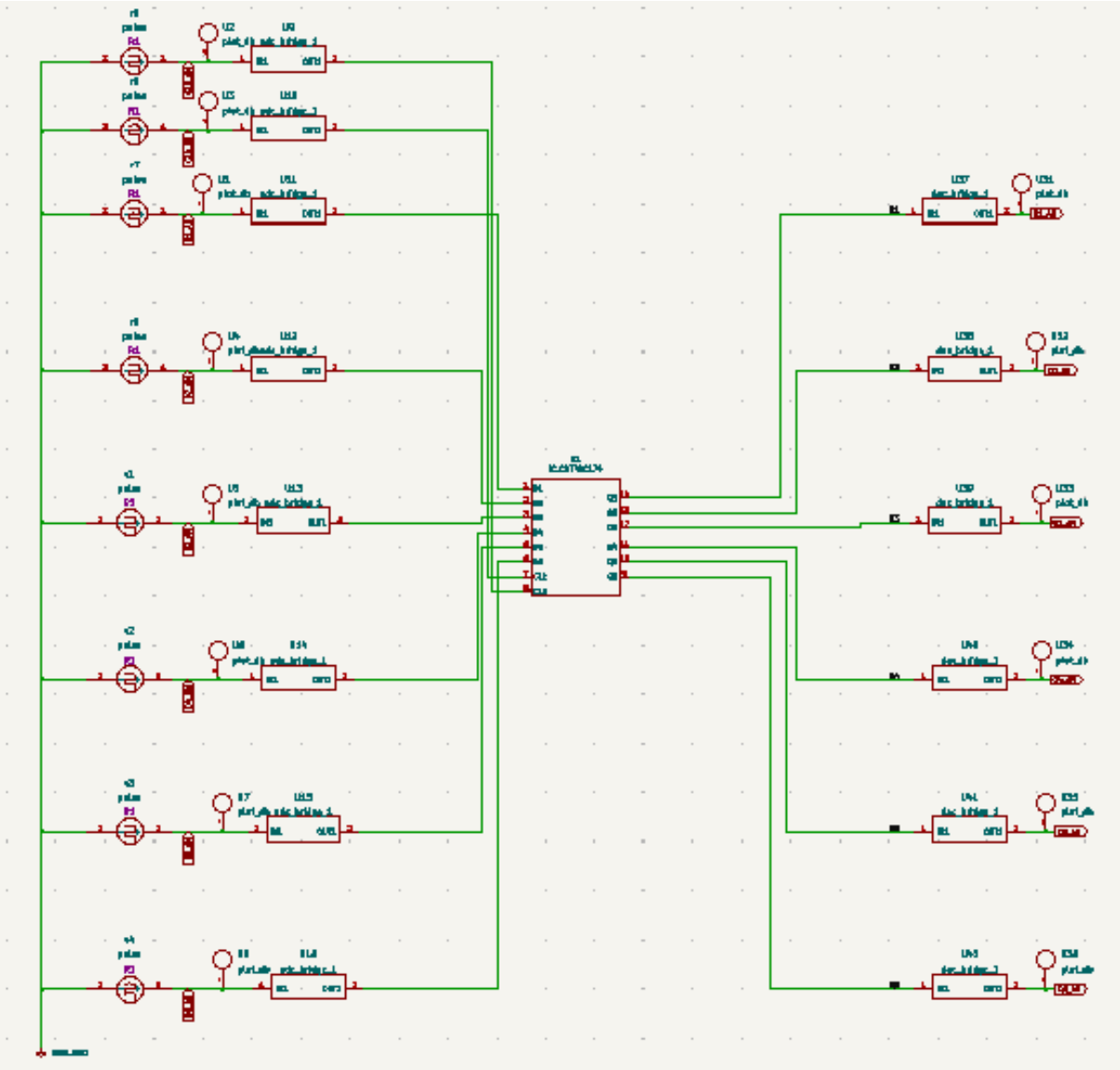

Figure 9.3: Test Circuit of CD74AC174

9.7 Function Table

INPUTS			OUTPUTS
RESET ($\overline{MR}$)	CLOCK CP	DATA Dn	Qn
L	X	X	L
H	↑	H	H
H	↑	L	L
H	L	X	Q0

Figure 9.4: Function Table of CD74AC174

9.8 Output Plot

The output waveform confirms that data is transferred to the outputs on the active clock edge. The simulation results agree with the expected operation.

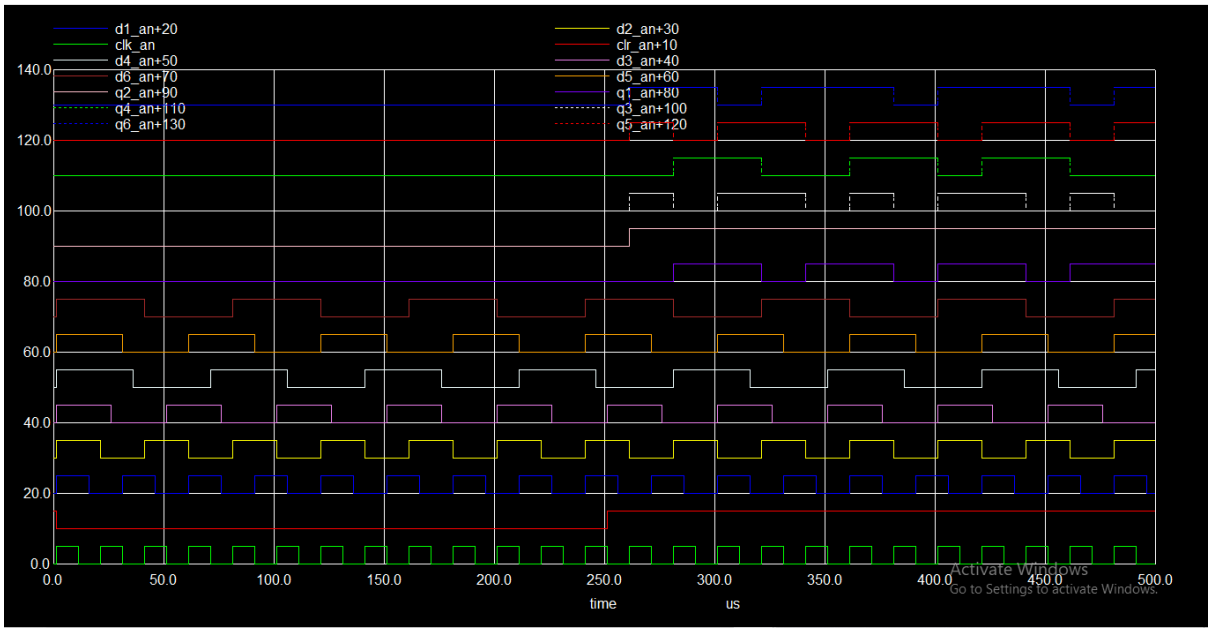

Figure 9.5: Output Plot of CD74AC174

Chapter 10

M74HC4024

10.1 General Description

The M74HC4024 is a 7-bit asynchronous binary counter implemented using high-speed CMOS technology. It divides the input clock frequency through a cascade of binary counter stages. Each stage provides a frequency output at half the frequency of the previous stage. The device offers low power consumption and high noise immunity. It is widely used in frequency division and timing applications.

10.2 Key Features

- Asynchronous ripple-counter operation.
- High-speed CMOS technology.
- Frequency division capability.
- Low power consumption.
- High noise immunity.

10.3 Applications

- Frequency dividers.
- Digital timers.
- Event counting systems.
- Clock generation circuits.
- Embedded controllers.
- Industrial automation.

10.4 Subcircuit

The M74HC4024 seven-bit asynchronous counter was implemented as an eSim subcircuit. The design uses cascaded flip-flops to perform binary counting.

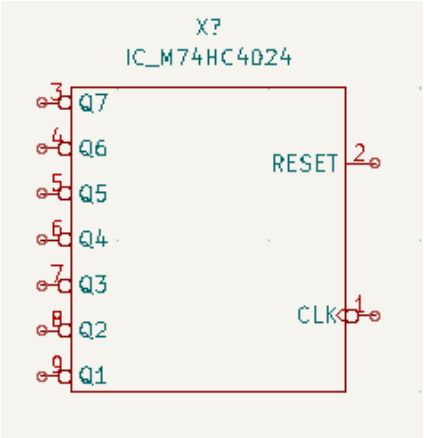

Figure 10.1: Subcircuit of M74HC4024

10.5 Subcircuit Schematic Diagram

The schematic diagram illustrates the ripple-counter configuration used in the implementation. Each stage divides the input frequency by two.

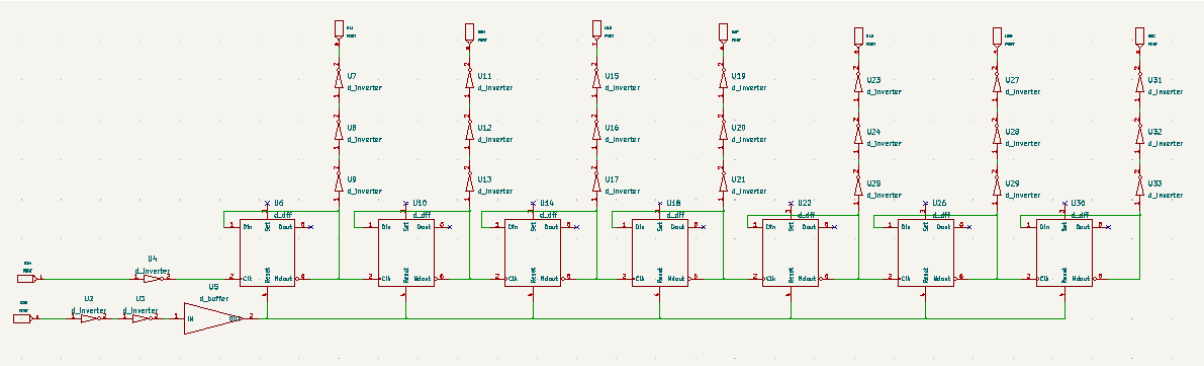

Figure 10.2: Subcircuit Schematic of M74HC4024

10.6 Test Circuit

A clock source and reset circuitry were used to test the counter operation. The output stages were monitored over multiple clock cycles.

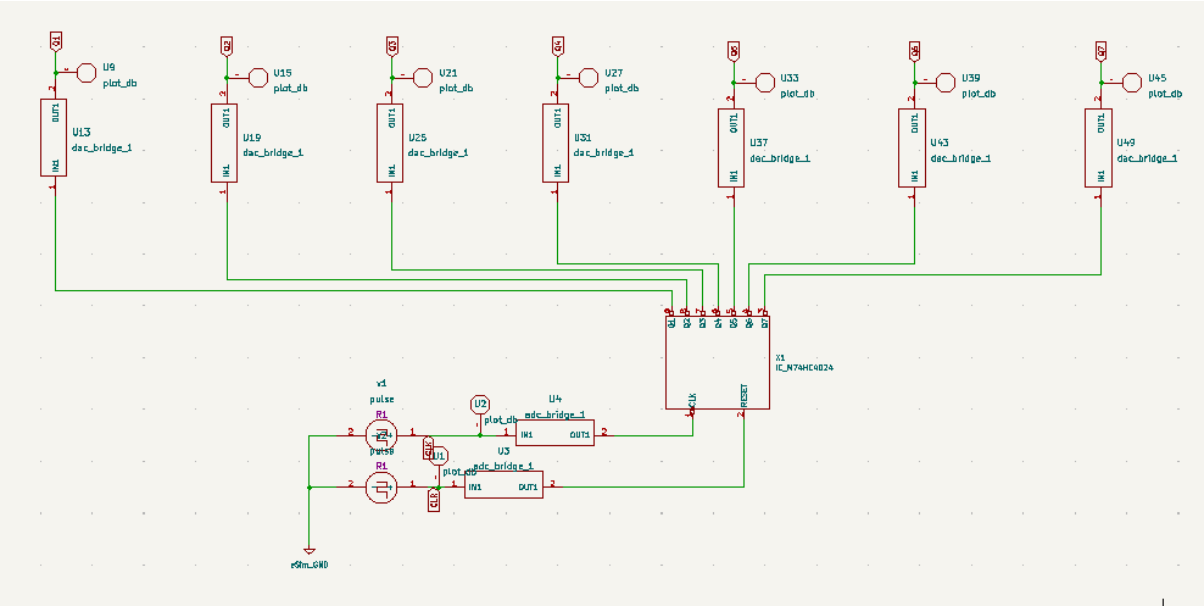

Figure 10.3: Test Circuit of M74HC4024

10.7 Function Table

CLOCK	CLEAR	OUTPUT STATE
X	H	ALL OUTPUTS = "L"
⎍	L	NO CHANGE
⎎	L	ADVANCE TO NEXT STATE

X: DON'T CARE

Figure 10.4: Function Table of M74HC4024

10.8 Output Plot

The output waveform demonstrates correct binary counting and frequency division. Each output exhibits the expected timing relationship.

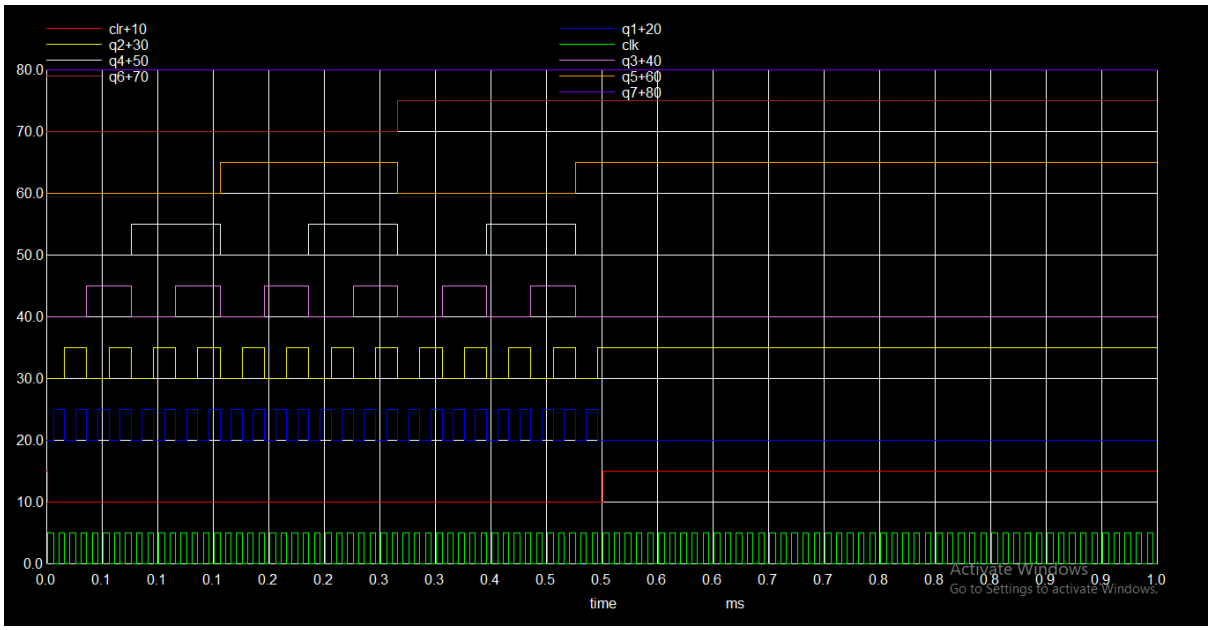

Figure 10.5: Output Plot of M74HC4024

Chapter 11

MC10E156

11.1 General Description

The MC10E156 is a high-speed 3-bit 4:1 multiplexer latch belonging to the ECL logic family. The device selects one of four input channels and stores the selected data using integrated latch circuitry. It provides extremely fast switching performance suitable for high-speed communication systems. Differential ECL operation ensures low propagation delays. The IC is commonly used in data routing and signal processing applications.

11.2 Key Features

- Three-bit wide data path.
- Four-to-one multiplexing function.
- High-speed ECL technology.
- Differential signal operation.
- Suitable for high-frequency systems.

11.3 Applications

- Data routing systems.
- Communication equipment.
- High-speed digital processing.
- Multiplexed data transmission.
- Test instrumentation.
- Signal selection networks.

11.4 Subcircuit

The MC10E156 3-bit 4:1 multiplexer latch was modeled as a high-speed eSim subcircuit. The design combines multiplexing and data latching functionality.

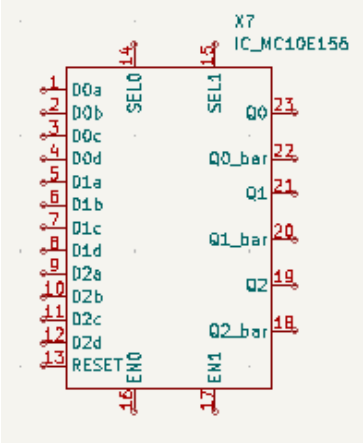

Figure 11.1: Subcircuit of MC10E156

11.5 Subcircuit Schematic Diagram

The schematic shows the multiplexer selection network and latch circuitry. The arrangement enables both data selection and storage operations.

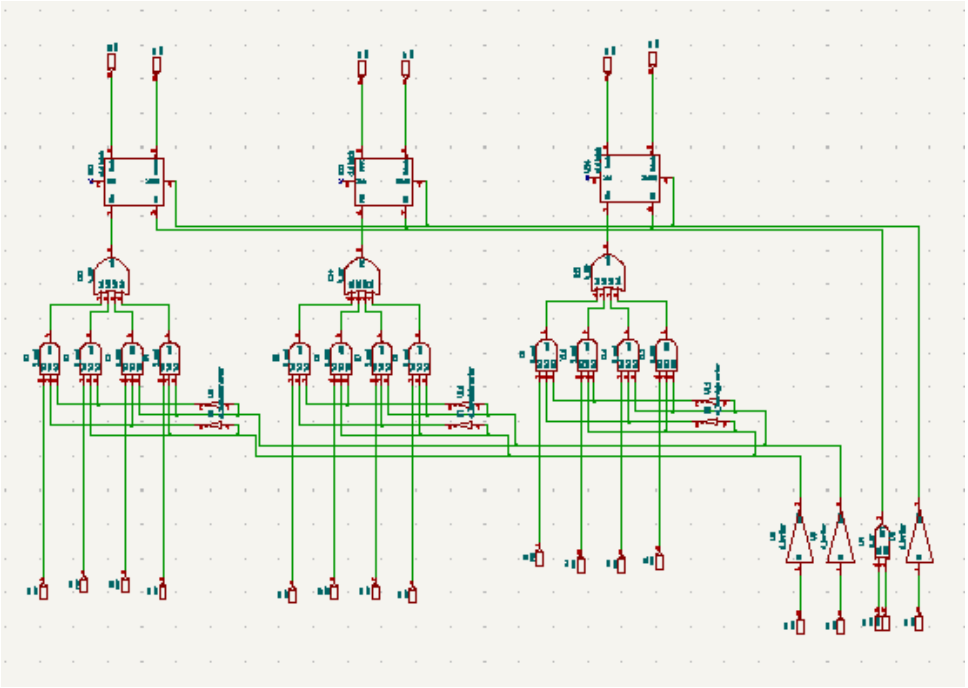

Figure 11.2: Subcircuit Schematic of MC10E156

11.6 Test Circuit

A test circuit was created to verify input selection and latch functionality. Various select and control signals were applied during simulation.

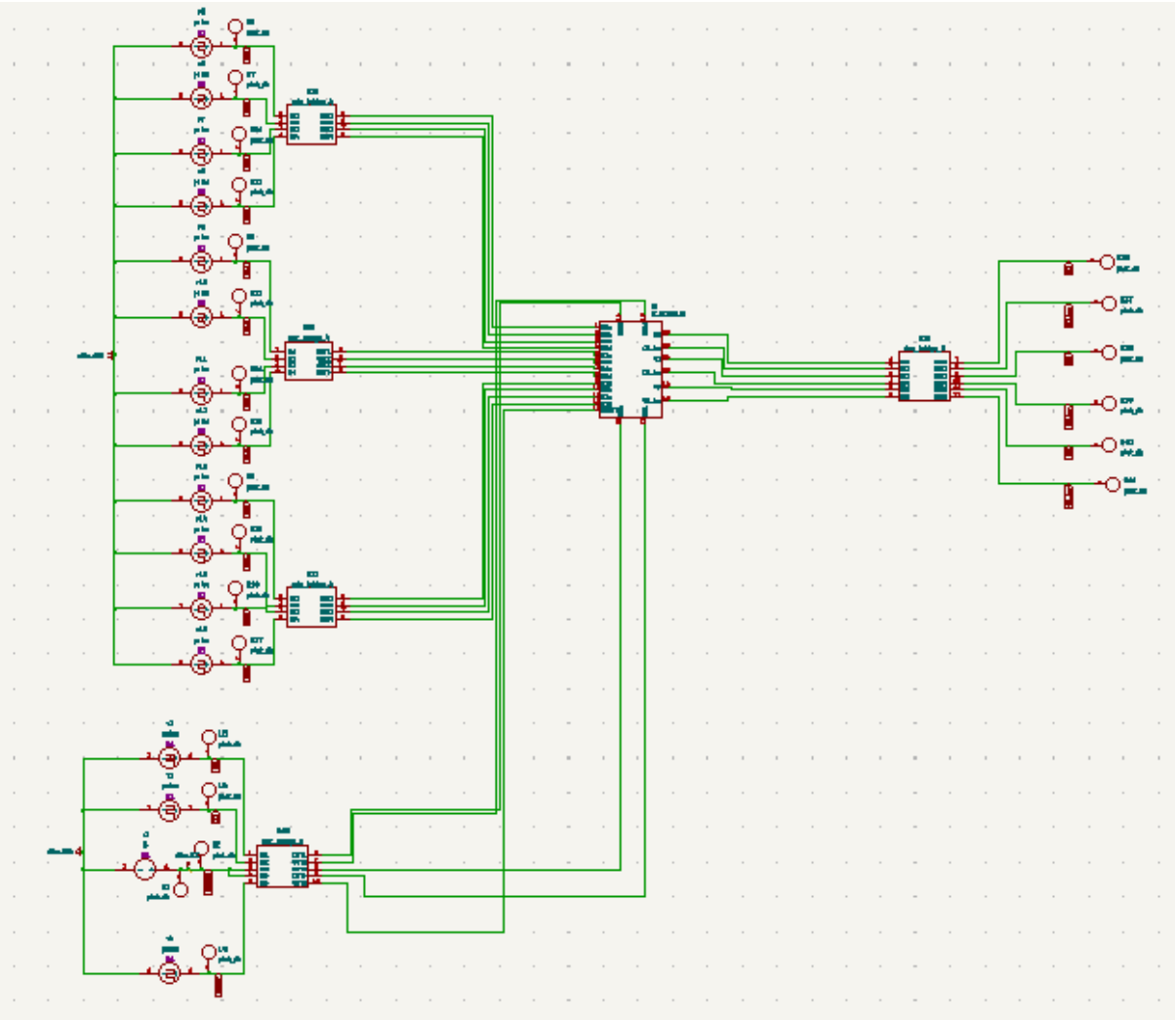

Figure 11.3: Test Circuit of MC10E156

11.7 Function Table

SEL1	SEL0	Data
L	L	a
L	H	b
H	L	c
H	H	d

Figure 11.4: Function Table of MC10E156

11.8 Output Plot

The output waveform confirms correct selection of input channels and proper latching behavior. The results match the intended device operation.

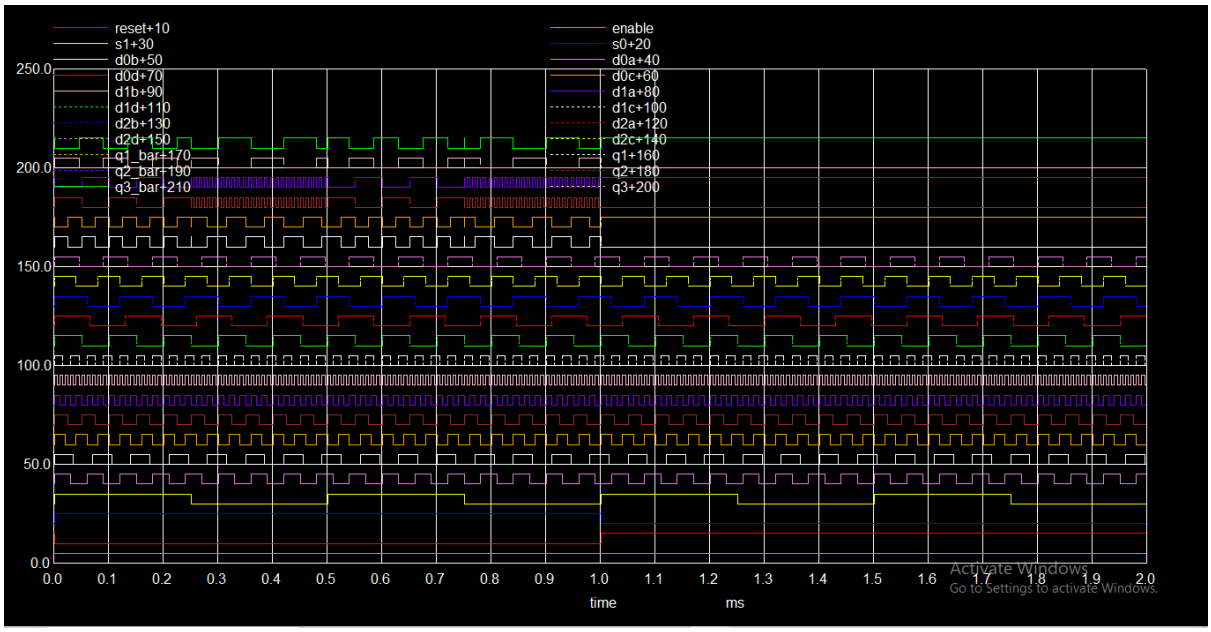

Figure 11.5: Output Plot of MC10E156

Chapter 12

MC10E155

12.1 General Description

The MC10E155 is a high-speed 6-bit 2:1 multiplexer latch designed using ECL technology. It selects one of two input data sources and stores the selected information in integrated latches. The device is optimized for high-speed digital applications requiring low propagation delays. Differential ECL architecture ensures reliable operation at high frequencies. It is commonly used in communication and data acquisition systems.

12.2 Key Features

- Six-bit wide multiplexer.
- Two-to-one data selection.
- Low propagation delay.
- Differential operation.
- High-speed performance.

12.3 Applications

- Data multiplexing systems.
- High-speed data acquisition.
- Telecommunications circuits.
- Digital switching networks.
- Signal routing applications.
- Test and measurement systems.

12.4 Subcircuit

The MC10E155 6-bit 2:1 multiplexer latch was implemented in eSim using high-speed logic elements. The design selects one of two data sources and stores the selected data.

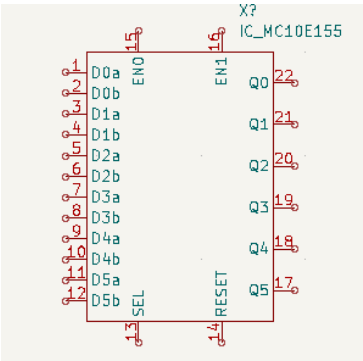

Figure 12.1: Subcircuit of MC10E155

12.5 Subcircuit Schematic Diagram

The schematic diagram illustrates the multiplexer network and latch stages used in the implementation. The structure follows the functional architecture of the device.

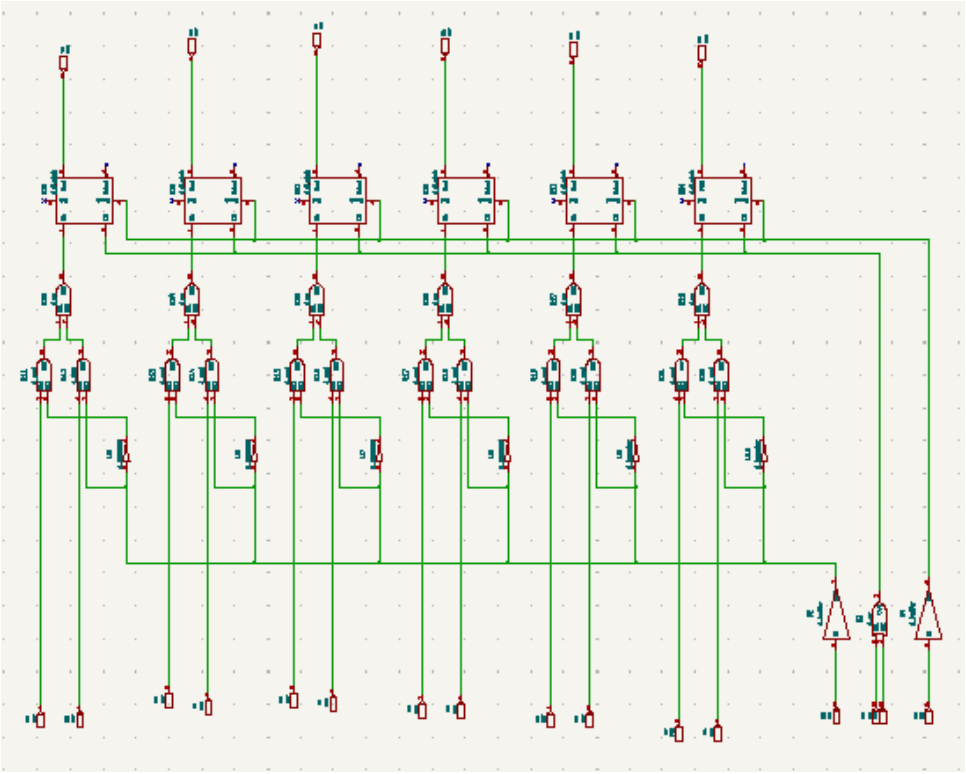

Figure 12.2: Subcircuit Schematic of MC10E155

12.6 Test Circuit

A test circuit was designed to validate multiplexing and latching operations. Different data patterns and control signals were applied.

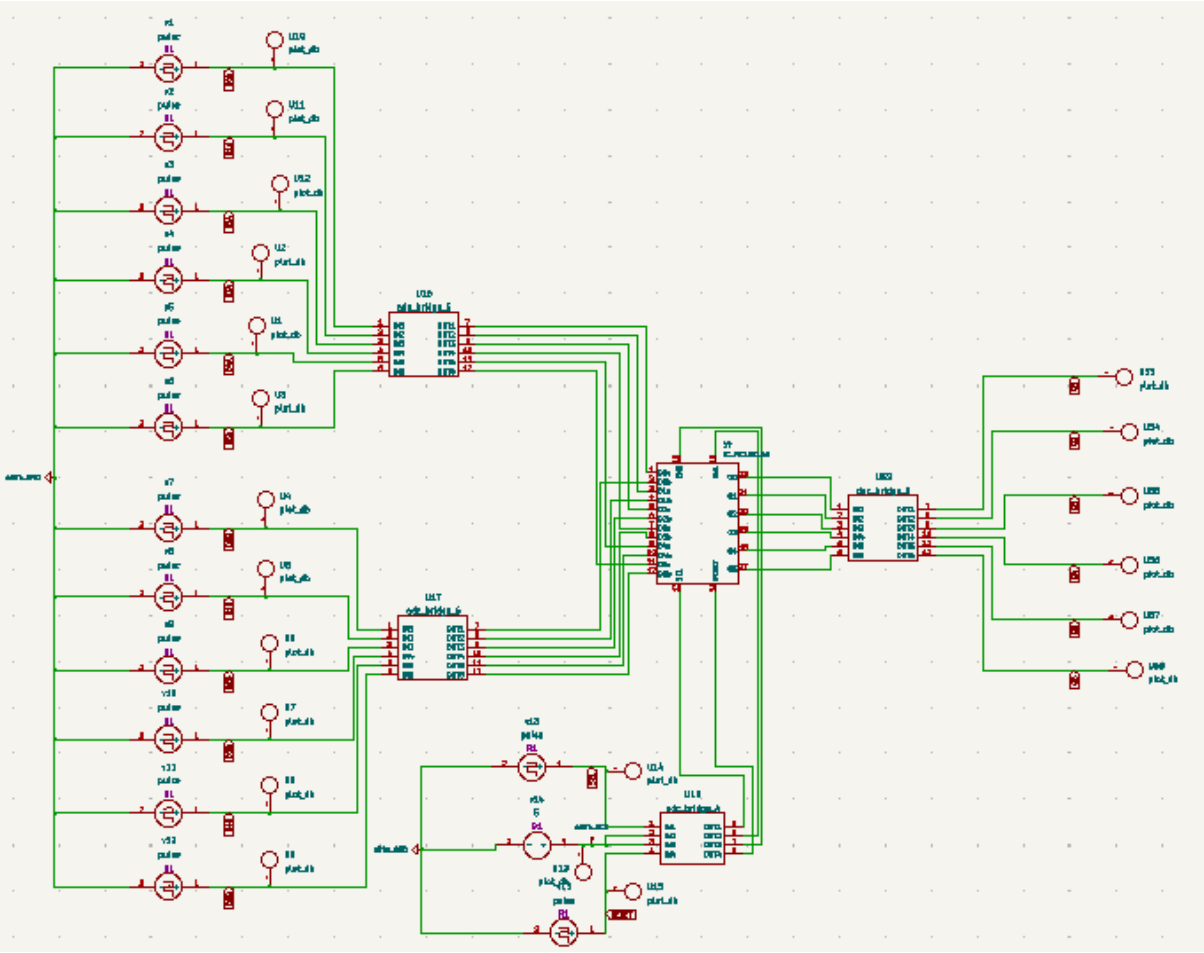

Figure 12.3: Test Circuit of MC10E155

12.7 Function Table

SEL	Data
H	a
L	b

Figure 12.4: Function Table of MC10E155

12.8 Output Plot

The output waveform demonstrates successful data selection and storage. The simulated results are consistent with datasheet specifications.

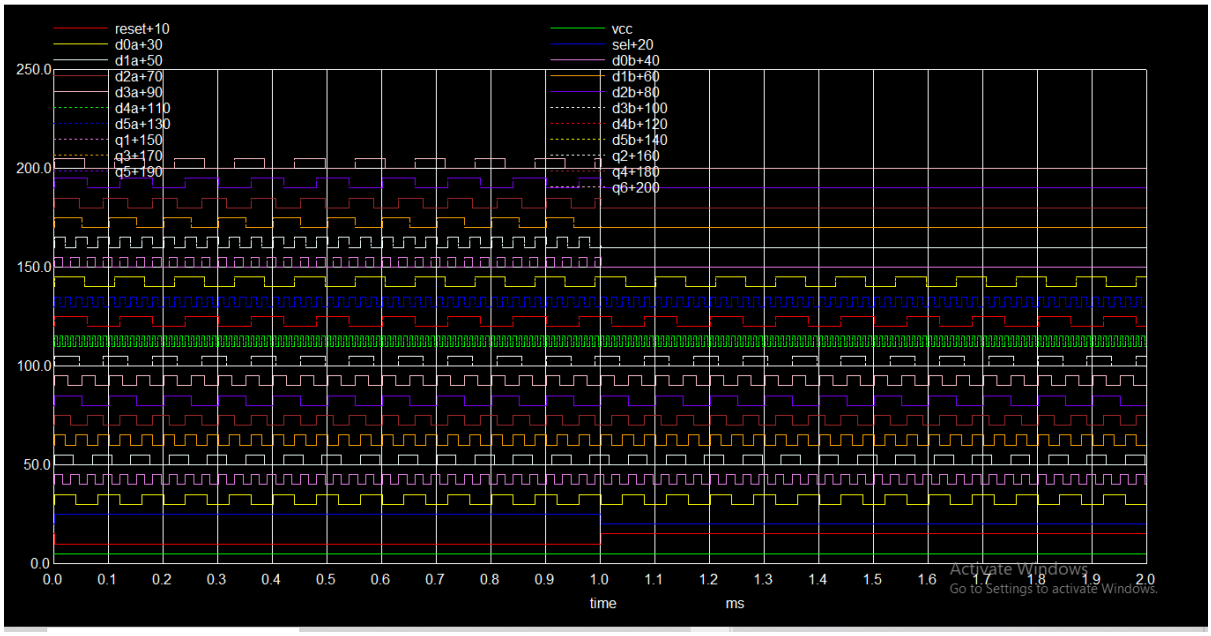

Figure 12.5: Output Plot of MC10E155

Chapter 13

CD74HC533

13.1 General Description

The CD74HC533 is an octal D-type transparent latch featuring 3-state inverting outputs. The device stores eight bits of data while the latch enable signal is active and holds the data when disabled. Its tristate outputs allow direct connection to shared buses without contention. High-speed CMOS technology provides low power consumption and reliable operation. The IC is suitable for data storage and bus interfacing applications.

13.2 Key Features

- Eight transparent D-type latches.
- Inverting output configuration.
- 3-state output capability.
- Low power consumption.
- Bus interface support.

13.3 Applications

- Data storage registers.
- Bus-oriented systems.
- Memory interfacing circuits.
- Embedded controllers.
- Digital communication systems.
- Data buffering applications.

13.4 Subcircuit

The CD74HC533 octal transparent latch was implemented as an eSim subcircuit with inverting tristate outputs. The design provides eight data storage channels.

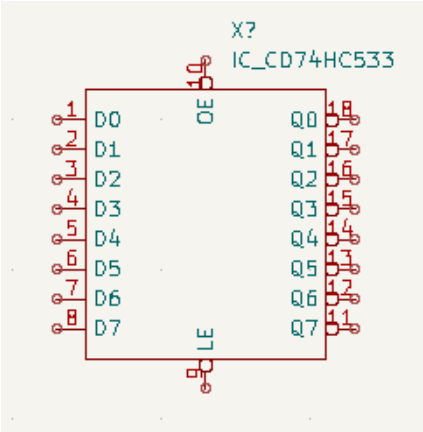

Figure 13.1: Subcircuit of CD74HC533

13.5 Subcircuit Schematic Diagram

The schematic diagram shows the transparent latch structure along with the tristate output control circuitry. The implementation accurately reflects the device operation.

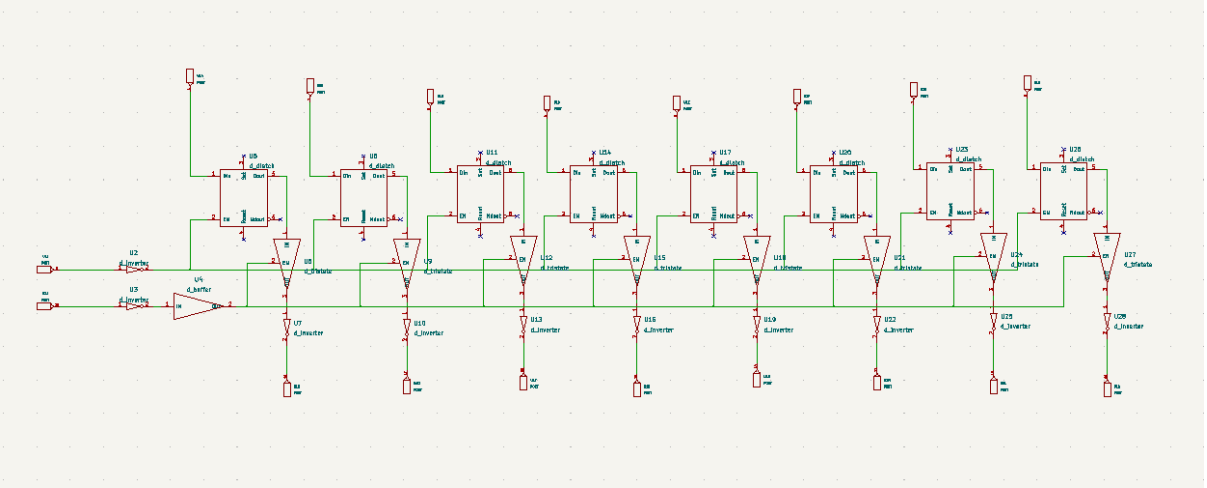

Figure 13.2: Subcircuit Schematic of CD74HC533

13.6 Test Circuit

A test circuit was developed to verify latch enable and output-enable functions. Various input combinations were applied during simulation.

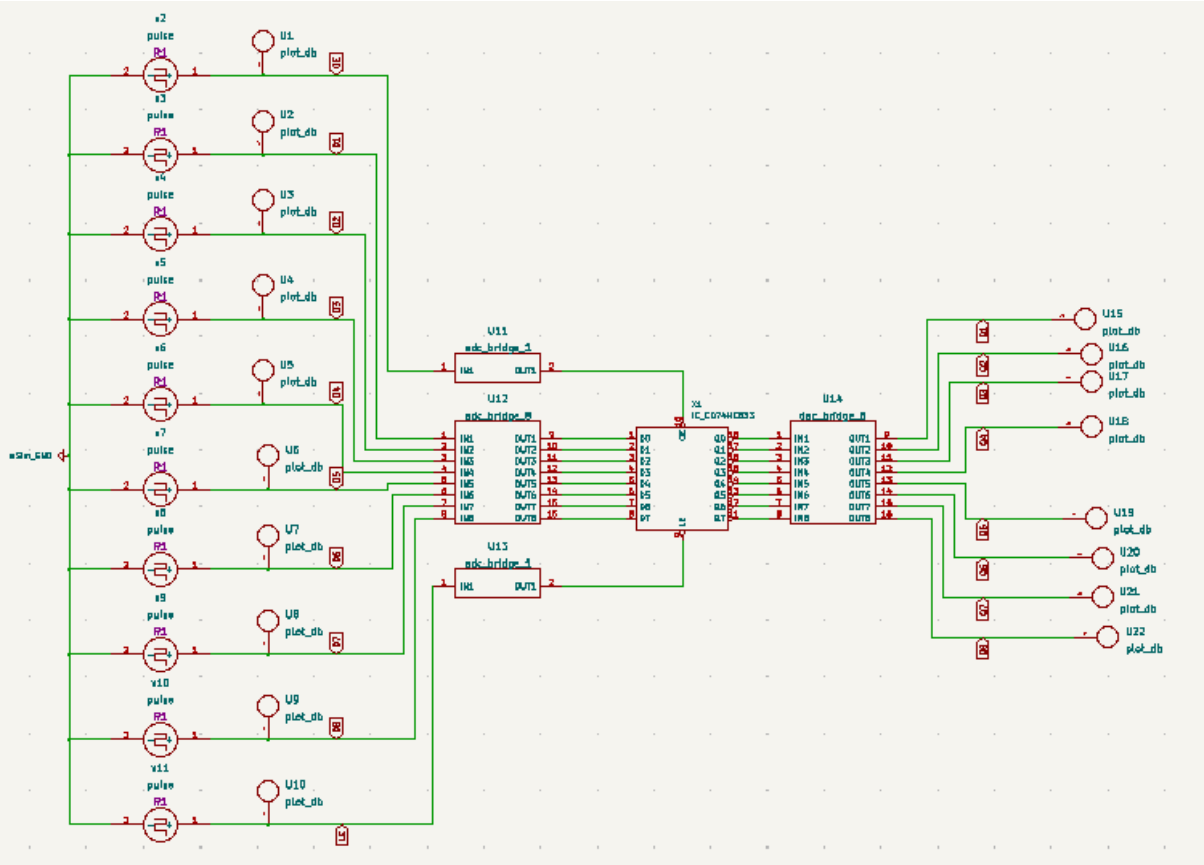

Figure 13.3: Test Circuit of CD74HC533

13.7 Function Table

$\overline{\text{OUTPUT ENABLE}}$	$\overline{\text{LATCH ENABLE}}$	DATA	Q OUTPUT
L	H	H	L
L	H	L	H
L	L	l	H
L	L	h	L
H	X	X	Z

Figure 13.4: Function Table of CD74HC533

13.8 Output Plot

The output waveform confirms proper latching, inversion, and tristate output behavior. The simulation results validate the functionality of the implemented subcircuit.

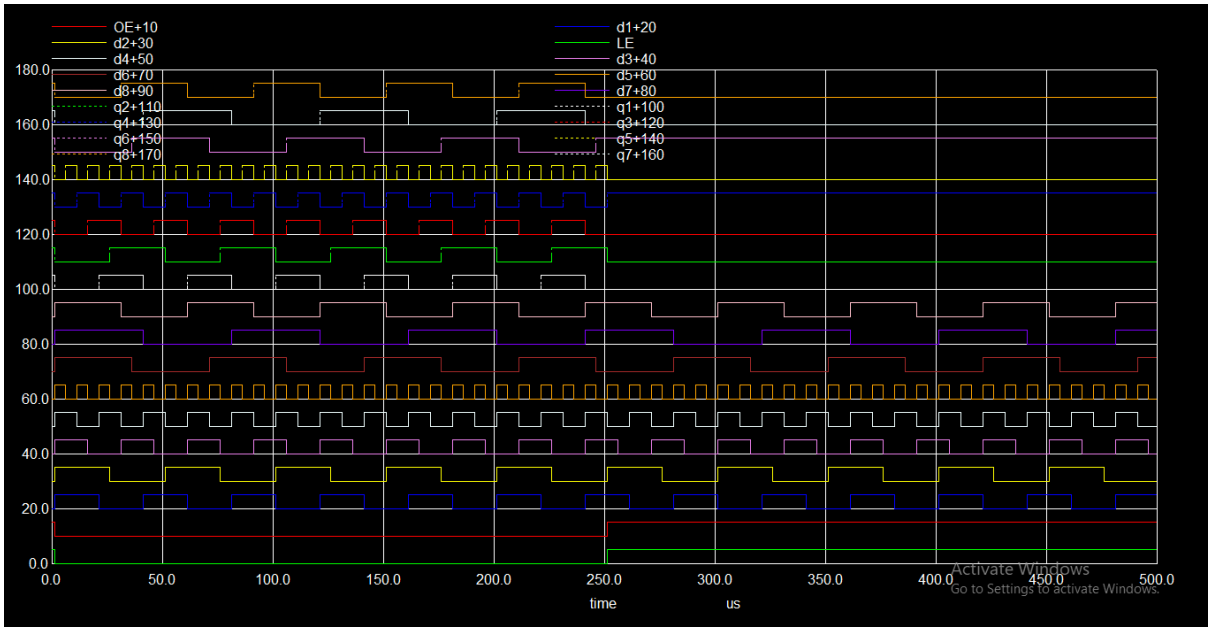

Figure 13.5: Output Plot of CD74HC533

Chapter 14

Conclusion and Future Scope

The project successfully achieved its objective of developing and validating a set of digital integrated circuits using the eSim platform. Each IC was designed as a subcircuit based on its respective datasheet and thoroughly tested using suitable simulation test circuits to verify its functionality. The contributions include various combinational and sequential logic devices such as delay elements, logic gates, buffers, multiplexers, latches, flip-flops, and counters.

These IC models serve as important building blocks for digital system design and simulation. Their inclusion in the eSim library enhances the availability of reusable digital components for students, educators, and researchers working with open-source EDA tools. The successful implementation and verification of these devices demonstrate the capability of eSim in supporting complex digital circuit development.

This work contributes to the continuous expansion of the eSim component library and promotes the adoption of open-source simulation tools in engineering education. Future efforts can focus on developing additional high-speed logic families, programmable logic devices, memory circuits, and mixed-signal ICs to further strengthen the eSim ecosystem and support more advanced circuit design applications.

Chapter 15

Circuits Contribution

This chapter lists all the Integrated Circuits (ICs) contributed during the internship. Each IC has been carefully modeled, verified, and tested in eSim. The contributions cover a wide range of digital logic functions including delay elements, logic gates, buffers, multiplexers, latches, flip-flops, and counters.

15.1 SANTHOSH C – List of ICs

1. 74LS31 – Hex Delay Element
2. NA53 – 5-Input NAND Gate
3. OR73 – 7-Input OR Gate Featuring 3x Drive Strength
4. GD74HCT58 – Dual AND-OR Gates
5. DM8098 – Tristate Hex Inverting Buffer
6. CD74AC174 – Hex D-Type Flip-Flop
7. M74HC4024 – 7-Bit Asynchronous Binary Counter
8. MC10E156 – 3-Bit 4:1 Multiplexer Latch
9. MC10E155 – 6-Bit 2:1 Multiplexer Latch
10. CD74HC533 – Octal D-Type Transparent Latch with 3-State Inverting Outputs

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[7] ON Semiconductor, "MC10E156 3-Bit 4:1 Multiplexer Latch Datasheet," [Online]. Available: `https://www.onsemi.com`.

[8] ON Semiconductor, "MC10E155 6-Bit 2:1 Multiplexer Latch Datasheet," [Online]. Available: `https://www.onsemi.com`.

[9] Texas Instruments, "CD74HC533 Octal Transparent Latch Datasheet," [Online]. Available: `https://www.ti.com`.

[10] NA53 Logic Gate Datasheet used during IC implementation.

[11] OR73 Logic Gate Datasheet used during IC implementation.

[12] GD74HCT58 Dual AND-OR Gate Datasheet used during IC implementation.