eSim Semester Long Internship Autumn 2025

On

Adding ICs as Subcircuits in eSim Library

Submitted by

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Acknowledgment

I express my sincere gratitude to Prof. Prabhu Ramachandran for providing me with the opportunity to be part of the FOSSEE internship program and for his continued efforts in promoting open-source engineering tool development. His leadership and vision have been instrumental in fostering meaningful student participation in the open-source ecosystem.

I also acknowledge Prof. Kannan M. Moudgalya for his foundational role in establishing and strengthening the FOSSEE initiative. His contributions to open-source education and the development of the FOSSEE fellowship framework have been pivotal in creating the academic and organisational platform through which this internship was undertaken.

My sincere appreciation extends to my mentor, Sumanto Kar, for his continual support, technical guidance, and encouragement throughout the duration of this project. His insights and feedback played a key role in refining ideas, overcoming challenges, and ensuring timely completion of the tasks assigned to me.

I would also like to thank my internal mentors, Mr. Varad Patil and Ms. Shanthi Priya K for their valuable guidance, coordination, and technical inputs during the internship. Their mentorship contributed significantly to the clarity, progress, and successful execution of the work.

This internship has been an enriching learning experience, allowing me to work closely with open-source EDA tools, develop IC subcircuits in eSim, and gain exposure to real-world circuit modeling and simulation workflows. The knowledge acquired during this period will undoubtedly support my future academic and professional pursuits.

I would also like to thank the entire FOSSEE team for their coordination, assistance, and timely interactions at various stages of this work. Their collective efforts ensured smooth workflow, resource accessibility, and effective project execution.

Contents

Chapter 1

Introduction

1.1 FOSSEE

FOSSEE, which stands for Free/Libre and Open Source Software for Education, is an organization based at IIT Bombay [3]. It is a remarkable initiative aimed at promoting the use of open-source software in education and research. It was established with the mission to reduce dependency on proprietary software and to encourage the adoption of open-source alternatives. FOSSEE offers a wide range of tools and resources that cater to various academic and professional needs.

It provides comprehensive documentation, tutorials, workshops, and hands-on training sessions to empower students, educators, and professionals to leverage open-source software for their projects and coursework. The organization's commitment to fostering a collaborative and inclusive environment has significantly contributed to the democratization of technology and has opened up new avenues for innovation and learning.

1.2 eSim

eSim, created by the FOSSEE project at IIT Bombay [4], is a versatile open-source software tool for circuit design and simulation. It combines various open-source software packages into one cohesive platform, making it easier to design, simulate, and analyze electronic circuits. This tool is particularly useful for students, educators, and professionals who need an affordable and accessible alternative to proprietary software.

eSim offers features for schematic creation, circuit simulation, and PCB design, and includes an extensive library of components. The Subcircuit feature is a significant enhancement, enabling users to design complex circuits by integrating simpler subcircuits. Through eSim, FOSSEE promotes the use of open-source solutions in engineering education and professional fields, encouraging innovation and collaboration.

1.3 NgSpice

NgSpice is an open-source SPICE simulator for electric and electronic circuits. It can simulate various circuit elements, including JFETs, bipolar and MOS transistors, passive elements (R, L, C), diodes and other devices, all interconnected in a netlist.

Digital circuits are also simulated, ranging from single gates to complex circuits, including combinations of analog, digital, and mixed-signal circuits. NgSpice offers a wealth of device models for active, passive, analog, and digital elements. Users input their circuits as netlists, and the output is one or more graphs of currents, voltages, and other electrical quantities, or saved in a data file.

1.4 Makechip

Makechip is a platform that offers convenient and accessible tools for digital circuit design. It provides both browser-based and desktop-based environments for coding, compiling, simulating, and debugging Verilog designs. Makechip supports a combination of open-source and proprietary tools, ensuring a comprehensive range of capabilities.

Users can simulate Verilog/SystemVerilog/Transaction-Level Verilog code in Makechip. eSim is interfaced with Makechip using a Python-based application called Makechip-App, which launches the Makechip IDE. Makechip aims to make circuit design easy and enjoyable for users of all skill levels. The platform provides a userfriendly interface, intuitive workflows, and a range of helpful features that simplify the design process and enhance the overall user experience.

The main drawback of these open-source tools is that they are not comprehensive. While some are capable of PCB design (e.g., KiCad), others focus on simulations (e.g., gEDA). To the best of our knowledge, there is no open-source software that combines circuit design, simulation, and layout design in one platform. eSim addresses this gap by integrating all these capabilities.

Chapter 2

Features of eSim

The objective behind the development of eSim is to provide an open-source EDA solution for electronics and electrical engineers. The software is capable of performing schematic creation, PCB design, and circuit simulation (analog, digital, and mixedsignal). It also provides facilities to create new models and components. Thus, eSim offers the following features:

1. Schematic Creation: eSim provides an easy-to-use graphical interface for drawing circuit schematics, making it accessible for users of all levels. Users can drag and drop components from the library onto the schematic, simplifying the design process. Comprehensive editing tools allow for easy modification of schematics, including moving, rotating, and labeling components.

2. Circuit Simulation: eSim supports SPICE (Simulation Program with Integrated Circuit Emphasis), a standard for simulating analog and digital circuits. Users can perform various types of analysis such as transient, AC, and DC, providing insights into circuit behavior over time and frequency. An integrated waveform viewer helps visualize simulation results, aiding in the analysis and debugging of circuit designs.

3. PCB Design: The PCB layout editor allows users to place components and route traces with precision. eSim includes DRC (Design Rule Check) capabilities to ensure that the PCB design adheres to manufacturing constraints and electrical rules. Users can generate Gerber files, which are standard for PCB fabrication, directly from their designs.

4. Subcircuit Feature: This feature enables users to create complex circuits by integrating smaller, simpler subcircuits, promoting modular and hierarchical design approaches. Subcircuits can be reused in different projects, saving time and effort in redesigning common circuit elements.

5. Open Source Integration: eSim integrates several open-source tools like KiCad, NgSpice, and GHDL, providing a comprehensive suite for electronic design automation. Being open-source, eSim is free to use, making advanced circuit design tools accessible without the need for expensive licenses.

Chapter 3

Problem Statement

To design and develop various analog and digital integrated circuit models in the form of sub-circuits using device model files already present in the eSim library. These IC models should be useful for future circuit design purposes by developers and users once they are successfully integrated into the eSim sub-circuit library.

3.1 Approach

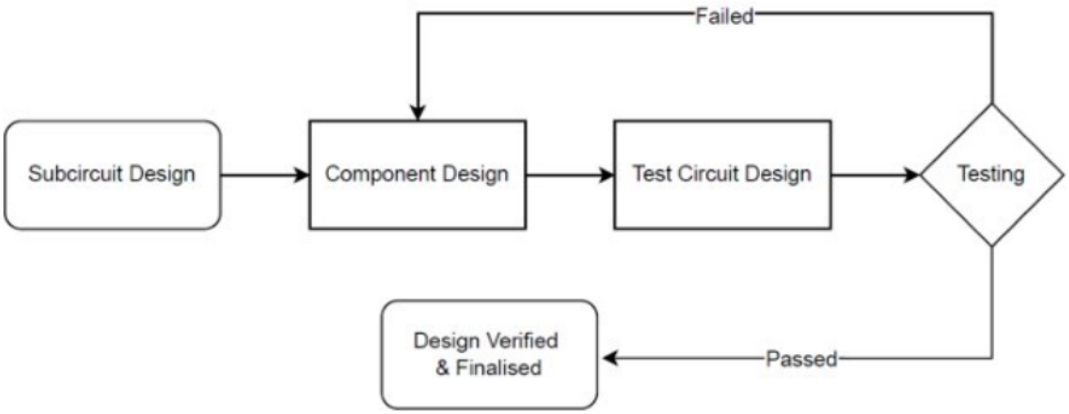

Figure 3.1: Flowchart of IC Design Approach Followed

Our approach to implementing the problem statement involved a systematic process, leveraging datasheets from leading Integrated Circuit (IC) manufacturers such as Texas Instruments, Analog Devices, and NXP Semiconductors. We focused on selecting ICs with diverse functionalities, including precision amplifiers, comparators, encoders, and audio amplifiers. The process is outlined in the following steps:

1. Analyzing Datasheets: The first step involved an in-depth review of datasheets for various analog and digital ICs. We aimed to identify circuits suitable for implementation in eSim that were not already present in the eSim library. This process included scrutinizing the detailed schematics of each IC, evaluating component values, and under-

standing truth tables. The goal was to select ICs that offered unique functionalities or enhancements not yet covered.

2. Subcircuit Creation: After selecting appropriate ICs, we proceeded to model these as sub-circuits within eSim. We utilized the model files available in the eSim device model library and ensured that our designs adhered strictly to the specifications outlined in the official datasheets. This phase also involved creating accurate symbol and pin diagrams for each IC, in accordance with the packaging and pin descriptions provided in the datasheets. This step was crucial for ensuring the fidelity of the subcircuit models.

3. Test Circuit Design: With the sub-circuits created, we then designed and built test circuits based on the datasheets. This step was essential for verifying the functionality of each sub-circuit. We developed a series of test cases and constructed corresponding test circuits to evaluate the performance and accuracy of the implemented IC models.

4. Schematic Testing: Following the construction of test circuits, we conducted simulations to analyze the outputs. This involved generating waveforms and plots to assess the behavior of the circuits. We employed KiCad for converting designs to NgSpice netlists and utilized eSim's simulation features to perform comprehensive testing.

If the simulated outputs deviated from expected results, it signaled potential errors in the schematic. In such instances, we revisited the design phase to identify and correct discrepancies. The iterative process of debugging and re-testing continued until the test cases produced satisfactory results. Once the IC models met the desired performance criteria, they were deemed successful, marking the completion of the design process.

Chapter 4

74ALS640

4.1 General Description

The 74ALS640 is an octal bus transceiver with inverting 3-state outputs from the ALS (Advanced Low-Power Schottky) logic family [5]. It enables bidirectional data transfer between two 8-bit buses using DIR (direction control) and OE (output enable) signals. Built using ALS technology, it provides high-speed operation, low power consumption, and TTL-compatible inputs and outputs.

4.2 Key Features

- 8-bit bidirectional bus transceiver for data transfer between two buses
- Inverting outputs, meaning transmitted data appears as logical complement.
- 3-state output control for bus isolation using Output Enable (OE).
- Direction control (DIR) enables selectable A→B or B→A data flow.
- ALS technology provides high-speed operation with low power consumption.

4.3 Applications

- Microprocessor bus interfacing for bidirectional data transfer.
- Memory system interfacing between CPU and memory buses.
- Digital communication systems for controlled data transmission.
- Bus isolation and buffering to prevent signal loading and contention.

4.4 Subcircuit

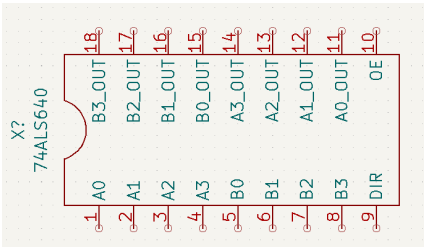

Figure 4.1: Subcircuit of 74ALS640

4.5 Subcircuit Schematic Diagram

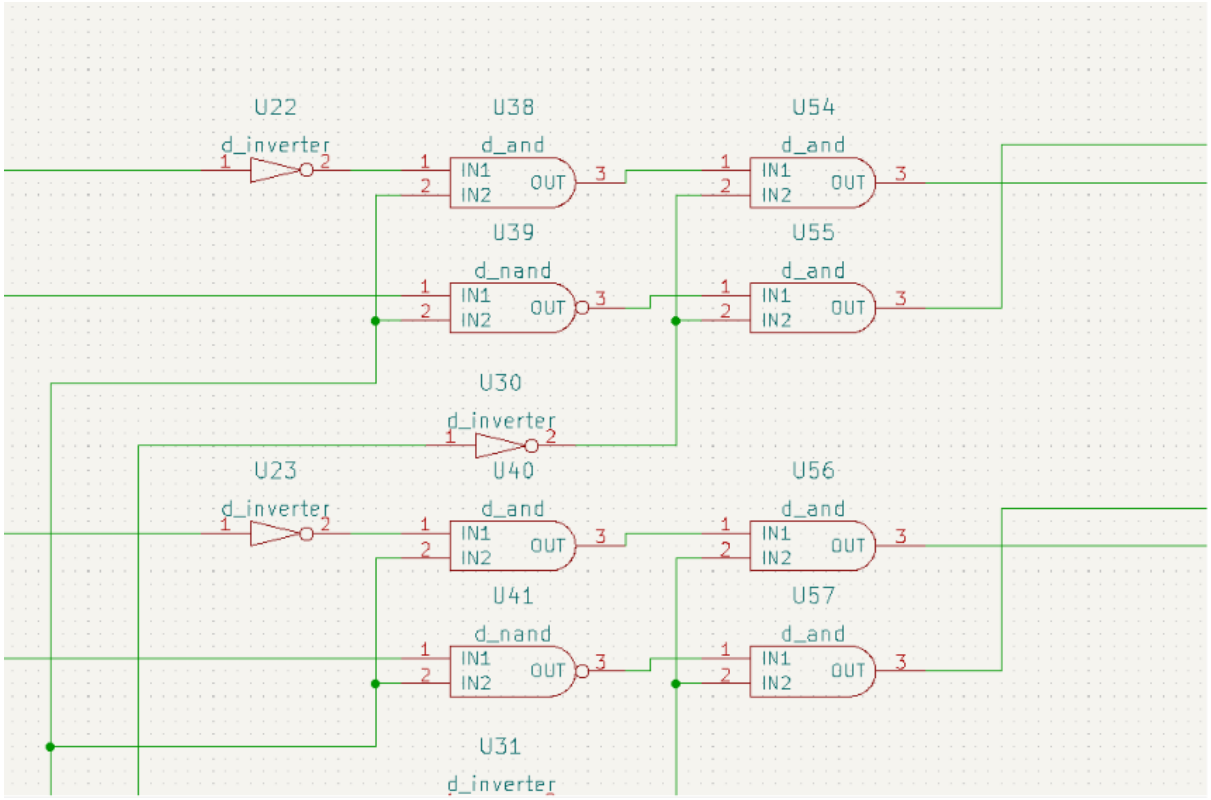

Figure 4.2: Subcircuit Schematic of the (Part of ic) 74ALS640

4.6 Test Circuit

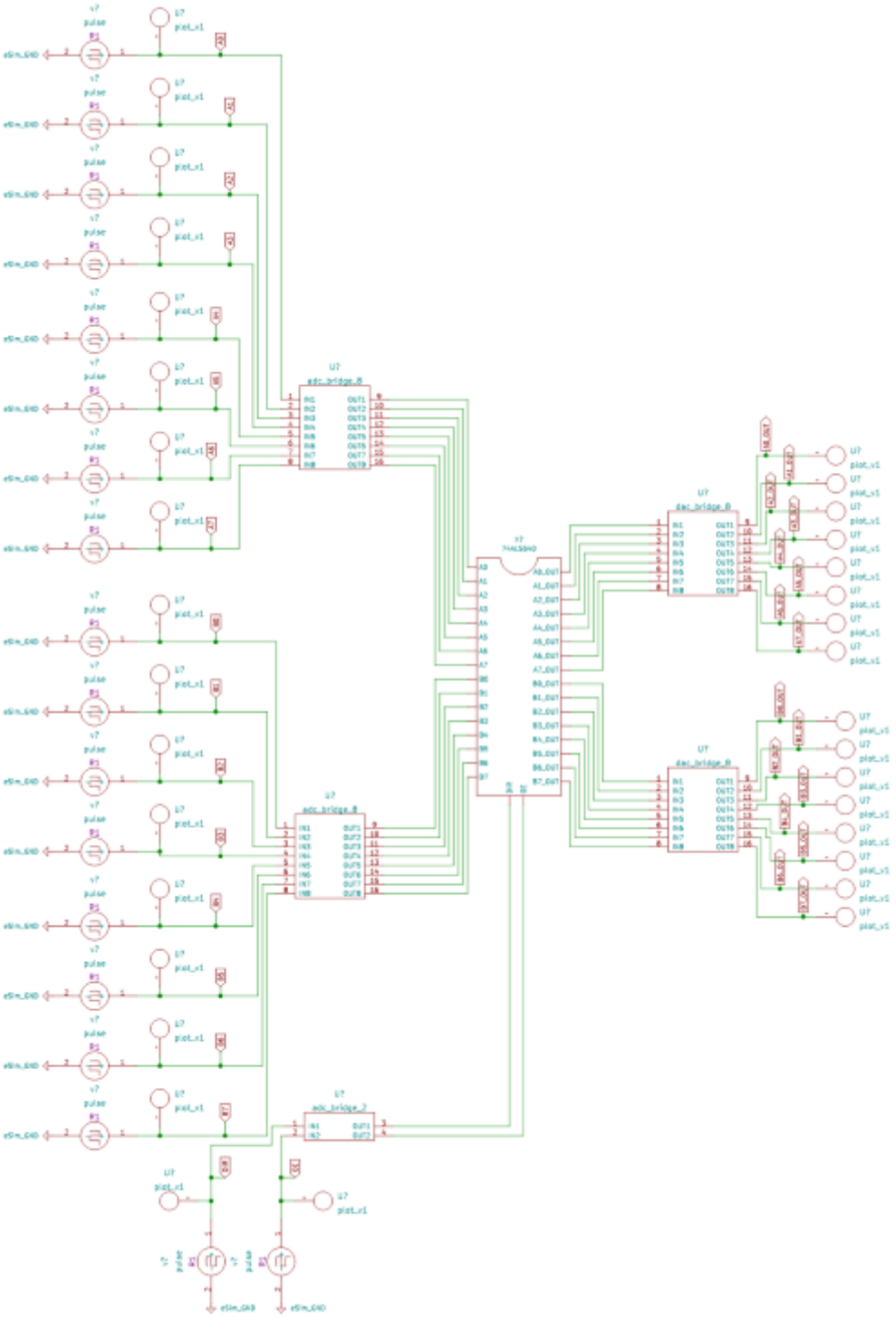

Figure 4.3: Test Circuit of the 74ALS640

4.7 Function Table

OE	DIR	Function	Expected Real IC Output	eSim Output Used
0	0	A → B	B = NOT(A)	B = NOT(A)
0	1	B → A	A = NOT(B)	A = NOT(B)
1	X	Disabled	Z (High Impedance)	0 (used instead of Z)

Figure 4.4: Function Table of the 74ALS640

4.8 Output Plot

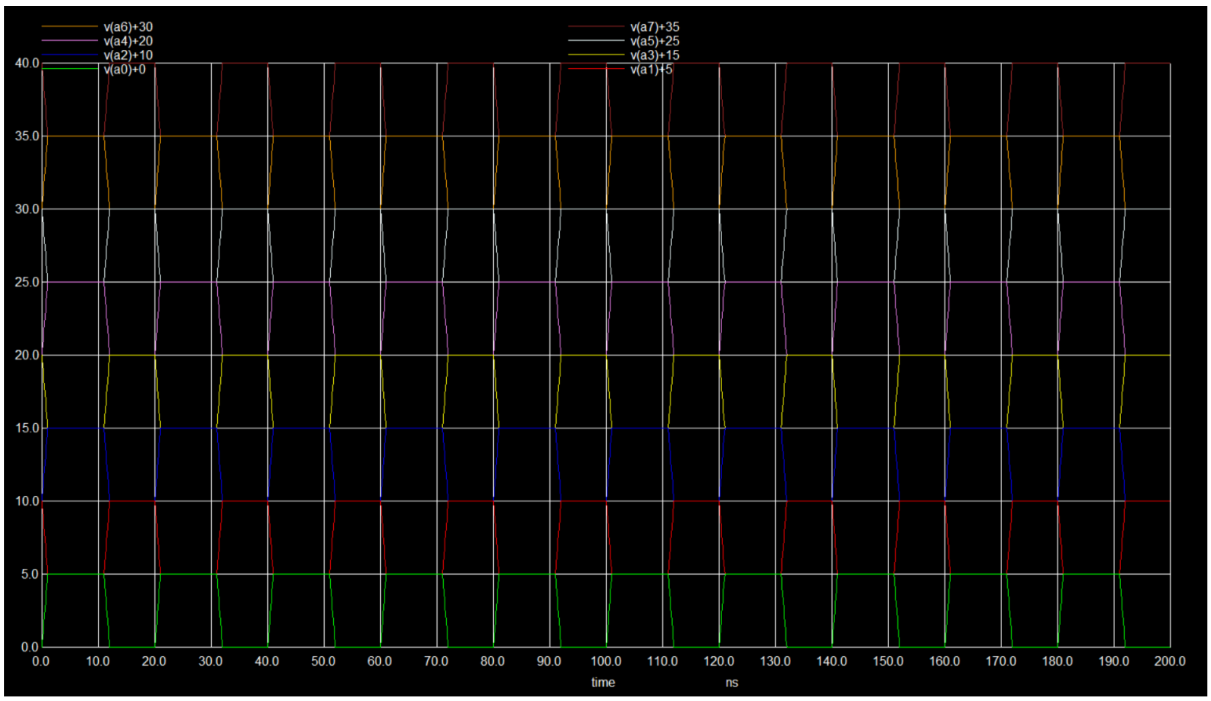

Figure 4.5: Control signals of the 74ALS640

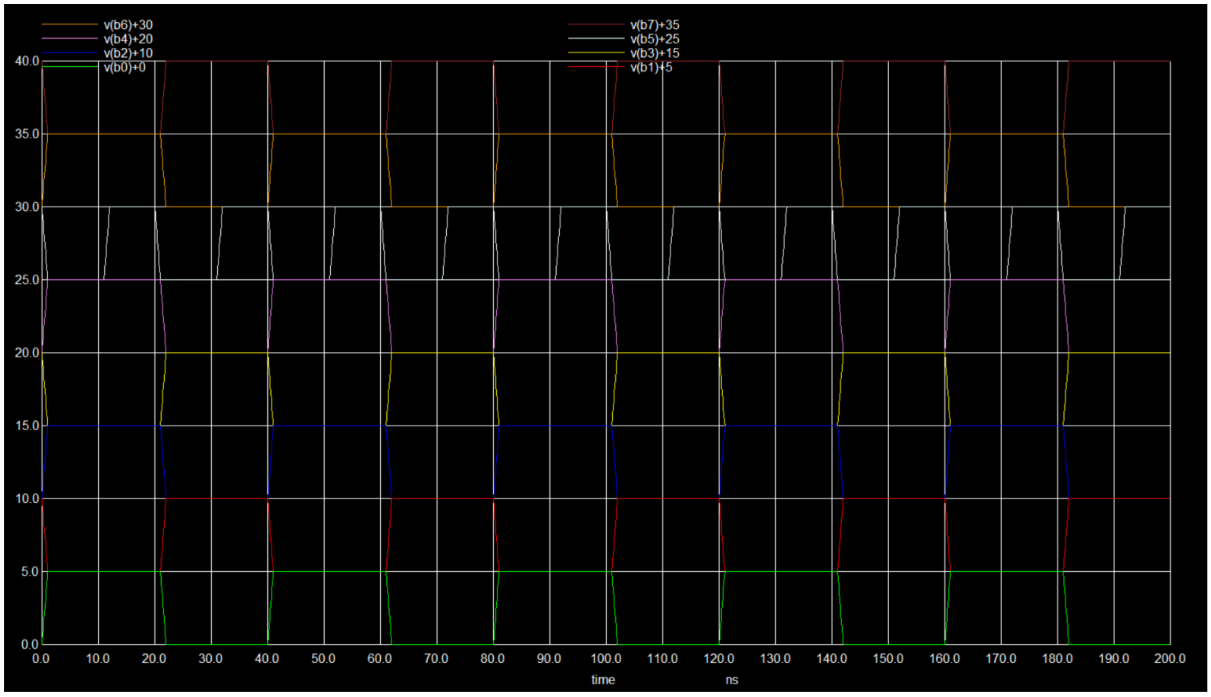

Figure 4.6: A inputs of the 74ALS640

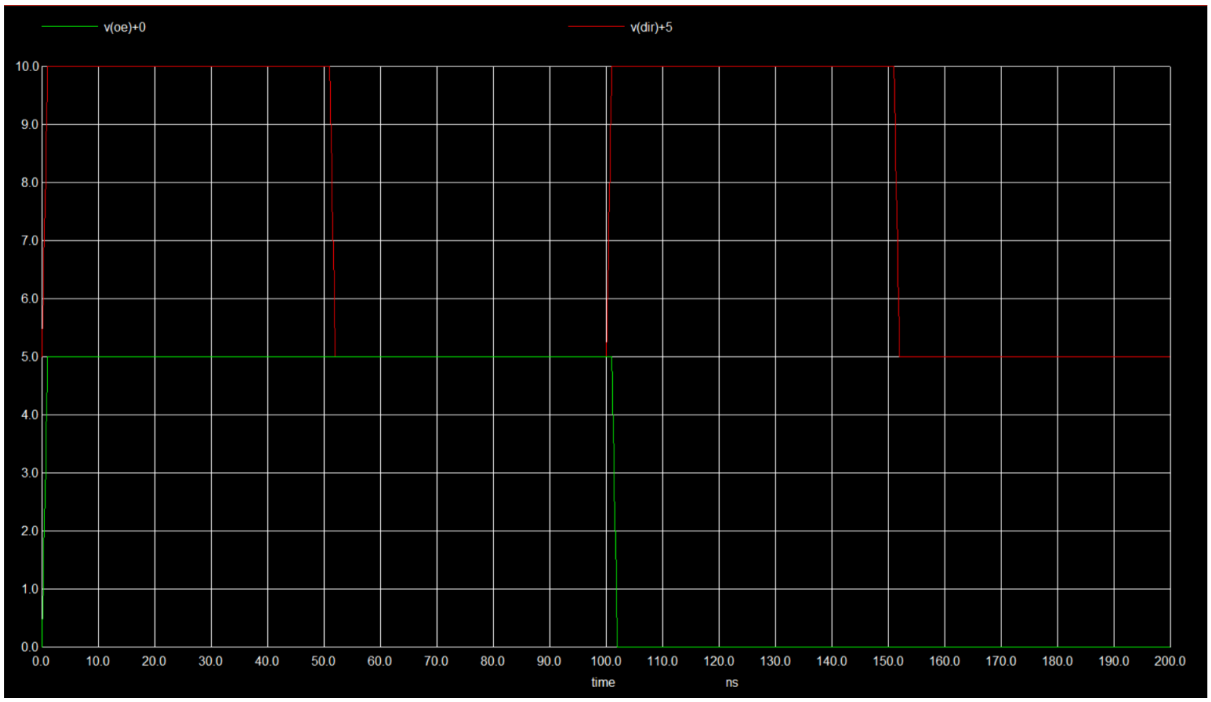

Figure 4.7: B inputs of the 74ALS640

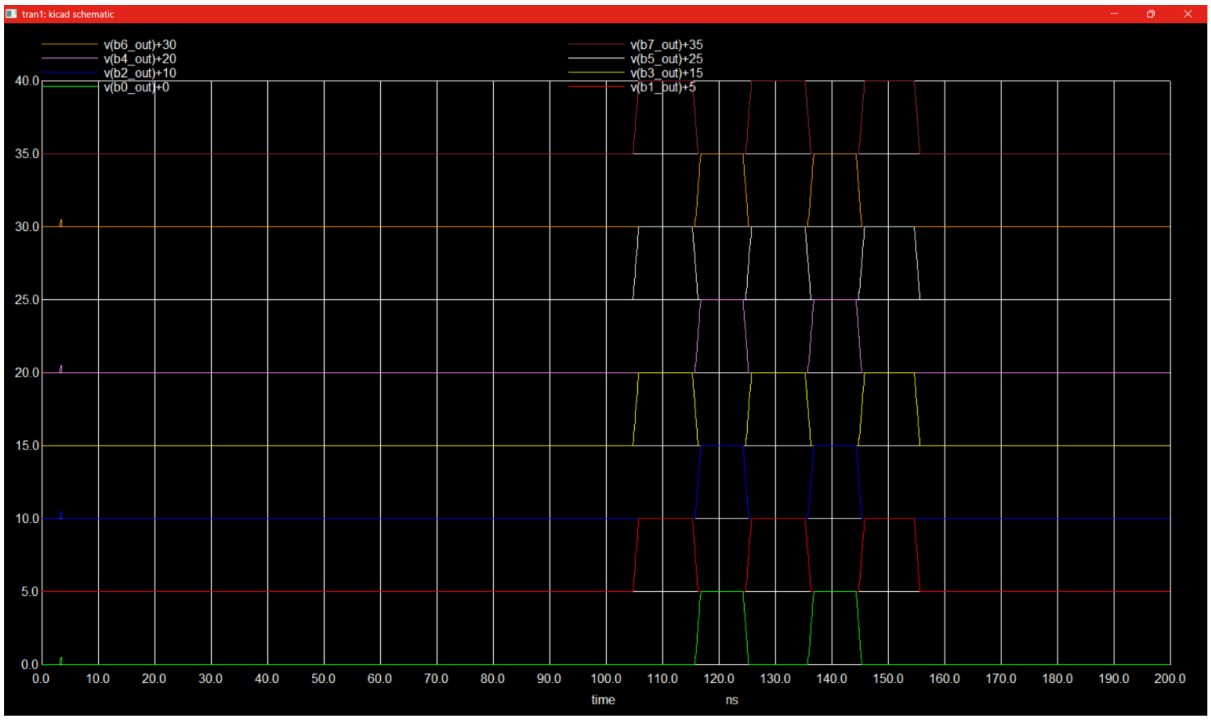

Figure 4.8: A outputs of the 74ALS640

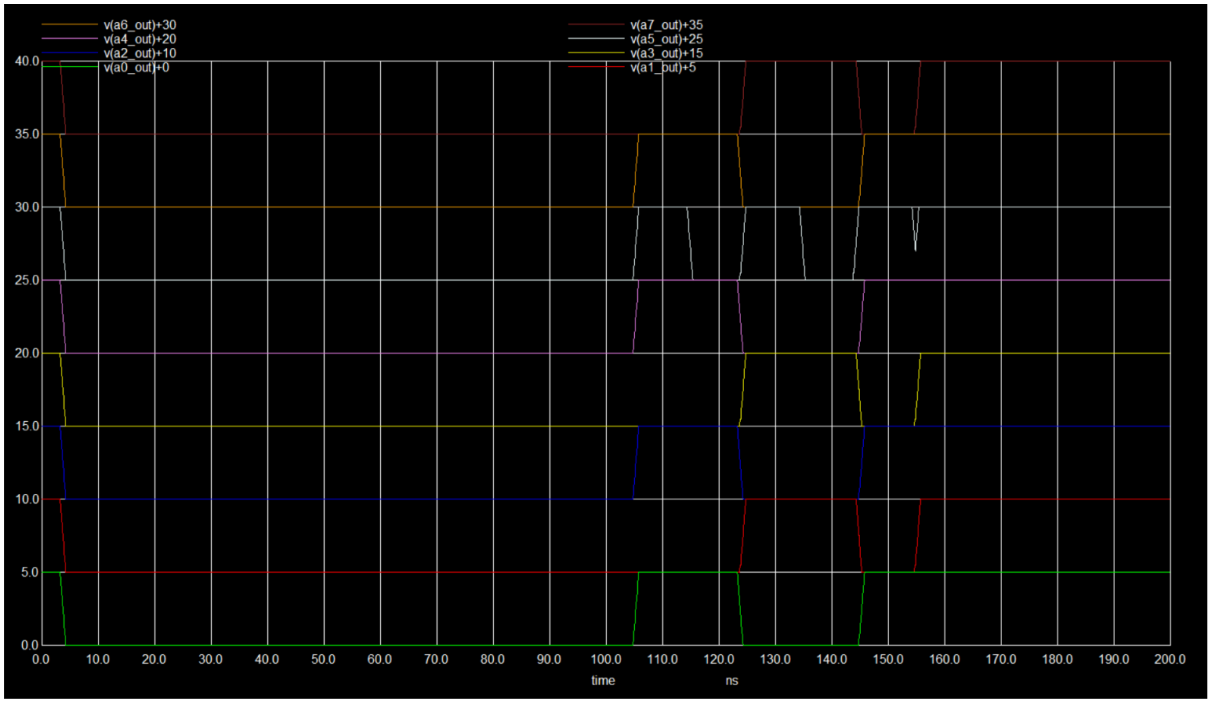

Figure 4.9: B outputs of the 74ALS640

Chapter 5

SN74S274

5.1 General Description

The SN74S274 is a 4×4 two's complement binary multiplier from the Schottky TTL (S) logic family [5]. It performs multiplication of two 4-bit signed binary inputs represented in two's complement form and produces an 8-bit signed output. Designed using high-speed Schottky technology, it provides fast arithmetic computation, reliable digital multiplication, and TTL-compatible inputs and outputs.

5.2 Key Features

- Performs signed multiplication of two 4-bit two's complement binary numbers.
- Produces an 8-bit signed output in two's complement format.
- Supports high-speed arithmetic computation using Schottky TTL technology.
- TTL-compatible inputs and outputs for easy digital system integration.
- Compact hardware implementation for real-time signed multiplication applications.

5.3 Applications

- Arithmetic Logic Units (ALUs) in processors and microcontrollers.
- Digital Signal Processing (DSP) systems for signed arithmetic operations.
- Embedded systems requiring fast hardware multiplication.
- Digital control and computation circuits in VLSI systems.

5.4 Subcircuit

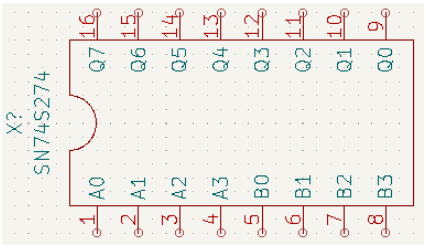

Figure 5.1: Subcircuit of SN74S274

5.5 Subcircuit Schematic Diagram

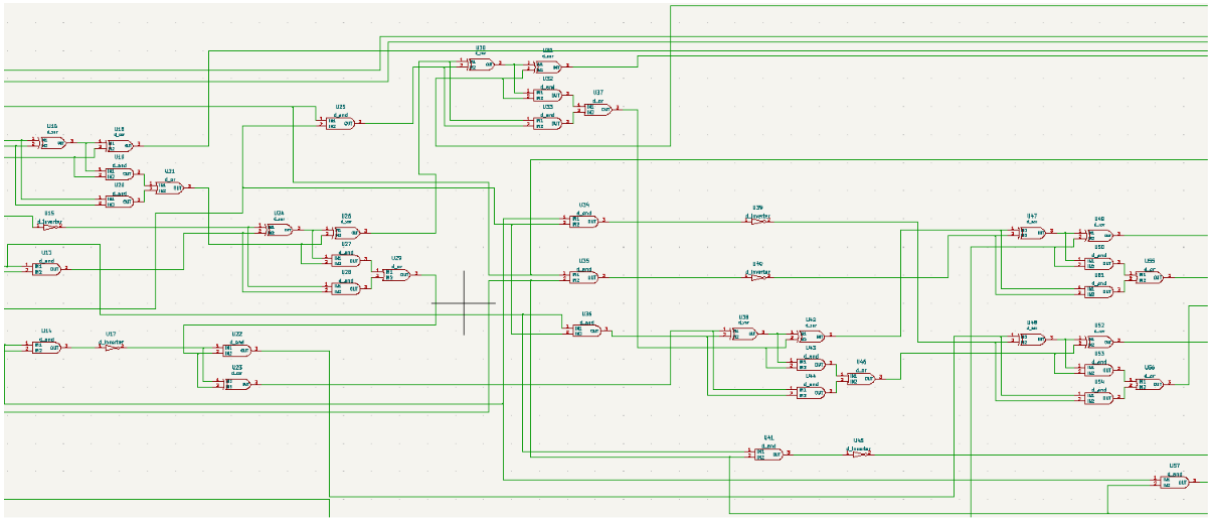

Figure 5.2: Subcircuit Schematic of the (Part of ic) SN74S274

5.6 Test Circuit

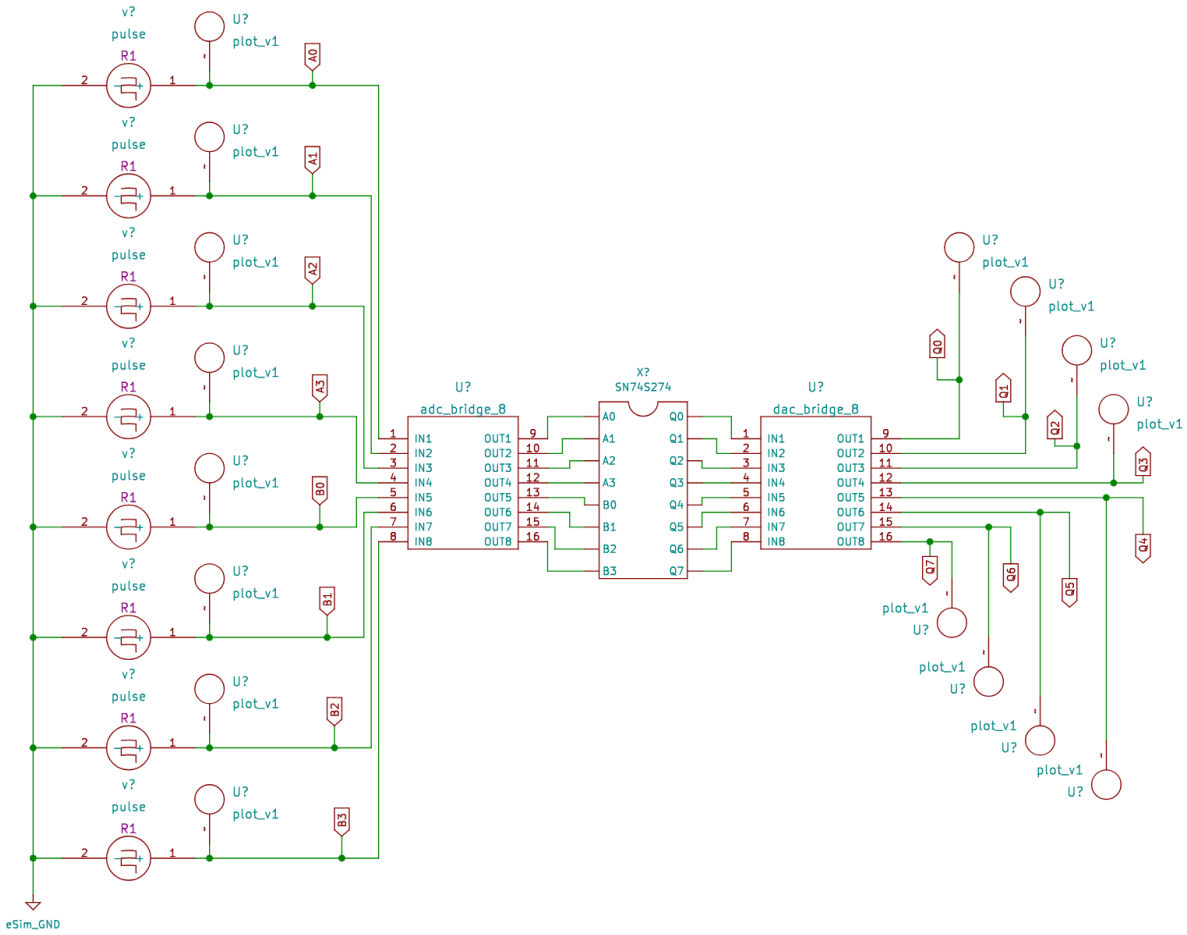

Figure 5.3: Test Circuit of the SN74S274

5.7 Function Table

A3	A2	A1	A0	B3	B2	B1	B0	P7	P6	P5	P4	P3	P2	P1	P0	Verification
0	0	1	1	0	1	0	1	0	0	0	0	1	1	1	1	3 × 5 = 15

Figure 5.4: Function Table of the SN74S274 One Test Case

5.8 Function Table

A3	A2	A1	A0	B3	B2	B1	B0	P7	P6	P5	P4	P3	P2	P1	P0	Verification
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 × 0 = 0
0	0	0	1	0	0	0	1	0	0	0	0	0	0	0	1	1 × 1 = 1
0	0	1	0	0	0	1	1	0	0	0	0	0	1	1	0	2 × 3 = 6
0	1	0	0	0	1	0	1	0	0	0	1	0	1	0	0	4 × 5 = 20
0	1	1	1	0	0	1	1	0	0	0	1	0	1	0	1	7 × 3 = 21
1	0	0	0	1	0	0	0	0	1	0	0	0	0	0	0	8 × 8 = 64
1	0	1	0	1	1	0	0	0	1	1	1	1	0	0	0	10 × 12 = 120
1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	1	15 × 15 = 225

Figure 5.5: Function Table of the SN74S274 for All Test case

5.9 Output Plot

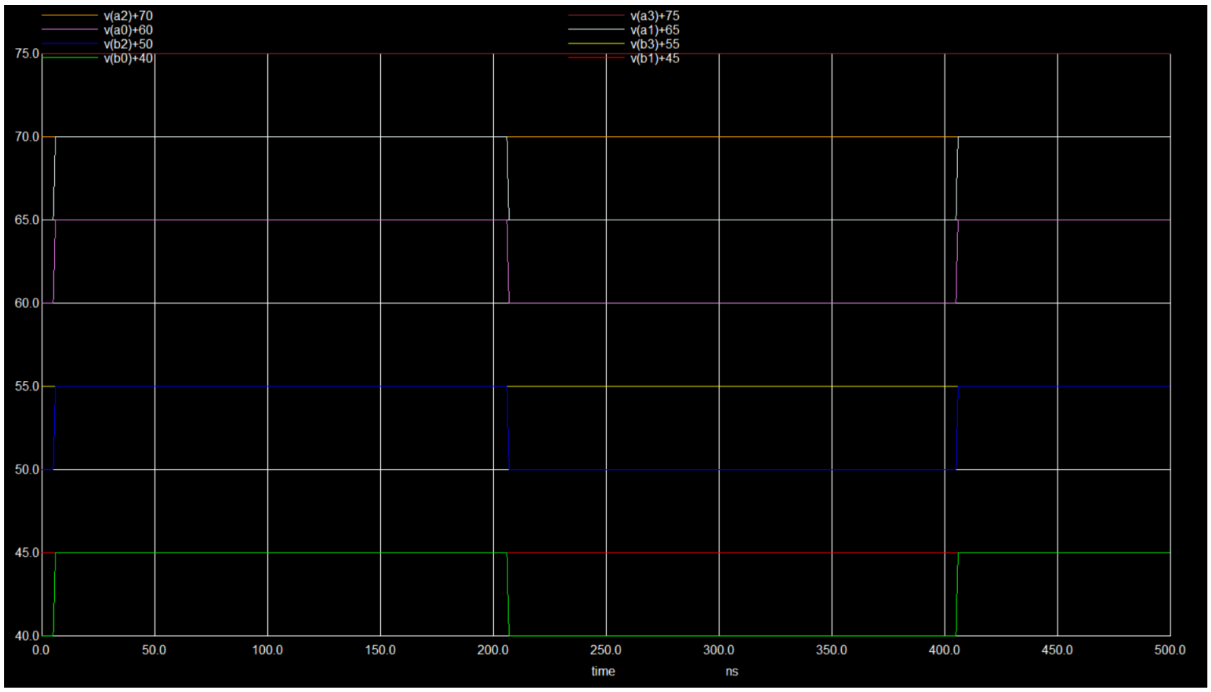

Figure 5.6: Input signals of the SN74S274 for one test case

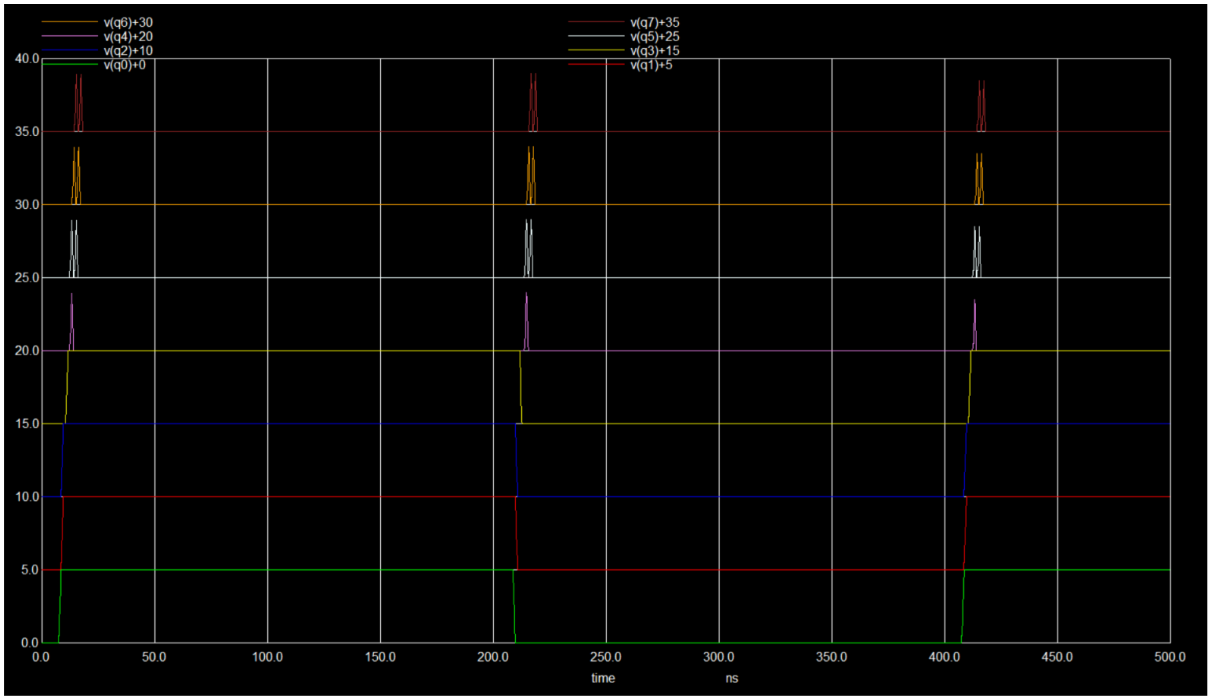

Figure 5.7: Output signals of the SN74S274 for one test case

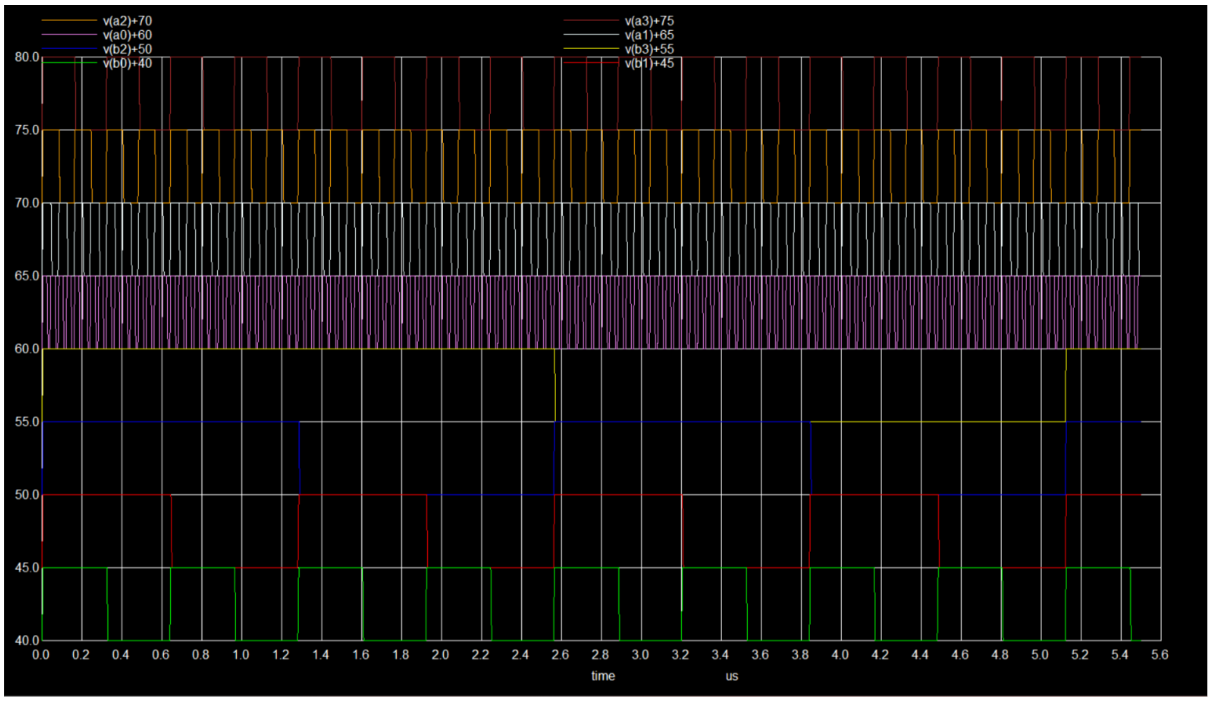

Figure 5.8: Input Signals of the SN74S274 for all test case

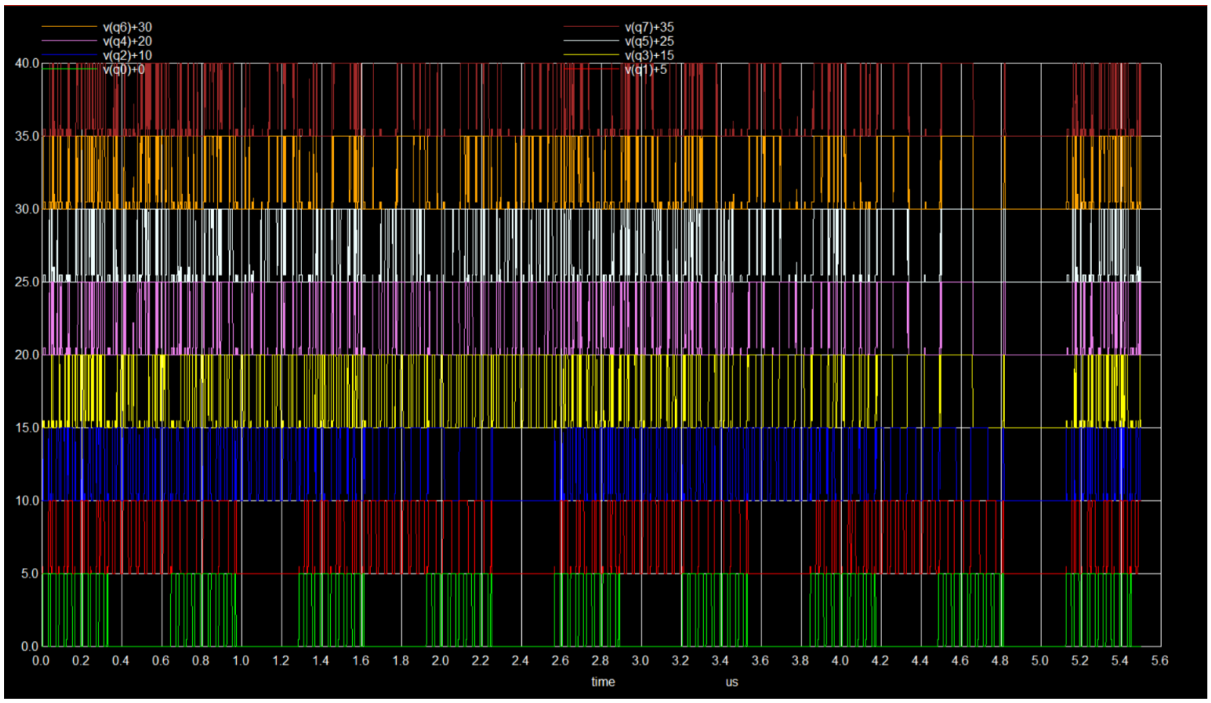

Figure 5.9: Output Signals of the SN74S274 for all test case

Chapter 6

TIBPAL20L8

6.1 General Description

The TIBPAL20L8 is a programmable array logic (PAL) device from the Texas Instruments Bipolar Programmable Logic family [5]. It features 20 input pins and 8 programmable outputs, enabling implementation of custom combinational and sequential digital logic functions. Built using high-speed bipolar technology, it provides fast logic operation, programmable AND-OR architecture, and TTL-compatible inputs and outputs, making it suitable for glue logic, address decoding, state machines, and custom digital control applications.

6.2 Key Features

- Provides 20 programmable input lines for implementing custom digital logic functions.
- Includes 8 programmable outputs configurable for combinational or registered logic operations.
- Uses programmable AND-OR logic architecture for flexible logic design implementation.
- Built with high-speed bipolar technology for fast propagation delay and reliable performance.
- Features TTL-compatible inputs and outputs for seamless integration in digital systems.

6.3 Applications

- Glue logic implementation in microprocessor and embedded systems.

- Address decoding and memory interfacing circuits.
- Finite State Machine (FSM) and digital control circuit design.
- Custom combinational and sequential logic replacement for SSI/MSI devices.

6.4 Subcircuit

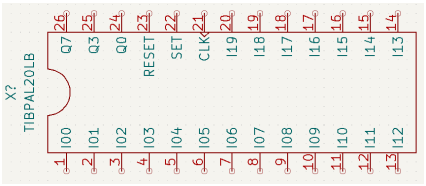

Figure 6.1: Subcircuit of TIBPAL20L8

6.5 Subcircuit Schematic Diagram

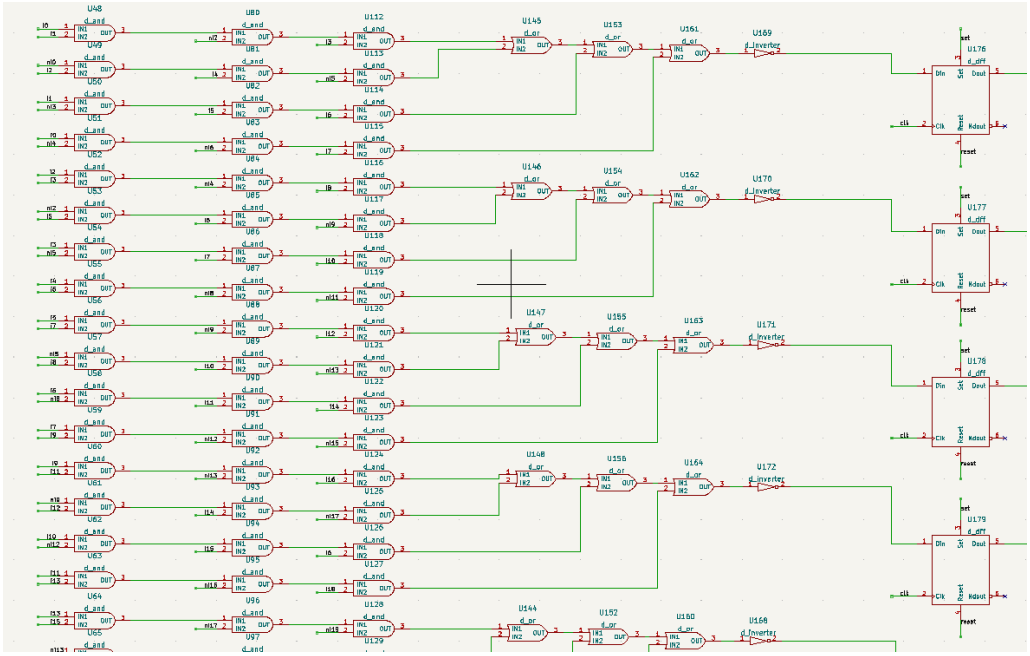

Figure 6.2: Subcircuit Schematic of the (Part of ic) TIBPAL20L8

6.6 Test Circuit

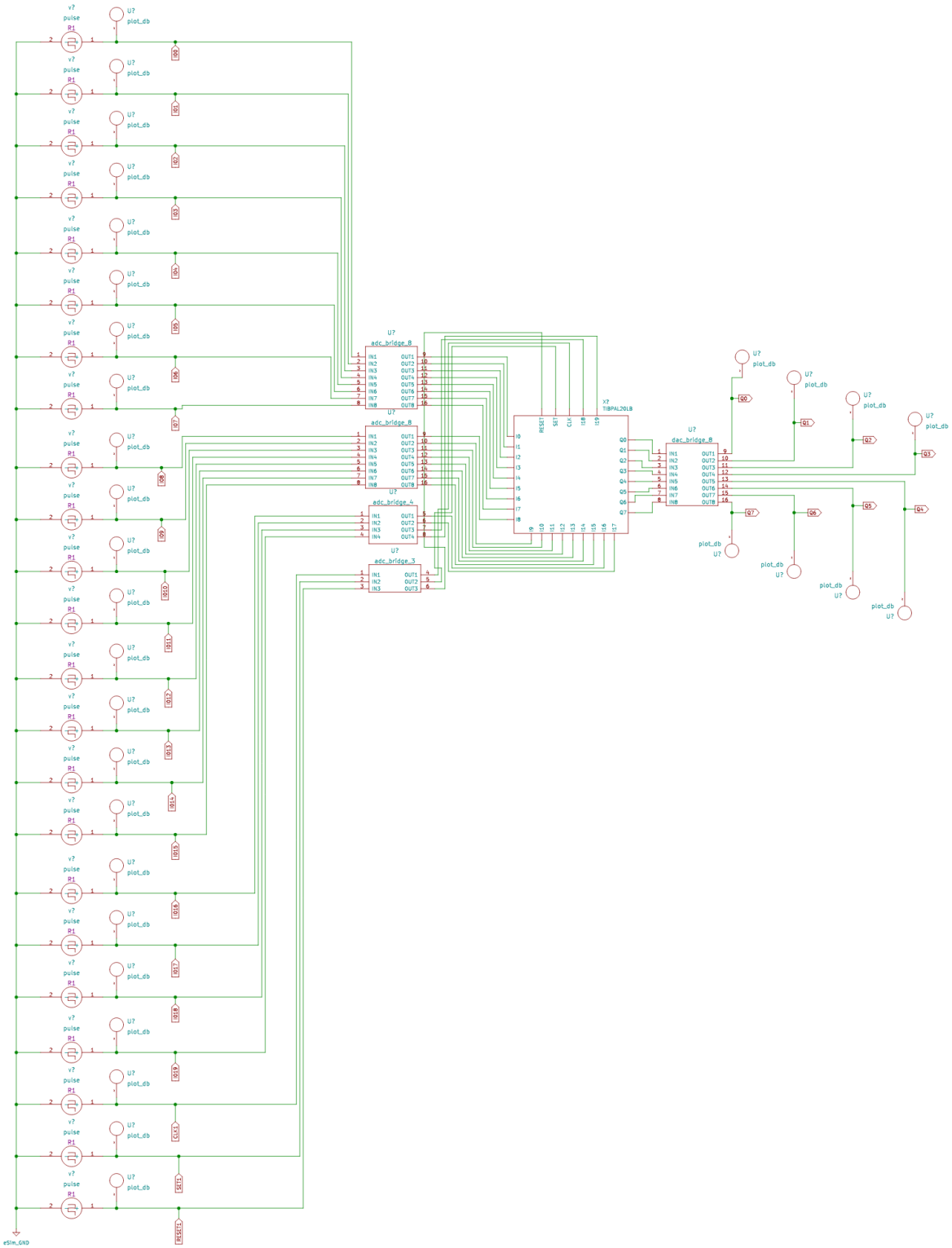

Figure 6.3: Test Circuit of the TIBPAL20L8

6.7 Function Table

Time	RESET	SET	Expected Output
0–100 ns	1	0	`00000000` (reset active)
100–200 ns	0	0	hold `00000000`
200–350 ns	0	1	`11111111` (set active)
350–700 ns	0	0	clocked operation / hold

Figure 6.4: Function Table of the TIBPAL20L8

6.8 Function Table

Test Case Verification Table

Test Case	CLK Pulse	RESET Pulse	SET Pulse	Expected Output	Verification
TC1: Reset Verification	`PULSE(0 5 0n 5n 5n 50n 100n)`	`PULSE(0 5 0n 5n 5n 100n 300n)`	`0`	`00000000`	While `RESET=1`, all outputs must stay LOW
TC2: Set + Clock Verification	`PULSE(0 5 0n 5n 5n 50n 100n)`	`0`	`PULSE(0 5 50n 5n 5n 100n 300n)`	`11111111` → hold/update	When `SET=1`, all outputs become HIGH; after SET goes LOW, outputs hold/update on next CLK

Figure 6.5: Function Table of the TIBPAL20L8 for All Test case

6.9 Input Plot

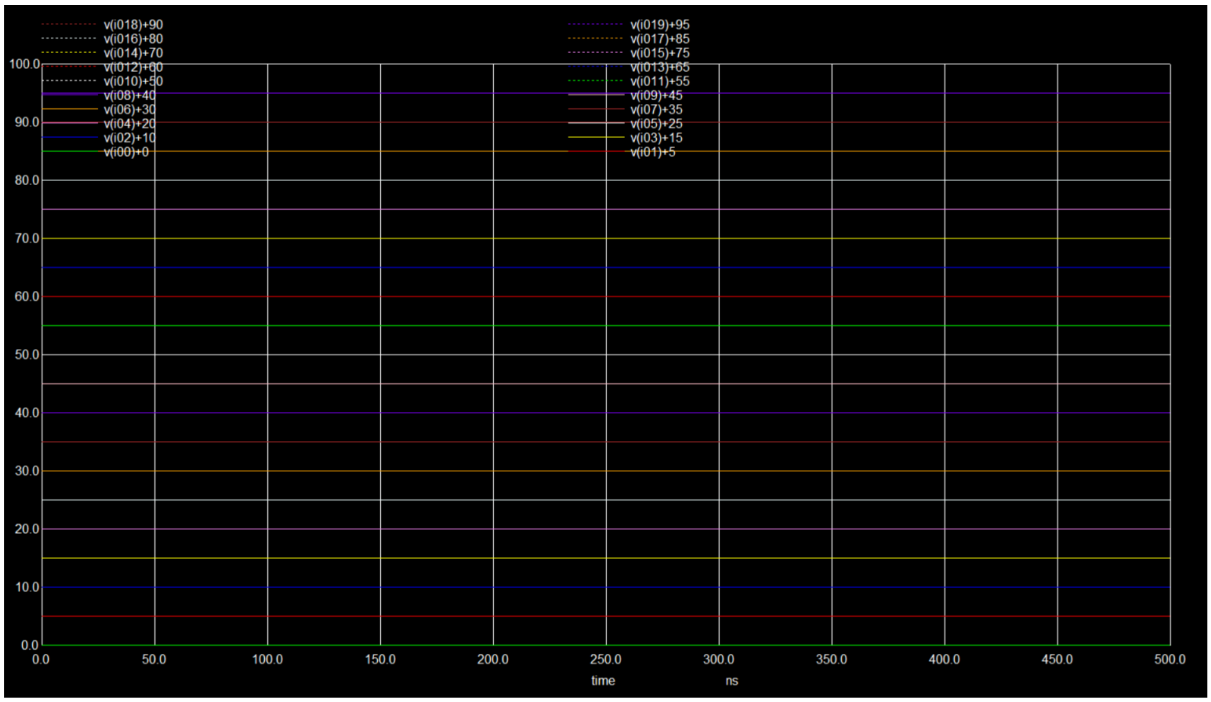

Figure 6.6: Input signals of the TIBPAL20L8

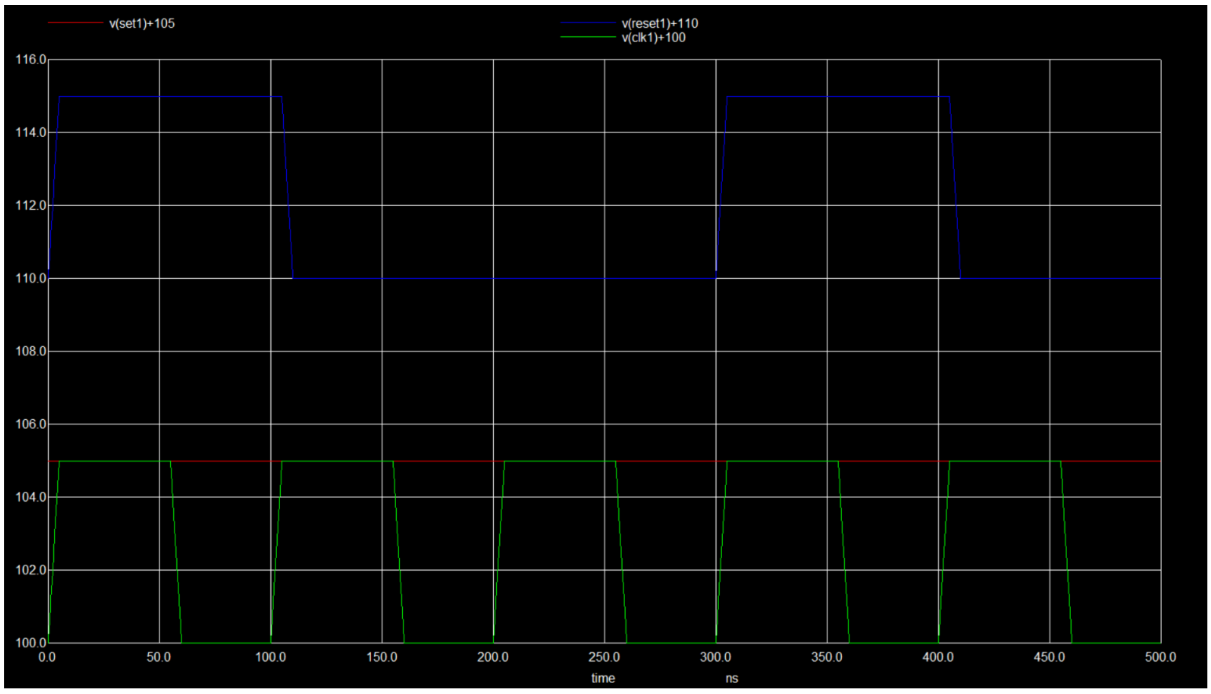

Figure 6.7: Input signals of the TIBPAL20L8 for Reset

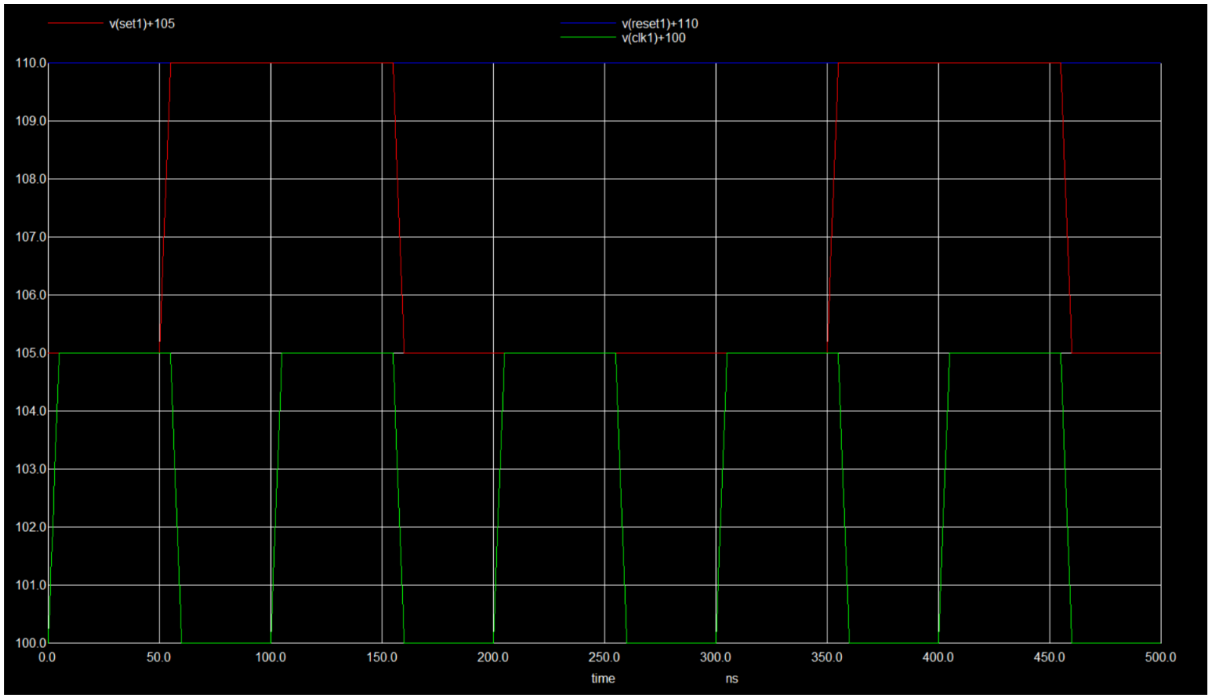

Figure 6.8: Input signals of the TIBPAL20L8 for one Set

6.10 Output Plot

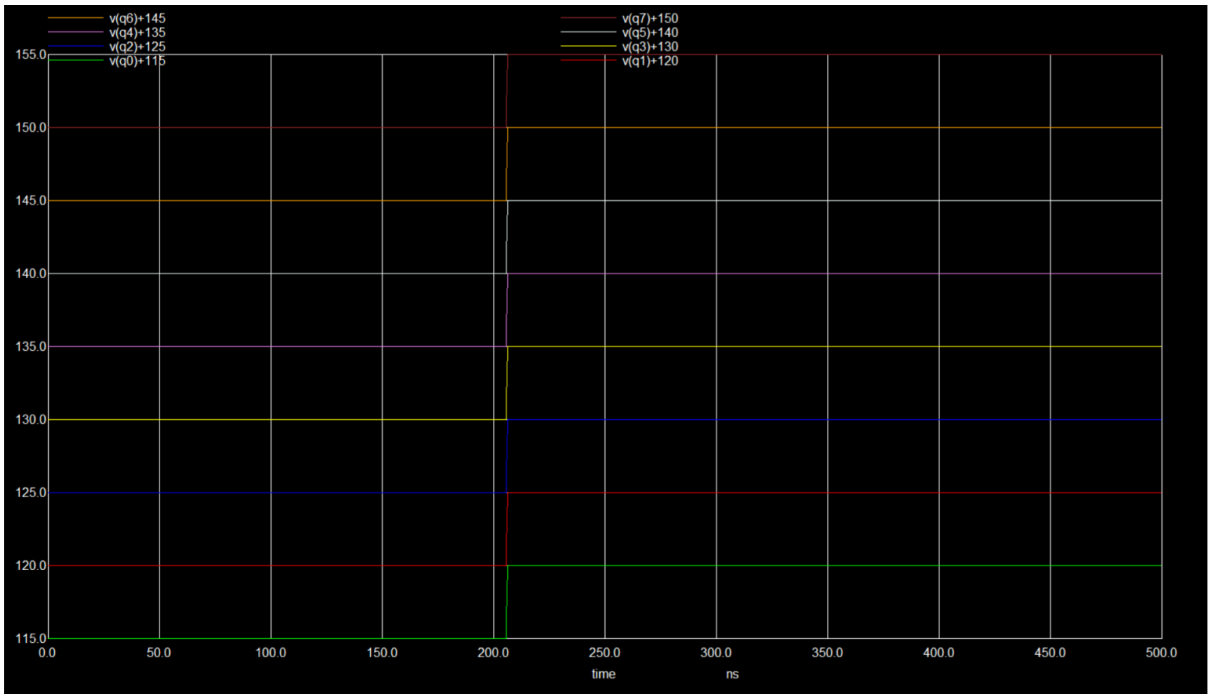

Figure 6.9: Output signals of the TIBPAL20L8 for reset logic

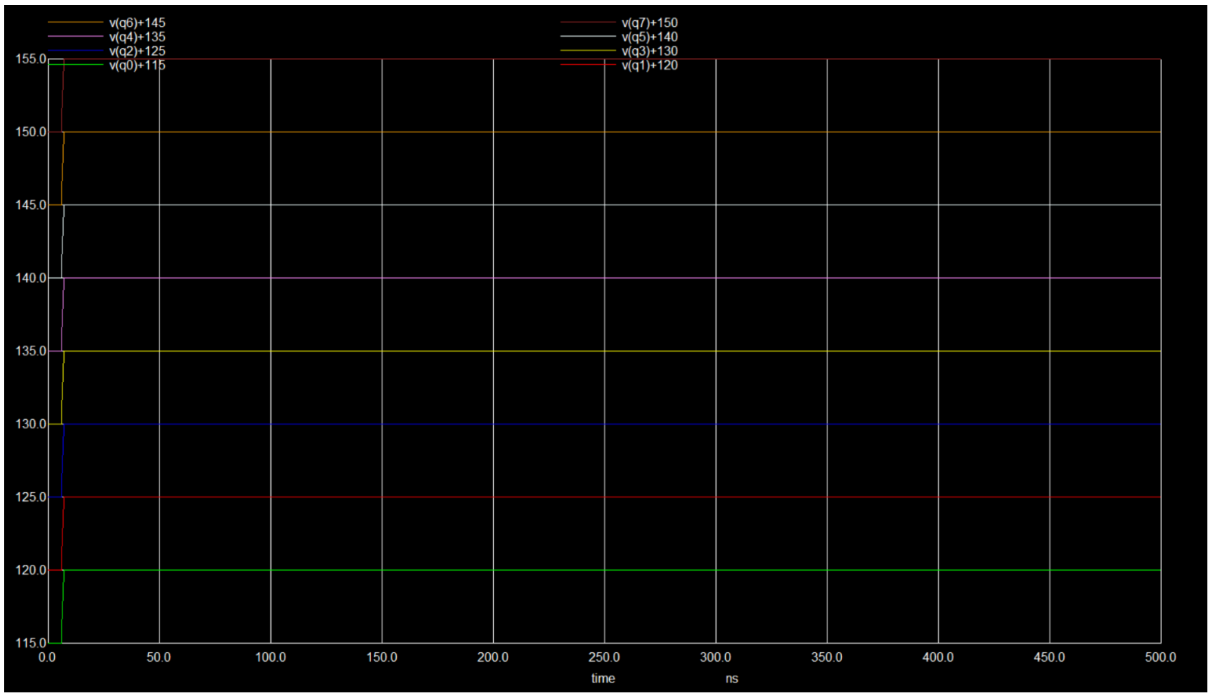

Figure 6.10: Output signals of the TIBPAL20L8 for set logic

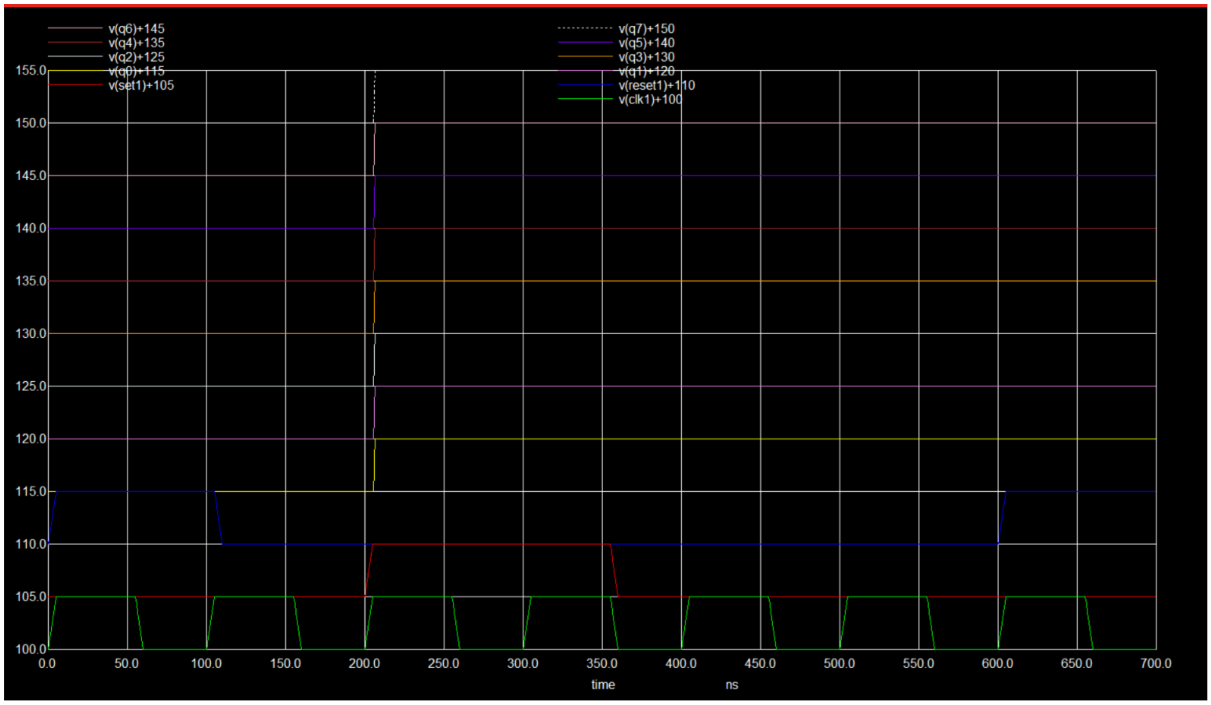

Figure 6.11: Output Signals of the TIBPAL20L8 for all test case

Chapter 7

SN74S134

7.1 General Description

The SN74S134 is a 12-input NAND gate with 3-state output from the Schottky TTL (S) logic family [5]. It performs a NAND operation on twelve input signals and provides a 3-state output, allowing the output to be enabled, disabled (high-impedance), or driven LOW/HIGH based on control signals. Built using high-speed Schottky technology, it offers fast switching performance, reliable logic operation, and TTL-compatible inputs and outputs.

7.2 Key Features

- Performs NAND operation on **12 independent input lines**.
- Includes **3-state output control** for bus sharing and output isolation.
- Supports **high-speed switching** using Schottky TTL technology.
- TTL-compatible inputs and outputs for easy system integration.
- Suitable for implementing wide-input logic functions in compact hardware.

7.3 Applications

- Bus-oriented systems requiring controlled 3-state outputs.
- Large combinational logic implementations with multiple inputs.
- Address decoding and enable logic circuits.
- Digital control systems and high-speed logic interfacing.

7.4 Subcircuit

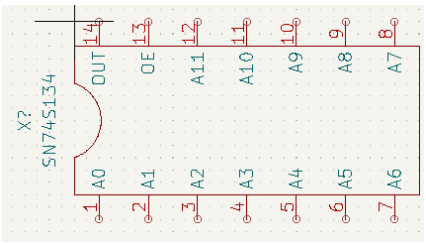

Figure 7.1: Subcircuit of SN74S134

7.5 Subcircuit Schematic Diagram

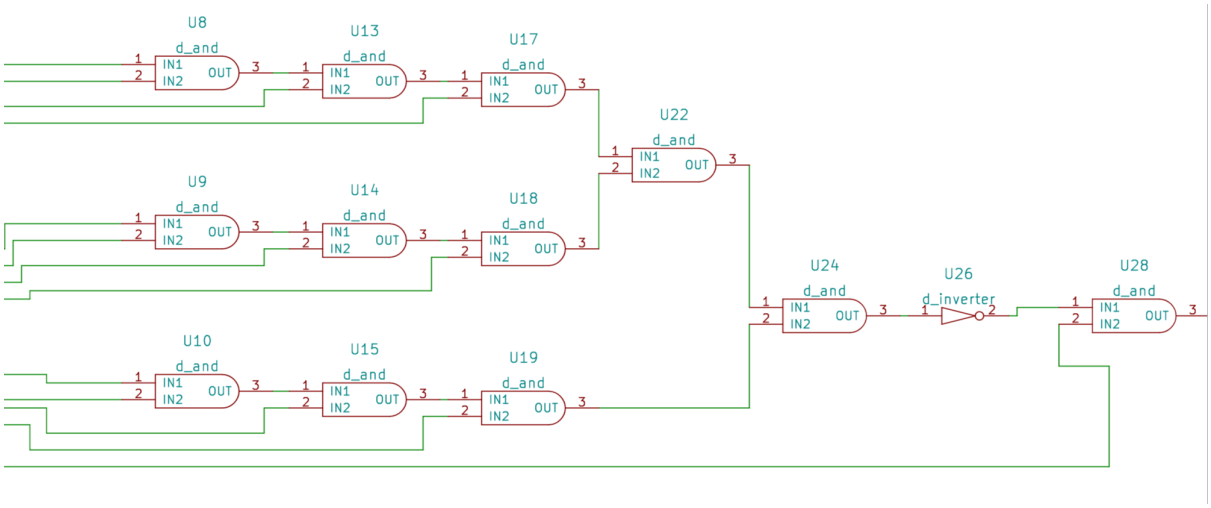

Figure 7.2: Subcircuit Schematic of the (Part of ic) SN74S134

7.6 Test Circuit

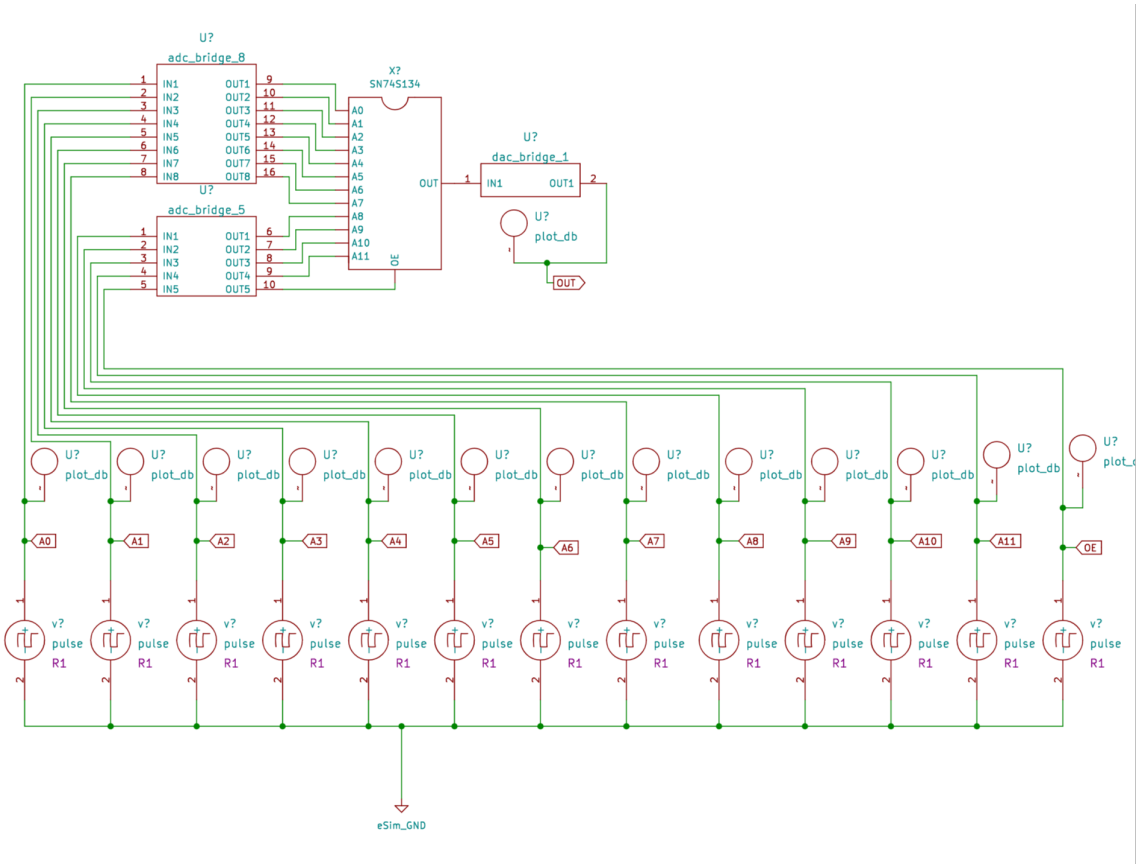

Figure 7.3: Test Circuit of the SN74S134

7.7 Function Table

OE	A0–A11 condition	NAND Output	Expected Y in eSim
0	all HIGH (111111111111)	0	0
0	any one LOW	1	1
0	multiple LOWs	1	1
1	all HIGH	Z (Hi-Z)	0 *(used in eSim)*
1	any one LOW	Z (Hi-Z)	0 *(used in eSim)*

Figure 7.4: Function Table of the SN74S134

7.8 Output Plot

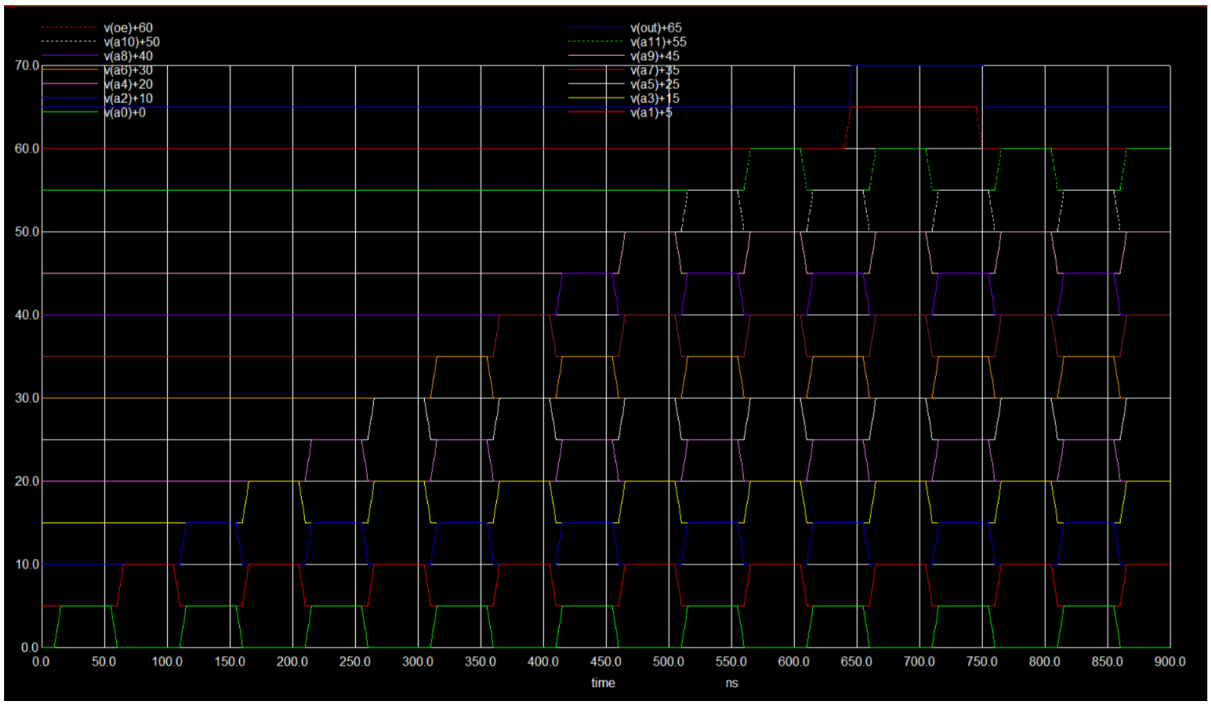

Figure 7.5: Input and Output signals of the SN74S134

Chapter 8

MC14561B

8.1 General Description

The MC14561B is a 9's complement generator from the CMOS logic family [5]. It generates the 9's complement of a 4-bit Binary-Coded Decimal (BCD) input, producing the arithmetic complement required for decimal subtraction operations. Designed using CMOS technology, the device offers low power consumption, reliable logic performance, and compatibility with digital arithmetic and calculator systems.

8.2 Key Features

- Generates the 9's complement of a 4-bit BCD input.
- Supports decimal arithmetic and subtraction operations.
- CMOS implementation for low power consumption.
- High noise immunity and reliable digital logic operation.
- Compatible with BCD-based arithmetic systems and calculators.

8.3 Applications

- Decimal subtraction and arithmetic circuits.
- BCD arithmetic logic units (ALUs).
- Digital calculators and computation systems.
- Embedded systems using decimal data processing.

8.4 Subcircuit

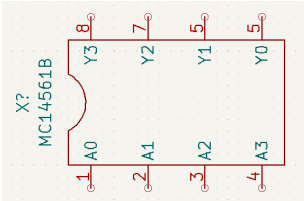

Figure 8.1: Subcircuit of MC14561B

8.5 Subcircuit Schematic Diagram

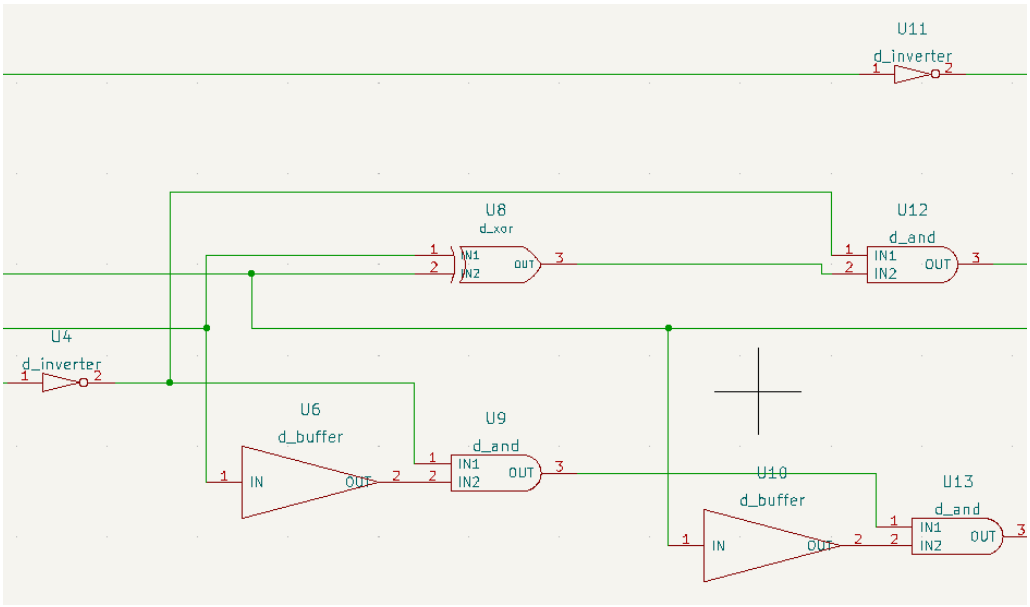

Figure 8.2: Subcircuit Schematic of the MC14561B

8.6 Test Circuit

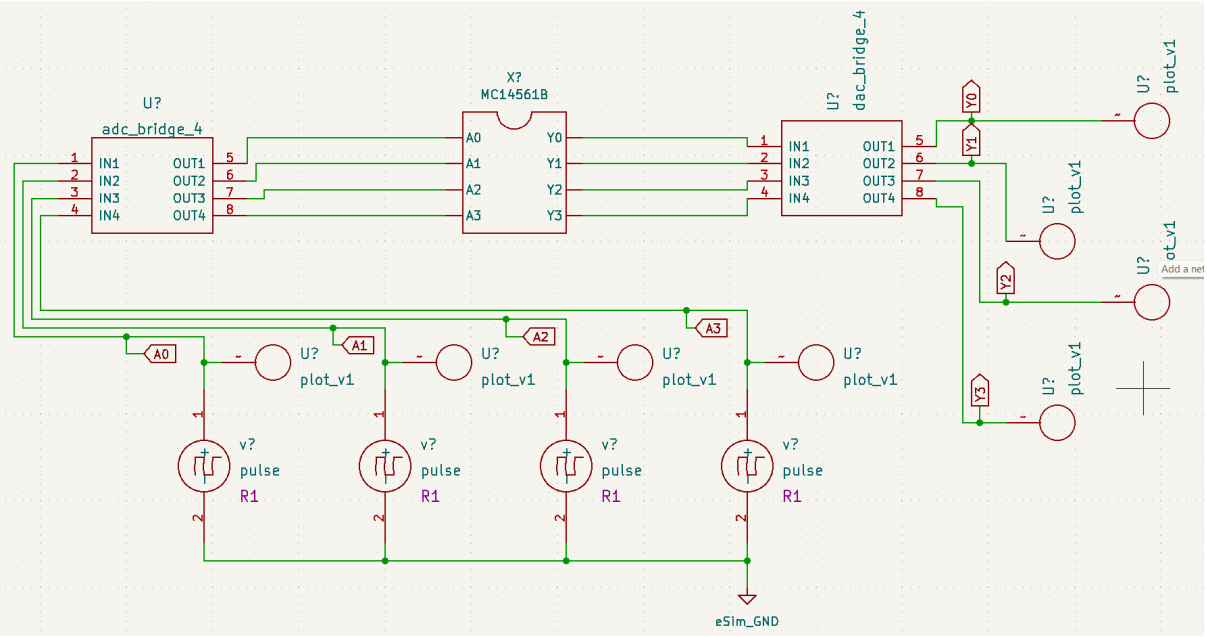

Figure 8.3: Test Circuit of the MC14561B

8.7 Function Table

Input (A3 A2 A1 A0)	Decimal	Expected Output (Y3 Y2 Y1 Y0)	9's Complement
0000	0	1001	9
0001	1	1000	8
0010	2	0111	7
0011	3	0110	6
0100	4	0101	5
0101	5	0100	4
0110	6	0011	3
0111	7	0010	2
1000	8	0001	1
1001	9	0000	0

Figure 8.4: Function Table of the MC14561B

8.8 Output Plot

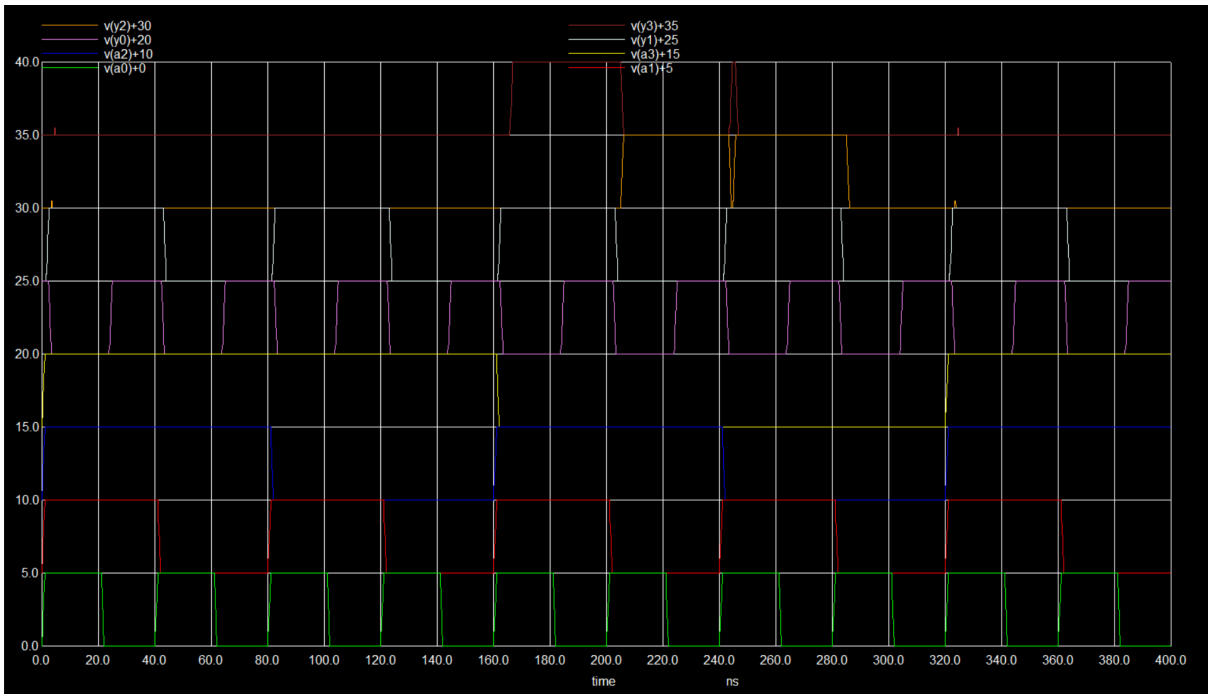

Figure 8.5: Input and Output signals of the MC14561B

Chapter 9

Am2902

9.1 General Description

The Am2902 is a 4-bit lookahead carry generator designed for bit-slice arithmetic systems [5]. It generates high-speed carry signals for cascaded ALU operations by using propagate and generate inputs from arithmetic logic units. The device improves arithmetic speed by reducing carry propagation delay in multi-bit digital systems.

9.2 Key Features

- Generates high-speed carry outputs for bit-slice ALU systems.
- Supports lookahead carry computation using propagate and generate inputs.
- Reduces carry propagation delay in arithmetic operations.
- Designed for cascading multiple 4-bit arithmetic units.
- TTL-compatible inputs and outputs for easy system integration.

9.3 Applications

- Bit-slice processor and ALU designs.
- High-speed arithmetic computation systems.
- Carry lookahead adders in digital processors.
- Embedded and VLSI arithmetic control circuits.

9.4 Subcircuit

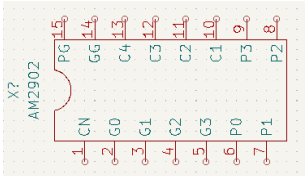

Figure 9.1: Subcircuit of Am2902

9.5 Subcircuit Schematic Diagram

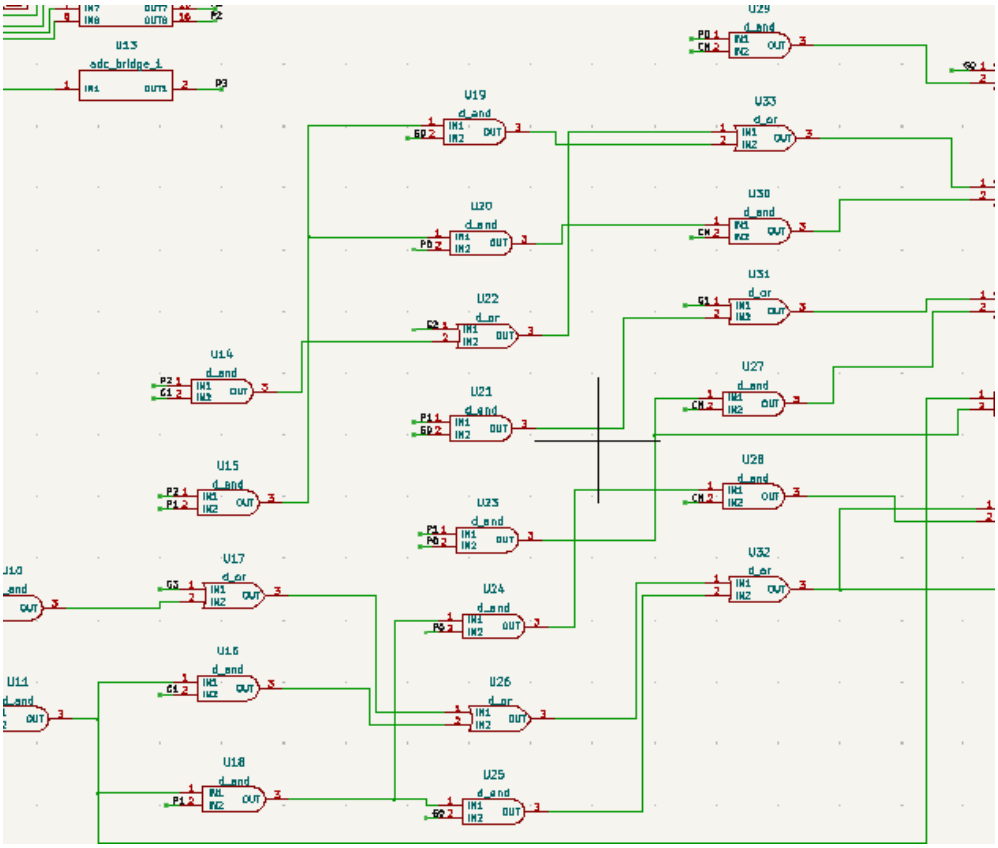

Figure 9.2: Subcircuit Schematic of the (Part of ic) Am2902

9.6 Test Circuit

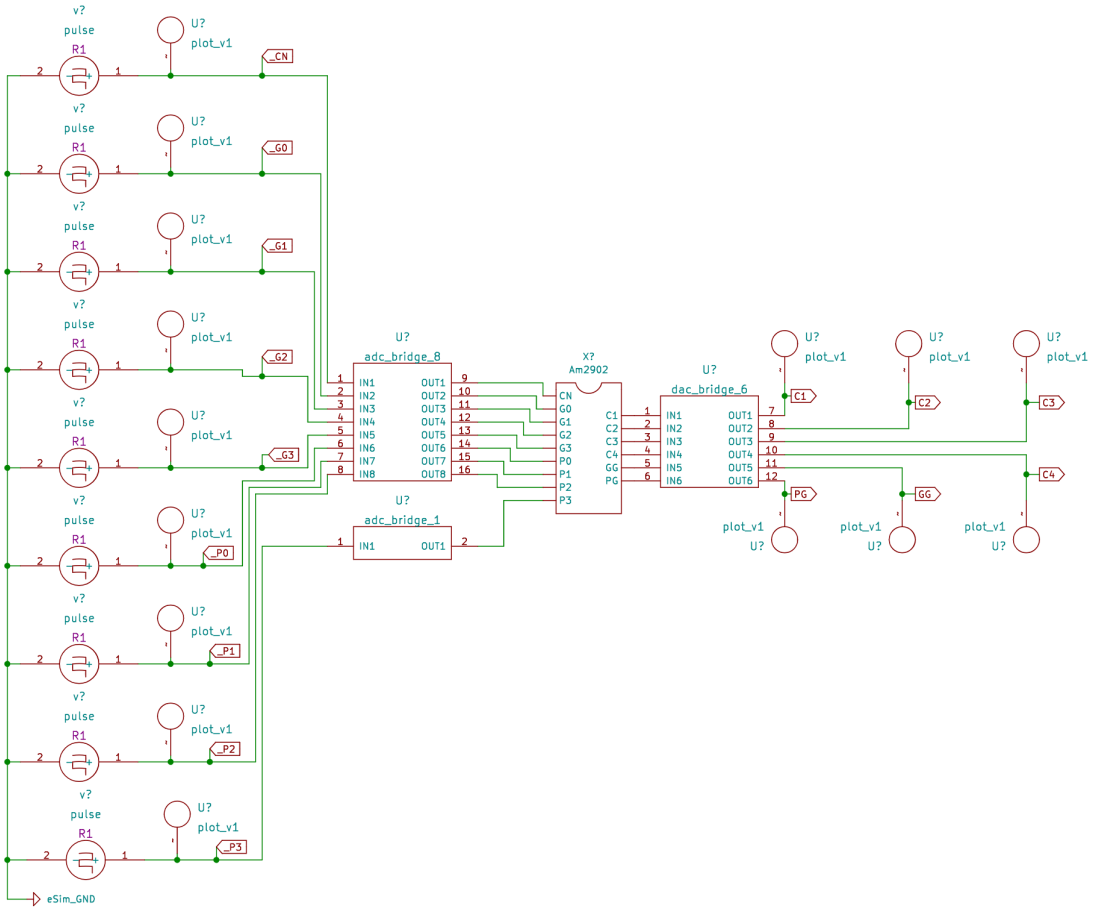

Figure 9.3: Test Circuit of the Am2902

9.7 Function Table

Test Case 1: Pure Propagate Check

Inputs:

All Propagate (P) = **1**

All Generate (G) = **0**

CN	C1	C2	C3	C4
0	0	0	0	0
1	1	1	1	1

Observation: Carry ripples through all stages (Pure Propagate).

Figure 9.4: Function Table of the Am2902 Test case 1

Test Case 2: Pure Generate Check

Inputs:

All Propagate (P) = **0**

All Generate (G) = **1**

CN	C1	C2	C3	C4
0	1	1	1	1

Observation: All carries are forced high independent of CN (Pure Generate).

Figure 9.5: Function Table of the Am2902 Test case 2

Test Case 3: Mixed Realistic Case

Inputs:

P = 1 0 1 0 (P3=0, P2=1, P1=0, P0=1)

G = 0 1 0 0 (G3=0, G2=0, G1=1, G0=0)

CN	C1	C2	C3	C4
0	0	1	1	1
1	1	1	1	1

Observation:

- Carries change according to CN
- Not all carries are equal
- Validates correct internal carry lookahead logic

Figure 9.6: Function Table of the Am2902 Test case 3

9.8 Output Plot

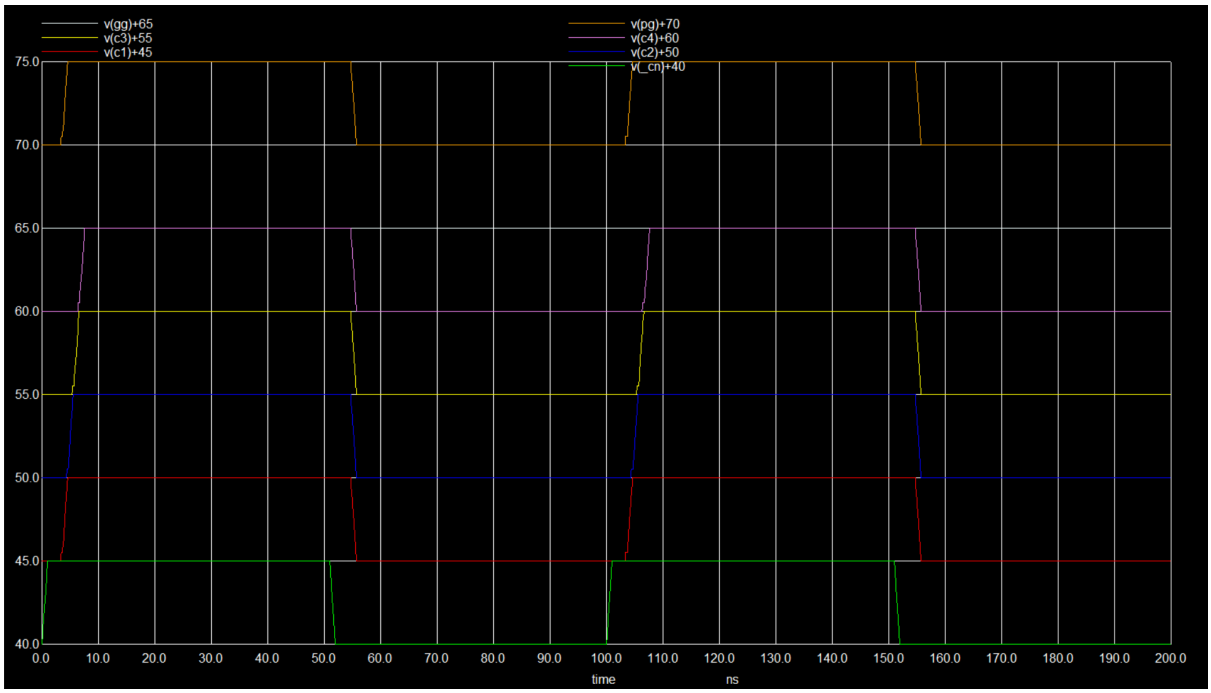

Figure 9.7: Input and Output signals of the Am2902 Test case 1

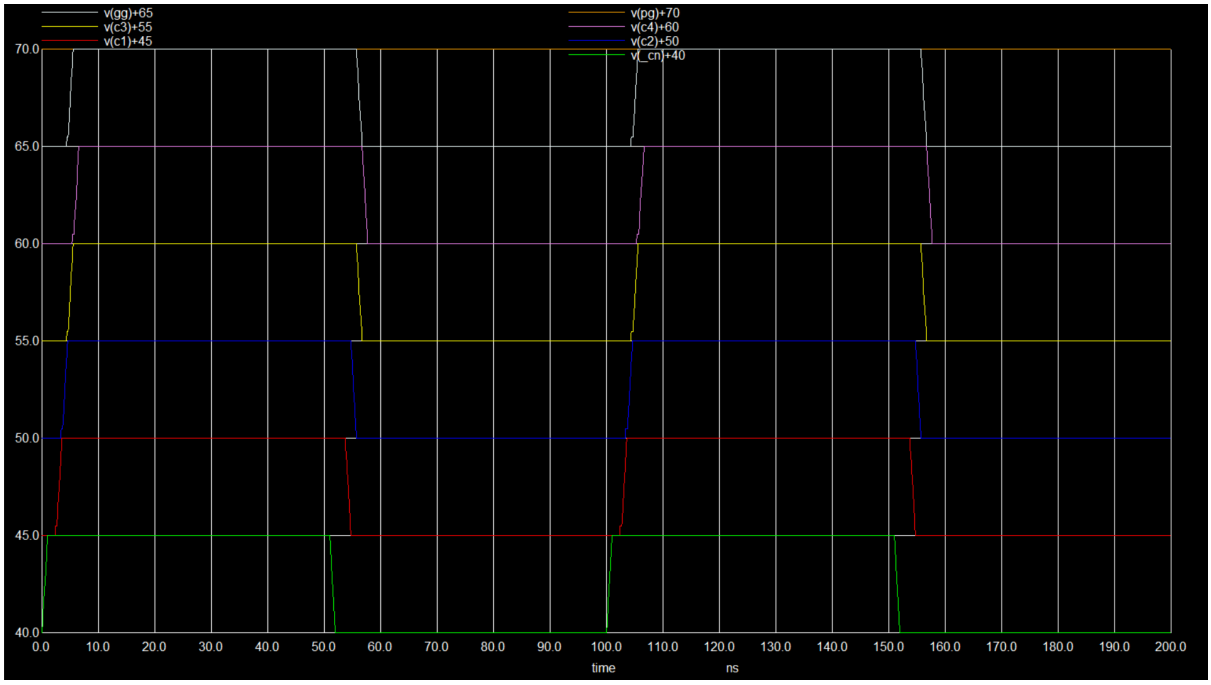

Figure 9.8: Input and Output signals of the Am2902 Test case 2

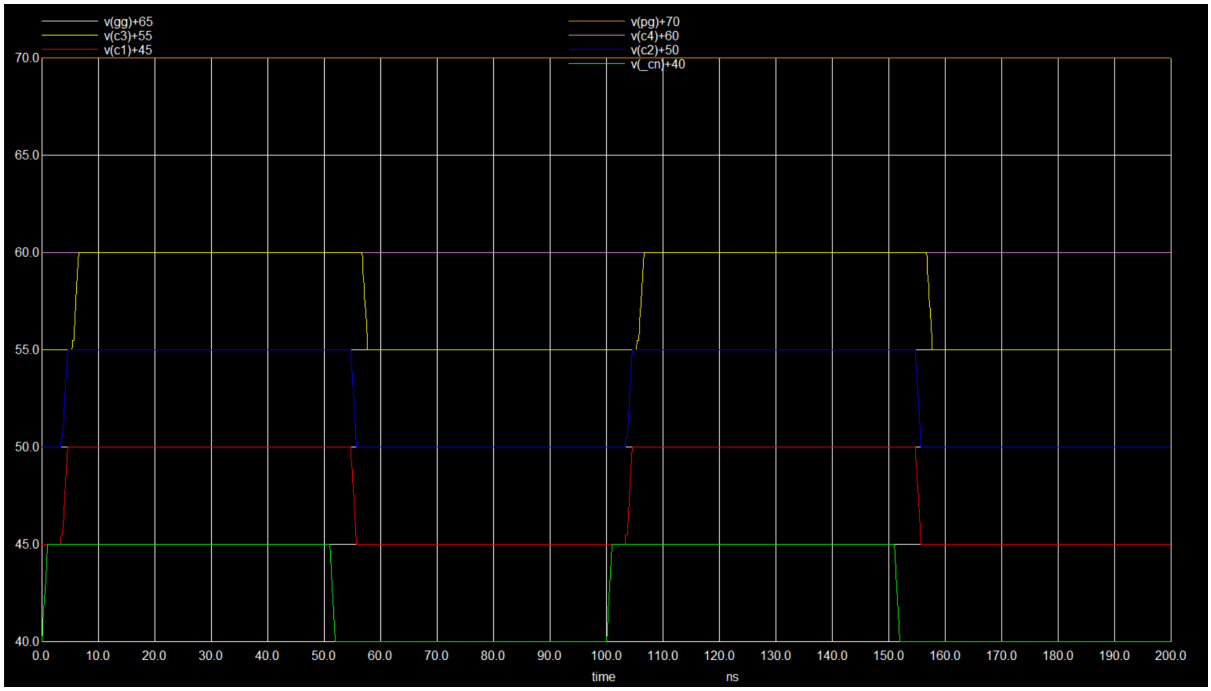

Figure 9.9: Input and Output signals of the Am2902 Test case 3

Chapter 10

SN74LS25

10.1 General Description

The SN74LS25 is a dual 4-input NOR gate with strobe from the Low-Power Schottky TTL (LS) logic family [5]. It contains two independent 4-input NOR gates, each featuring a strobe control input that can force the output LOW regardless of the data inputs. Designed using low-power Schottky technology, the device provides high-speed logic operation, reduced power consumption, and TTL-compatible inputs and outputs for reliable digital system integration.

10.2 Key Features

- Contains two independent 4-input NOR gates.
- Includes strobe control inputs for output enable and logic control.
- Performs NOR logic operation on four input signals.
- Low-power Schottky TTL implementation for reduced power consumption.
- TTL-compatible inputs and outputs for easy interfacing.

10.3 Applications

- Digital control and combinational logic circuits.
- Bus control and gating applications using strobe functionality.
- Embedded systems requiring compact NOR logic implementation.
- High-speed digital systems and TTL interfacing applications.

10.4 Subcircuit

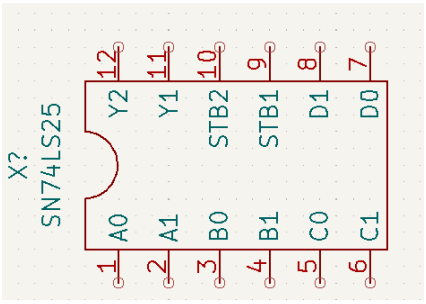

Figure 10.1: Subcircuit of SN74LS25

10.5 Subcircuit Schematic Diagram

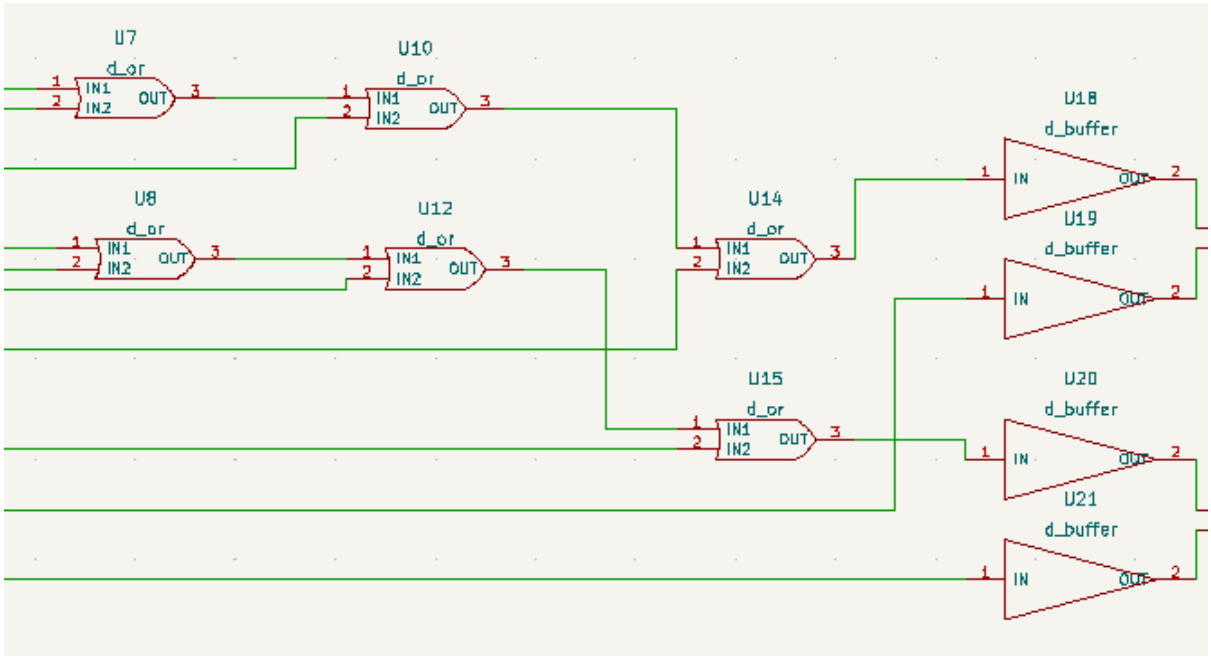

Figure 10.2: Subcircuit Schematic of the (Part of ic) SN74LS25

10.6 Test Circuit

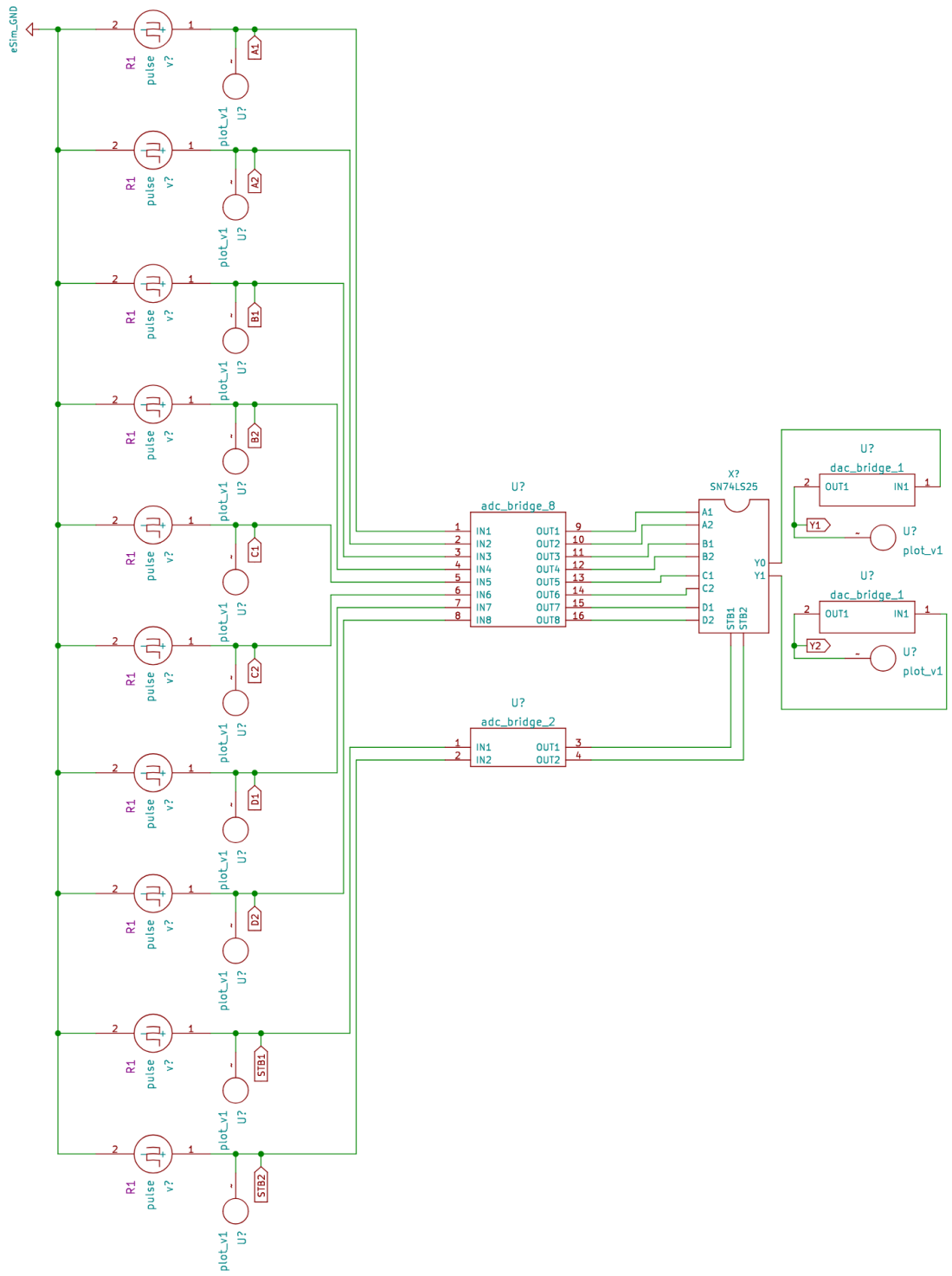

Figure 10.3: Test Circuit of the SN74LS25

10.7 Function Table

Time Interval	A	B	C	D	STB	Expected Y	Reason
0ns – 20ns	0	0	0	0	0	1	All inputs LOW → NOR output HIGH
20ns – 40ns	1	0	0	0	0	0	A=1 forces NOR LOW
40ns – 60ns	1	1	0	0	0	0	Multiple HIGH inputs → NOR LOW
60ns – 80ns	1	1	1	0	0	0	Any HIGH input keeps output LOW
80ns – 100ns	1	1	1	1	0	0	All HIGH → NOR LOW
100ns – 120ns	0	1	1	1	0	0	B/C/D HIGH → output LOW
120ns – 140ns	X	X	X	X	1	0	STB active HIGH forces output LOW
140ns – 160ns	X	X	X	X	1	0	Output remains forced LOW
160ns – 180ns	0	0	1	1	0	0	Inputs active again after STB LOW
180ns – 200ns	0	0	0	1	0	0	D=1 → NOR LOW
200ns – 220ns	0	0	0	0	0	1	All LOW again → output HIGH
220ns – 240ns	1	0	0	0	0	0	A=1 → output LOW
240ns – 300ns	X	X	X	X	1	0	STB again forces output LOW
300ns – 500ns	pulse combinations	pulse combinations	pulse combinations	pulse combinations	pulse combinations	According to NOR logic	Continuous dynamic verification

Figure 10.4: Function Table of the SN74LS25

10.8 Output Plot

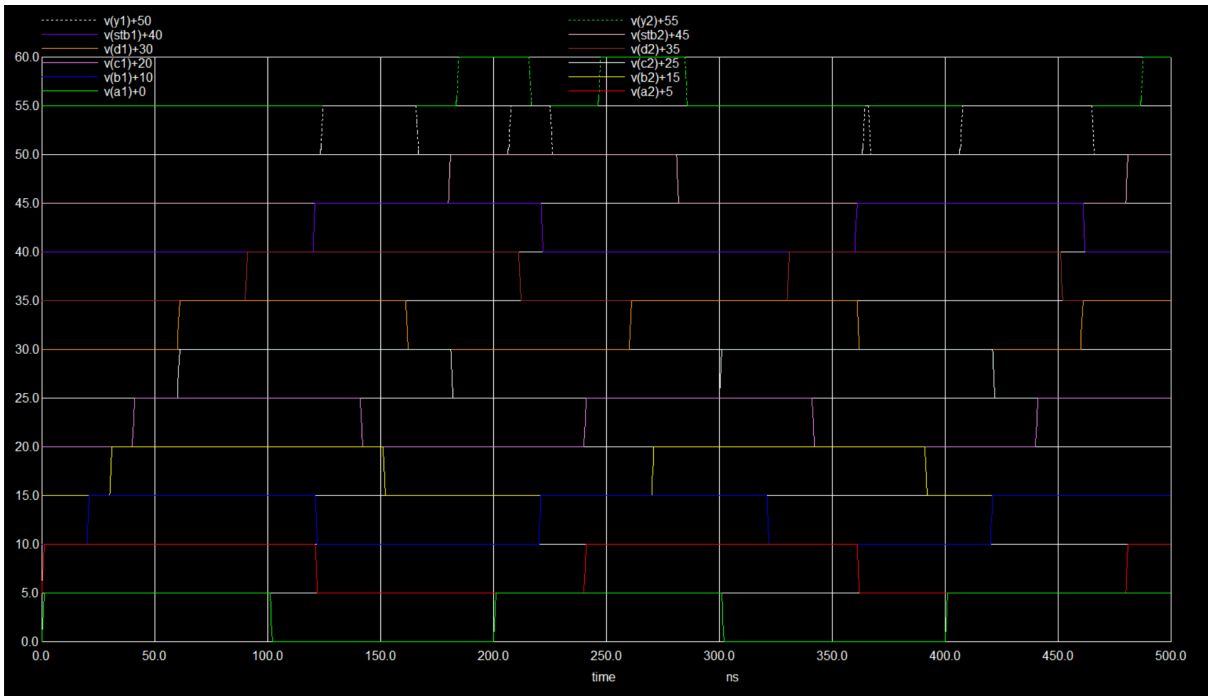

Figure 10.5: Input and Output signals of the SN74LS25

Chapter 11

MC14530B

11.1 General Description

The MC14530B is a dual 5-input majority gate from the CMOS logic family [5]. It contains two independent majority gates, each producing a HIGH output when three or more of the five inputs are HIGH. Designed using CMOS technology, the device provides low power consumption, reliable logic operation, and compatibility with a wide range of digital systems.

11.2 Key Features

- Contains two independent 5-input majority gates.
- Output becomes HIGH when three or more inputs are HIGH.
- CMOS implementation for low power consumption.
- High noise immunity and reliable digital operation.
- Suitable for voting logic and fault-tolerant digital systems.

11.3 Applications

- Majority voting and decision-making circuits.
- Fault-tolerant and redundant digital systems.
- Digital control and arbitration logic.
- Embedded systems and combinational logic applications.

11.4 Subcircuit

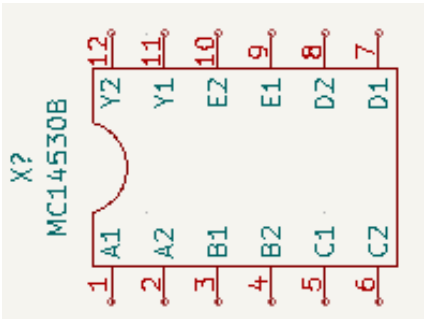

Figure 11.1: Subcircuit of MC14530B

11.5 Subcircuit Schematic Diagram

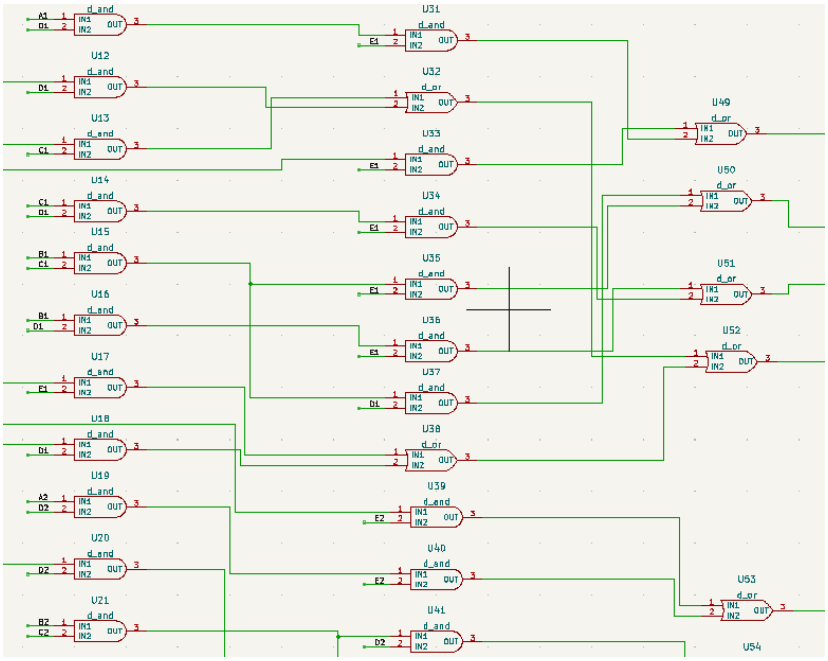

Figure 11.2: Subcircuit Schematic of the (Part of ic) MC14530B

11.6 Test Circuit

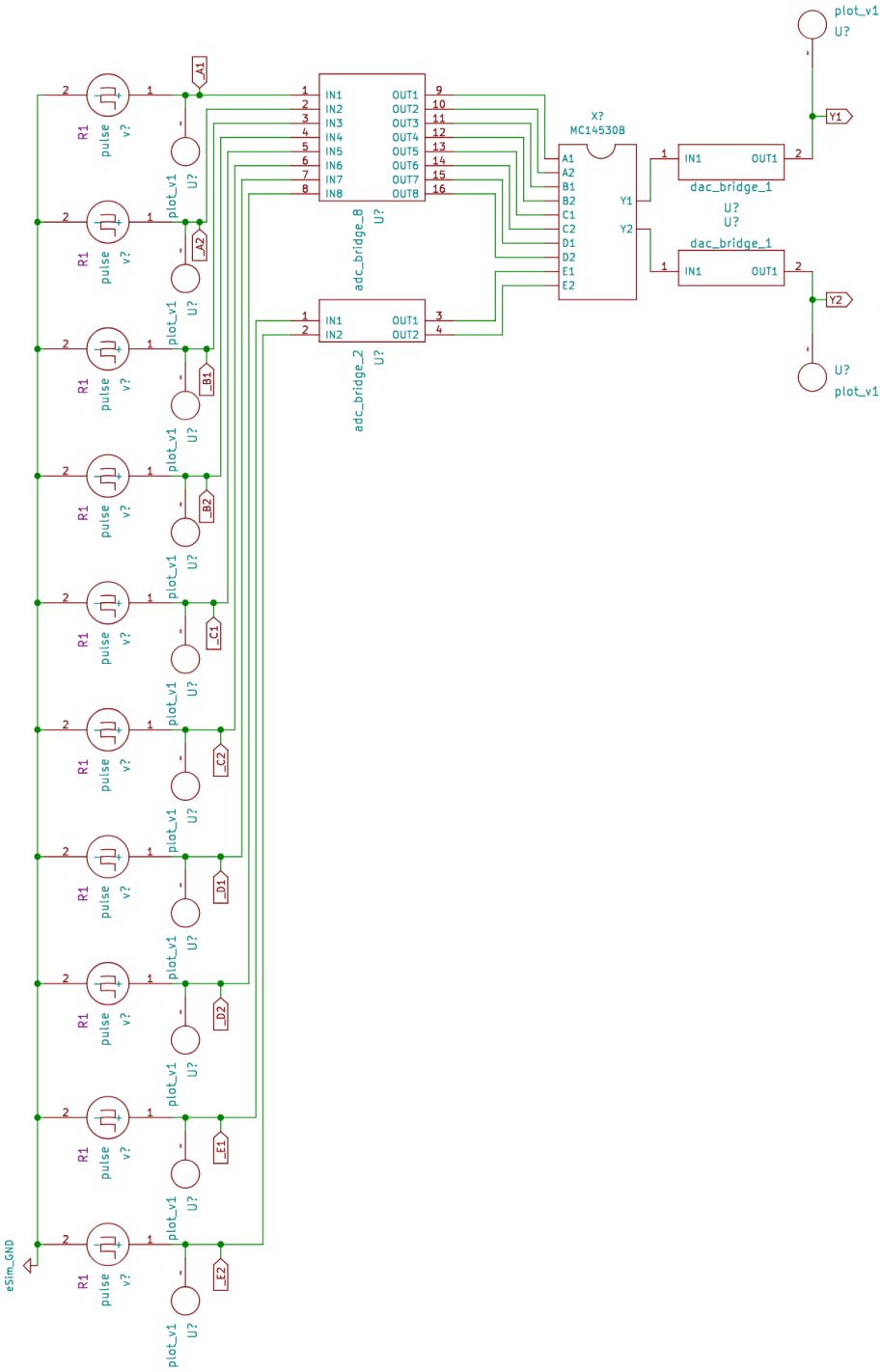

Figure 11.3: Test Circuit of the MC14530B

11.7 Function Table

Time	A	B	C	D	E	Number of HIGH Inputs	Expected Y	Status
0 ns	0	0	0	0	0	0	0	
20 ns	1	0	0	0	0	1	0	
40 ns	1	1	0	0	0	2	0	
60 ns	1	1	1	0	0	3	1	✅
80 ns	1	1	1	1	0	4	1	✅
100 ns	1	1	1	1	1	5	1	✅

Figure 11.4: Function Table of the MC14530B

11.8 Output Plot

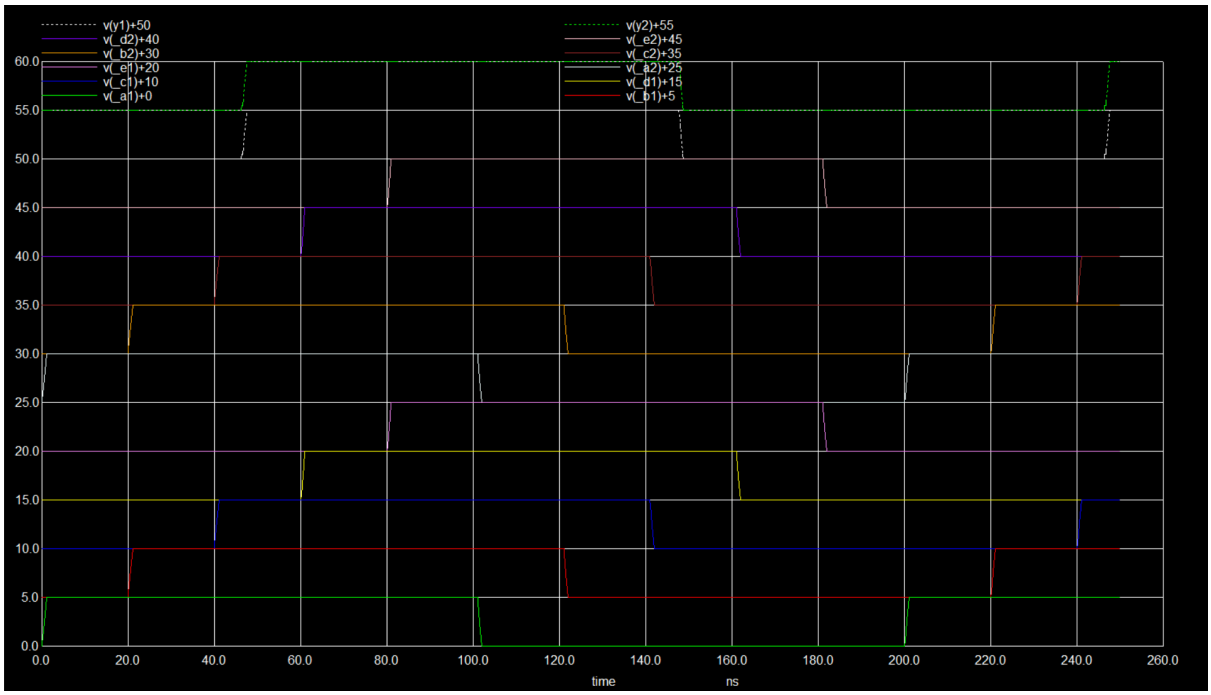

Figure 11.5: Input and Output signals of the MC14530B

Chapter 12

SN74S281

12.1 General Description

The SN74S281 is a high-speed Arithmetic Logic Unit (ALU) with carry lookahead capability from the Schottky TTL (S) logic family [5]. It performs arithmetic and logical operations on binary data inputs and supports fast carry generation using lookahead carry techniques for improved computational speed. Designed using Schottky TTL technology, the device offers high-speed operation, reliable arithmetic processing, and TTL-compatible inputs and outputs suitable for digital computing systems.

12.2 Key Features

- Performs arithmetic and logic operations on binary inputs.
- Supports carry lookahead functionality for high-speed computation.
- Provides fast carry propagation between bit slices.
- High-speed Schottky TTL implementation for improved performance.
- TTL-compatible inputs and outputs for easy system integration.

12.3 Applications

- Arithmetic Logic Units (ALUs) in processors and microcontrollers.
- High-speed arithmetic computation systems.
- Bit-slice processor architectures and digital computing systems.
- Embedded systems requiring fast arithmetic and logic operations.

12.4 Subcircuit

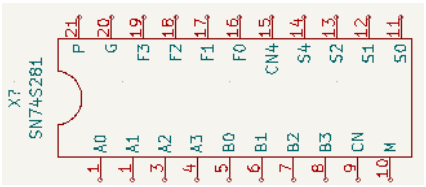

Figure 12.1: Subcircuit of SN74S281

12.5 Subcircuit Schematic Diagram

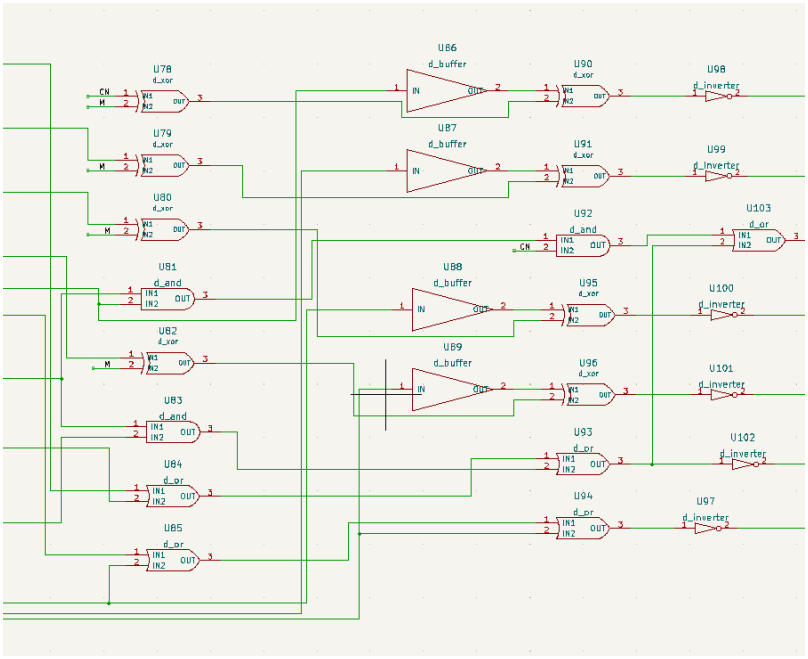

Figure 12.2: Subcircuit Schematic of the (Part of ic) SN74S281

12.6 Test Circuit

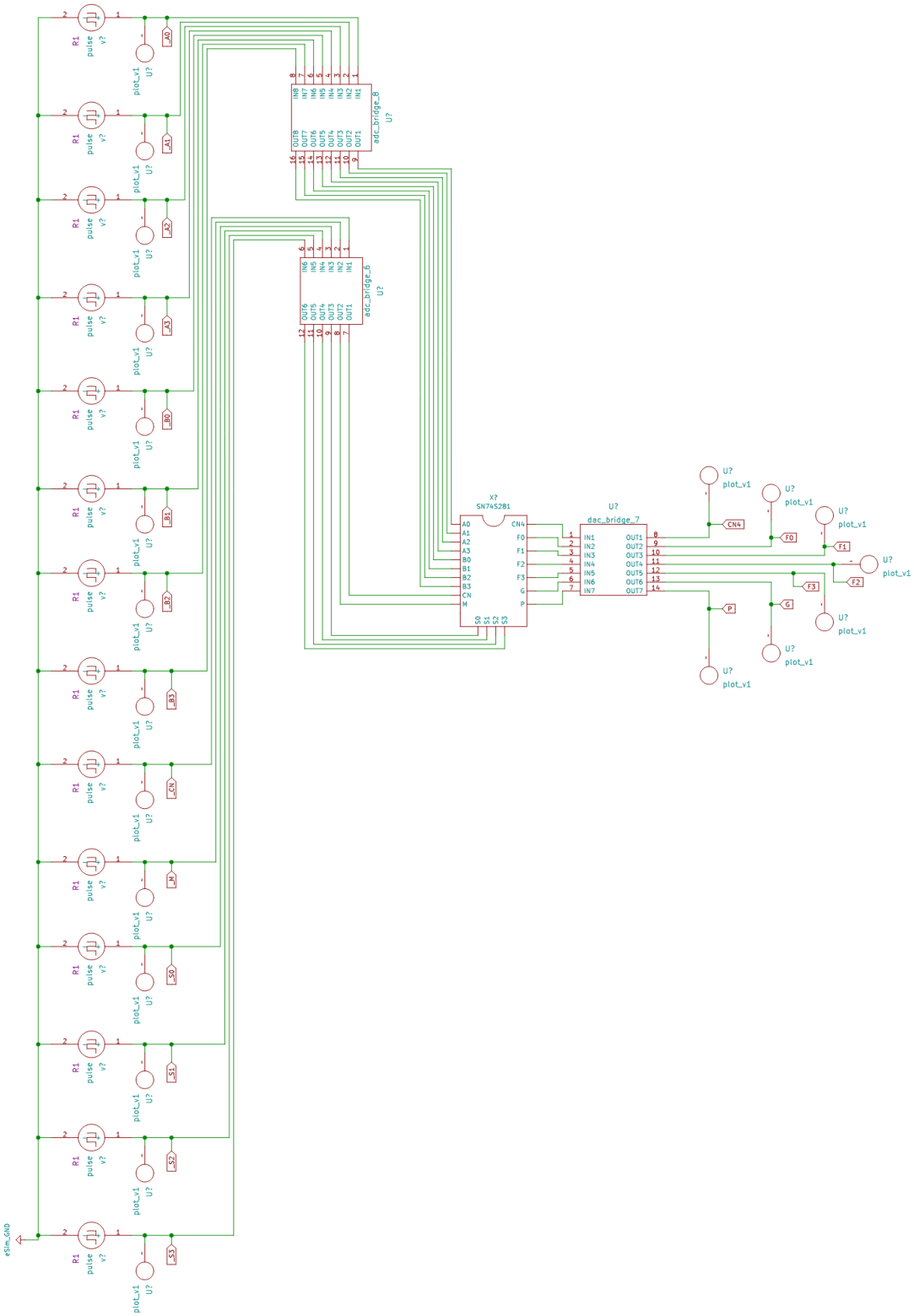

Figure 12.3: Test Circuit of the SN74S281

12.7 Function Table

Test Case 1: Logic Mode (Invert A)

Parameter	Value	Details
Mode (M)	1	Logic Mode
Select (S)	0000	Function: F = ~A
Input A	1010	A3=1, A2=0, A1=1, A0=0
Input B	Don't Care	B inputs ignored
Expected F	0101	~A (Bitwise NOT of A)
Cn	0	Not used in logic mode

Purpose: Verify Logic Inversion operation.

Figure 12.4: Function Table of the SN74S281 Test case 1

Test Case 2: Arithmetic Addition

Parameter	Value	Details
Mode (M)	0	Arithmetic Mode
Select (S)	1001	Function: F = A + B
Input A	0011	Decimal 3
Input B	0101	Decimal 5
Expected F	1000	Decimal 8
Expected Cn+4 (Carry Out)	0	No overflow

Purpose: Verify basic 4-bit addition (3 + 5 = 8).

Figure 12.5: Function Table of the SN74S281 Test case 2

Test Case 3: Carry Out Test

Parameter	Value	Details
Mode (M)	0	Arithmetic Mode
Select (S)	1001	Function: F = A + B
Input A	1111	Decimal 15
Input B	0001	Decimal 1
Expected F	0000	Result with overflow
Expected Cn+4 (Carry Out)	1	Carry generated (16 in decimal)

Purpose: Verify carry-out generation on maximum value overflow (15 + 1 = 16).

Figure 12.6: Function Table of the SN74S281 Test case 3

12.8 Output Plot

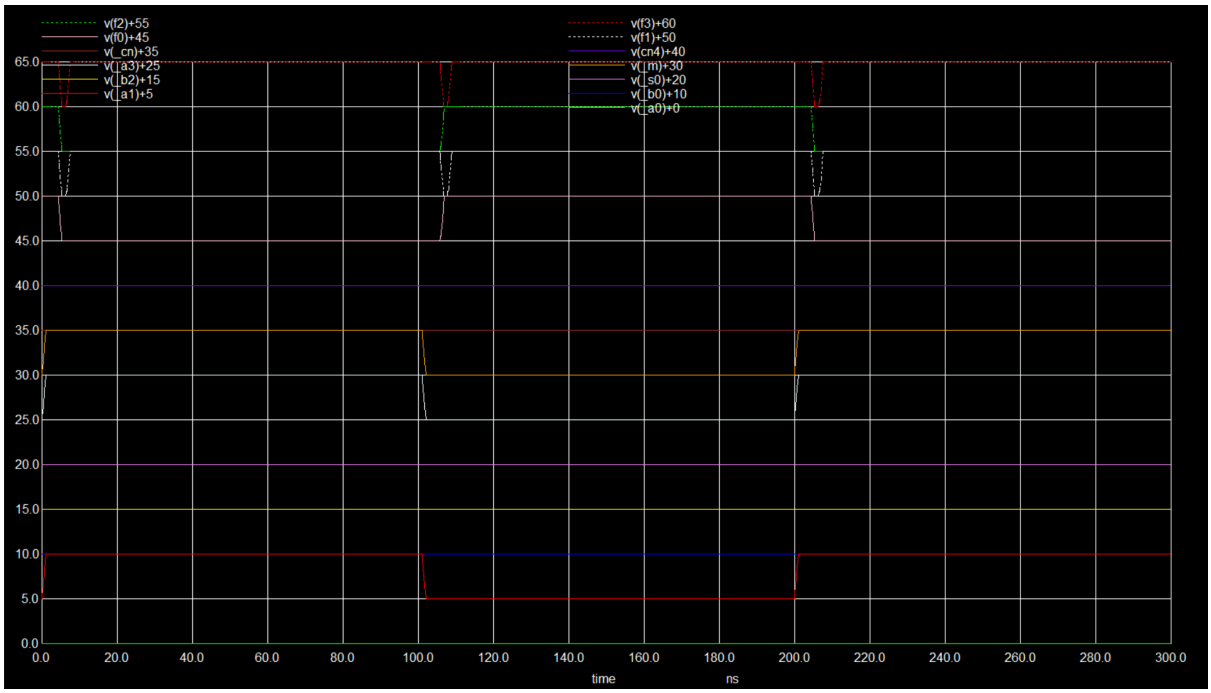

Figure 12.7: Input and Output signals of the SN74S281 Test case 1

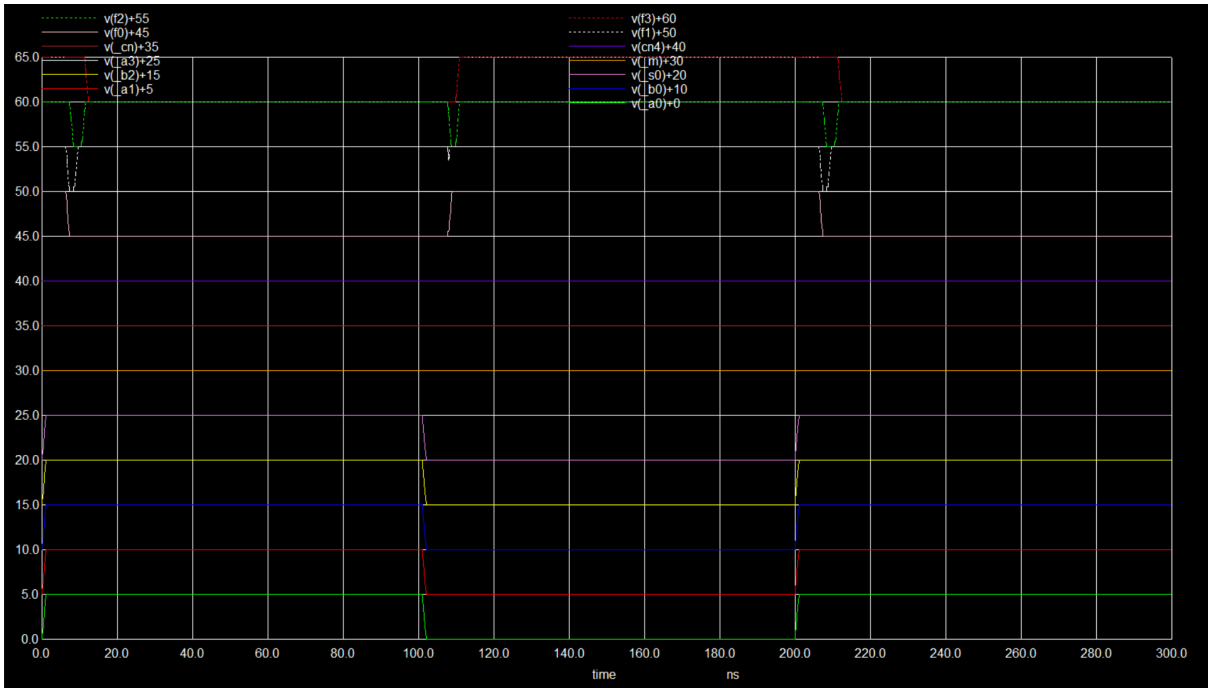

Figure 12.8: Input and Output signals of the SN74S281 Test case 2

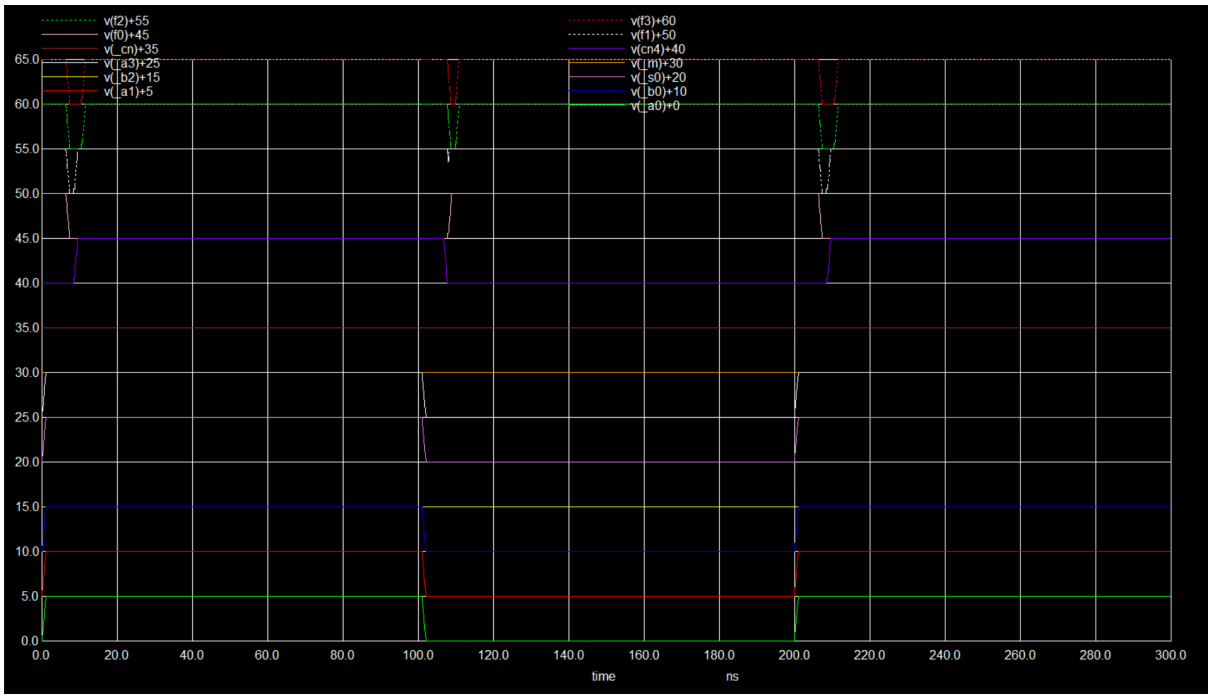

Figure 12.9: Input and Output signals of the SN74S281 Test case 3

Chapter 13

MC14521B

13.1 General Description

The MC14521B is a 24-stage frequency divider from the CMOS logic family [5]. It divides an input clock frequency through a chain of binary counter stages and provides multiple divided frequency outputs. Designed using CMOS technology, the device offers low power consumption, high noise immunity, and reliable frequency division for digital timing and clock generation applications.

13.2 Key Features

- 24-stage binary frequency divider implementation.
- Provides multiple divided clock frequency outputs.
- CMOS technology for low power consumption.
- High noise immunity and stable digital operation.
- Supports clock generation and timing applications.

13.3 Applications

- Digital clock and timing generation circuits.
- Frequency division and clock scaling applications.
- Embedded systems requiring slow timing signals.
- Counters, timers, and digital control systems.

13.4 Subcircuit

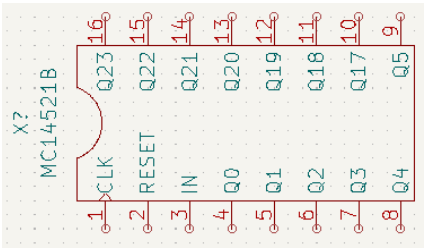

Figure 13.1: Subcircuit of MC14521B

13.5 Subcircuit Schematic Diagram

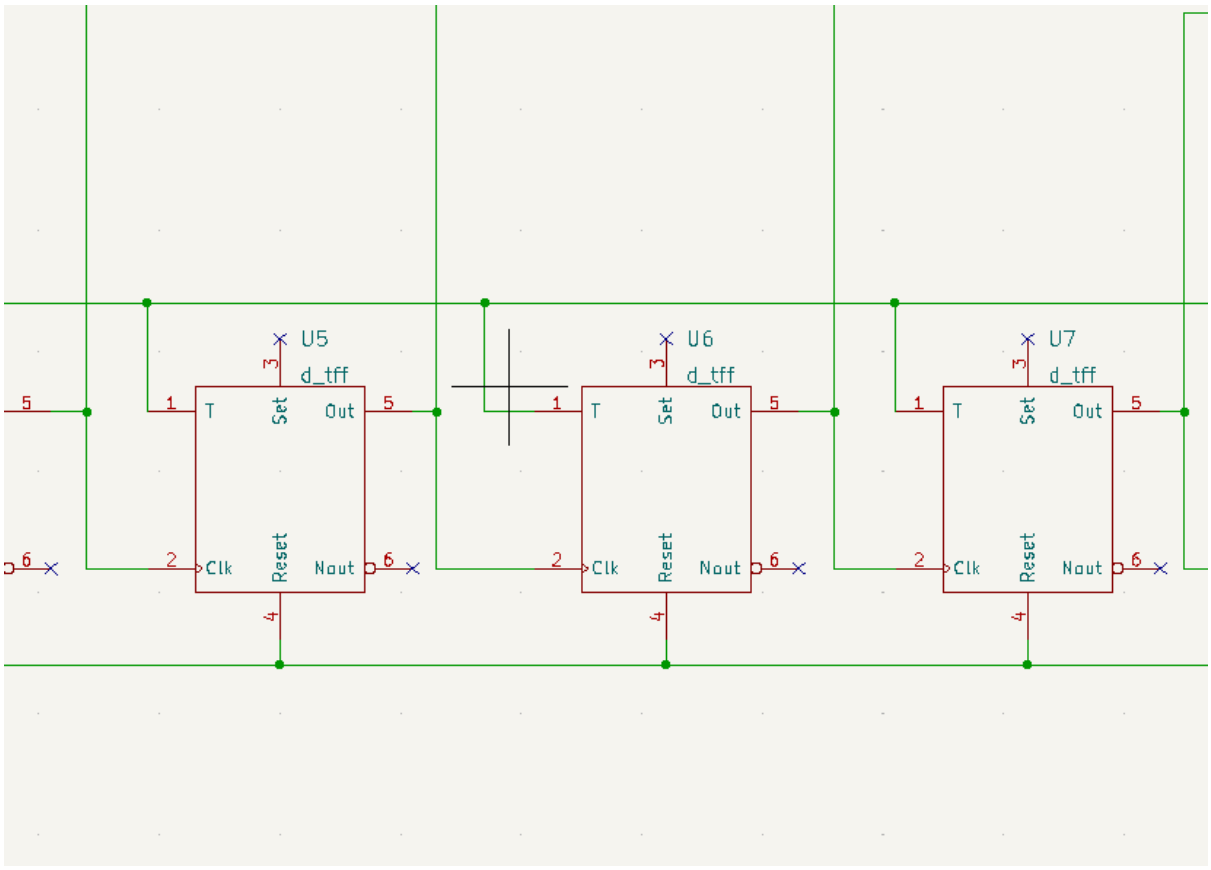

Figure 13.2: Subcircuit Schematic of the (Part of ic) MC14521B

13.6 Test Circuit

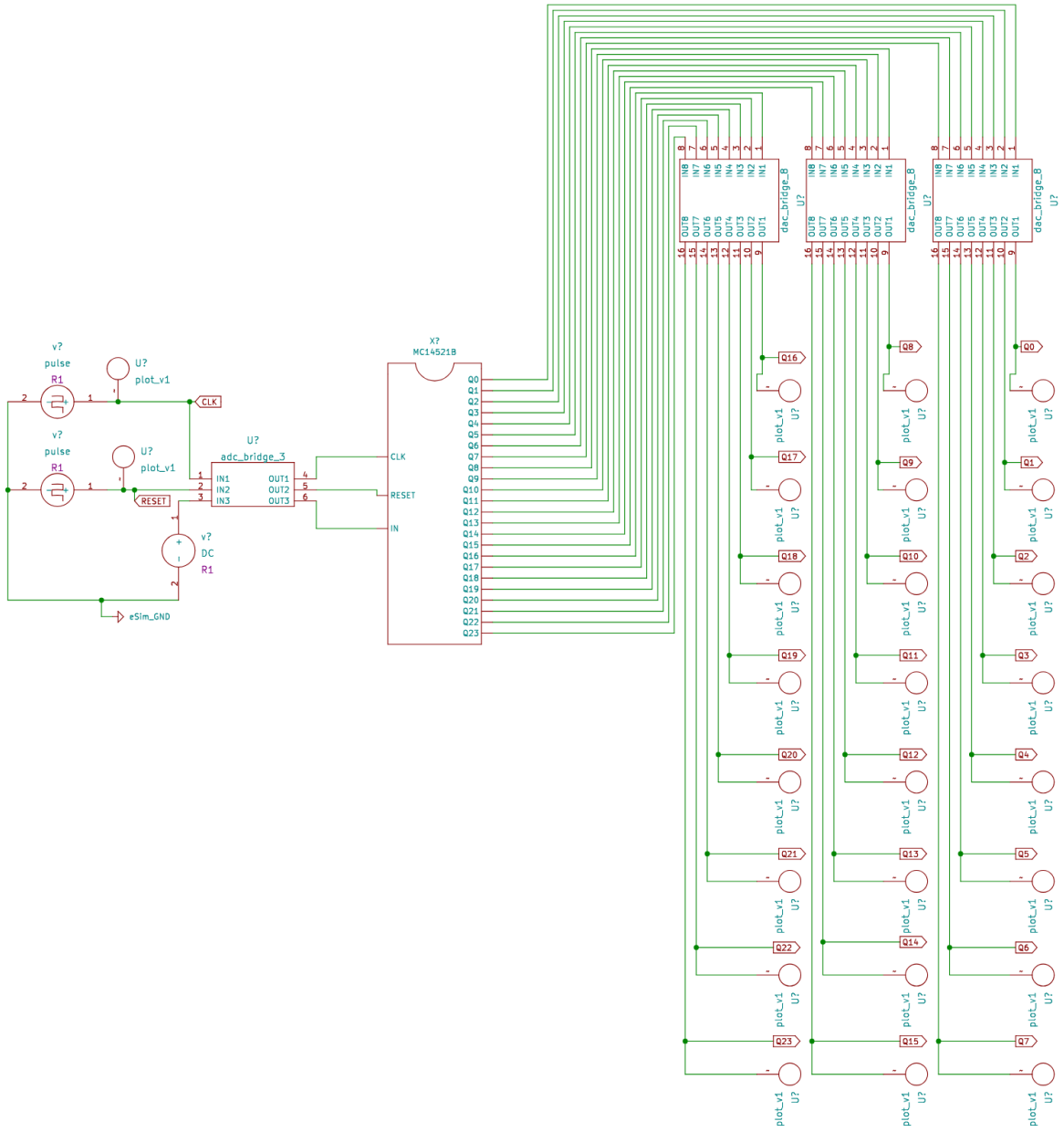

Figure 13.3: Test Circuit of the MC14521B

13.7 Output Plot

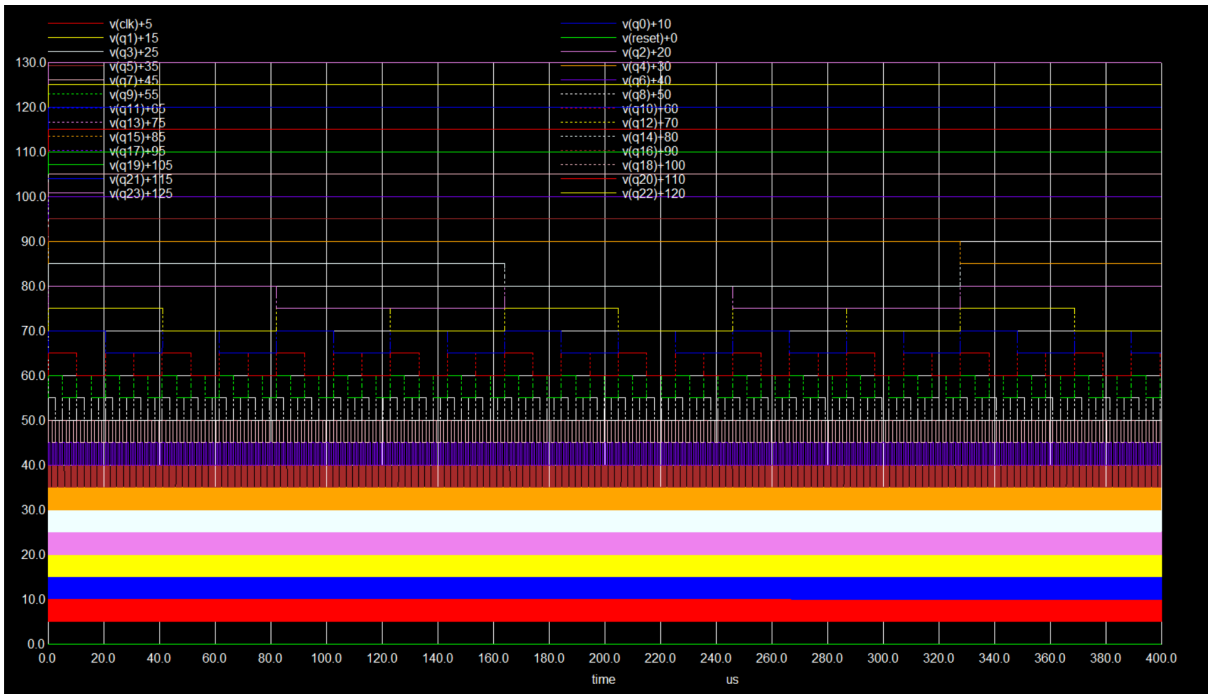

Figure 13.4: Input and Output signals of the MC14521B

Chapter 14

Conclusion and Future Scope

The project successfully fulfilled its objective of contributing a diverse set of accurately modeled digital logic ICs to the eSim subcircuit library. Each IC was implemented based on its official datasheet and rigorously tested through appropriate simulation testbenches to ensure its functional correctness and reliability. The contributions include a variety of fundamental digital components such as Adders, Encoders, Decoders, Multiplexers, Flip-Flops, Latches, Comparators, and Display Drivers.

These digital IC models serve as essential building blocks for designing and simulating complex digital systems, making them valuable resources for students, educators, and researchers using eSim. By integrating these verified models into the eSim library, the project has enhanced the platform's capability to support real-world digital logic design and experimentation.

This initiative not only reinforces the importance of open-source EDA tools in academic and research settings but also lays the groundwork for future developments. As the eSim device model library continues to grow, we anticipate a broader adoption among the engineering community and the creation of increasingly sophisticated circuits. The outcomes of this project thus represent a meaningful step forward in strengthening the ecosystem of accessible, open-source circuit simulation tools.

Chapter 15

Circuits Contribution

This chapter lists all the Integrated Circuits (ICs) contributed during the fellowship. Each IC has been carefully modeled and tested, and is now part of the eSim library. The contributions include both analog and digital ICs, covering a wide range of functionalities.

15.1 PRIYADHARSAN D – List of ICs

1. 74ALS640 – Octal Bus Transceiver with Inverted 3-State Outputs
2. SN74S274 – 4×4 Two's Complement Multiplier
3. TIBPAL20L8 – 20-Input, 8-Output Programmable Array Logic
4. SN74S134 – 12-Input NAND Gate with 3-State Output
5. MC14561B – 9's Complement Generator
6. Am2902 – 4-Bit Lookahead Carry Generator (Bit-Slice Support)
7. SN74LS25 – Dual 4-Input NOR Gate with Strobe
8. MC14530B – Dual 5-Input Majority Gate (Output HIGH if 3+ Inputs HIGH)
9. SN74S281 – ALU with Carry Lookahead
10. MC14521B – 24-Stage Frequency Divider

Bibliography

[1] FOSSEE Official Website, [Online]. Available: https://fossee.in. [Accessed: Jan. 20, 2026].

[2] eSim Official Website, [Online]. Available: https://esim.fossee.in/. [Accessed: Jan. 20, 2026].

[3] ALLDATASHEET, "74ALS640 Datasheet," [Online]. Available: https://www.alldatasheet.com/datasheet-pdf/view/50975/FAIRCHILD/DM74ALS640.html.

[4] ALLDATASHEET, "SN74S274 Datasheet," [Online]. Available: https://www.alldatasheet.com/datasheet-pdf/pdf/152942/TI/SN74S274.html.

[5] ALLDATASHEET, "TIBPAL20L8 Datasheet," [Online]. Available: https://www.alldatasheet.com/datasheet-pdf/pdf/28765/TI/TIBPAL20L8.html.

[6] ALLDATASHEET, "SN74S134 Datasheet," [Online]. Available: https://www.alldatasheet.com/datasheet-pdf/pdf/28155/TI/SN74S134.html.

[7] ALLDATASHEET, "MC14561B Datasheet," [Online]. Available: https://www.alldatasheet.com/html-pdf/898355/MOTOROLA/MC14561B/385/1/MC14561B.html.

[8] ALLDATASHEET, "Am2902 Datasheet," [Online]. Available: https://www.jameco.com/Jameco/Products/ProdDS/2303071.pdf?srsltid=AfmBOopi5C3fY8cdrl5zAYwxmeC-ozeWm5aBf9CSsOqX7H_xxNA_OUSn.

[9] ALLDATASHEET, "SN74LS25 Datasheet," [Online]. Available: https://www.circuits-diy.com/74ls25-nor-gate-ic-datasheet/.

[10] ALLDATASHEET, "MC14530B Datasheet," [Online]. Available: https://www.alldatasheet.com/datasheet-pdf/pdf/158409/MOTOROLA/MC14530B.html.

[11] ALLDATASHEET, "SN74S281 Datasheet," [Online]. Available: https://www.datasheetarchive.com/datasheet/SN74S281FN/Texas-Instruments?term=sn74s281.

[12] ALLDATASHEET, "MC14521B Datasheet," [Online]. Available: https://www.alldatasheet.com/datasheet-pdf/pdf/155722/MOTOROLA/MC14521B.html.