eSim Semester Long Internship

Spring 2026

On

Designing Integrated Circuits in eSim

Submitted by

Kaviya Dharshini G

Department of EE – VLSI
Chennai Institute of Technology

Under the guidance of

Prof.Prabhu Ramachandran
Principal Investigator
Department of Aerospace Engineering Indian Institute of Technology

February 2026

Acknowledgment

I would like to express my sincere gratitude to **Prof. Prabhu Ramachandran** for providing me the opportunity to be part of the FOSSEE internship programme and for supporting open-source engineering tool development at IIT Bombay.

I sincerely thank my mentor **Mr. Varad Patil** for his continuous support, technical guidance, and encouragement throughout this project.

I also thank **Sumanto Kar** and the entire FOSSEE team for their coordination and timely assistance at various stages of this work.

This internship has been an enriching experience, allowing me to work with open-source EDA tools, develop IC subcircuits in eSim, and gain exposure to real-world circuit modelling and simulation workflows.

Contents

Chapter 1

Introduction

1.1 FOSSEE

FOSSEE (Free/Libre and Open Source Software for Education) is an initiative based at IIT Bombay aimed at promoting the use of open-source software in education and research. It was established to reduce dependency on proprietary software and to encourage open-source alternatives. FOSSEE offers documentation, tutorials, workshops, and hands-on training to empower students, educators, and professionals.

1.2 eSim

eSim, created by the FOSSEE project at IIT Bombay, is a versatile open-source software tool for circuit design and simulation. It combines multiple open-source packages into one cohesive platform, making it easier to design, simulate, and analyse electronic circuits. eSim is particularly useful as an affordable alternative to proprietary EDA tools, and includes a subcircuit feature that enables complex hierarchical circuit design.

1.3 NgSpice

NgSpice is an open-source SPICE simulator for electric and electronic circuits. It simulates circuit elements such as JFETs, BJTs, MOSFETs, passive components (R, L, C), and diodes. Digital, analog, and mixed-signal circuits can all be simulated. Users input circuits as netlists, and the output consists of voltage and current waveforms or saved data files.

1.4 Makechip

Makechip is a platform for digital circuit design offering browser-based and desktop environments for coding, compiling, simulating, and debugging Verilog designs. eSim interfaces with Makechip via a Python-based application called *Makechip-App*.

Chapter 2

Features of eSim

The objective behind eSim is to provide an open-source EDA solution for electronics and electrical engineers. It supports schematic creation, PCB design, and circuit simulation (analog, digital, and mixed-signal). Key features include:

1. **Schematic Creation:** An easy-to-use graphical interface for drawing circuit schematics with drag-and-drop components.
2. **Circuit Simulation:** Supports SPICE-based transient, AC, and DC analysis with an integrated waveform viewer.
3. **PCB Design:** A PCB layout editor with DRC (Design Rule Check) and Gerber file export.
4. **Subcircuit Feature:** Enables modular and hierarchical design by integrating reusable subcircuits.
5. **Open Source Integration:** Integrates KiCad, NgSpice, and GHDL for a comprehensive, free EDA suite.

Chapter 3

Problem Statement

To design and develop various analog and digital integrated circuit models in the form of sub-circuits using device model files already present in the eSim library. These IC models should be useful for future circuit design purposes by developers and users once they are successfully integrated into the eSim sub-circuit library.

3.1 Approach

The approach involved a systematic process leveraging datasheets from leading IC manufacturers such as Texas Instruments, NXP Semiconductors, and Intersil.

1. **Analysing Datasheets:** In-depth review of datasheets to identify ICs suitable for eSim, including scrutinising schematics, component values, and truth tables.
2. **Subcircuit Creation:** Modelling selected ICs as sub-circuits within eSim using available device model files, and creating accurate symbol and pin diagrams per the datasheet.
3. **Test Circuit Design:** Designing test circuits based on datasheets to verify the functionality of each sub-circuit.
4. **Schematic Testing:** Running simulations, generating waveforms, and iterating until outputs matched expected results.

Chapter 4

74LS125

4.1 General Description

The 74LS125 is a quad bus buffer gate with tri-state outputs from the LS (Low-power Schottky) TTL family. Each of the four independent buffers features an active-LOW output-enable (OE) input; when OE is HIGH the output is placed in a high-impedance state, effectively disconnecting the buffer from the bus.

4.2 Key Features

- Quad bus buffer with tri-state outputs
- Active-LOW output-enable (OE) per buffer
- Standard TTL voltage levels (4.75 V – 5.25 V)
- High-impedance output state for bus control
- TTL-compatible inputs and outputs

4.3 Applications

- Data bus buffering and isolation
- Bidirectional bus control
- Memory address/data bus driving
- Output expansion in microprocessor systems

4.4 Subcircuit Symbol

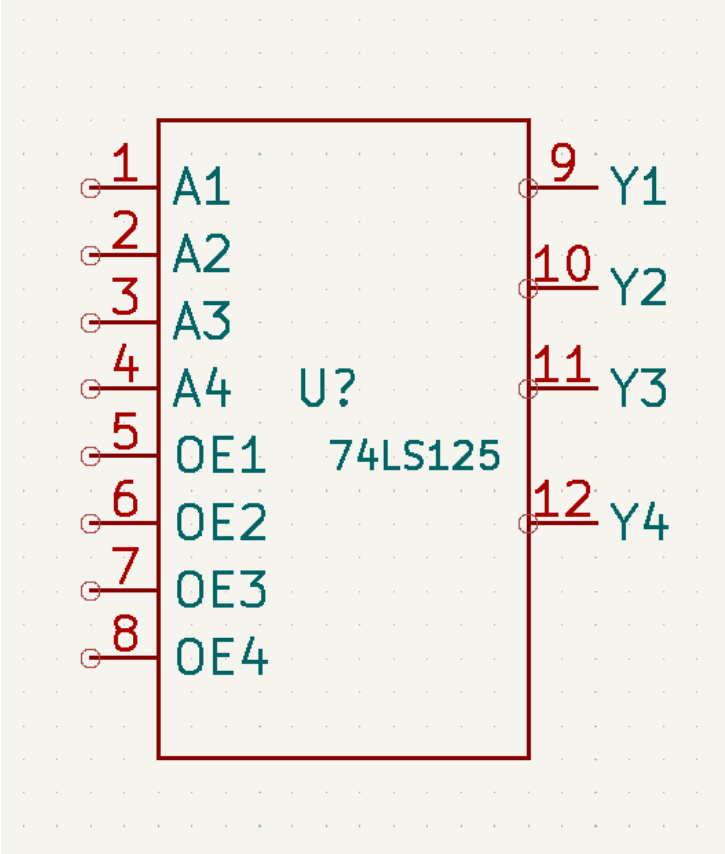

Figure 4.1: Subcircuit Symbol of the 74LS125

4.5 Subcircuit Schematic Diagram

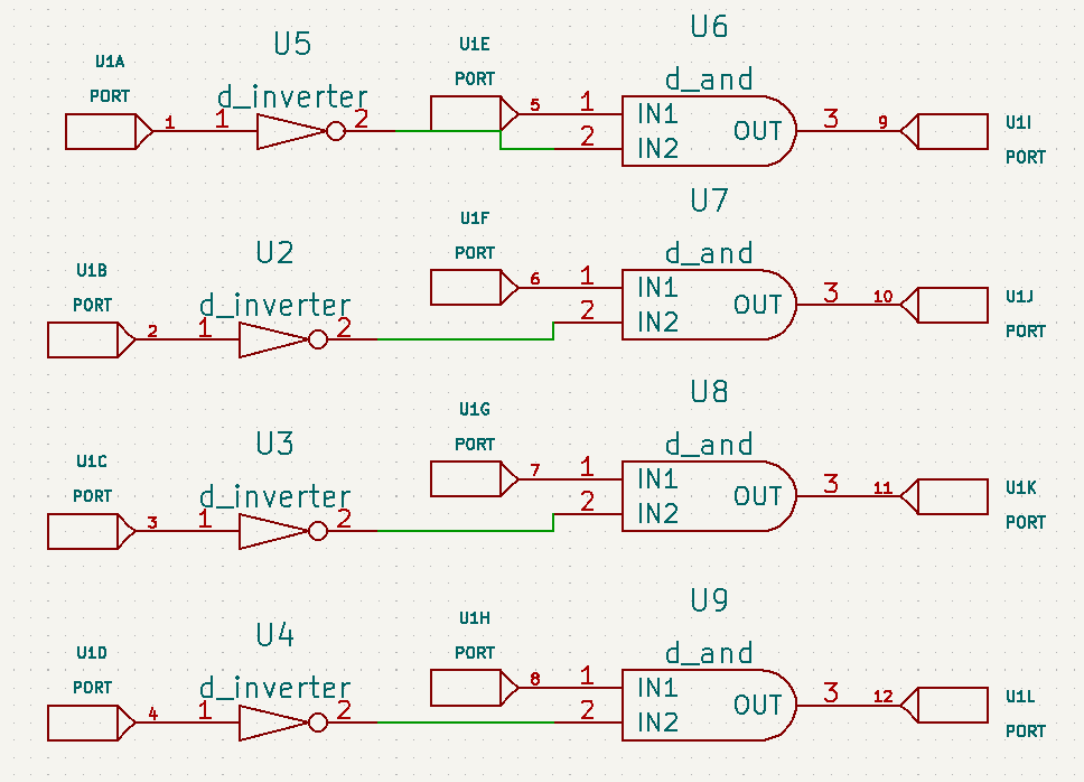

Figure 4.2: Subcircuit Schematic of the 74LS125

4.6 Test Circuit

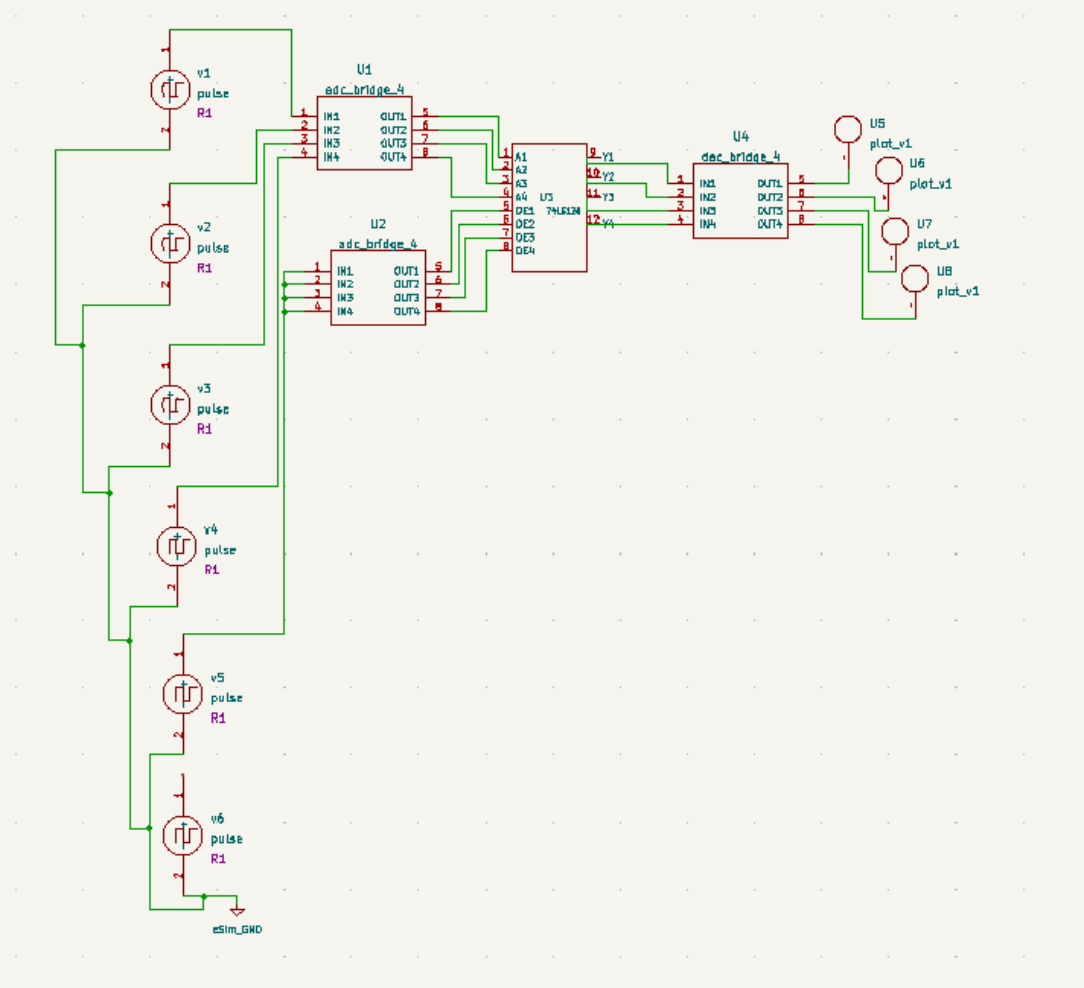

Figure 4.3: Test Circuit of the 74LS125

4.7 Function Table

$$Y = A$$

Inputs		Output
A	C	Y
L	L	L
H	L	H
X	H	Hi-Z

Figure 4.4: Function Table of the 74LS125

4.8 Output Plot

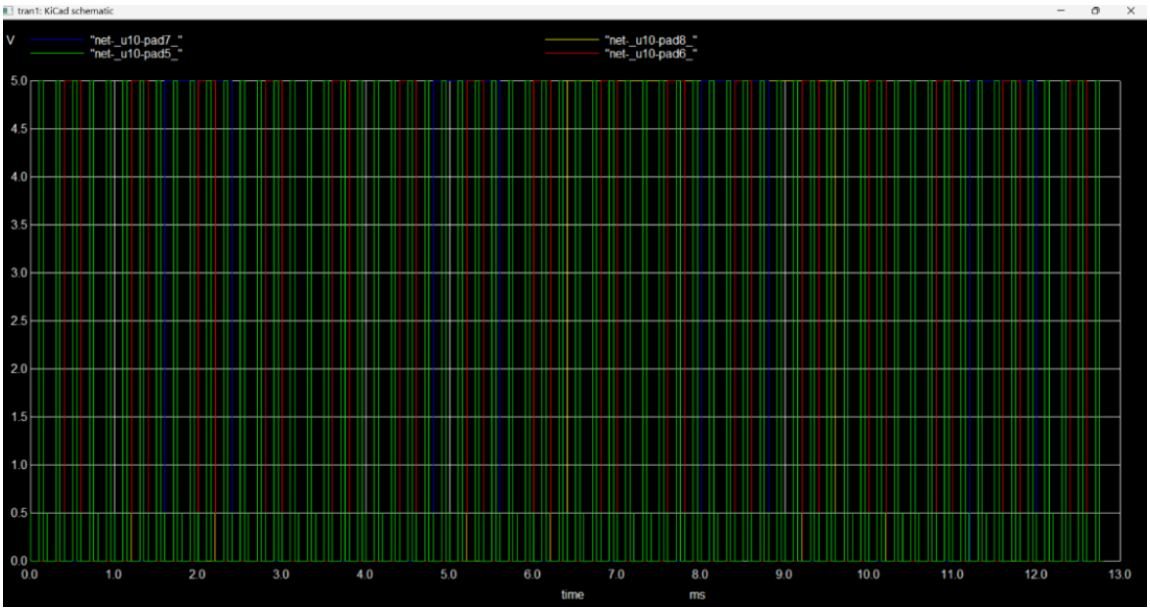

Figure 4.5: Output of the 74LS125

Chapter 5

74LS165

5.1 General Description

The 74LS165 is an 8-bit parallel-in / serial-out shift register from the LS TTL family. Data is loaded in parallel on a LOW-to-HIGH transition of the shift/load input, then shifted out serially on each clock pulse. It is widely used in serial communication and data conversion applications.

5.2 Key Features

- 8-bit parallel-in, serial-out shift register
- Parallel load on LOW-to-HIGH shift/load transition
- Complementary serial outputs (Q_H and $\overline{Q_H}$)
- Clock inhibit input for gated operation
- Standard TTL voltage operation

5.3 Applications

- Serial data transmission
- Parallel-to-serial data conversion
- Keyboard scanning
- Data acquisition systems

5.4 Subcircuit Symbol

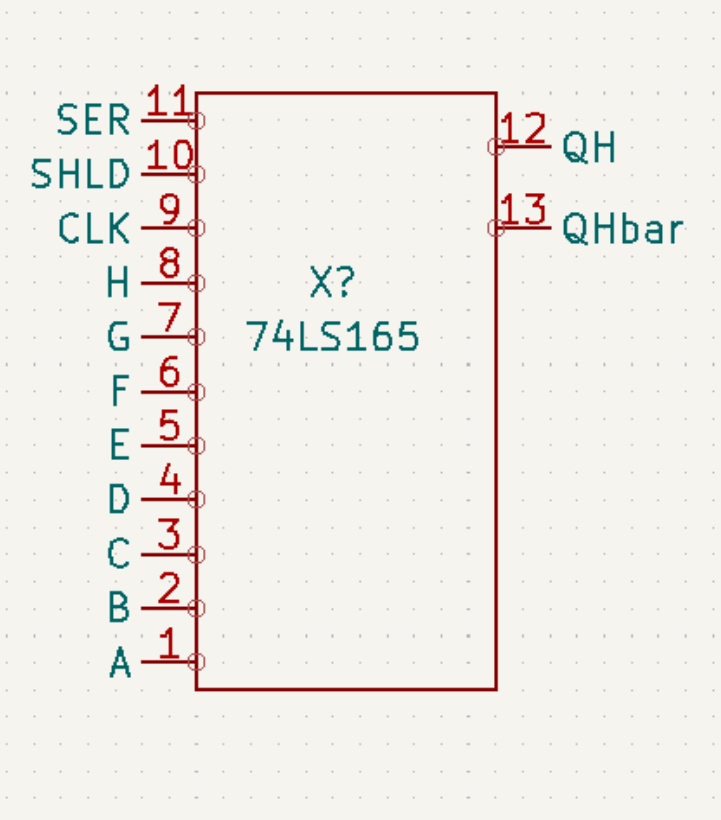

Figure 5.1: Subcircuit Symbol of the 74LS165

5.5 Subcircuit Schematic Diagram

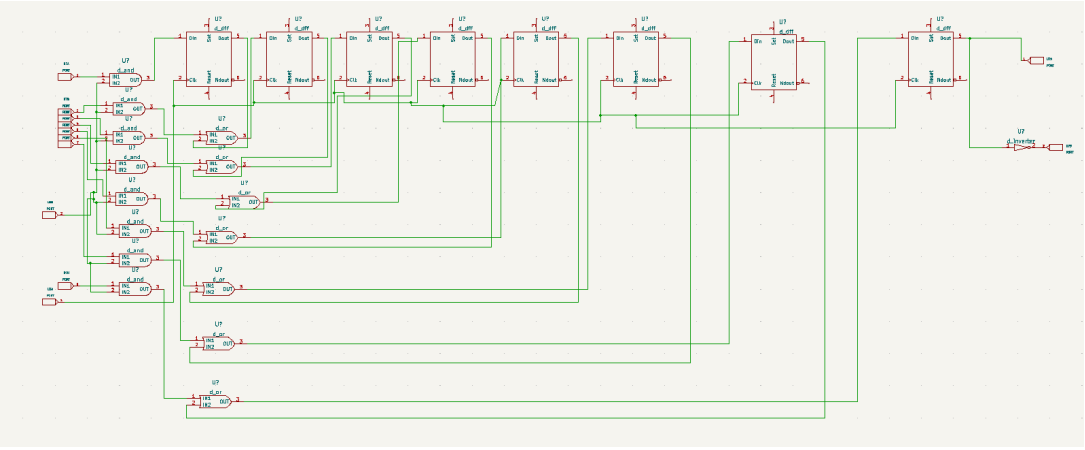

Figure 5.2: Subcircuit Schematic of the 74LS165

5.6 Test Circuit

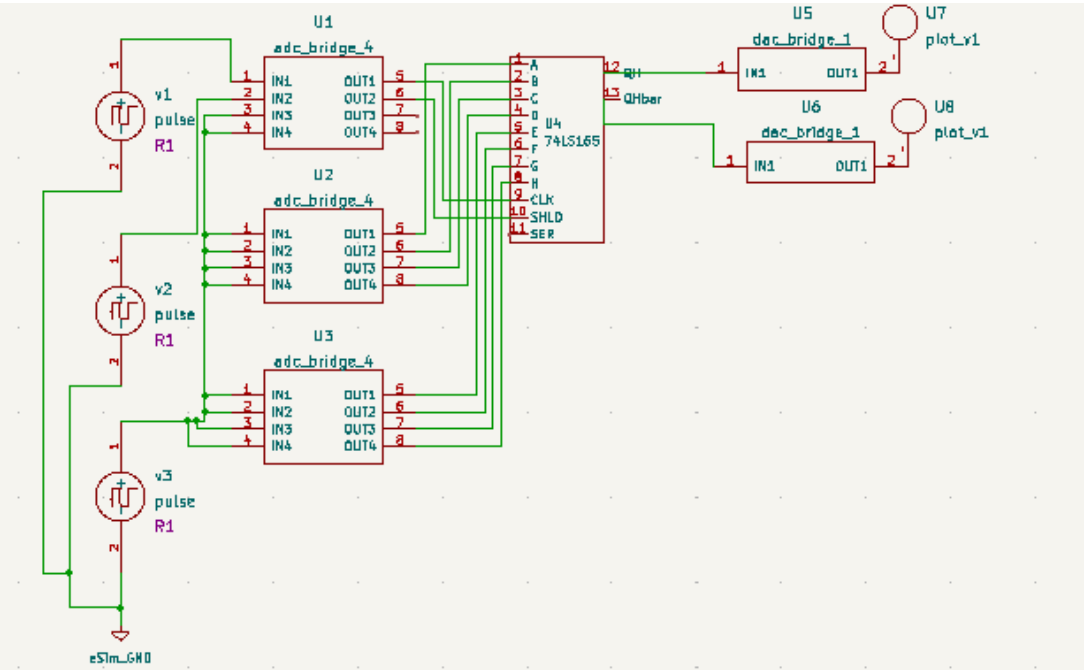

Figure 5.3: Test Circuit of the 74LS165

5.7 Function Table

Inputs					Internal Outputs		Output
Shift/ Load	Clock Inhibit	Clock	Serial	Parallel A...H	Q_A	Q_B	Q_H
L	X	X	X	a...h	a	b	h
H	L	L	X	X	Q_{A0}	Q_{B0}	Q_{H0}
H	L	↑	H	X	H	Q_{An}	Q_{Gn}
H	L	↑	L	X	L	Q_{An}	Q_{Gn}
H	H	X	X	X	Q_{A0}	Q_{B0}	Q_{H0}

Figure 5.4: Function Table of the 74LS165

5.8 Output Plot

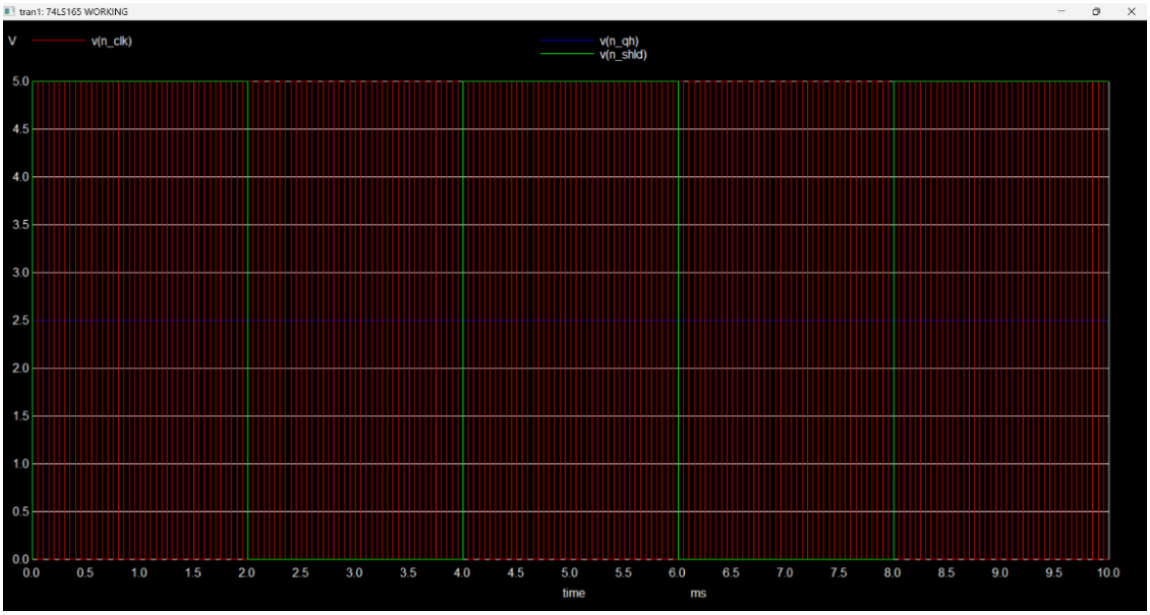

Figure 5.5: Output of the 74LS165

Chapter 6

CD4051

6.1 General Description

The CD4051 is a single 8-channel analog multiplexer / demultiplexer from the CMOS 4000-series family. Three binary select inputs choose one of eight independent channels to connect to the common I/O pin. It operates over a wide supply range (3 V to 18 V) and handles both digital and analog signals.

6.2 Key Features

- Single 8-channel analog multiplexer/demultiplexer
- Wide supply voltage range: 3 V – 18 V
- Low ON resistance ($\approx$80 Ω at $V_{DD} = 15$ V)
- Active-LOW inhibit input
- Handles rail-to-rail analog signals

6.3 Applications

- Analog signal routing and switching
- Data acquisition systems
- Sample-and-hold circuits
- Audio channel selection

6.4 Subcircuit Symbol

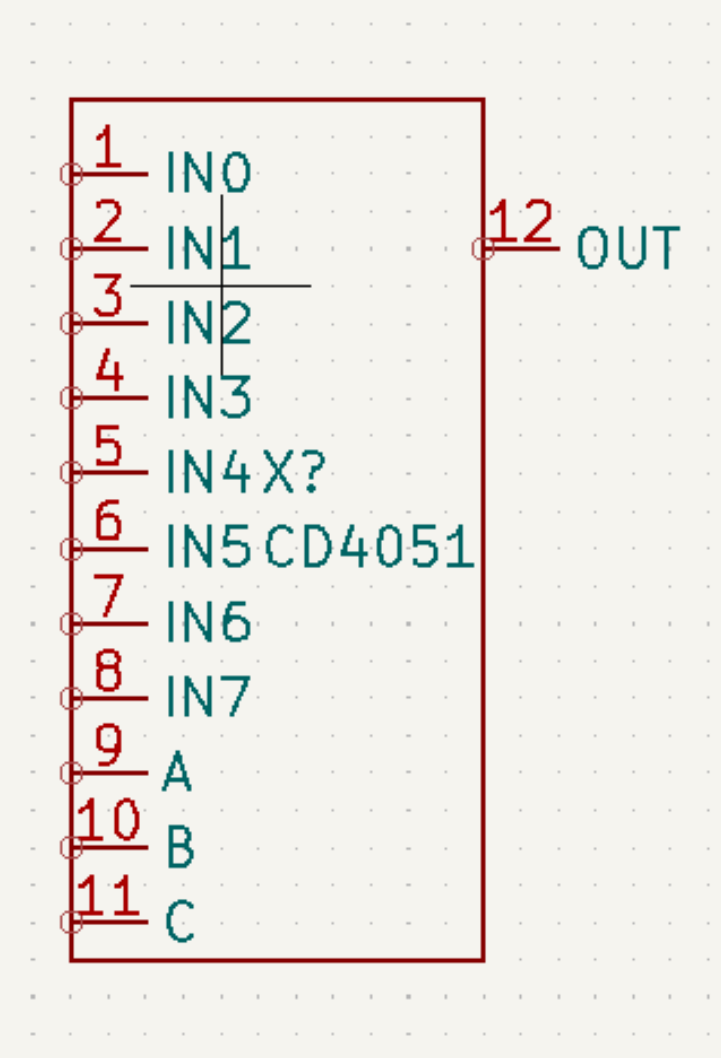

Figure 6.1: Subcircuit Symbol of the CD4051

6.5 Subcircuit Schematic Diagram

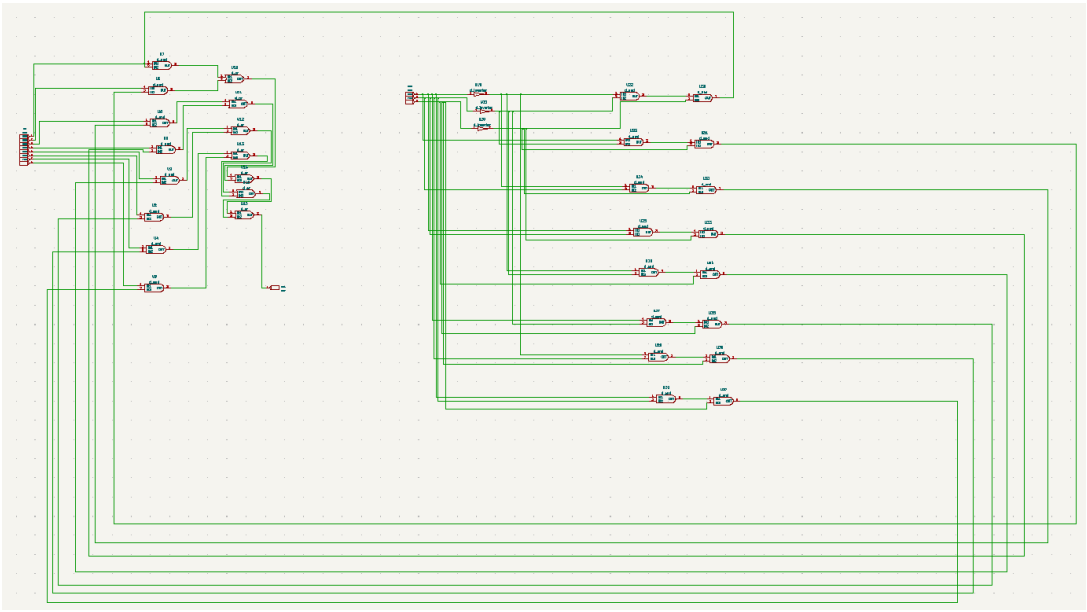

Figure 6.2: Subcircuit Schematic of the CD4051

6.6 Test Circuit

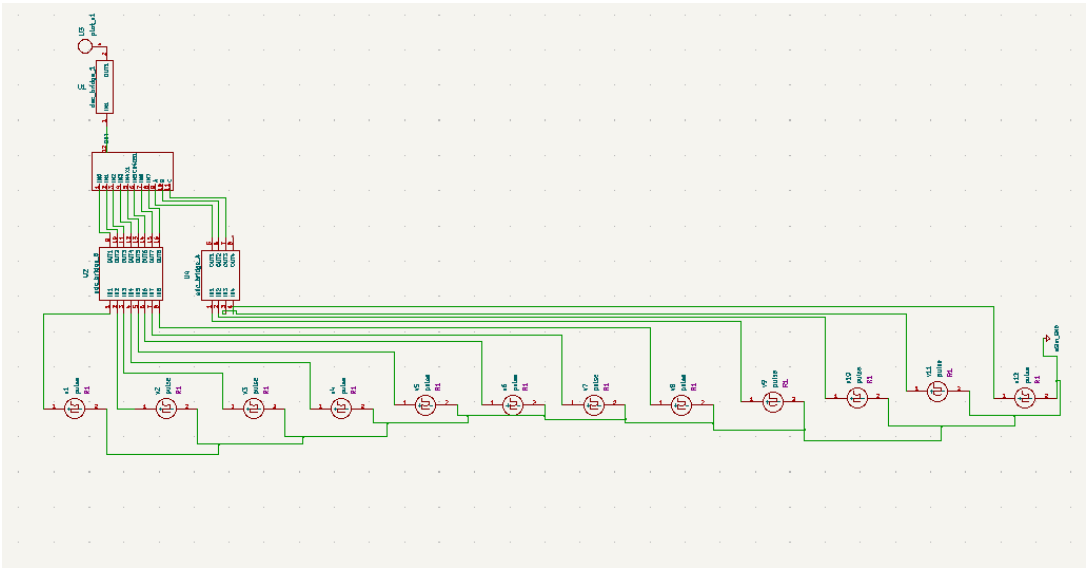

Figure 6.3: Test Circuit of the CD4051

6.7 Function Table

Input (*A, B, C, D*)	Output (True)	Output (Complement)
Low (0)	Low (0)	High (1)
High (1)	High (1)	Low (0)

Figure 6.4: Function Table of the CD4051

6.8 Output Plot

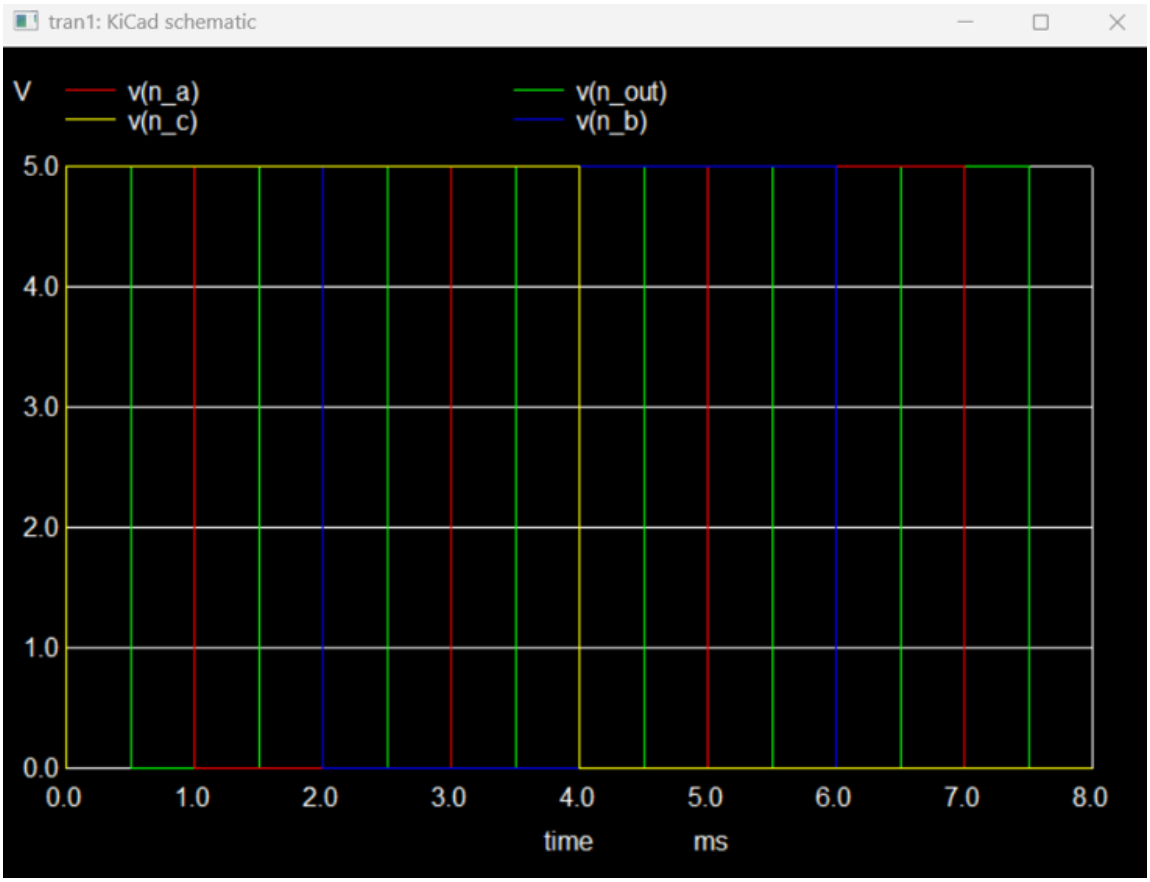

Figure 6.5: Output of the CD4051

Chapter 7

74LS123

7.1 General Description

The 74LS123 is a dual retriggerable monostable multivibrator (one-shot) from the LS TTL family. Each half has active-LOW and active-HIGH trigger inputs, a direct clear input, and complementary Q and $\overline{Q}$ outputs. The output pulse width is set externally by a resistor and capacitor.

7.2 Key Features

- Dual retriggerable monostable multivibrator
- Triggerable from either positive or negative edge
- Direct reset (clear) input
- Pulse width set by external R and C
- Standard TTL voltage operation

7.3 Applications

- Pulse width generation and stretching
- Missing pulse detection
- Debouncing mechanical switches
- Timing and delay circuits

7.4 Subcircuit Symbol

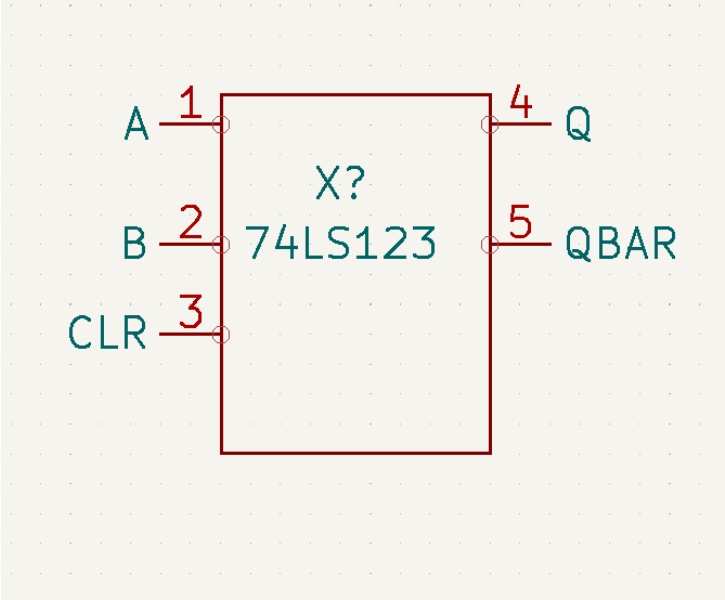

Figure 7.1: Subcircuit Symbol of the 74LS123

7.5 Subcircuit Schematic Diagram

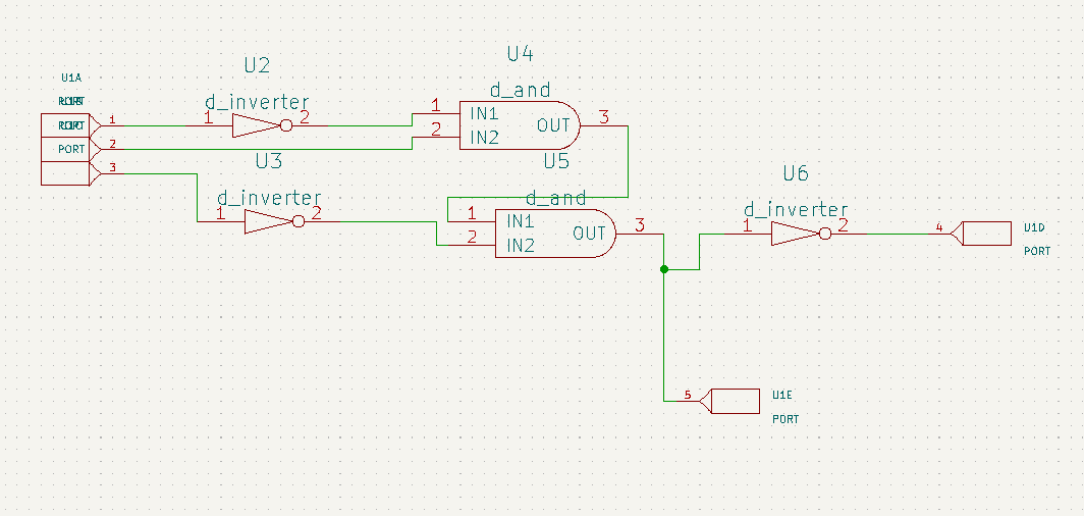

Figure 7.2: Subcircuit Schematic of the 74LS123

7.6 Test Circuit

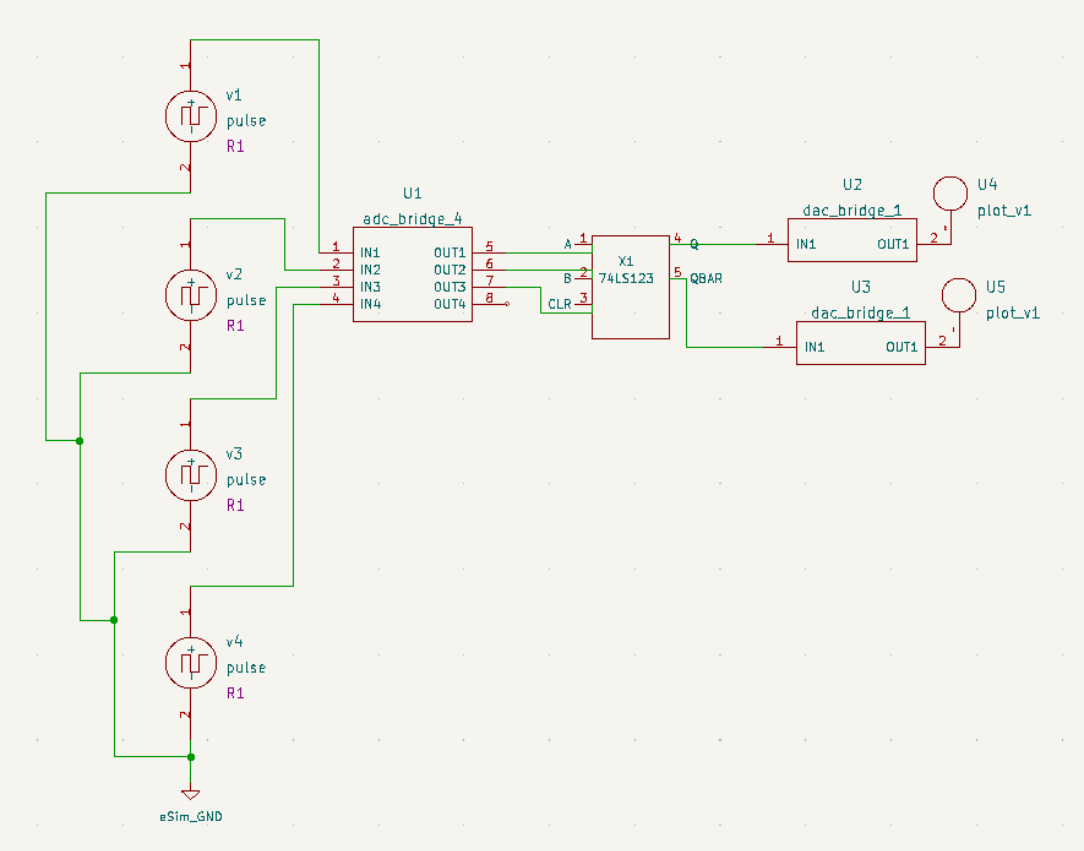

Figure 7.3: Test Circuit of the 74LS123

7.7 Function Table

Inputs			Outputs	
CLEAR	A	B	Q	$\overline{Q}$
L	X	X	L	H
X	H	X	L	H
X	X	L	L	H
H	L	↑	⊓	⊔
H	↓	H	⊓	⊔
↑	L	H	⊓	⊔

Figure 7.4: Function Table of the 74LS123

7.8 Output Plot

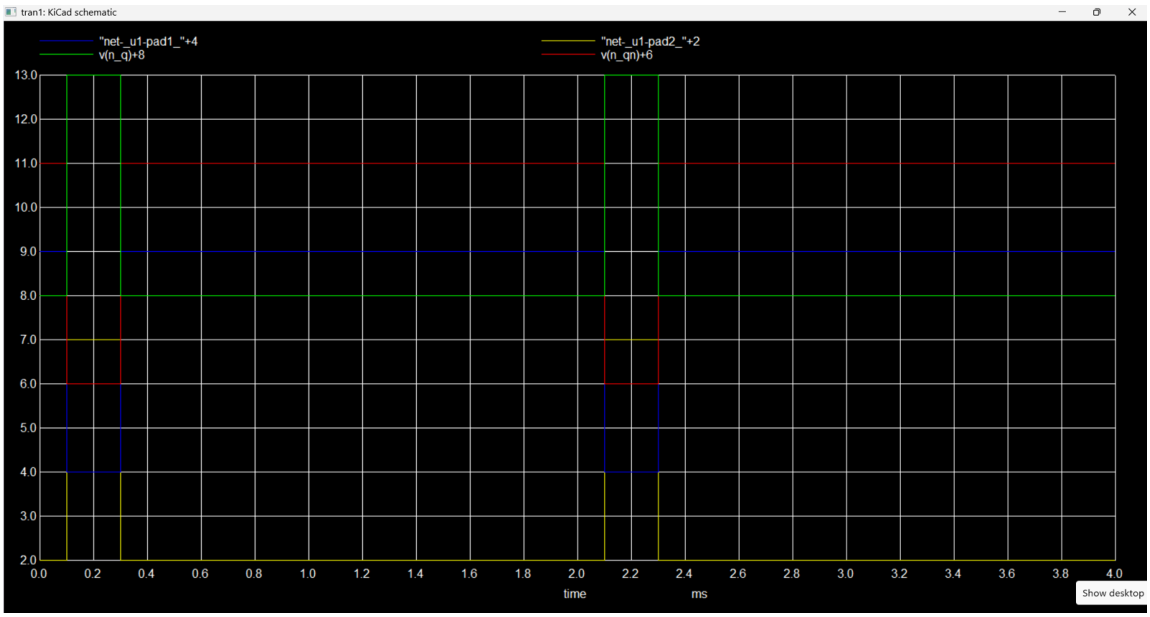

Figure 7.5: Output of the 74LS123

Chapter 8

74LS161

8.1 General Description

The 74LS161 is a synchronous 4-bit binary counter with synchronous clear from the LS TTL family. It features synchronous parallel load, two active-HIGH count-enable inputs (P and T), a ripple carry output (RCO) for cascading, and a synchronous clear input. The counter increments on the rising clock edge.

8.2 Key Features

- Synchronous 4-bit binary counter
- Synchronous parallel load
- Synchronous clear (active LOW)
- Ripple carry output (RCO) for cascading
- Standard TTL voltage operation

8.3 Applications

- Frequency division and counting
- Digital timing and sequencing
- Address generation in memory systems
- Modulo-N counters using feedback

8.4 Subcircuit Symbol

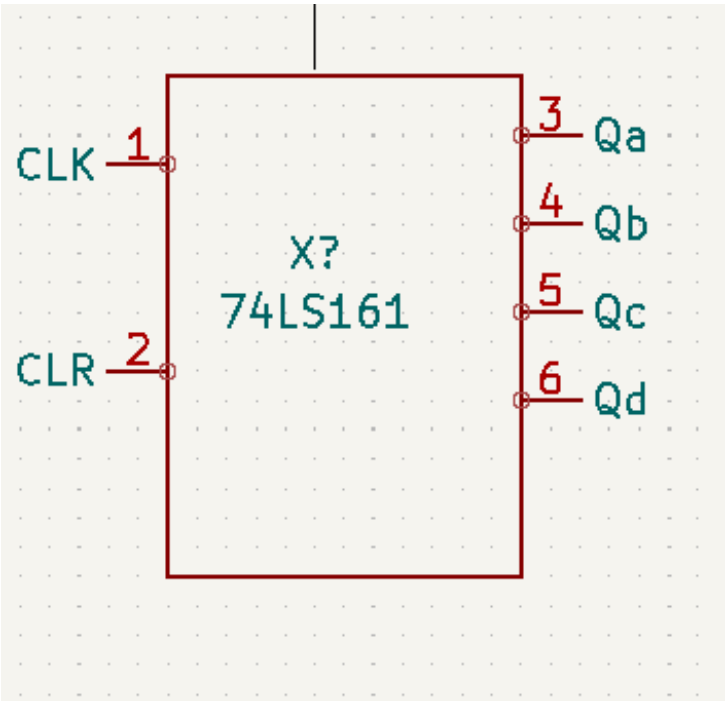

Figure 8.1: Subcircuit Symbol of the 74LS161

8.5 Subcircuit Schematic Diagram

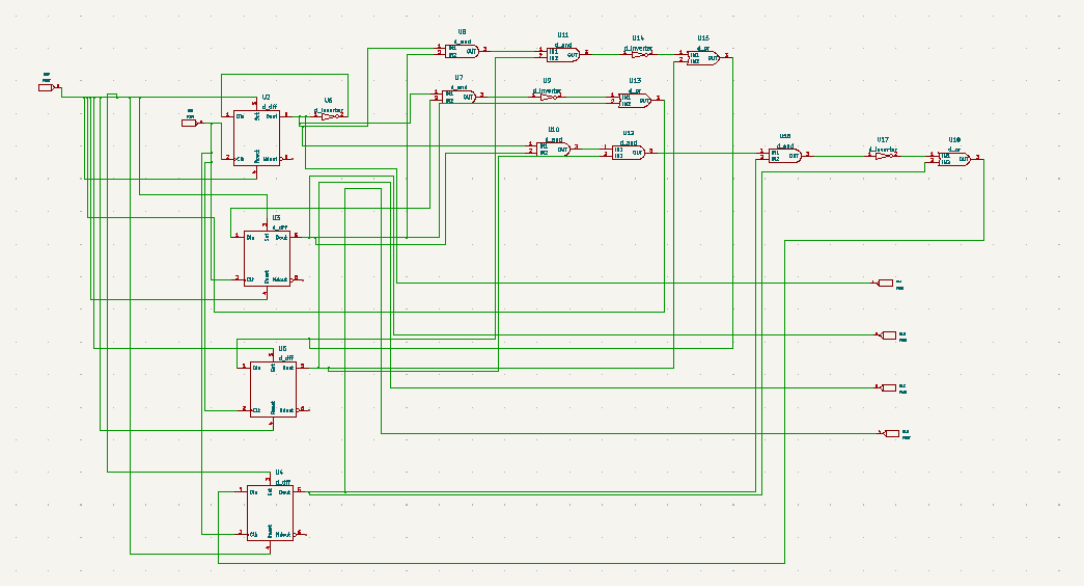

Figure 8.2: Subcircuit Schematic of the 74LS161

8.6 Test Circuit

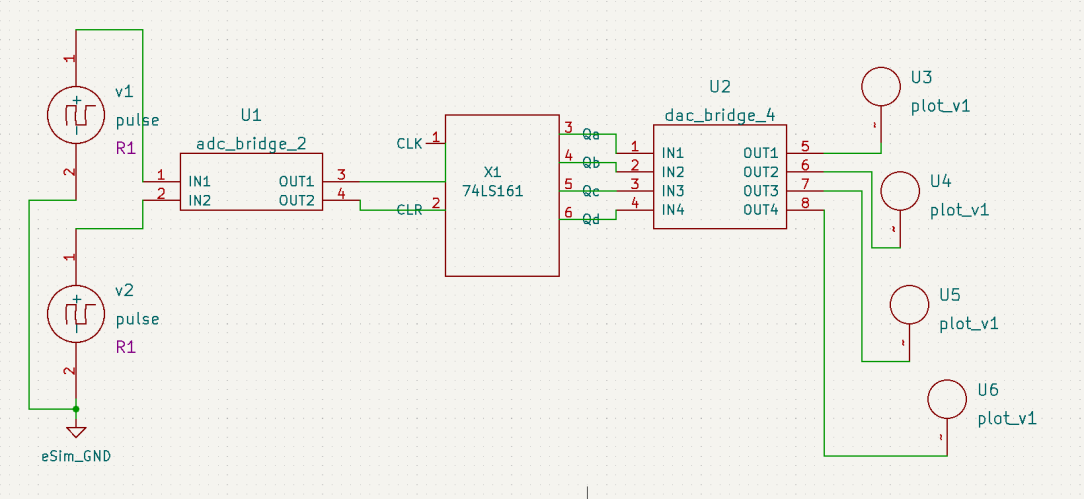

Figure 8.3: Test Circuit of the 74LS161

8.7 Function Table

Input									Output			
CP	$\overline{CR}$	$\overline{LD}$	P	T	D_3	D_2	D_1	D_0	Q_3	Q_2	Q_1	Q_0
×	0	×	×	×	×	×	×	×	0	0	0	0
↑	1	0	×	×	d	c	b	a	d	c	b	a
×	1	1	0	×	×	×	×	×	Retain			
×	1	1	×	0	×	×	×	×	Retain (C=0)			
↑	1	1	1	1	×	×	×	×	Count			

Figure 8.4: Function Table of the 74LS161

8.8 Output Plot

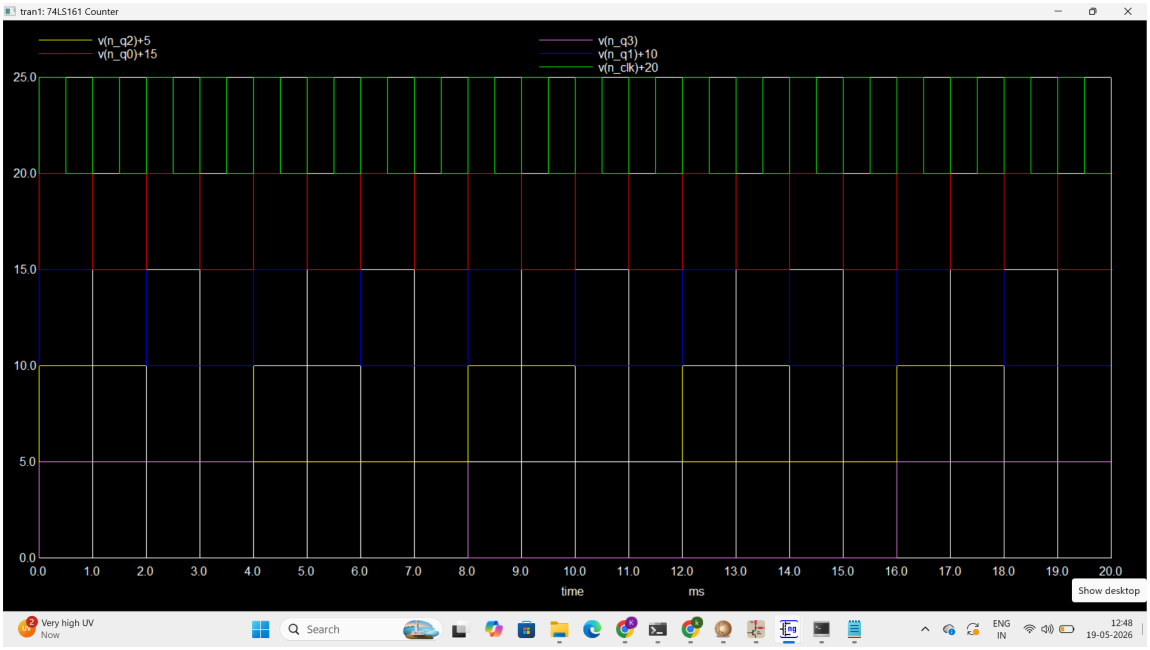

Figure 8.5: Output of the 74LS161

Chapter 9

CD4046

9.1 General Description

The CD4046 is a CMOS Phase-Locked Loop (PLL) IC consisting of a low-power linear voltage-controlled oscillator (VCO) and two phase comparators. Phase Comparator I is an XOR gate; Phase Comparator II is an edge-triggered flip-flop type. It is widely used for frequency synthesis, FM demodulation, and clock recovery.

9.2 Key Features

- CMOS phase-locked loop with VCO
- Two phase comparators (XOR and edge-triggered)
- Wide VCO frequency range (up to 1.4 MHz at $V_{DD} = 10\,\text{V}$)
- Wide supply range: 3 V – 18 V
- Source follower output for demodulated signal

9.3 Applications

- Frequency synthesis and multiplication
- FM demodulation
- Clock recovery and synchronisation
- Motor speed control

9.4 Subcircuit Symbol

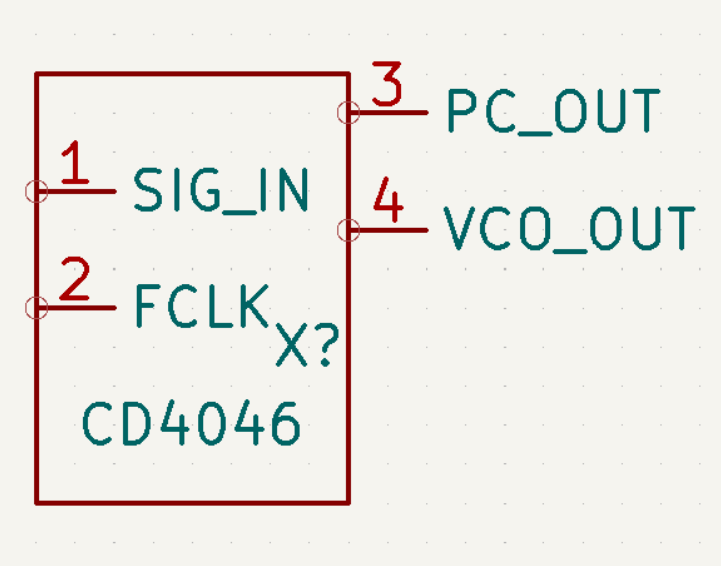

Figure 9.1: Subcircuit Symbol of the CD4046

9.5 Subcircuit Schematic Diagram

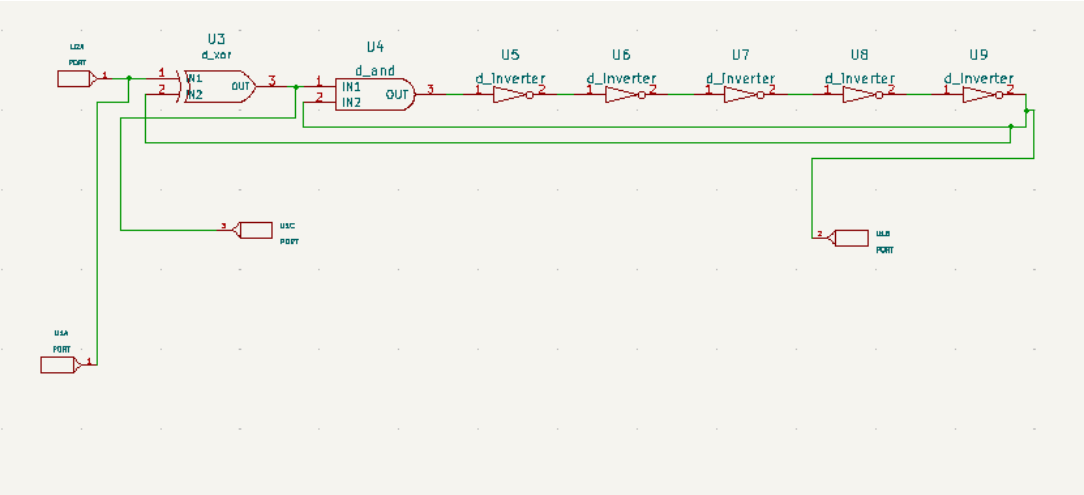

Figure 9.2: Subcircuit Schematic of the CD4046

9.6 Test Circuit

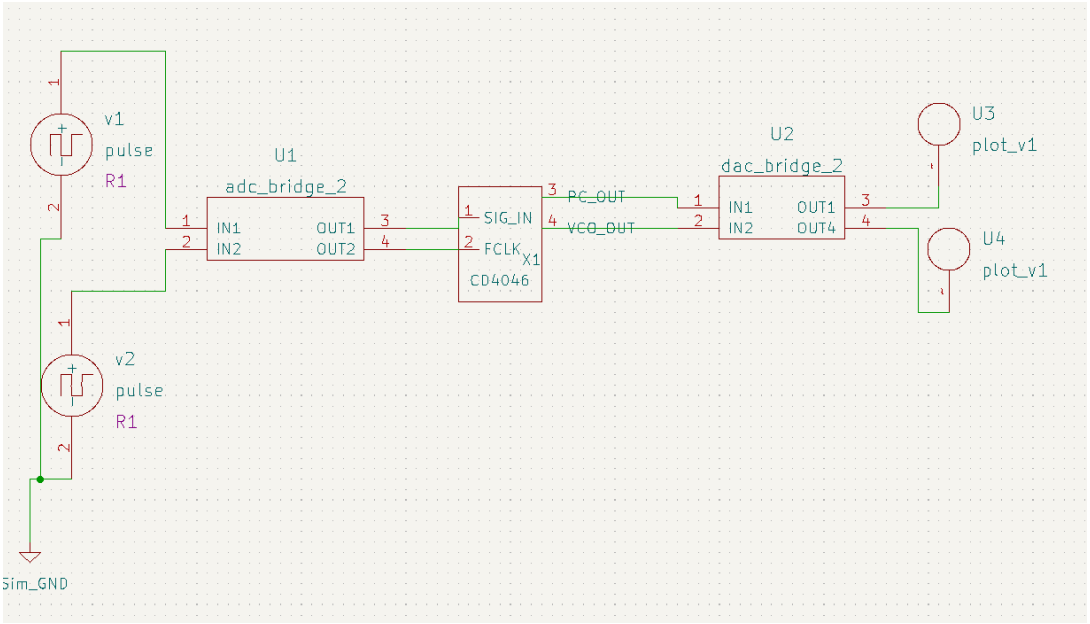

Figure 9.3: Test Circuit of the CD4046

9.7 Function Table

C1 (25V)	Frequency Range
1µF	0 – 100Hz
0.1µF	10Hz – 1kHz
0.01µF	100Hz – 10kHz

Figure 9.4: Function Table of the CD4046

9.8 Output Plot

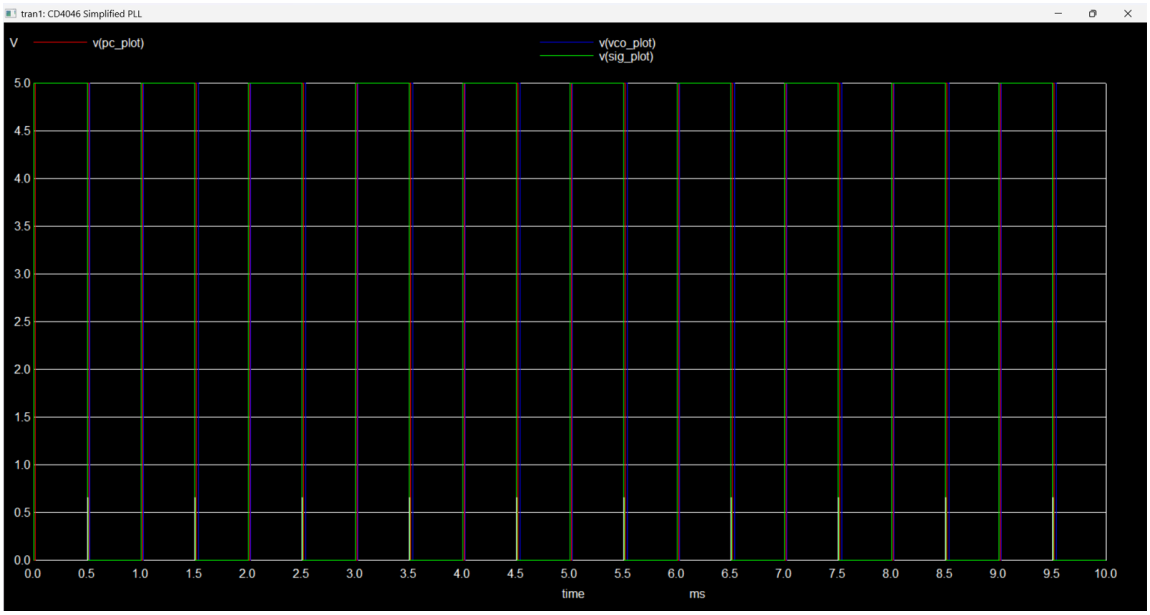

Figure 9.5: Output of the CD4046

Chapter 10

SN7497

10.1 General Description

The SN7497 is a synchronous 6-bit binary rate multiplier from the TTL logic family. It multiplies a clock frequency by a binary fraction set on its six input lines, producing an output pulse rate proportional to the programmed value. It operates from a standard 5 V TTL supply and is used in digital frequency synthesis applications.

10.2 Key Features

- 6-bit synchronous binary rate multiplier
- Synchronous clear and cascade inputs
- Standard TTL voltage operation (4.75 V – 5.25 V)
- Unity/cascade output for cascading multiple devices
- Output enable (Z input) control

10.3 Applications

- Digital frequency synthesis
- Pulse rate generation
- Arithmetic operations in digital systems
- Cascadable rate multiplication

10.4 Subcircuit Symbol

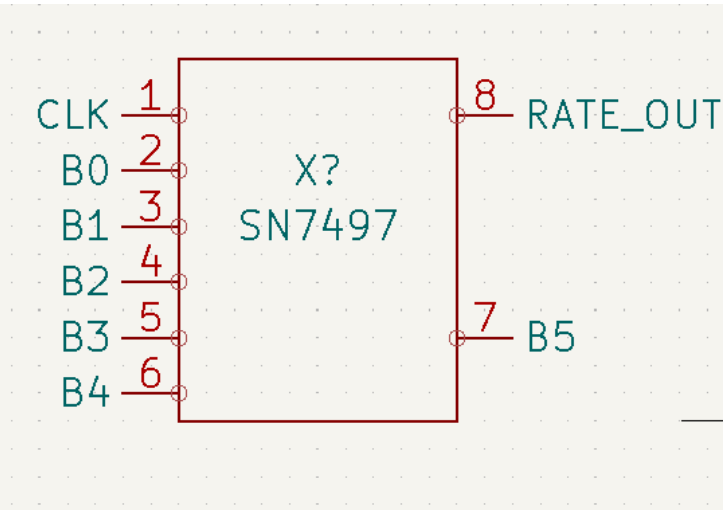

Figure 10.1: Subcircuit Symbol of the SN7497

10.5 Subcircuit Schematic Diagram

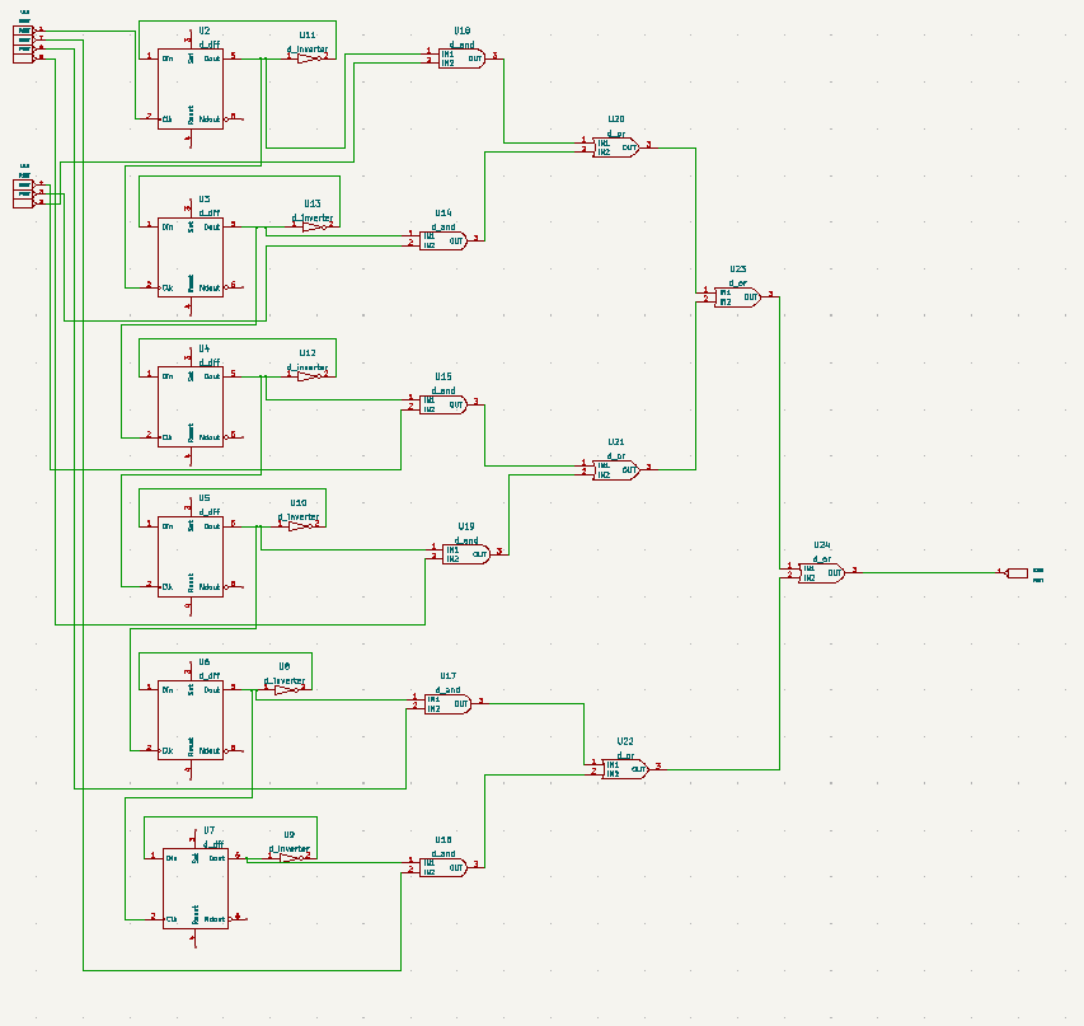

Figure 10.2: Subcircuit Schematic of the SN7497

10.6 Test Circuit

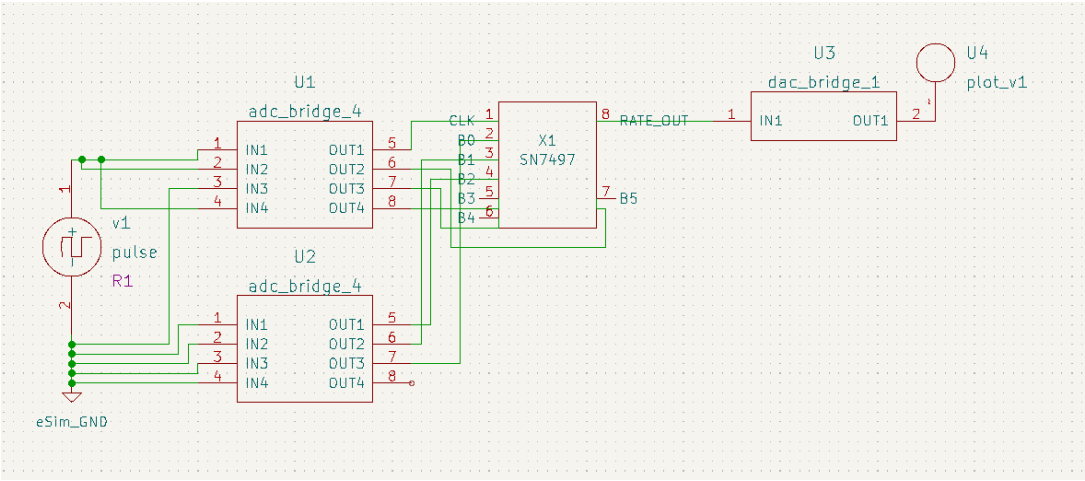

Figure 10.3: Test Circuit of the SN7497

10.7 Function Table

SELECT INPUTS		DATA INPUTS				STROBE	OUTPUT
B	A	C0	C1	C2	C3	$\bar{G}$	Y
X	X	X	X	X	X	H	L
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
L	H	X	L	X	X	L	L
L	H	X	H	X	X	L	H
H	L	X	X	L	X	L	L
H	L	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

Figure 10.4: Function Table of the SN7497

10.8 Output Plot

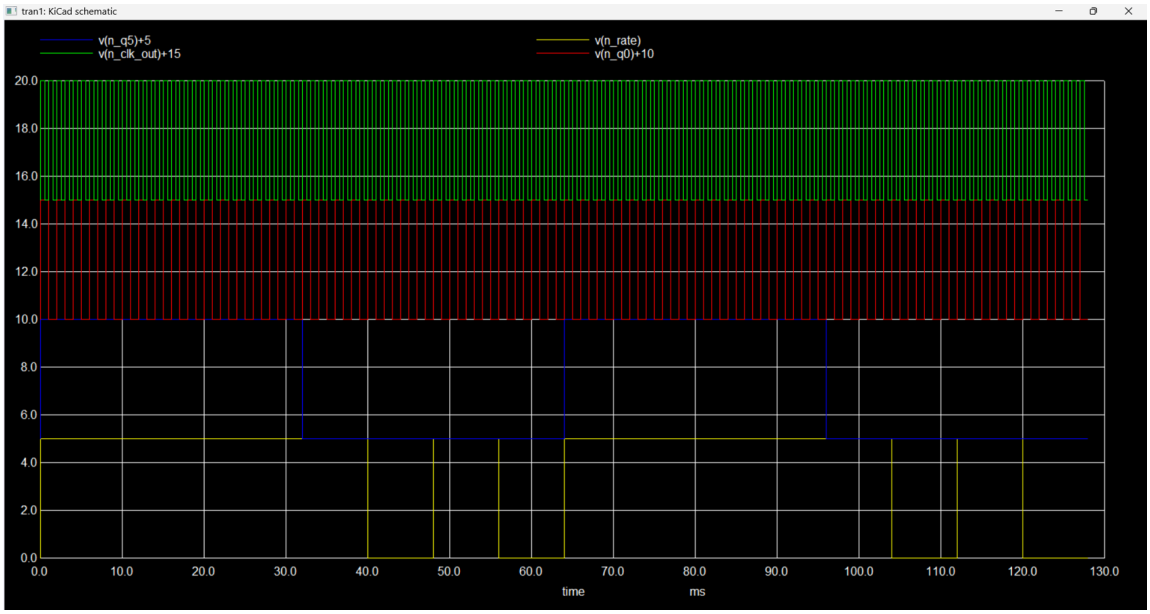

Figure 10.5: Output of the SN7497

Chapter 11

SN74121

11.1 General Description

The SN74121 is a monostable multivibrator (one-shot) with Schmitt-trigger inputs from the TTL logic family. It features complementary Q and $\overline{Q}$ outputs, an internal timing resistor (2 kΩ), and the ability to use an external resistor/capacitor to set pulse widths from 30 ns to 28 s. The Schmitt-trigger inputs provide noise immunity for slowly changing signals.

11.2 Key Features

- Monostable multivibrator with Schmitt-trigger inputs
- Internal 2 kΩ timing resistor
- External R/C for pulse widths from 30 ns to 28 s
- Complementary Q and $\overline{Q}$ outputs
- Standard TTL voltage operation

11.3 Applications

- Pulse width generation
- Signal delay and stretching
- Debouncing noisy input signals
- Missing pulse detection

11.4 Subcircuit Symbol

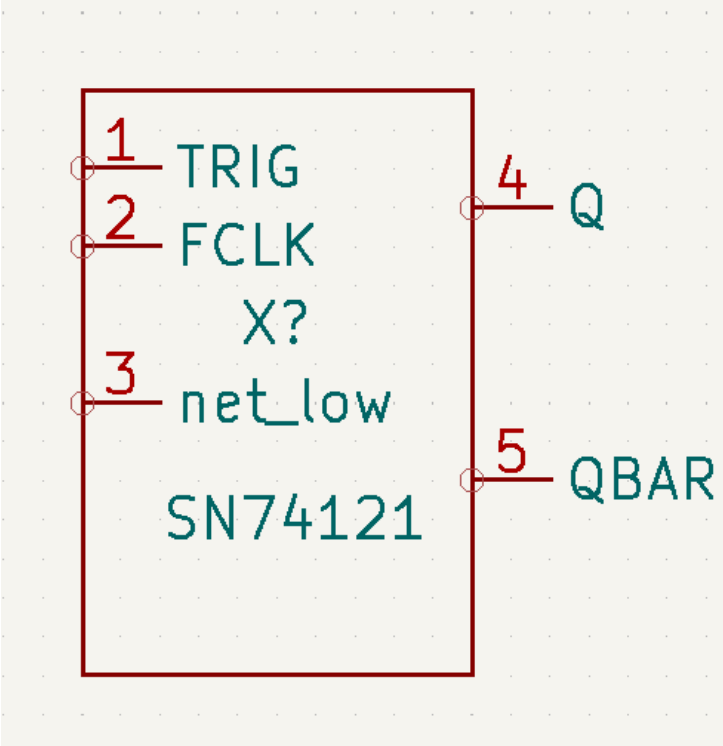

Figure 11.1: Subcircuit Symbol of the SN74121

11.5 Subcircuit Schematic Diagram

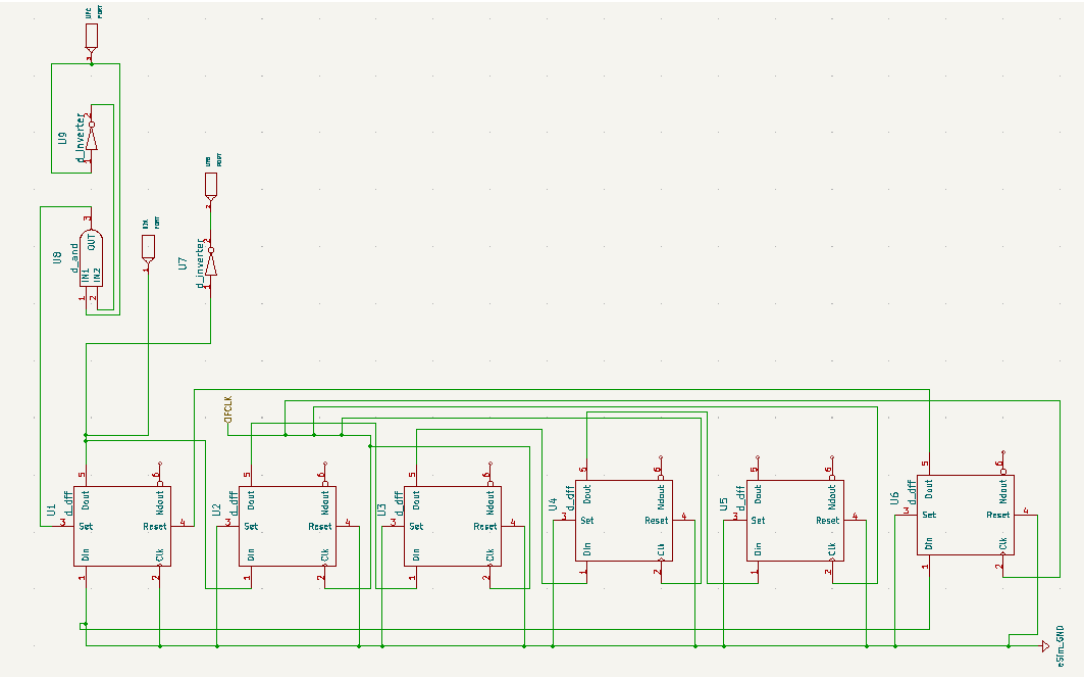

Figure 11.2: Subcircuit Schematic of the SN74121

11.6 Test Circuit

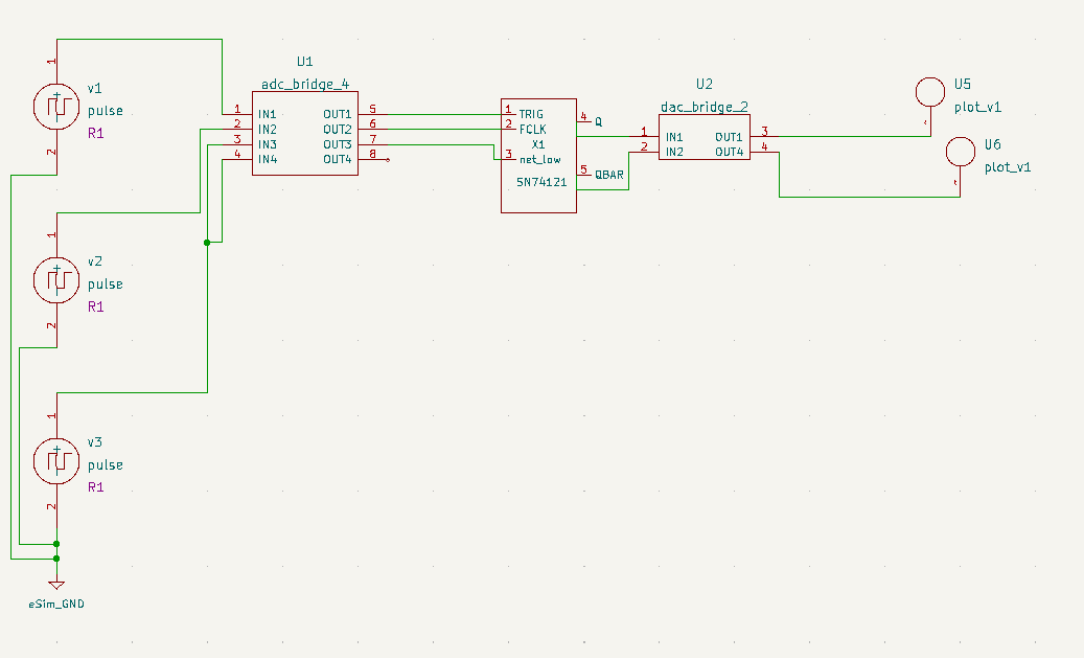

Figure 11.3: Test Circuit of the SN74121

11.7 Function Table

Inputs			Outputs	
A1	A2	B	Q	$\overline{Q}$
L	X	H	L	H
X	L	H	L	H
X	X	L	L	H
H	H	X	L	H
H	↓	H	⎍	⎍
↓	H	H	⎍	⎍
↓	↓	H	⎍	⎍
L	X	↑	⎍	⎍
X	L	↑	⎍	⎍

Figure 11.4: Function Table of the SN74121

11.8 Output Plot

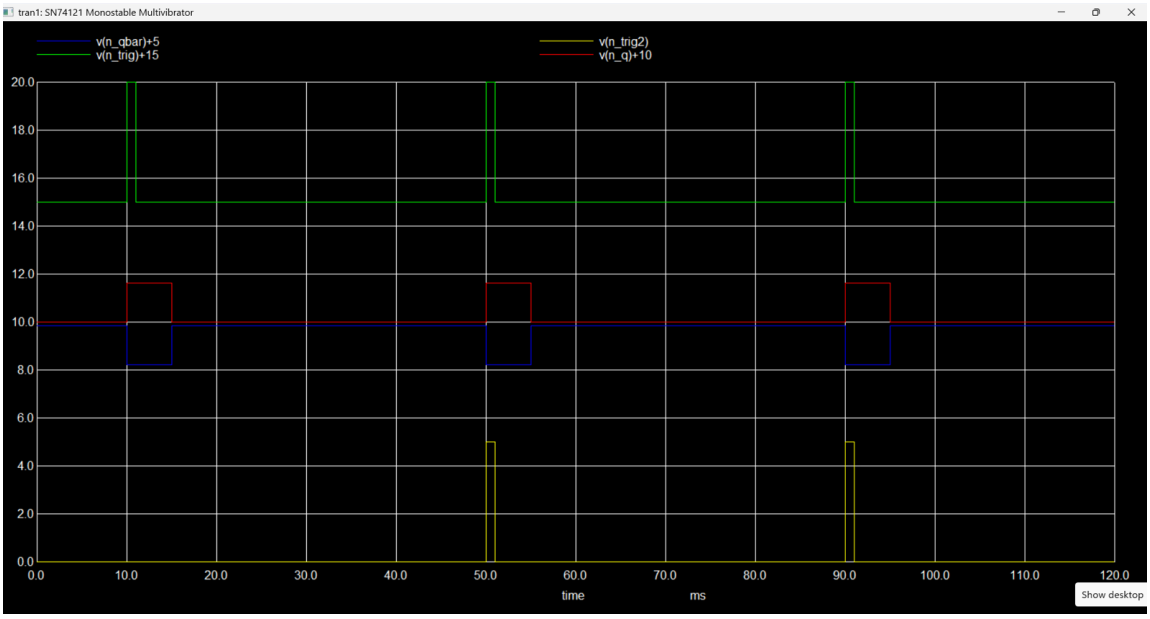

Figure 11.5: Output of the SN74121

Chapter 12

CD4520B

12.1 General Description

The CD4520B is a dual synchronous 4-bit up counter from the CMOS 4000B-series. It contains two identical independent 4-bit binary counters, each with a clock input, an enable input, and an active-HIGH reset. The counter advances on the rising edge of the clock when the enable is HIGH. Both counters can be cascaded for wider counting applications.

12.2 Key Features

- Dual synchronous 4-bit binary up counter
- Positive-edge clock triggered with active-HIGH enable
- Active-HIGH synchronous reset
- Wide supply voltage range: 3 V – 18 V
- Cascadable for wider word lengths

12.3 Applications

- Frequency division and event counting
- Digital clocks and timers
- Address sequencing in memory systems
- General-purpose counting in CMOS circuits

12.4 Subcircuit Symbol

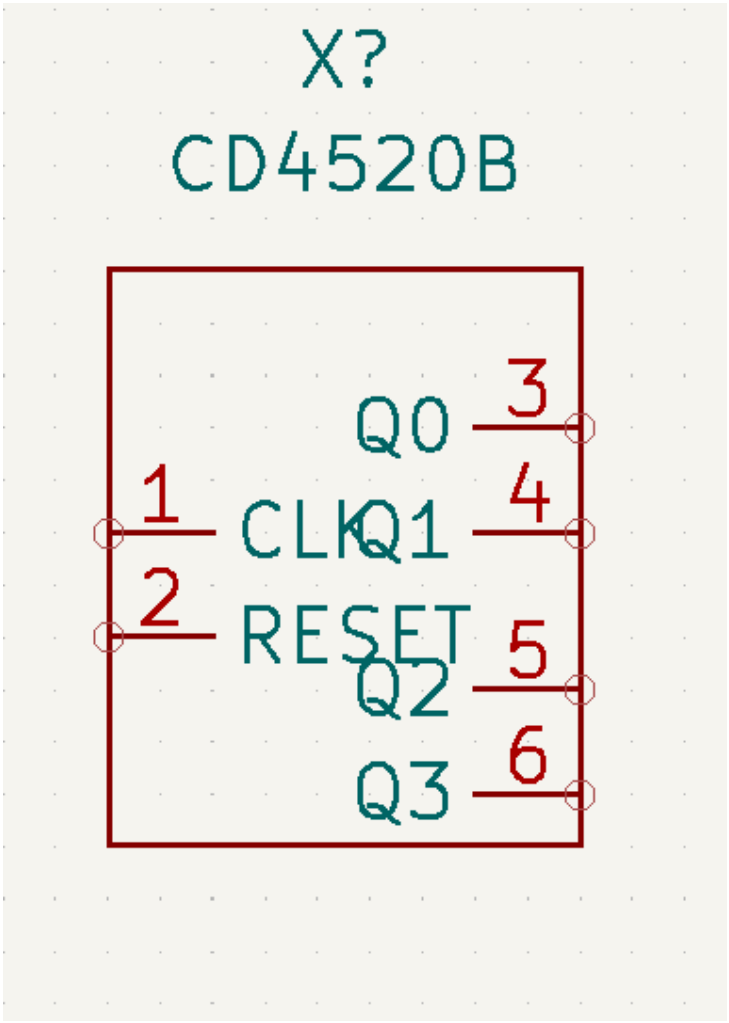

Figure 12.1: Subcircuit Symbol of the CD4520B

12.5 Subcircuit Schematic Diagram

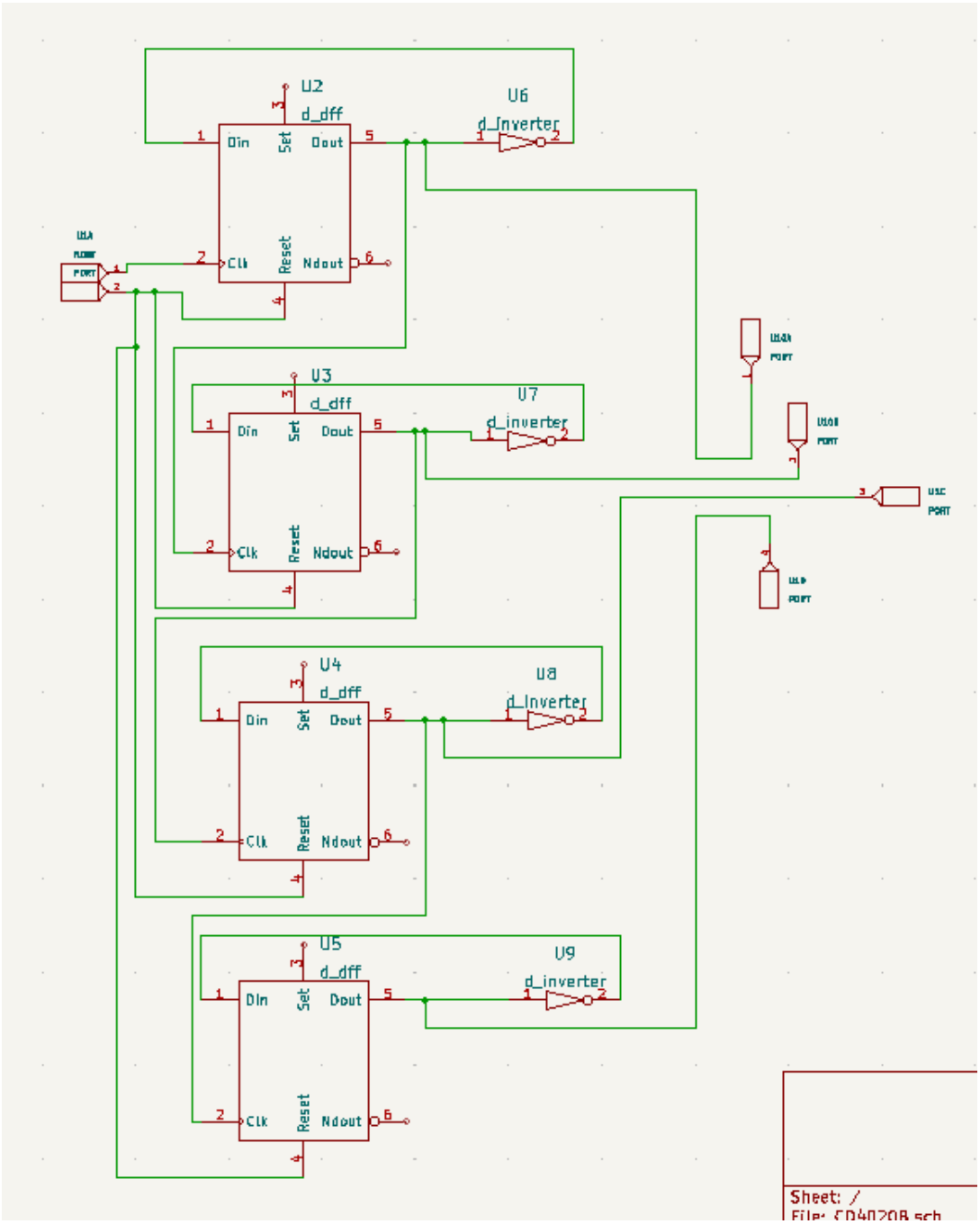

Figure 12.2: Subcircuit Schematic of the CD4520B

12.6 Test Circuit

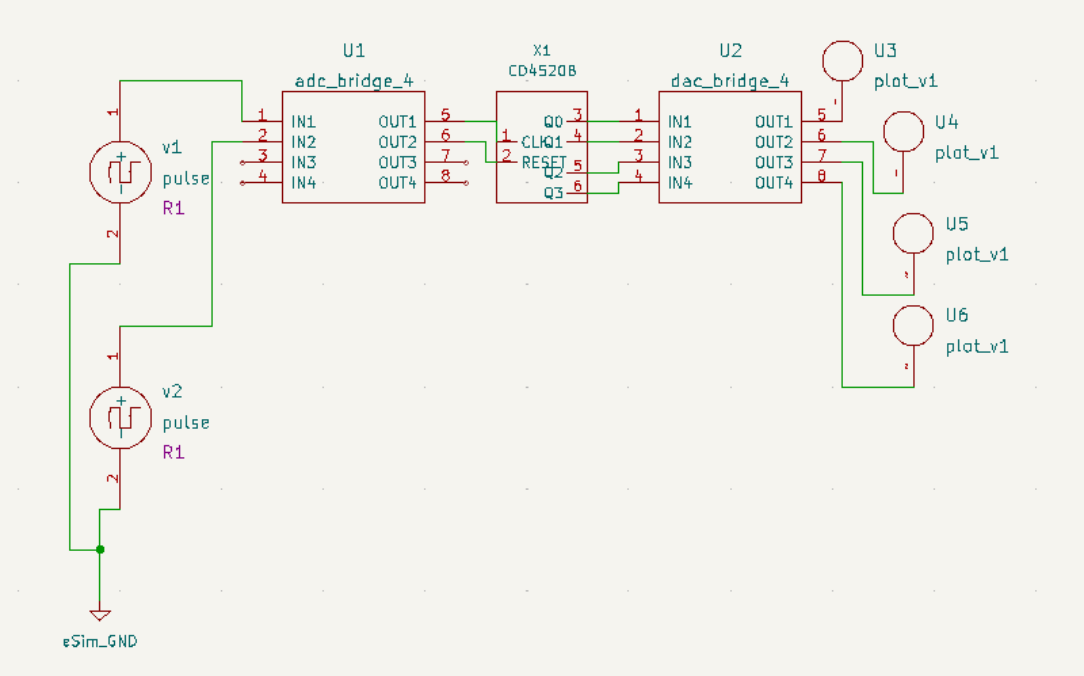

Figure 12.3: Test Circuit of the CD4520B

12.7 Function Table

CLOCK	ENABLE	RESET	ACTION
↑	1	0	Increment Counter
0	↓	0	Increment Counter
↓	X	0	No Change
X	↑	0	No Change
↑	0	0	No Change
1	↓	0	No Change
X	X	1	Q1 thru Q4 = 0

Figure 12.4: Function Table of the CD4520B

12.8 Output Plot

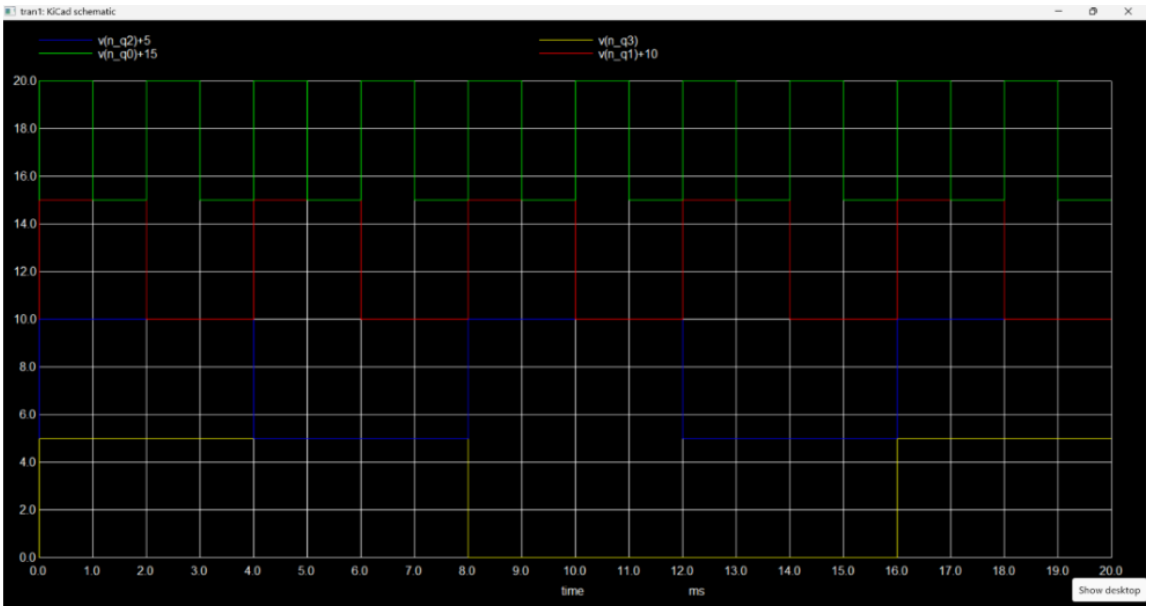

Figure 12.5: Output of the CD4520B

Chapter 13

74HC112

13.1 General Description

The 74HC112 is a dual negative-edge-triggered J-K flip-flop with individual set ($\overline{S}$) and clear ($\overline{CD}$) inputs from the HC (High-speed CMOS) family. Each flip-flop has independent J, K, clock, set, and clear inputs along with complementary Q and $\overline{Q}$ outputs. It operates from 2 V to 6 V and is TTL-compatible.

13.2 Key Features

- Dual negative-edge-triggered J-K flip-flop
- Individual active-LOW asynchronous set and clear
- High-speed CMOS performance
- Wide supply range: 2 V – 6 V
- TTL-compatible inputs and outputs

13.3 Applications

- Toggle and divide-by-two circuits
- Sequential state machines
- Data storage and synchronisation
- Frequency counters and dividers

13.4 Subcircuit Symbol

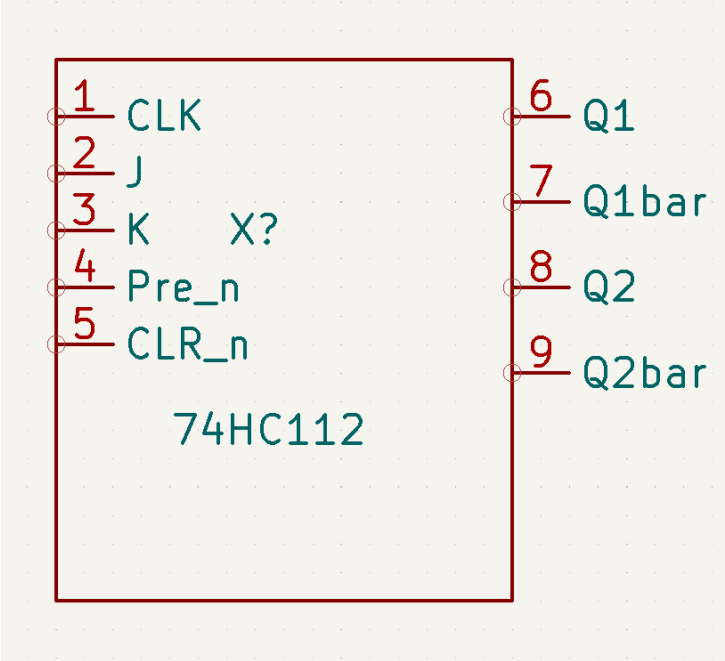

Figure 13.1: Subcircuit Symbol of the 74HC112

13.5 Subcircuit Schematic Diagram

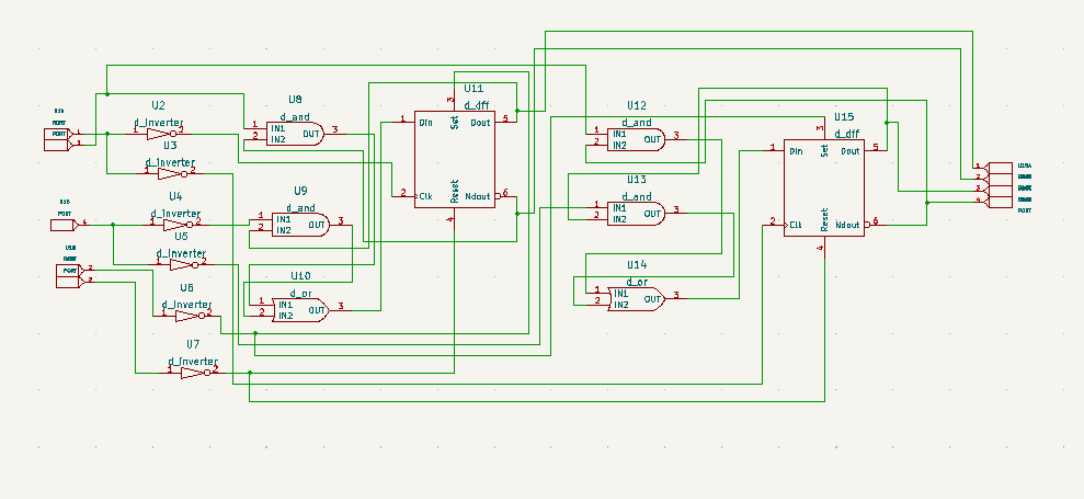

Figure 13.2: Subcircuit Schematic of the 74HC112

13.6 Test Circuit

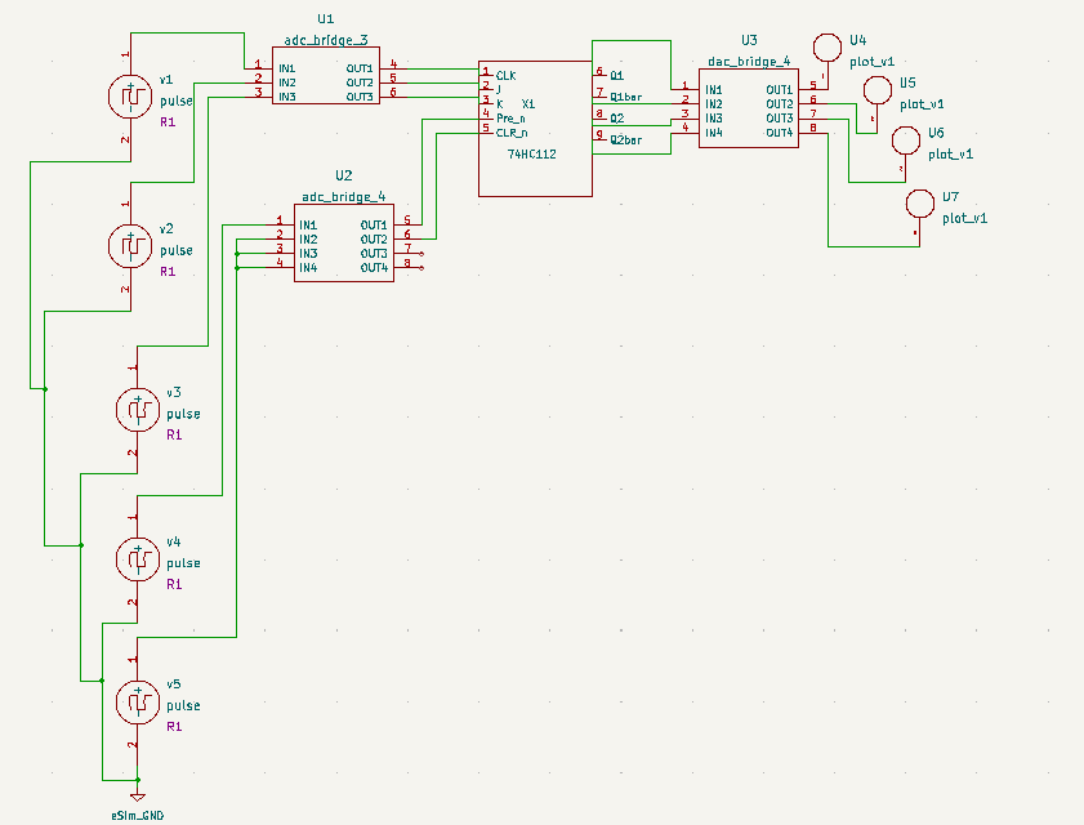

Figure 13.3: Test Circuit of the 74HC112

13.7 Function Table

OPERATING MODE	INPUTS					OUTPUTS	
	$n\overline{S}_D$	$n\overline{R}_D$	$n\overline{CP}$	nJ	nK	nQ	$n\overline{Q}$
asynchronous set	L	H	X	X	X	H	L
asynchronous reset	H	L	X	X	X	L	H
undetermined	L	L	X	X	X	H	L
toggle	H	H	↓	h	h	$\overline{q}$	q
load “0” (reset)	H	H	↓	l	h	L	H
load “1” (set)	H	H	↓	h	l	H	L
hold “no change”	H	H	↓	l	l	q	$\overline{q}$

Figure 13.4: Function Table of the 74HC112

13.8 Output Plot

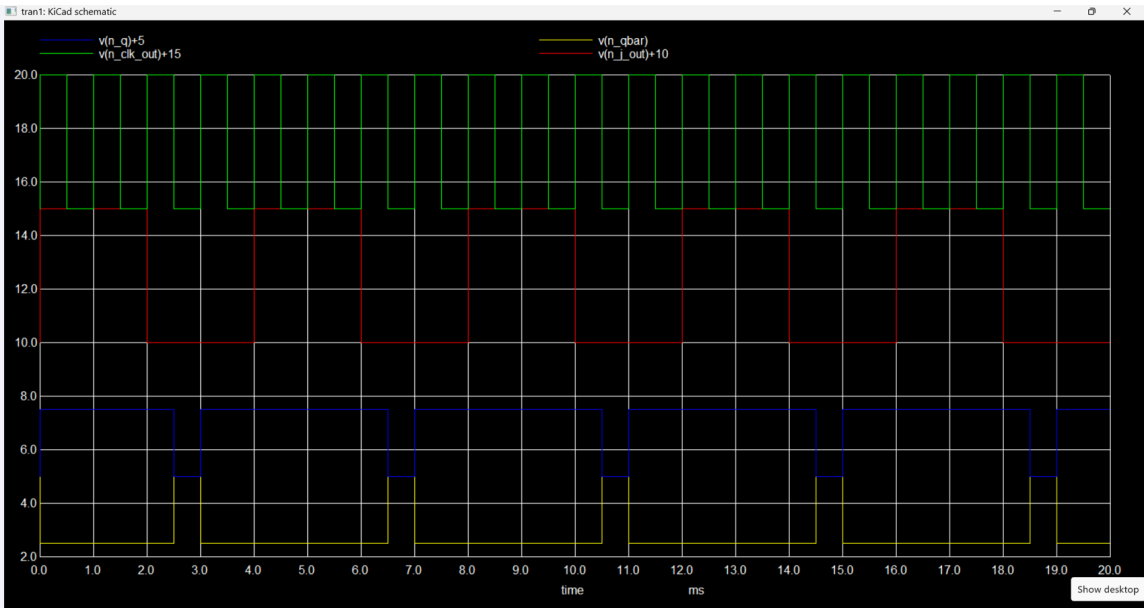

Figure 13.5: Output of the 74HC112

Chapter 14

Conclusion and Future Scope

The project successfully fulfilled its objective of contributing a diverse set of accurately modelled digital logic ICs to the eSim subcircuit library. Each IC was implemented based on its official datasheet and rigorously tested through simulation testbenches to ensure functional correctness and reliability.

The contributions include fundamental digital components such as buffers, shift registers, multiplexers, counters, a PLL, a rate multiplier, monostable multivibrators, and J-K flip-flops – covering a broad range of digital design use cases. These verified models serve as valuable resources for students, educators, and researchers using eSim.

As the eSim device model library continues to grow, broader adoption is anticipated among the engineering community, enabling increasingly sophisticated open-source circuit simulation.

Chapter 15

Circuits Contribution

This chapter lists all the Integrated Circuits (ICs) contributed during the fellowship. Each IC has been carefully modelled, simulated, and verified.

15.1 Kaviya Dharshini G – List of ICs

1. **74LS125** – Quad Tri-State Bus Buffer
2. **74LS165** – 8-Bit Parallel-In / Serial-Out Shift Register
3. **CD4051** – Single 8-Channel Analog Multiplexer/Demultiplexer
4. **74LS123** – Dual Retriggerable Monostable Multivibrator
5. **74LS161** – Synchronous 4-Bit Binary Counter
6. **CD4046** – CMOS Phase-Locked Loop (PLL)
7. **SN7497** – 6-Bit Binary Rate Multiplier
8. **SN74121** – Monostable Multivibrator with Schmitt-Trigger Inputs
9. **CD4520B** – Dual Synchronous 4-Bit Up Counter
10. **74HC112** – Dual Negative-Edge-Triggered J-K Flip-Flop

Bibliography

[1] FOSSEE Official Website, [Online]. Available: https://fossee.in. [Accessed: Jan. 2026].

[2] eSim Official Website, [Online]. Available: https://esim.fossee.in/. [Accessed: Jan. 2026].

[3] Texas Instruments, "74LS125 Datasheet," [Online]. Available: https://www.alldatasheet.com/datasheet-pdf/view/27648/TI/SN74LS125A.html.

[4] Texas Instruments, "74LS165 Datasheet," [Online]. Available: https://www.alldatasheet.com/datasheet-pdf/view/27696/TI/SN74LS165.html.

[5] Texas Instruments, "CD4051B Datasheet," [Online]. Available: https://www.ti.com/lit/ds/symlink/cd4051b.pdf.

[6] Texas Instruments, "74LS123 Datasheet," [Online]. Available: https://www.alldatasheet.com/datasheet-pdf/view/27642/TI/SN74LS123.html.

[7] Texas Instruments, "74LS161 Datasheet," [Online]. Available: https://www.alldatasheet.com/datasheet-pdf/view/27670/TI/SN74LS161A.html.

[8] Texas Instruments, "CD4046B Datasheet," [Online]. Available: https://www.ti.com/lit/ds/symlink/cd4046b.pdf.

[9] Texas Instruments, "SN7497 Datasheet," [Online]. Available: https://www.ti.com/lit/ds/symlink/sn7497.pdf.

[10] Texas Instruments, "SN74121 Datasheet," [Online]. Available: https://www.alldatasheet.com/datasheet-pdf/view/27560/TI/SN74121.html.

[11] Texas Instruments, "CD4520B Datasheet," [Online]. Available: https://www.ti.com/lit/ds/symlink/cd4520b.pdf.

[12] NXP Semiconductors, "74HC112 Datasheet," [Online]. Available: https://www.alldatasheet.com/datasheet-pdf/view/15521/PHILIPS/74HC112.html.