eSim Semester Long Internship Spring 2026

on

Openroad Integration in eSim

Submitted by

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Abstract

This report documents the work carried out during the FOSSEE Summer Internship 2026 at IIT Bombay. The primary objective of this internship was to integrate the eSim Electronic Design Automation (EDA) tool with the OpenROAD RTL-to-GDSII physical design flow, thereby creating a complete end-to-end open-source EDA pipeline — from schematic capture all the way to silicon layout generation.

Before this integration existed, eSim users could draw circuits, simulate them using Ngspice, and verify digital logic using NgVeri. However, there was no way to take those designs further into physical implementation — meaning students and researchers could not generate actual chip layouts from their eSim designs.

This internship bridges that gap. The work involved writing new Python modules, modifying existing eSim source files, creating Docker-based deployment infrastructure, and providing complete example circuits that demonstrate the full flow from schematic to GDSII layout. All code developed during this internship is available as Pull Request #473 on the FOSSEE/eSim GitHub repository, and also at the dedicated plugin repository: https://github.com/FOSSEE/eSim-to-OpenROAD_Design_Flow_Plugin

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Chapter 1

Introduction to eSim

1.1 Overview

eSim is a free and open-source Electronic Design Automation (EDA) tool developed by FOSSEE (Free and Open Source Software for Education) at IIT Bombay. It is designed to help students, researchers, and engineers design, simulate, and analyze electronic circuits without needing expensive proprietary software. eSim brings together several well-established open-source tools under a single unified graphical interface, making it accessible even to beginners in electronics design.

Think of eSim as a complete electronics workbench on your computer — you can draw your circuit, run simulations, see waveforms, design digital logic, and now, with this integration, even generate chip layouts — all for free.

The major tools integrated within eSim are:

- **KiCad** — A powerful open-source tool for drawing electronic schematics and designing PCB (Printed Circuit Board) layouts. It is the starting point for any design in eSim.
- **Ngspice** — The simulation engine that takes your circuit schematic and runs SPICE-based analog and mixed-signal simulations. It produces output files (`.cir.out`) that describe how voltages and currents behave over time.
- **GHDL and Verilator** — Open-source tools for simulating digital hardware description language (HDL) code written in VHDL or Verilog.
- **Makerchip** — An online IDE for writing and simulating TL-Verilog and SystemVerilog designs, integrated directly into eSim.
- **NgVeri** — A unique eSim module that converts Verilog digital models into Ngspice-

compatible code models, enabling mixed-signal simulations where digital and analog blocks interact.

- **OpenROAD Bridge (new)** — The module developed during this internship that takes eSim-generated netlists and feeds them into the OpenROAD physical design flow to produce chip layouts.

eSim is widely used across Indian academic institutions as a cost-effective and legally accessible alternative to commercial EDA suites such as Cadence Virtuoso, Mentor Graphics, and Synopsys Design Compiler, which cost hundreds of thousands of dollars per license.

1.2 History and Motivation

The eSim project was initiated under the FOSSEE programme at IIT Bombay with the primary motivation of democratizing access to EDA tools for Indian engineering students. Before eSim existed, circuit simulation courses in Indian colleges were either skipped due to lack of software licenses, or conducted using illegal copies of proprietary tools.

The development of eSim went through several important milestones:

- **Early versions** focused primarily on SPICE-based analog circuit simulation using Ngspice as the backend.
- **KiCad integration** was added to provide a proper schematic editor, replacing the need to write SPICE netlists by hand.
- **Version 2.x** introduced NgVeri and GHDL support, enabling mixed-signal simulation where a Verilog digital block can be co-simulated with an analog Ngspice circuit.
- **Version 2.5 (current)** introduced Docker-based deployment for better portability and reproducibility across different machines.
- **This internship (2026)** adds OpenROAD integration, enabling physical design from eSim for the first time.

The motivation for this specific internship project was clear: eSim could already help students design and simulate circuits, but it had no path to physical implementation. A student could design a full adder in eSim, simulate it, verify it works — but could not take it further to see how it would look as an actual chip layout. The OpenROAD integration fills this gap completely.

1.3 Architecture of eSim

The eSim architecture follows a modular, pipeline-based design philosophy. Each module is responsible for a specific transformation of the circuit data — from a human-drawn schematic all the way down to simulation results and now physical layout files.

The key principle is that each stage produces output files that serve as input for the next stage. This makes the system modular and extensible — which is exactly what made it possible to add the OpenROAD integration without breaking any existing functionality.

Table 1.1: eSim Component Overview and Responsibilities

Component	**Technology**	**What It Does**
Schematic Editor	KiCad 6.0	The user draws the circuit here. Produces a `.cir` netlist file.
Analog Simulator	Ngspice	Runs SPICE simulation. Produces `.cir.out` waveform data.
Digital Simulator	GHDL / Verilator	Compiles and simulates Verilog/VHDL digital logic models.
NgVeri Module	Python + Verilator	Converts Verilog digital models into Ngspice code models for mixed-signal use.
Maker Module	Python (PyQt5)	The main GUI tab that orchestrates NgVeri, Makerchip, and other operations.
OpenROAD Bridge	Python (NEW)	Takes the `.cir.out` netlist, converts it to Verilog, and launches the OpenROAD physical design flow.

The `src/maker/` directory is the brain of eSim's Python backend. All the important orchestration and conversion logic lives here. The files in this directory that were created or modified as part of this internship are:

- `Maker.py` — The main Makerchip tab widget class
- `NgVeri.py` — The NgVeri tab widget class
- `ModelGeneration.py` — Handles Verilog-to-Ngspice model generation
- `createkicad.py` — Creates KiCad symbol files
- `netlist_to_verilog.py` — **NEW:** The core OpenROAD bridge script
- `OpenROAD.py` — **NEW:** The PyQt5 GUI entry point for OpenROAD

1.4 The KiCad-to-Ngspice Pipeline

To understand where the OpenROAD integration fits in, it is important to first understand the standard eSim workflow. When a user works with eSim, the circuit goes through the following transformation stages:

1. **Schematic Capture in KiCad** — The user opens KiCad inside eSim and draws the circuit by placing components and connecting wires. This is a fully visual process — no code is written at this stage.
2. **Netlist Export** — KiCad exports the schematic as a `.cir` netlist file. This file describes all components and connections in SPICE format, which is a text-based circuit description language used by simulators.
3. **Ngspice Conversion** — eSim processes the netlist and converts it to a format that Ngspice can simulate. This step handles things like component model lookups and simulation command generation.
4. **Simulation** — Ngspice runs the actual simulation and writes the results to a `.cir.out` file. This file contains voltage and current values at every node over time.
5. **Waveform Viewing** — The simulation results are visualized using the GAW3 analog waveform viewer, allowing the user to inspect voltage and current plots.
6. **Verilog Generation (NEW)** — The `netlist_to_verilog.py` script reads the `.cir.out` file and generates a structural Verilog (`.v`) file that represents the logic of the circuit.
7. **Physical Design (NEW)** — OpenROAD takes the Verilog file and runs the complete RTL-to-GDSII physical design flow, producing a chip layout at each stage (synthesis, floorplan, placement, routing, final GDSII).
8. **Layout Viewing (NEW)** — The OpenROAD GUI opens automatically at the furthest completed stage, allowing the user to visually inspect the chip layout.

1.5 Importance of PDKs and the SkyWater 130nm PDK

A Process Design Kit (PDK) is a set of files provided by a semiconductor foundry that describes how their manufacturing process works. In simple terms, a PDK tells the EDA tools: "here are the rules, dimensions, and properties of the transistors, wires, and other structures you can use when designing a chip for our factory."

Without a PDK, physical design tools like OpenROAD cannot produce a real, manufac-

turable chip layout — they would not know what sizes to use, what materials are available, or what design rules must be followed.

This integration uses the **SkyWater 130nm High Density PDK (sky130hd)**, which is the world's first fully open-source PDK, released by SkyWater Technology Foundry in partnership with Google in 2020. It represents a 130 nanometer CMOS process, which means the smallest transistor features are 130 nanometers wide — large by modern standards, but perfect for educational and research designs.

The sky130hd PDK was chosen for this project because:

- It is completely free and open-source — no license required
- It is officially supported by OpenROAD Flow Scripts
- It has been used in many successful academic tapeouts
- It provides all necessary files: standard cells, timing models, routing rules, DRC decks, and LVS rules

Chapter 2

eSim Installation and Setup

2.1 System Requirements

Before setting up the integrated eSim + OpenROAD environment, it is important to ensure your system meets the following requirements. The OpenROAD build process is particularly demanding in terms of disk space and RAM, as it compiles several large tools from source including Yosys, OpenROAD, and the SkyWater PDK. Skipping any of these requirements may lead to build failures or very slow performance.

2.2 Step-by-Step Installation

This section walks through the complete installation process from a fresh Ubuntu 22.04 machine. Follow each step carefully and in order. Do not skip any step, as each one prepares the environment for the next.

2.2.1 Step 1: Install Docker

Docker is a containerization platform that allows software to run in isolated environments called containers. In this integration, Docker is used to run the OpenROAD flow scripts in a controlled environment where all dependencies are pre-installed and version-pinned. This avoids the common problem of "it works on my machine but not yours."

```
sudo apt-get update
sudo apt-get install -y docker.io
sudo systemctl start docker
sudo systemctl enable docker
sudo usermod -aG docker $USER
```

Listing 2.1: Install Docker on Ubuntu 22.04

Table 2.1: System Requirements for eSim + OpenROAD Integration

Component	**Requirement and Reason**
Operating System	Ubuntu 22.04 LTS — All scripts and dependencies have been tested on this version. Other versions may work but are not guaranteed.
RAM	Minimum 8 GB. 16 GB strongly recommended because OpenROAD compilation and place-and-route are memory-intensive operations.
Storage	At least 50 GB free space. OpenROAD-flow-scripts alone requires 15–20 GB after building.
Processor	64-bit x86 CPU. Multi-core processor recommended to speed up the OpenROAD build process.
Docker	Latest version of docker.io. Required for running OpenROAD inside a container during the flow execution.
Git	Any recent version. Required for cloning repositories.
Internet	Required during initial setup for downloading packages and cloning repositories. Not needed after setup.

Important: After running the above commands, you must log out and log back in. This is necessary for the `usermod` change to take effect. Without this step, Docker commands will require `sudo` every time.

2.2.2 Step 2: Clone the eSim Repository

Clone the main FOSSEE eSim repository from GitHub. This downloads the complete eSim source code, examples, library files, and scripts to your local machine.

```
git clone https://github.com/FOSSEE/eSim.git
cd eSim
```

Listing 2.2: Clone eSim from GitHub

2.2.3 Step 3: Switch to PR #473 (OpenROAD Integration Branch)

This is the most important step for getting the OpenROAD integration. Pull Request #473 contains all the modifications made during this internship — the new Python scripts, modified source files, example circuits, and updated Docker configuration.

If this PR has already been merged into the main branch by the time you read this report,

you can skip this step and the main branch will already contain all the integration code. If the PR is still pending, you must explicitly check it out as shown below.

```
git fetch origin pull/473/head:openroad-bridge
git checkout openroad-bridge
```

Listing 2.3: Checkout PR #473 OpenROAD Integration Branch

You can verify you are on the correct branch by running:

```
git branch
# Should show: * openroad-bridge
```

Listing 2.4: Verify current branch

2.2.4 Step 4: Install OpenROAD Flow Scripts

OpenROAD Flow Scripts is the open-source RTL-to-GDSII physical design flow that we are integrating with eSim. This step clones and builds the entire OpenROAD toolchain including Yosys (synthesis), OpenROAD (place and route), and all supporting utilities. The build process takes approximately 30–60 minutes depending on your machine.

```
git clone --recursive \
  https://github.com/The-OpenROAD-Project/OpenROAD-flow-scripts.git
cd OpenROAD-flow-scripts
./build_openroad.sh --local
```

Listing 2.5: Clone and Build OpenROAD Flow Scripts

The `-recursive` flag is essential because OpenROAD has many git submodules (nested repositories) that must also be downloaded. The `-local` flag tells the build script to install tools locally in the repository folder rather than system-wide.

For the full official tutorial, refer to: https://openroad-flow-scripts.readthedocs.io/en/latest/tutorials/FlowTutorial.html

2.2.5 Step 5: Launch eSim

After completing the above steps, launch eSim using the launcher script:

```
cd ~/eSim
bash scripts/launcher-esim.sh
```

Listing 2.6: Launch eSim with OpenROAD Integration

The launcher script sets up the required Python path, runs the setup configuration script, and starts the eSim GUI application. Once eSim opens, you will find the **OpenROAD-GDSII** button available in the workspace, which triggers the complete physical design flow.

2.3 Directory Structure of eSim

Understanding the directory structure of eSim is important for any intern or developer who wants to make modifications or debug issues. The key directories and their purposes are described below:

```
eSim/
|
|-- src/                          # All Python source code
|   |-- frontEnd/                 # PyQt5 GUI application entry point
|   |-- maker/                    # Core backend orchestration modules
|   |   |-- Maker.py              # Makerchip tab (Verilog file
    management)
|   |   |-- NgVeri.py             # NgVeri tab (Verilog to Ngspice)
|   |   |-- ModelGeneration.py    # Ngspice code model generation
|   |   |-- createkicad.py        # KiCad symbol file creation
|   |   |-- netlist_to_verilog.py  # NEW: SPICE to Verilog + OpenROAD
    runner
|   |   |-- OpenROAD.py             # NEW: PyQt5 GUI bridge for OpenROAD
|   |   |-- Appconfig.py          # Application configuration handler
|   |   `-- makerchip.py          # Makerchip IDE integration
|
|-- Examples/                     # Sample circuits for testing
|   |-- FullAdder/                # Full adder example (NEW)
|   |-- Half_Adder/               # Half adder with OpenROAD files (NEW)
|   `-- counter/                  # Counter circuit example (NEW)
|
|-- library/                      # Component and symbol libraries
|   |-- kicadLibrary/             # KiCad symbol files
|   `-- modelParamXML/            # XML parameter files for Ngspice
    models
|
|-- scripts/                      # Shell scripts for setup and launch
|   |-- launcher-esim.sh          # Main eSim launcher (MODIFIED)
|   `-- setup-esim.sh             # First-run configuration (MODIFIED)
|
|-- nghdl/                        # NGHDL (Ngspice+GHDL) related files
|   `-- install-nghdl-scripts/    # NGHDL installer scripts (MODIFIED)
|
`-- docker-launcher/              # Docker deployment infrastructure
    `-- Dockerfile                # Multi-stage Docker image (MODIFIED)
```

Listing 2.7: eSim Complete Directory Structure

2.4 Installation Scripts Modified During This Internship

As part of the integration work, three shell scripts required modification to support the OpenROAD environment and fix compatibility issues with Ubuntu 22.04.

2.4.1 scripts/launcher-esim.sh

The launcher script is the main entry point for starting eSim. It was modified to export the correct Python path and ensure the application starts with all necessary environment variables set. The key change was ensuring that `PYTHONPATH` includes the eSim source directory so that all internal imports resolve correctly.

```
#!/bin/bash
# Launcher script for eSim (PR #473 OpenROAD Integration Version)

# Add eSim source to Python path so all imports work correctly
export PYTHONPATH=$HOME/eSim/src:$PYTHONPATH

# Suppress verbose Qt logging that clutters the terminal
export QT_LOGGING_RULES="qt5.*=false"

# Run the setup script on first launch to initialize config files
$HOME/eSim/scripts/setup-esim.sh

# Navigate to the eSim front-end directory
cd $HOME/eSim/src/frontEnd

# Start the eSim PyQt5 application
exec python3 ./Application.py "$@"
```

Listing 2.8: Updated launcher-esim.sh

2.4.2 scripts/setup-esim.sh

The setup script runs on first launch and creates the necessary configuration files for eSim and NGHDL. It checks whether the config directories already exist before writing them, so it is safe to run multiple times without overwriting user settings.

```
#!/usr/bin/bash
config_dir_esim="$HOME/.esim"
config_dir_nghdl="$HOME/.nghdl"
eSim_HOME="$HOME/eSim"
NGHDL_HOME="$HOME/nghdl-simulator"

# Only create eSim config if not already done
```

```
if [ ! -d "$config_dir_esim/.setup_done" ]; then
    mkdir -p $config_dir_esim
    echo "[eSim]" > $config_dir_esim/config.ini
    echo "eSim_HOME = $eSim_HOME" >> $config_dir_esim/config.ini
    echo "LICENSE = %(eSim_HOME)s/LICENSE" >> $config_dir_esim/config.
    ini
    touch "$config_dir_esim/.setup_done"
fi
```

Listing 2.9: Key section of setup-esim.sh

2.4.3 nghdl/install-nghdl-scripts/install-nghdl-22.04.sh

This script installs the NGHDL simulator (Ngspice with GHDL support). It was updated to fix package name changes in Ubuntu 22.04, particularly around LLVM version references. Ubuntu 22.04 ships with LLVM 14 by default, whereas the previous script assumed LLVM 11.

Chapter 3

eSim and OpenROAD Integration

3.1 What is OpenROAD?

OpenROAD (Open Roadmap for EDA) is a fully open-source, automated RTL-to-GDSII physical design flow developed under the DARPA OpenROAD programme. In simple terms, it takes your digital logic design written in Verilog and automatically converts it into a manufacturable chip layout file (GDSII format) that can be sent to a semiconductor foundry for fabrication.

Before OpenROAD existed, RTL-to-GDSII tools were exclusively proprietary and extremely expensive — often costing millions of dollars for a full institutional license. OpenROAD changed this by providing the complete flow for free, making it possible for universities, research groups, and individual designers to produce real chip layouts.

The OpenROAD flow uses the following individual tools:

- **Yosys** — Logic synthesis: converts Verilog RTL to a gate-level netlist using a standard cell library
- **OpenROAD app** — Handles floorplanning, placement, clock tree synthesis, and routing
- **KLayout** — Final GDSII viewer and DRC checking
- **Magic** — Additional layout viewing and LVS checking

The complete stage-by-stage breakdown of the OpenROAD flow is shown below:

Table 3.1: OpenROAD Flow Stages and Their Descriptions

Stage	Name	What Happens
1	Synthesis	Yosys converts the Verilog code to a netlist of logic gates from the sky130hd standard cell library.
2	Floorplan	The die area and core area boundaries are defined. IO pins are placed around the periphery.
3.1	Global Placement	All standard cells are placed approximately within the core area to minimize wire length.
3.2	IO Placement	Input/output pins are precisely placed.
3.3	Macro Placement	Any large memory blocks or IP macros are placed.
3.4	Resizing	Cells are resized and buffers inserted to meet timing.
3.5	Detail Placement	Final legal placement ensuring no overlaps.
4	CTS	A clock tree network is built to distribute the clock signal with minimal skew.
5	Routing	Metal wires are routed between all cells following design rules.
6	Final	DRC checking, GDS stream-out, final reports generated.

3.2 Why Integrate eSim with OpenROAD?

The integration of eSim with OpenROAD creates something that did not exist before: a completely free, open-source design flow that takes a circuit from initial schematic all the way to a chip layout. This has significant educational value because students can now:

- Design a circuit in eSim visually using KiCad schematics
- Simulate it to verify correct operation using Ngspice
- Generate a structural Verilog representation automatically
- Run physical design to see how the circuit would be laid out on silicon
- Visualize the chip layout in OpenROAD's GUI

This entire journey — from drawing a circuit to seeing a chip layout — happens within a single open-source toolchain, requiring no proprietary software or paid licenses. This is a significant contribution to open EDA education.

3.3 Integration Architecture Overview

The integration was implemented by creating two new Python modules in the `src/maker/` directory of eSim. These modules sit between eSim's existing simulation pipeline and the OpenROAD flow scripts, acting as a translation and orchestration layer.

The complete data flow through the integrated system is:

```
[User draws circuit in KiCad schematic editor]
                    |
                    v
       KiCad exports schematic
       as SPICE netlist (.cir)
                    |
                    v
   eSim converts .cir to .cir.out
   (Ngspice simulation output file)
                    |
                    v
 [User clicks OpenROAD-GDSII button in eSim GUI]
                    |
                    v
       OpenROAD.py (GUI bridge)
       validates netlist path
       and calls the script
                    |
                    v
     netlist_to_verilog.py
     reads .cir.out, finds .v file,
     extracts module name, generates
     config.mk and constraint.sdc
                    |
                    v
   OpenROAD Flow Scripts (via Docker)
   Stage 1: Synthesis (Yosys)
   Stage 2: Floorplan
   Stage 3: Placement
   Stage 4: Clock Tree Synthesis
   Stage 5: Routing
   Stage 6: Final GDSII
                    |
                    v
   OpenROAD GUI opens automatically
   at furthest completed stage
   showing the chip layout
```

Listing 3.1: Complete eSim to OpenROAD Data Flow

3.4 The netlist_to_verilog.py Module — Detailed Explanation

This is the most important file created during this internship. It is a 250-line Python script that acts as the complete automation engine for the OpenROAD integration. Every time a user clicks the OpenROAD-GDSII button in eSim, this script runs and handles the entire process from finding the Verilog file to launching the GUI.

3.4.1 Module Name Normalization

When eSim circuits are named by users, they often contain spaces, hyphens, parentheses, or other special characters that are illegal in Verilog identifiers (Verilog module names must follow IEEE 1364-2005 naming rules). The `normalize_module_name()` function sanitizes the circuit name to ensure it is a valid Verilog identifier while preserving the original case and meaning as much as possible.

```
def normalize_module_name(name):
    """
    Preserves original case (Halfwave_Rectifier stays Halfwave_Rectifier).
    Only fixes invalid characters and collapses double underscores.
    For example:
      "Full Adder"    -> "Full_Adder"
      "my-circuit!"   -> "my_circuit"
      "RC__Filter"    -> "RC_Filter"
    """
    name = re.sub(r'[^a-zA-Z0-9_]', '_', name)
    name = re.sub(r'_+', '_', name)
    return name.strip('_')
```

Listing 3.2: Module Name Normalization Function

3.4.2 Intelligent Stage ODB Detection

One of the smart features of this integration is that it does not require the OpenROAD flow to complete fully before showing results. The script checks all possible stage output files from the last stage backwards, and opens the GUI at whichever stage completed successfully. This means if synthesis works but placement fails, the user can still see the synthesized netlist — they are not left with a blank screen.

```
STAGE_ODBS = [
    ("6_final.odb",        "Stage 6 - Final"),
    ("5_route.odb",        "Stage 5 - Routing"),
    ("4_cts.odb",          "Stage 4 - Clock Tree Synthesis"),
    ("3_5_place_dp.odb",   "Stage 3.5 - Detail Placement"),
```

```
    ("3_4_place_resized.odb", "Stage 3.4 - Resizing"),
    ("3_3_place_mpl.odb",  "Stage 3.3 - Macro Placement"),
    ("3_2_place_iop.odb",  "Stage 3.2 - IO Placement"),
    ("3_1_place_gp.odb",   "Stage 3.1 - Global Placement"),
    ("2_floorplan.odb",    "Stage 2 - Floorplan"),
    ("1_synth.odb",        "Stage 1 - Synthesis"),
]

def find_latest_odb(orfs_flow, module_name):
    base_dir = os.path.join(
        orfs_flow, "results", "sky130hd", module_name, "base")
    for odb_file, stage_label in STAGE_ODBS:
        full_path = os.path.join(base_dir, odb_file)
        if os.path.isfile(full_path):
            print(f"[v] Found: {stage_label} -> {odb_file}")
            return odb_file, stage_label
    return None, None
```

Listing 3.3: Stage ODB Detection — Checks All Stages

3.4.3 Automatic Clock Detection

Digital designs can be either combinational (no clock) or sequential (clocked, using flip-flops). The timing constraints for OpenROAD differ significantly between these two cases. The script automatically detects which type of design it is dealing with by searching the Verilog source for clock-related keywords, and generates the appropriate SDC timing constraint file accordingly.

```
def is_clocked_design(verilog_path):
    with open(verilog_path, "r", encoding="utf-8") as f:
        content = f.read()
    return (
        re.search(r"\bposedge\b", content) is not None or
        re.search(r"\bnegedge\b", content) is not None or
        re.search(r"\binput\s+.*\bclk\b",
                  content, re.IGNORECASE) is not None or
        re.search(r"\binput\b[^;\n]*\bclock\b",
                  content, re.IGNORECASE) is not None
    )
```

Listing 3.4: Automatic Clock Detection Logic

3.4.4 Automatic Config File Generation

The OpenROAD flow requires two configuration files: a `config.mk` Makefile fragment that specifies the design parameters, and a `constraint.sdc` file that specifies timing

constraints. These files were previously written manually. This integration generates them automatically from the circuit name and detected design type.

```
def build_config(module_name, project_name):
    return f"""export DESIGN_NAME = {module_name}
export PLATFORM    = sky130hd
export VERILOG_FILES = \
    ./designs/sky130hd/{project_name}/{project_name}.v
export SDC_FILE      = \
    ./designs/sky130hd/{project_name}/constraint.sdc
export DIE_AREA  = 0 0 100 100
export CORE_AREA = 10 10 90 90
"""

def build_sdc(is_clocked):
    if is_clocked:
        return "create_clock [get_ports clk] -period 10\n"
    return "set_units -time ns\n"
```

Listing 3.5: Automatic config.mk Generation

3.5 The OpenROAD.py Module — The GUI Bridge

While `netlist_to_verilog.py` does all the heavy lifting, the `OpenROAD.py` module is what connects eSim's GUI to that script. It is a PyQt5 class that handles user interaction, validates inputs, shows appropriate error messages, and triggers the conversion.

```
import os
import subprocess
from PyQt5 import QtWidgets

class OpenROADLogic:
    def __init__(self, project_path):
        self.project_path = project_path
        self.project_name = os.path.basename(project_path)

    def run(self):
        home_dir = os.path.expanduser("~")
        script_path = os.path.join(
            home_dir, "eSim", "src", "maker",
            "netlist_to_verilog.py")
        netlist_path = os.path.join(
            self.project_path,
            f"{self.project_name}.cir.out")

        if not os.path.exists(netlist_path):
            QtWidgets.QMessageBox.critical(
```

```
                None, "Error",
                "Netlist (.cir.out) not found!\n\n"
                "Please run 'Convert KiCad to Ngspice' first.")
            return

        try:
            result = subprocess.run(
                ['python3', script_path, netlist_path],
                capture_output=True, text=True)

            if result.returncode == 0:
                QtWidgets.QMessageBox.information(
                    None, "Success",
                    f"Verilog conversion successful for "
                    f"'{self.project_name}'!\n\n"
                    "Ready for OpenROAD synthesis.")
            else:
                QtWidgets.QMessageBox.warning(
                    None, "Script Error",
                    f"The conversion script failed:\n\n"
                    f"{result.stderr}")

        except Exception as e:
            QtWidgets.QMessageBox.critical(
                None, "Execution Error",
                f"Could not trigger the conversion script:\n{str(e)}")
```

Listing 3.6: Complete OpenROAD.py Module

Chapter 4

Docker Setup and Deployment

4.1 Why Docker for This Integration?

When building a complex software integration like eSim + OpenROAD, one of the biggest challenges is dependency management. OpenROAD alone depends on dozens of libraries at specific versions — CMake, Boost, TCL, SWIG, and many others. If these are installed system-wide, they can conflict with other software on the machine. Additionally, different users on different machines will inevitably have slightly different library versions, leading to the classic "it works on my machine" problem.

Docker solves this entirely by packaging the complete environment — the operating system, all libraries, all tools, all configuration — into a single image file. When you run that image, you always get exactly the same environment, regardless of what host machine you are on.

The specific advantages for this integration are:

- **Reproducibility** — Every user runs the exact same environment. If it works for the developer, it will work for the next intern.
- **Dependency isolation** — OpenROAD's complex dependencies are contained inside the Docker image and cannot interfere with the host system.
- **Version pinning** — The specific versions of OpenROAD, eSim, KiCad, and all tools are locked into the image, preventing unexpected breakage from updates.
- **Easy onboarding** — A new intern or user can get a fully working eSim + OpenROAD environment with a single `docker pull` command, without spending days on installation.
- **Cross-machine portability** — The same Docker image works on any Linux ma-

chine, making it easy to share work.

4.2 Existing Docker Infrastructure in eSim

The FOSSEE eSim repository already contained a `docker-launcher/` folder with a sophisticated multi-stage Dockerfile before this internship began. This Dockerfile built a complete eSim environment with:

- Ubuntu 22.04 LTS as the base operating system
- KiCad 6.0 with all symbol libraries
- Ngspice for SPICE simulation
- GHDL for VHDL simulation
- Verilator for Verilog simulation
- GAW3 waveform viewer (built from source)
- Python 3 virtual environment with all eSim dependencies
- TigerVNC server for remote GUI access
- noVNC for browser-based GUI access
- XFCE4 desktop environment inside the container

This was an excellent foundation. The task during this internship was to extend this Dockerfile by adding an OpenROAD installation stage.

4.3 OpenROAD Addition to the Dockerfile

The following block was added to the existing Dockerfile immediately before the `ENTRYPOINT` instruction. This placement ensures that OpenROAD is installed after all eSim components are in place, and that the OpenROAD tools are available in the `PATH` when eSim starts.

```
########################################
# Install OpenROAD Flow Scripts
########################################
USER root

RUN apt-get update && apt-get install -y \
    cmake ninja-build tcl-dev libreadline-dev \
    libffi-dev libboost-all-dev swig \
    && rm -rf /var/lib/apt/lists/*

```

```
RUN git clone --recursive \
    https://github.com/The-OpenROAD-Project/OpenROAD-flow-scripts.git \
    /opt/openroad \
    && cd /opt/openroad \
    && ./build_openroad.sh --local

ENV PATH="/opt/openroad/tools/install/OpenROAD/bin:${PATH}"
ENV OPENROAD_HOME=/opt/openroad

RUN chown -R ${USERNAME}:${USERNAME} /opt/openroad

USER ${USERNAME}
```

Listing 4.1: OpenROAD Block Added to docker-launcher/Dockerfile

4.4 Building and Running the Docker Image

4.4.1 Build the Image

The following command builds the complete eSim + OpenROAD Docker image. Note that this will take a significant amount of time (1–2 hours) because it compiles OpenROAD entirely from source. This only needs to be done once.

```
cd ~/eSim/docker-launcher
docker build -t esim-openroad:latest .
```

Listing 4.2: Build Docker Image

4.4.2 Run with X11 on Linux

If you are running on a local Linux machine with an X11 display server, use this command to run the container with GUI support:

```
docker run -it \
  -e DISPLAY=$DISPLAY \
  -v /tmp/.X11-unix:/tmp/.X11-unix \
  esim-openroad:latest
```

Listing 4.3: Run Container with X11 Display

4.4.3 Run with VNC (any OS)

If you are on Windows, macOS, or a remote server without X11, use VNC mode. This starts a VNC server inside the container and exposes it on port 6080. You can then access the eSim GUI through any web browser:

```
docker run -it -p 6080:6080 esim-openroad:latest --vnc
```

Listing 4.4: Run Container with VNC Mode

Then open your browser and navigate to: `http://localhost:6080/vnc.html`

Chapter 5

Comprehensive Code Comparison

5.1 Overview of Changes

This chapter provides a complete summary of every file that was created or modified during this internship. Understanding what changed and why is essential for any future intern or developer who wants to build on this work, fix issues, or extend the integration further.

The changes fall into three categories:

1. **New files** — Files that did not exist before and were created entirely during this internship
2. **Modified files** — Existing eSim files that were updated to support the OpenROAD integration or fix portability issues
3. **New examples** — New circuit examples that demonstrate the integration and serve as test cases

5.2 Summary of All Changes

5.3 Detailed Analysis of Key Changes

5.3.1 Changes to Maker.py

The `Maker.py` file is the PyQt5 widget class for the Makerchip tab in eSim. It was originally written with hardcoded absolute paths that contained the original developer's username. This meant it would fail immediately on any other machine where the username was different.

Table 5.1: Complete List of Modified and Added Files

File Path	Status	Purpose
src/maker/netlist_to_verilog.py	NEW	Core SPICE-to-Verilog translator and OpenROAD flow runner
src/maker/OpenROAD.py	NEW	PyQt5 GUI bridge connecting eSim button to the conversion script
src/maker/Maker.py	Modified	Fixed hardcoded paths for portability
src/maker/NgVeri.py	Modified	Safer file handling, fixed lint_off path operations
src/maker/ModelGeneration.py	Modified	Extended for digital cell model generation
src/maker/createkicad.py	Modified	Updated KiCad symbol integration
scripts/launcher-esim.sh	Modified	Added PYTHONPATH and Qt env variable exports
scripts/setup-esim.sh	Modified	Updated config path generation
nghdl/install-nghdl-22.04.sh	Modified	Fixed Ubuntu 22.04 LLVM package compatibility
docker-launcher/Dockerfile	Modified	Added OpenROAD installation stage
library/kicadLibrary/eSim-symbols/ eSim_Ngveri.kicad_sym	Modified	Added new digital symbols for OpenROAD-compatible designs
library/modelParamXML/Ngveri/counter.xml	NEW	Counter circuit Ngspice model parameters
library/modelParamXML/Ngveri/fulladder.xml	NEW	Full adder Ngspice model parameters
library/modelParamXML/Ngveri/halfwave_rectifier.xml	NEW	Halfwave rectifier model parameters
Examples/FullAdder/ (multiple files)	NEW	Complete full adder example with KiCad and OpenROAD files
Examples/Half_Adder/ (multiple files)	NEW	Half adder with .v, .sdc, config.mk ready for OpenROAD
Examples/counter/	NEW	Counter circuit example

The fix was straightforward but important: replace all hardcoded paths with dynamic paths using `os.path.expanduser()` which returns the current user's home directory regardless of username.

```
# BEFORE (broken on any machine except original developer's):
init_path = '/home/adarsh_10811/eSim/'

# AFTER (works on any machine, any username):
init_path = os.path.expanduser("~/eSim/")
```

Listing 5.1: Maker.py Path Fix for Portability

5.3.2 Changes to NgVeri.py

The `NgVeri.py` file handles the NgVeri tab in eSim, which manages the conversion of Verilog models to Ngspice code models. Two key issues were fixed:

Issue 1: Unsafe path construction

String concatenation for file paths is fragile and platform-dependent. The code was updated to use `os.path.join()` which correctly handles path separators on all operating systems.

```
# BEFORE: String concatenation -- fragile and Linux-specific
file = open(init_path + "library/tlv/lint_off.txt", 'r')

# AFTER: os.path.join -- correct on all platforms
file_path = os.path.join(init_path, "library", "tlv", "lint_off.txt")
with open(file_path, 'r') as file:
    data = file.readlines()
```

Listing 5.2: NgVeri.py Safer Path Construction

Issue 2: Missing exception handling in lint_off_edit()

The `lint_off_edit()` function previously had no error handling around file operations. If the lint_off.txt file was missing or unreadable, the application would crash silently. A try/except block was added to show a proper error dialog instead.

```
try:
    file_path = os.path.join(init_path, "library/tlv/lint_off.txt")
    with open(file_path, 'r') as file:
        data = file.readlines()
    data = [line for line in data if line.strip() != text]
    with open(file_path, 'w') as file:
        file.writelines(data)
except Exception as e:
    QtWidgets.QMessageBox.warning(
        None, "Warning",
        f"Could not remove lint_off entry '{text}'",
        QtWidgets.QMessageBox.Ok
```

```
13      )
```

Listing 5.3: NgVeri.py Exception Handling Added

Chapter 6

Detailed File-by-File Analysis

6.1 netlist_to_verilog.py — Complete Analysis

6.1.1 The Problem This File Solves

eSim generates SPICE netlists (`.cir.out`) after simulation. These files describe circuit behavior in terms of voltages, currents, and component models. However, OpenROAD requires a completely different input format: structural Verilog (`.v`), which describes the circuit as a hierarchy of logic gates and their interconnections.

The problem is not just format conversion. SPICE net names often contain characters that are illegal in Verilog (spaces, brackets, slashes, etc.), and SPICE does not have the concept of a "module name" the way Verilog does. The `netlist_to_verilog.py` script handles all of these translation challenges automatically, without requiring the user to understand any of this complexity.

6.1.2 Verilog File Search Logic

Rather than requiring the user to specify exactly where the Verilog file is, the script searches multiple candidate locations automatically. This makes the flow much more user-friendly — the user just clicks a button and the script figures out where everything is.

```
def find_generated_verilog(selected_path, project_name, orfs_design_dir):
    project_dir = os.path.dirname(selected_path) or "."
    home_dir    = os.path.expanduser("~")

    candidates = [
        os.path.join(project_dir, f"{project_name}.v"),
        os.path.join(home_dir, f"{project_name}.v"),
```

```
        os.path.join(orfs_design_dir, f"{project_name}.v"),
        selected_path.replace(".cir.out", ".v"),
    ]

    for path in candidates:
        if os.path.isfile(path):
            print(f"[v] Found Verilog: {path}")
            return path

    return None
```

Listing 6.1: Multi-location Verilog File Search

6.1.3 Main Flow Execution

The `main()` function orchestrates the complete flow from receiving the `.cir.out` path to launching the OpenROAD GUI. Each step is clearly logged to the terminal so users can see exactly what is happening and where any issues occur.

```
def main():
    selected_path = os.path.abspath(sys.argv[1])
    project_name  = os.path.basename(selected_path)\
                        .replace(".cir.out", "")

    orfs_root    = os.path.expanduser("~/OpenROAD-flow-scripts")
    if not os.path.isdir(orfs_root):
        fail("OpenROAD not found. Please install it first.")

    design_dir = os.path.join(
        orfs_root, "flow", "designs", "sky130hd", project_name)
    os.makedirs(design_dir, exist_ok=True)

    verilog_path = find_generated_verilog(
        selected_path, project_name, design_dir)

    module_name = normalize_module_name(
        extract_top_module_name(verilog_path))
    clocked     = is_clocked_design(verilog_path)

    shutil.copyfile(verilog_path,
        os.path.join(design_dir, f"{project_name}.v"))
    write_file(os.path.join(design_dir, "constraint.sdc"),
        build_sdc(clocked))
    write_file(os.path.join(design_dir, "config.mk"),
        build_config(module_name, project_name))

    cmd = [docker_shell, "make",
```

```
        f"DESIGN_CONFIG=./designs/sky130hd/{project_name}/config.mk",
        "finish"]
    subprocess.run(cmd, cwd=orfs_flow, env=env)

    stage_odb, stage_label = find_latest_odb(orfs_flow, module_name)
    # ... write TCL script and launch openroad -gui
```

Listing 6.2: Main Function Flow in netlist_to_verilog.py

6.2 Example Circuits

6.2.1 Half Adder Example

The Half Adder is the simplest example that demonstrates the complete eSim-to-OpenROAD flow. A half adder takes two single-bit inputs (A and B) and produces a Sum output (A XOR B) and a Carry output (A AND B). It was chosen as the first example because its logic is simple enough to verify manually, yet complex enough to demonstrate the full flow.

```
module Half_Adder (
    input  A,
    input  B,
    output Sum,
    output Carry
);
    assign Sum   = A ^ B;
    assign Carry = A & B;
endmodule
```

Listing 6.3: Half Adder Verilog (Half_Adder.v)

```
export DESIGN_NAME   = Half_Adder
export PLATFORM      = sky130hd
export VERILOG_FILES = \
    ./designs/sky130hd/Half_Adder/Half_Adder.v
export SDC_FILE      = \
    ./designs/sky130hd/Half_Adder/constraint.sdc
export DIE_AREA      = 0 0 100 100
export CORE_AREA     = 10 10 90 90
```

Listing 6.4: Half Adder OpenROAD Config (config.mk)

```
# Combinational design -- no clock constraint needed
set_units -time ns
```

Listing 6.5: Half Adder Timing Constraints (Half_Adder.sdc)

6.2.2 Full Adder Example

The Full Adder extends the Half Adder by adding a carry-in input. It adds three single-bit inputs (A, B, and Cin) and produces a Sum and a Carry-out. This example demonstrates that the integration works for slightly more complex designs with more ports and internal logic.

6.2.3 Counter Example

The Counter example demonstrates a sequential (clocked) design. Unlike the Half Adder and Full Adder which are combinational, the counter uses flip-flops and requires a clock signal. This exercises the clock detection logic in `netlist_to_verilog.py` and verifies that the correct clock constraint SDC is generated.

Chapter 7

Guidance for Future Interns

7.1 Where This Work Left Off

This chapter is written specifically for the next intern or developer who will continue this work. It explains the current state of the integration, what works, what does not work yet, and what the most valuable next steps would be.

As of May 2026, the following has been completed and works:

- The `netlist_to_verilog.py` script correctly finds Verilog files, generates config files, and launches the OpenROAD flow
- The `OpenROAD.py` GUI bridge connects the eSim button to the script
- The Docker image builds successfully with eSim + OpenROAD
- The Half Adder, Full Adder, and Counter examples work through the complete flow
- The intelligent stage detection opens the GUI at the furthest completed stage

The following areas need further work:

- The actual SPICE-to-Verilog conversion (parsing the `.cir.out` file and generating the `.v` file) currently requires the user to have a `.v` file already. A future intern should implement the actual netlist parser.
- The OpenROAD-GDSII button needs to be properly wired into the eSim GUI in `src/frontEnd/`
- Testing on more complex circuit examples beyond the basic digital gates
- Automatic handling of analog components that cannot be directly synthesized

7.2 How to Set Up the Development Environment

If you are starting as a new intern and want to continue this work, follow these steps exactly:

```
# Step 1: Install Docker
sudo apt-get update
sudo apt-get install -y docker.io
sudo systemctl start docker
sudo usermod -aG docker $USER
# LOG OUT AND LOG BACK IN after this step!

# Step 2: Clone eSim
git clone https://github.com/FOSSEE/eSim.git
cd eSim

# Step 3: Checkout the OpenROAD integration branch
git fetch origin pull/473/head:openroad-bridge
git checkout openroad-bridge

# Step 4: Install OpenROAD (takes 30-60 minutes)
cd ~
git clone --recursive \
  https://github.com/The-OpenROAD-Project/OpenROAD-flow-scripts.git
cd OpenROAD-flow-scripts
./build_openroad.sh --local

# Step 5: Launch eSim
cd ~/eSim
bash scripts/launcher-esim.sh
```

Listing 7.1: Complete Setup for New Interns

7.3 Key Files to Understand First

If you are a new intern trying to understand the codebase quickly, start by reading these files in this order:

1. **src/maker/OpenROAD.py** — Short and simple. Shows how the GUI calls the script.
2. **src/maker/netlist_to_verilog.py** — The main script. Read the function names and docstrings first, then the main() function.
3. **docker-launcher/Dockerfile** — Understand what tools are installed and in what order.

4. **Examples/Half_Adder/** — Look at all the files in this directory to understand what inputs and outputs the flow expects.
5. **src/maker/NgVeri.py** — Understand how the existing NgVeri tab works, as OpenROAD follows a similar pattern.

7.4 Common Issues and Troubleshooting

- **"OpenROAD not found" error** — Make sure you have cloned and built OpenROAD-flow-scripts in your home directory. Check that `~/OpenROAD-flow-scripts/` exists.
- **"Netlist not found" error** — You must run "Convert KiCad to Ngspice" in eSim before clicking the OpenROAD button. The `.cir.out` file must exist in the project folder.
- **"Verilog file not found" error** — Place your `.v` file in the same directory as the `.cir.out` file, or in your home directory. The script searches both locations.
- **Docker permission error** — Run `sudo usermod -aG docker $USER` and then log out and log back in. The group change does not take effect until you re-login.
- **OpenROAD GUI does not open** — Check that the flow at least completed synthesis. Look in `~/OpenROAD-flow-scripts/flow/logs/sky130hd/` for error logs.

Chapter 8

Conclusion and Future Work

8.1 Conclusion

This internship successfully delivered the foundational infrastructure for integrating eSim with the OpenROAD physical design flow. Before this work, eSim users had no path from their circuit designs to physical chip layouts. After this work, the complete pipeline exists: draw a circuit in eSim, simulate it, click one button, and watch the OpenROAD flow synthesize, place, and route the design on the SkyWater 130nm PDK.

The key contributions of this internship are:

1. **netlist_to_verilog.py** — A 250+ line Python script that intelligently bridges eSim's SPICE world with OpenROAD's Verilog world, handling module name sanitization, clock detection, config generation, flow execution, and GUI launching automatically.
2. **OpenROAD.py** — A clean PyQt5 GUI bridge that connects the eSim button press to the conversion script with proper error handling and user feedback.
3. **Docker Integration** — Extended the existing eSim Dockerfile to include OpenROAD, enabling one-command deployment of the complete integrated environment.
4. **Portability Fixes** — Fixed hardcoded paths in Maker.py and NgVeri.py that would have prevented the code from running on any machine other than the original developer's.
5. **Example Circuits** — Three working example circuits (Half Adder, Full Adder, Counter) that demonstrate and validate the integration.
6. **Documentation** — Complete README files and this report that explain the integration in detail for future interns.

All of this work is available publicly as Pull Request #473 on FOSSEE/eSim and as the dedicated plugin repository at https://github.com/FOSSEE/eSim-to-OpenROAD_Design_Flow_Plugin.

8.2 Future Work

The following directions are recommended for future interns who continue this project:

- **Complete SPICE-to-Verilog Parser** — Implement a proper parser that reads the `.cir.out` netlist and generates the `.v` file automatically, eliminating the need for users to provide the Verilog file manually.
- **GUI Integration** — Wire the OpenROAD-GDSII button properly into the eSim main window GUI in `src/frontEnd/`.
- **More Example Circuits** — Add examples for flip-flops, multiplexers, decoders, ALUs, and other common digital circuits.
- **PDK Selection** — Allow users to choose between sky130hd and other open PDKs like GF180MCU from the eSim interface.
- **Flow Result Display** — Show timing reports, area reports, and DRC results directly inside the eSim GUI after the OpenROAD flow completes.
- **Analog-Digital Boundary** — Develop a methodology for handling mixed-signal designs where some components are analog (handled by Ngspice) and some are digital (handled by OpenROAD).

References

1. FOSSEE eSim Repository: https://github.com/FOSSEE/eSim
2. PR #473 — eSim to OpenROAD Integration: https://github.com/FOSSEE/eSim/pull/473
3. eSim to OpenROAD Plugin Repository: https://github.com/FOSSEE/eSim-to-OpenROAD_Design_Flow_Plugin
4. OpenROAD Flow Scripts: https://github.com/The-OpenROAD-Project/OpenROAD-flow-scri
5. OpenROAD Flow Tutorial: https://openroad-flow-scripts.readthedocs.io/en/latest/tutorials/FlowTutorial.html
6. SkyWater 130nm PDK: https://github.com/google/skywater-pdk
7. Docker Documentation: https://docs.docker.com
8. KiCad EDA: https://www.kicad.org
9. Ngspice Manual: http://ngspice.sourceforge.net/docs.html
10. FOSSEE IIT Bombay: https://fossee.in