eSim Semester Long Internship

Spring 2026

On

Designing Integrated Circuits in eSim

Submitted by

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Acknowledgment

I would like to express my sincere gratitude to the FOSSEE team, IIT Bombay, for providing me the opportunity to be part of the FOSSEE internship programme and for supporting open-source engineering tool development at IIT Bombay.

I sincerely thank my mentors Mr. Sumanto Kar and Mr. Varad Vilasrao Patil for their continuous support, technical guidance, and encouragement throughout this project.

I also thank the faculty members and management of Thapathali Engineering Institute for their support and encouragement.

This internship has been an enriching experience, allowing me to work with open-source EDA tools, develop IC subcircuits in eSim, and gain exposure to real-world circuit modelling and simulation workflows.

Executive Summary

This report documents the work carried out during the Spring 2026 FOSSEE Semester Long Internship, hosted by IIT Bombay, on the theme of *Designing Integrated Circuits in eSim*. The objective of the internship was to extend eSim's open-source subcircuit library with accurately modelled, datasheet-verified digital logic devices spanning several TTL and CMOS families.

Ten integrated circuits were selected, modelled as hierarchical subcircuits using eSim's schematic editor, and validated against their respective manufacturer datasheets. Each device was built using a consistent set of generic logic-gate and flip-flop primitives, and its behaviour was confirmed through NgSpice-based transient simulation against the datasheet's function table. The contributed devices – counters, registers, latches, a bus buffer, a 4-bit ALU, a J-K flip-flop, a register file, and a multiplexer – collectively cover a representative cross-section of the building blocks used in digital system design.

The remainder of this report is organised as follows: Chapters 1–3 introduce FOSSEE, eSim, and the problem statement and methodology. Chapters 4–13 document each contributed IC in turn, giving its general description, key features, applications, subcircuit symbol, datasheet pin diagram, test circuit, function table, and simulated output waveforms. Chapter 14 concludes the report and outlines directions for future work, and Chapter 15 summarises the complete list of contributions.

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Chapter 1

Introduction

1.1 FOSSEE

FOSSEE (Free/Libre and Open Source Software for Education) is an initiative based at IIT Bombay aimed at promoting the use of open-source software in education and research. It was established to reduce dependency on proprietary software and to encourage open-source alternatives. FOSSEE offers documentation, tutorials, workshops, and hands-on training to empower students, educators, and professionals.

1.2 eSim

eSim, created by the FOSSEE project at IIT Bombay, is a versatile open-source software tool for circuit design and simulation. It combines multiple open-source packages into one cohesive platform, making it easier to design, simulate, and analyse electronic circuits. eSim is particularly useful as an affordable alternative to proprietary EDA tools, and includes a subcircuit feature that enables complex hierarchical circuit design.

1.3 NgSpice

NgSpice is an open-source SPICE simulator for electric and electronic circuits. It simulates circuit elements such as JFETs, BJTs, MOSFETs, passive components (R, L, C), and diodes. Digital, analog, and mixed-signal circuits can all be simulated. Users input circuits as netlists, and the output consists of voltage and current waveforms or saved data files.

1.4 Makechip

Makechip is a platform for digital circuit design offering browser-based and desktop environments for coding, compiling, simulating, and debugging Verilog designs. eSim interfaces with Makechip via a Python-based application called Makechip-App.

Chapter 2

Features of eSim

The objective behind eSim is to provide an open-source EDA solution for electronics and electrical engineers. It supports schematic creation, PCB design, and circuit simulation (analog, digital, and mixed-signal). Key features include:

1. **Schematic Creation:** An easy-to-use graphical interface for drawing circuit schematics with drag-and-drop components.
2. **Circuit Simulation:** Supports SPICE-based transient, AC, and DC analysis with an integrated waveform viewer.
3. **PCB Design:** A PCB layout editor with DRC (Design Rule Check) and Gerber file export.
4. **Subcircuit Feature:** Enables modular and hierarchical design by integrating reusable subcircuits.
5. **Open Source Integration:** Integrates KiCad, NgSpice, and GHDL for a comprehensive, free EDA suite.

Chapter 3

Problem Statement

To design and develop various digital integrated circuit models in the form of sub-circuits using device model files already present in the eSim library. These IC models should be useful for future circuit design purposes by developers and users once they are successfully integrated into the eSim sub-circuit library.

3.1 Approach

The approach involved a systematic process leveraging datasheets from leading IC manufacturers such as Texas Instruments and other semiconductor vendors.

1. **Analysing Datasheets:** In-depth review of datasheets to identify ICs suitable for eSim, including scrutinising internal logic, pin configurations, and truth tables.
2. **Subcircuit Creation:** Modelling selected ICs as sub-circuits within eSim using available device model files, and creating accurate symbol and pin diagrams as per the datasheet.
3. **Test Circuit Design:** Designing test circuits based on datasheets to verify the functionality of each sub-circuit.
4. **Schematic Testing:** Running simulations, generating waveforms, and iterating until outputs matched expected results.

Chapter 4

74LS93

Primary reference: Texas Instruments SN54LS90/92/93, SN74LS90/92/93 datasheet

4.1 General Description

The 74LS93 is a 4-bit binary ripple counter from the LS (Low-power Schottky) TTL family. It internally consists of a divide-by-2 section (driven by input CKA) and a divide-by-8 section (driven by input CKB), which can be used independently or cascaded together (by externally connecting Q_A to CKB) to form a divide-by-16 counter. Two active-HIGH master-reset inputs (R0(1) and R0(2)) reset all four flip-flops asynchronously when both are HIGH [3].

4.2 Key Features

- 4-bit ripple counter: separate divide-by-2 and divide-by-8 sections
- Cascadable to form a divide-by-16 counter
- Dual active-HIGH asynchronous master-reset inputs
- Toggles on the HIGH-to-LOW clock transition
- Standard TTL voltage operation (4.75 V – 5.25 V)

4.3 Applications

- Frequency division circuits
- Digital clocks and event counters
- Timing generation in digital systems
- Building block for higher modulo counters

4.4 Subcircuit Symbol

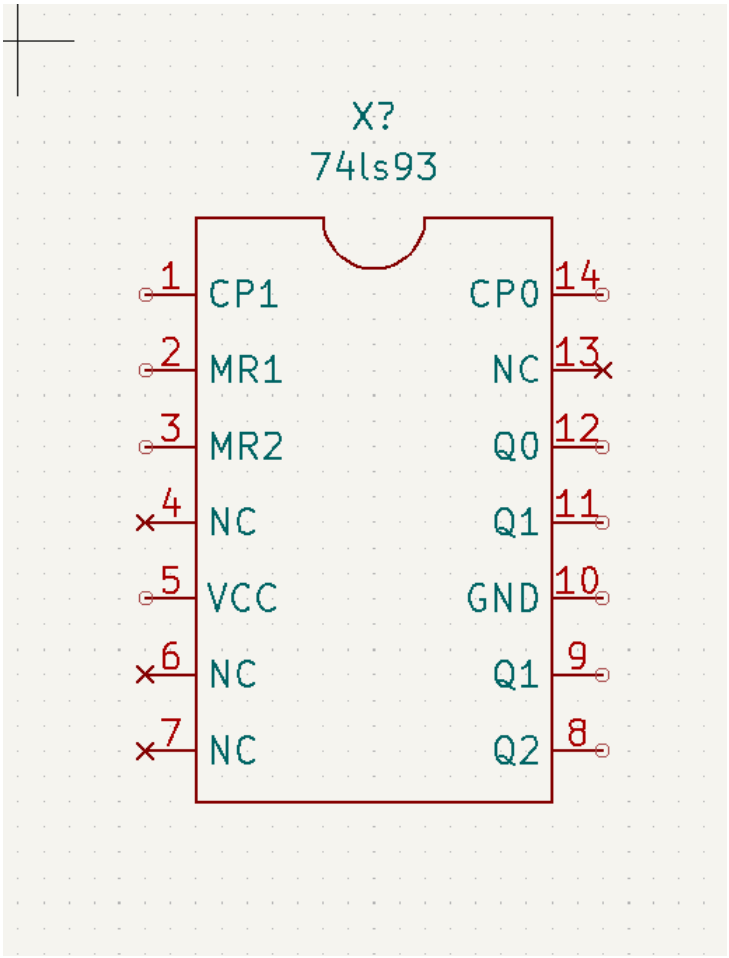

Figure 4.1: Subcircuit Symbol of the 74LS93

4.5 Subcircuit Schematic Diagram

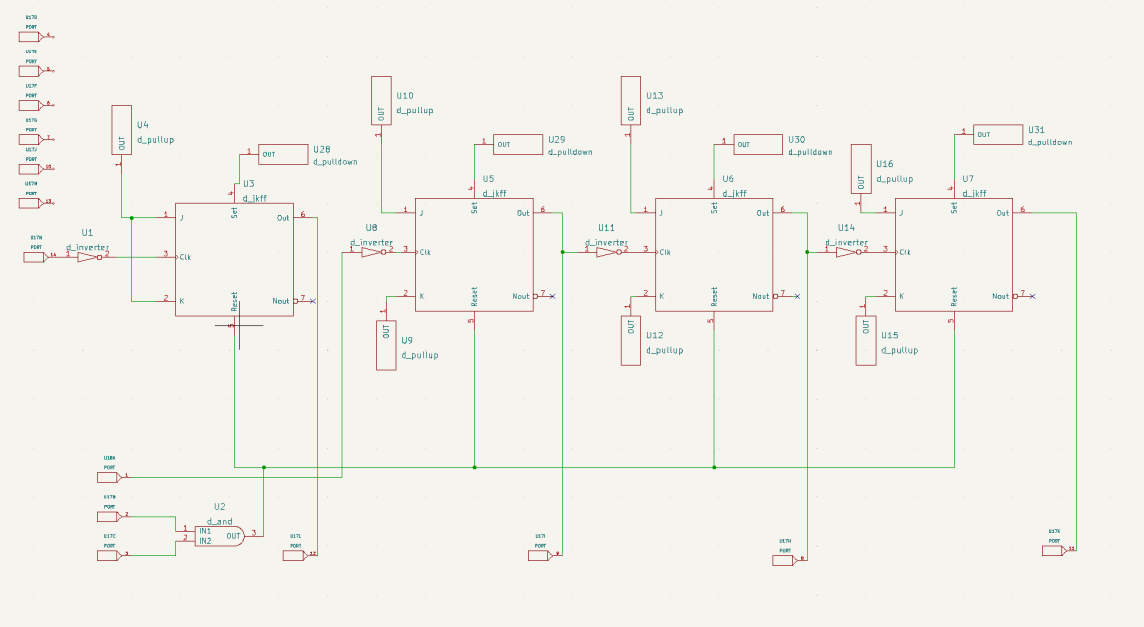

Figure 4.2: Subcircuit Schematic (internal gate-level structure) of the 74LS93

4.6 Test Circuit

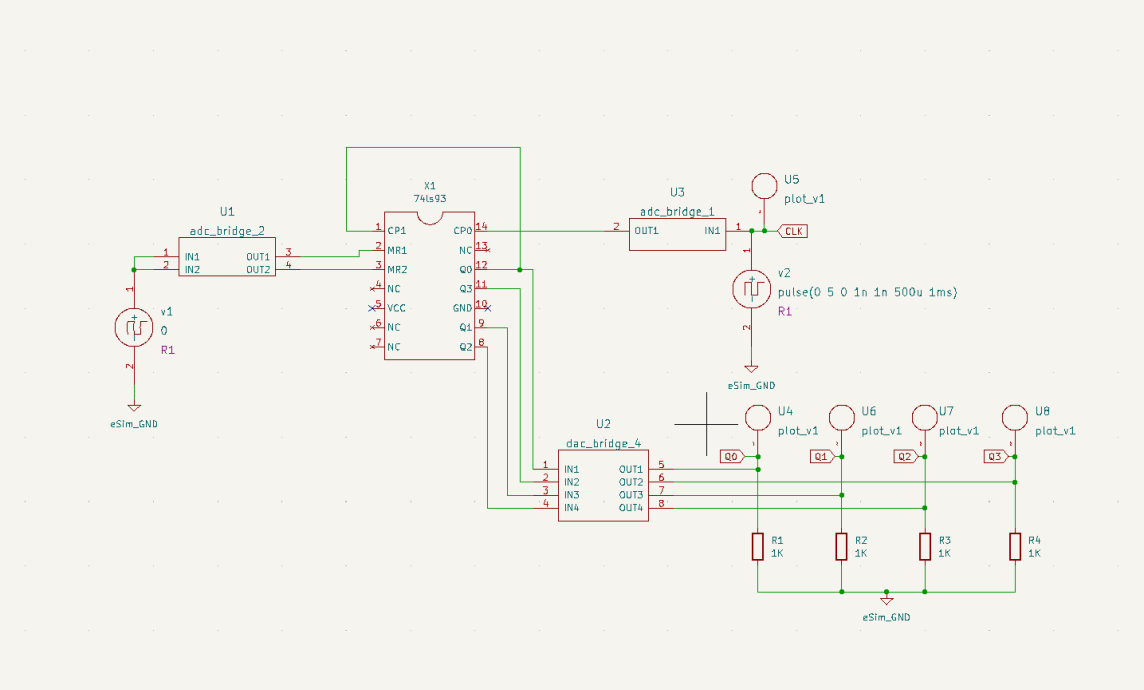

Figure 4.3: Test Circuit of the 74LS93

4.7 Function Table

Reset Inputs (R0(1), R0(2))	Output State
Both HIGH	$Q_A = Q_B = Q_C = Q_D = 0$
At least one LOW	Counts (reset inactive)

Table 4.1: Function Table of the 74LS93

4.8 Output Plot

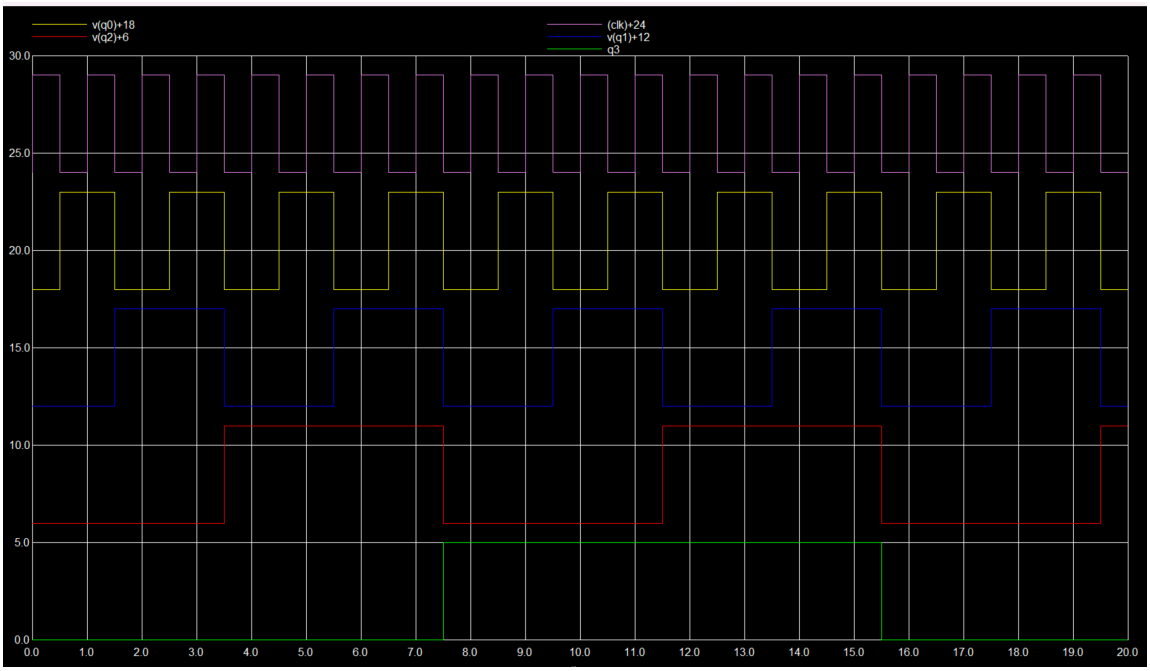

Figure 4.4: Output of the 74LS93

Chapter 5

74LS175

Primary reference: Texas Instruments SN54/74LS174, SN54/74LS175 datasheet

5.1 General Description

The 74LS175 is a quad D-type positive-edge-triggered flip-flop from the LS TTL family. All four flip-flops share a common clock and a common active-LOW asynchronous clear. Each flip-flop provides both true (Q) and complementary ($\overline{Q}$) outputs, making it suitable for building registers and buffered latch banks [4].

5.2 Key Features

- Four D-type positive-edge-triggered flip-flops
- Common active-LOW clear (CLR) resets all outputs simultaneously
- Complementary Q and $\overline{Q}$ outputs on every flip-flop
- Single common clock input for synchronous operation
- Standard TTL voltage operation

5.3 Applications

- General-purpose data storage registers
- Buffer registers between logic stages
- Pattern generators
- Synchronising asynchronous signals

5.4 Subcircuit Symbol

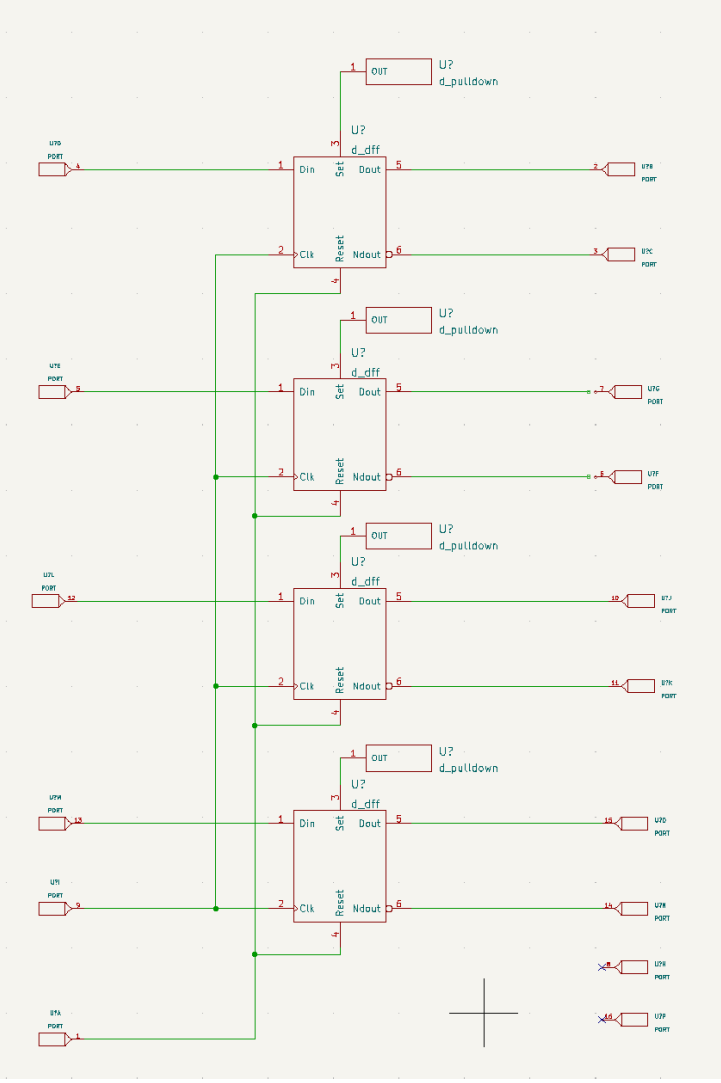

Figure 5.1: Subcircuit Symbol of the 74LS175

5.5 Datasheet Pin Diagram

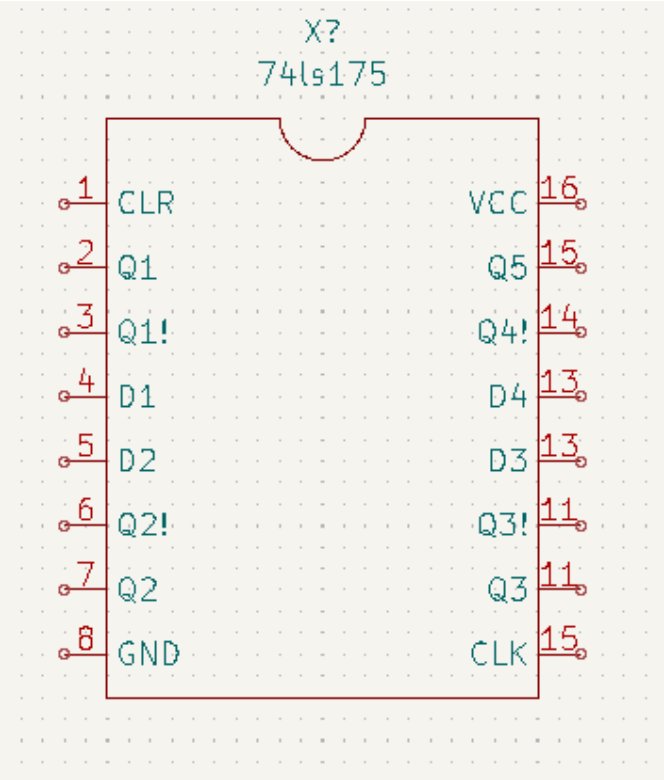

Figure 5.2: Pin Diagram of the 74LS175

5.6 Test Circuit

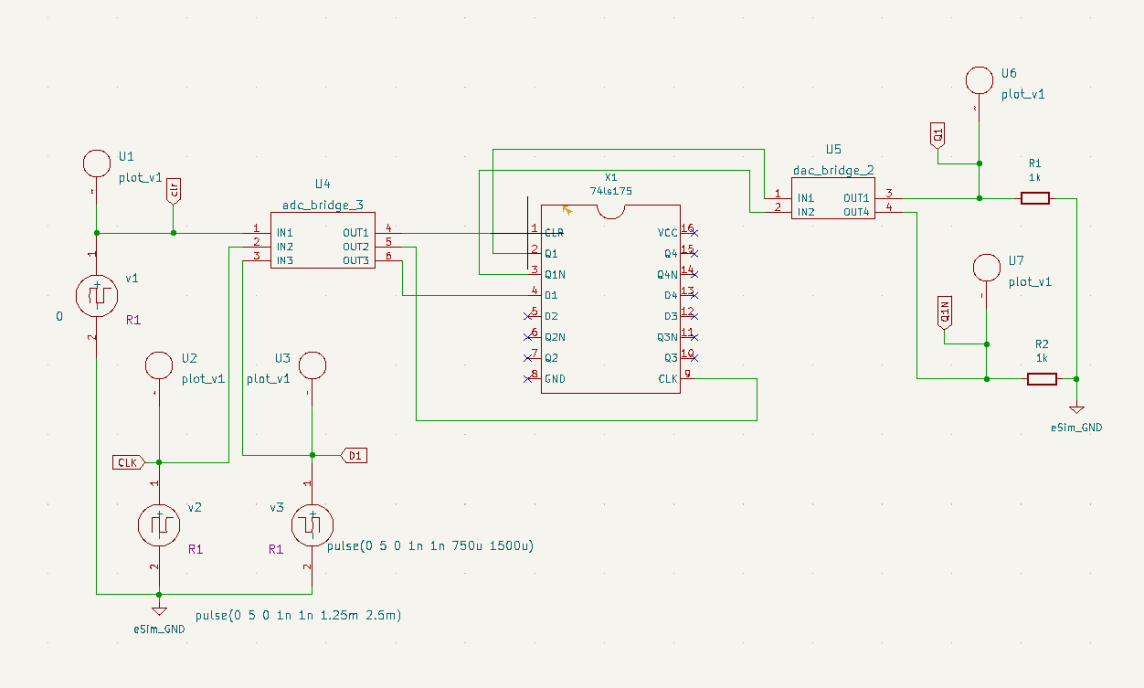

Figure 5.3: Test Circuit of the 74LS175

5.7 Function Table

Clear	**Clock**	**D**	**Output (Q)**
L	X	X	L
H	↑	H	H
H	↑	L	L
H	L	X	No change

Table 5.1: Function Table of the 74LS175

5.8 Output Plot

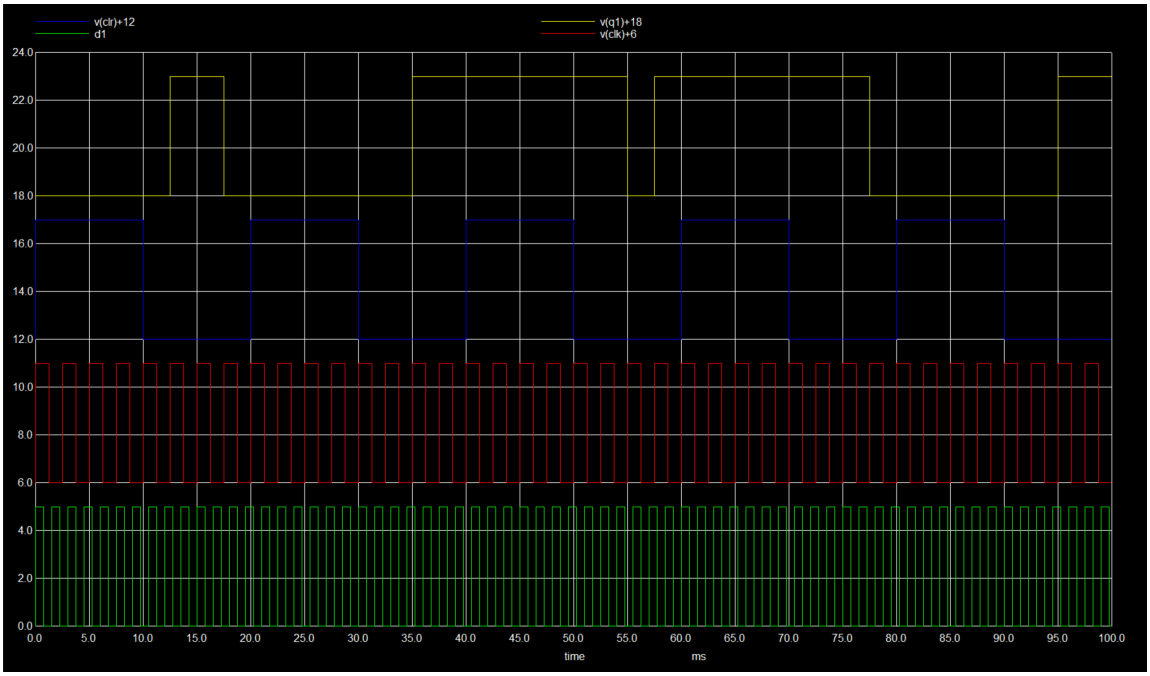

Figure 5.4: Output of the 74LS175

Chapter 6

74LS374

Primary reference: Texas Instruments SN54/74LS373, SN54/74LS374 datasheet

6.1 General Description

The 74LS374 is an octal D-type edge-triggered flip-flop with 3-state outputs from the LS TTL family. Data on the eight D inputs is stored on the LOW-to-HIGH transition of the clock, and a single active-LOW output-enable (OE) input places all eight outputs in a high-impedance state when HIGH, allowing the device to drive a shared data bus [5].

6.2 Key Features

- Eight positive-edge-triggered D-type flip-flops
- 3-state outputs for bus-oriented applications
- Single active-LOW output-enable input
- Broadside data storage in one clock edge
- Standard TTL voltage operation

6.3 Applications

- Microprocessor address/data latching
- Bus-oriented register applications
- Pipeline registers
- I/O port expansion

6.4 Subcircuit Symbol

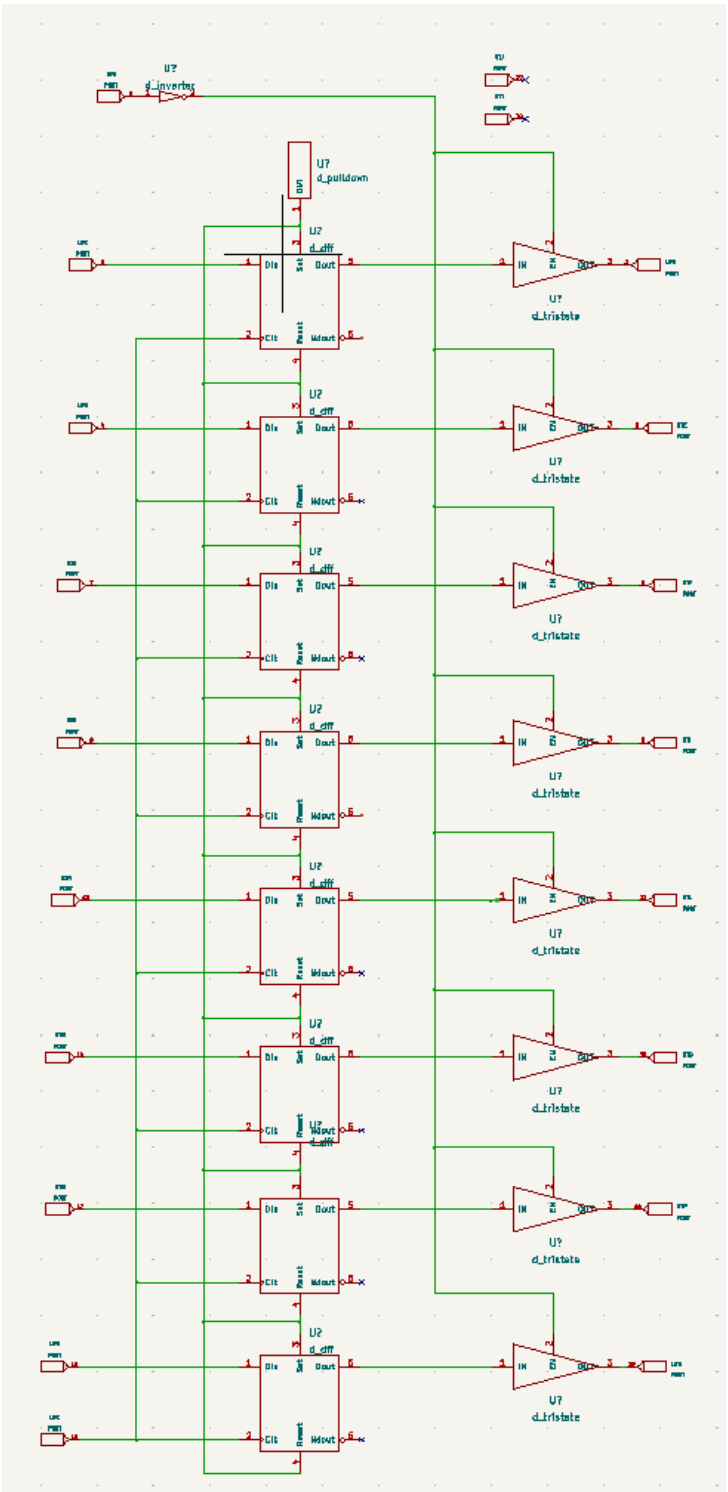

Figure 6.1: Subcircuit Symbol of the 74LS374

6.5 Datasheet Pin Diagram

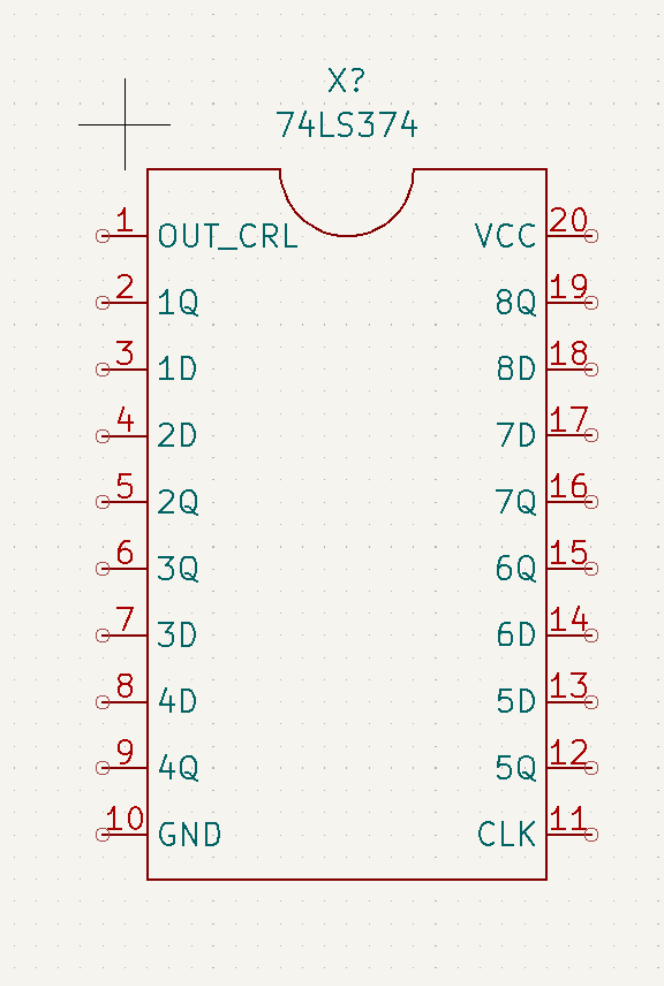

Figure 6.2: Pin Diagram of the 74LS374

6.6 Test Circuit

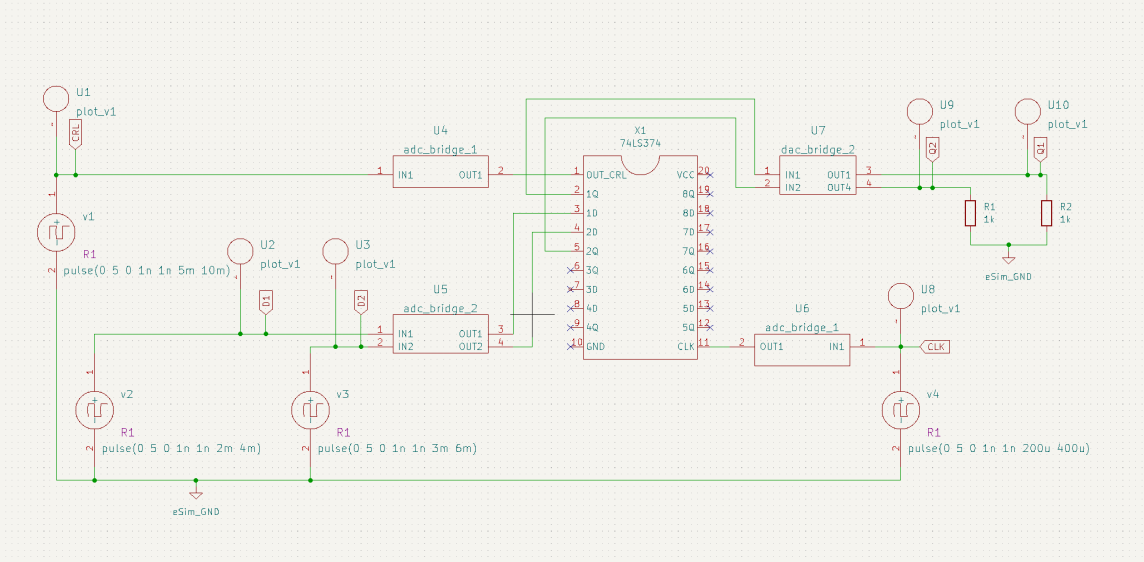

Figure 6.3: Test Circuit of the 74LS374

6.7 Function Table

OE	Clock	D	Output
L	↑	H	H
L	↑	L	L
H	X	X	Hi-Z

Table 6.1: Function Table of the 74LS374

6.8 Output Plot

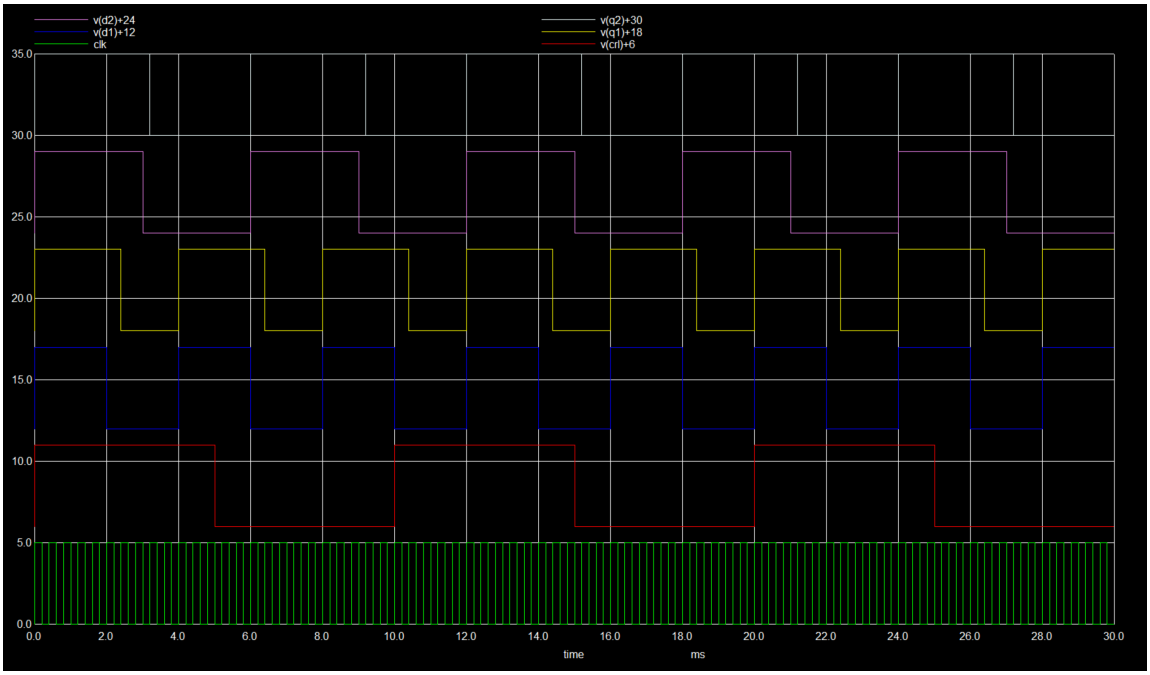

Figure 6.4: Output of the 74LS374

Chapter 7

CD4024BC

Primary reference: Texas Instruments CD4020B, CD4024B, CD4040B datasheet

7.1 General Description

The CD4024BC is a 7-stage ripple-carry binary counter from the CMOS 4000B-series family. A single clock input drives all seven internal divide-by-2 stages in cascade, and a single active-HIGH asynchronous reset clears every stage to zero. Only three of the seven outputs (Q1–Q3) are typically brought out along with the higher-order taps Q4–Q7 required by the application [6].

7.2 Key Features

- 7-stage (divide-by-128) ripple binary counter
- Single-phase clock input, negative-edge triggered
- Asynchronous active-HIGH reset
- Wide supply voltage range: 3 V – 18 V
- Low power CMOS operation

7.3 Applications

- Frequency division / clock generation
- Timers and real-time clock circuits
- Digital watches and counting instruments
- General-purpose event counting

7.4 Subcircuit Symbol

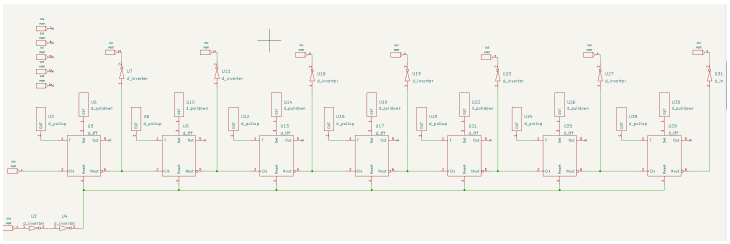

Figure 7.1: Subcircuit Symbol of the CD4024BC

7.5 Datasheet Pin Diagram

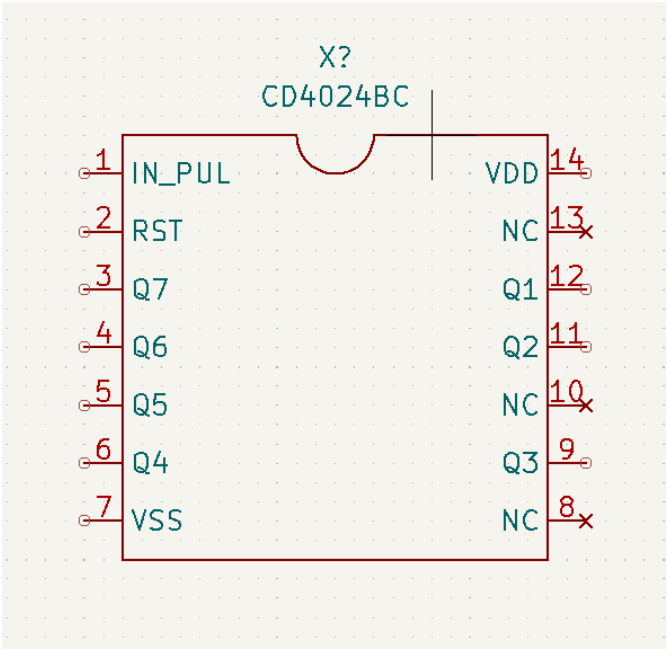

Figure 7.2: Pin Diagram of the CD4024BC

7.6 Test Circuit

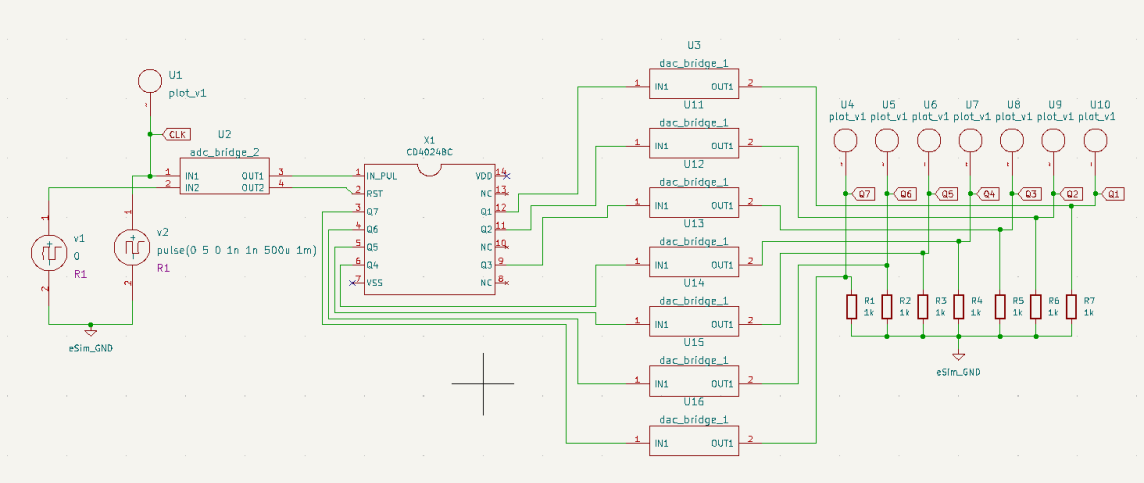

Figure 7.3: Test Circuit of the CD4024BC

7.7 Function Table

Reset	Action
H	All outputs = 0
L	Counts on falling edge of clock

Table 7.1: Function Table of the CD4024BC

7.8 Output Plot

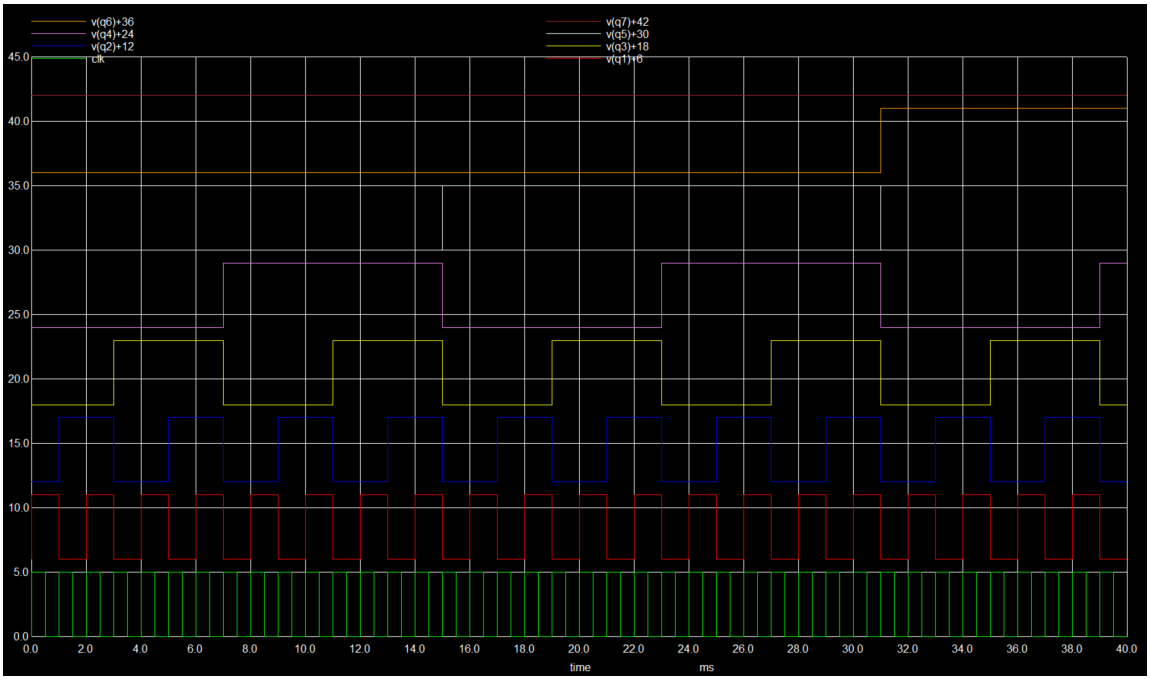

Figure 7.4: Output of the CD4024BC

Chapter 8

SN74LS244

Primary reference: Texas Instruments SN54/74LS240, SN54/74LS241, SN54/74LS244 datasheet

8.1 General Description

The SN74LS244 is an octal buffer/line driver with 3-state outputs from the LS TTL family. It is organised as two independent groups of four non-inverting buffers, each group controlled by its own active-LOW output-enable input ($1\overline{OE}$, $2\overline{OE}$), making it well suited for bidirectional and high-drive bus interface applications [7].

8.2 Key Features

- Octal non-inverting buffer, organised as two groups of four
- Independent active-LOW output-enable per group
- High output drive current for bus/line driving
- 3-state outputs for shared-bus operation
- Standard TTL voltage operation

8.3 Applications

- Bus interfacing and line driving
- Address/data buffering in microprocessor systems
- Clock distribution buffering
- Memory and peripheral chip-select buffering

Subcircuit Assets

The SN74LS244 subcircuit symbol, test circuit, and simulated output plots had not yet been exported from eSim at the time this report was compiled, and so are not reproduced here. Once available, they can be inserted using the same `\reportfig` command employed throughout the other chapters, for example:

```
\reportfig{figs/ls244_symbol.png}{0.6}{Subcircuit Symbol of the SN74LS244}
```

The functional behaviour of the device, summarised in the function table below, was nonetheless verified against the datasheet.

8.4 Function Table

$\overline{OE}$	**Input (A)**	**Output (Y)**
L	L	L
L	H	H
H	X	Hi-Z

Table 8.1: Function Table of the SN74LS244

Chapter 9

SN74S181

Primary reference: Texas Instruments SN54/74LS181, SN54/74S181 Arithmetic Logic Unit/Function Generator datasheet

9.1 General Description

The SN74S181 is a 4-bit Arithmetic Logic Unit (ALU) built with Schottky TTL technology. It performs 16 logic functions and 16 arithmetic operations on two 4-bit operands (A and B), selected by four mode/select lines (S0–S3) and a mode-control input (M). It also provides carry generate/propagate outputs (G, P) and a comparator output (A = B) for building fast lookahead-carry adder/ALU systems [8].

9.2 Key Features

- Performs 16 arithmetic and 16 logic operations on 4-bit words
- Full carry lookahead generate (G) and propagate (P) outputs
- Mode control input to select arithmetic or logic operation
- Ripple carry input/output for cascading multiple ALU slices
- A = B comparator output

9.3 Applications

- CPU/ALU datapath design in digital computers
- High-speed arithmetic and logic processing
- Cascadable multi-bit ALU systems using carry lookahead
- Digital comparators

9.4 Subcircuit Symbol

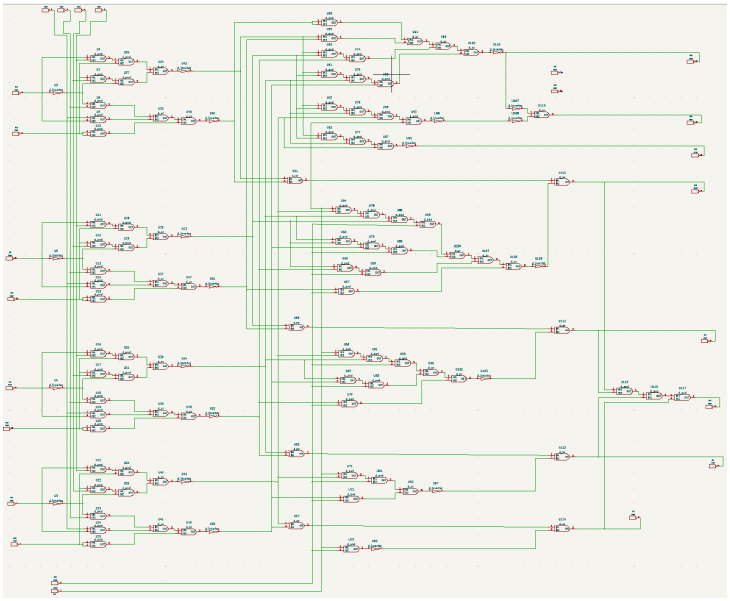

Figure 9.1: Subcircuit Symbol of the SN74S181

9.5 Datasheet Pin Diagram

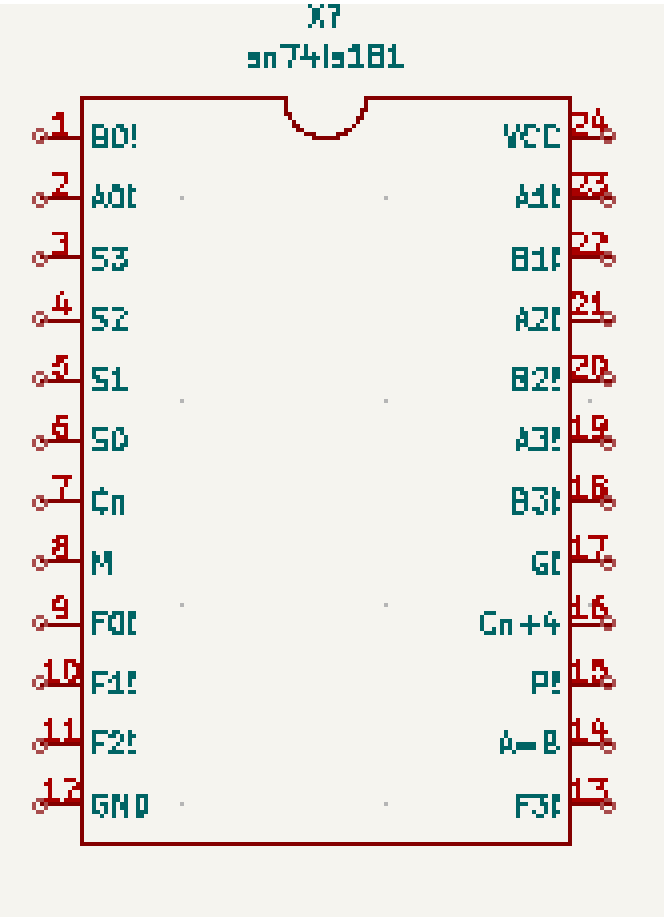

Figure 9.2: Pin Diagram of the SN74S181

9.6 Test Circuit

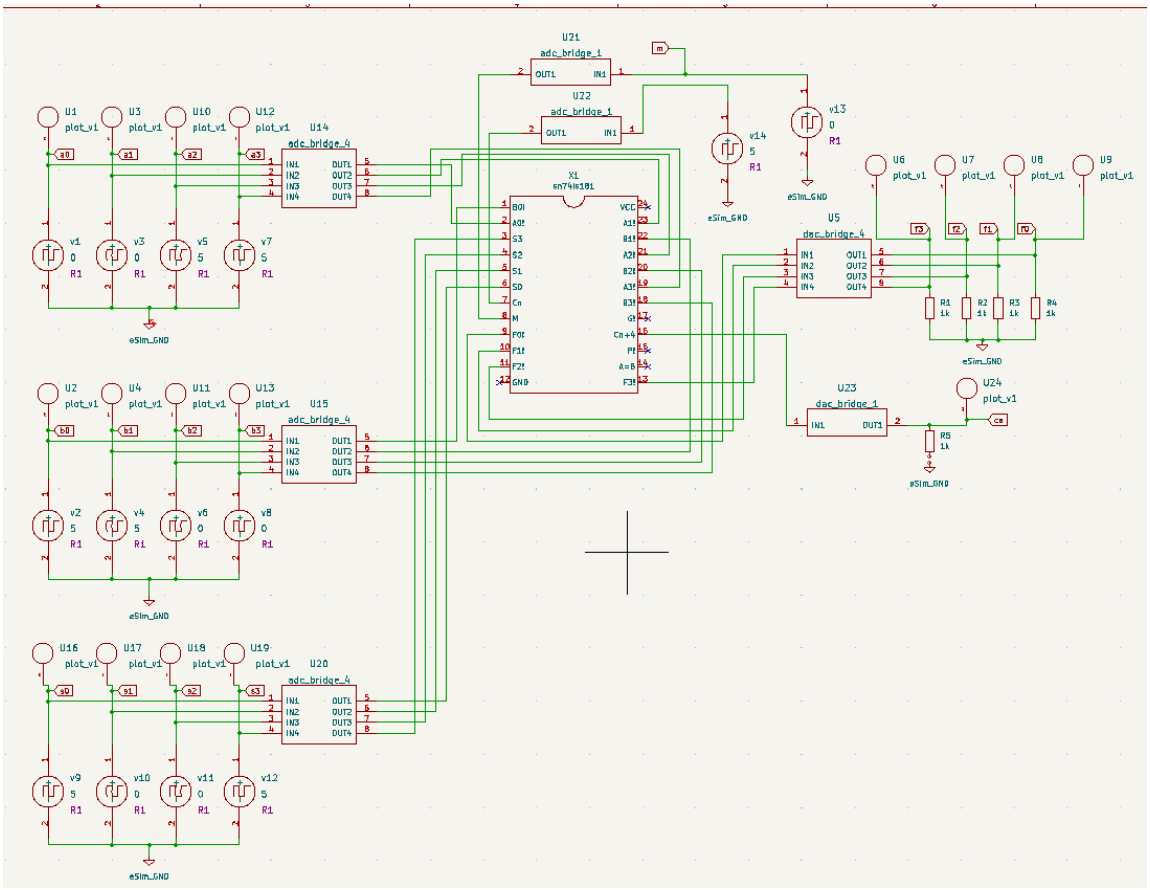

Figure 9.3: Test Circuit of the SN74S181

9.7 Function Table

Mode (M)	S3S2S1S0	Operation
H (Logic)	0000	$F = \overline{A}$
H (Logic)	1111	$F = A$
L (Arithmetic)	0000	$F = A$ (plus carry)
L (Arithmetic)	1001	$F = A + B$ (plus carry)

Table 9.1: Abridged Function Table of the SN74S181 (see datasheet for the complete 32-row table)

9.8 Output Plots

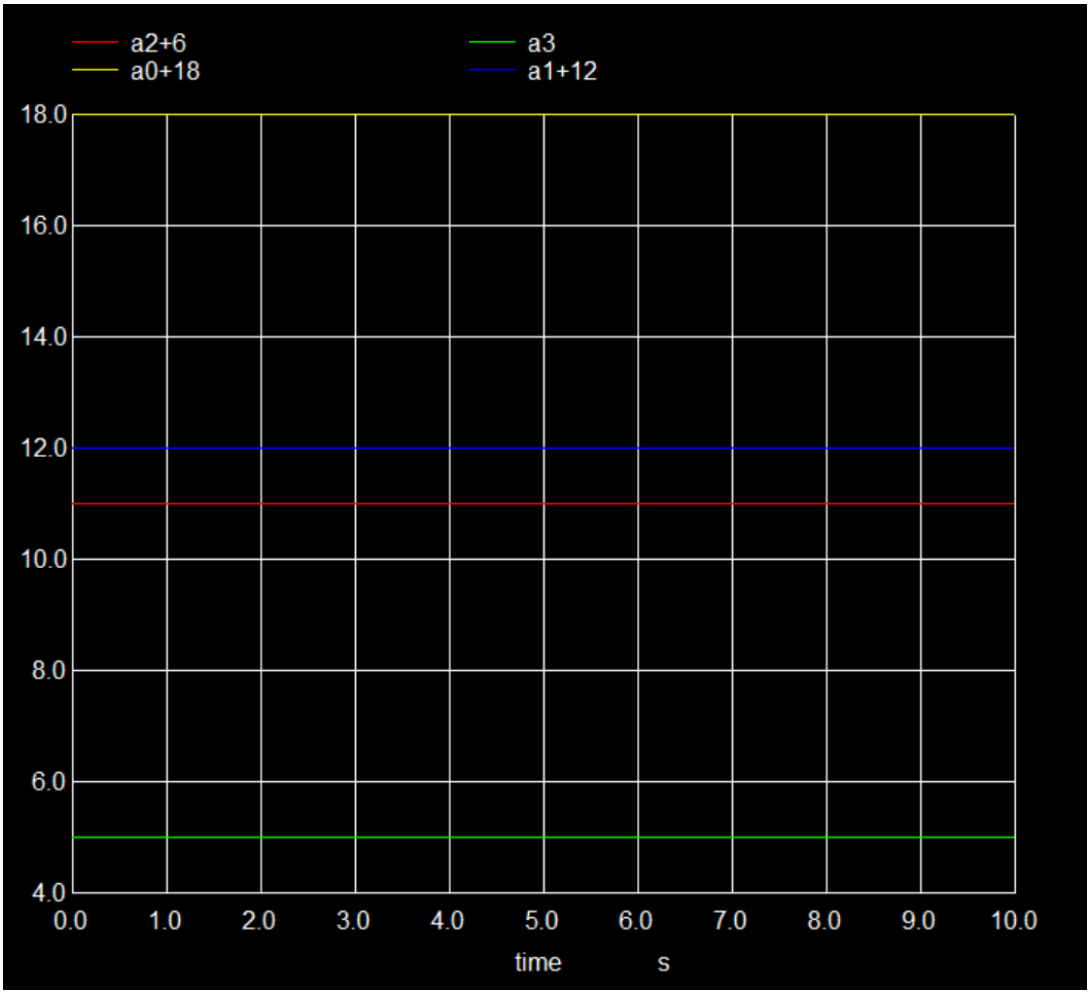

Figure 9.4: Output Plot A – Operand / Result Waveform of the SN74S181

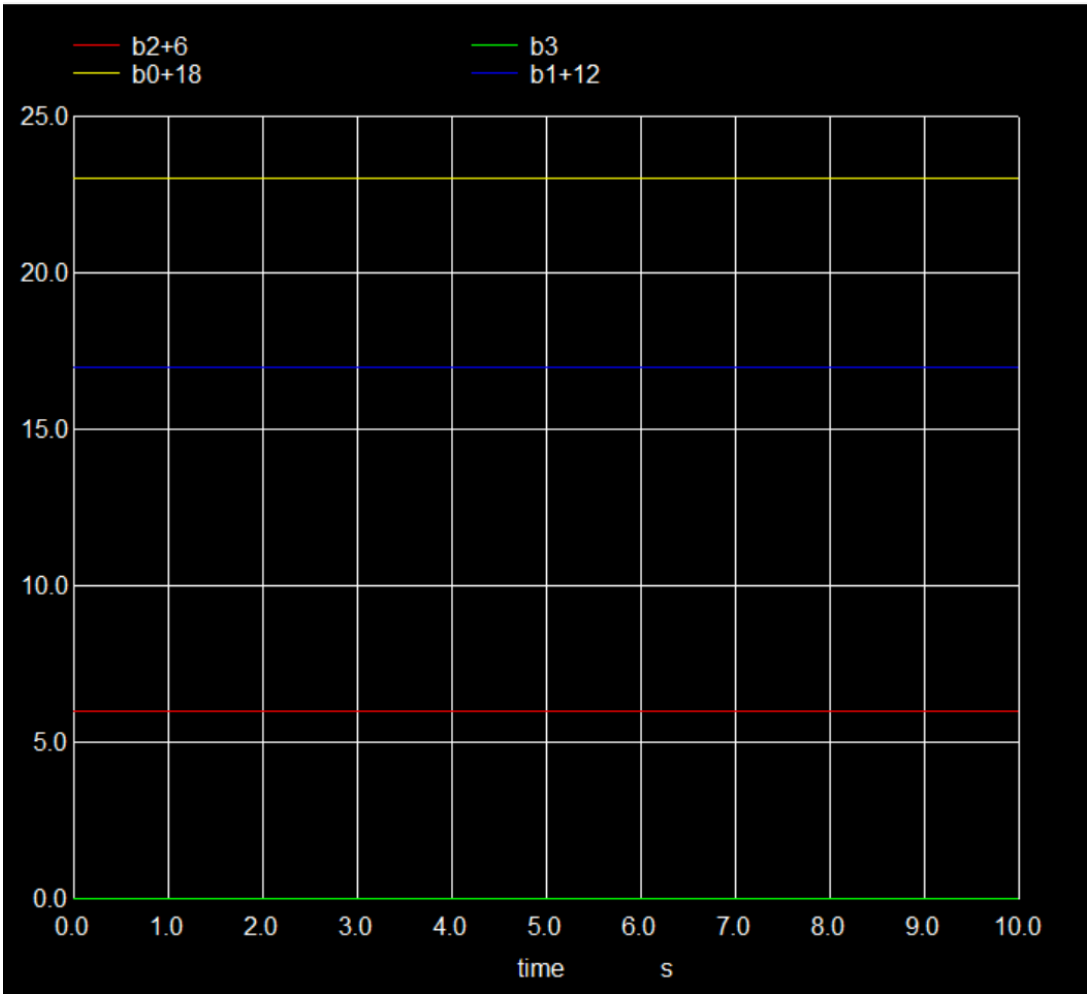

Figure 9.5: Output Plot B – Operand / Result Waveform of the SN74S181

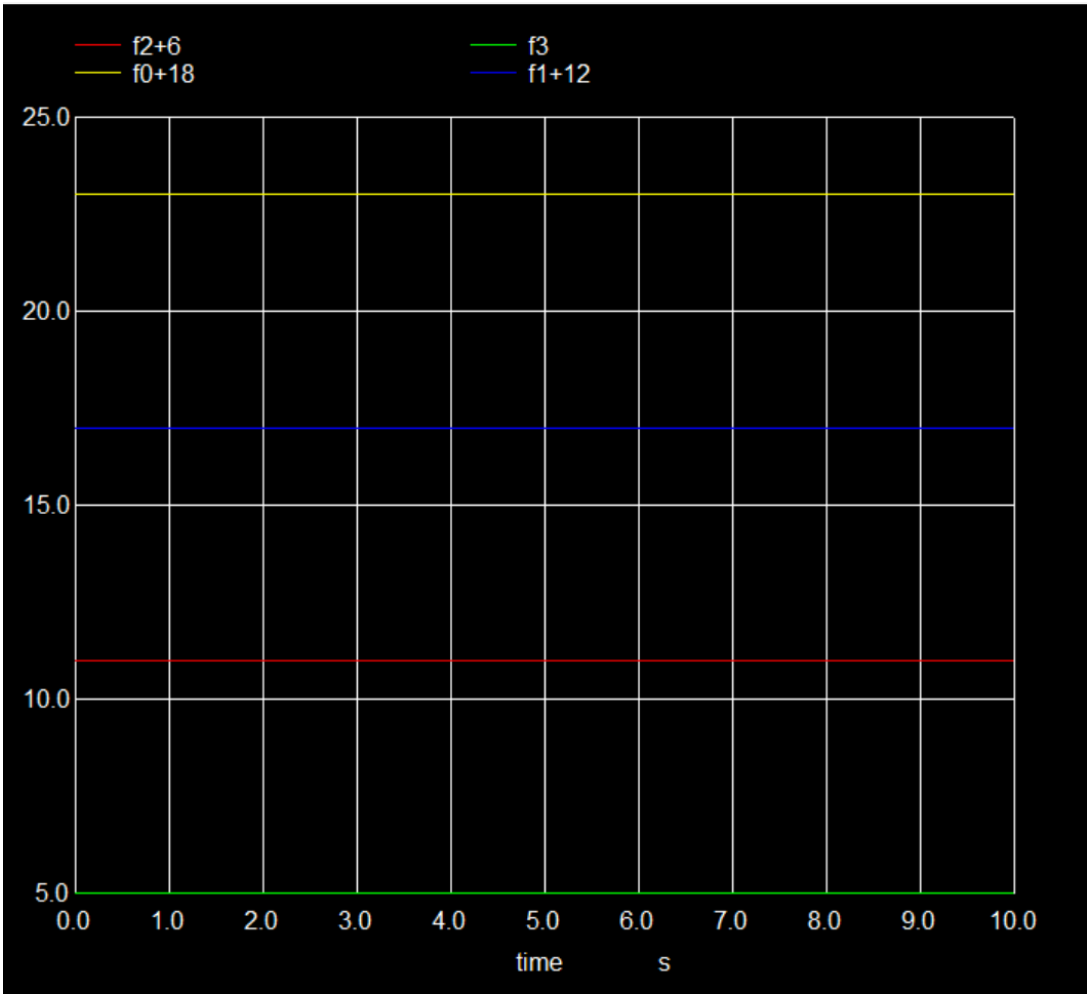

Figure 9.6: Output Plot F – Function Output of the SN74S181

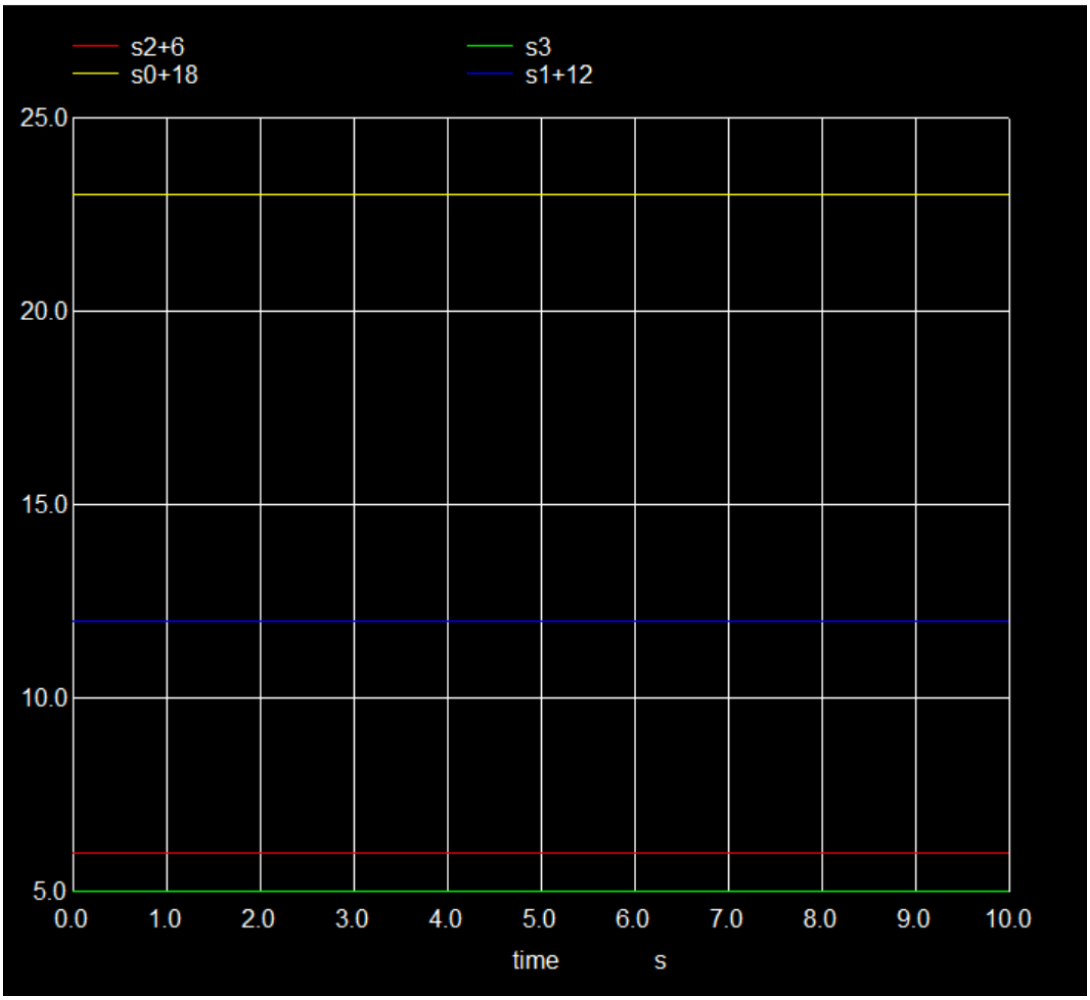

Figure 9.7: Output Plot S – Select/Mode Control Waveform of the SN74S181

Chapter 10

SN5470

Primary reference: Texas Instruments SN5470, SN7470 AND-Gated J-K Flip-Flop datasheet

10.1 General Description

The SN5470 is an AND-gated, positive-edge-triggered J-K flip-flop from the standard TTL logic family (the military-temperature-range counterpart of the SN7470). Each of the J and K inputs is formed from three AND-ed input lines (J1J2J3 and K1K2K3), and the device offers direct active-LOW preset and clear inputs in addition to the clocked J-K behaviour [9].

10.2 Key Features

- AND-gated J and K inputs (three inputs ANDed per side)
- Positive-edge-triggered clocking
- Direct active-LOW preset and clear inputs
- Complementary Q and $\overline{Q}$ outputs
- Standard TTL voltage operation

10.3 Applications

- Control logic requiring AND-gated enable conditions
- Shift registers and counters
- General sequential logic design
- Frequency division (toggle mode)

10.4 Subcircuit Symbol

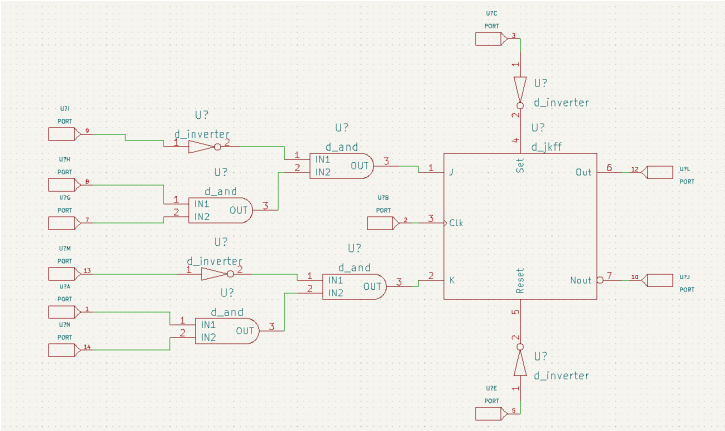

Figure 10.1: Subcircuit Symbol of the SN5470

10.5 Datasheet Pin Diagram

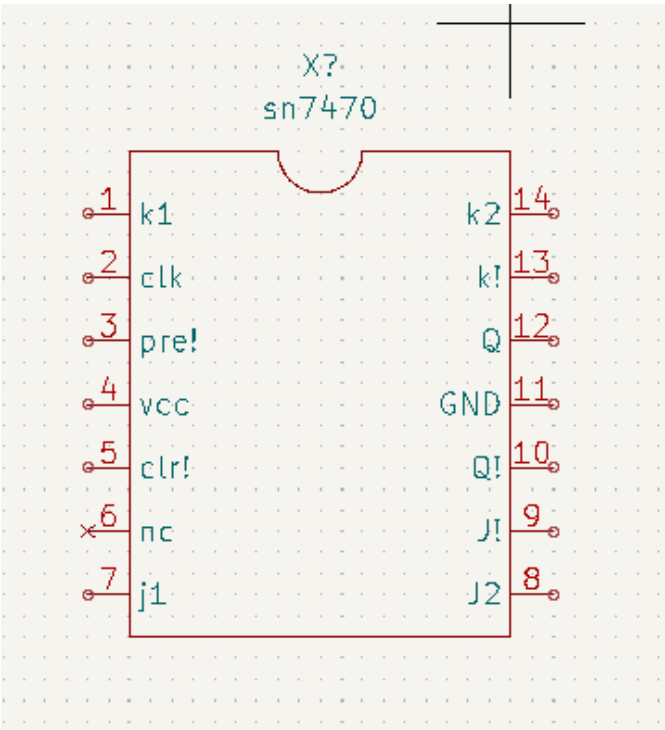

Figure 10.2: Pin Diagram of the SN5470

10.6 Test Circuit

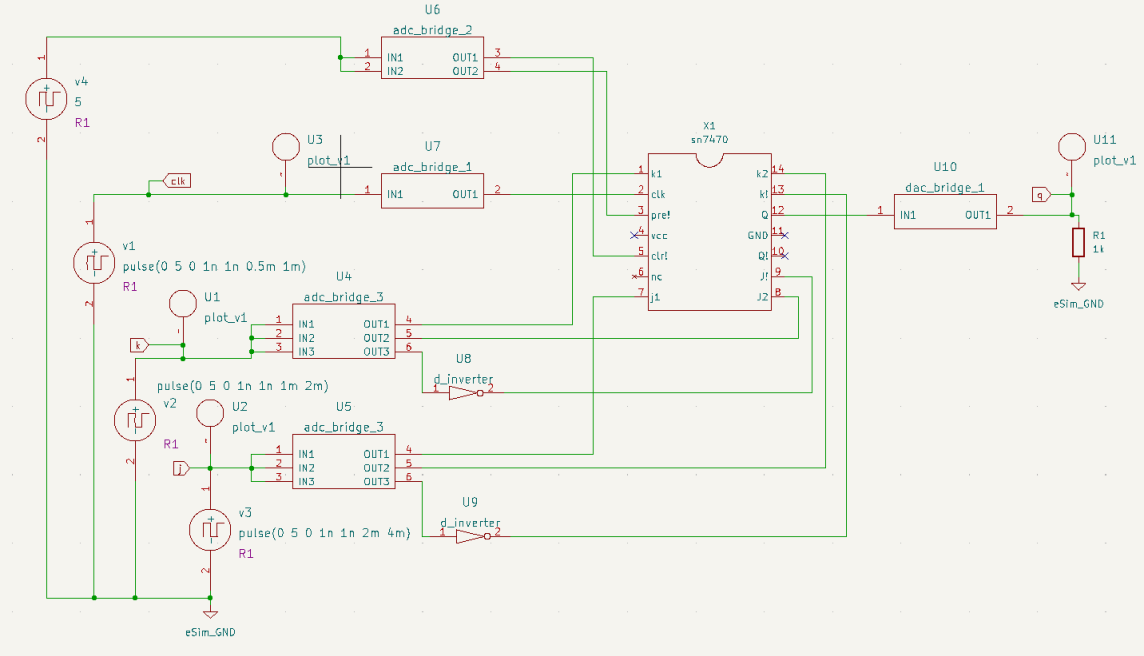

Figure 10.3: Test Circuit of the SN5470

10.7 Function Table

Preset	Clear	Clock	Action
L	H	X	Q = H (asynchronous preset)
H	L	X	Q = L (asynchronous clear)
H	H	↑	Q toggles per J-K truth table

Table 10.1: Function Table of the SN5470

10.8 Output Plot

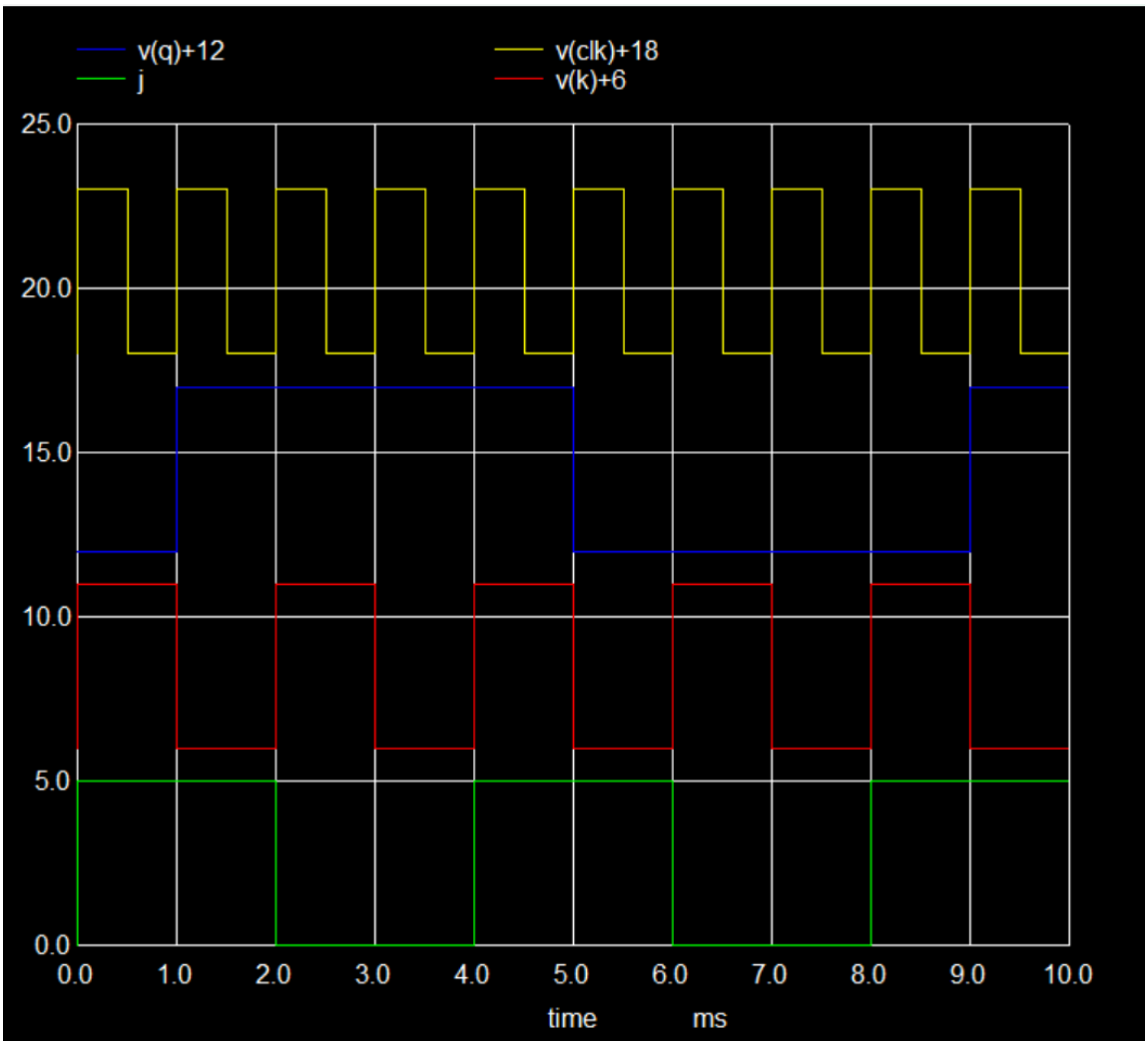

Figure 10.4: Output of the SN5470

Chapter 11

74LS670

Primary reference: Texas Instruments SN54/74LS670 4-by-4 Register File datasheet

11.1 General Description

The 74LS670 is a 4-word by 4-bit register file with 3-state outputs from the LS TTL family. It provides independent read and write address decoding, so that any of the four internal 4-bit registers can be written to while a different (or the same) register is simultaneously read out through the 3-state output bus [10].

11.2 Key Features

- 4-word $\times$ 4-bit register file (16 flip-flops total)
- Independent 2-bit read-address and write-address decoding
- 3-state outputs with active-LOW output-enable
- Active-LOW write-enable input
- Standard TTL voltage operation

11.3 Applications

- Small scratch-pad memories and register files
- CPU general-purpose register banks
- FIFO/buffer constructions
- Digital signal routing and storage

11.4 Subcircuit Symbol

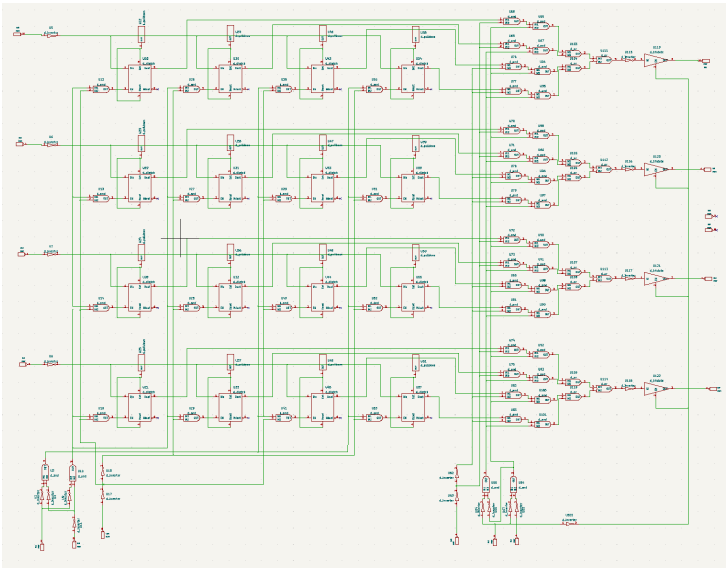

Figure 11.1: Subcircuit Symbol of the 74LS670

11.5 Subcircuit Schematic Diagram

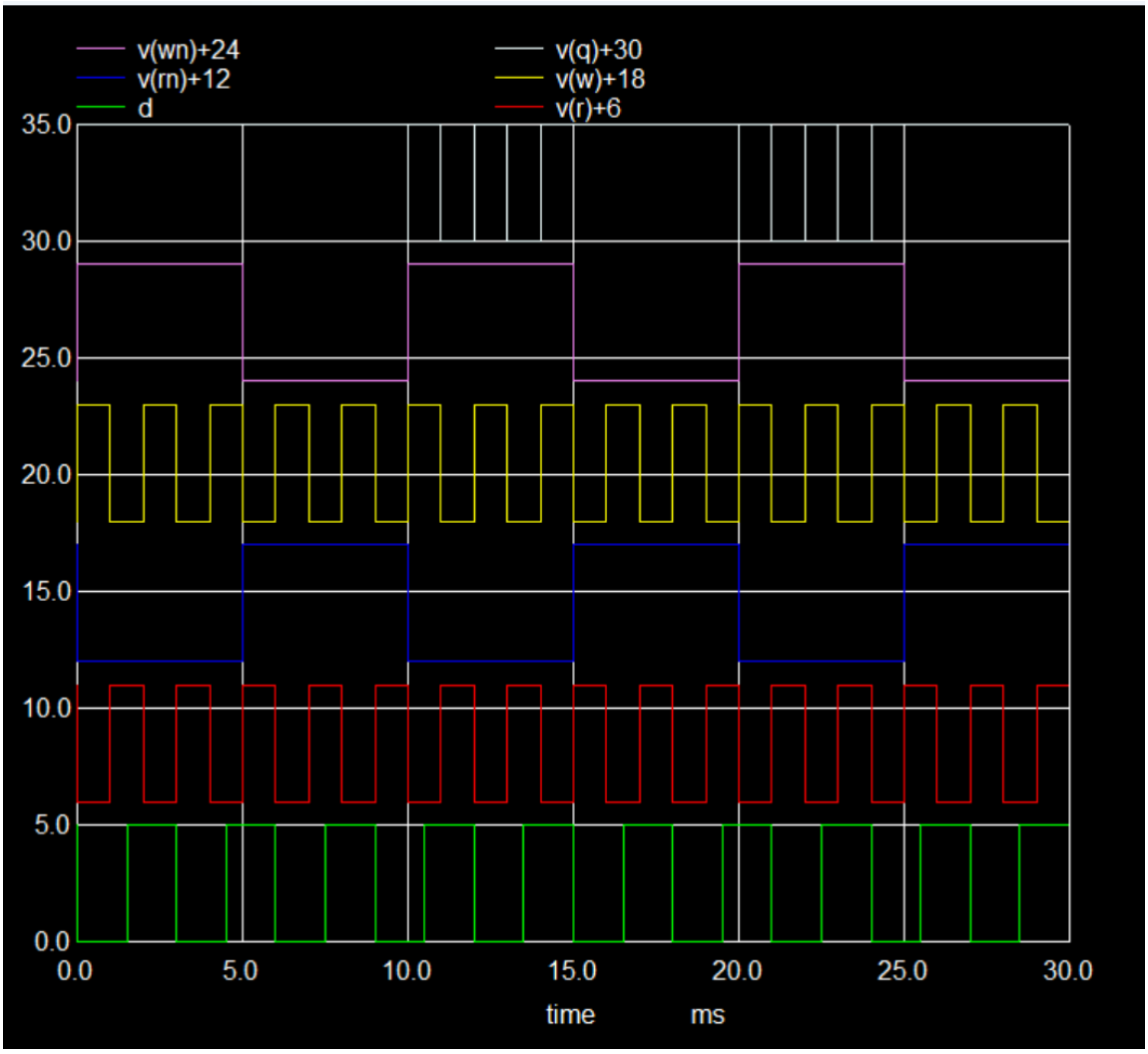

Figure 11.2: Subcircuit Schematic of the 74LS670

11.6 Datasheet Pin Diagram

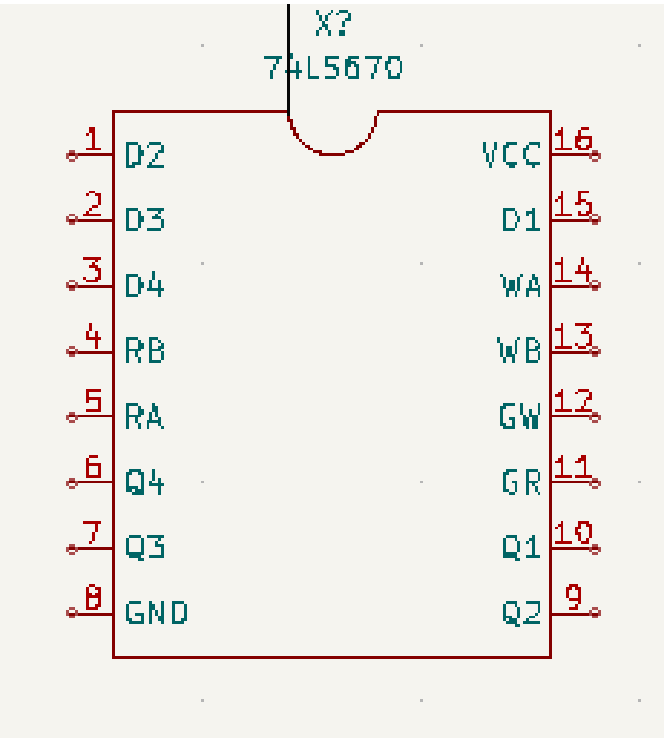

Figure 11.3: Pin Diagram of the 74LS670

11.7 Test Circuit

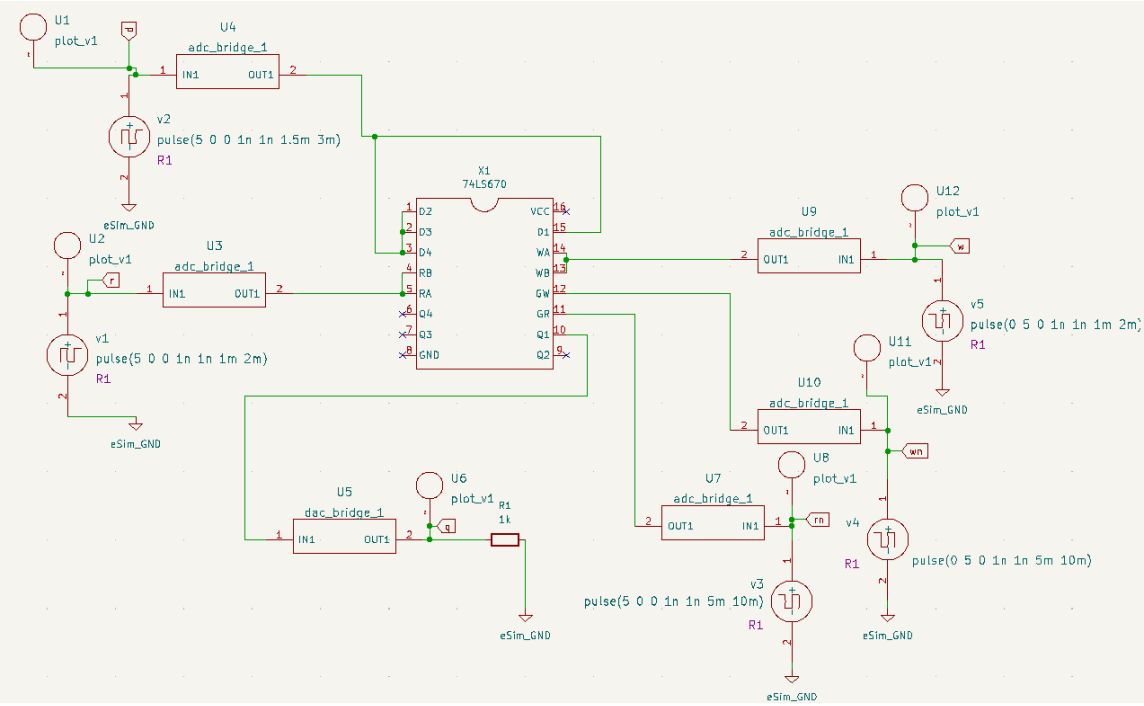

Figure 11.4: Test Circuit of the 74LS670

11.8 Function Table

Write Enable	Output Enable	Action
L	L	Write selected word; read selected word out
H	L	Read-only, selected word driven onto outputs
X	H	Outputs Hi-Z

Table 11.1: Function Table of the 74LS670

Chapter 12

74LS173

Primary reference: Texas Instruments SN54173/SN54LS173A, SN74173/SN74LS173A 4-Bit D-Type Register datasheet

12.1 General Description

The 74LS173 is a 4-bit D-type register with 3-state outputs from the LS TTL family. Data entry is controlled by two active-LOW data-input-enable lines, and the outputs are controlled by two active-LOW output-enable lines, allowing the register to be used directly on a bidirectional data bus. A common active-HIGH asynchronous clear resets all four bits [11].

12.2 Key Features

- Four D-type edge-triggered flip-flops with 3-state outputs
- Two active-LOW data-input-enable controls
- Two active-LOW output-enable controls
- Common active-HIGH asynchronous master reset
- Standard TTL voltage operation

12.3 Applications

- Bus-oriented general-purpose registers
- Microprocessor accumulator/register applications
- Data buffering between bus segments
- Temporary data storage in digital systems

12.4 Subcircuit Symbol

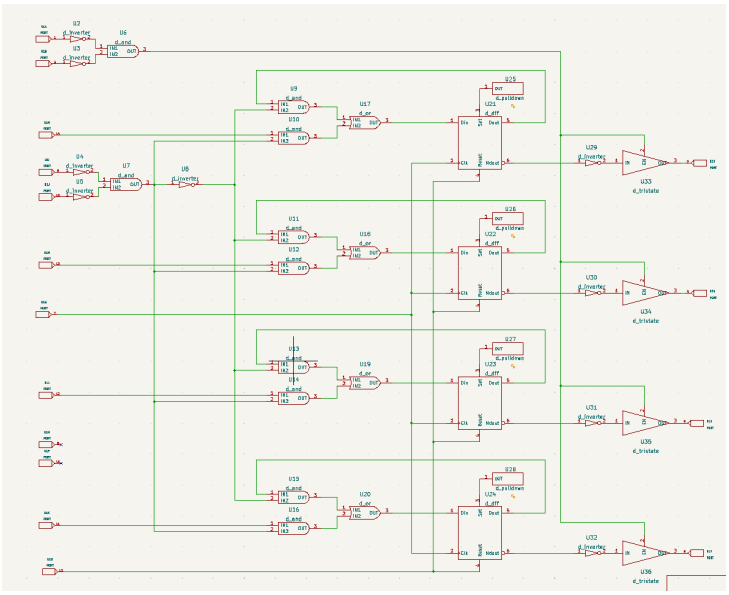

Figure 12.1: Subcircuit Symbol of the 74LS173

12.5 Datasheet Pin Diagram

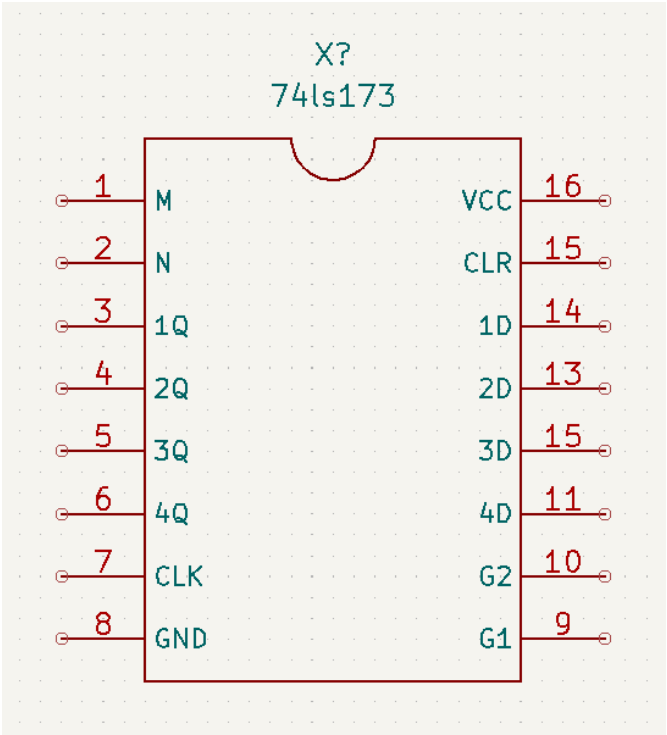

Figure 12.2: Pin Diagram of the 74LS173

12.6 Test Circuit

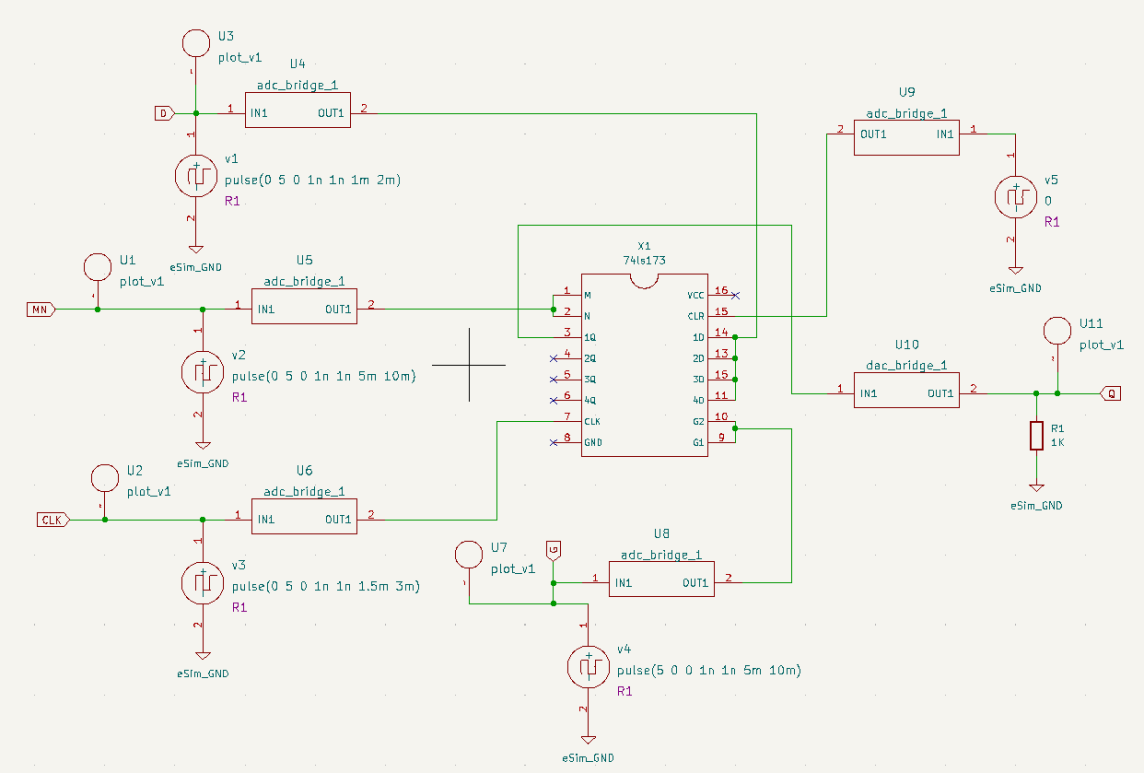

Figure 12.3: Test Circuit of the 74LS173

12.7 Function Table

Clear	Input Enable	Clock	Action
H	X	X	All outputs = 0
L	L	↑	Data loaded into register
L	H	X	Register holds data

Table 12.1: Function Table of the 74LS173

12.8 Output Plot

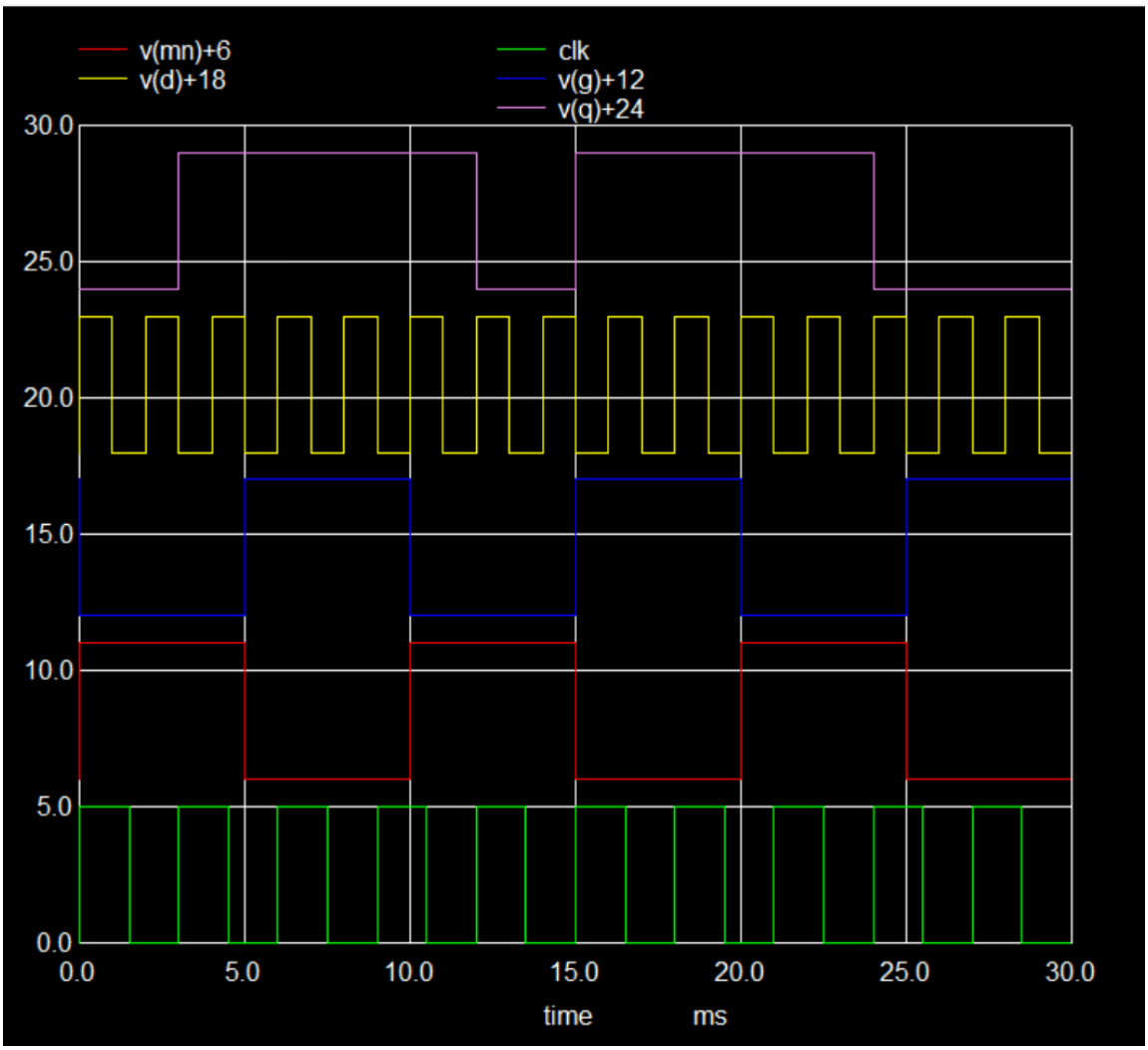

Figure 12.4: Output of the 74LS173

Chapter 13

74LVC157

Primary reference: Texas Instruments SN54/74LVC157A Quadruple 2-Line to 1-Line Data Selector/Multiplexer datasheet

13.1 General Description

The 74LVC157 is a quad 2-input multiplexer built in Low-Voltage CMOS (LVC) technology. It selects one of two 4-bit data sources (bus A or bus B) and routes it to a common set of four non-inverting outputs, under the control of a shared select input, with a single active-LOW enable input for tri-stating/disabling all outputs [12].

13.2 Key Features

- Quad 2-input non-inverting multiplexer
- Common select line for all four channels
- Single active-LOW output-enable/disable input
- Low-voltage CMOS operation (down to 1.65 V–3.6 V typical)
- High-speed switching with low propagation delay

13.3 Applications

- Data-source selection in low-voltage digital systems
- Bus switching and signal routing
- Portable and battery-operated equipment
- Interfacing between mixed logic-level buses

13.4 Subcircuit Symbol

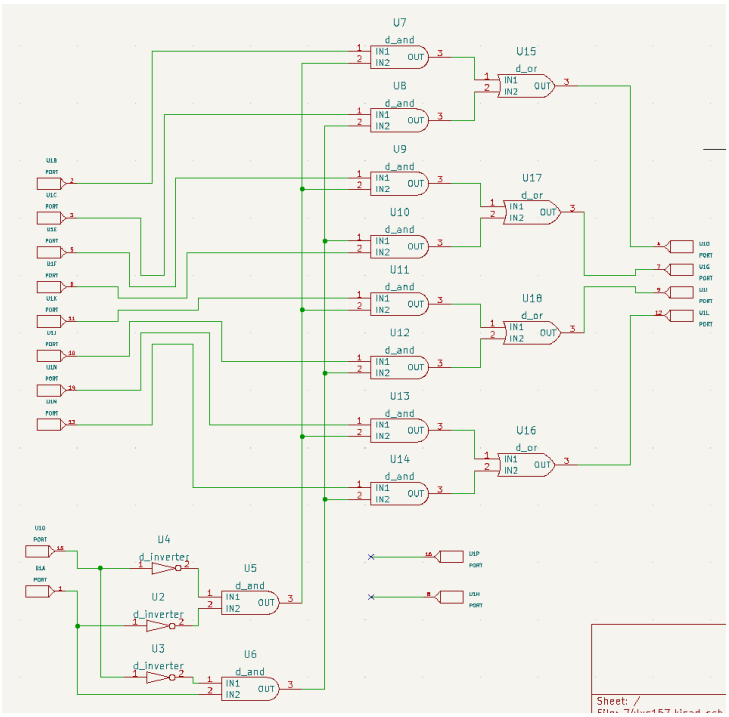

Figure 13.1: Subcircuit Symbol of the 74LVC157

13.5 Datasheet Pin Diagram

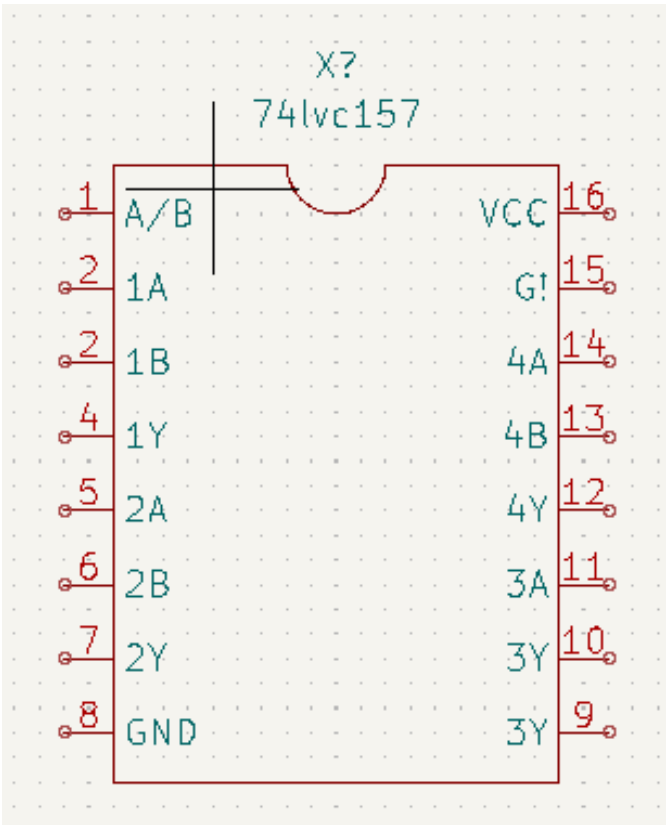

Figure 13.2: Pin Diagram of the 74LVC157

13.6 Test Circuit

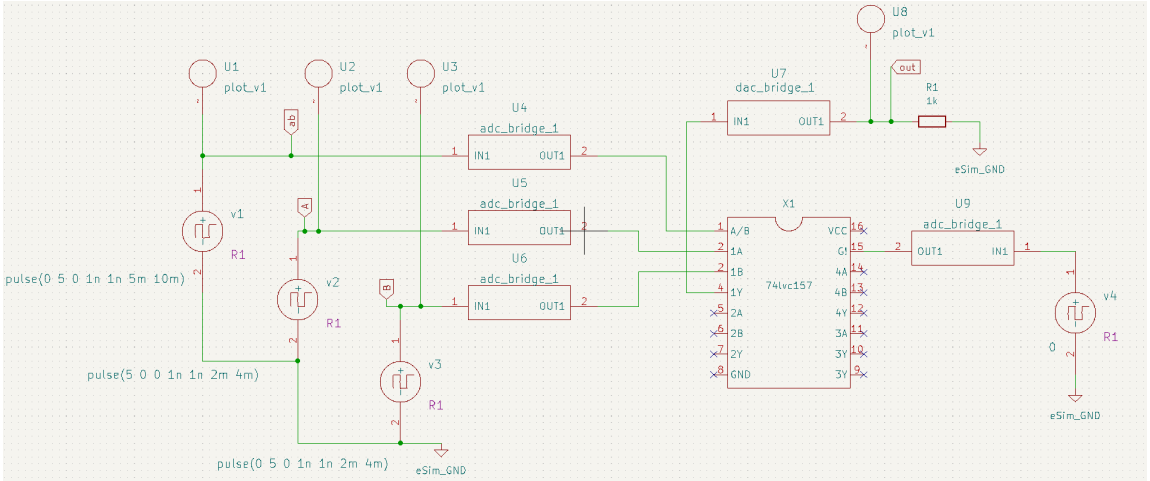

Figure 13.3: Test Circuit of the 74LVC157

13.7 Function Table

Enable	Select	Inputs (A, B)	Output (Y)
H	X	X	L (all outputs disabled)
L	L	A	Y = A
L	H	B	Y = B

Table 13.1: Function Table of the 74LVC157

13.8 Output Plot

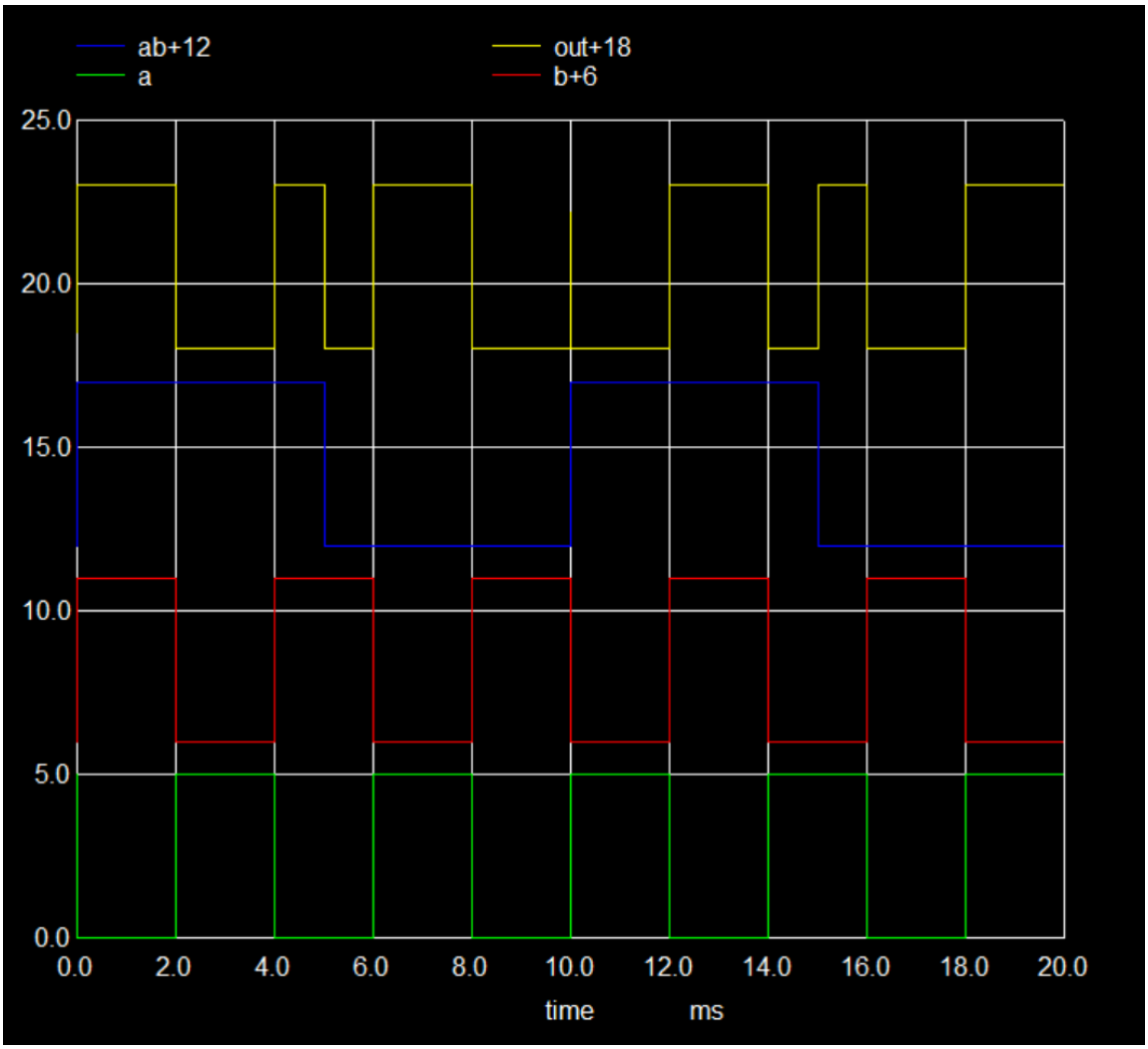

Figure 13.4: Output of the 74LVC157

Chapter 14

Conclusion and Future Scope

This project successfully fulfilled its objective of contributing a diverse set of accurately modelled digital logic ICs to the eSim subcircuit library. Each IC was implemented based on its manufacturer datasheet and verified through NgSpice-based simulation testbenches to confirm functional correctness against the published function table.

The contributions include counters, registers, latches, a bus buffer, an arithmetic logic unit, a J-K flip-flop, a register file, and a multiplexer – together covering a wide range of digital design building blocks. These verified models serve as valuable resources for students, educators, and researchers using eSim.

Future Scope

- Export and add the missing SN74LS244 subcircuit symbol, test circuit, and output-plot figures once available.
- Extend the library with additional members of the same device families (e.g., the 74LS90/74LS92 counters and the 74LS373 latch) using the same generic-gate modelling approach.
- Package the verified subcircuits with accompanying documentation directly into the official eSim library repository for community use.
- As the eSim device model library continues to grow, broader adoption is anticipated among the engineering community, enabling increasingly sophisticated open-source circuit simulation.

Chapter 15

Circuits Contribution

This chapter lists all the Integrated Circuits (ICs) contributed during the internship. Each IC has been carefully modelled, simulated, and verified.

Aarpan Thapa – List of ICs

1. 74LS93 – 4-Bit Binary Ripple Counter
2. 74LS175 – Quad D-Type Positive-Edge-Triggered Flip-Flop
3. 74LS374 – Octal D-Type Edge-Triggered Flip-Flop (3-State)
4. CD4024BC – 7-Stage Ripple-Carry Binary Counter
5. SN74LS244 – Octal Buffer/Line Driver (3-State)
6. SN74S181 – 4-Bit Arithmetic Logic Unit (ALU)
7. SN5470 – AND-Gated Positive-Edge-Triggered J-K Flip-Flop
8. 74LS670 – 4-Word $\times$ 4-Bit Register File (3-State)
9. 74LS173 – 4-Bit D-Type Register (3-State)
10. 74LVC157 – Quad 2-Input Multiplexer (Low-Voltage CMOS)

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