eSim Summer Fellowship 2026

On

Designing Integrated Circuit in eSim & Device Modelling in eSim

Submitted by

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Contents

Chapter 1

Introduction

FOSSEE (Free/Libre and Open Source Software for Education) project promotes the use of FLOSS tools to improve the quality of education in our country. It aims to reduce dependency on proprietary software in educational institutions. It encourages the use of FLOSS tools through various activities to ensure commercial software is replaced by equivalent FLOSS tools. It also develops new FLOSS tools and upgrades existing tools to meet requirements in academia and research.

The FOSSEE project is part of the National Mission on Education through Information and Communication Technology (ICT), Ministry of Human Resource Development (MHRD), Government of India.

1.1 eSim

eSim is a CAD tool that helps electronic system designers to design, test, and analyze their circuits. The important feature of this tool is that it is open source, allowing users to modify the source as per their needs. The software provides a generic, modular, and extensible platform for experimenting with electronic circuits. eSim is built using various free/libre and open-source software components including:

1.1.1 KiCad

Integrated software where all functions of circuit drawing, control, layout, library management, and access to the PCB design software are carried out.

1.1.2 Ngspice

Ngspice is a general-purpose circuit simulation program for nonlinear dc, nonlinear transient, and linear ac analysis.

1.1.3 KiCad to Ngspice Converter

Analysis parameters, source details are provided through this module. It allows us to add and edit the device models and subcircuits included in the circuit schematic.

1.1.4 Subcircuit Builder

This module allows the user to create a subcircuit for a component. Once the subcircuit for a component is created, the user can use it in other circuits.

1.1.5 NGHDL

A module for mixed signal circuit simulation, is also integrated with eSim. It makes use of VHDL code.

1.1.6 NgVeri

NgVeri, a module for mixed signal circuit simulation, is also integrated with eSim. It makes use of Verilog/System Verilog/Transaction-Level Verilog code.

1.1.7 Makerchip

Makerchip is a cloud-based browser application developed by Redwood EDA to do digital circuit design. One can simulate Verilog/SystemVerilog/Transaction-Level Verilog code in Makerchip.

Chapter 2

Features of eSim

eSim offers a comprehensive set of features that make it a powerful open-source alternative for electronic design automation:

Open-source and Free: eSim is fully open-source, allowing unrestricted access without licensing costs, making it ideal for educational institutions and individual users.

Integrated Toolchain: Combines multiple open-source tools such as KiCad for schematic capture and PCB design, NgSpice for analog/digital simulation, and NGHDL for digital logic.

Mixed-Signal Simulation: Supports both analog and digital simulation, allowing users to design and simulate mixed-signal circuits within the same environment.

Subcircuit Feature: Enables hierarchical and modular design by allowing complex circuits to be broken into reusable subcircuit blocks.

Device Modeling: Supports custom device modeling, allowing users to simulate real-world semiconductor devices using user-defined SPICE models.

SkyWater SKY130 PDK Support: Provides access to open-source 130 nm process design kit for IC design and simulation.

Python Integration: Allows automation, scripting, and advanced analysis using Python interfaces.

User-Friendly Interface: Offers an intuitive GUI that simplifies circuit creation, simulation setup, and result analysis.

Cross-Platform Support: Compatible with major operating systems like Linux and Windows.

Active Community and Documentation: Extensive documentation, tutorials, and community support provided through the FOSSEE ecosystem.

Chapter 3

Problem Statement

3.1 Subcircuit Design and Integration

The objective is to design and develop various Analog and Digital Integrated Circuit (IC) models in the form of subcircuits using device model files already available in the eSim library. These IC models, once successfully integrated into the eSim Subcircuit Library, will serve as reusable components for circuit design purposes by developers and end users.

Approach

Our implementation began with a detailed study of datasheets from reputed IC manufacturers such as Texas Instruments, Analog Devices, and NXP Semiconductors.

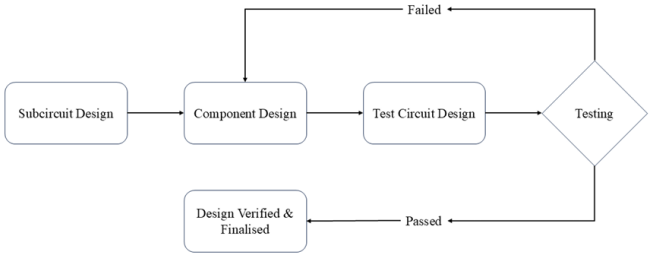

Figure 3.1: *Flowchart of approach for designing IC models*

1. **Analyzing Datasheets:** The first step involved reviewing datasheets of various analog and digital ICs to identify models not currently present in the eSim library. Once a candidate IC was shortlisted, we analyzed its detailed schematic, electrical characteristics, and truth table.

2. **Subcircuit Creation:** The selected IC was modeled as a subcircuit in eSim using only the existing device model files in the eSim library, strictly adhering to official datasheet specifications.
3. **Test Circuit Design:** After the subcircuit was modeled, we designed test circuits as recommended in the respective datasheets to validate the functional behavior of the IC under various input conditions.
4. **Schematic Testing:** The designed test circuits were then simulated using eSim's KiCad-to-NgSpice conversion and simulation interface. Output waveforms and plots were analyzed to verify expected performance.

3.2 Device Modeling using Model Editor

To design, develop and test various Analog and Digital Integrated Circuit Models using the sub-circuit feature in eSim and also to model semiconductor devices using eSim's model editor by fitting SPICE parameters from datasheet characteristics and validating them through simulation.

Approach

1. **Parameter Extraction:** Device parameters like saturation current, ideality factor, capacitances, and breakdown voltage are extracted from the datasheet I-V curves.
2. **Model File Creation:** The extracted parameters are entered into eSim's Model Editor manually to generate device XML files compatible with NgSpice.
3. **Test Circuit Design:** Test circuits are created to validate the newly modeled devices under typical operating conditions.
4. **Simulation and Validation:** The designed test circuits are simulated using NgSpice, and the results are compared with datasheet curves to confirm accuracy of the model.

Chapter 4

Integrated Circuit Design

4.1 CD4585B – 4-Bit Magnitude Comparator

4.1.1 Description

The CD4585B is a 4-bit magnitude comparator designed for computer and logic applications that require the comparison of two 4-bit words. This logic circuit determines whether one 4-bit word (Binary or BCD) is 'less than", 'equal to", or 'greater than" a second 4-bit word. The device includes eight complementary input pins (A0–A3 and B0–B3) and three outputs: A<, $A = B, and A¿$.

Features of CD4585B

- **Expandability:** Capable of expansion to 8, 12, 16, and up to 4N bits by cascading multiple units.
- **Medium-Speed Operation:** Compares two 4-bit words in typically 180 ns at 10 V.
- **Noise Margin:** Provides a noise margin of 1 V at VDD = 5 V, 2 V at VDD = 10 V, and 2.5 V at VDD = 15 V.

4.1.2 Pin Diagram

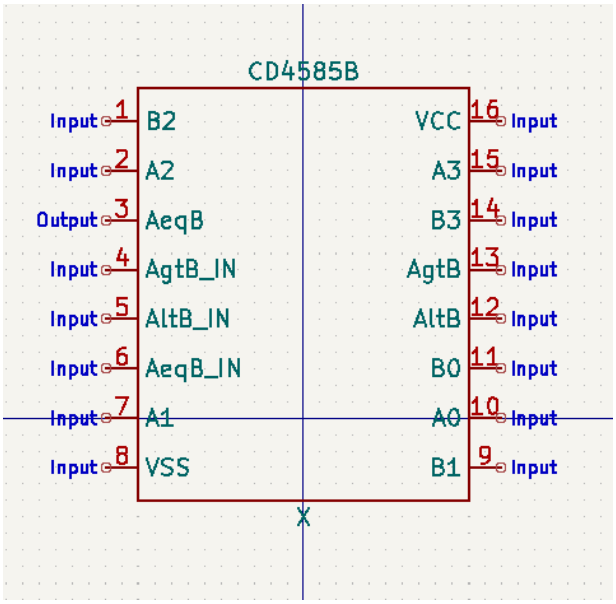

Figure 4.1: *Pin Diagram of CD4585B*

4.1.3 Sub-Circuit Diagram

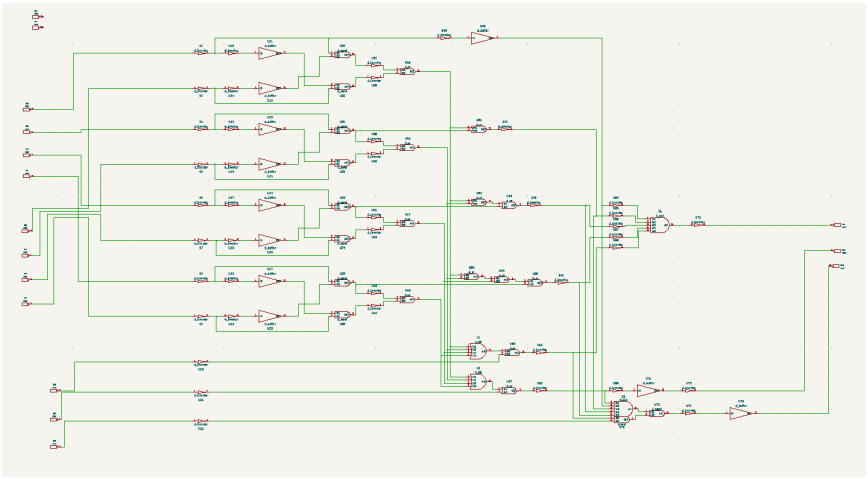

Figure 4.2: *Sub-Circuit of CD4585B*

4.1.4 Test-Circuit Diagram

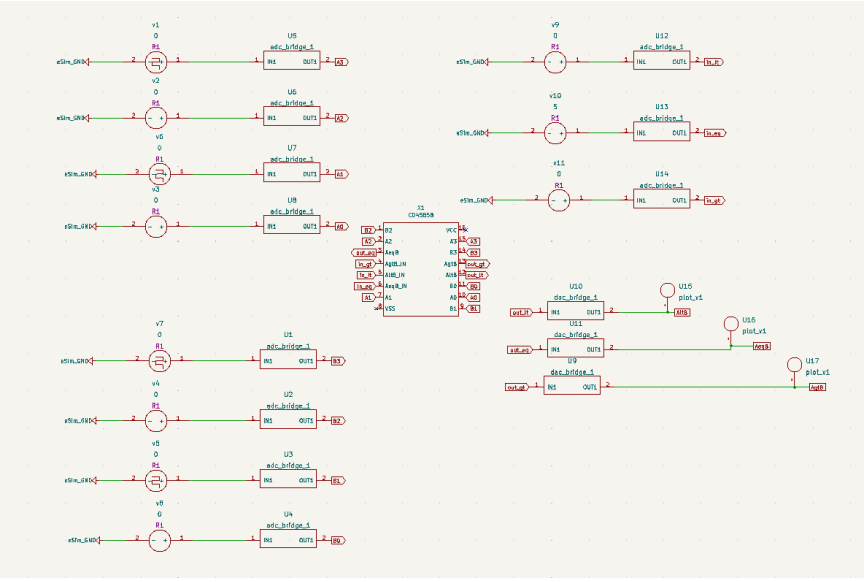

Figure 4.3: *Test Circuit of CD4585B*

4.1.5 NgSpice Plot – Input

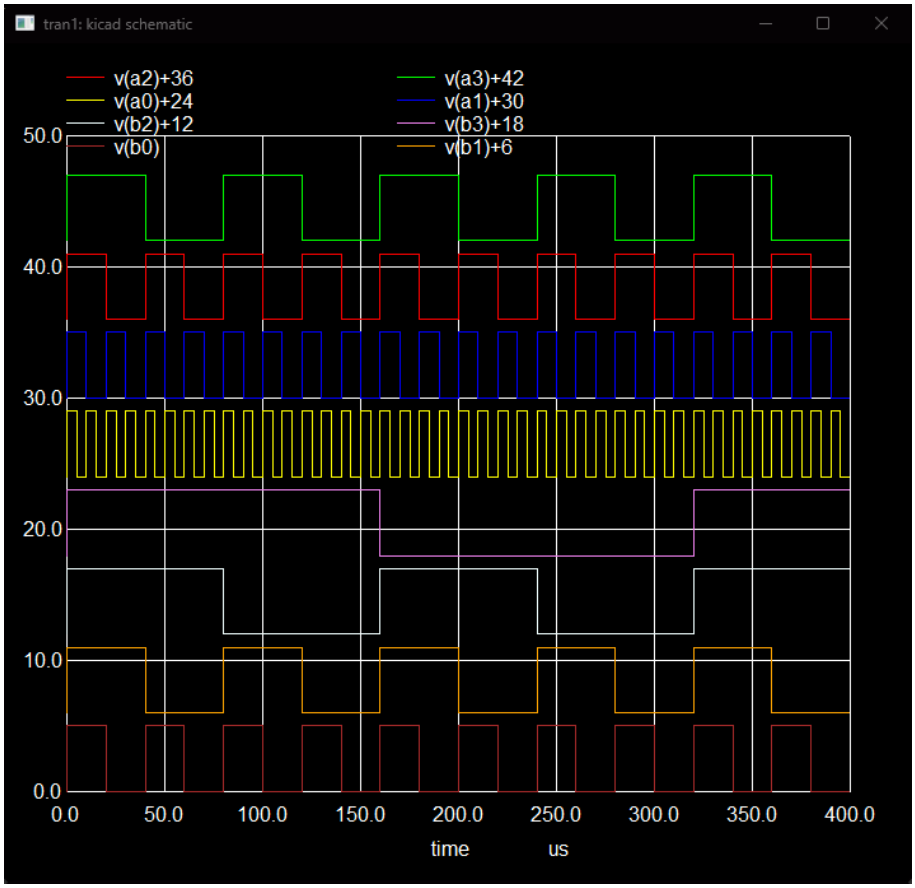

Figure 4.4: *Input Graph of CD4585B*

4.1.6 NgSpice Plot – Output

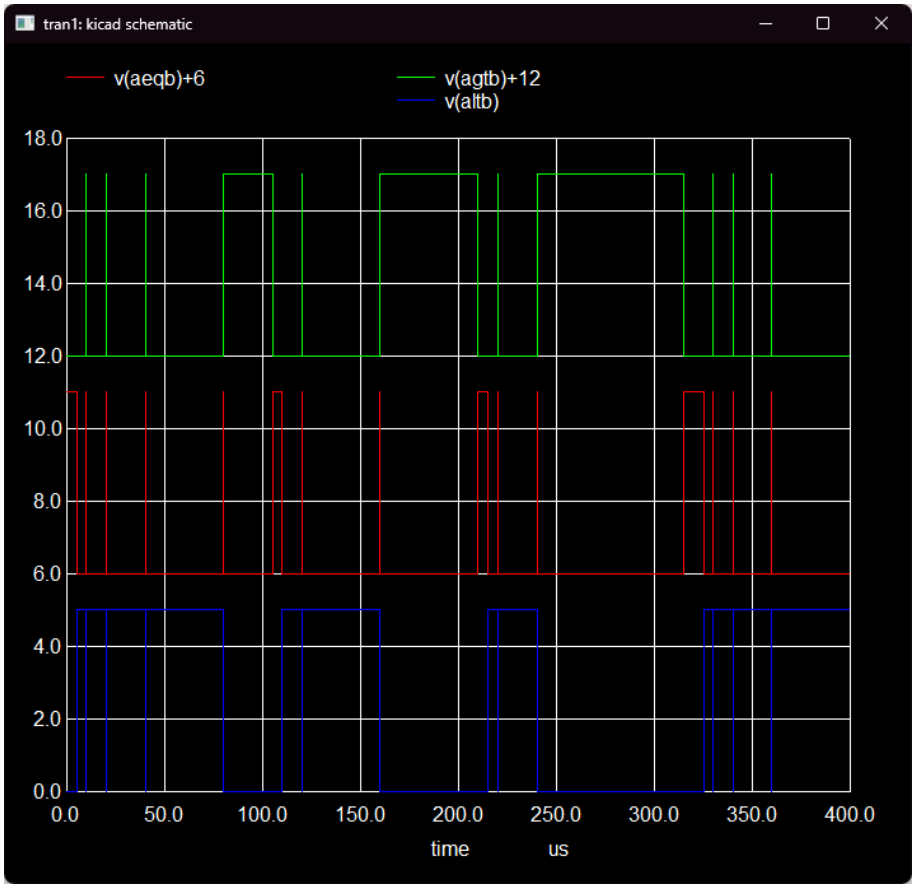

Figure 4.5: *Output Graph of CD4585B*

4.2 CA3240 – Dual BiMOS Operational Amplifier

4.2.1 Description

The CA3240 and CA3240A are dual versions of the popular CA3140 series integrated circuit operational amplifiers. These devices are designed to combine the advantages of both MOS and bipolar transistors on a single monolithic chip. They utilize gate-protected MOSFET (PMOS) input transistors, which provide very high input impedance, very low input current, and the ability to operate with the input common-mode voltage down to 0.5 V below the negative supply rail.

Features of CA3240

- **Design:** Operates as a dual version of the CA3140 operational amplifier.

- **Compensation:** The devices are internally compensated.
- **Common-Mode Range:** Offers a wide common-mode input voltage range that can be swung 0.5 V below the negative supply.

4.2.2 Pin Diagram

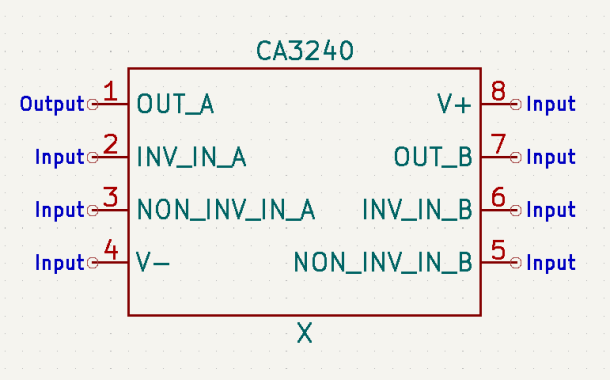

Figure 4.6: *Pin Diagram of CA3240*

4.2.3 Sub-Circuit Diagram

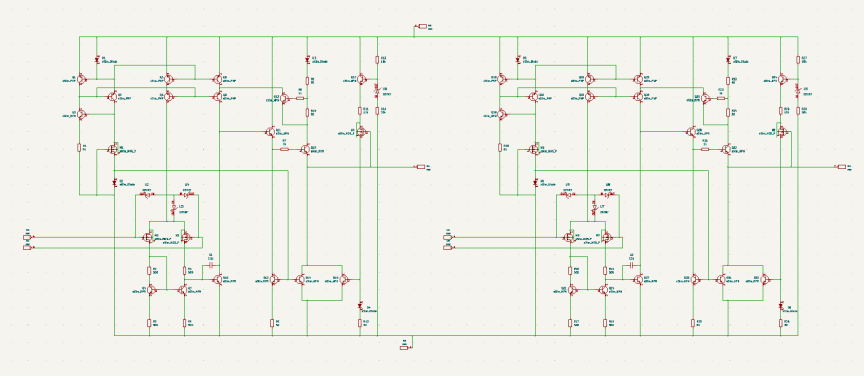

Figure 4.7: *Sub-Circuit of CA3240*

4.2.4 Test-Circuit Diagram

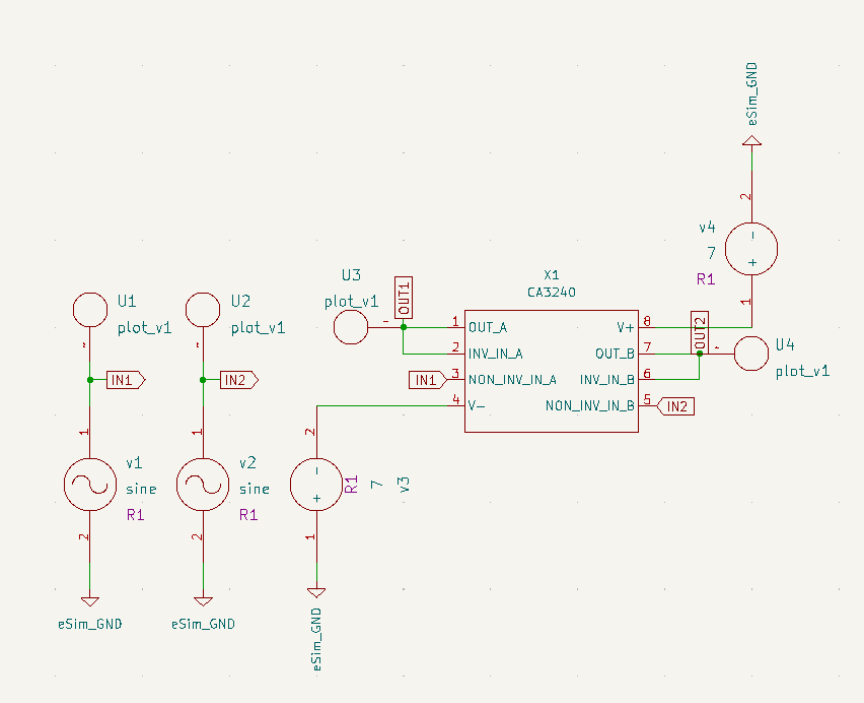

Figure 4.8: *Test Circuit of CA3240*

4.2.5 NgSpice Plot – Input

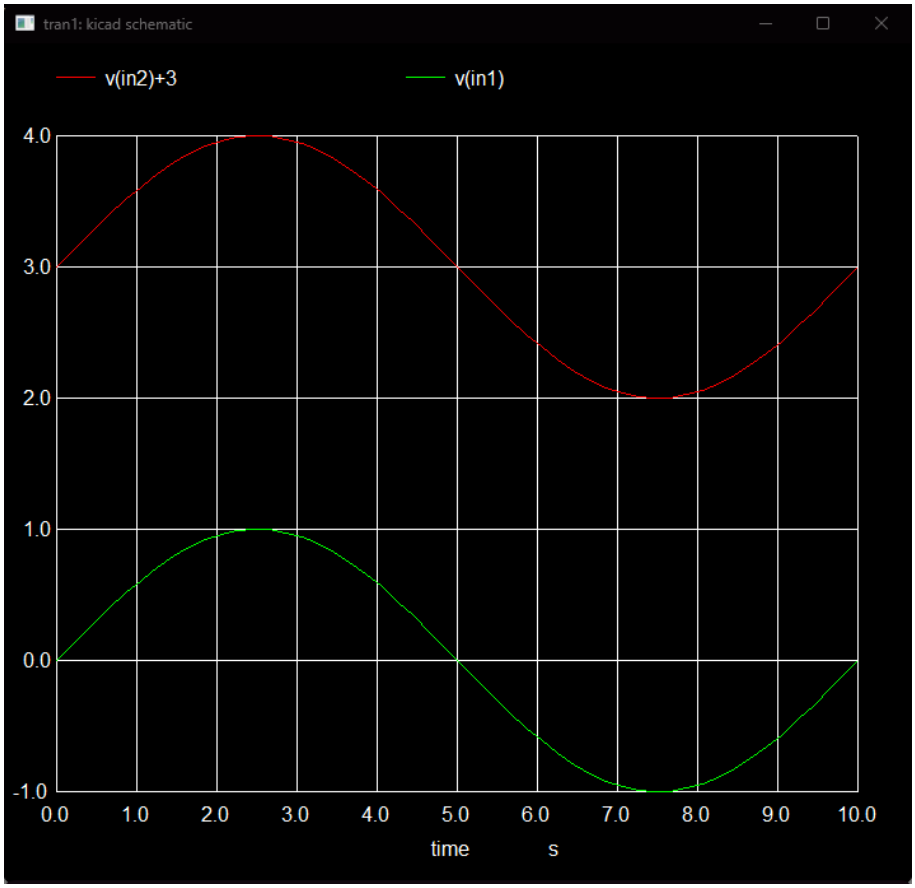

Figure 4.9: *Input Graph of CA3240*

4.2.6 NgSpice Plot – Output

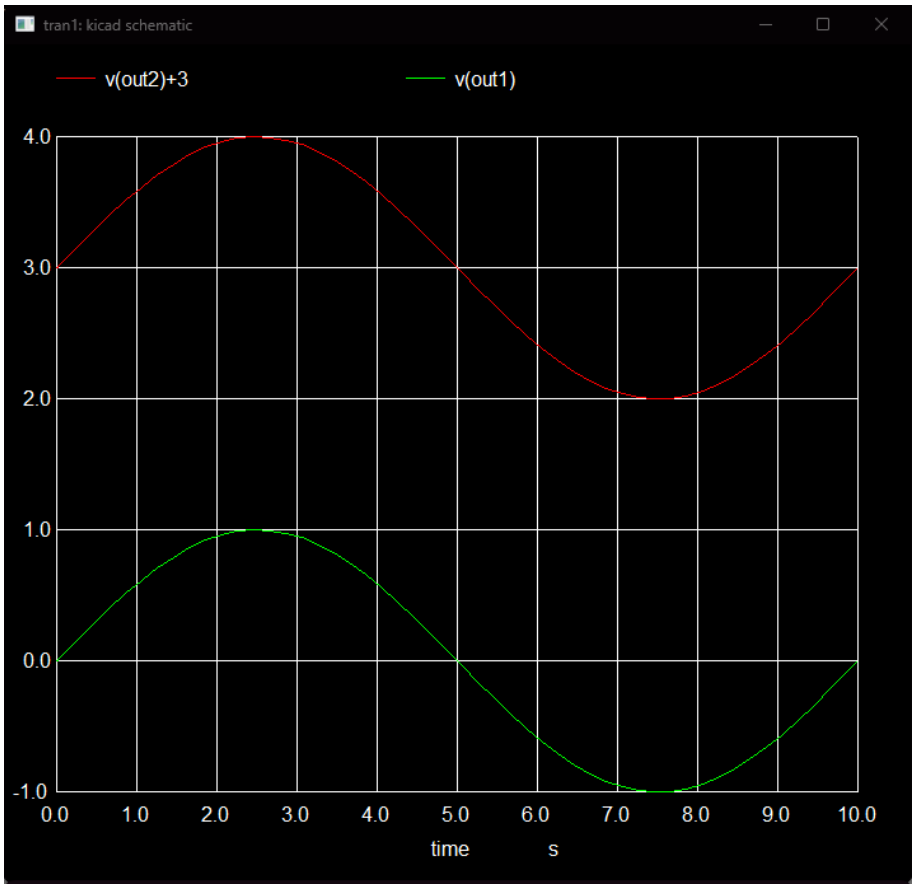

Figure 4.10: *Output Graph of CA3240*

4.3 CD4014B – 8-Stage Static Shift Register

4.3.1 Description

The CD4014B is a CMOS 8-stage static shift register with a high-voltage (20 V) rating. It operates as a synchronous parallel or serial input/serial output register. The device includes common CLOCK and PARALLEL/SERIAL CONTROL inputs, a single SERIAL data input, and individual parallel 'JAM" inputs for each stage.

Features of CD4014B

- **Operating Speed:** Capable of medium-speed operation with a typical clock rate of 12 MHz at VDD − VSS = 10 V.
- **Architecture:** Designed for fully static operation, containing 8 master-slave flip-flops plus output buffering and control logic.

- **Input Current:** Maximum input current of $1\,\mu at 18\,V over the full package - temperature range$.

4.3.2 Pin Diagram

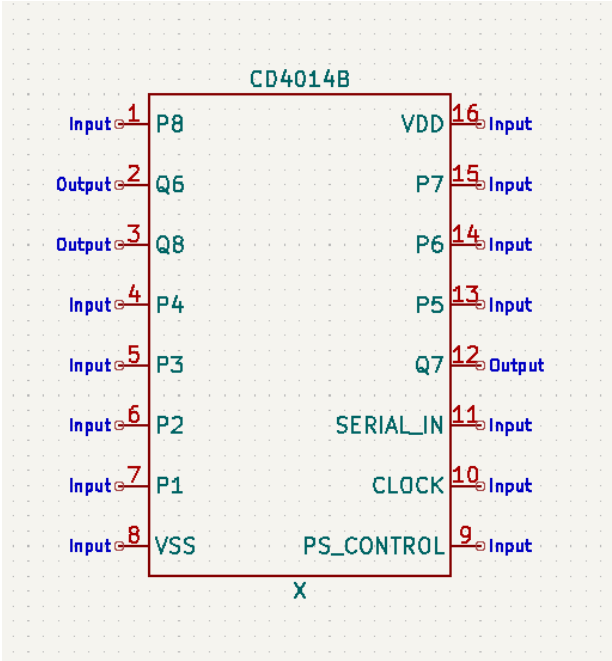

Figure 4.11: *Pin Diagram of CD4014B*

4.3.3 Sub-Circuit Diagram

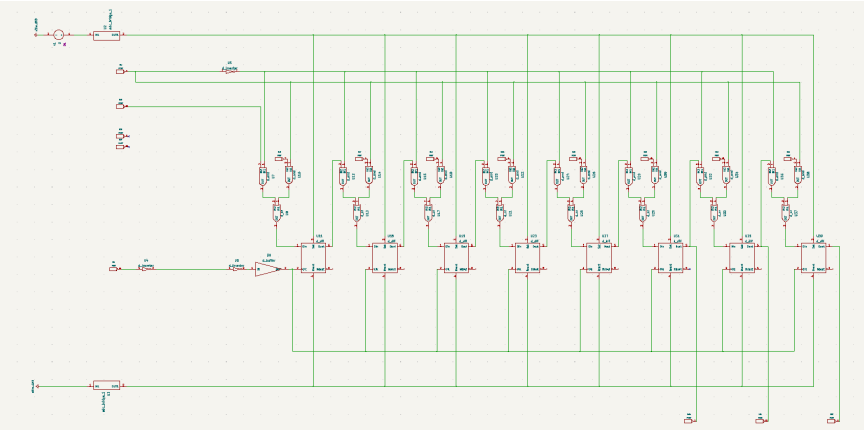

Figure 4.12: *Sub-Circuit of CD4014B*

4.3.4 Test-Circuit Diagram

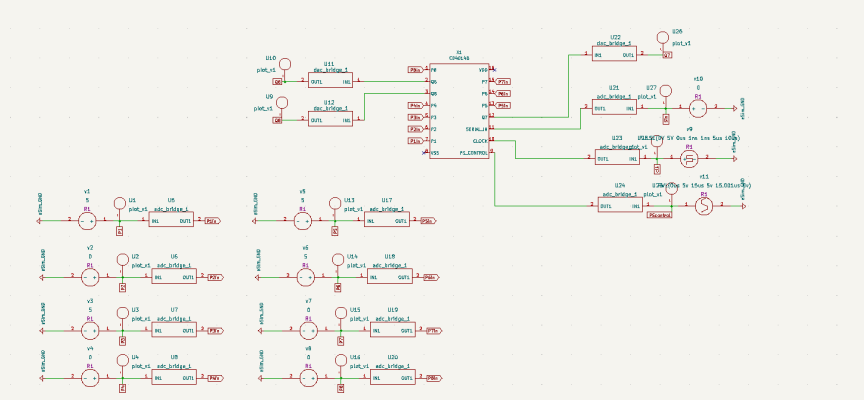

Figure 4.13: *Test Circuit of CD4014B*

4.3.5 NgSpice Plot – Input

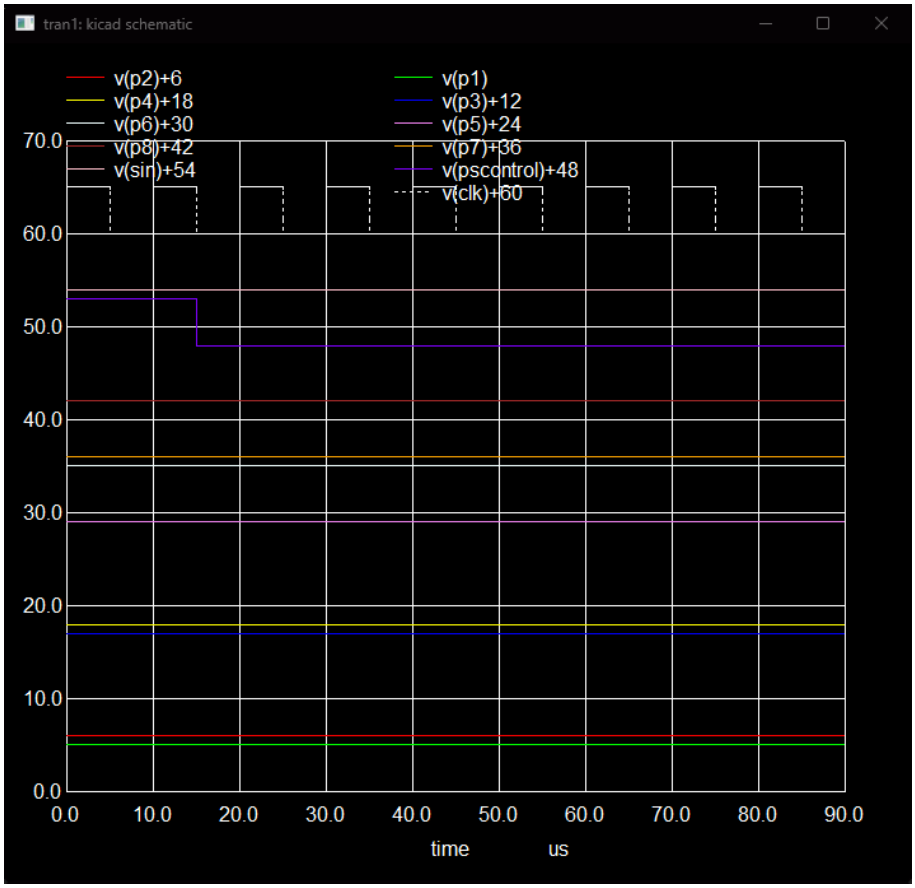

Figure 4.14: *Input Graph of CD4014B*

4.3.6 NgSpice Plot – Output

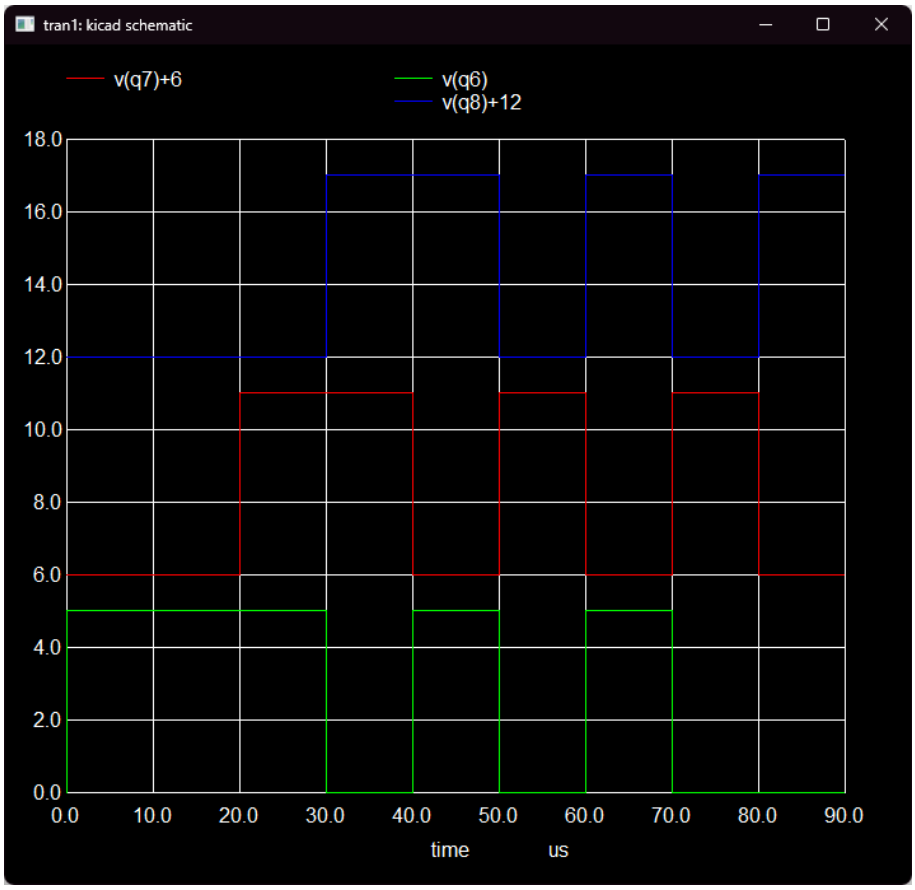

Figure 4.15: *Output Graph of CD4014B*

4.4 CD4041UB – Quad True/Complement Buffer

4.4.1 Description

The CD4041UB types are quad true/complement buffers that consist of n- and p-channel units featuring low channel resistance and high current sourcing and sinking capabilities. These devices are intended for use as a buffer, line driver, or CMOS-to-TTL driver.

Features of CD4041UB

- **Current Drive:** Provides balanced sink and source current, approximately 4 times the standard ‘B” drive.
- **Input Current:** Maximum input current of $1\,\mu at 18\,V over the full package temperature range.$
- **Delay:** Offers equalized delay to true and complement outputs.

4.4.2 Pin Diagram

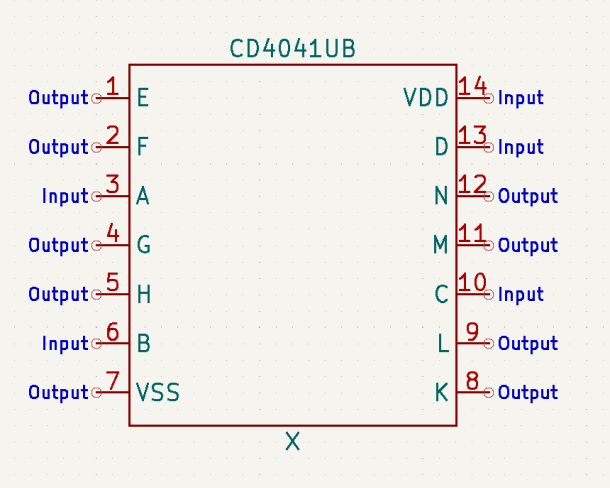

Figure 4.16: *Pin Diagram of CD4041UB*

4.4.3 Sub-Circuit Diagram

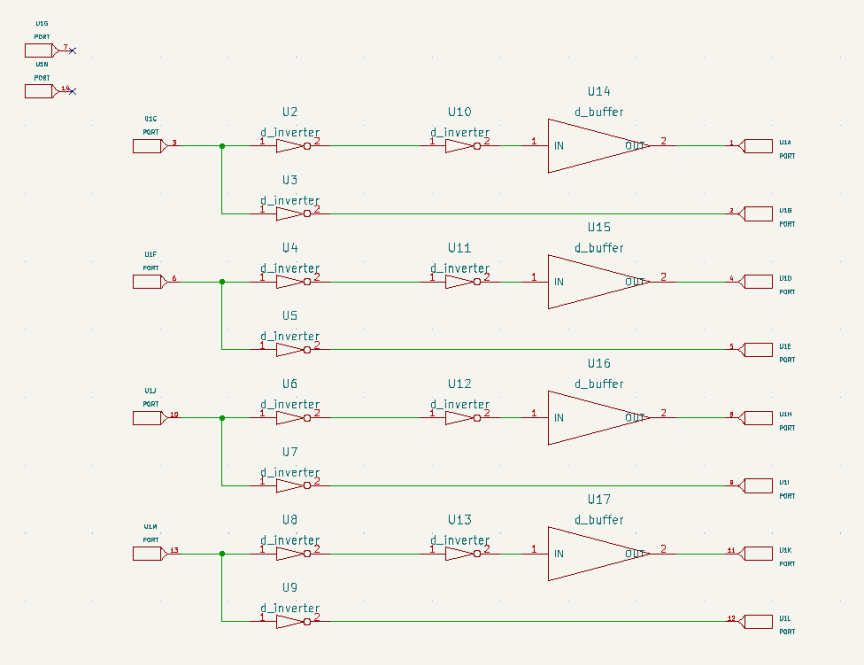

Figure 4.17: *Sub-Circuit of CD4041UB*

4.4.4 Test-Circuit Diagram

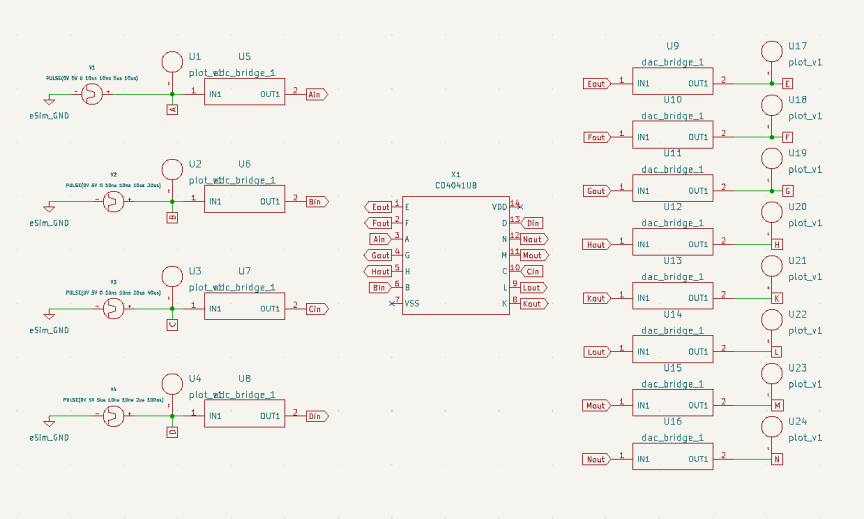

Figure 4.18: *Test Circuit of CD4041UB*

4.4.5 NgSpice Plot – Input

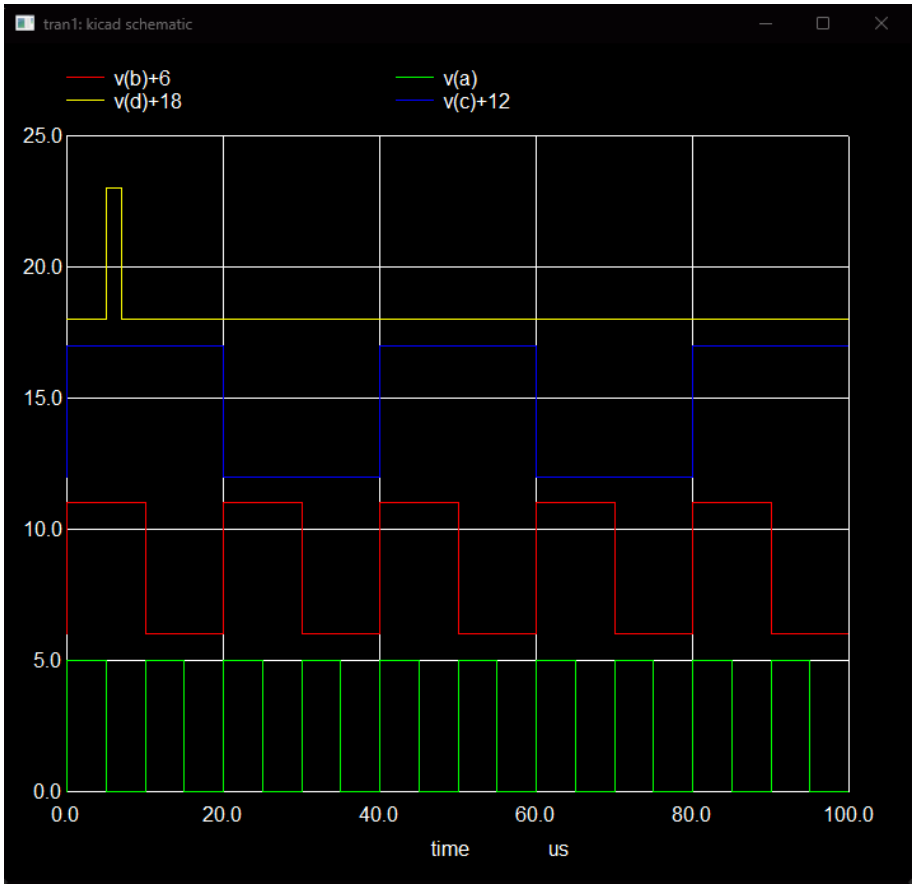

Figure 4.19: *Input Graph of CD4041UB*

4.4.6 NgSpice Plot – Output

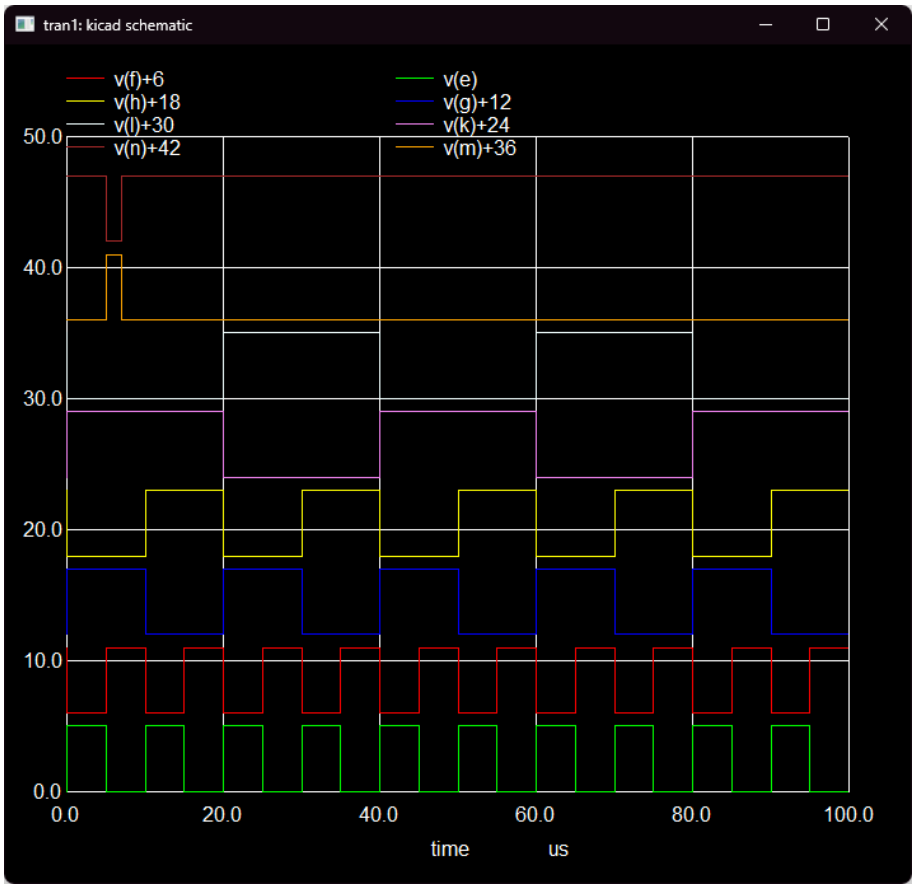

Figure 4.20: *Output Graph of CD4041UB*

4.5 74F538 – 1-of-8 Decoder/Demultiplexer

4.5.1 Description

The 74F538 is a decoder/demultiplexer that accepts three Address (A0–A2) input signals and decodes them to select one of eight mutually exclusive outputs. It includes a polarity control input (P) that dictates whether the outputs are active LOW or active HIGH. The device also features two active-LOW Enable inputs (G1, G2) that must both be asserted to enable the outputs.

Features of 74F538

- **Operating Voltage Range:** Supports supply voltage (VCC) range typically from 4.5 V to 5.5 V.
- **Logic Function:** Functions as a 3-to-8 line decoder/demultiplexer with polarity control.

- **Output Configuration:** Features 3-state outputs, allowing direct connection to bus lines.

4.5.2 Pin Diagram

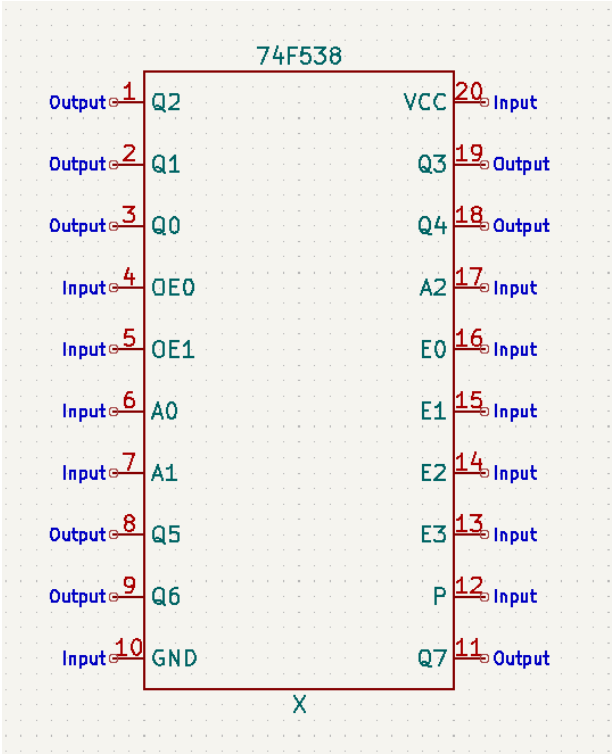

Figure 4.21: *Pin Diagram of 74F538*

4.5.3 Sub-Circuit Diagram

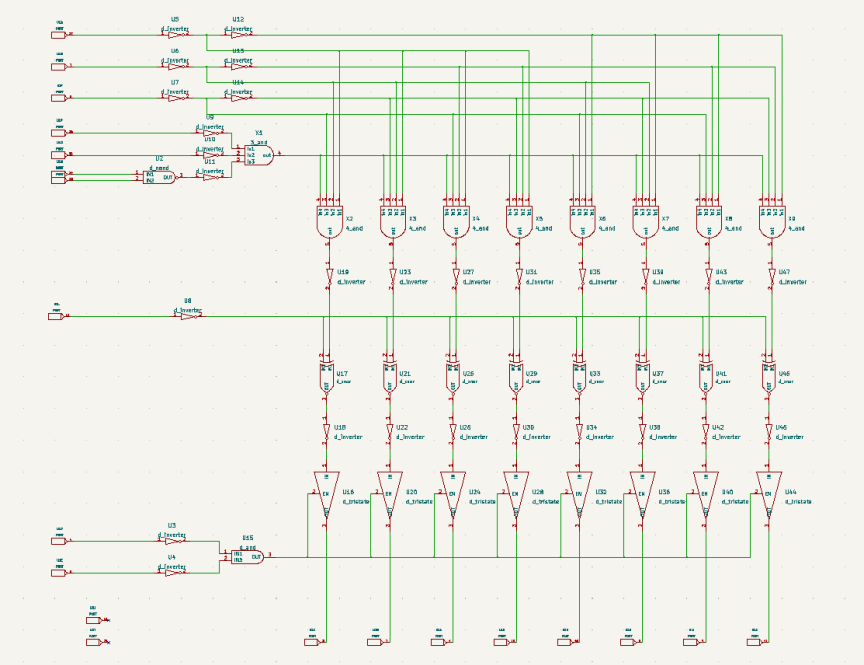

Figure 4.22: *Sub-Circuit of 74F538*

4.5.4 Test-Circuit Diagram

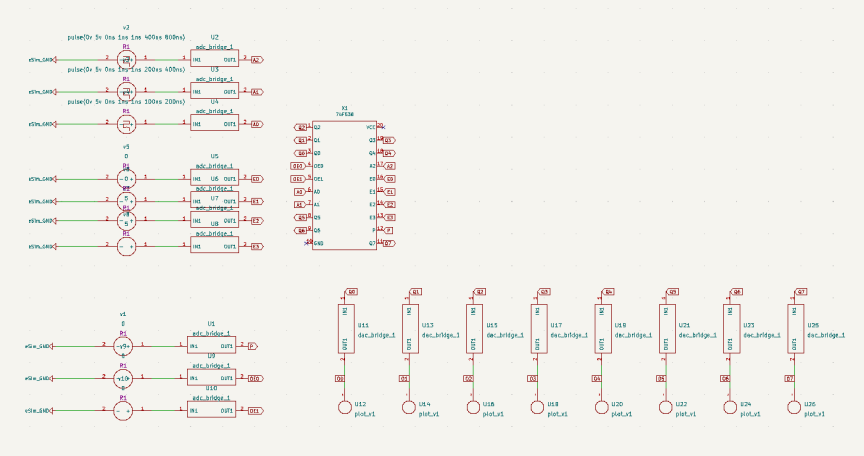

Figure 4.23: *Test Circuit of 74F538*

4.5.5 NgSpice Plot – Input

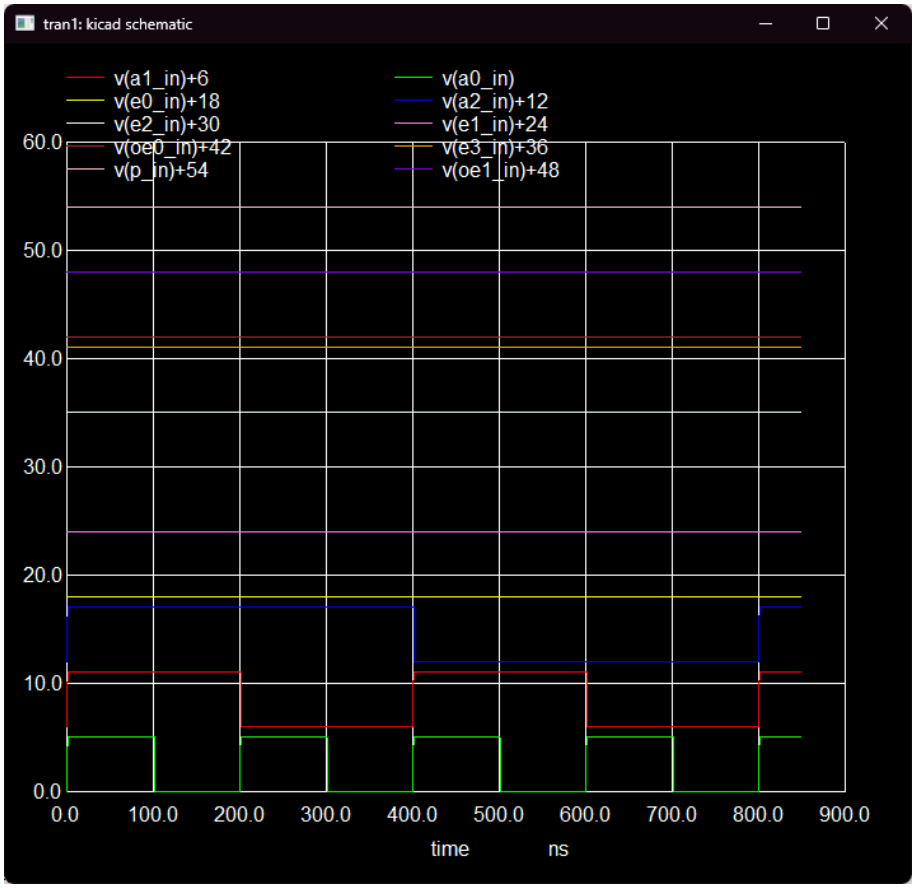

Figure 4.24: *Input Graph of 74F538*

4.5.6 NgSpice Plot – Output

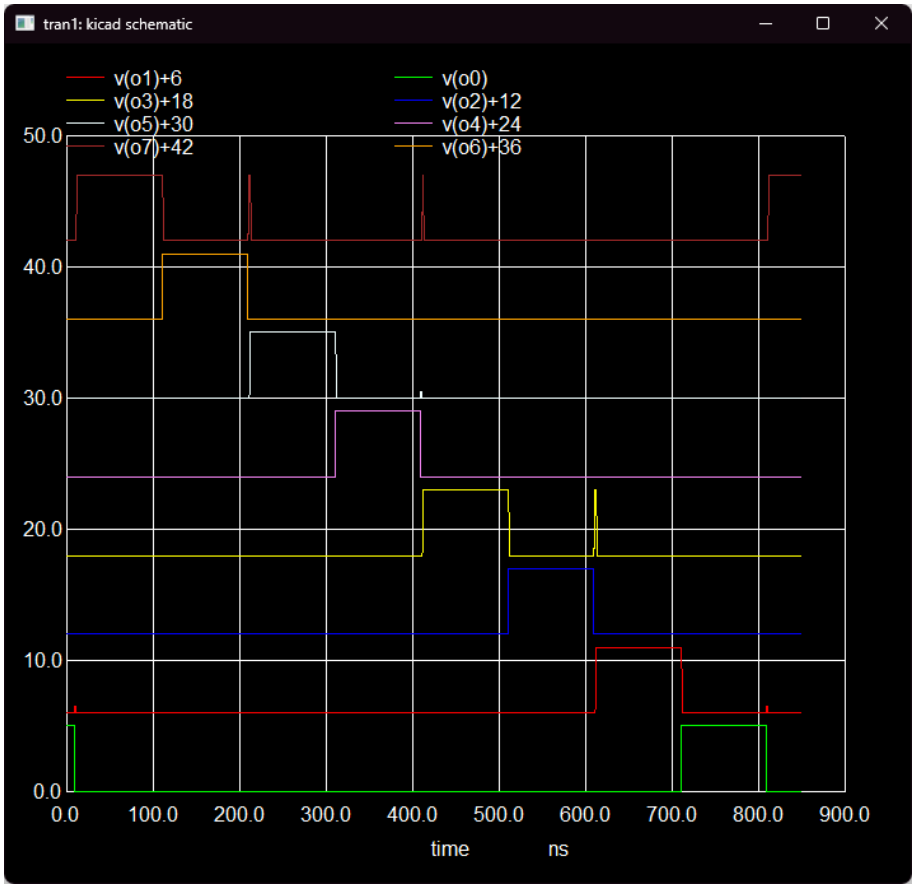

Figure 4.25: *Output Graph of 74F538*

4.6 CD4076B – 4-Bit D-Type Register with 3-State Outputs

4.6.1 Description

The CD4076B types are four-bit registers consisting of D-type flip-flops that feature three-state outputs. The device is equipped with Data Disable inputs to control the entry of data into the flip-flops. When both Data Disable inputs are low, data at the D inputs are loaded into their respective flip-flops on each positive clock transition.

Additionally, Output Disable inputs are provided. When these Output Disable inputs are both low, the normal logic states of the four outputs are available to the load. The outputs can be disabled independently of the clock by applying a high logic level to either Output Disable input.

Features of CD4076B

- **Output Symmetry:** Provides standardized, symmetrical output characteristics.
- **Input Control:** The input can be disabled without gating the clock.
- **Input Current Limits:** Maximum input current is $1\,\mu at 18\,V; 100\,nA at 5\,V and 10\,V$.

- **Noise Margin:** Provides 1 V at VDD = 5 V; 2 V at VDD = 10 V; 2.5 V at VDD = 15 V.
- **Output Control Lines:** Includes gated output control lines for enabling or disabling the outputs.

4.6.2 Pin Diagram

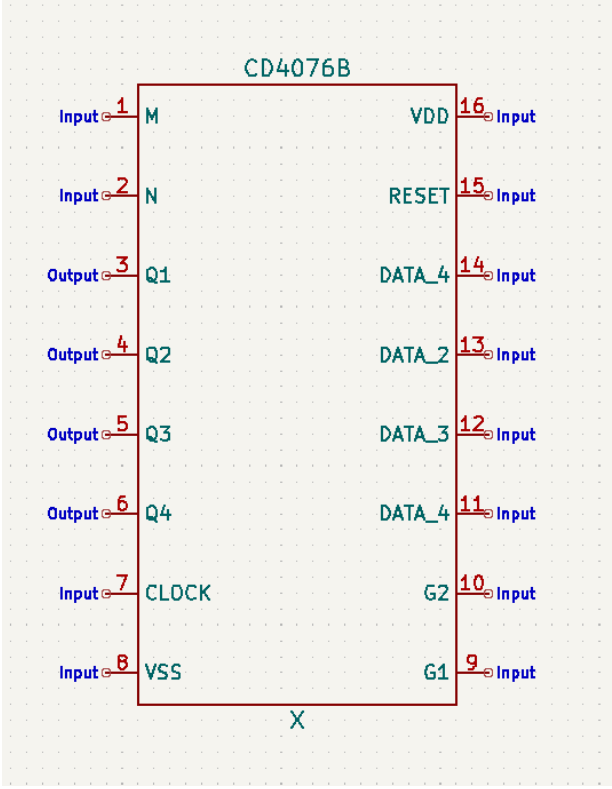

Figure 4.26: *Pin Diagram of CD4076B*

4.6.3 Sub-Circuit Diagram

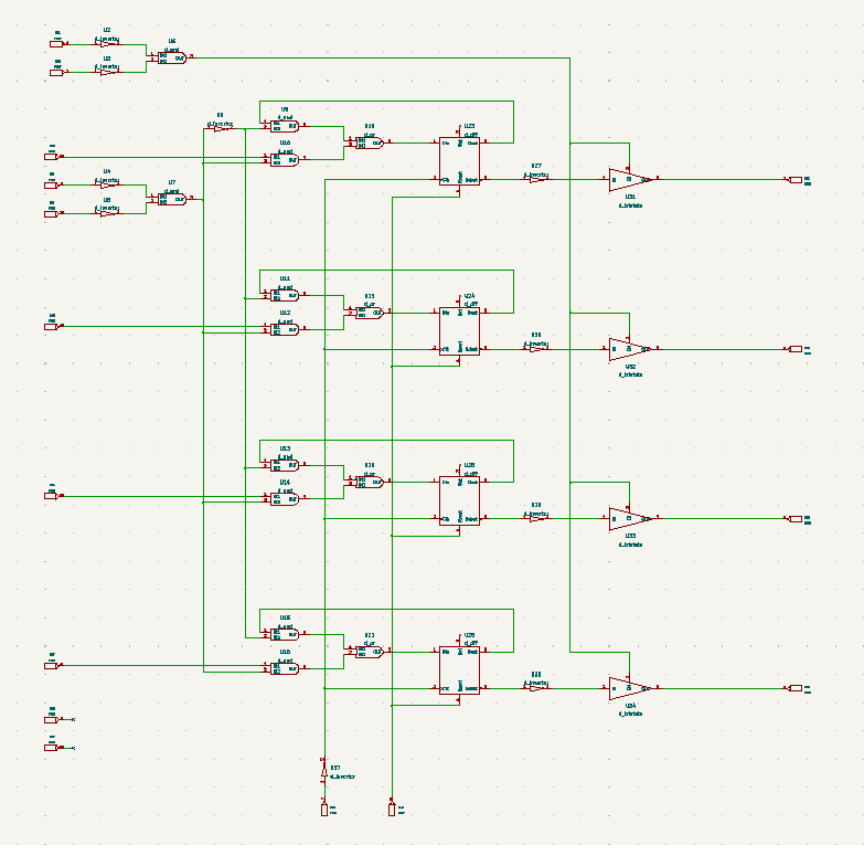

Figure 4.27: *Sub-Circuit of CD4076B*

4.6.4 Test-Circuit Diagram

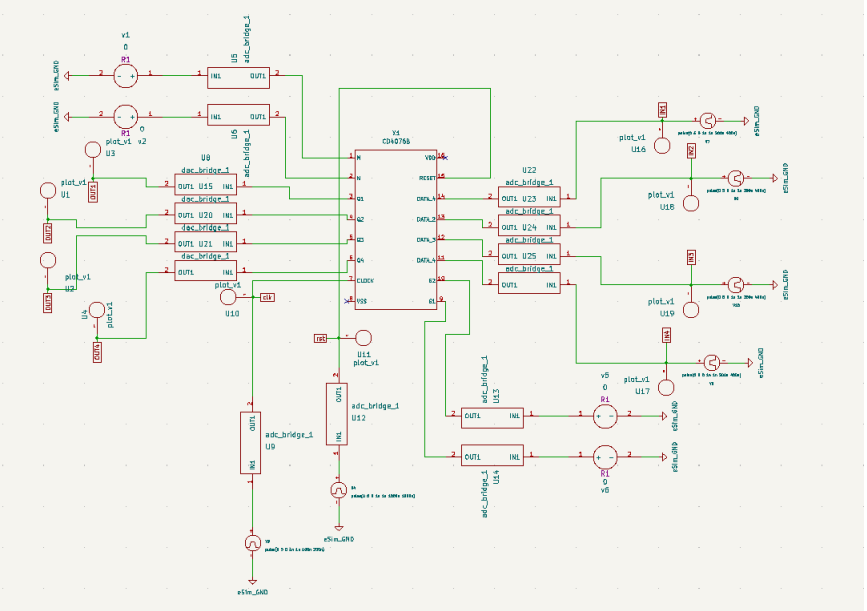

Figure 4.28: *Test Circuit of CD4076B*

4.6.5 NgSpice Plot – Input

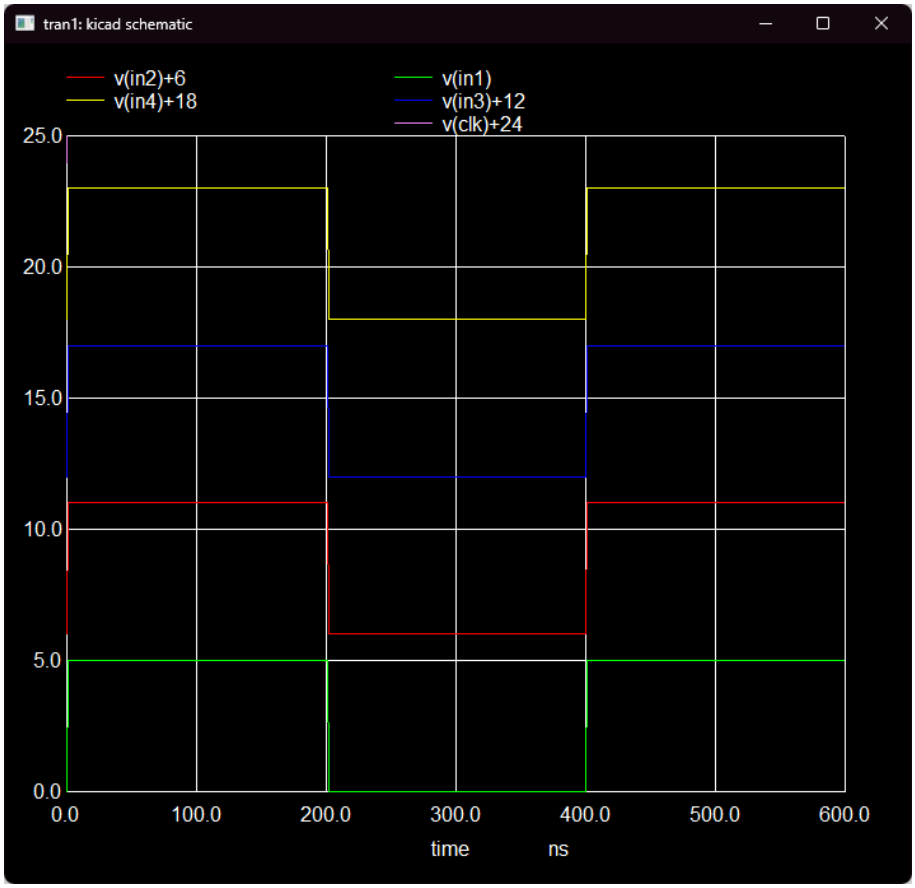

Figure 4.29: *Input Graph of CD4076B*

4.6.6 NgSpice Plot – Output

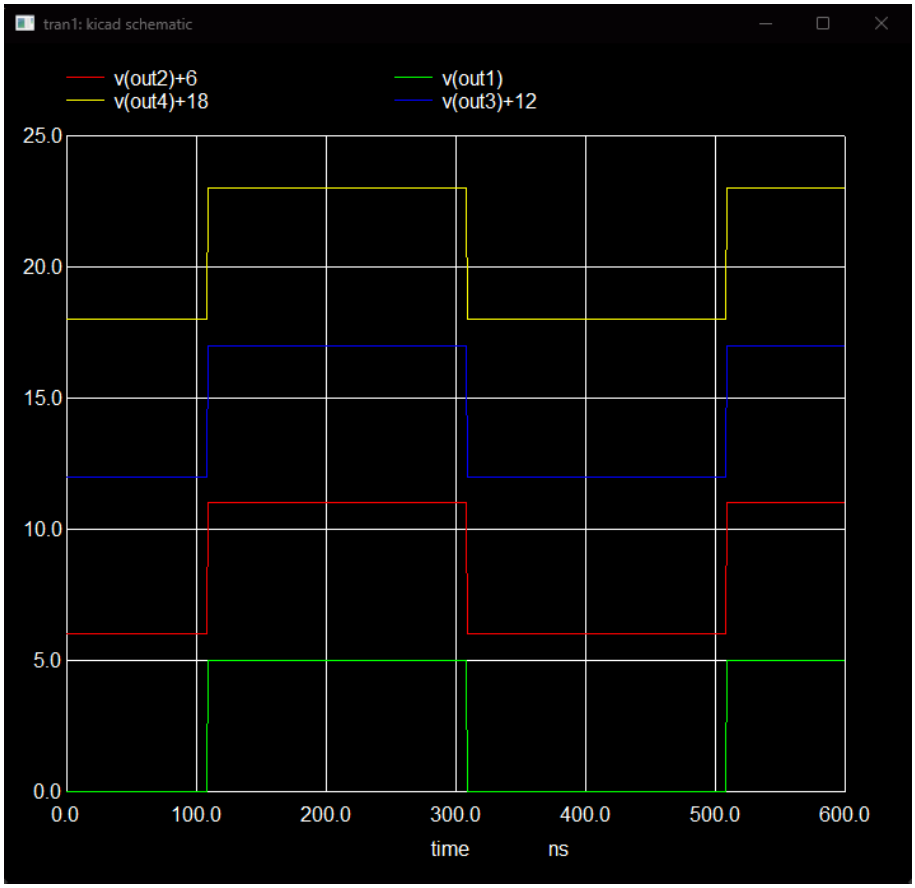

Figure 4.30: *Output Graph of CD4076B*

Chapter 5

Device Modeling

Device modelling in eSim refers to the process of designing fundamental semiconductor devices such as BJTs, MOSFETs, and diodes through physics-based SPICE-level modelling. This approach involves formulating accurate `.model` statements that encapsulate key parameters — such as threshold voltage, saturation current, carrier mobility, and junction capacitances — derived from manufacturer datasheets or empirical measurements.

5.1 IRF3205 – N-channel Power MOSFET

5.1.1 Description

The IRF3205 is an N-channel HEXFET power MOSFET manufactured by International Rectifier, designed for high-efficiency switching applications. Housed in a TO-220AB package, it is rated for a maximum drain-to-source voltage (VDSS) of 55 V, continuous drain currents up to 110 A at $= 25°.The device is optimized for low on-resistance (RDS(on) \approx 8.0\,\mathrm{m}\Omega)$ and high-speed switching.

5.1.2 SPICE Model

```
.MODEL IRF3205 NMOS( TPG=1 TOX=9.5n CJ=550u ETA=0.02125 VMAX=1.8E05 GAMMA=0.62 CGSO=2.4n
LD=50n MJSW=0.35 PB=1.1 CGBO=0.45n XJ=0.2U CGDO=0.5n KAPPA=0.1 LEVEL=3 VTO=3.0 NFS=7.20E11
THETA=0.23 CJSW=0.3n PHI=0.7 RSH=0 MJ=0.6 UO=420 KP=42 DELTA=0.88 NSUB=1.40E17 RD=0.004
RS=0.004 RG=1.65 )
```

Figure 5.1: *SPICE Model of IRF3205*

5.1.3 Simulation Setup and Methodology

To evaluate the static characteristics of the IRF3205 MOSFET model in eSim, a standard DC sweep test bench was set up. The N-channel MOSFET source terminal is connected to ground, with the bulk/body diode terminal also tied to ground. Two separate analyses were performed:

- **Output Characteristics (I*vs.* VDS):** A nested DC sweep where the drain-to-source voltage (VDS) was swept from 0 V to 20 V for multiple fixed gate voltages (VGS = 4 V to 6 V in 0.5 V steps).
- **Transfer Characteristics (I*vs.* VGS):** A single DC sweep of the gate voltage from 0 V to 6 V while holding VDS at 10 V.

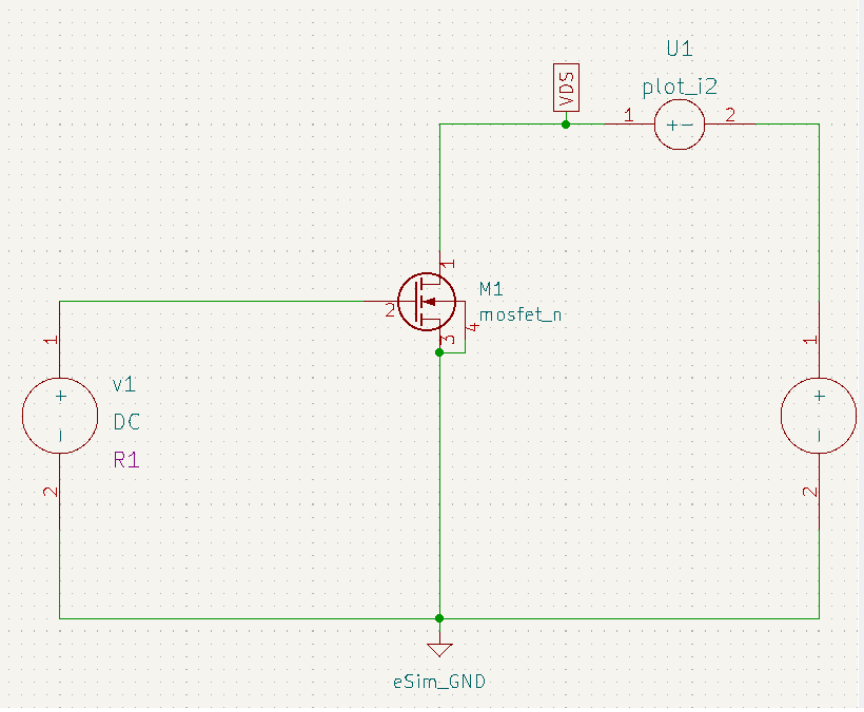

Figure 5.2: *Test Circuit for IRF3205*

5.1.4 Output Characteristics (I*vs.* VDS)

For each constant VGS curve, the drain current rises linearly in the ohmic (linear/triode) region at low VDS levels before saturating at higher VDS values. At lower gate drive voltages (around 4.5 V to 5.0 V), the drain current saturates near the 10 A – 40 A range. At higher gate voltages, the device demonstrates a steep initial slope, confirming the expected ultra-low RDS(on) ($\approx .0\,m\Omega$).

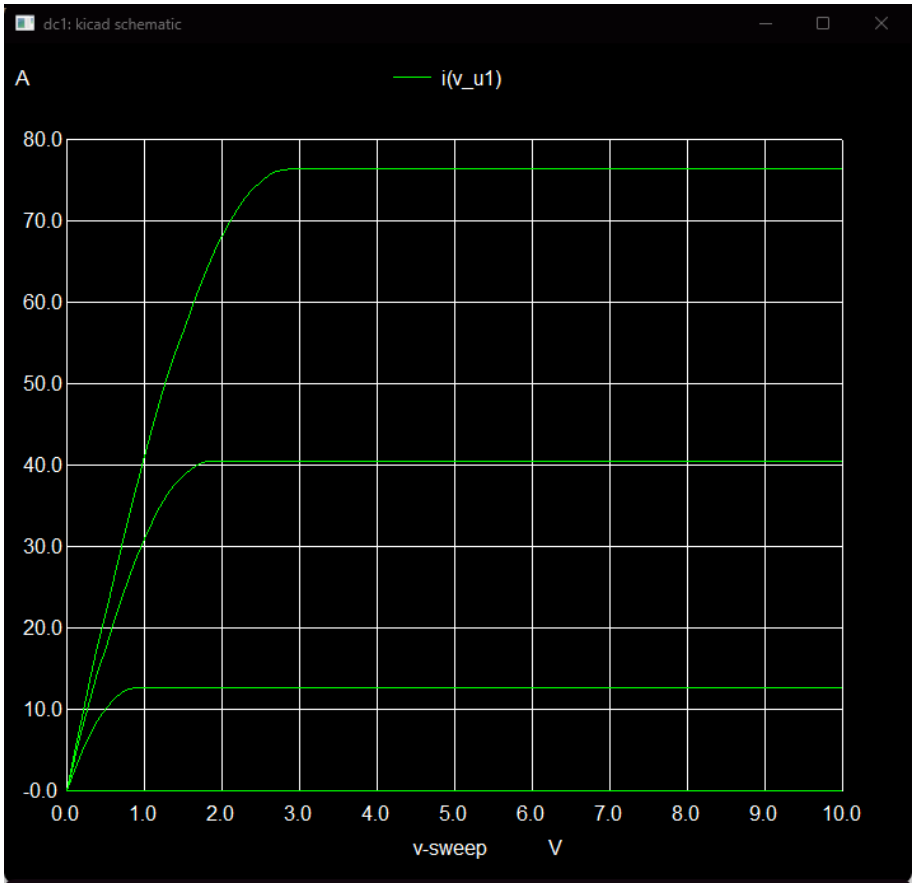

Figure 5.3: *Output Characteristic Curve of IRF3205*

5.1.5 Transfer Characteristics (I$vs.\ VGS$)

The curve shows negligible conduction for VGS $< 3.0\,\mathrm{V}$. Once VGS exceeds approximately $3.1\,\mathrm{V}$, the device turns on and I$risessteeply.Thesimulatedturn-ononset(\approx .1\,V)fallswithinthespecifieddatasheetrange(VGS(th) = 2.0\,Vto4.0\,V).Thecurrenttrajectoryclose datasheetcurve, reaching\approx\ AaroundVGS = 5.0\,V.$

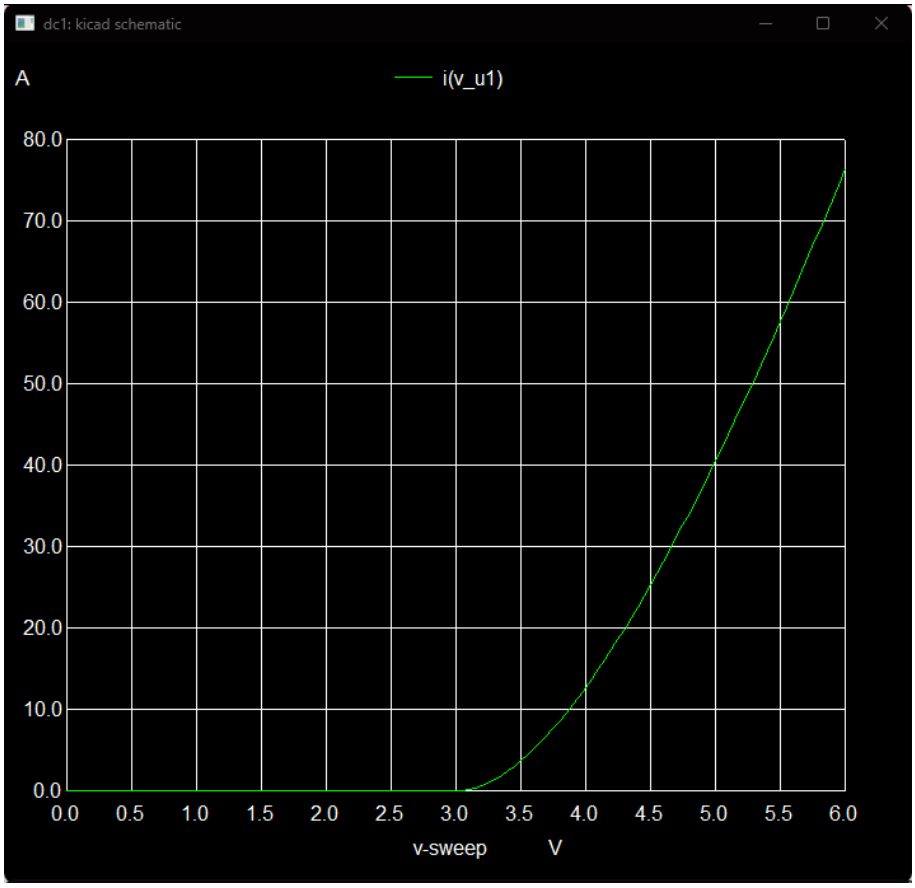

Figure 5.4: *Transfer Characteristic Curve of IRF3205*

5.2 IRF9540N – P-channel Power MOSFET

5.2.1 Description

The IRF9540N is a Fifth Generation P-channel HEXFET power MOSFET manufactured by International Rectifier, designed for high-efficiency switching and power management applications. Housed in a standard TO-220AB plastic package, it is rated for a maximum drain-to-source voltage (VDSS) of −100 V and continuous drain current up to −19 A. The device is characterized by low RDS(on) of 0.117 Ω.

5.2.2 SPICE Model

```
.MODEL IRF9540N PMOS( TPG=-1 TOX=600e-9 CJ=950u ETA=0.025 VMAX=0.3u GAMMA=0.52 CGSO=1.2e-9
LD=70n MJSW=0.25 PB=1 CGBO=0.45n XJ=0.2U CGDO=0.9e-9 KAPPA=8.0 LEVEL=1 VTO=-4.0 NFS=6.50E11
THETA=0.2 CJSW=0.2n PHI=0.7 RSH=2.5 MJ=0.5 UO=130 KP=9.5 DELTA=0.25 NSUB=6e16 )
```

Figure 5.5: *SPICE Model of IRF9540N*

5.2.3 Simulation Setup and Methodology

A P-channel MOSFET symbol was used. The source terminal is tied to ground and the gate is driven by a variable supply. Two analyses were performed:

- **Output Characteristics:** Nested DC sweep of the drain-to-source voltage magnitude from 0 V to 20 V for multiple fixed gate bias magnitudes (VGS = 4 V to 8 V).
- **Transfer Characteristics:** Single DC sweep of gate-to-source bias magnitude (VGS) from 0 V to 8 V while holding VDS constant.

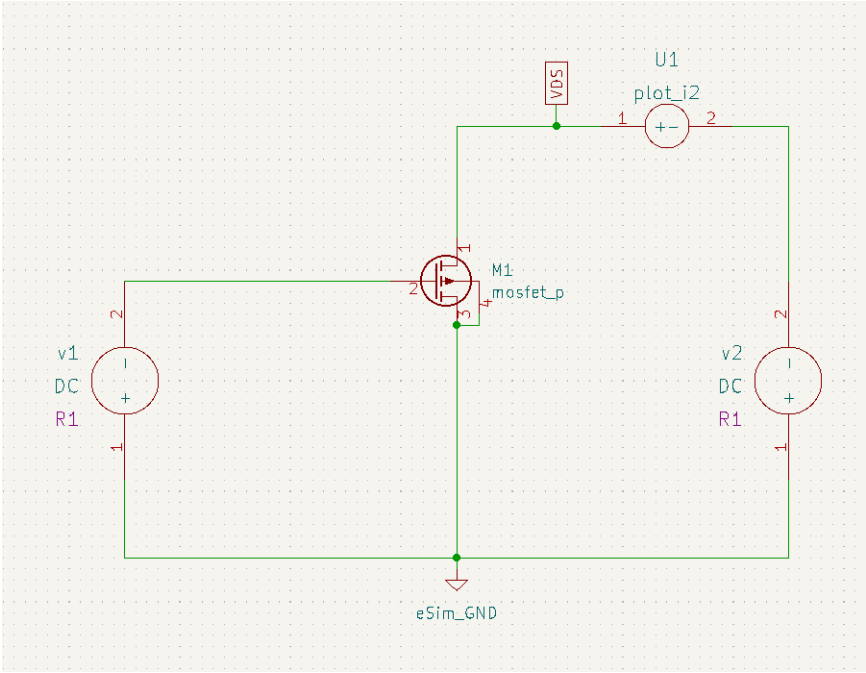

Figure 5.6: *Test Circuit for IRF9540N*

5.2.4 Output Characteristics (I$vs.$ VDS)

For each constant VGS curve, the drain current magnitude rises linearly in the ohmic region at low VDS levels before transitioning cleanly into saturation. The initial slope in the ohmic region reflects the low RDS(on) characteristic of 0.117 Ω.

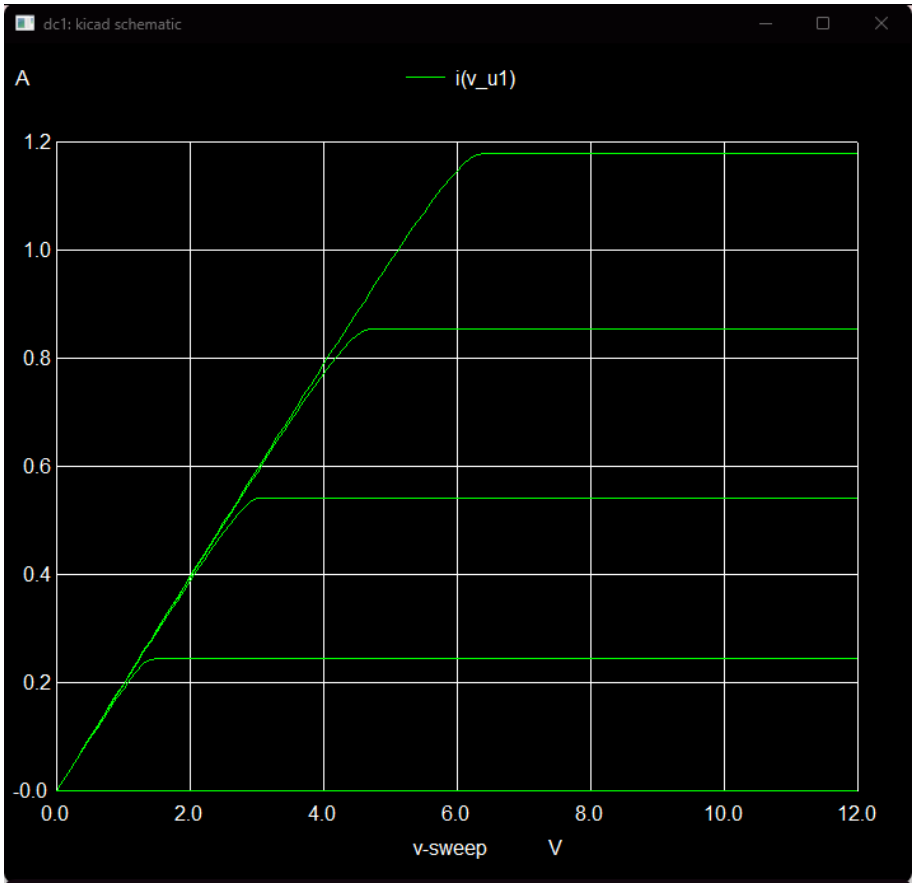

Figure 5.7: *Output Characteristic Curve of IRF9540N*

5.2.5 Transfer Characteristics (I*vs. VGS*)

The curve demonstrates zero conduction for VGS $< 4.0\,\text{V}$. Once VGS exceeds $4.0\,\text{V}$, the P-channel MOSFET turns on. Gate Threshold Voltage: The onset of conduction observed around VGS $= 4.0\,\text{V}$ matches the maximum Gate Threshold Voltage (VGS(th)) specified in the datasheet.

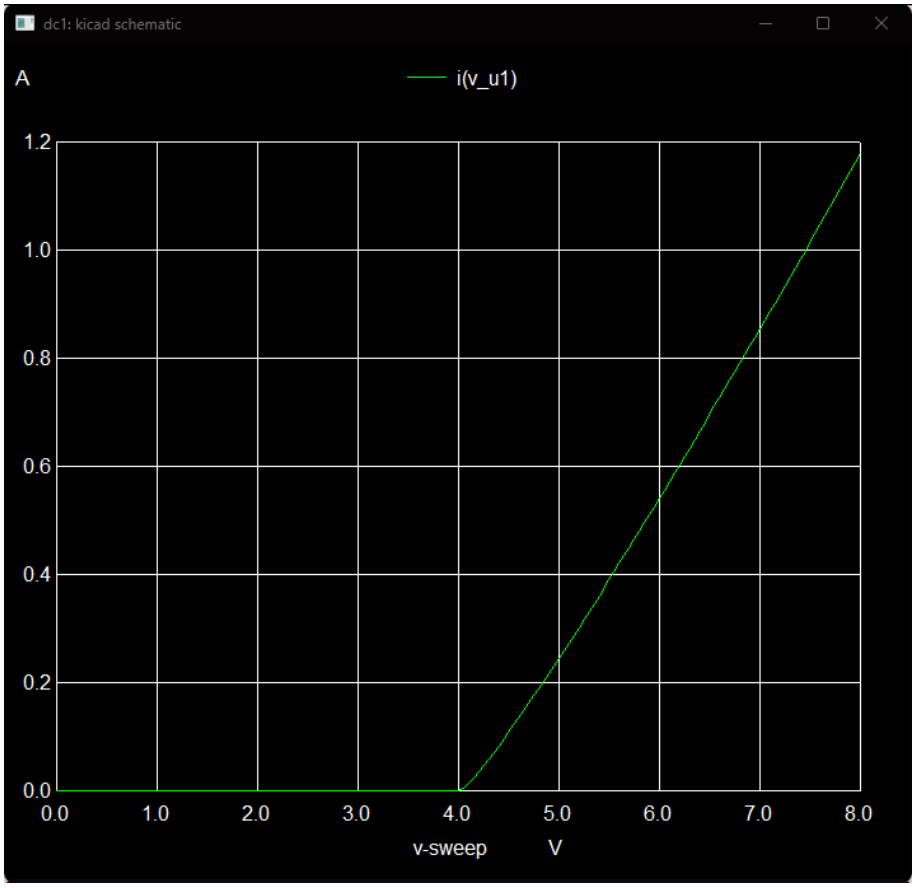

Figure 5.8: *Transfer Characteristic Curve of IRF9540N*

5.3 1N5408 – General-Purpose Power Silicon Rectifier Diode

5.3.1 Description

The 1N5408 is a general-purpose power silicon rectifier diode housed in a standard DO-201AD plastic package. It is designed for high efficiency, high current capability, and high surge capability in power rectification applications. The device is rated for a maximum average forward rectified current (IF(AV)) of 3 A, with a maximum repetitive peak reverse voltage (VRRM) of 1000 V.

5.3.2 SPICE Model

```
.MODEL IRF9540N PMOS( TPG=-1 TOX=600e-9 CJ=950u ETA=0.025 VMAX=0.3u GAMMA=0.52 CGSO=1.2e-9
LD=70n MJSW=0.25 PB=1 CGBO=0.45n XJ=0.2U CGDO=0.9e-9 KAPPA=8.0 LEVEL=1 VTO=-4.0 NFS=6.50E11
THETA=0.2 CJSW=0.2n PHI=0.7 RSH=2.5 MJ=0.5 UO=130 KP=9.5 DELTA=0.25 NSUB=6e16 )
```

Figure 5.9: *SPICE Model of 1N5408*

5.3.3 Simulation Setup and Methodology

Two DC sweep test benches were configured:

- **Forward Characteristics (I*vs.* V):** The diode was forward biased; the supply was swept from 0 V to 2 V in small steps to capture the exponential I-V characteristic.
- **Reverse Characteristics (I*vs.* V):** The diode was reverse biased; the supply was swept from 0 V to −1000 V to characterize the blocking capability.

5.3.4 Forward Characteristics (I*vs.* V)

Below approximately 0.4 V to 0.5 V, the diode exhibits negligible conduction. Beyond this turn-on knee voltage, the current increases exponentially. Conduction begins around 0.6 V, aligning with the standard silicon PN junction forward knee voltage. The curve trajectory reflects the low forward voltage drop rating specified as max 1.0 V at 3 A.

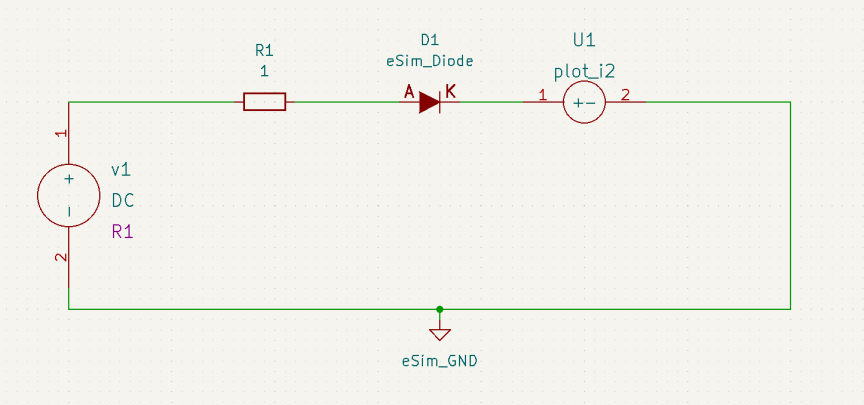

Figure 5.10: *Test Circuit for Forward Bias of 1N5408*

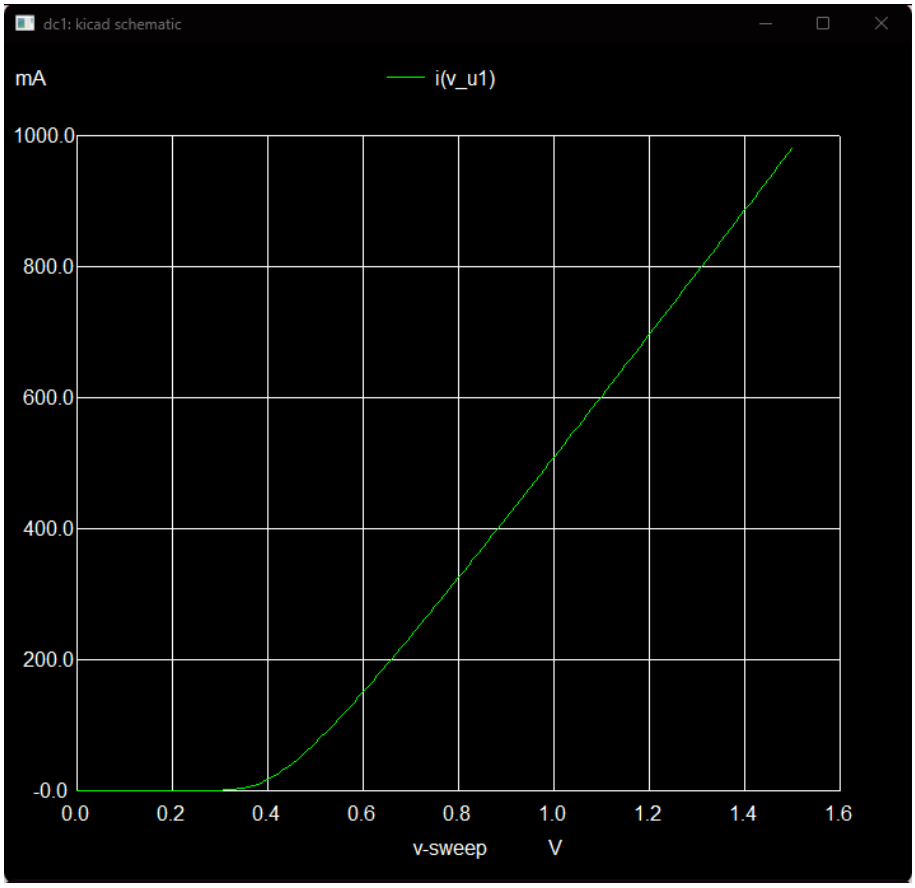

Figure 5.11: *Forward Bias Curve of 1N5408*

5.3.5 Reverse Characteristics (I*vs.* V)

During the reverse sweep from 0 V down to −1000 V, the diode maintains effective reverse blocking with negligible leakage current throughout the rated operating range. Maximum Repetitive Peak Reverse Voltage (VRRM) is verified at 1000 V.

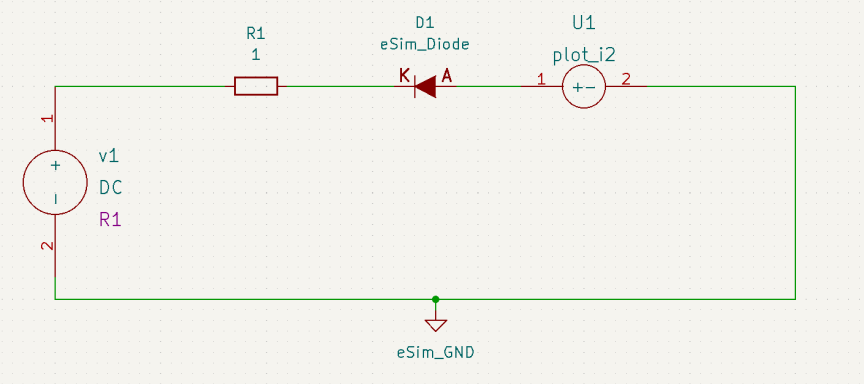

Figure 5.12: *Test Circuit for Reverse Bias of 1N5408*

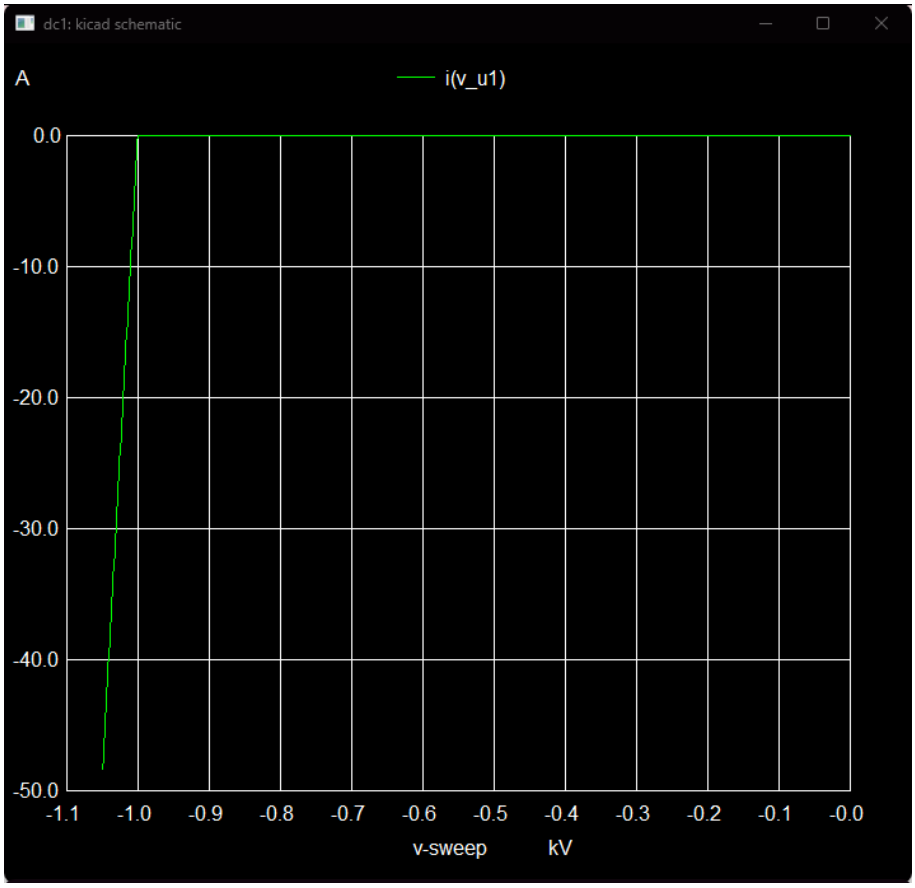

Figure 5.13: *Reverse Bias Curve of 1N5408*

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4. CD4041UB
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5. 74F538
   https://www.alldatasheet.com/datasheet-pdf/view/15452/PHILIPS/74F538.html
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   https://www.alldatasheet.com/datasheet-pdf/view/68328/IRF/IRF9540N.html
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   https://www.alldatasheet.com/datasheet-pdf/view/931127/DIODES/1N5408.html