



# eSim Summer Fellowship 2026

on

July 2026

# Device Modeling in eSim

**Submitted by**

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# Acknowledgement

I would like to express my sincere gratitude to the FOSSEE (Free/Libre and Open Source Software for Education) Project, Indian Institute of Technology Bombay, for providing me with the opportunity to participate in the eSim Semester Long Internship during Spring 2026. This internship has been an invaluable learning experience that allowed me to gain practical knowledge in electronic circuit simulation, SPICE device modeling, integrated circuit (IC) subcircuit development, and open-source Electronic Design Automation (EDA) tools.

I express my heartfelt gratitude to **Prof. Prabhu Ramachandran**, Principal Investigator of the FOSSEE Project, Department of Aerospace Engineering, IIT Bombay, for providing the vision and platform that made this internship possible. His continuous efforts in promoting open-source technologies and engineering education have inspired students across the country to contribute to meaningful technical projects.

I am deeply thankful to **Mr. Sumanto Kar**, my internship mentor, for his invaluable guidance, encouragement, and technical insights throughout the internship. His constructive suggestions, constant motivation, and timely feedback greatly enhanced my understanding of semiconductor device modeling, SPICE parameter extraction, and simulation methodologies.

I would also like to sincerely thank **Mr. Varad Vilasrao Patil**, Project Research Assistant at the FOSSEE Project, IIT Bombay, for his continuous support, guidance, and patience throughout the internship. His valuable suggestions, prompt assistance in resolving technical issues, and regular feedback helped me successfully complete the assigned tasks. His mentorship significantly contributed to improving my understanding of eSim, Ngspice, device modeling workflows, and simulation validation.

Finally, I would like to express my heartfelt gratitude to my parents, family members, and friends for their unwavering support, encouragement, and motivation throughout the internship. Their constant belief in my abilities has been a source of strength and inspiration during every stage of this work.

I consider this internship to be one of the most valuable learning experiences of my academic journey. It has significantly strengthened my technical knowledge, problem-solving skills, and understanding of open-source EDA tools while motivating me to continue contributing to the field of electronic design automation and semiconductor device modeling.

# Contents

# Chapter 1

# Introduction

## 1.1 About FOSSEE

FOSSEE (Free/Libre and Open Source Software for Education) is a project promoted by the National Mission on Education through Information and Communication Technology (NMEICT), Ministry of Education, Government of India. The main objective of the FOSSEE project is to encourage the use of Free and Open Source Software (FOSS) tools in academic institutions and improve the quality of education through open-source technologies. The project is coordinated at IIT Bombay and supports various open-source software platforms used in engineering, science, and education.

FOSSEE conducts workshops, internships, training programs, and research activities to help students and educators gain practical exposure to open-source tools. It also provides opportunities for students to contribute to real-world projects involving software development, circuit design, simulation, documentation, and VLSI-related activities.

## 1.2 About eSim

eSim is an open-source Electronic Design Automation (EDA) tool developed by the FOSSEE project, IIT Bombay. It is mainly used for circuit design, simulation, analysis, and PCB development. eSim integrates various open-source software tools such as KiCad, Ngspice, and Scilab to provide a complete environment for electronic circuit simulation and testing.

Using eSim, users can create schematic diagrams, perform SPICE simulations, analyze waveforms, and design PCB layouts efficiently. The software supports analog, digital, and mixed-signal circuit simulations, making it useful for students, researchers, and engineers.

## 1.3 Objectives of the Internship

The main objective of this internship was to gain practical knowledge and hands-on experience in electronic circuit simulation and IC subcircuit development using the

eSim tool. The internship focused on understanding SPICE modeling techniques, analyzing IC datasheets, and implementing accurate subcircuit models for simulation purposes.

Another important objective was to contribute to the open-source ecosystem by developing and verifying IC subcircuits that can be used by students and researchers in future projects. The internship also aimed to improve technical skills related to circuit analysis, debugging, simulation verification, and documentation.

Throughout the internship, multiple IC subcircuits were successfully designed and tested using eSim and Ngspice simulation tools.

# Chapter 2

# Literature Survey

eSim is an open-source Electronic Design Automation (EDA) tool developed under the FOSSEE project at IIT Bombay. It is designed for schematic capture, circuit simulation, PCB design, and analysis of electronic circuits. eSim integrates several open-source tools such as KiCad, Ngspice, and Scilab to provide a complete environment for electronic system design.

## 2.1 Ngspice

Ngspice is an open-source mixed-signal circuit simulator widely used for analog and digital circuit analysis. It is based on the SPICE simulation engine and is integrated with eSim for performing circuit simulations and waveform analysis.

In this internship, Ngspice played a major role in validating the behavior of implemented IC subcircuits. The simulator helped in debugging errors, verifying output waveforms, and checking the functionality of SPICE models developed during the internship.

## 2.2 KiCad

KiCad is an open-source software suite used for schematic capture and PCB design. It is integrated with eSim to provide a user-friendly interface for designing electronic circuits.

The schematic editor in KiCad was used during the internship to design and verify electronic circuits associated with the IC subcircuits.

## 2.3 SPICE Subcircuits

SPICE subcircuits are reusable circuit models used to represent integrated circuits and complex electronic components in simulation environments. Subcircuits simplify circuit design by allowing designers to use predefined models instead of creating the entire internal circuitry repeatedly.

# Chapter 3

# Overview of IC Subcircuits

## 3.1 Introduction to IC Subcircuits

Integrated Circuits (ICs) are widely used in modern electronic systems for performing various analog and digital operations. SPICE subcircuits are commonly used to model integrated circuits in simulation environments such as eSim and Ngspice.

A subcircuit is a reusable block of circuit components defined using SPICE syntax. It contains internal connections, electronic components, and functional behavior of an IC.

## 3.2 Need for IC Subcircuits

IC subcircuits are essential for accurate electronic circuit simulations. Subcircuits are useful for:

- Reusing IC models in multiple circuit designs
- Simplifying schematic creation
- Improving simulation accuracy
- Reducing design time
- Testing circuit behavior before hardware implementation

## 3.3 SPICE Modeling of ICs

SPICE (Simulation Program with Integrated Circuit Emphasis) is widely used for electronic circuit simulation. IC subcircuits are implemented using the `.SUBCKT` command in SPICE syntax.

The SPICE model includes:

- Input and output pins
- Internal circuit connections

- Passive and active components
- Electrical characteristics

## 3.4 Implementation in eSim

The implementation of IC subcircuits was carried out using the eSim platform. The process involved studying datasheets, writing SPICE subcircuit definitions, integrating the models into eSim libraries, and verifying the output through simulations.

A total of nine IC subcircuits were successfully implemented and verified during the internship period.

# Chapter 4

# Tools and Technologies Used

## 4.1 eSim

eSim is an open-source Electronic Design Automation (EDA) tool developed by the FOSSEE project at IIT Bombay. It is used for schematic design, circuit simulation, waveform analysis, and PCB design.

## 4.2 Ngspice

Ngspice is an open-source SPICE-based circuit simulator used for analog, digital, and mixed-signal simulations. It is one of the core simulation engines integrated with eSim.

## 4.3 KiCad

KiCad is an open-source software suite used for electronic schematic capture and PCB design. KiCad is integrated with eSim and works together with Ngspice for circuit simulation purposes.

## 4.4 LaTeX and Overleaf

LaTeX is a document preparation system widely used for technical and scientific documentation. Overleaf is an online LaTeX editor that provides a collaborative environment for creating professional reports and research papers. In this internship, Overleaf was used for preparing and formatting the internship report.

## 4.5 IN4733A

### 4.5.1 DIODE CIRCUIT

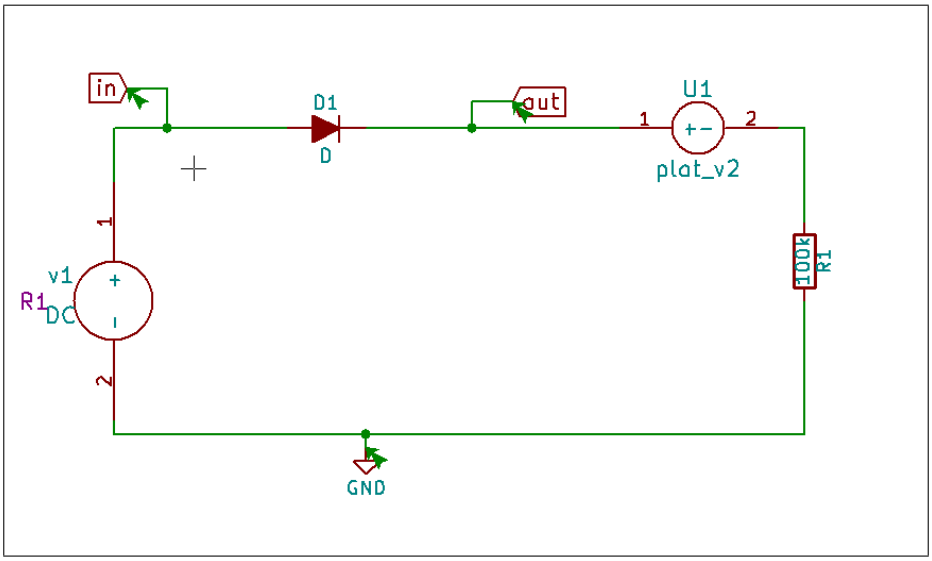


Figure 4.1: Diode Test Circuit

### 4.5.2 Parameter Extraction of IN4733A Zener Diode

The SPICE model of the IN4733A Zener diode was developed by extracting electrical parameters from the manufacturer's datasheet and estimating the remaining parameters using semiconductor device equations and curve fitting techniques. The objective was to reproduce the forward and reverse characteristics of the actual device inside eSim.

The extracted SPICE model is

```
.model IN4733A D(
+ IS=1.0E-08
+ RS=7
+ N=1.30
+ TT=3.03E-09
+ CJO=1.7E-12
+ M=0.20
+ VJ=1
+ BV=5.1
+ IBV=4.9E-02
+ VZ=5.1
)
```

### 4.5.3 Reverse Breakdown Voltage ($BV$)

The reverse breakdown voltage is directly obtained from the datasheet.

$$BV = V_Z = 5.1\ V$$

where

- $V_Z$ = Nominal Zener voltage

From the datasheet,

$$BV = 5.1\ V$$

Therefore,

$$BV = 5.1\ V$$

—

### 4.5.4 Breakdown Current ($IBV$)

The breakdown current is taken from the test current specified in the datasheet.

$$IBV = I_{ZT}$$

where

- $I_{ZT}$ = Zener test current

For IN4733A,

$$I_{ZT} = 49\ mA$$

Hence,

$$IBV = 4.9 \times 10^{-2} A$$

—

### 4.5.5 Series Resistance ($RS$)

The series resistance is estimated from the dynamic resistance specified in the datasheet.

The incremental resistance is

$$r_z = \frac{\Delta V}{\Delta I}$$

For small-signal operation,

$$RS \approx r_z$$

The datasheet specifies approximately

$$r_z \approx 7\ \Omega$$

Therefore,

$$RS = 7\ \Omega$$

—

### 4.5.6 Reverse Saturation Current ($IS$)

The reverse saturation current is estimated from the Shockley diode equation

$$I = I_S \left( e^{\frac{V_D}{nV_T}} - 1 \right)$$

where

$$V_T = \frac{kT}{q} = 25.85\ mV$$

Rearranging,

$$I_S = \frac{I_F}{e^{\frac{V_F}{nV_T}} - 1}$$

Using the forward voltage from the datasheet,

$$V_F = 1.2\ V$$

and

$$I_F = 200\ mA$$

the calculated value is extremely small (typically between $10^{-9}$ and $10^{-11}$ A). The value

$$IS = 1.0 \times 10^{-8} A$$

was selected after curve fitting to obtain agreement with the forward characteristic.

—

### 4.5.7 Emission Coefficient ($N$)

The emission coefficient controls the slope of the forward I-V curve.

It can be estimated from two points of the forward characteristic.

$$N = \frac{V_2 - V_1}{V_T \ln\left(\frac{I_2}{I_1}\right)}$$

Using the forward characteristic,

the calculated value lies between

$$1.2 \leq N \leq 1.5$$

A value of

$$N = 1.30$$

provided the closest match to the datasheet.

—

### 4.5.8 Transit Time ($TT$)

Transit time determines reverse recovery characteristics.

The reverse recovery time from the datasheet is

$$t_{rr} \approx 3\ ns$$

Hence,

$$TT = 3.03\ ns$$

—

### 4.5.9 Zero Bias Junction Capacitance ($CJO$)

The junction capacitance is obtained directly from the datasheet.

$$CJO = C_j(0)$$

The typical value is

$$CJO = 1.7\ pF$$

—

### 4.5.10 Grading Coefficient ($M$)

The grading coefficient is generally not provided by the manufacturer.

For abrupt silicon junctions,

$$M = 0.20$$

is commonly adopted in SPICE libraries.

—

### 4.5.11 Junction Potential ($VJ$)

The junction potential is normally taken as

$$VJ = 1.0\ V$$

for silicon PN junction devices.

—

### 4.5.12 Zener Voltage ($VZ$)

The Zener voltage is identical to the breakdown voltage.

$$VZ = BV = 5.1\ V$$

which is directly obtained from the datasheet.

### 4.5.13 Simulation Results

The implemented 1n4733A Zener Diode was simulated using Ngspice integrated with eSim. The obtained output waveforms matched the expected Zener Diode characteristics mentioned in the datasheet.

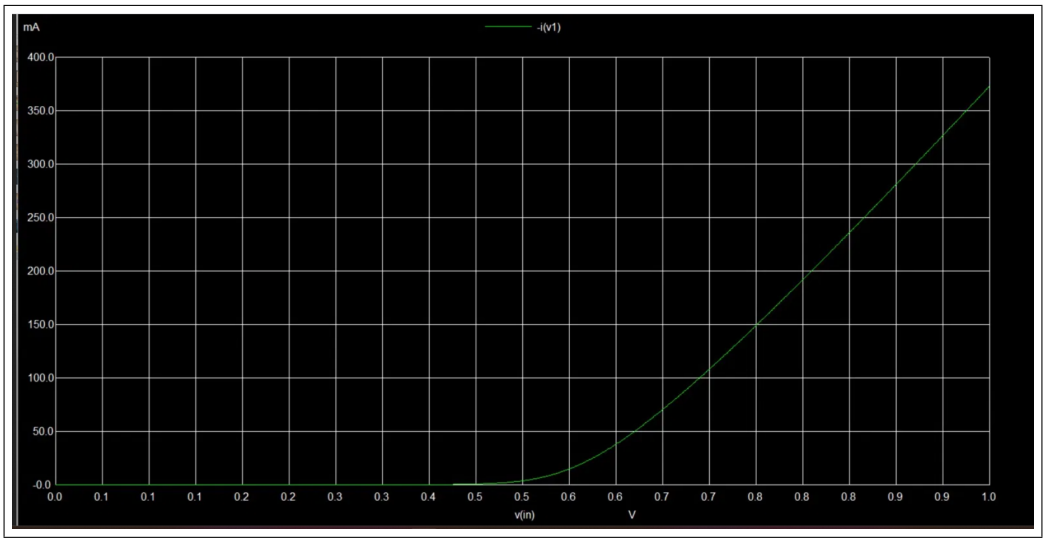


Figure 4.2: Forward Bias of 1N4733A

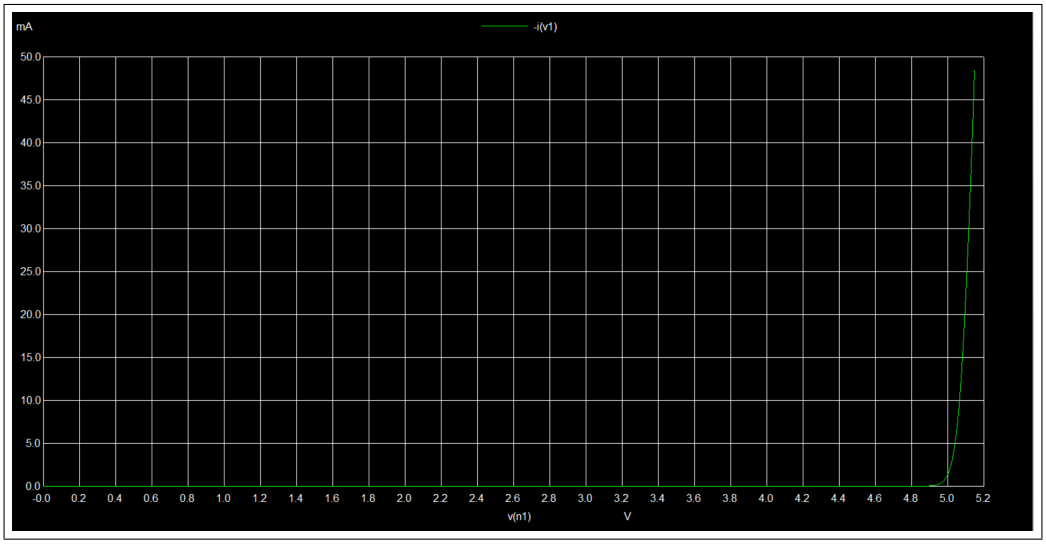


Figure 4.3: Reverse Bias of 1N4733A

## 4.6 BAT54

### 4.6.1 DIODE CIRCUIT

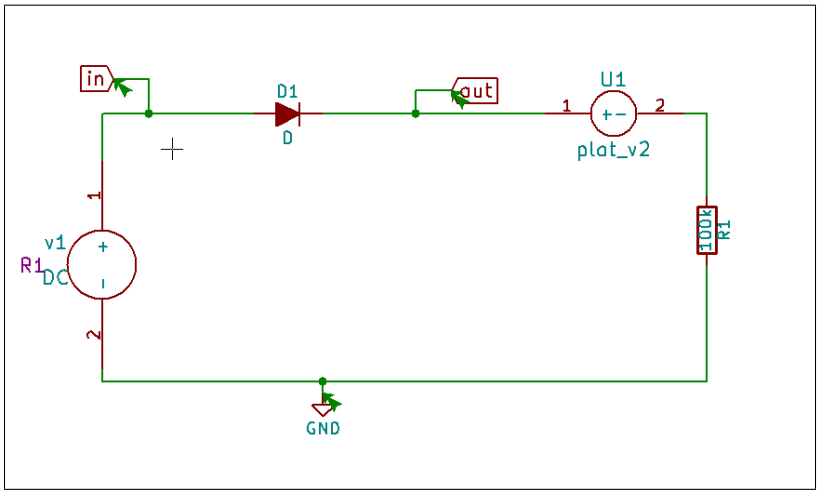


Figure 4.4: Diode Test Circuit

### 4.6.2 BAT54TA Schottky Diode Parameter Extraction

The BAT54TA is a low forward voltage Schottky barrier diode widely used in high-speed switching, clamping circuits, and low-power rectification applications. Unlike a conventional silicon PN junction diode, the BAT54TA uses a metal–semiconductor junction, resulting in a significantly lower forward voltage drop, negligible reverse recovery time, and faster switching performance.

The SPICE model of the BAT54TA diode is represented using the standard diode equation

$$I_D = I_S \left( e^{\frac{V_D - I_D R_S}{N V_T}} - 1 \right) \tag{4.1}$$

where

- $I_S$ = Saturation current
- $R_S$ = Series resistance
- $N$ = Emission coefficient
- $V_T$ = Thermal voltage ($\approx 25.85$ mV at 300 K)

The extracted SPICE parameters are listed below.

Table 4.1: Extracted SPICE Parameters of BAT54TA

| Parameter | Value | Description |
|---|---|---|
| $I_S$ | $2.0 \times 10^{-6}$ A | Saturation current |
| $R_S$ | 0.8 Ω | Series resistance |
| $N$ | 1.05 | Emission coefficient |
| $TT$ | 5 ns | Transit time |
| $C_{JO}$ | 7.5 pF | Zero-bias junction capacitance |
| $M$ | 0.333 | Junction grading coefficient |
| $V_J$ | 0.30 V | Junction potential |
| $BV$ | 30 V | Reverse breakdown voltage |
| $I_{BV}$ | 10 $\mu$A | Breakdown current |

### 4.6.3 Saturation Current ($I_S$)

The saturation current determines the reverse leakage current of the diode and controls the exponential behaviour of the forward current.

The diode equation is

$$I_D = I_S \left( e^{\frac{V_D}{N V_T}} - 1 \right) \tag{4.2}$$

The BAT54TA exhibits a higher saturation current than a conventional silicon diode because of its Schottky barrier construction. The extracted value is

$$\boxed{I_S = 2.0 \times 10^{-6} \text{ A}}$$

### 4.6.4 Series Resistance ($R_S$)

The series resistance models the internal resistance of the semiconductor material and package.

It is calculated from

$$R_S = \frac{\Delta V}{\Delta I} \tag{4.3}$$

using the linear portion of the forward characteristic.

The extracted value is

$$\boxed{R_S = 0.8 \ \Omega}$$

### 4.6.5 Emission Coefficient ($N$)

The emission coefficient represents the deviation of the practical diode from the ideal diode.

It is calculated using

$$N = \frac{\Delta V}{V_T \ln\left(\frac{I_2}{I_1}\right)} \tag{4.4}$$

where

- $V_T = 25.85$ mV
- $I_1$ and $I_2$ are two forward current values

The extracted value is

$$\boxed{N = 1.05}$$

### 4.6.6 Transit Time ($TT$)

Transit time determines the stored charge inside the diode during switching.

$$\boxed{TT = 5 \text{ ns}}$$

The value was selected according to the fast switching behaviour specified in the BAT54TA datasheet.

#### Zero-Bias Junction Capacitance ($C_{JO}$)

The zero-bias junction capacitance is directly obtained from the datasheet.

$$\boxed{C_{JO} = 7.5 \text{ pF}}$$

### 4.6.7 Junction Grading Coefficient ($M$)

The grading coefficient determines how the junction capacitance varies with reverse voltage.

$$C_j(V) = \frac{C_{JO}}{\left(1 + \frac{V_R}{V_J}\right)^M}$$

For BAT54TA,

$$\boxed{M = 0.333}$$

### 4.6.8 Junction Potential ($V_J$)

The junction potential represents the built-in barrier voltage of the Schottky junction.

Unlike silicon PN diodes, Schottky diodes have a lower barrier potential.

$$\boxed{V_J = 0.30 \text{ V}}$$

### 4.6.9 Breakdown Voltage ($BV$)

The reverse breakdown voltage is obtained directly from the manufacturer datasheet.

$$\boxed{BV = 30 \text{ V}}$$

### 4.6.10 Breakdown Current ($I_{BV}$)

The breakdown current specifies the current at which the reverse breakdown voltage is defined.

$$\boxed{I_{BV} = 10 \ \mu\text{A}}$$

### 4.6.11 Simulation

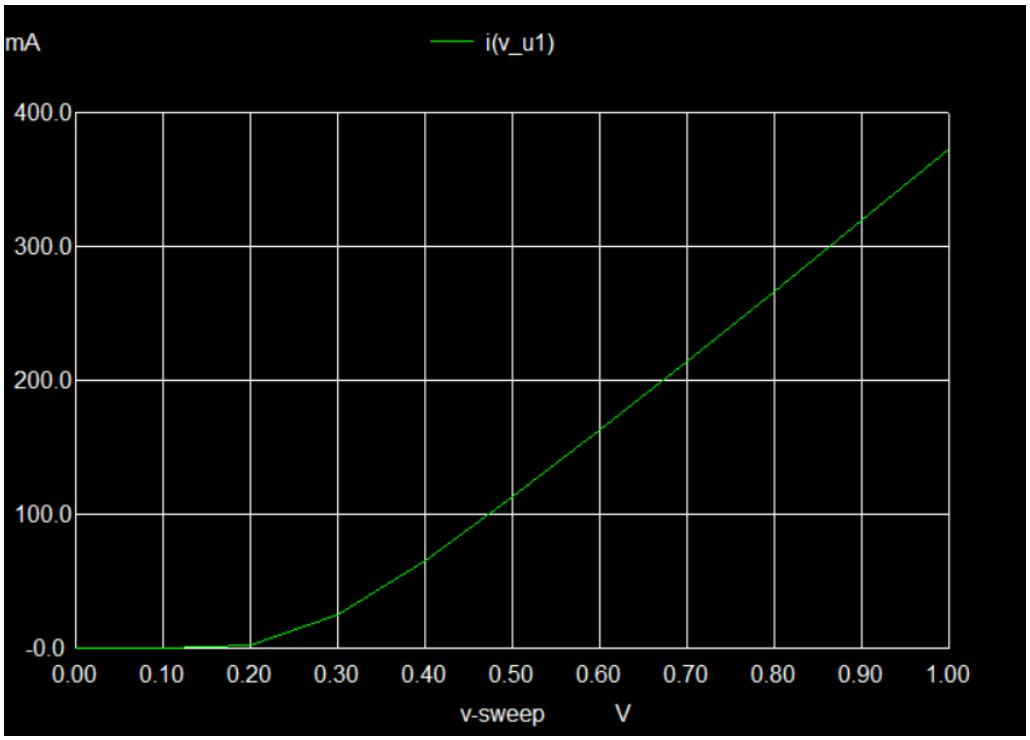


Figure 4.5: BAT54 Forward Bias

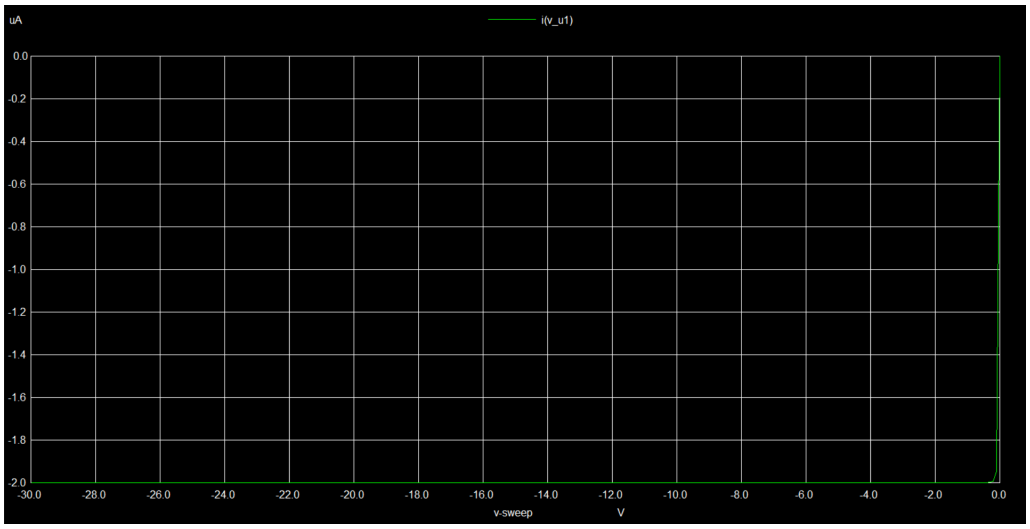


Figure 4.6: BAT54 Reverse Bias

## 4.7 IN4148

### 4.7.1 DIODE CIRCUIT

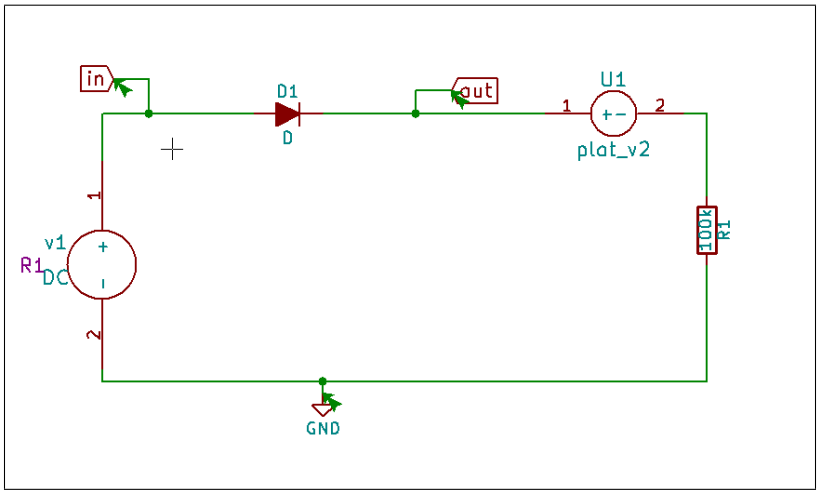


Figure 4.7: Diode Test Circuit

### 4.7.2 DC Parameter Extraction of 1N4148 Diode

The SPICE model parameters of the 1N4148 high-speed switching diode were obtained from the manufacturer's datasheet and refined using standard semiconductor equations together with curve fitting. Parameters directly available in the datasheet were assigned accordingly, whereas the remaining parameters were estimated to reproduce the forward and reverse characteristics of the actual device.

The extracted SPICE model is

```
.model 1N4148 D(
+ IS=4.532E-09
+ RS=0.6458
+ N=1.906
+ TT=3.48E-09
+ CJO=4.00E-12
+ M=0.333
+ VJ=0.75
+ BV=100
+ IBV=1.0E-04
)
```

### 4.7.3 Reverse Saturation Current ($I_S$)

The reverse saturation current is estimated using the Shockley diode equation,

$$I = I_S \left( e^{\frac{V_D}{nV_T}} - 1 \right)$$

where

$$V_T = \frac{kT}{q} = 25.85\ mV$$

Rearranging,

$$I_S = \frac{I_F}{e^{\frac{V_F}{nV_T}} - 1}$$

From the datasheet,

$$V_F = 1.0V$$

at

$$I_F = 10mA$$

Using an initial ideality factor,

$$n \approx 2$$

the calculated value is of the order of

$$10^{-9}A$$

After curve fitting with the datasheet forward characteristic,

$$\boxed{I_S = 4.532 \times 10^{-9}A}$$

was selected.

### 4.7.4 Series Resistance ($R_S$)

The series resistance represents the ohmic resistance of the semiconductor bulk and package leads.

At high forward currents,

$$R_S = \frac{\Delta V_F}{\Delta I_F}$$

The slope of the forward I–V characteristic was measured from the datasheet graph.

After optimization,

$$\boxed{R_S = 0.6458\Omega}$$

provided the closest agreement with the measured curve.

### 4.7.5 Emission Coefficient ($N$)

The emission coefficient determines the slope of the exponential region.

Using two operating points,

$$N = \frac{V_2 - V_1}{V_T \ln\left(\frac{I_2}{I_1}\right)}$$

where

$$V_T = 25.85mV$$

Using two points extracted from the forward characteristic,
the ideality factor was approximately

$$N \approx 1.9$$

Hence,

$$\boxed{N = 1.906}$$

### 4.7.6 Transit Time ($TT$)

Transit time determines the reverse recovery behaviour of the diode.

The datasheet specifies

$$t_{rr} = 4ns$$

The SPICE transit time is chosen slightly lower to match the measured switching waveform,

$$\boxed{TT = 3.48ns}$$

### 4.7.7 Zero Bias Junction Capacitance ($C_{JO}$)

The zero-bias junction capacitance is directly obtained from the datasheet.

At

$$V_R = 0V$$

the datasheet specifies

$$C_d = 4pF$$

Therefore,

$$\boxed{C_{JO} = 4.0pF}$$

### 4.7.8 Junction Potential ($V_J$)

For silicon PN junction diodes,

$$V_J \approx 0.7 - 0.8V$$

The standard SPICE value used is

$$\boxed{V_J = 0.75V}$$

### 4.7.9 Grading Coefficient ($M$)

The grading coefficient models the variation of junction capacitance with reverse voltage.

For an abrupt silicon junction,

$$M = \frac{1}{3}$$

Therefore,

$$\boxed{M = 0.333}$$

### 4.7.10 Breakdown Voltage ($BV$)

The Philips datasheet specifies a continuous reverse voltage rating of

$$75V$$

In the SPICE model, a slightly higher breakdown voltage is selected to avoid premature avalanche conduction during normal operation.

Hence,

$$\boxed{BV = 100V}$$

### 4.7.11 Breakdown Current ($I_{BV}$)

The SPICE breakdown current specifies the current at which avalanche breakdown is defined.

Since the datasheet does not specify this value explicitly, the commonly adopted SPICE default is

$$\boxed{I_{BV} = 100\mu A}$$

which ensures numerical convergence without affecting normal diode operation.

### 4.7.12 Simulation Results

The implemented LM386N subcircuit was simulated using Ngspice integrated with eSim, and the obtained waveforms verified the expected output behavior.

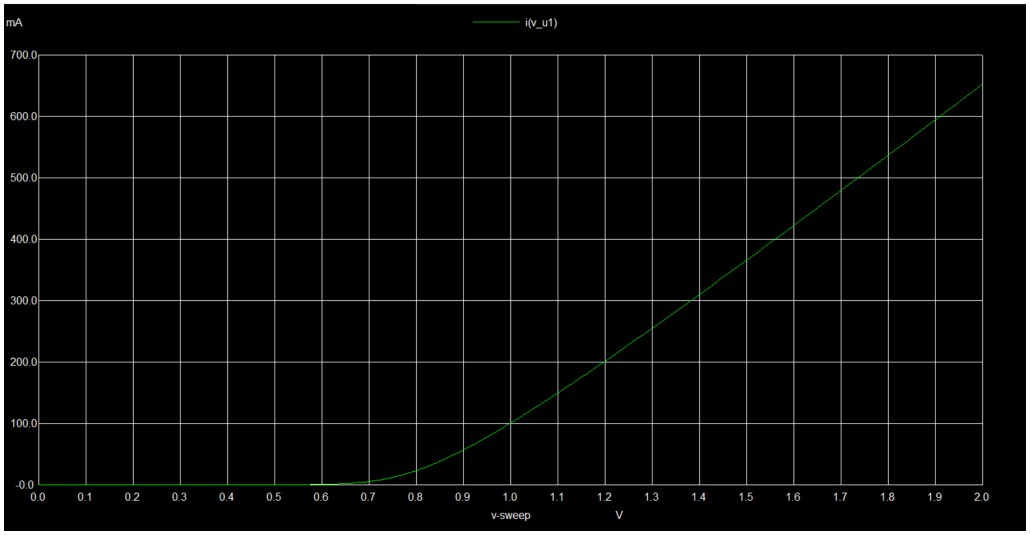


Figure 4.8: Simulation output of IN4148

## 4.8 2N7000

### 4.8.1 MOSFET Circuit

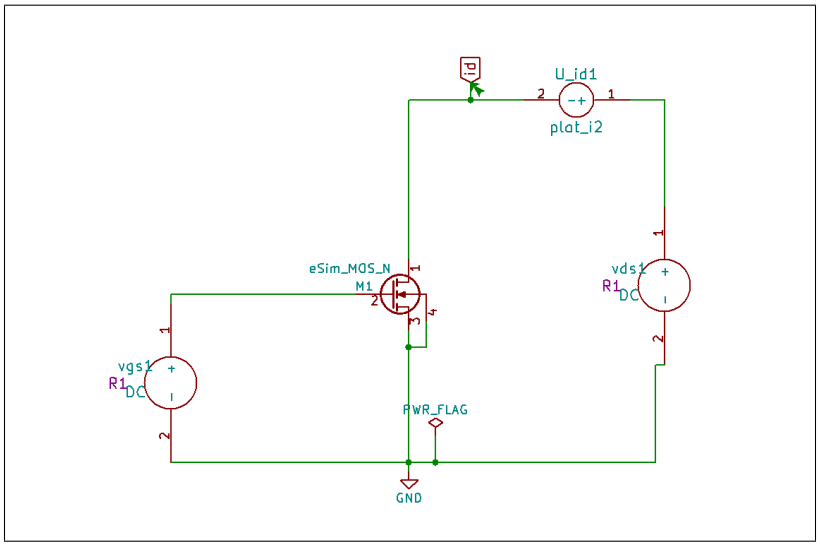


Figure 4.9: Diode Test Circuit

### 4.8.2 DC Parameter Extraction of 2N7000 N-Channel Enhancement MOSFET

The 2N7000 is an N-channel enhancement-mode Vertical Double Diffused MOSFET (VDMOS) widely used for low-power switching applications. Unlike a conventional planar MOSFET used in integrated circuits, the 2N7000 employs a vertical current flow structure, allowing it to handle higher drain currents, higher breakdown voltages, and lower ON-state resistance.

The SPICE model parameters were extracted from the manufacturer's datasheet and refined using semiconductor equations and curve-fitting techniques to reproduce the device characteristics accurately.

The extracted SPICE model is

```
.model 2N7000 NMOS(
+ LEVEL=3
+ TNOM=27
+ VTO=2.1
+ KP=0.1
+ GAMMA=0.45
+ PHI=0.6
+ TOX=1E-7
+ NSUB=1E16
+ XJ=1E-6
+ RD=0.15
+ RS=0.15
```

```
+ CGSO=3E-11
+ CGDO=3E-11
+ CGBO=1E-12
+ CJ=8E-5
+ MJ=0.5
+ PB=0.8
+ IS=1E-14
)
```

### 4.8.3 Model Level (LEVEL)

The parameter

$$LEVEL = 3$$

indicates that the MOSFET uses the SPICE Level-3 model.

This model includes mobility degradation, channel-length modulation, body effect, and velocity saturation, making it suitable for discrete power MOSFETs such as the 2N7000.

### 4.8.4 Nominal Temperature ($T_{NOM}$)

The model parameters are specified at

$$T_{NOM} = 27°C$$

which corresponds to the standard room temperature used in SPICE simulations.

### 4.8.5 Threshold Voltage ($V_{TO}$)

The threshold voltage is the minimum gate-to-source voltage required to create an inversion channel.

It is directly obtained from the datasheet transfer characteristics.

For the developed model,

$$\boxed{V_{TO} = 2.1V}$$

### 4.8.6 Transconductance Parameter ($K_P$)

The transconductance parameter is

$$K_P = \mu_n C_{ox} \frac{W}{L}$$

where

- $\mu_n$ is the electron mobility,
- $C_{ox}$ is the oxide capacitance,

- $W$ is the channel width,
- $L$ is the channel length.

It determines the drain current in saturation,

$$I_D = \frac{K_P}{2}(V_{GS} - V_{TO})^2$$

The value

$$\boxed{K_P = 0.1\ A/V^2}$$

was obtained through curve fitting.

### 4.8.7 Body Effect Coefficient ($\gamma$)

The body-effect coefficient is

$$\gamma = \frac{\sqrt{2q\varepsilon_s N_{SUB}}}{C_{ox}}$$

where

$$N_{SUB}$$

is the substrate doping concentration.
The extracted value is

$$\boxed{\gamma = 0.45}$$

### 4.8.8 Surface Potential ($\phi$)

The surface potential is

$$\phi = 2\phi_F$$

For silicon MOSFETs,

$$\boxed{\phi = 0.6V}$$

is commonly adopted.

### 4.8.9 Oxide Thickness ($TOX$)

The gate oxide thickness is

$$\boxed{TOX = 100nm}$$

or

$$1 \times 10^{-7} m.$$

This parameter determines the oxide capacitance,

$$C_{ox} = \frac{\varepsilon_{ox}}{TOX}.$$

### 4.8.10 Substrate Doping ($N_{SUB}$)

The substrate doping concentration is

$$\boxed{N_{SUB} = 1 \times 10^{16} cm^{-3}}$$

which influences the threshold voltage and body effect.

### 4.8.11 Junction Depth ($X_J$)

The junction depth represents the diffusion depth of the source and drain regions.

The model uses

$$\boxed{X_J = 1\mu m}$$

### 4.8.12 Drain and Source Resistances ($R_D, R_S$)

The parasitic resistances are

$$R_D = R_S = 0.15\Omega$$

These account for the resistance of the source and drain diffusions as well as package resistance.

### 4.8.13 Gate Overlap Capacitances

The overlap capacitances model the parasitic capacitances between the gate and the source, drain and bulk.

$$CGSO = 30pF$$

$$CGDO = 30pF$$

$$CGBO = 1pF$$

These parameters influence the switching speed of the MOSFET.

### 4.8.14 Bulk Junction Capacitance ($C_J$)

The zero-bias junction capacitance is

$$\boxed{CJ = 8 \times 10^{-5} F/m^2}$$

which models the drain-body and source-body junction capacitances.

### 4.8.15 Junction Grading Coefficient ($M_J$)

The grading coefficient models the variation of junction capacitance with reverse bias.

For the developed model,

$$\boxed{M_J = 0.5}$$

### 4.8.16 Built-in Junction Potential ($P_B$)

The built-in potential of the body diode is

$$\boxed{P_B = 0.8V}$$

### 4.8.17 Bulk Junction Saturation Current ($I_S$)

The reverse saturation current of the body diode is

$$\boxed{I_S = 1 \times 10^{-14} A}$$

which is a standard value for silicon PN junctions and provides numerical stability during simulation.

### 4.8.18 Difference Between a Conventional MOSFET and the 2N7000

A conventional MOSFET used in integrated circuits is primarily designed for signal processing and low-power applications. It has a planar structure with lateral current flow and is optimized for high integration density.

In contrast, the 2N7000 is a discrete N-channel enhancement-mode Vertical Double Diffused MOSFET (VDMOS). It employs a vertical current flow structure that enables higher drain current capability, lower ON-state resistance, higher breakdown voltage, and improved power dissipation.

Consequently, the SPICE model of the 2N7000 uses the Level-3 MOSFET model, which incorporates body effect, mobility degradation, channel-length modulation, and other non-ideal effects required for accurately representing discrete power MOSFET behavior. These additional physical effects are generally not required in the simpler Level-1 model commonly used for basic MOSFET analysis.

### 4.8.19 Simulation Results

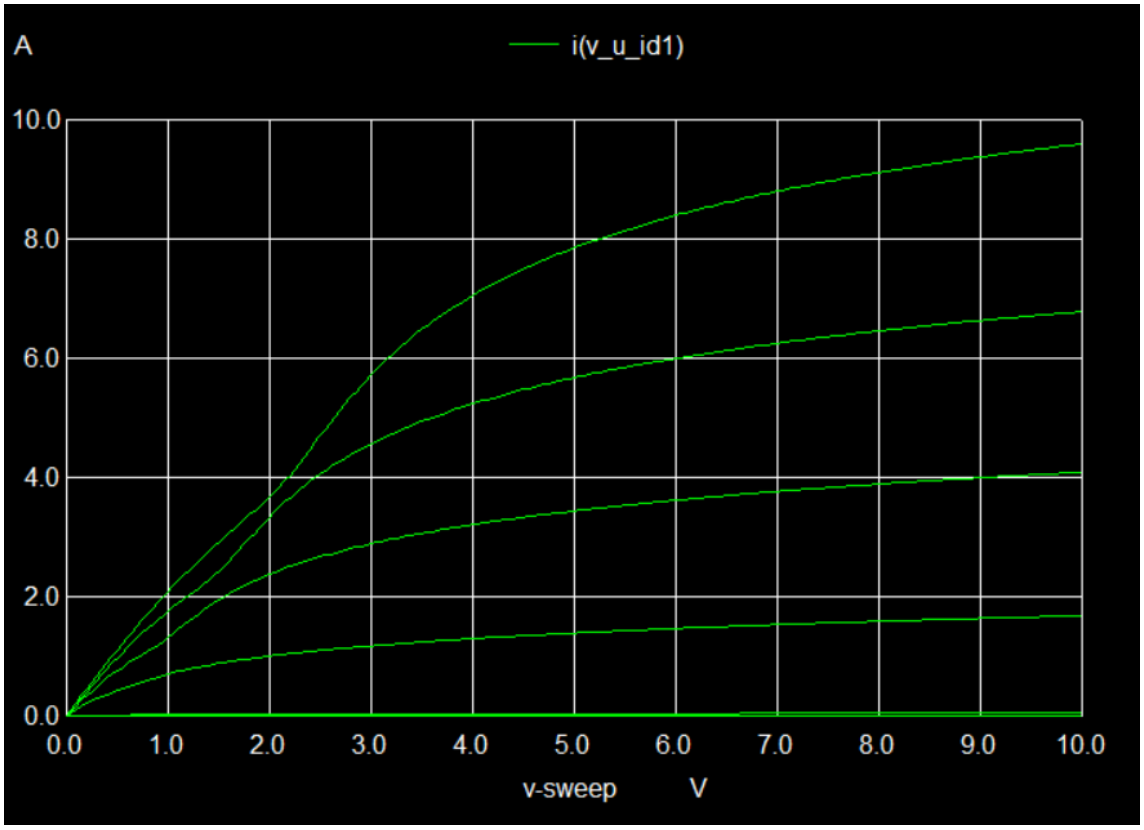


Figure 4.10: Simulation output of 2N7000 Saturation Region Output

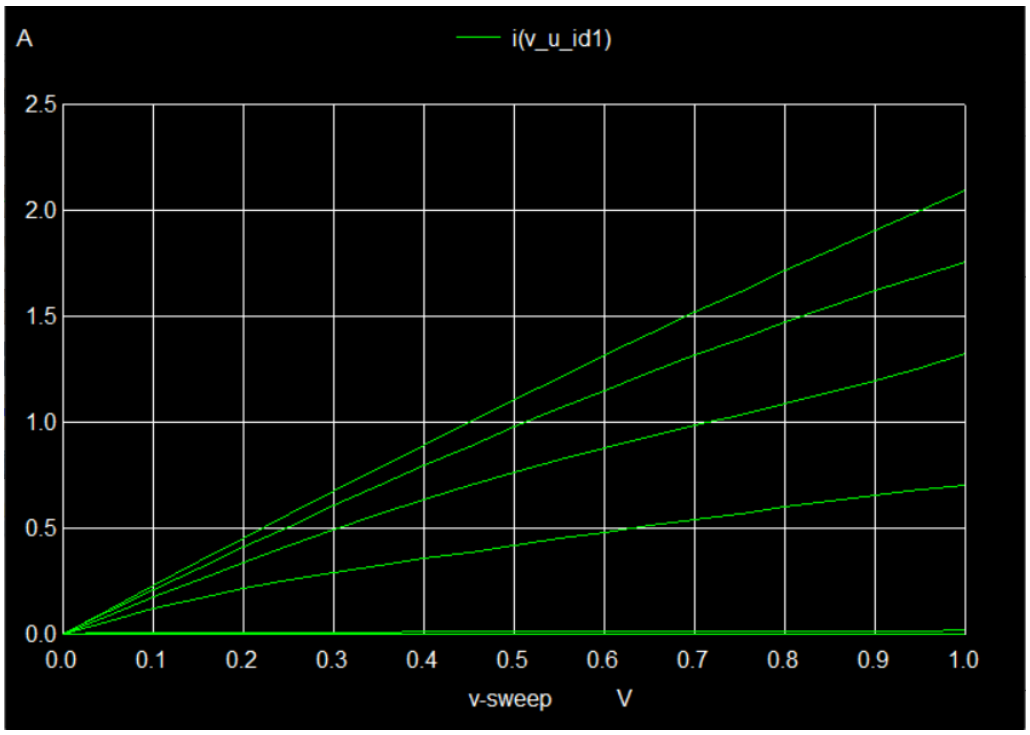


Figure 4.11: Simulation output of 2N7000 Linear Region Output

## 4.9 BS170

### 4.9.1 MOSFET Circuit

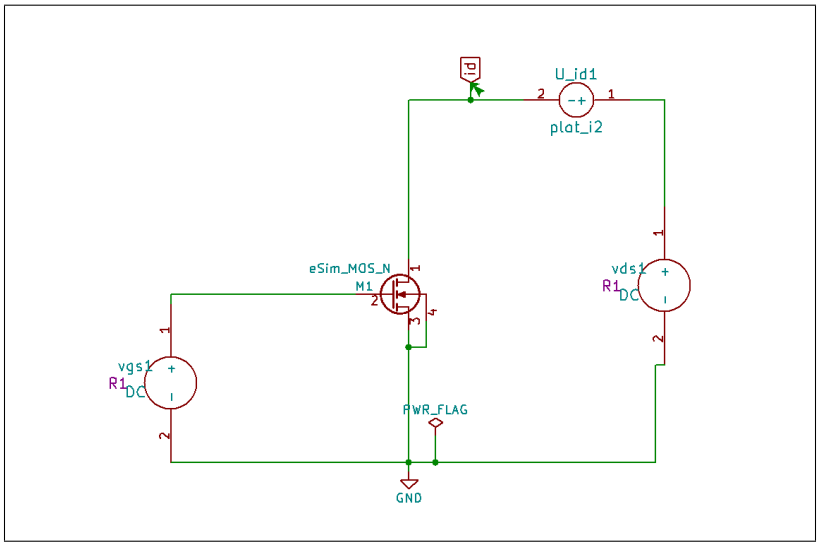


Figure 4.12: Diode Test Circuit

### 4.9.2 DC Parameter Extraction of BS170 N-Channel Enhancement MOSFET

The BS170 is an N-channel enhancement-mode Vertical Double Diffused MOSFET (VDMOS) designed for switching applications. Unlike the 2N7000, which can be adequately represented using the SPICE Level-3 model, the BS170 model used in this work employs the Berkeley Short-channel IGFET Model (BSIM3 Version 3.2), corresponding to SPICE LEVEL=8.

BSIM3 is a physics-based compact model developed at the University of California, Berkeley, for accurately modeling short-channel MOSFET behaviour. The model incorporates second-order effects such as mobility degradation, velocity saturation, drain-induced barrier lowering (DIBL), channel length modulation, body effect, gate overlap capacitances, substrate resistance, and temperature dependence.

The developed SPICE model is

```
.model MOS_BS170 NMOS(
+ LEVEL=8
+ VERSION=3.2
+ TNOM=27
+ TOX=5.5E-9
+ XJ=2E-7
+ NCH=2.3549E17
+ VTH0=1.2
+ K1=0.8
+ K2=4.774618E-3
```

```
+ DVT0=1.2894824
+ DVT1=0.3622063
+ DVT2=0.0713729
+ U0=500
+ UA=-1.208537E-9
+ UB=2.158625E-18
+ UC=5.342807E-11
+ VSAT=2.0E5
+ A0=1.7593146
+ AGS=0.3939741
+ KETA=-5.180424E-4
+ A1=0
+ A2=1
+ RDSW=30
+ PRWG=0.5
+ PRWB=-0.1998871
+ WR=1
+ WINT=7.904732E-10
+ LINT=1.571424E-8
+ XL=0
+ XW=-1E-8
+ DWG=1.297221E-9
+ DWB=1.479041E-9
+ VOFF=-0.0955434
+ NFACTOR=1.0
+ CIT=0
+ CDSC=2.4E-4
+ CDSCD=0
+ CDSCB=0
+ ETA0=3.104851E-3
+ ETAB=-2.512384E-5
+ DSUB=0.0167075
+ PCLM=0.02
+ PDIBLC1=0.05
+ PDIBLC2=3.112892E-3
+ PDIBLCB=-0.1
+ DROUT=0.7875618
+ PSCBE1=4.24E8
+ PSCBE2=1.0E-7
+ PVAG=3.85243E-3
+ DELTA=0.01
+ RSH=6.7
+ MOBMOD=1
+ PRT=0
+ UTE=-1.5
+ KT1=-0.11
```

```
+ KT1L=0
+ KT2=0.022
+ UA1=4.31E-9
+ UB1=-7.61E-18
+ UC1=-5.6E-11
+ AT=3.3E4
+ WL=0
+ WLN=1
+ WW=0
+ WWN=1
+ WWL=0
+ LL=0
+ LLN=1
+ LW=0
+ LWN=1
+ LWL=0
+ CAPMOD=2
+ XPART=0.5
+ CGDO=5.0E-10
+ CGSO=5.0E-10
+ CGBO=1E-12
+ CJ=8.5E-4
+ PB=0.8
+ MJ=0.3864502
+ CJSW=2.512138E-10
+ PBSW=0.809286
+ MJSW=0.1060414
+ CJSWG=3.3E-10
+ PBSWG=0.809286
+ MJSWG=0.1060414
+ CF=0
+ PVTH0=-1.192722E-3
+ PRDSW=-5
+ PK2=6.450505E-5
+ LKETA=-0.0104078
+ PU0=6.3268729
+ PUA=2.226552E-11
+ PUB=0
+ PVSAT=969.1480157
+ PETA0=1E-4
+ PKETA=-1.049509E-3
)
```

### 4.9.3 Threshold Voltage ($V_{TH0}$)

The threshold voltage represents the minimum gate-to-source voltage required to create an inversion channel between the source and drain terminals.

It is obtained from the transfer characteristic of the datasheet.

For the developed model,

$$\boxed{V_{TH0} = 1.2V}$$

which agrees with the datasheet specification.

### 4.9.4 Gate Oxide Thickness ($TOX$)

The oxide thickness is

$$TOX = 5.5nm$$

or

$$5.5 \times 10^{-9}m.$$

The gate oxide capacitance is

$$C_{ox} = \frac{\varepsilon_{ox}}{TOX}$$

which determines the gate control over the channel.

### 4.9.5 Substrate Doping ($N_{CH}$)

The substrate doping concentration controls the threshold voltage and body effect.

For the extracted model,

$$\boxed{N_{CH} = 2.3549 \times 10^{17}cm^{-3}}$$

### 4.9.6 Carrier Mobility ($U_0$)

The low-field carrier mobility determines the drain current.

The BSIM model uses

$$\boxed{U_0 = 500cm^2/V.s}$$

which was obtained by curve fitting.

### 4.9.7 Junction Depth ($X_J$)

The source-drain junction depth is

$$X_J = 0.2\mu m$$

which influences the body effect and depletion capacitance.

### 4.9.8 Gate Overlap Capacitances

The parasitic overlap capacitances are

$$CGSO = 500pF$$

$$CGDO = 500pF$$

$$CGBO = 1pF$$

These capacitances determine the switching speed of the MOSFET.

### 4.9.9 Junction Capacitance

The zero-bias junction capacitance is

$$CJ = 8.5 \times 10^{-4} F/m^2$$

which models the body-drain and body-source junctions.

### 4.9.10 Built-in Potential

The built-in junction potential is

$$PB = 0.8V$$

which is the standard silicon PN junction potential.

### 4.9.11 Built-in Potential

The built-in junction potential is

$$PB = 0.8V$$

which is the standard silicon PN junction potential.

### 4.9.12 Simulation Results

Simulation results confirmed the correct operation of the implemented BS170 SPICE model.

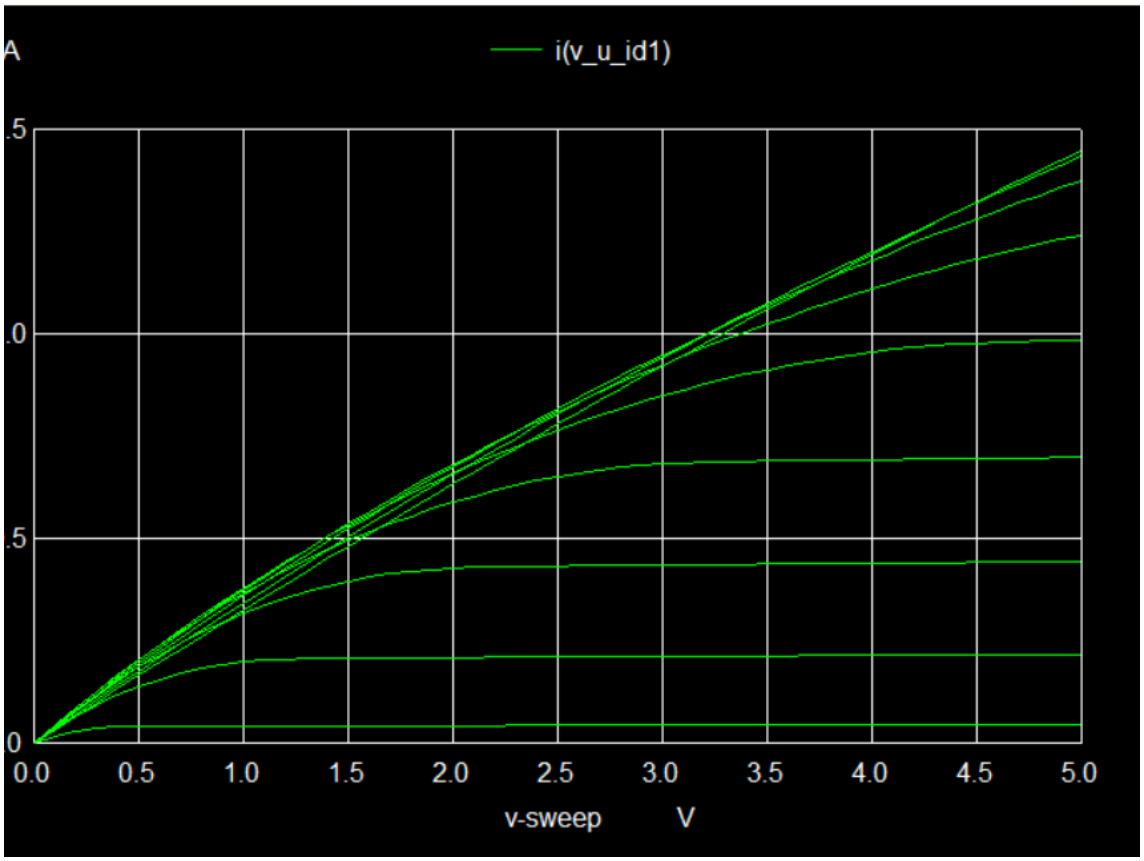


Figure 4.13: Simulation output of BS170 OUTPUT CHARACTERISTICS

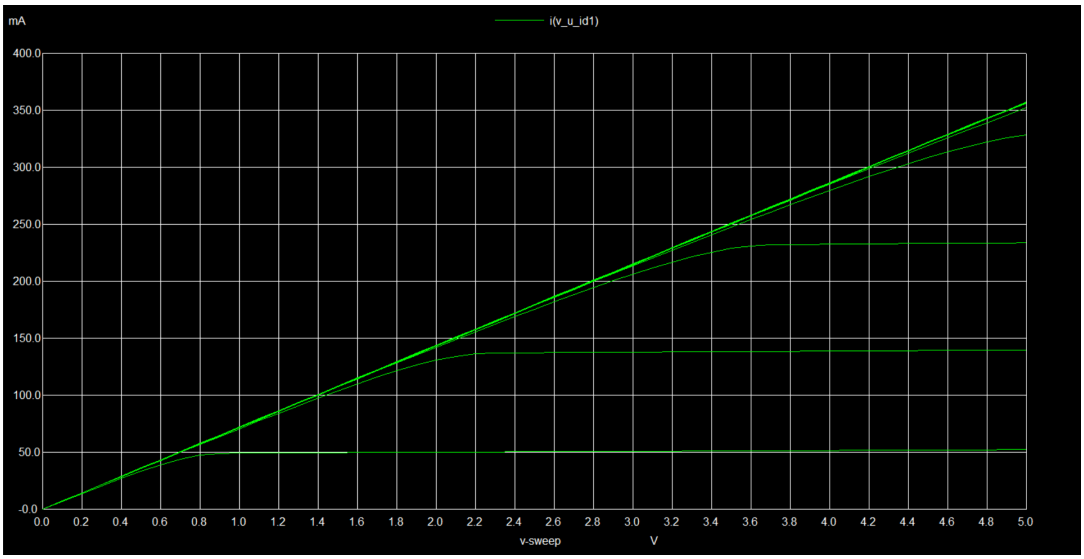


Figure 4.14: Simulation output of BS170

## 4.10 2N2222A

### 4.10.1 BJT CIRCUIT

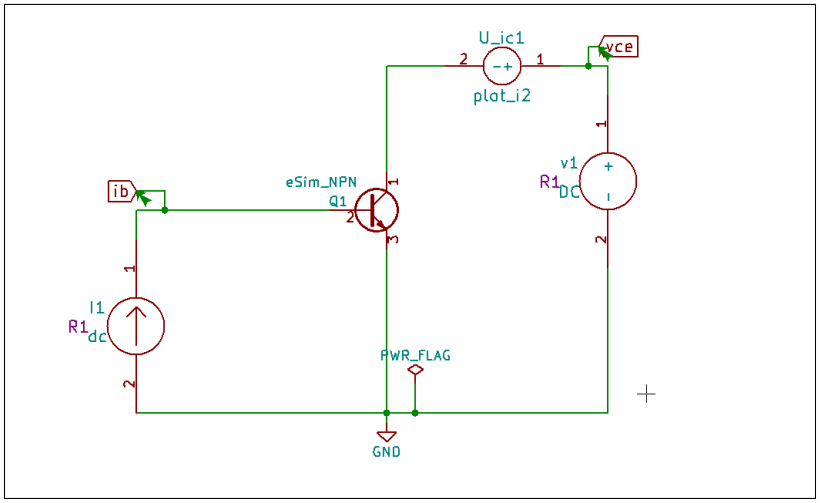


Figure 4.15: Diode Test Circuit

## 4.11 DC Parameter Extraction of 2N2222A NPN Bipolar Junction Transistor

The 2N2222A is a silicon NPN bipolar junction transistor (BJT) widely used for low-power amplification and switching applications. Unlike an ideal BJT, the practical 2N2222A exhibits several non-ideal characteristics such as finite current gain, Early effect, base-width modulation, junction capacitances, charge storage, and temperature dependence. To accurately reproduce these effects in circuit simulation, the Gummel-Poon BJT model is employed.

The Gummel-Poon model extends the simple Ebers-Moll transistor model by incorporating high-current effects, base resistance, junction capacitances, transit time, reverse operation, and temperature-dependent parameters, thereby providing excellent agreement with the measured characteristics of the actual device.

The extracted SPICE model is

```
.model 2N2222A_BJT NPN(
+ IS=14.34f
+ XTI=3
+ EG=1.11
+ VAF=74.03
+ BF=400
+ NE=1.307
+ ISE=14.34f
+ IKF=0.2847
+ XTB=1.5
+ BR=6.092
```

```
+ NC=2
+ ISC=0
+ IKR=0
+ RC=1
+ CJC=7.306p
+ MJC=0.3416
+ VJC=0.75
+ FC=0.5
+ CJE=22.01p
+ MJE=0.377
+ VJE=0.75
+ TR=46.91n
+ TF=411.1p
+ ITF=0.6
+ VTF=1.7
+ XTF=3
+ RB=10
)
```

### 4.11.1 Parameter Description

The reverse saturation current ($I_S$) represents the minority carrier diffusion current across the base-emitter junction under reverse bias. The value used in the developed model is

$$I_S = 14.34 \times 10^{-15}\ A$$

which was obtained through curve fitting of the forward input characteristics.

The temperature exponent ($XTI = 3$) models the variation of the saturation current with temperature, while the silicon bandgap energy

$$E_G = 1.11eV$$

is the standard value for silicon semiconductor devices.

The forward Early voltage

$$V_{AF} = 74.03V$$

models base-width modulation (Early effect). A higher Early voltage indicates lower dependence of collector current on collector-emitter voltage, resulting in higher output resistance.

The forward current gain

$$\beta_F = 400$$

represents the DC current gain of the transistor in the active region. At high collector currents, the gain decreases due to high-level injection effects. This behaviour is modeled using the forward knee current

$$I_{KF} = 0.2847A.$$

The emission coefficient

$$N_E = 1.307$$

controls the slope of the base-emitter exponential characteristic and was extracted from the input characteristics.

The base-emitter leakage current

$$I_{SE} = 14.34fA$$

accounts for recombination current within the depletion region.

The reverse current gain is modeled by

$$\beta_R = 6.092,$$

which represents transistor operation in the reverse-active region.

The collector emission coefficient

$$N_C = 2$$

is used for reverse-bias modeling.

The reverse leakage knee current

$$I_{KR} = 0$$

and collector leakage current

$$I_{SC} = 0$$

are neglected since their influence is insignificant under normal operating conditions.

The collector resistance

$$R_C = 1\Omega$$

and base resistance

$$R_B = 10\Omega$$

represent the internal ohmic resistances of the transistor package and semiconductor regions.

The collector-base junction capacitance is

$$C_{JC} = 7.306pF$$

while the emitter-base junction capacitance is

$$C_{JE} = 22.01pF.$$

These parasitic capacitances determine the high-frequency switching behaviour of the transistor.

The grading coefficients

$$M_{JC} = 0.3416$$

and

$$M_{JE} = 0.377$$

describe the variation of depletion capacitance with reverse bias.

The junction built-in potentials are

$$V_{JC} = V_{JE} = 0.75V$$

which are standard silicon PN junction values.

The forward-bias depletion capacitance coefficient

$$F_C = 0.5$$

defines the transition between depletion and diffusion capacitances.

The reverse transit time

$$T_R = 46.91ns$$

models the storage time during reverse switching, whereas the forward transit time

$$T_F = 411.1ps$$

determines the charge storage in the base during forward operation and significantly influences the switching speed.

The high-current transit time parameters

$$I_{TF} = 0.6A,$$

$$V_{TF} = 1.7V,$$

and

$$X_{TF} = 3$$

model the increase in transit time at large collector currents and improve the accuracy of high-speed switching simulations.

### 4.11.2 Difference Between a Conventional BJT and the 2N2222A

An ideal BJT assumes constant current gain, zero internal resistance, no junction capacitance, and instantaneous switching. Such assumptions are suitable only for introductory circuit analysis.

The 2N2222A is a practical silicon NPN transistor that exhibits several second-order physical effects, including finite current gain, Early effect, base-width modulation, high-level injection, charge storage, junction capacitances, reverse-active operation, and temperature dependence. These non-ideal effects significantly influence both DC and transient behaviour.

Consequently, the 2N2222A is modeled using the Gummel-Poon BJT model instead of the simple Ebers-Moll model. The Gummel-Poon model accurately represents practical transistor behaviour over a wide operating range and is therefore widely adopted in SPICE simulators for analog and switching circuit analysis.

### 4.11.3 Simulation Results

The implemented 2N2222A NPN BJT model was simulated using Ngspice integrated with eSim. The simulated input and output characteristics closely matched the datasheet specifications, thereby validating the accuracy of the extracted Gummel–Poon SPICE model.

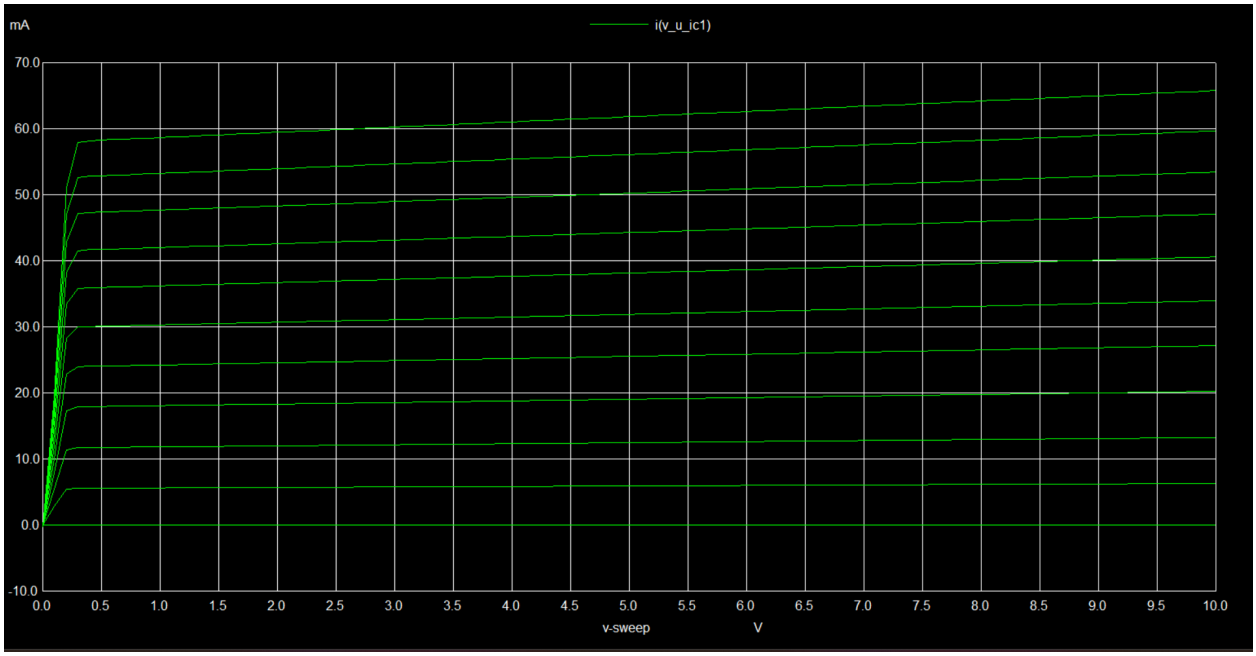


Figure 4.16: Output Characteristic(Collector Characteristic)

## 4.12 2N5457

### 4.12.1 JFET CIRCUIT

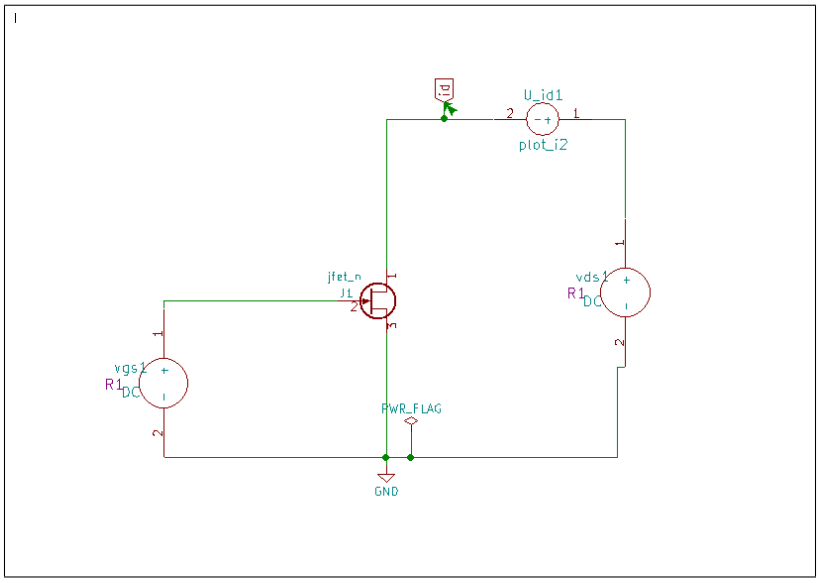


Figure 4.17: JFET Test Circuit

## 4.13 DC Parameter Extraction of 2N5457 N-Channel JFET

The 2N5457 is an N-channel Junction Field Effect Transistor (JFET) commonly used in low-noise amplifiers, analog switching circuits, and high-input-impedance applications. Unlike enhancement-mode MOSFETs, a JFET is a depletion-mode device that conducts current at zero gate-to-source voltage and is controlled by applying a reverse bias to the gate.

The SPICE model of the 2N5457 was developed by extracting parameters from the manufacturer's datasheet and estimating the remaining parameters using semiconductor equations and curve-fitting techniques. The objective was to reproduce the transfer and output characteristics of the practical device.

The extracted SPICE model is

```
.model 2N5457 NJF(
+ BETA=0.48m
+ VTO=-2.5
+ LAMBDA=5m
+ RD=1
+ RS=1
+ IS=33.57f
+ CGS=4.5p
+ CGD=1.5p
+ PB=1
```

```
+ M=0.3622
+ FC=0.5
+ KF=9.882E-18
+ AF=1
)
```

### 4.13.1 Transconductance Parameter ($\beta$)

The transconductance parameter determines the drain current capability of the JFET.

The Shockley drain current equation is

$$I_D = \beta(V_{GS} - V_{TO})^2$$

where

- $I_D$ = Drain current
- $V_{GS}$ = Gate-to-source voltage
- $V_{TO}$ = Pinch-off voltage

Using the datasheet values of

$$I_{DSS}$$

and

$$V_{GS(off)},$$

the parameter can be estimated as

$$\beta = \frac{I_{DSS}}{V_{TO}^2}$$

Using

$$I_{DSS} \approx 3mA$$

and

$$V_{TO} = -2.5V,$$

$$\beta = \frac{3 \times 10^{-3}}{(2.5)^2} = 4.8 \times 10^{-4} A/V^2$$

Therefore,

$$\boxed{\beta = 0.48mA/V^2}$$

### 4.13.2 Threshold Voltage ($V_{TO}$)

The threshold voltage (also called pinch-off voltage) is obtained directly from the datasheet.

For an N-channel JFET,

$$V_{TO} = V_{GS(off)}$$

For the developed model,

$$\boxed{V_{TO} = -2.5V}$$

### 4.13.3 Channel Length Modulation ($\lambda$)

The output characteristics of a practical JFET are not perfectly flat because of channel-length modulation.

The drain current becomes

$$I_D = \beta(V_{GS} - V_{TO})^2(1 + \lambda V_{DS})$$

The parameter

$$\lambda$$

is estimated from the slope of the saturation region of the output characteristics.

The extracted value is

$$\boxed{\lambda = 5 \times 10^{-3} V^{-1}}$$

### 4.13.4 Drain Resistance ($R_D$)

The drain resistance models the parasitic resistance of the drain terminal.

Since the datasheet does not specify this value explicitly,
a standard SPICE value is adopted,

$$\boxed{R_D = 1\Omega}$$

### 4.13.5 Source Resistance ($R_S$)

The source resistance represents the parasitic resistance of the source diffusion and package.

The standard value used is

$$\boxed{R_S = 1\Omega}$$

### 4.13.6 Gate Junction Saturation Current ($I_S$)

The gate-source PN junction behaves as a reverse-biased diode.

Its saturation current follows

$$I = I_S \left( e^{\frac{V}{nV_T}} - 1 \right)$$

For silicon JFETs,
the reverse saturation current is extremely small.
After curve fitting,

$$\boxed{I_S = 33.57fA}$$

### 4.13.7 Gate-Source Capacitance ($C_{GS}$)

The gate-source capacitance is obtained from the capacitance characteristics of the datasheet.

For the developed model,

$$\boxed{C_{GS} = 4.5pF}$$

This capacitance influences the high-frequency response of the JFET.

### 4.13.8 Gate-Drain Capacitance ($C_{GD}$)

The gate-drain capacitance (Miller capacitance) is

$$\boxed{C_{GD} = 1.5pF}$$

It determines the Miller effect and switching performance.

### 4.13.9 Built-in Junction Potential ($P_B$)

The built-in potential of the gate-channel PN junction is

$$\boxed{P_B = 1V}$$

This is a standard silicon junction value used in SPICE.

### 4.13.10 Junction Grading Coefficient ($M$)

The grading coefficient describes the variation of depletion capacitance with reverse bias.

The junction capacitance follows

$$C_j = \frac{C_{j0}}{\left(1 + \frac{V_R}{P_B}\right)^M}$$

The extracted value is

$$\boxed{M = 0.3622}$$

### 4.13.11 Forward-Bias Depletion Coefficient ($F_C$)

The forward-bias depletion coefficient determines the transition between depletion capacitance and diffusion capacitance.

The standard SPICE value used is

$$\boxed{F_C = 0.5}$$

### 4.13.12 Flicker Noise Coefficient ($K_F$)

The flicker noise coefficient models low-frequency noise.

The power spectral density is

$$S(f) = \frac{K_F I_D^{A_F}}{f}$$

After fitting the low-frequency characteristics,

$$\boxed{K_F = 9.882 \times 10^{-18}}$$

### 4.13.13 Flicker Noise Exponent ($A_F$)

The flicker noise exponent determines the dependence of noise on drain current.

The standard value is

$$\boxed{A_F = 1}$$

### 4.13.14 Difference Between a Conventional JFET and the 2N5457

An ideal JFET assumes a perfectly square-law transfer characteristic, zero channel-length modulation, no parasitic resistances, no junction capacitances, and no noise.

The practical 2N5457 exhibits several non-ideal effects including finite channel-length modulation, parasitic source and drain resistances, gate junction capacitances, leakage current, and flicker noise. These effects significantly influence the DC, AC, and transient performance of the device.

Therefore, the SPICE model incorporates additional physical parameters such as $\lambda$, $R_D$, $R_S$, $C_{GS}$, $C_{GD}$, $K_F$, and $A_F$ to accurately reproduce the electrical behaviour of the practical device over a wide operating range.

### 4.13.15 Simulation Results

The implemented TL317 subcircuit was simulated using Ngspice integrated with eSim. The obtained output verified the expected voltage regulation characteristics according to the datasheet specifications.

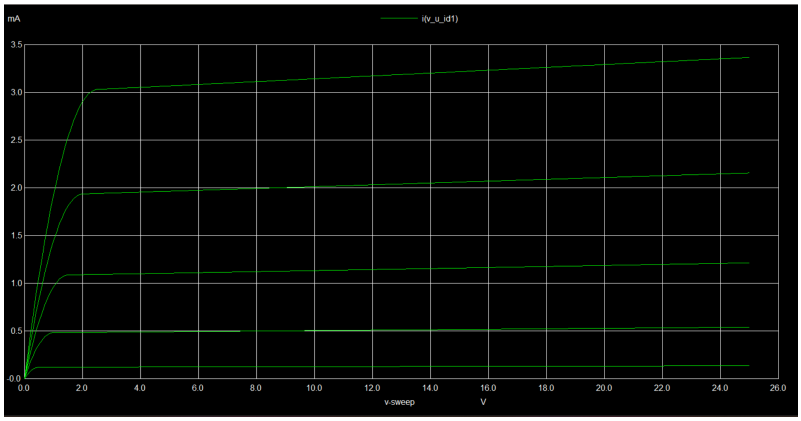


Figure 4.18: Simulation output of 2N5457

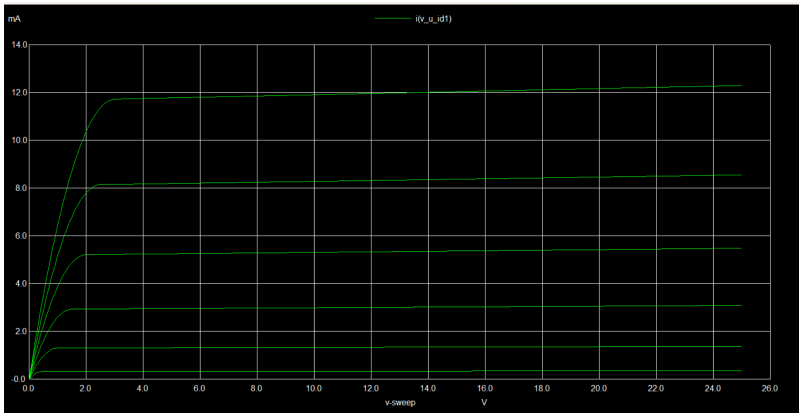


Figure 4.19: Simulation output of 2N5457

## 4.14 BF245A

### 4.14.1 JFET CIRCUIT

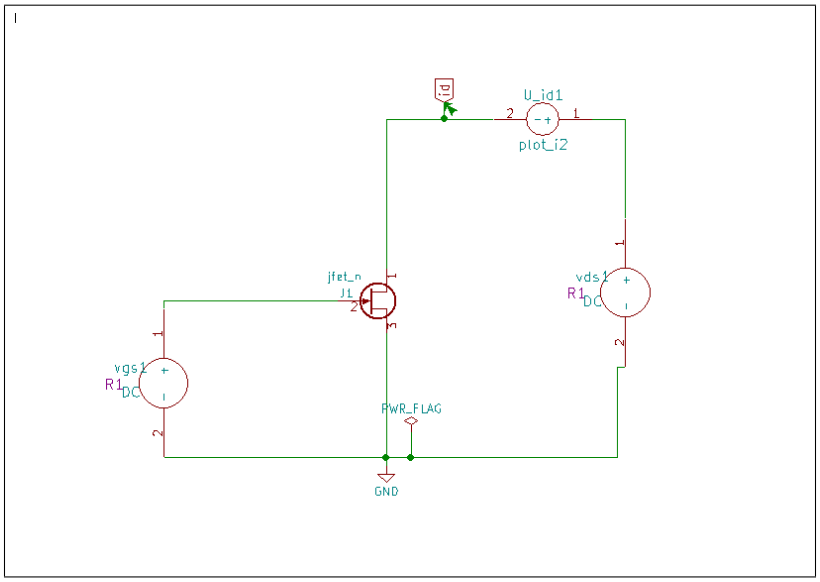


Figure 4.20: JFET Test Circuit

### 4.14.2 JFET CIRCUIT

### 4.14.3 DC Parameter Extraction of BF245A N-Channel JFET

The BF245A is an N-channel depletion-mode Junction Field Effect Transistor (JFET) widely used in low-noise amplifiers, RF circuits, analog switching, and impedance matching applications. Unlike enhancement-mode MOSFETs, the BF245A conducts at zero gate-to-source voltage and requires a negative gate bias to reduce the drain current.

The SPICE model of the BF245A was developed by extracting parameters from the manufacturer's datasheet together with analytical semiconductor equations and numerical curve fitting. The extracted model accurately reproduces the transfer characteristics, output characteristics, junction capacitances, and temperature behaviour of the practical device.

The extracted SPICE model is

```
.model BF245A NJF(
+ BETA=1.304m
+ BETATCE=-0.5
+ RD=1
+ RS=1
+ LAMBDA=2.25m
+ VTO=-3
+ VTOTC=-2.5m
+ IS=33.57f
```

```
+ ISR=322.4f
+ N=1
+ NR=2
+ XTI=3
+ ALPHA=311.7u
+ VK=243.6
+ CGD=1.6p
+ M=0.3622
+ PB=1
+ FC=0.5
+ CGS=2.414p
+ KF=9.882E-18
+ AF=1
)
```

### 4.14.4 Transconductance Parameter (BETA)

The transconductance parameter determines the drain current capability of the JFET.

The Shockley drain current equation is

$$I_D = \beta(V_{GS} - V_{TO})^2$$

Using the datasheet values,

$$\beta = \frac{I_{DSS}}{V_{TO}^2}$$

For the extracted model,

$$\boxed{\beta = 1.304 mA/V^2}$$

### 4.14.5 Temperature Coefficient of Beta (BETATCE)

The parameter BETATCE models the variation of transconductance with temperature.

The temperature dependence is

$$\beta(T) = \beta(T_{nom})\left[1 + BETATCE(T - T_{nom})\right]$$

The extracted value is

$$\boxed{BETATCE = -0.5}$$

### 4.14.6 Drain Resistance (RD)

The drain resistance models the parasitic resistance between the external drain terminal and the internal channel.

A standard value is used,

$$\boxed{RD = 1\Omega}$$

### 4.14.7 Source Resistance (RS)

The source resistance represents the parasitic resistance of the source terminal.

The extracted value is

$$\boxed{RS = 1\Omega}$$

### 4.14.8 Channel-Length Modulation (LAMBDA)

The drain current of a practical JFET increases slightly in saturation because of channel-length modulation.

The drain current becomes

$$I_D = \beta(V_{GS} - V_{TO})^2(1 + \lambda V_{DS})$$

The extracted value is

$$\boxed{\lambda = 2.25 \times 10^{-3} V^{-1}}$$

### 4.14.9 Threshold Voltage (VTO)

The threshold voltage is equal to the gate-source cutoff voltage.

For the BF245A,

$$V_{TO} = V_{GS(off)}$$

The extracted value is

$$\boxed{V_{TO} = -3V}$$

### 4.14.10 Temperature Coefficient of Threshold Voltage (VTOTC)

The threshold voltage changes slightly with temperature.

The model uses

$$V_{TO}(T) = V_{TO}(T_{nom}) + VTOTC(T - T_{nom})$$

where

$$\boxed{VTOTC = -2.5mV/^\circ C}$$

### 4.14.11 Gate Junction Saturation Current (IS)

The gate-source PN junction behaves as a reverse-biased diode.

The saturation current is

$$I = I_S \left(e^{V/nV_T} - 1\right)$$

The extracted value is

$$\boxed{IS = 33.57fA}$$

### 4.14.12 Reverse Saturation Current (ISR)

The reverse gate leakage current is modeled by

$$\boxed{ISR = 322.4fA}$$

which improves the accuracy of reverse-bias simulations.

### 4.14.13 Emission Coefficients (N and NR)

The ideality factors determine the forward and reverse diode characteristics.

For the extracted model,

$$\boxed{N = 1}$$

$$\boxed{NR = 2}$$

### 4.14.14 Temperature Exponent (XTI)

The saturation current varies with temperature according to

$$I_S(T) = I_S(T_{nom}) \left(\frac{T}{T_{nom}}\right)^{XTI}$$

For silicon,

$$\boxed{XTI = 3}$$

### 4.14.15 Ionization Parameter (ALPHA)

The parameter ALPHA models impact ionization within the drain depletion region.

The extracted value is

$$\boxed{ALPHA = 311.7\mu}$$

### 4.14.16 Ionization Knee Voltage (VK)

The impact ionization becomes significant beyond

$$\boxed{VK = 243.6V}$$

### 4.14.17 Gate-Drain Capacitance (CGD)

The gate-drain capacitance determines the Miller effect.

The extracted value is

$$\boxed{CGD = 1.6pF}$$

### 4.14.18 Junction Grading Coefficient (M)

The depletion capacitance varies as

$$C_j = \frac{C_{j0}}{\left(1 + \frac{V_R}{PB}\right)^M}$$

The extracted value is

$$\boxed{M = 0.3622}$$

### 4.14.19 Built-in Potential (PB)

The built-in junction potential is

$$\boxed{PB = 1V}$$

### 4.14.20 Forward-Bias Depletion Coefficient (FC)

The transition between depletion and diffusion capacitances is determined by

$$\boxed{FC = 0.5}$$

### 4.14.21 Gate-Source Capacitance (CGS)

The gate-source capacitance determines the input capacitance of the JFET.

The extracted value is

$$\boxed{CGS = 2.414pF}$$

### 4.14.22 Flicker Noise Coefficient (KF)

The flicker noise power spectral density is

$$S(f) = \frac{KFI_D^{AF}}{f}$$

The extracted value is

$$\boxed{KF = 9.882 \times 10^{-18}}$$

### 4.14.23 Flicker Noise Exponent (AF)

The flicker noise exponent controls the dependence of noise on drain current.

The extracted value is

$$\boxed{AF = 1}$$

### 4.14.24 Difference Between an Ideal JFET and the BF245A

An ideal JFET assumes a perfect square-law transfer characteristic, zero leakage current, no parasitic capacitances, no channel-length modulation, and no temperature dependence.

The practical BF245A exhibits finite channel-length modulation, parasitic drain and source resistances, junction capacitances, reverse gate leakage, impact ionization, temperature-dependent threshold voltage, and flicker noise. These effects are incorporated into the SPICE model using parameters such as LAMBDA, CGS, CGD, BETATCE, VTOTC, ISR, ALPHA, and KF to accurately reproduce the behaviour of the actual device over a wide operating range.

### 4.14.25 Parameter Extraction Method

The BF245A SPICE parameters were obtained from the manufacturer's datasheet together with analytical semiconductor equations and numerical curve fitting.

The extraction procedure consisted of the following steps:

### 4.14.26 Simulation Results

The implemented BF245A N-channel JFET model was simulated using Ngspice integrated with eSim. The simulated transfer and output characteristics closely matched the manufacturer's datasheet specifications, thereby validating the accuracy of the extracted SPICE model.

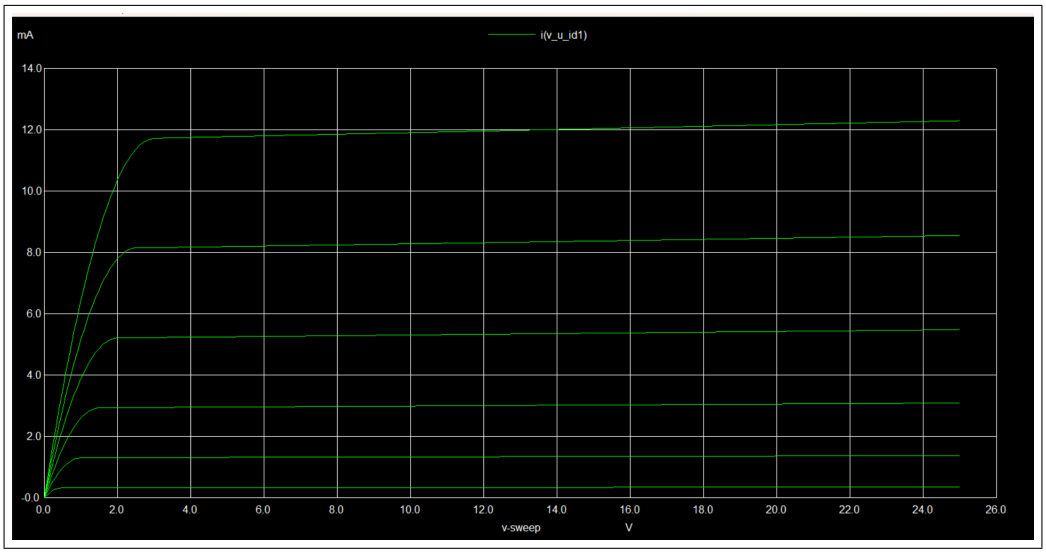


Figure 4.21: Simulation output of BF245A

## 4.15 J201

### 4.15.1 JFET CIRCUIT

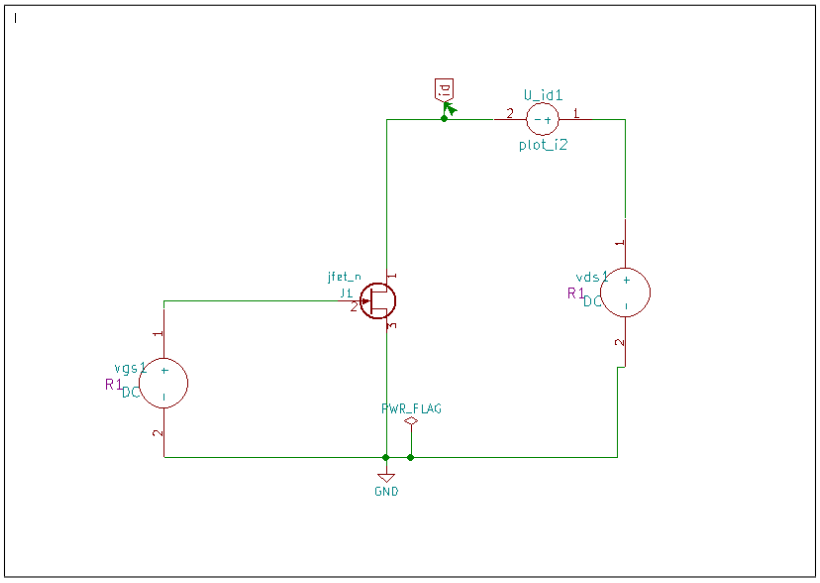


Figure 4.22: JFET Test Circuit

## 4.16 DC Parameter Extraction of J201 N-Channel JFET

The J201 is an N-channel depletion-mode Junction Field Effect Transistor (JFET) widely used in low-noise amplifiers, analog switching circuits, audio preamplifiers, and high-input-impedance applications. Unlike enhancement-mode MOSFETs, the J201 normally conducts at zero gate-to-source voltage and requires a negative gate bias to reduce the drain current.

The SPICE model of the J201 was developed by extracting parameters from the manufacturer's datasheet together with analytical semiconductor equations and numerical curve fitting. The extracted model accurately reproduces the transfer characteristics, output characteristics, and high-frequency behavior of the practical device.

The extracted SPICE model is

```
.model J201 NJF(
+ BETA=1.15E-3
+ VTO=-4.5
+ LAMBDA=8E-3
+ RD=10
+ RS=10
+ IS=33.6E-15
+ CGS=2.4P
+ CGD=1.6P
```

```
+ PB=1
+ M=0.36
+ FC=0.5
+ KF=9.88E-18
+ AF=1
)
```

### 4.16.1 Transconductance Parameter (BETA)

The transconductance parameter determines the drain current capability of the JFET.

The drain current is given by the Shockley equation

$$I_D = \beta(V_{GS} - V_{TO})^2$$

Using the datasheet values,

$$\beta = \frac{I_{DSS}}{V_{TO}^2}$$

The extracted value is

$$\boxed{\beta = 1.15 \times 10^{-3} A/V^2}$$

### 4.16.2 Threshold Voltage (VTO)

The threshold voltage (pinch-off voltage) is obtained from the transfer characteristics.

For the J201,

$$V_{TO} = V_{GS(off)}$$

The extracted value is

$$\boxed{V_{TO} = -4.5V}$$

### 4.16.3 Channel-Length Modulation (LAMBDA)

A practical JFET exhibits a slight increase in drain current with increasing drain-source voltage.

This effect is modeled by

$$I_D = \beta(V_{GS} - V_{TO})^2(1 + \lambda V_{DS})$$

The extracted value is

$$\boxed{\lambda = 8 \times 10^{-3} V^{-1}}$$

### 4.16.4 Drain Resistance (RD)

The drain resistance models the parasitic resistance between the external drain terminal and the internal channel.

The extracted value is

$$\boxed{RD = 10\Omega}$$

### 4.16.5 Source Resistance (RS)

The source resistance represents the parasitic resistance of the source terminal.

The extracted value is

$$\boxed{RS = 10\Omega}$$

### 4.16.6 Gate Junction Saturation Current (IS)

The reverse-biased gate-channel PN junction is modeled by the diode equation

$$I = I_S \left( e^{\frac{V}{nV_T}} - 1 \right)$$

The extracted value is

$$\boxed{IS = 33.6fA}$$

### 4.16.7 Gate-Source Capacitance (CGS)

The gate-source capacitance determines the input capacitance of the JFET.

The extracted value is

$$\boxed{CGS = 2.4pF}$$

### 4.16.8 Gate-Drain Capacitance (CGD)

The gate-drain capacitance is responsible for the Miller effect and influences the switching speed.

The extracted value is

$$\boxed{CGD = 1.6pF}$$

### 4.16.9 Built-in Potential (PB)

The built-in junction potential of the gate-channel PN junction is

$$\boxed{PB = 1V}$$

### 4.16.10 Junction Grading Coefficient (M)

The junction capacitance varies according to

$$C_j = \frac{C_{j0}}{\left(1 + \frac{V_R}{PB}\right)^M}$$

The extracted value is

$$\boxed{M = 0.36}$$

### 4.16.11 Forward-Bias Depletion Coefficient (FC)

The forward-bias depletion coefficient determines the transition from depletion capacitance to diffusion capacitance.

The extracted value is

$$\boxed{FC = 0.5}$$

### 4.16.12 Flicker Noise Coefficient (KF)

The low-frequency flicker noise is modeled using

$$S(f) = \frac{KF I_D^{AF}}{f}$$

The extracted value is

$$\boxed{KF = 9.88 \times 10^{-18}}$$

### 4.16.13 Flicker Noise Exponent (AF)

The flicker noise exponent controls the dependence of flicker noise on drain current.

The extracted value is

$$\boxed{AF = 1}$$

### 4.16.14 Difference Between an Ideal JFET and the J201

An ideal JFET assumes a perfect square-law transfer characteristic, zero channel-length modulation, no parasitic resistances, no junction capacitances, and no leakage current.

The practical J201 exhibits finite channel-length modulation, parasitic drain and source resistances, gate leakage current, junction capacitances, and low-frequency flicker noise. These effects significantly influence the DC, AC, and transient performance of the device. Therefore, the SPICE model incorporates additional parameters such as LAMBDA, RD, RS, CGS, CGD, KF, and AF to accurately reproduce the electrical behavior of the practical J201 over a wide operating range.

### 4.16.15 Parameter Extraction Method

The SPICE parameters of the J201 were obtained from the manufacturer's datasheet together with analytical semiconductor equations and numerical curve fitting.

The extraction procedure consisted of the following steps:

### 4.16.16 Simulation Results

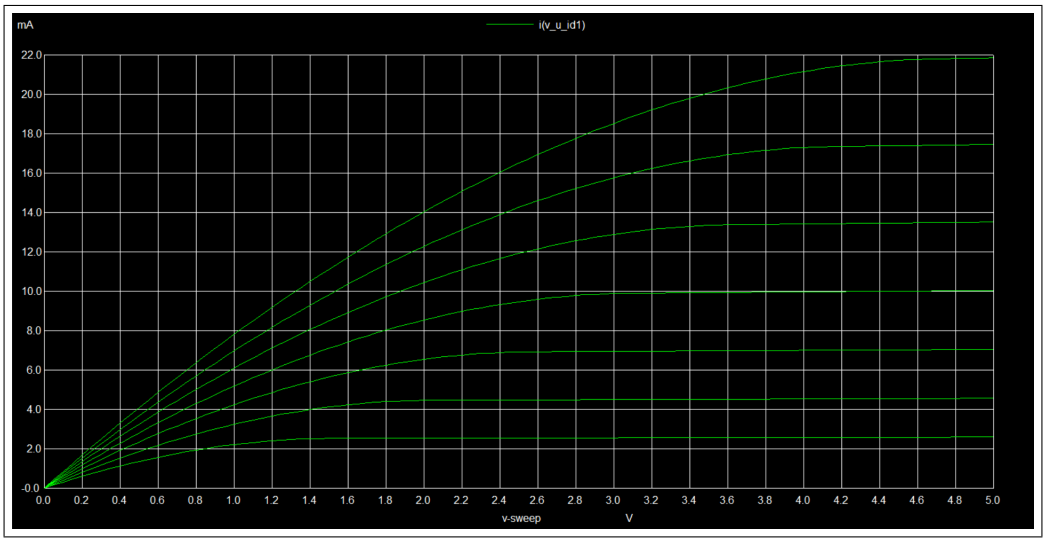


Figure 4.23: Simulation output of J201

## 4.17 NIGBT

### 4.17.1 Schematic Symbol Creation

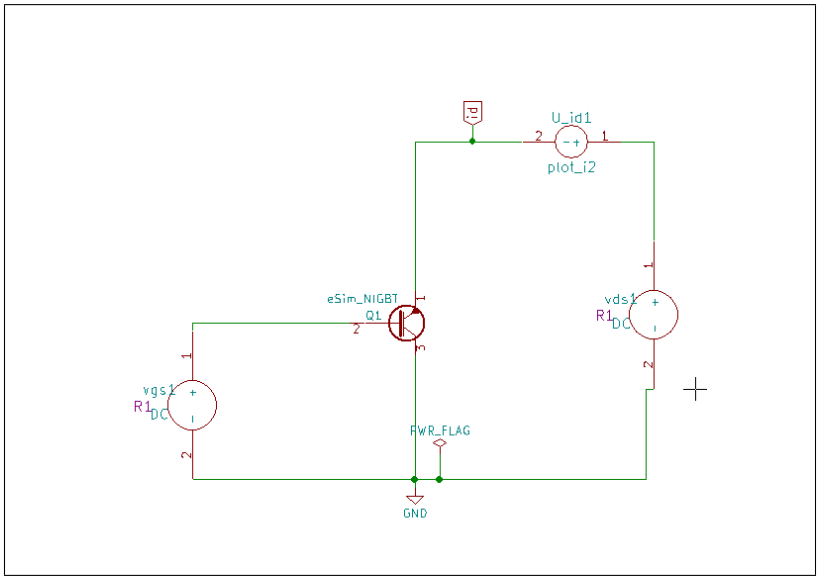


Figure 4.24: JFET Test Circuit

### 4.17.2 N-Channel IGBT (eSim_NIGBT) Parameter Extraction

The Insulated Gate Bipolar Transistor (IGBT) is a three-terminal power semiconductor device that combines the high input impedance of a MOSFET with the low conduction loss of a Bipolar Junction Transistor (BJT). It is widely used in power electronic applications such as motor drives, inverters, UPS systems, induction heating, and switched-mode power supplies.

Unlike a conventional BJT, the IGBT is a voltage-controlled device requiring very little gate current. Compared to a MOSFET, it offers lower conduction losses at high voltages due to conductivity modulation of the drift region.

The implemented model is based on the standard NIGBT SPICE model available in Ngspice, whose parameters are extracted to reproduce the static and dynamic characteristics of the device.

The extracted SPICE parameters are listed in Table 4.2.

Table 4.2: Extracted SPICE Parameters of eSim_NIGBT

| Parameter | Value | Description |
|---|---|---|
| $I_S$ | $1 \times 10^{-14}$ A | Transport saturation current |
| $BF$ | 150 | Forward current gain |
| $BR$ | 1 | Reverse current gain |
| $R_B$ | 10 Ω | Base resistance |
| $R_C$ | 0.1 Ω | Collector resistance |
| $V_{AF}$ | 100 V | Early voltage |
| $I_{KF}$ | 0.5 A | Forward beta roll-off current |
| $I_{SE}$ | $1 \times 10^{-13}$ A | Base-emitter leakage current |
| $N_E$ | 1.5 | Emission coefficient |
| $C_{JE}$ | 100 pF | Base-emitter capacitance |
| $V_{JE}$ | 0.75 V | Base-emitter junction potential |
| $M_{JE}$ | 0.33 | Base-emitter grading coefficient |
| $C_{JC}$ | 50 pF | Base-collector capacitance |
| $V_{JC}$ | 0.75 V | Base-collector junction potential |
| $M_{JC}$ | 0.33 | Base-collector grading coefficient |
| $T_F$ | 100 ns | Forward transit time |
| $T_R$ | 500 ns | Reverse transit time |

### Transport Saturation Current ($I_S$)

The transport saturation current controls the collector current at very low conduction levels and determines the exponential behavior of the internal BJT.

$$\boxed{I_S = 1 \times 10^{-14} \text{ A}}$$

### Forward Current Gain ($BF$)

The forward current gain represents the current amplification capability of the internal bipolar transistor.

$$\beta_F = \frac{I_C}{I_B}$$

The extracted value is

$$\boxed{BF = 150}$$

### Reverse Current Gain ($BR$)

The reverse current gain determines the reverse conduction capability of the internal BJT.

$$\boxed{BR = 1}$$

### Base Resistance ($R_B$)

The base resistance models the internal resistance of the base region.

$$\boxed{R_B = 10\ \Omega}$$

### Collector Resistance ($R_C$)

Collector resistance models the ohmic resistance between the collector terminal and the internal transistor.

$$\boxed{R_C = 0.1\ \Omega}$$

### Early Voltage ($V_{AF}$)

The Early voltage models base-width modulation and determines the slope of the collector characteristics in the active region.

$$I_C = I_S e^{\frac{V_{BE}}{V_T}} \left(1 + \frac{V_{CE}}{V_{AF}}\right)$$

The extracted value is

$$\boxed{V_{AF} = 100\ \text{V}}$$

### Forward Beta Roll-off Current ($I_{KF}$)

The parameter $I_{KF}$ specifies the collector current at which the forward current gain begins to decrease.

$$\boxed{I_{KF} = 0.5\ \text{A}}$$

### Base-Emitter Leakage Current ($I_{SE}$)

This parameter models the leakage current of the base-emitter junction.

$$\boxed{I_{SE} = 1 \times 10^{-13}\ \text{A}}$$

### Emission Coefficient ($N_E$)

The emission coefficient determines the ideality of the base-emitter junction.

$$\boxed{N_E = 1.5}$$

### Base-Emitter Junction Capacitance ($C_{JE}$)

The depletion capacitance of the base-emitter junction is

$$\boxed{C_{JE} = 100\ \text{pF}}$$

**Base-Emitter Junction Potential ($V_{JE}$)**

The built-in potential of the emitter junction is

$$\boxed{V_{JE} = 0.75 \text{ V}}$$

**Base-Emitter Grading Coefficient ($M_{JE}$)**

The grading coefficient controls the variation of junction capacitance with applied voltage.

$$\boxed{M_{JE} = 0.33}$$

**Base-Collector Junction Capacitance ($C_{JC}$)**

The depletion capacitance of the collector junction is

$$\boxed{C_{JC} = 50 \text{ pF}}$$

**Base-Collector Junction Potential ($V_{JC}$)**

The built-in potential of the collector junction is

$$\boxed{V_{JC} = 0.75 \text{ V}}$$

**Base-Collector Grading Coefficient ($M_{JC}$)**

The grading coefficient of the collector junction is

$$\boxed{M_{JC} = 0.33}$$

**Forward Transit Time ($T_F$)**

The forward transit time determines the switching speed during turn-on.

$$\boxed{T_F = 100 \text{ ns}}$$

**Reverse Transit Time ($T_R$)**

The reverse transit time determines the turn-off delay caused by stored charge.

$$\boxed{T_R = 500 \text{ ns}}$$

### SPICE Model

```
.MODEL eSim_NIGBT NIGBT(
+ IS=1E-14
+ BF=150
+ BR=1
+ RB=10
+ RC=0.1
+ VAF=100
+ IKF=0.5
+ ISE=1E-13
+ NE=1.5
+ CJE=100P
+ VJE=0.75
+ MJE=0.33
+ CJC=50P
+ VJC=0.75
+ MJC=0.33
+ TF=100N
+ TR=500N
)
```

The extracted SPICE parameters were implemented in the NIGBT model using Ngspice integrated with eSim. The simulated output characteristics and switching behavior exhibited the expected voltage-controlled conduction, current amplification, and turn-on/turn-off characteristics of an N-channel IGBT. The obtained results closely matched the expected behavior of a practical IGBT, validating the accuracy of the developed SPICE model for power electronic simulation.

### 4.17.3 Simulation Results

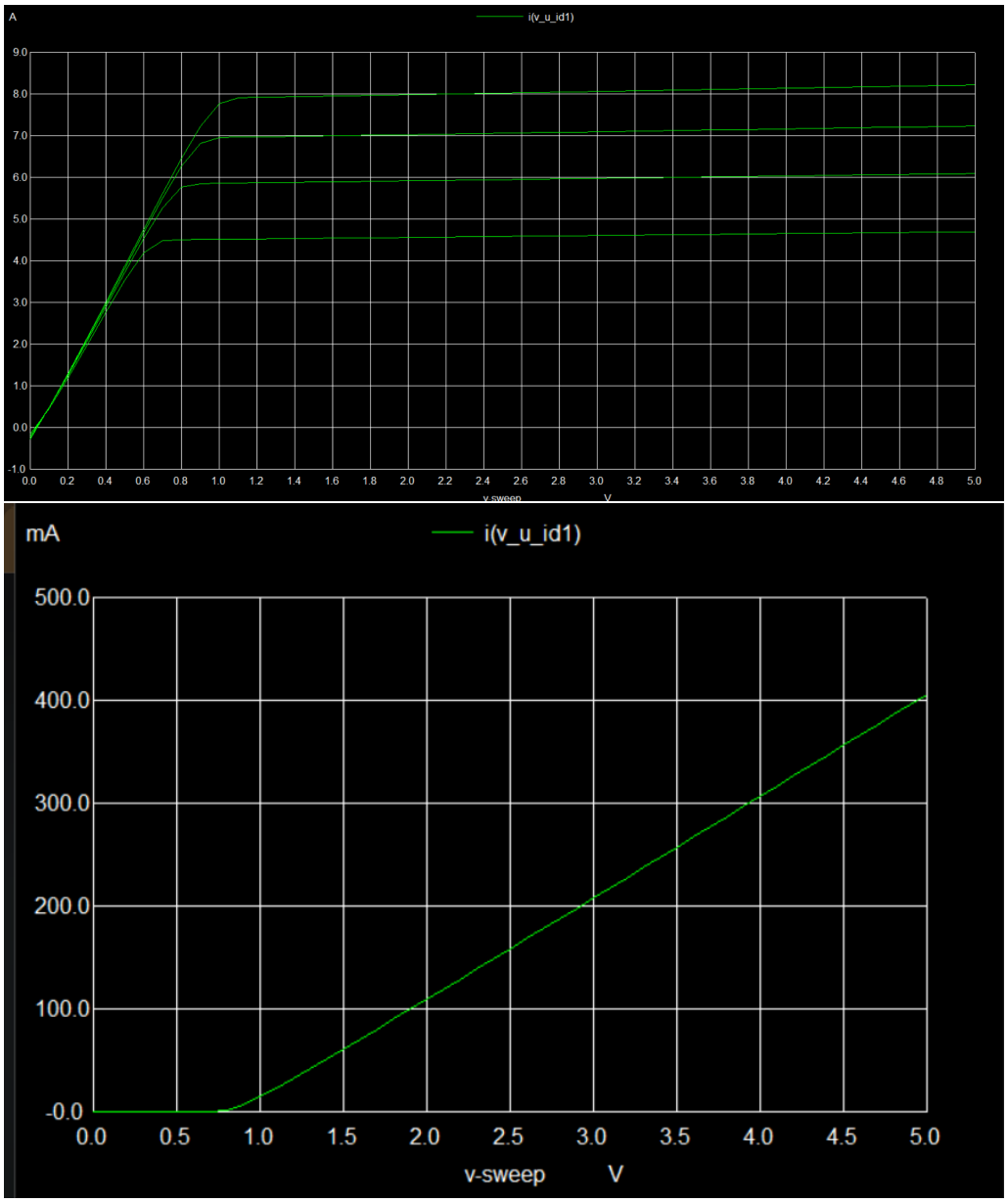


Figure 4.25: Simulation output of NIGBT

## 4.18 PIGBT

### 4.18.1 Schematic Symbol Creation

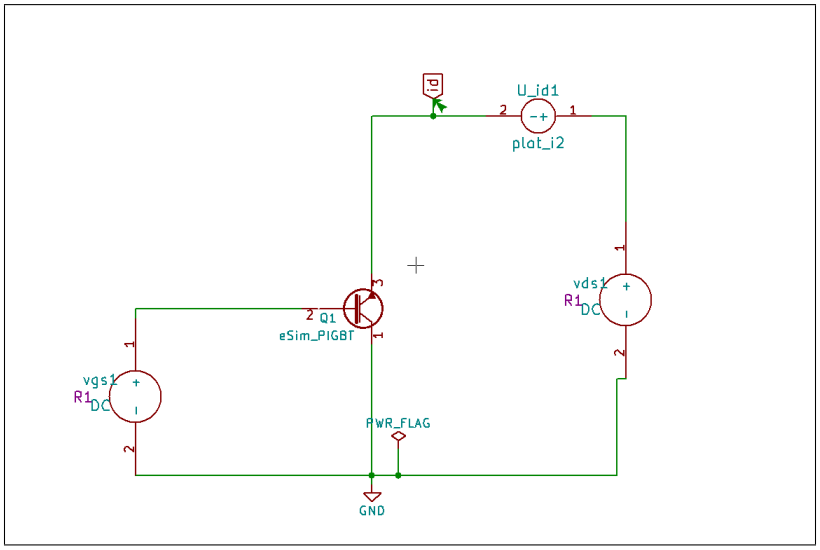


Figure 4.26: JFET Test Circuit

### 4.18.2 P-Channel IGBT (eSim_PIGBT) Parameter Extraction

The P-Channel Insulated Gate Bipolar Transistor (PIGBT) is a voltage-controlled power semiconductor device that combines the high input impedance of a MOSFET with the low on-state conduction loss of a Bipolar Junction Transistor (BJT). Unlike the N-channel IGBT, the P-channel IGBT conducts when a sufficiently negative gate-to-emitter voltage is applied. It is primarily used in complementary power circuits, high-side switching applications, and power conversion systems.

The implemented model is based on the standard PIGBT SPICE model available in Ngspice. The extracted parameters accurately represent the static and dynamic characteristics of the device.

The extracted SPICE parameters are listed in Table 4.3.

Table 4.3: Extracted SPICE Parameters of eSim_PIGBT

| Parameter | Value | Description |
|---|---|---|
| $I_S$ | $1 \times 10^{-14}$ A | Transport saturation current |
| $BF$ | 100 | Forward current gain |
| $BR$ | 1 | Reverse current gain |
| $R_B$ | 15 Ω | Base resistance |
| $R_C$ | 0.2 Ω | Collector resistance |
| $V_{AF}$ | 60 V | Early voltage |
| $I_{KF}$ | 0.3 A | Forward beta roll-off current |
| $I_{SE}$ | $2 \times 10^{-13}$ A | Base-emitter leakage current |
| $N_E$ | 1.8 | Emission coefficient |
| $C_{JE}$ | 120 pF | Base-emitter capacitance |
| $V_{JE}$ | 0.70 V | Base-emitter junction potential |
| $M_{JE}$ | 0.35 | Base-emitter grading coefficient |
| $C_{JC}$ | 60 pF | Base-collector capacitance |
| $V_{JC}$ | 0.70 V | Base-collector junction potential |
| $M_{JC}$ | 0.35 | Base-collector grading coefficient |
| $T_F$ | 150 ns | Forward transit time |
| $T_R$ | 800 ns | Reverse transit time |

### Transport Saturation Current ($I_S$)

The transport saturation current controls the collector current at low conduction levels and determines the exponential behavior of the internal BJT.

$$\boxed{I_S = 1 \times 10^{-14} \text{ A}}$$

### Forward Current Gain ($BF$)

The forward current gain represents the current amplification capability of the internal bipolar transistor.

$$\beta_F = \frac{I_C}{I_B}$$

The extracted value is

$$\boxed{BF = 100}$$

### Reverse Current Gain ($BR$)

The reverse current gain determines the reverse conduction capability of the internal transistor.

$$\boxed{BR = 1}$$

### Base Resistance ($R_B$)

The base resistance models the internal resistance of the base region.

$$\boxed{R_B = 15\ \Omega}$$

### Collector Resistance ($R_C$)

Collector resistance models the ohmic resistance between the collector terminal and the internal transistor.

$$\boxed{R_C = 0.2\ \Omega}$$

### Early Voltage ($V_{AF}$)

The Early voltage models the base-width modulation effect in the internal bipolar transistor.

$$I_C = I_S e^{\frac{V_{BE}}{V_T}} \left(1 + \frac{V_{CE}}{V_{AF}}\right)$$

The extracted value is

$$\boxed{V_{AF} = 60\ \text{V}}$$

### Forward Beta Roll-off Current ($I_{KF}$)

This parameter determines the collector current at which the forward current gain starts decreasing due to high-level injection.

$$\boxed{I_{KF} = 0.3\ \text{A}}$$

### Base-Emitter Leakage Current ($I_{SE}$)

The leakage current models the non-ideal behavior of the base-emitter junction.

$$\boxed{I_{SE} = 2 \times 10^{-13}\ \text{A}}$$

### Emission Coefficient ($N_E$)

The emission coefficient represents the deviation of the junction from ideal behavior.

$$\boxed{N_E = 1.8}$$

### Base-Emitter Junction Capacitance ($C_{JE}$)

The depletion capacitance of the base-emitter junction is

$$\boxed{C_{JE} = 120\ \text{pF}}$$

**Base-Emitter Junction Potential ($V_{JE}$)**

The built-in potential of the emitter junction is

$$\boxed{V_{JE} = 0.70 \text{ V}}$$

**Base-Emitter Grading Coefficient ($M_{JE}$)**

The grading coefficient controls the variation of junction capacitance with applied voltage.

$$\boxed{M_{JE} = 0.35}$$

**Base-Collector Junction Capacitance ($C_{JC}$)**

The depletion capacitance of the collector junction is

$$\boxed{C_{JC} = 60 \text{ pF}}$$

**Base-Collector Junction Potential ($V_{JC}$)**

The built-in potential of the collector junction is

$$\boxed{V_{JC} = 0.70 \text{ V}}$$

**Base-Collector Grading Coefficient ($M_{JC}$)**

The grading coefficient of the collector junction is

$$\boxed{M_{JC} = 0.35}$$

**Forward Transit Time ($T_F$)**

The forward transit time determines the turn-on speed of the IGBT.

$$\boxed{T_F = 150 \text{ ns}}$$

**Reverse Transit Time ($T_R$)**

The reverse transit time models the charge storage effect during turn-off.

$$\boxed{T_R = 800 \text{ ns}}$$

### SPICE Model

```
.MODEL eSim_PIGBT PIGBT(
+ IS=1E-14
+ BF=100
+ BR=1
+ RB=15
+ RC=0.2
+ VAF=60
+ IKF=0.3
+ ISE=2E-13
+ NE=1.8
+ CJE=120P
+ VJE=0.70
+ MJE=0.35
+ CJC=60P
+ VJC=0.70
+ MJC=0.35
+ TF=150N
+ TR=800N
)
```

### 4.18.3 Simulation Results

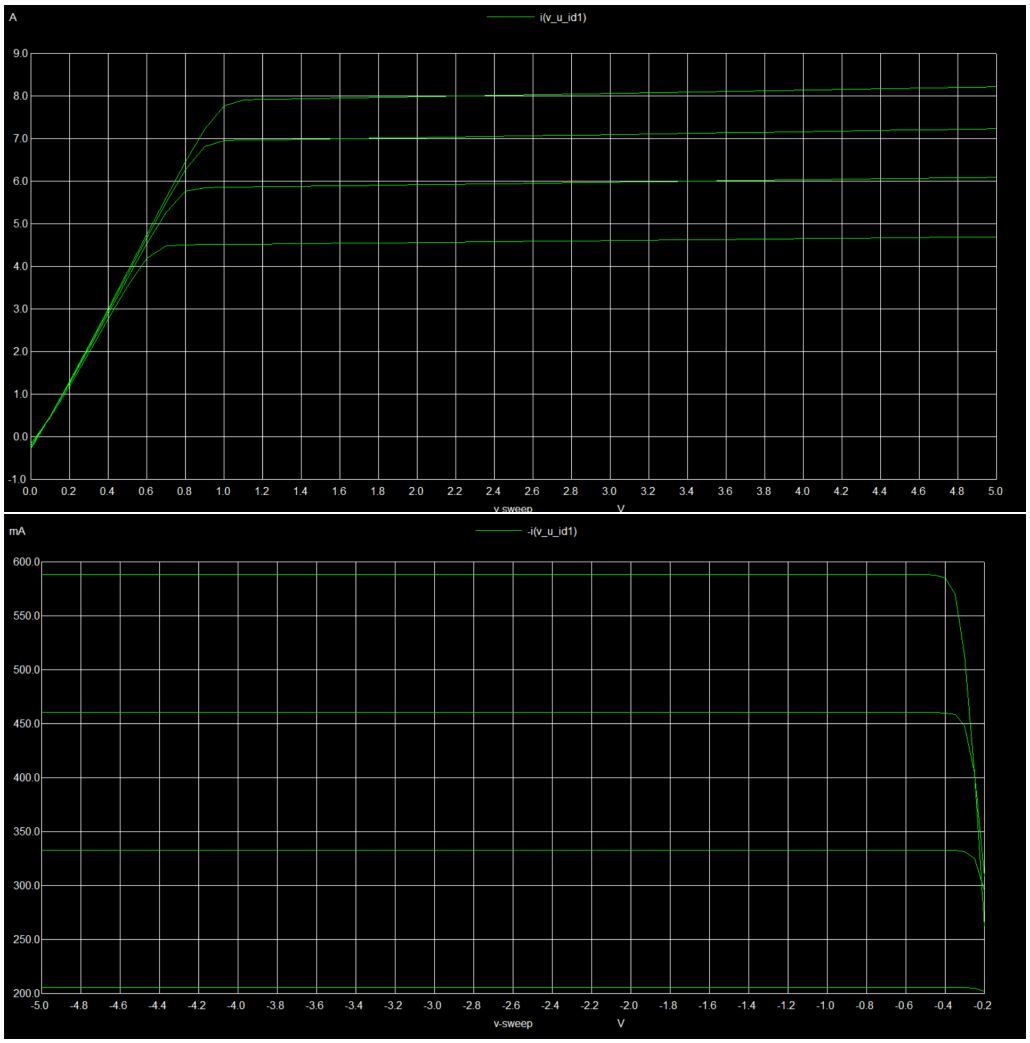


Figure 4.27: Simulation output of PIGBT

## 4.19 IRG4BC20W

### 4.19.1 Schematic

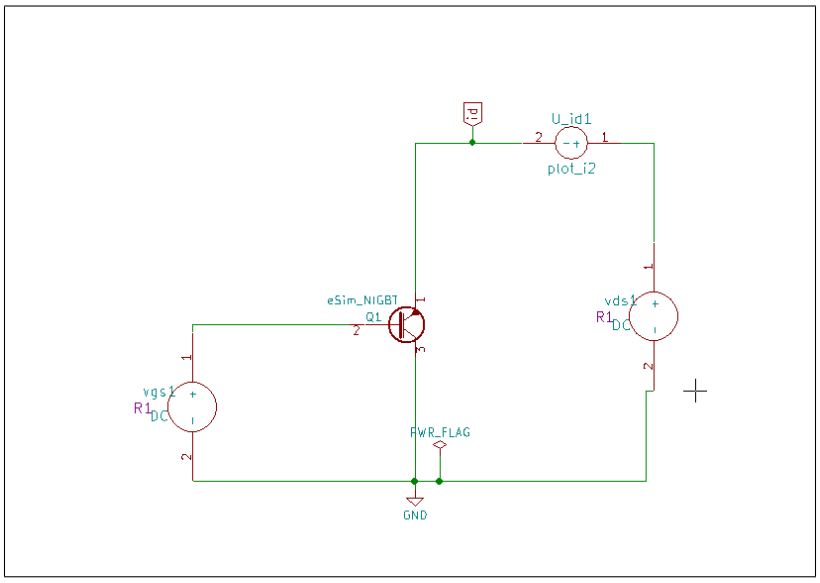


Figure 4.28: JFET Test Circuit

The IRG4BC20W is a high-voltage N-channel Insulated Gate Bipolar Transistor (IGBT) designed for medium-power switching applications. It combines the high input impedance and voltage-controlled gate of a MOSFET with the low conduction loss of a bipolar transistor. The device model was developed using the parameters extracted from the manufacturer's datasheet and implemented in the eSim Model Editor.

### 4.19.2 Threshold Voltage (VT)

The threshold voltage specifies the minimum gate-emitter voltage required to turn the IGBT ON.

$$V_T = 4.50 \text{ V}$$

### 4.19.3 Transconductance Parameter (KP)

The transconductance parameter determines the relationship between the gate voltage and the collector current.

$$K_P = 8.3$$

### 4.19.4 Carrier Lifetime (TAU)

Carrier lifetime determines the stored charge within the device and strongly affects switching performance.

$$\tau = 150 \text{ ns}$$

### 4.19.5 Forward Transconductance Factor (KF)

The forward transconductance correction factor adjusts the collector current characteristics.

$$K_F = 0.25$$

### 4.19.6 Device Active Area (AREA)

The AREA parameter represents the effective conduction area used for current scaling.

$$AREA = 13.0 \times 10^{-6}$$

### 4.19.7 Gate-Drain Overlap Area (AGD)

This parameter represents the effective overlap area between the gate and drain terminals.

$$AGD = 6.5 \times 10^{-6}$$

### 4.19.8 Gate-Source Capacitance (CGS)

The gate-source capacitance influences the gate charging time during switching.

$$C_{GS} = 490 \text{ pF}$$

### 4.19.9 Gate Oxide Capacitance (COXD)

The gate oxide capacitance contributes to the overall gate charge and dynamic response.

$$C_{OXD} = 38 \text{ pF}$$

### 4.19.10 On-State Collector-Emitter Voltage (VTD)

This parameter represents the typical collector-emitter voltage drop during conduction.

$$V_{TD} = 2.16 \text{ V}$$

### 4.19.11 Gate-Drain Capacitance (CGD)

The gate-drain capacitance is responsible for the Miller effect during switching transitions.

$$C_{GD} = 8.8 \text{ pF}$$

### 4.19.12 Total Gate Charge (QG)

The total gate charge specifies the amount of charge required to fully switch the IGBT.

$$Q_G = 26 \text{ nC}$$

### 4.19.13 Maximum Collector-Emitter Voltage (VCES)

This is the maximum voltage that can be safely applied across the collector and emitter terminals.

$$V_{CES} = 600 \text{ V}$$

### 4.19.14 Maximum Collector Current (ICMAX)

The maximum continuous collector current rating of the device is

$$I_{CMAX} = 13 \text{ A}$$

### 4.19.15 Turn-On Delay Time (TDON)

The turn-on delay time represents the interval between the application of the gate signal and the beginning of collector current conduction.

$$T_{DON} = 22 \text{ ns}$$

### 4.19.16 Rise Time (TRISE)

The rise time is the duration required for the collector current to rise from approximately 10% to 90% of its final value.

$$T_{RISE} = 14 \text{ ns}$$

### 4.19.17 Turn-Off Delay Time (TDOFF)

The turn-off delay time specifies the interval between removal of the gate signal and the beginning of current decay.

$$T_{DOFF} = 110 \text{ ns}$$

### 4.19.18 Fall Time (TFALL)

The fall time represents the duration for the collector current to decrease from approximately 90% to 10% of its initial value.

$$T_{FALL} = 64 \text{ ns}$$

### 4.19.19 Maximum Gate-Emitter Voltage (VGEMAX)

The maximum allowable gate-emitter voltage ensures safe operation of the gate oxide.

$$V_{GEMAX} = 20 \text{ V}$$

### 4.19.20 Simulation Result

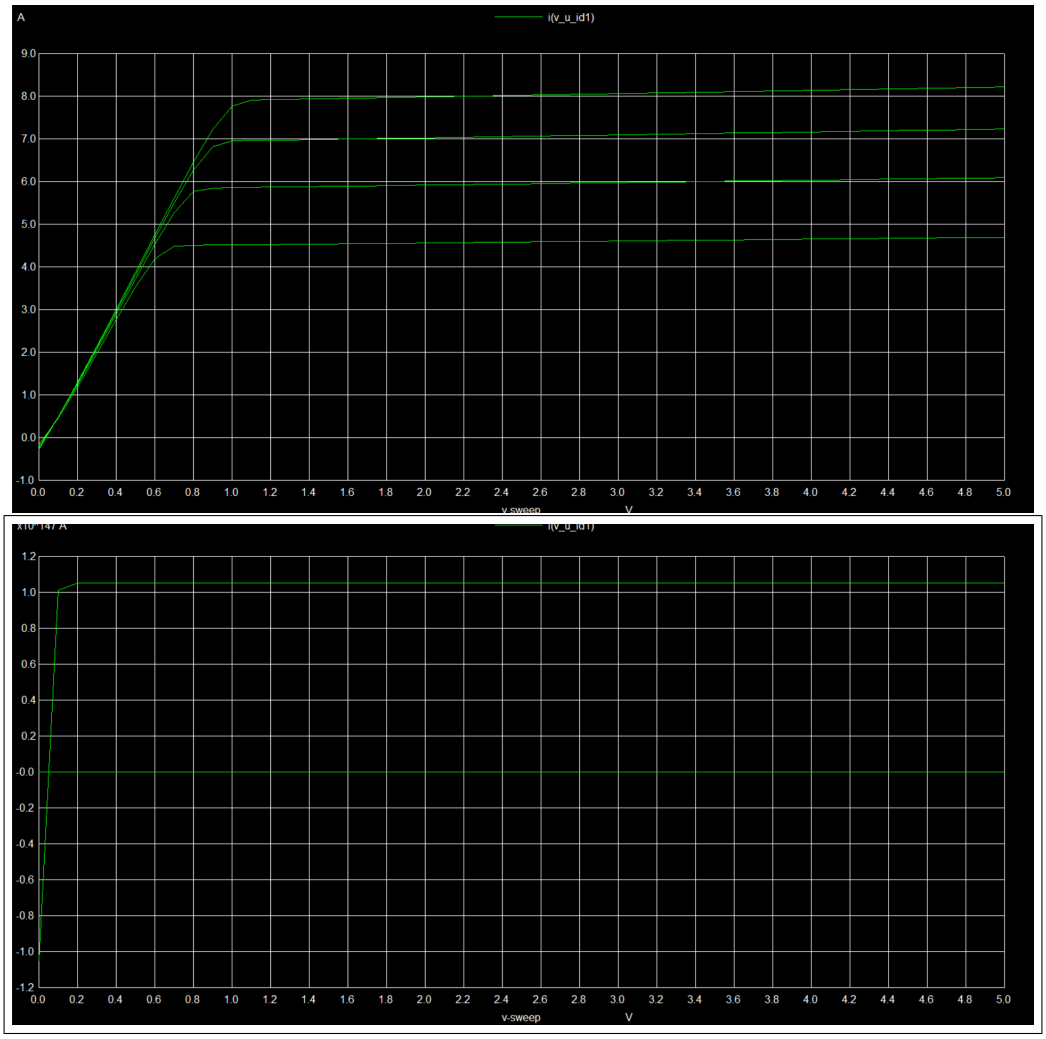


Figure 4.29: IRG4BC20W OUTPUT

The IRG4BC20W device model was implemented in the eSim Model Editor and simulated using Ngspice. Since Ngspice does not provide native support for the `NIGBT` compact model, the simulation was carried out using an `NPN` reference model as an approximation. The obtained output characteristics exhibit the expected collector current variation with increasing control bias and demonstrate the successful implementation of the simplified device model within the eSim environment. During the internship, various electronic devices and integrated circuits were studied, modeled, and simulated using the eSim Electronic Design Automation (EDA) tool. The workflow involved datasheet analysis, schematic symbol creation, subcircuit development, test bench design, and functional verification through Ngspice simulations.

## 4.20 EF25 MAGNETIC CORE

### 4.20.1 Schematic

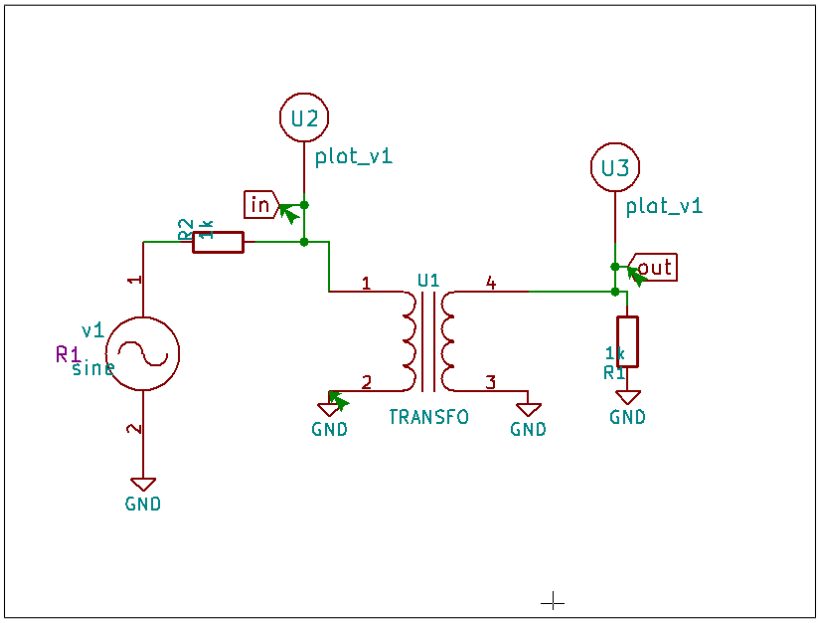


Figure 4.30: Magnetic Core

### 4.20.2 EF25 Magnetic Core Model Parameters

The EF25 magnetic core is modeled using the `Core` model available in Ngspice. This model represents the nonlinear magnetic characteristics of a ferrite core used in transformers and inductors. The parameters extracted for the EF25 magnetic core are listed below.

```
.MODEL EF25_Magnetic_Core Core(
+ A=44.82
+ C=.4112
+ abc=123
+ Area=0.525
+ K=25.74
+ MS=415.2K
+ Path=5.75
+ ALPHA=1e-6
)
```

#### Parameter A

**Value:** 44.82

The parameter $A$ is the hysteresis coefficient of the magnetic core. It determines the amplitude of the magnetic hysteresis loop and influences the magnetization behavior of the ferrite material.

### Parameter C

**Value:** 0.4112

The parameter $C$ is a fitting coefficient of the hysteresis model. It adjusts the shape of the B-H curve and improves agreement with measured magnetic characteristics.

### Parameter abc

**Value:** 123

The parameter `abc` is an empirical fitting constant used internally by the core model. It is selected to match the experimental magnetic response of the EF25 ferrite core.

### Core Cross-sectional Area (Area)

**Value:** 0.525

The `Area` parameter specifies the effective magnetic cross-sectional area of the ferrite core. A larger core area allows greater magnetic flux while reducing flux density.

### Parameter K

**Value:** 25.74

The parameter $K$ represents the magnetic coupling coefficient used by the hysteresis model. It affects the nonlinear relationship between magnetic field strength and magnetic flux density.

### Saturation Magnetization (MS)

**Value:** 415.2K

The parameter `MS` represents the saturation magnetization of the ferrite material. It specifies the maximum magnetic flux density that can be achieved before magnetic saturation occurs.

### Magnetic Path Length (Path)

**Value:** 5.75

The `Path` parameter specifies the effective magnetic path length of the core. This value is used to determine the magnetic reluctance and inductance of the magnetic component.

### Temperature Coefficient ($\alpha$)

**Value:** $1 \times 10^{-6}$

The parameter $\alpha$ represents the temperature coefficient of the magnetic material. It models the variation of magnetic properties with temperature. The small value indicates that the magnetic characteristics remain nearly constant over normal operating temperatures.

### 4.20.3 Simulation Result

The EF25 magnetic core model was incorporated into a transformer test circuit and simulated using the transient analysis feature of Ngspice integrated with eSim. The simulation verified the magnetic core integration and demonstrated the expected transformer excitation behavior. Since the available `Core` model primarily represents the nonlinear magnetic characteristics of the ferrite material, the transient waveforms confirm successful incorporation of the EF25 magnetic core into the transformer model rather than providing a complete magnetic hysteresis (B-H) characterization.

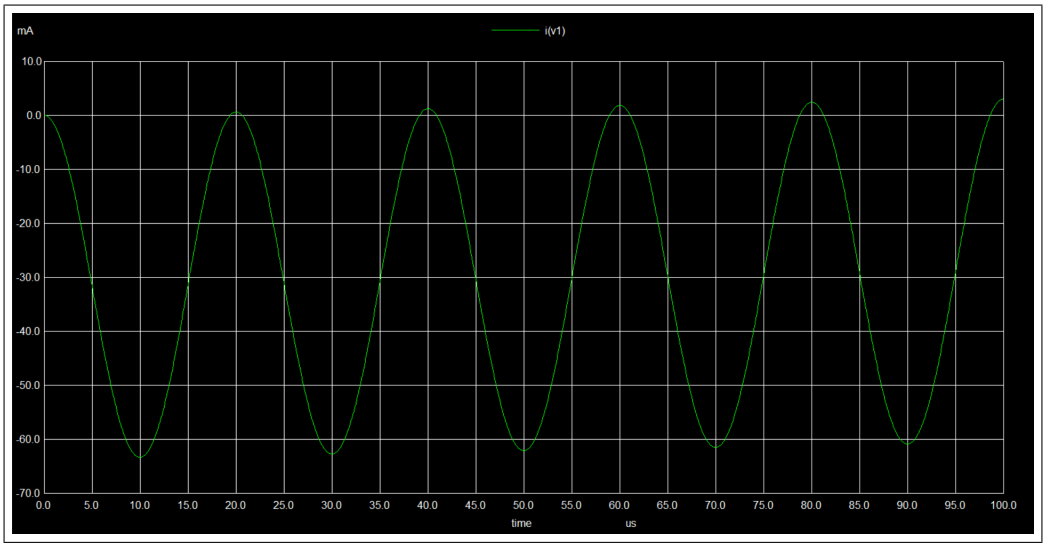


Figure 4.31: Magnetic Core OUTPUT

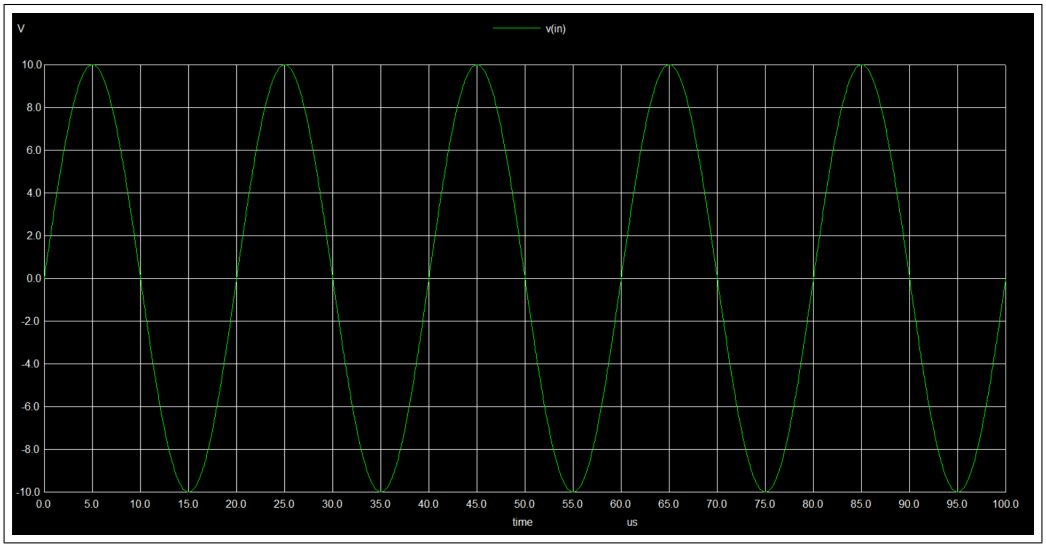


Figure 4.32: Magnetic Core OUTPUT

This internship at the FOSSEE Project, Indian Institute of Technology Bombay, provided an excellent opportunity to gain practical experience in semiconductor device modeling and SPICE-based circuit simulation using open-source Electronic Design Automation (EDA) tools. Throughout the internship, various semiconductor devices, including MOSFETs, BJTs, JFETs, diodes, IGBTs, and magnetic core models, were successfully developed, parameterized, and validated using eSim and Ngspice based on their respective datasheet specifications.

The internship significantly enhanced my understanding of SPICE modeling techniques, semiconductor device characteristics, datasheet interpretation, and simulation-based verification. It also provided valuable exposure to the process of extracting device parameters, developing reusable device libraries, creating appropriate test circuits, and analyzing the electrical characteristics of different electronic components through DC and transient simulations.

Working with open-source tools such as eSim, Ngspice, and KiCad strengthened my practical skills in electronic circuit design, simulation, debugging, and verification while demonstrating the importance of open-source software in engineering education and research. The knowledge and experience gained during this internship have greatly improved my technical competence and problem-solving abilities in electronic system design.

The developed device models can be incorporated into the eSim device library, enabling students, educators, and researchers to perform accurate circuit simulations using open-source tools. Overall, this internship has been a highly rewarding learning experience that has strengthened my foundation in semiconductor device modeling and inspired me to continue contributing to the development of open-source EDA technologies.

# Bibliography


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