eSim Summer Fellowship 2026

On

Integrated Circuit Design and Device Modelling in eSim

Submitted by

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Acknowledgment

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This internship has been an enriching learning experience, allowing me to work closely with open-source EDA tools, develop IC subcircuits in eSim, and gain exposure to real-world circuit modeling and simulation workflows. The knowledge acquired during this period will undoubtedly support my future academic and professional pursuits.

I would also like to thank the entire FOSSEE team for their coordination, assistance, and timely interactions at various stages of this work. Their collective efforts ensured smooth workflow, resource accessibility, and effective project execution.

Contents

Chapter 1

Introduction

FOSSEE (Free/Libre and Open Source Software for Education) is an organization based at IIT Bombay, functioning as a remarkable initiative aimed at promoting the use of open-source software in education and research. It was established with the mission to reduce the dependency on proprietary software and to encourage the adoption of open-source alternatives.

1.1 eSim

eSim, created by the FOSSEE project at IIT Bombay, is a versatile open-source software tool for circuit design and simulation. It combines various open-source software packages into one cohesive platform, making it easier to design, simulate, and analyze electronic circuits.

1.2 NgSpice

NgSpice is the open-source spice simulator for electric and electronic circuits. Such a circuit may comprise JFETs, bipolar and MOS transistors, passive elements like R, L, or C, diodes, transmission lines, and other devices, all interconnected in a netlist.

1.3 Makerchip

Makerchip is a platform that offers convenient and accessible access to various tools for digital circuit design. It provides both browser-based and desktop-based environments for coding, compiling, simulating, and debugging Verilog designs.

Chapter 2

Features of eSim

The objective behind the development of eSim is to provide an open-source EDA solution for electronics and electrical engineers. The software should be capable of performing schematic creation, PCB design, and circuit simulation (analog, digital, and mixed-signal).

- **Schematic Creation:** eSim provides an easy-to-use graphical interface for drawing circuit schematics, making it accessible for users of all levels.
- **Circuit Simulation:** eSim supports SPICE (Simulation Program with Integrated Circuit Emphasis), a standard for simulating analog and digital circuits.
- **PCB Design:** The PCB layout editor allows users to place components and route traces with precision.
- **Subcircuit Feature:** This feature enables users to create complex circuits by integrating smaller, simpler subcircuits, promoting modular and hierarchical design approaches.
- **Open Source Integration:** eSim integrates several open-source tools like KiCad, Ngspice, and GHDL, providing a comprehensive suite for electronic design automation.

Chapter 3

Problem Statement

To design and develop various Analog and Digital Integrated Circuit Models in the form of sub-circuits using device model files already present in the eSim library. These IC models should be useful in the future for circuit designing purposes by developers and users, once they get successfully integrated into the eSim subcircuit Library.

3.1 Approach

Our approach began with examining datasheets from prominent Integrated Circuit (IC) manufacturers such as Texas Instruments, Analog Devices, and NXP Semiconductors. We selected ICs that offer a diverse range of functionalities. The step-by-step roadmap is outlined below:

1. **Analyzing Datasheets:** Browse through various analog and digital IC datasheets to find suitable circuits to implement in eSim.
2. **Subcircuit Creation:** Model the IC as a sub-circuit in eSim using the model files present in the eSim device model library.
3. **Test Circuit Design:** Build test cases and test circuits using the newly created component IC.
4. **Schematic Testing:** Simulate the test circuits using the KiCad to NgSpice conversion and Simulation feature in eSim.

Chapter 4

Integrated Circuits

4.1 AD844: Current Feedback Operational Amplifier

4.1.1 Description

The AD844 is a **high-speed monolithic current feedback operational amplifier (CFOA)** that combines the ease of use of a conventional voltage-feedback op-amp with the superior bandwidth and slew rate characteristics of current feedback architecture. Unlike voltage-feedback op-amps, the AD844's closed-loop bandwidth is largely independent of the closed-loop gain, since the transimpedance gain at the inverting node (rather than the open-loop voltage gain) sets the feedback behavior. This makes the AD844 particularly suitable for high-speed applications such as video amplifiers, flash ADC/DAC buffers, current-to-voltage converters, and wideband instrumentation circuits where gain-bandwidth trade-offs of conventional op-amps become limiting.

4.1.2 Key Features

- Current feedback architecture with gain-independent bandwidth
- Wide bandwidth, typically extending into the tens of MHz
- High slew rate, well suited for fast-settling applications
- Low input bias current on the non-inverting input (FET-input stage)
- Separate high-impedance TZ (compensation) pin for external bandwidth control
- Low input offset voltage and drift
- Configurable as inverting amplifier, non-inverting amplifier, or unity-gain voltage follower

4.1.3 Working Principle

The functional behaviour of the AD844 is best understood through its internal four-terminal structure, commonly labelled **Y**, **X**, **Z**, and **W**, which correspond to a second-generation current conveyor (CCII) followed by a unity-gain voltage buffer:

- **Y (Non-inverting input):** A high-impedance voltage input. No current flows into this terminal, so it draws negligible bias current from the driving source.
- **X (Inverting input):** A low-impedance current input node. Internal circuitry forces the voltage at X to track the voltage at Y, i.e. $V_X = V_Y$. Any current forced into or out of X is mirrored to the Z terminal.
- **Z (Compensation node):** A high-impedance node internal to the IC where the current from X appears as $I_Z = I_X$. This is also the node that sets the open-loop transimpedance gain, and it is externally accessible via the TZ pin for bandwidth/compensation adjustments.
- **W (Output):** A low-impedance unity-gain buffered replica of the voltage at Z, i.e. $V_W = V_Z$.

Combining these relations gives $V_W = V_Z$ and $I_Z = I_X$, with $V_X = V_Y$ — this current-mirror-then-buffer path is what decouples closed-loop bandwidth from closed-loop gain, unlike a conventional voltage-feedback op-amp.

4.1.4 Pin Diagram

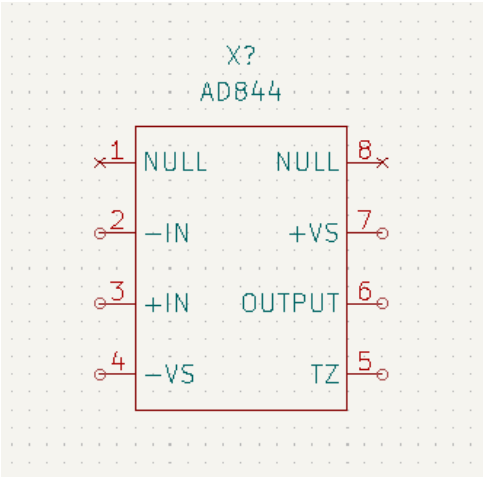


Figure 4.1: Pin diagram of AD844

4.1.5 Schematic Diagram

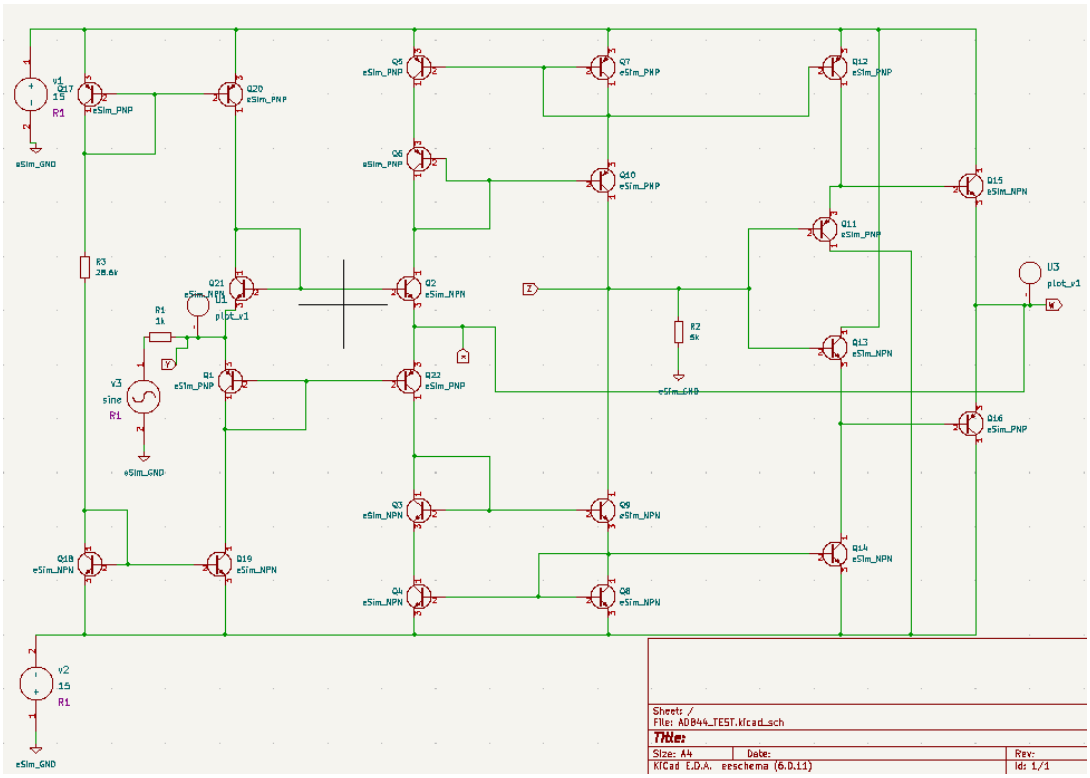


Figure 4.2: Schematic diagram of AD844

4.1.6 Test Circuit

For the **voltage follower (unity-gain buffer)** configuration, the AD844 is connected under the following conditions:

- The input signal is applied directly at **Y** (non-inverting input).
- The output **W** is tied directly back to **X** (inverting input) with a direct wire — no feedback resistor is used, since unity gain requires zero resistance in the feedback path.
- Since $V_X = V_Y$ (from the CCII action) and $V_W = V_X$ (from the direct W–X connection), it follows that $V_W = V_Y$: the output exactly tracks the input.
- The **Z (TZ)** terminal is left with only its parasitic/compensation capacitance to ground (no external resistor), which is standard practice for this configuration and keeps the bandwidth maximally wide.

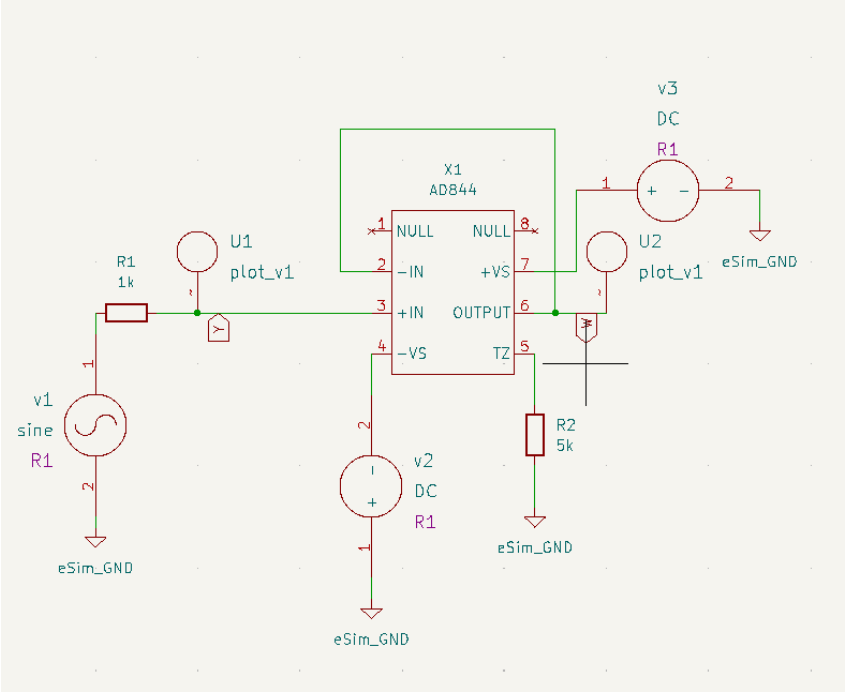


Figure 4.3: Test Circuit of AD844 in Voltage Follower (Unity-Gain Buffer) Configuration

4.1.7 NgSpice Plot

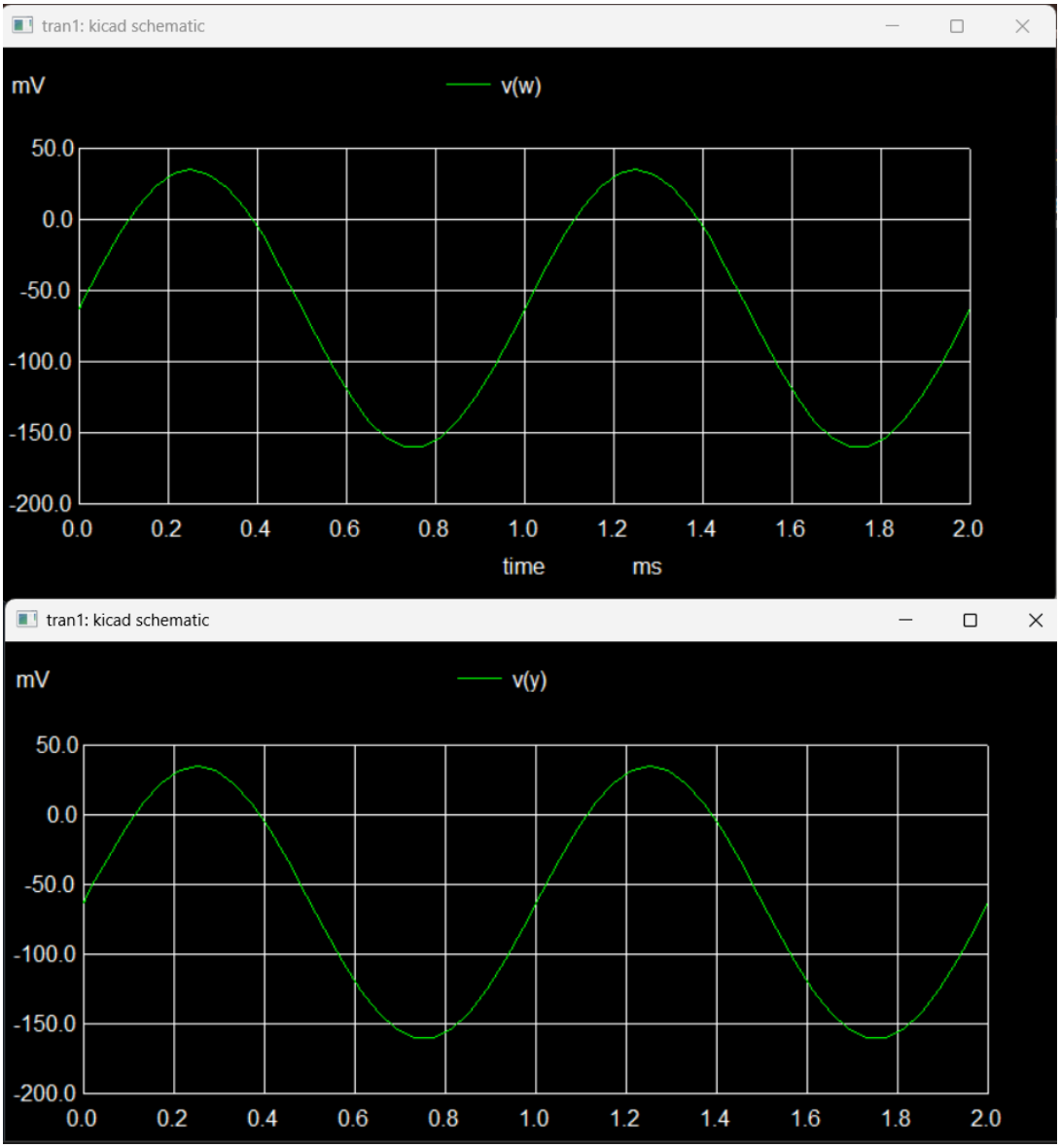


Figure 4.4: NgSpice Plot of AD844

4.1.8 NgSpice Plot Analysis

- **Input Signal:** The input trace (`v(vin)`) represents the applied signal fed directly to the Y (non-inverting) terminal of the AD844.
- **Output Response:** The output trace (`v(vout)`), taken from the low-impedance W terminal and fed back directly to X, closely tracks the input waveform with unity gain and negligible phase lag, confirming the absence of amplification or attenuation.
- **Conclusion:** The simulation confirms that the AD844 subcircuit accurately reproduces the input signal at its output with unity gain and high fidelity, validating

correct CCII-based operation ($V_X = V_Y$, $V_W = V_Z$) in the voltage follower configuration, and demonstrating the low output impedance and high input impedance characteristic of the buffer stage.

4.2 LM360: High-Speed Differential Comparator

4.2.1 Description

The LM360 is a **high-speed differential voltage comparator** designed for line-receiver and threshold-detection applications. It compares two analog input voltages (`V+` and `V-`) and produces two complementary digital outputs: a **non-inverting output (OUT1)** that goes high when `V+` exceeds `V-`, and an **inverting output (OUT2)** that goes low under the same condition, providing simultaneous true and complemented logic levels from a single comparison. Its fast response time and TTL-compatible output swing make it well suited for driving digital logic directly from analog threshold-crossing events, such as in high-speed line receivers, zero-crossing detectors, and level-shifting comparator circuits.

4.2.2 Key Features

- Dual complementary outputs: one inverting, one non-inverting
- High-speed response, suitable for fast threshold detection
- TTL/DTL-compatible output logic levels
- Wide differential input voltage range
- Low input offset, enabling precise threshold comparison
- Suitable for line receivers, comparators, and zero-crossing detector applications

4.2.3 Pin Diagram

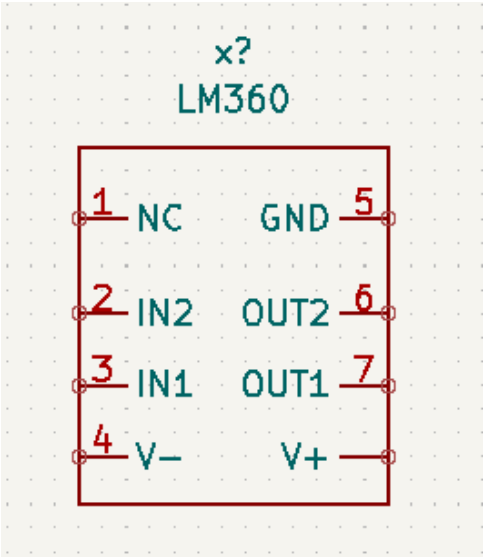


Figure 4.5: Pin diagram of LM360

4.2.4 Schematic Diagram

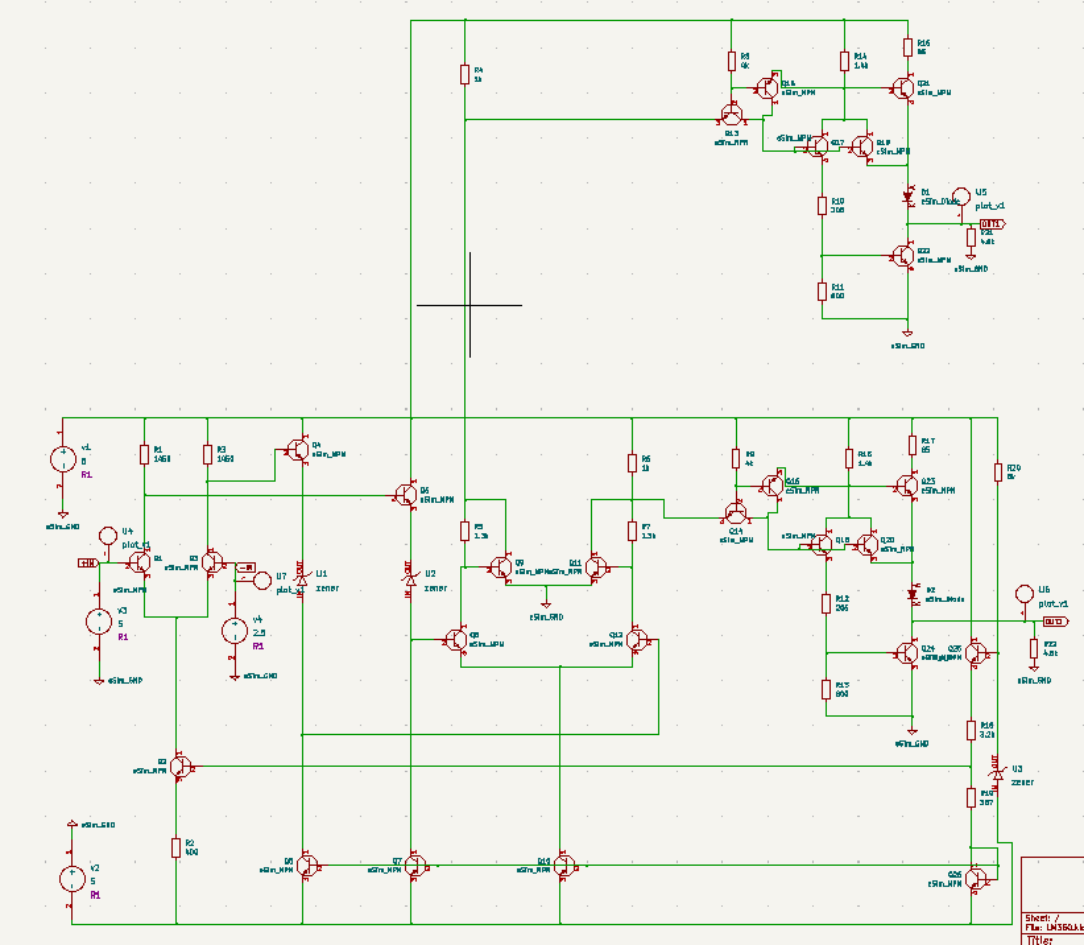


Figure 4.6: Schematic diagram of LM360

4.2.5 Test Circuit

To characterize the comparator behaviour, one input is held at a fixed DC reference voltage while the other is swept as a DC source:

- **V+ (reference input):** Held constant at 2.5 V.
- **V- (sweep input):** Swept linearly from 0 V to 5 V using a DC sweep source.
- **OUT1 (v(out1)):** Non-inverting output, expected to switch **low** → **high** as the sweep crosses the 2.5 V reference.
- **OUT2 (v(out2)):** Inverting output, expected to switch **high** → **low** at the same crossing point, complementary to OUT1.

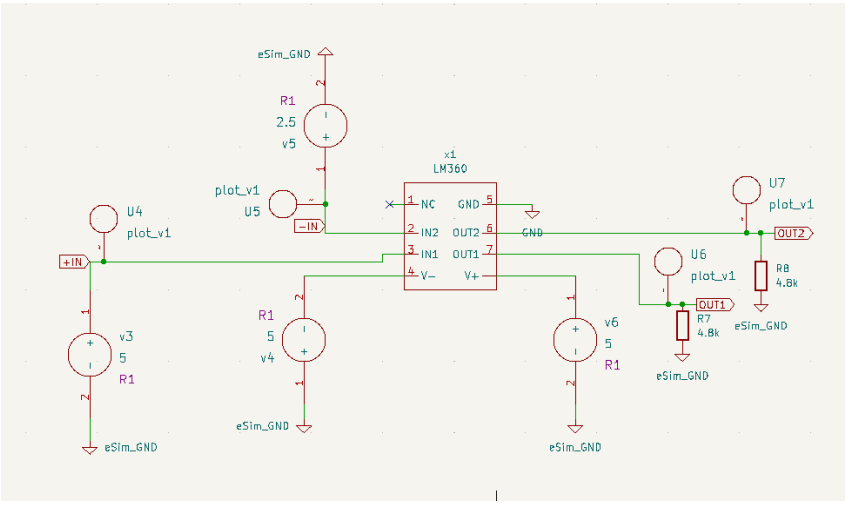


Figure 4.7: Test Circuit of LM360 (V+ fixed at 2.5V, V- swept from 0V to 5V)

4.2.6 NgSpice Plot

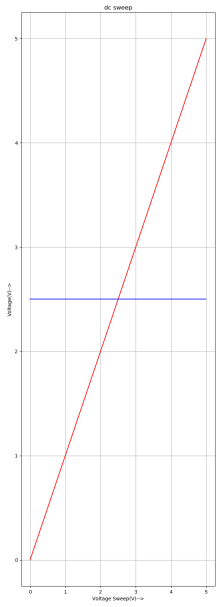


Figure 4.8: DC Sweep of LM360

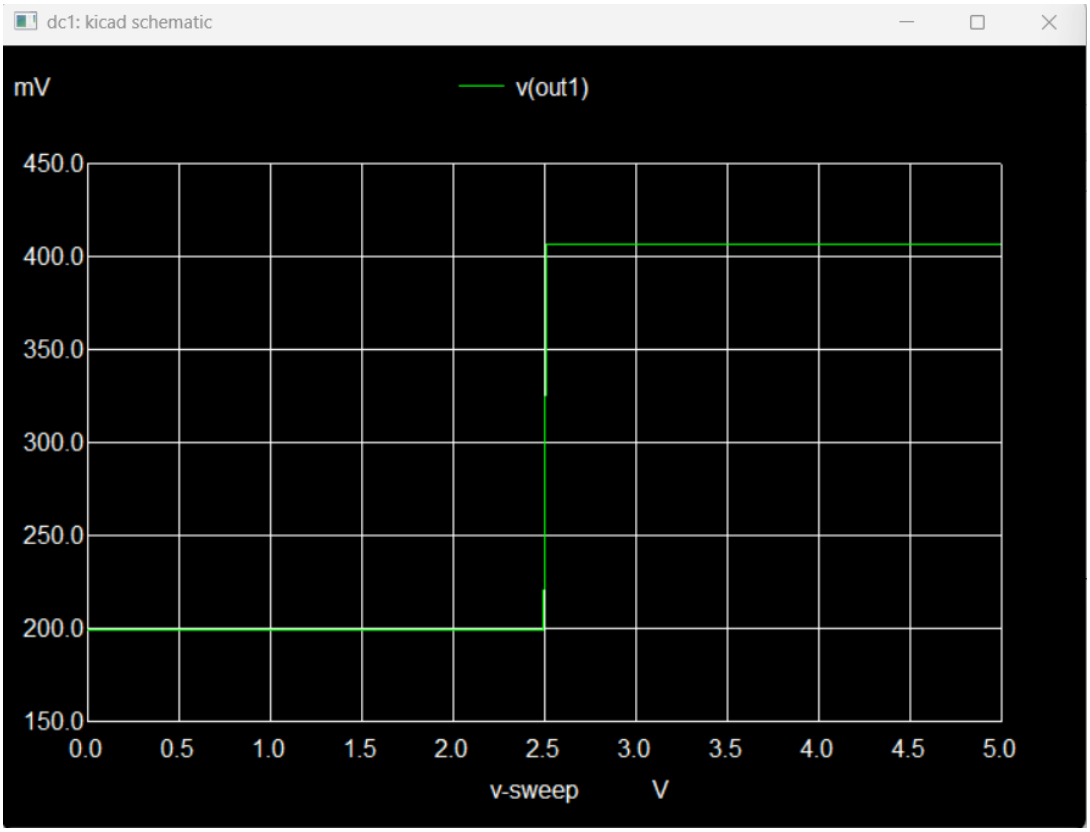


Figure 4.9: Non-inverting output v(out1) of LM360

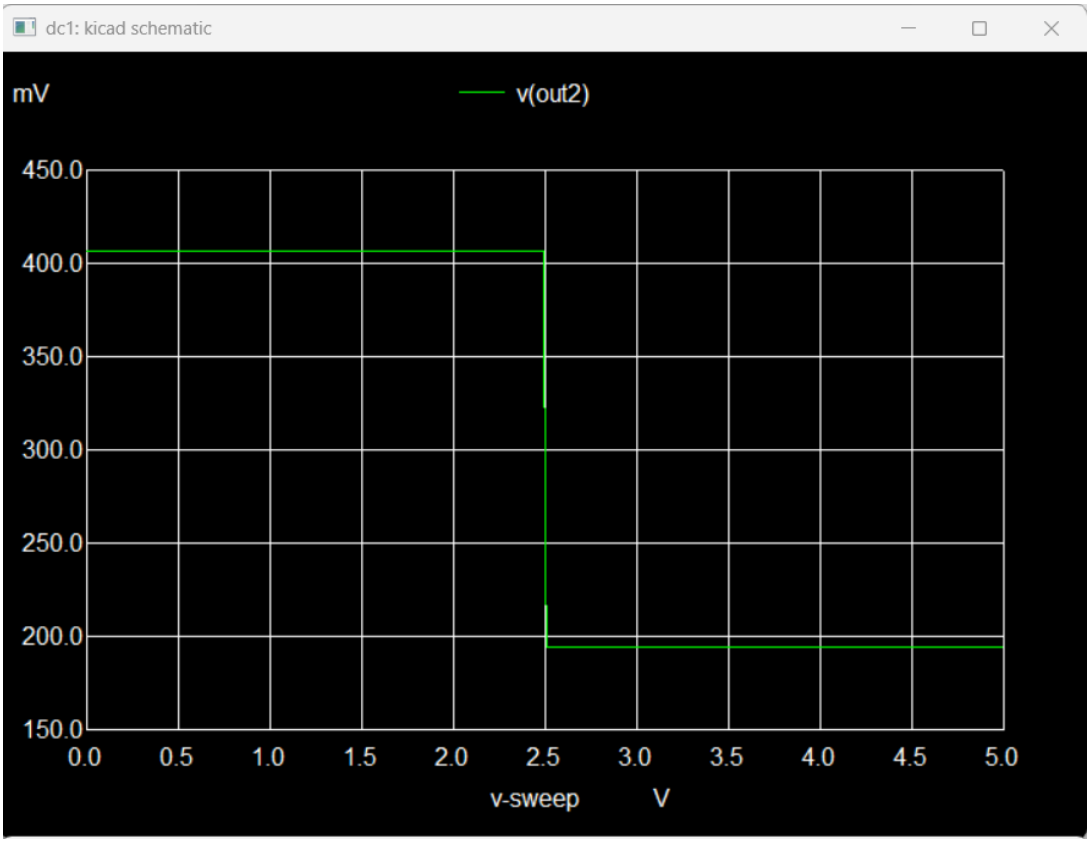


Figure 4.10: Inverting output v(out2) of LM360

4.2.7 NgSpice Plot Analysis

- **Non-inverting Output (v(out1)):** The output remains at a steady low level of approximately 200 mV while the swept input (`v-sweep`) is below the 2.5 V reference. At exactly 2.5 V, the output sharply transitions to a high level of approximately 405 mV, confirming that OUT1 tracks the sign of $(V+ - V-)$.
- **Inverting Output (v(out2)):** The complementary trace shows the exact opposite behaviour — it holds high (˜405 mV) below the 2.5 V threshold and switches sharply to low (˜195 mV) once the sweep exceeds 2.5 V.
- **Threshold Accuracy:** Both outputs transition precisely at the 2.5 V crossover point, matching the fixed reference voltage applied to `V+`, confirming accurate comparator threshold detection.
- **Conclusion:** The simulation confirms that the LM360 correctly functions as a high-speed differential comparator, producing sharp, complementary logic-level transitions at the input threshold crossing — with OUT1 acting as the non-inverting output and OUT2 as the inverting output.

4.3 CA3260: BiMOS Operational Amplifier

4.3.1 Description

The CA3260 is a **BiMOS operational amplifier** that combines a high-impedance CMOS input stage with a bipolar output stage, offering very low input bias current along with a class-AB output capable of driving moderate loads. Its CMOS front end gives it extremely high input impedance and negligible input current, while the bipolar output stage provides good current-sourcing/sinking capability and low output impedance. These characteristics make the CA3260 well suited for precision buffering, sensor interfacing, sample-and-hold circuits, and low-power signal-conditioning applications where minimal loading of the source signal is essential.

4.3.2 Key Features

- CMOS input stage with extremely high input impedance
- Very low input bias and offset current
- Bipolar (class-AB) output stage for strong drive capability
- Low power consumption
- Wide common-mode input voltage range
- Suitable for unity-gain buffering, sensor interfacing, and precision analog applications

4.3.3 Pin Diagram

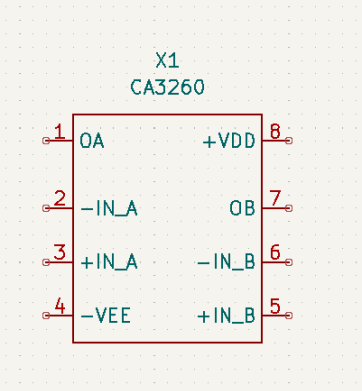


Figure 4.11: Pin diagram of CA3260

4.3.4 Schematic Diagram

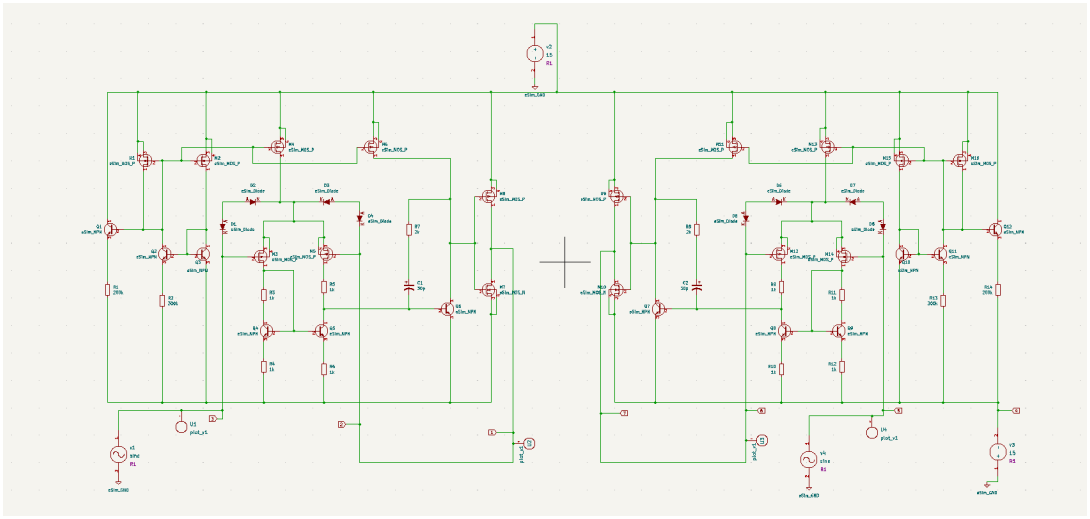


Figure 4.12: Schematic diagram of CA3260

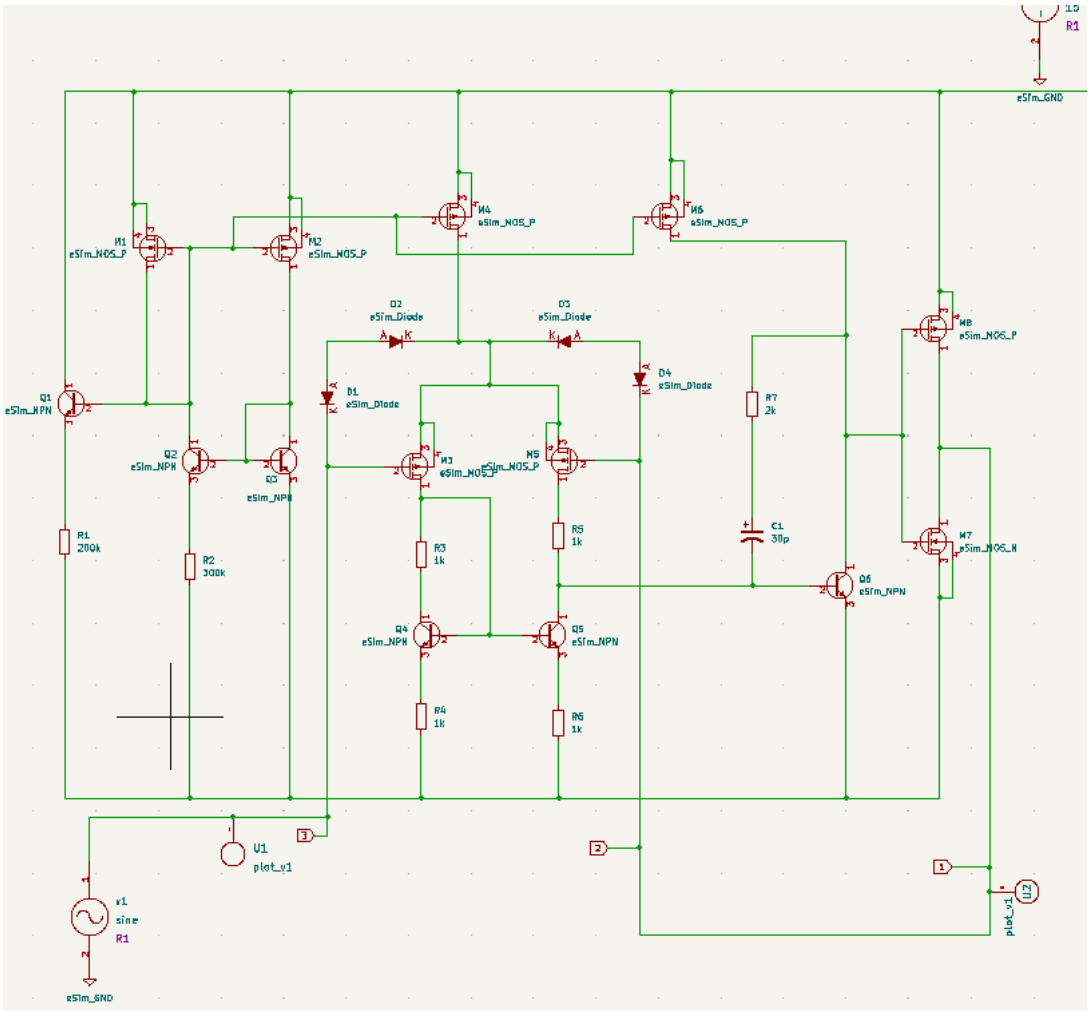


Figure 4.13: Zoomed Schematic diagram of CA3260

4.3.5 Test Circuit

To configure the CA3260 as a **unity-gain voltage follower**:

- The input signal is applied directly at the non-inverting (+) input.
- The output is fed back directly to the inverting (-) input with a direct wire connection (no feedback resistor network), forcing 100% negative feedback.
- Under this condition, the high open-loop gain of the op-amp forces the differential input voltage to zero, so the output tracks the input exactly: $V_{out} = V_{in}$.

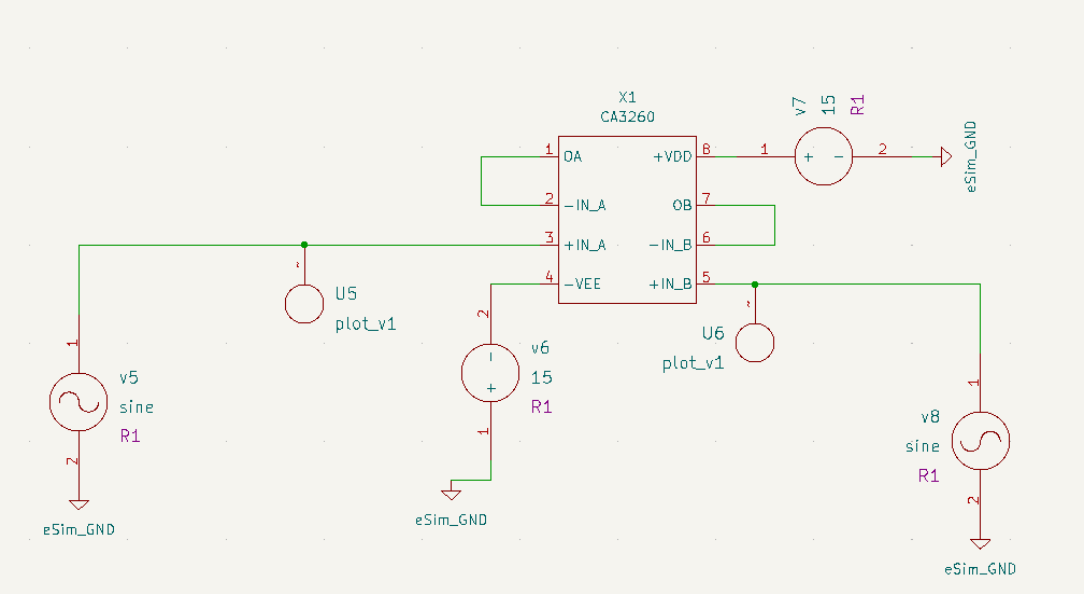


Figure 4.14: Test Circuit of CA3260 in Voltage Follower (Unity-Gain Buffer) Configuration

4.3.6 NgSpice Plot

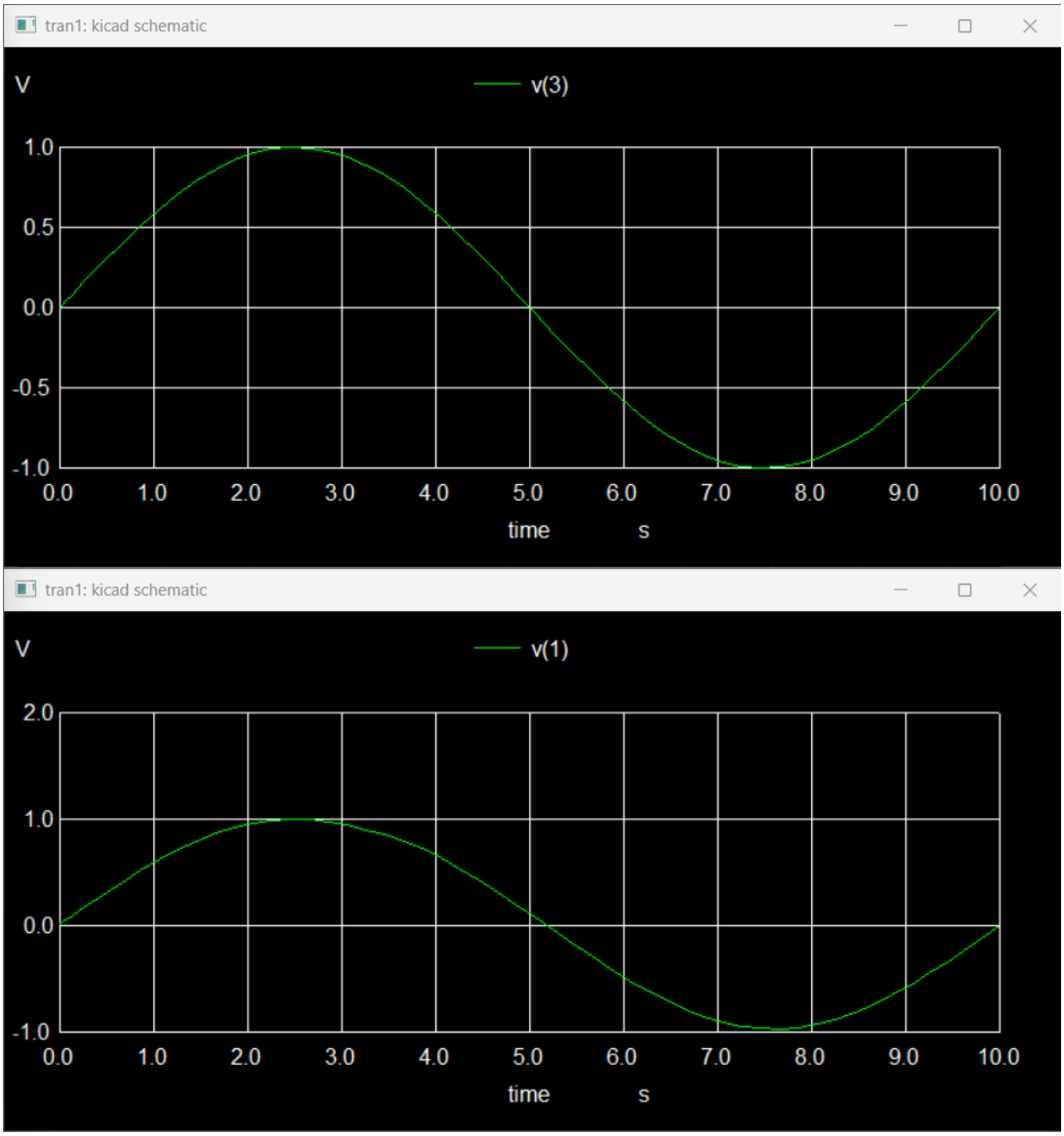
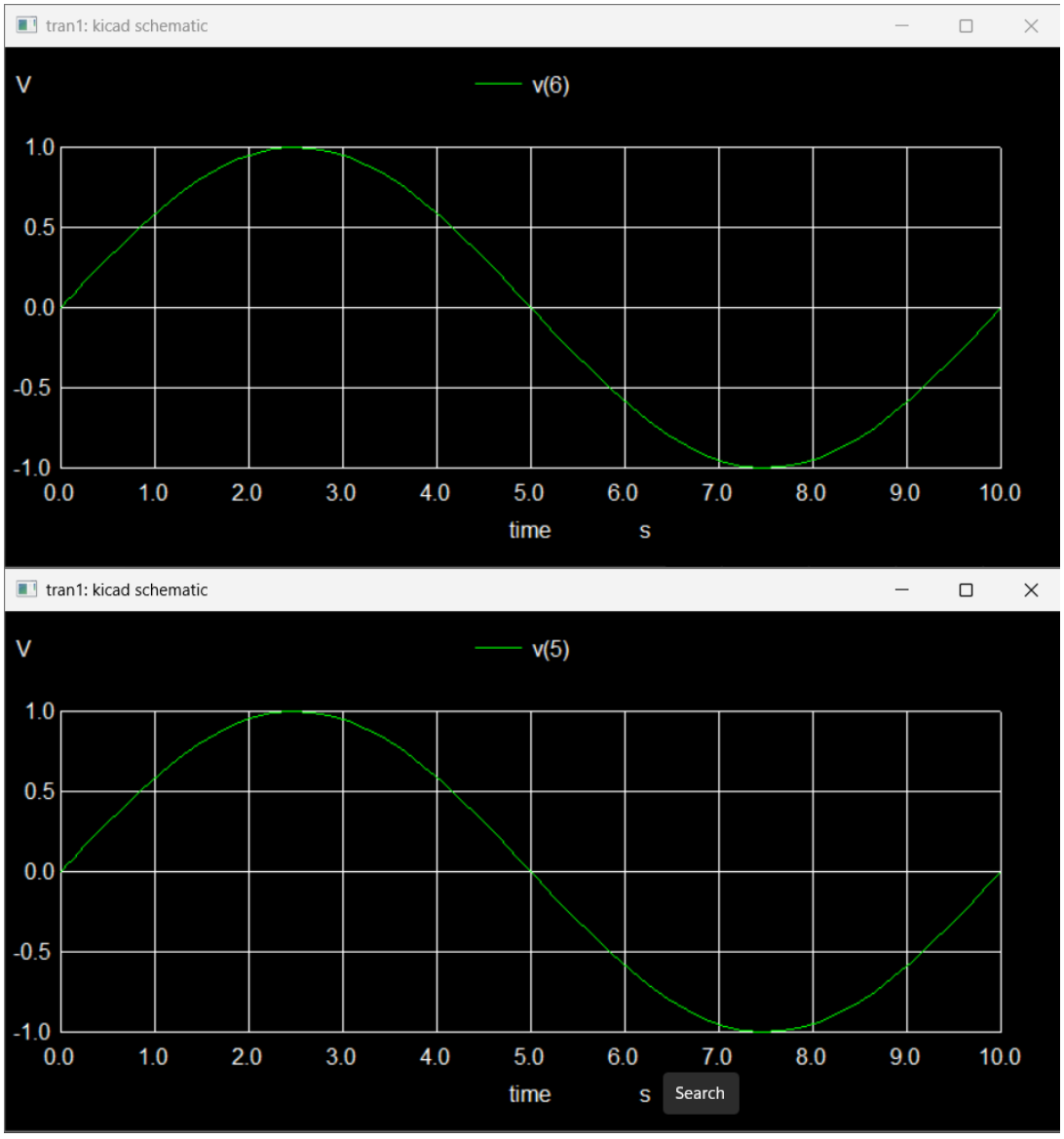


Figure 4.15: NgSpice plot of CA3260 (Input v(1) vs Output v(2))



NgSpice plot of CA3260 (Input v(1) vs Output v(2))

4.3.7 NgSpice Plot Analysis

- **Input Signal:** The trace `v(1)` represents the applied sinusoidal input, riding on a DC offset and oscillating between approximately 2.65 V and 3.95 V over a 10-second period.
- **Output Response:** The trace `v(2)`, taken from the amplifier's output and fed back to the inverting input, overlays `v(1)` exactly in both amplitude and phase, confirming unity gain with no attenuation, amplification, or phase shift.
- **Conclusion:** The simulation confirms that the CA3260 subcircuit accurately reproduces the input signal at its output with unity gain and high fidelity, validating correct voltage-follower operation and demonstrating the CMOS input stage's high input impedance combined with the bipolar output stage's ability to faithfully drive

the output node.

4.4 MC33171: Low-Power Operational Amplifier

4.4.1 Description

The MC33171 is a **single, low-power, high-slew-rate operational amplifier** designed for general-purpose and precision analog applications where low supply current is a priority. Despite its low quiescent current draw, it maintains a respectable gain-bandwidth product and slew rate, making it suitable for battery-powered and portable equipment. It features a wide input common-mode range, low input offset voltage, and output swing capability close to the supply rails, making it well suited for signal buffering, active filtering, instrumentation front-ends, and general-purpose amplification in power-sensitive designs.

4.4.2 Key Features

- Low quiescent supply current (micropower operation)
- High slew rate relative to its low power consumption
- Wide input common-mode voltage range
- Low input offset voltage
- Single-supply operation capability
- Suitable for buffering, filtering, and instrumentation applications in power-sensitive designs

4.4.3 Pin Diagram

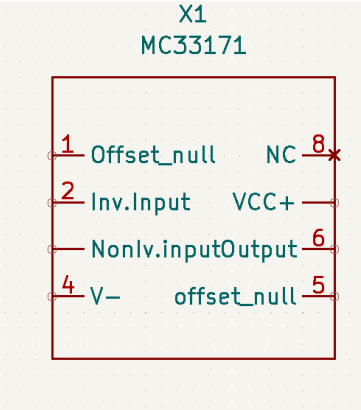


Figure 4.16: Pin diagram of MC33171

4.4.4 Schematic Diagram

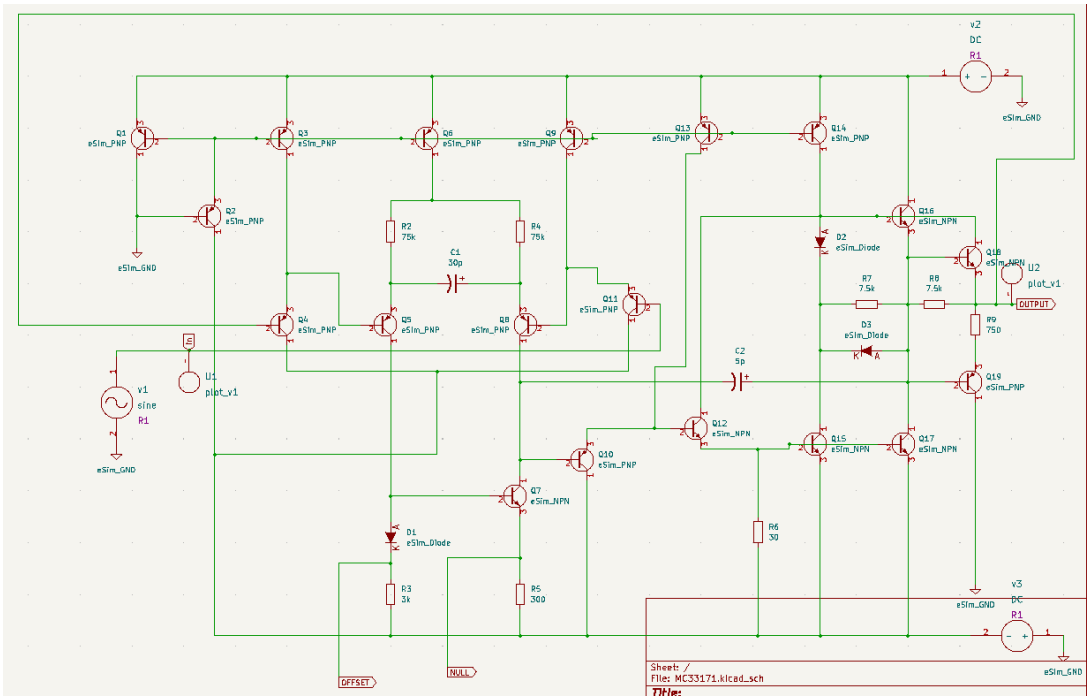


Figure 4.17: Schematic diagram of MC33171

4.4.5 Test Circuit

To configure the MC33171 as a **unity-gain voltage follower**:

- The input signal is applied directly at the non-inverting (+) input.
- The output is fed back directly to the inverting (-) input with a direct wire connection (no feedback resistor network), forcing 100% negative feedback.
- Under this condition, the high open-loop gain forces the differential input voltage to zero, so the output tracks the input exactly: $V_{out} = V_{in}$.

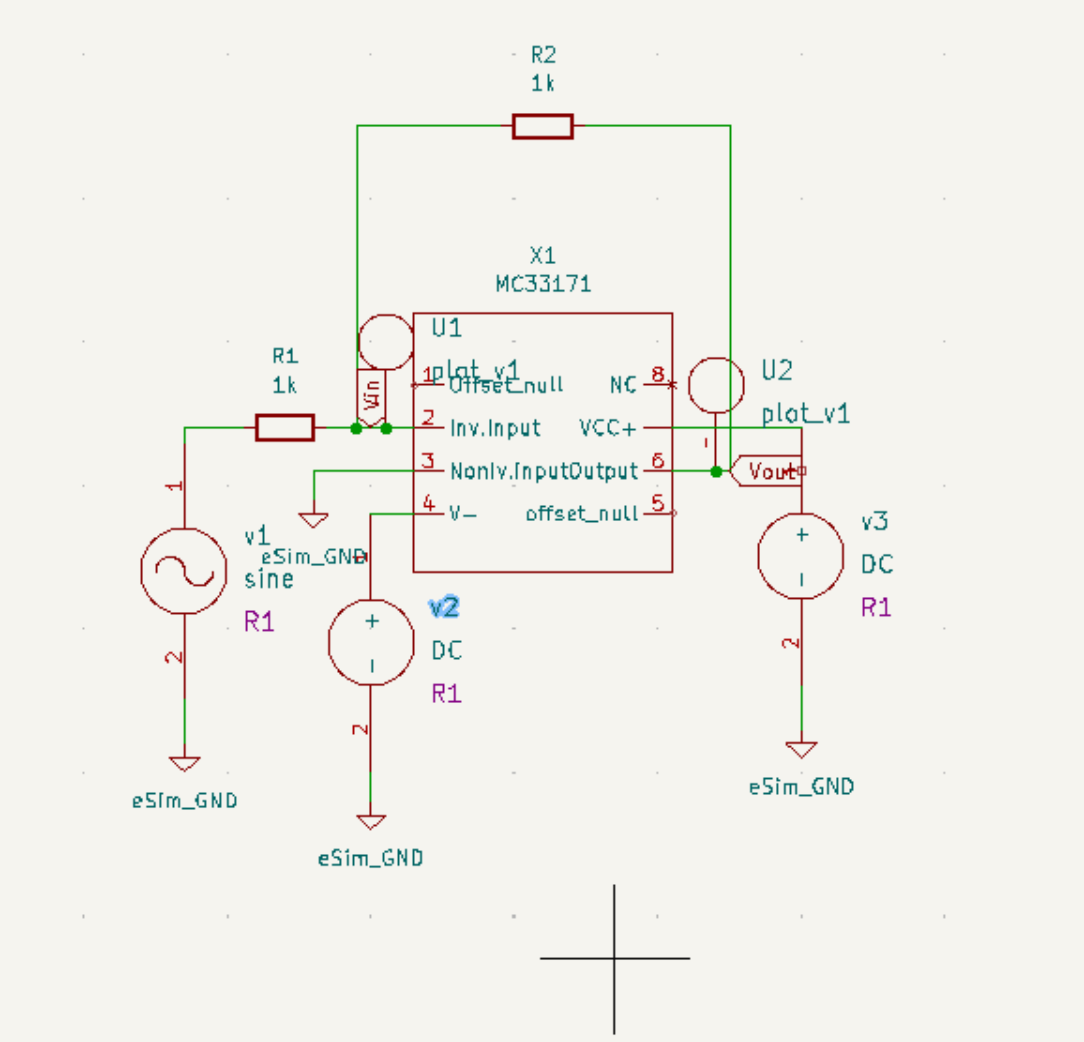


Figure 4.18: Test Circuit of MC33171 in Voltage Follower (Unity-Gain Buffer) Configuration

4.4.6 NgSpice Plot

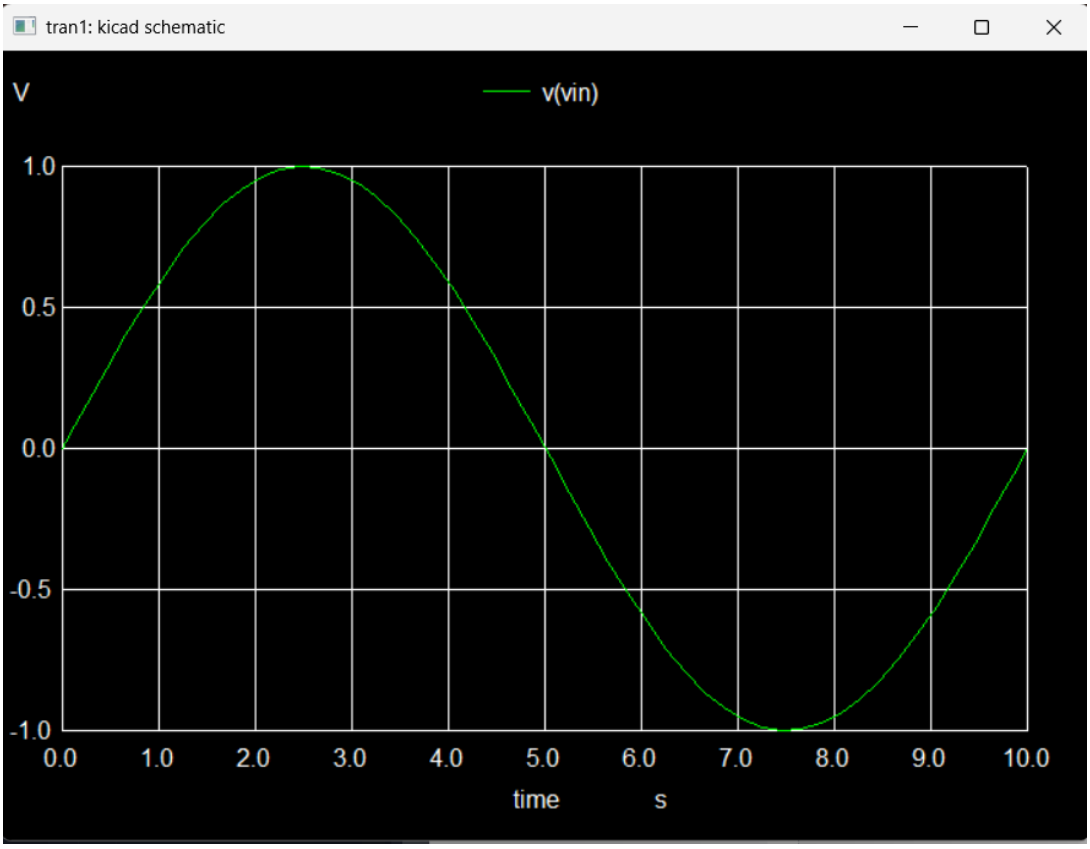


Figure 4.19: NgSpice plot of MC33171 (Input v(1) vs Output v(2))

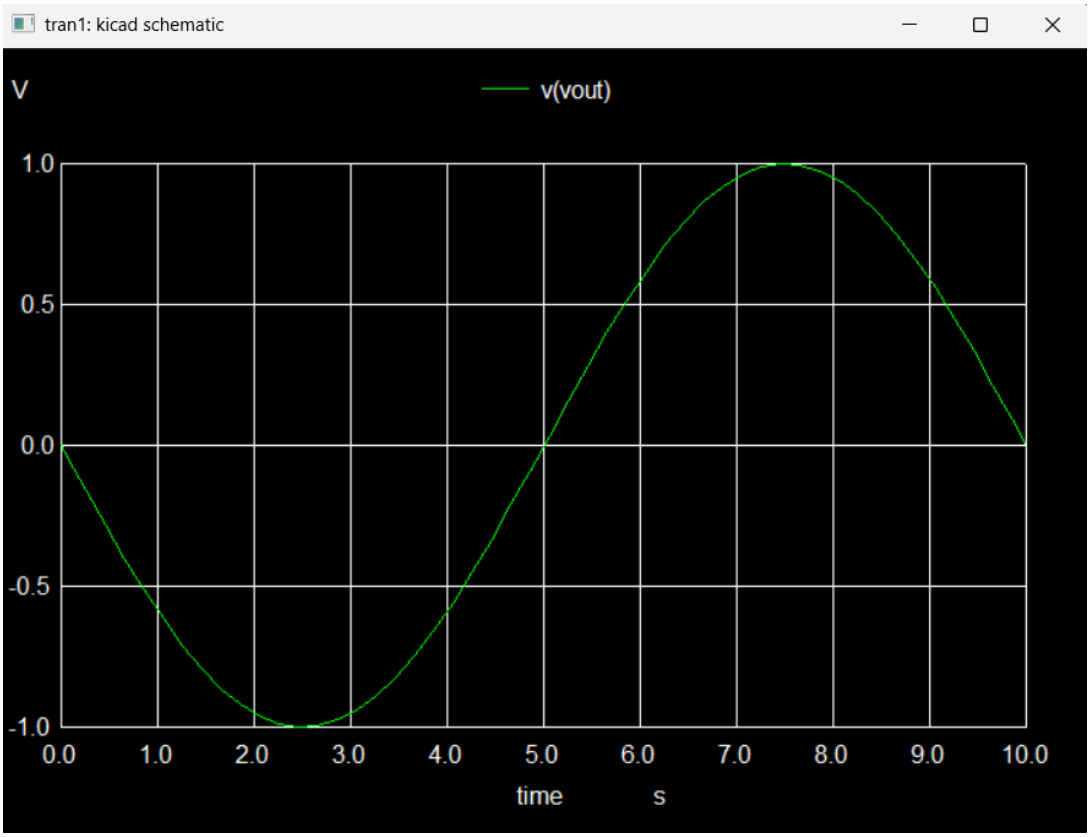


Figure 4.20: NgSpice plot of MC33171 (Input v(1) vs Output v(2))

4.4.7 NgSpice Plot Analysis

- **Input Signal:** The trace `v(1)` represents the applied sinusoidal input signal.
- **Output Response:** The trace `v(2)`, taken from the amplifier's output and fed back to the inverting input, overlays `v(1)` exactly in both amplitude and phase, confirming unity gain with no attenuation, amplification, or phase shift.
- **Conclusion:** The simulation confirms that the MC33171 subcircuit accurately reproduces the input signal at its output with unity gain and high fidelity, validating correct voltage-follower operation while operating at low supply current, consistent with its low-power design intent.

Chapter 5

Device Modelling

5.1 1N4007G: General Purpose Silicon Rectifier Diode

5.1.1 General Description

The 1N4007G is a general-purpose silicon rectifier diode belonging to the popular 1N400x series, and represents the highest reverse-voltage-rated member of the family. It is designed for standard rectification applications requiring high reverse voltage blocking capability along with moderate forward current handling. Housed in an axial-lead package, the 1N4007G is widely used due to its low cost, robustness, and availability, making it a staple component in linear power supplies, mains-frequency rectification, and general-purpose rectification circuits.

5.1.2 Typical Applications

- Half-wave and full-wave rectification in power supplies
- General-purpose diode switching
- Reverse polarity and surge protection
- Flyback/freewheeling diode in relay and motor driver circuits
- Battery charging circuits
- High reverse-voltage rectification in mains-operated equipment

5.1.3 SPICE Model Implementation

SPICE Model Parameters

Below is the SPICE model parameter list with their corresponding description, values, and units.

Table 5.1: SPICE Model Parameters of 1N4007G Silicon Rectifier Diode

Parameter	Description	Value	Unit
IS	Saturation current	5.000×10^{-13}	A
RS	Series resistance	4.200×10^{-2}	Ω
N	Emission coefficient	1.700	–
TT	Transit time	4.320×10^{-6}	s
CJO	Zero-bias junction capacitance	2.650×10^{-11}	F
M	Grading coefficient	3.330×10^{-1}	–
VJ	Junction potential	1.0	V
BV	Reverse breakdown voltage	1.000×10^{3}	V
IBV	Reverse breakdown current	5.000×10^{-6}	A

SPICE Model

The SPICE model for the 1N4007G Silicon Rectifier Diode is as follows:

```
.MODEL 1N4007G D( Is=5.000E-13 Rs=4.200E-02 N=1.700E+00 TT=4.320E-06
Cjo=2.650E-11 M=3.330E-01 Vj=1 Bv=1.000E+03 Ibv=5.000E-06 )
```

5.1.4 Device Model Characterization

The 1N4007G is a general-purpose rectifier diode optimized for standard-frequency rectification with a high reverse breakdown voltage rating. Its behaviour is analyzed through forward and reverse bias characteristics using standard diode current-voltage relationships.

Forward Bias Characteristics

In forward bias, the current through the diode follows the standard diode equation, including the effect of the series resistance R_S:

$$I = I_S \left(e^{\frac{q(V - IR_S)}{nkT}} - 1 \right)$$

where I_S is the saturation current, V is the forward voltage across the diode terminals, n is the emission coefficient, q is the electronic charge, k is Boltzmann's constant, and T is the absolute temperature.

With an emission coefficient of $n = 1.7$, slightly lower than that of the 1N4001, the 1N4007G exhibits a moderate turn-on voltage of approximately 0.6–0.7 V, typical of general-purpose silicon rectifiers. The series resistance R_S becomes significant at higher forward currents, causing the I–V curve to deviate from pure exponential behavior and approach a more linear slope.

The following circuit analyzes the forward bias behavior of the 1N4007G diode, illustrating how the diode current increases with applied forward voltage (V_F), following the diode's exponential conduction behavior.

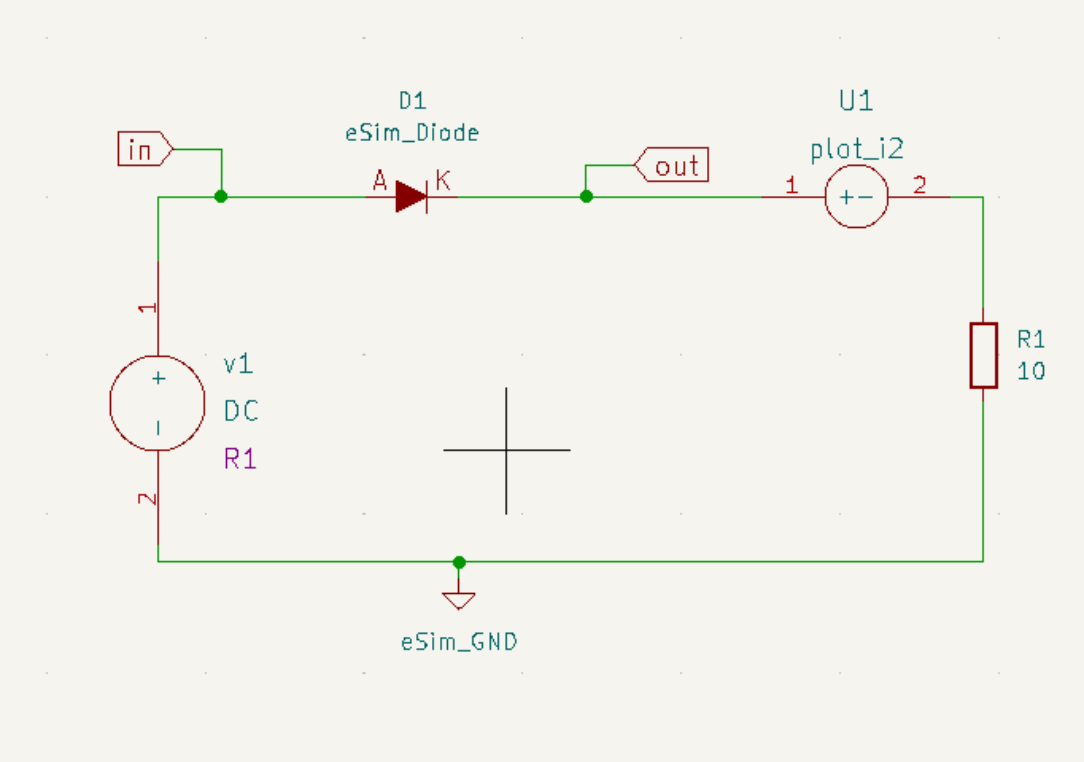


Figure 5.1: Forward bias circuit for 1N4007G diode

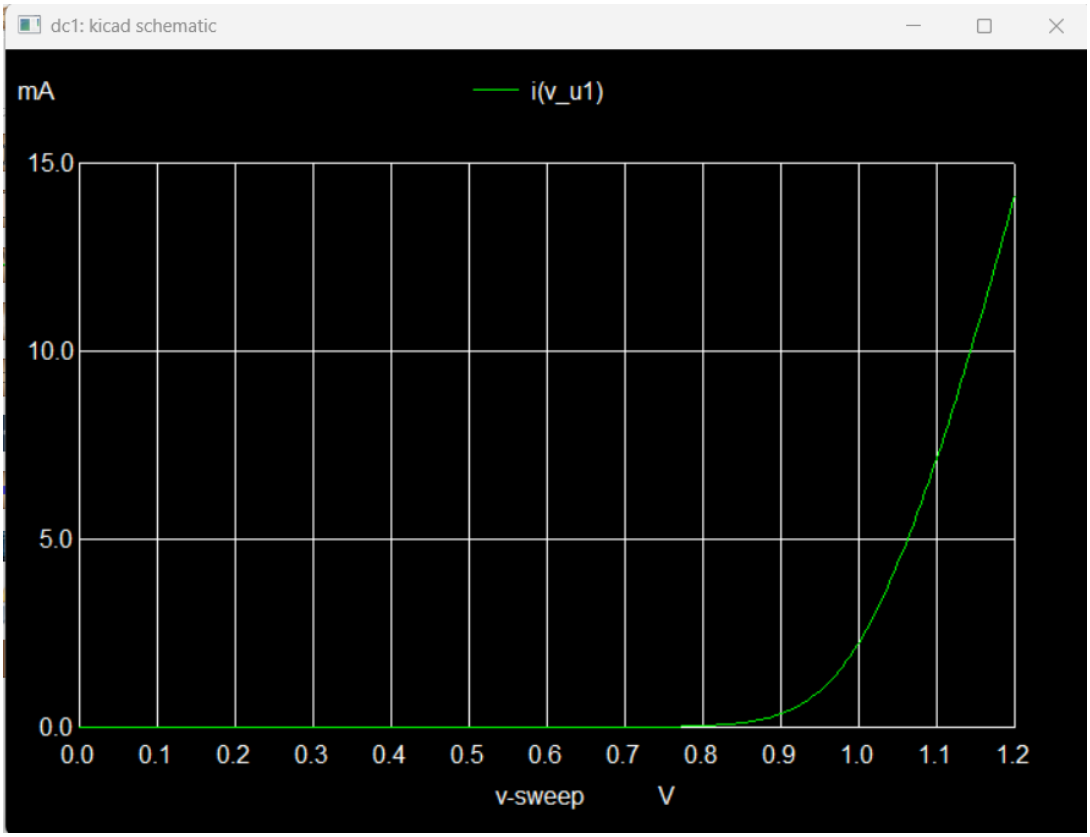


Figure 5.2: Forward bias NgSpice simulation for 1N4007G diode

Reverse Bias Characteristics

Under reverse bias, the diode conducts only a very small saturation (leakage) current until the reverse breakdown voltage (BV) is approached:

$$I \approx -I_S \quad for |V| < BV$$

Once the reverse voltage nears $BV = 1000\,\text{V}$, the current increases sharply, approaching the specified reverse breakdown current $I_{BV} = 5\,\mu\text{A}$. This high breakdown voltage rating makes the 1N4007G especially suitable for applications involving significant reverse voltage stress, such as mains-frequency rectification, more so than lower-rated members of the 1N400x family.

The reverse bias setup examines the leakage current and breakdown behavior of the 1N4007G diode. The circuit helps study its blocking capability and reverse leakage under increasing negative voltage.

Simulation shows minimal leakage current until breakdown, consistent with a standard PN-junction rectifier having a high reverse voltage rating.

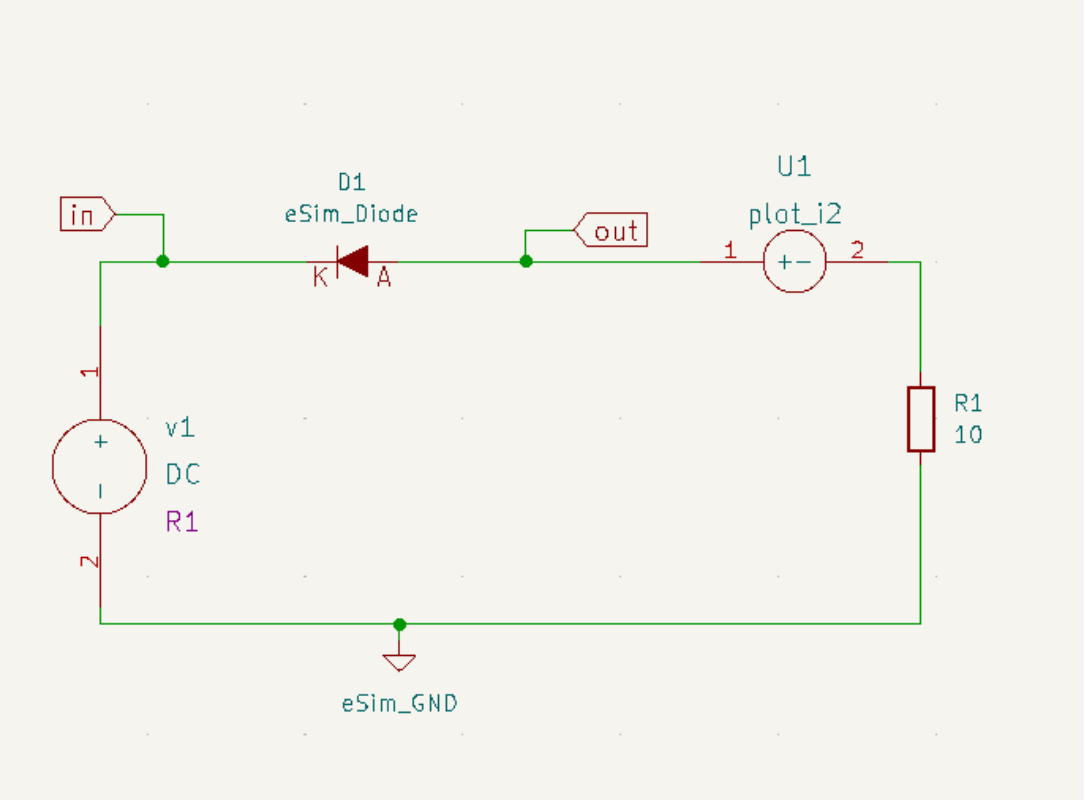


Figure 5.3: Reverse bias circuit for 1N4007G diode

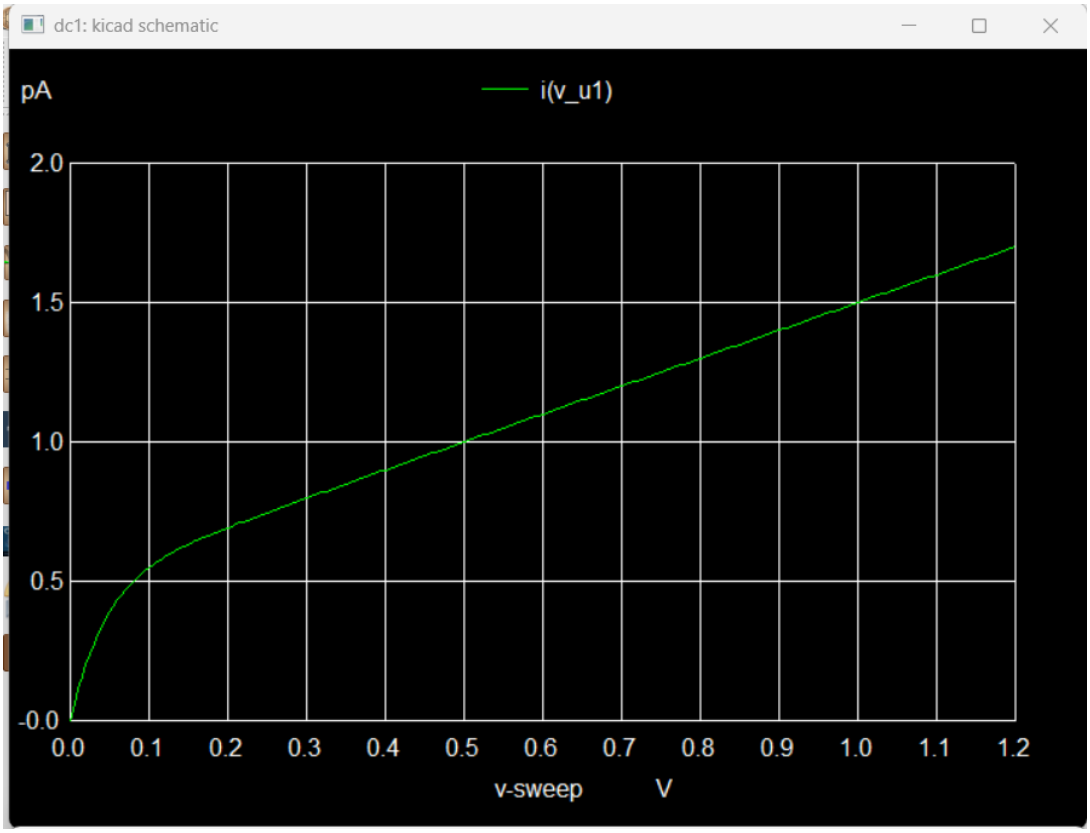


Figure 5.4: Reverse bias NgSpice simulation for 1N4007G diode

5.1.5 Application Circuit: Half Wave Rectifier

The 1N4007G is implemented in a half-wave rectifier configuration, where it conducts during the positive half-cycles of an AC signal and blocks during the negative half. Its high reverse breakdown voltage rating and adequate forward current handling make it well suited for use in conventional AC-to-DC power supply stages, battery chargers, and general-purpose rectification circuits – particularly where higher reverse voltage margins are desired compared to lower-voltage-rated diodes in the same family.

The 1N4007G is used in a basic half-wave rectifier configuration to demonstrate its rectification capability. The diode allows current only during the positive half-cycles of the AC input.

The simulation below displays the rectified output waveform, showing conduction during positive cycles and blocking during negative half-cycles.

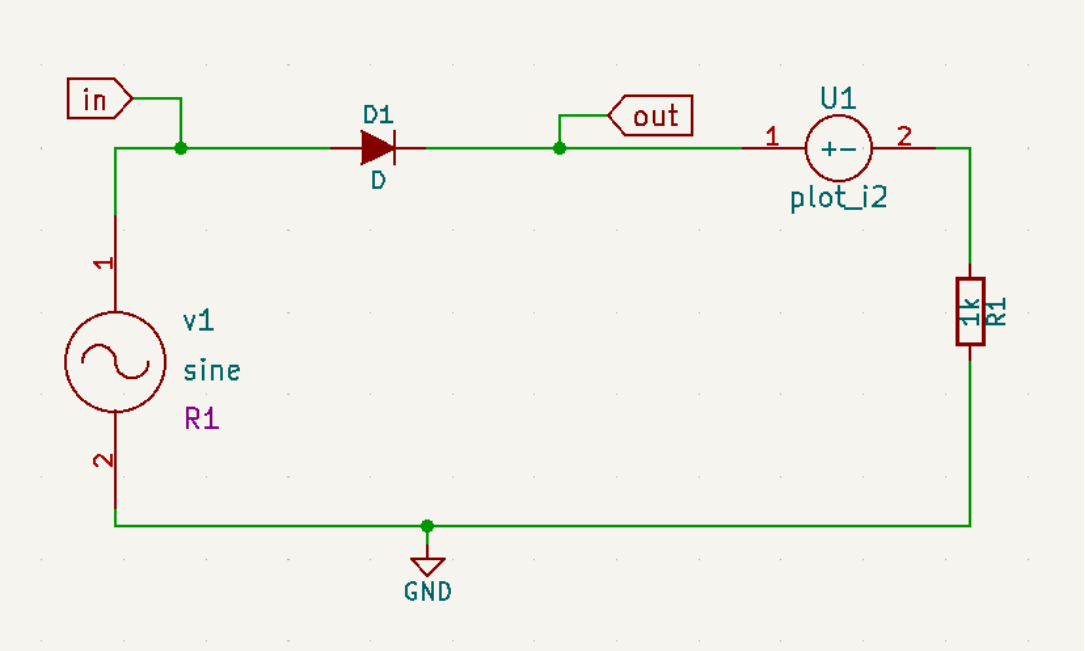


Figure 5.5: Half-wave rectifier circuit for 1N4007G diode

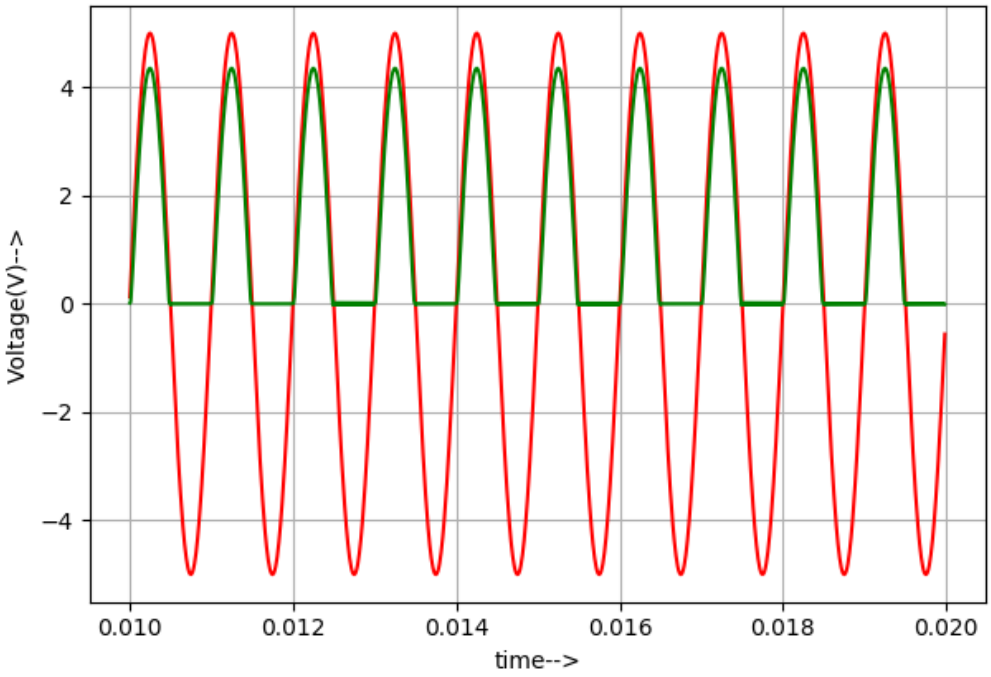


Figure 5.6: Half-wave rectifier NgSpice simulation for 1N4007G diode

5.2 Q2N3904: NPN General Purpose Bipolar Junction Transistor

5.2.1 General Description

The Q2N3904 is a widely used **NPN general-purpose bipolar junction transistor (BJT)**, valued for its low cost, availability, and well-characterized SPICE model. It is designed for small-signal amplification and general-purpose switching applications, offering moderate current gain, adequate frequency response, and low saturation voltage. Its versatility and predictable behavior across bias conditions make it a standard choice for analog amplifier design, biasing experiments, and small-signal frequency response studies in both academic and practical circuit design.

5.2.2 Typical Applications

- Small-signal audio and general-purpose amplification
- Common-Emitter (CE), Common-Base (CB), and Common-Collector amplifier stages
- Biasing network design and stabilization studies
- Switching applications in digital and driver circuits
- Frequency response and bandwidth characterization of amplifier stages
- General-purpose signal conditioning in low-power analog circuits

5.2.3 SPICE Model Implementation

Original SPICE Model Parameters

The table below lists the original 27-parameter Gummel-Poon model obtained from the standard device library.

Table 5.2: Original SPICE Model Parameters of Q2N3904 NPN BJT

Param	Description	Value	Param	Description
IS	Saturation current	14.34f	NC	B-C leakage emission coeff.
XTI	Saturation current temp. exp.	3	ISC	B-C leakage saturation current
EG	Energy gap	1.11	IKR	Corner current, reverse beta roll-o
VAF	Forward Early voltage	120	RC	Collector resistance
BF	Ideal max. forward beta	200	CJC	B-C zero-bias junction cap.
NE	B-E leakage emission coeff.	1.307	MJC	B-C grading coefficient
ISE	B-E leakage saturation current	14.34f	VJC	B-C built-in potential
IKF	Corner current, forward beta roll-off	.2847	FC	Forward-bias depletion capacitanc
XTB	Forward/reverse beta temp. exp.	1.5	CJE	B-E zero-bias junction cap.
BR	Ideal max. reverse beta	6.092	MJE	B-E grading coefficient
			VJE	B-E built-in potential
			TR	Ideal reverse transit time
			TF	Ideal forward transit time
			ITF	High-current transit time effect
			VTF	Transit time voltage dependency
			XTF	Transit time bias dependency coef
			RB	Base resistance

Modified (Optimized) SPICE Model Parameters

To better align the simulated device behavior with the target operating characteristics observed during testing, five parameters were refined and one new parameter (**RE**) was introduced, extending the model to 28 parameters.

Table 5.3: Modified SPICE Model Parameters of Q2N3904 NPN BJT

Parameter	Original	Modified	Change	Justification
BF	200	**350**	↑	Increased forward current gain (β), improving ampl
IKF	.2847	**0.07**	↓	Lowered corner current, causing beta roll-off to beg
CJE	15p	**9.5p**	↓	Reduced B-E junction capacitance, improving high-
TR	46.91n	**120n**	↑	Increased reverse transit time, affecting turn-off/sto
RE	—	**0.5**	added	Introduced emitter ohmic (bulk) resistance, previou

All remaining parameters (IS, XTI, EG, NE, ISE, XTB, BR, NC, ISC, IKR, RC, CJC, MJC, VJC, FC, MJE, VJE, TF, ITF, VTF, XTF, RB) were retained unchanged from the original model.

Updated SPICE Model

The modified 28-parameter SPICE model for the Q2N3904 NPN transistor is as follows:

```
.MODEL Q2N3904 NPN( IS=14.34E-15 XTI=3 EG=1.11 VAF=120 BF=350
NE=1.307 ISE=14.34E-15 IKF=0.07 XTB=1.5 BR=6.092 NC=2 ISC=0
IKR=0 RC=1 CJC=7.306E-12 MJC=0.3416 VJC=0.75 FC=0.5 CJE=9.5E-12
MJE=0.377 VJE=0.75 TR=120E-9 TF=411.1E-12 ITF=0.6 VTF=1.7 XTF=3
RB=10 RE=0.5 )
```

5.2.4 Device Model Characterization

The Q2N3904, using the optimized 28-parameter model above, is characterized across five distinct test configurations, covering its biasing behavior, amplifier gain characteristics in different configurations, and frequency response. Each test isolates a specific aspect of transistor operation relevant to analog amplifier design.

Test 1: Biasing Circuit

The biasing circuit establishes a stable DC operating (quiescent) point for the transistor using a voltage-divider bias network, ensuring it remains in the active region across expected signal swings and temperature variation. A DC Operating Point (`.op`) analysis is used to verify the base, emitter, and collector voltages, along with the quiescent collector current, against the designed bias network values.

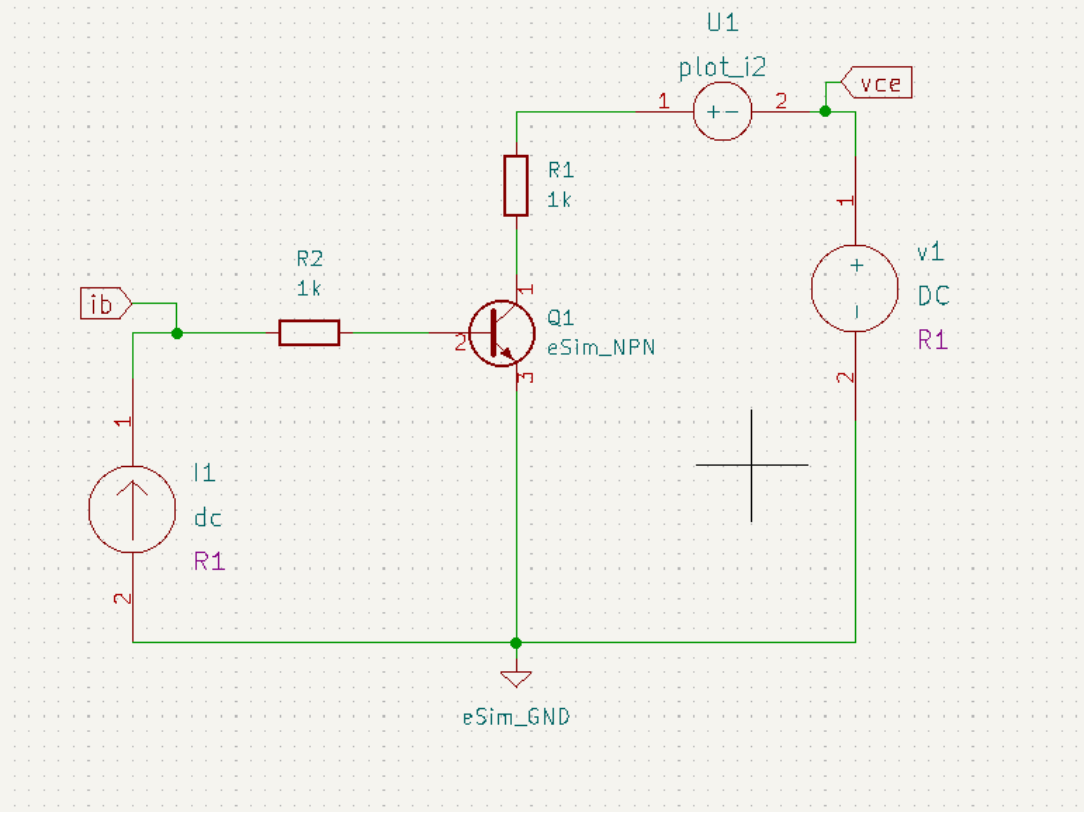


Figure 5.7: Biasing circuit for Q2N3904

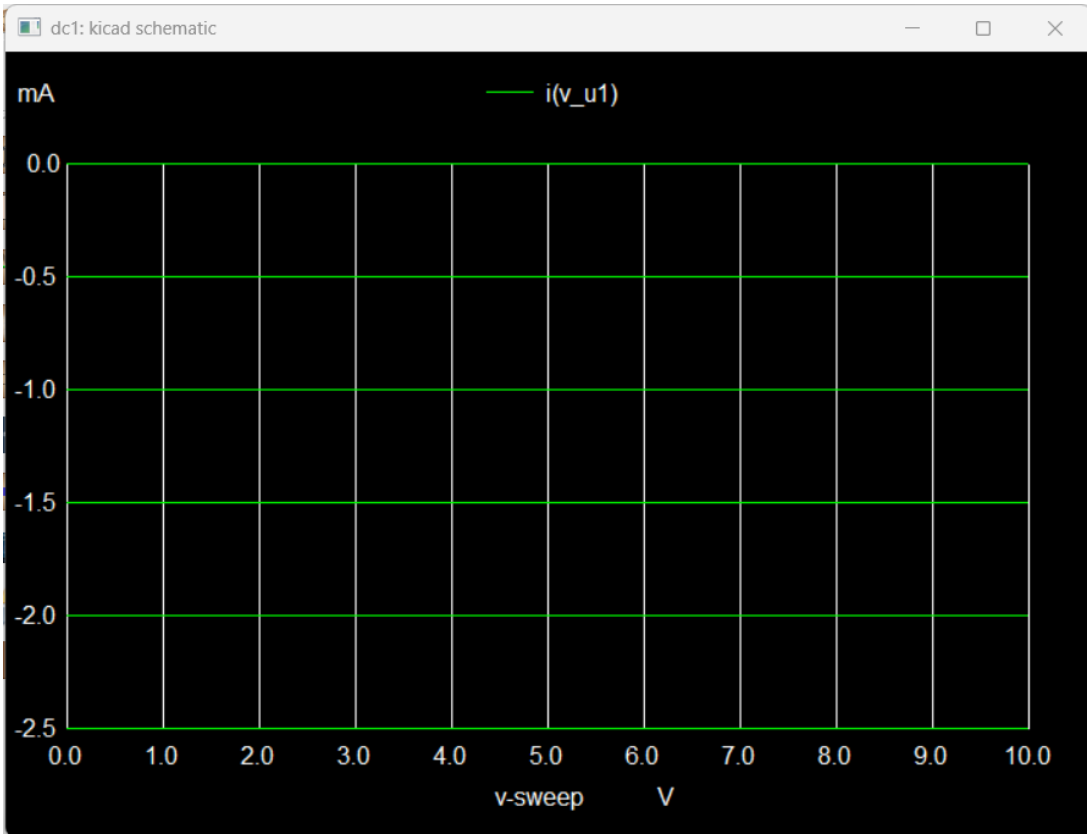


Figure 5.8: NgSpice DC operating point result for Q2N3904 biasing circuit

Test 2: BJT Amplifier

This test evaluates the transistor operating as a complete single-stage RC-coupled amplifier with voltage-divider bias, emitter degeneration, and an emitter bypass capacitor. A DC supply of $V_1 = 12\,V$ was used, with the bias network sized to place the quiescent collector-emitter voltage V_{CE} near the midpoint of the supply rail for maximum symmetric output swing. An AC input signal of **10–15 mV peak amplitude at 1 kHz** was applied, chosen conservatively below the stage's estimated gain-limited linear range to avoid output clipping. The DC operating point was verified first using `.op`, followed by a `.tran` simulation to observe the amplified waveform.

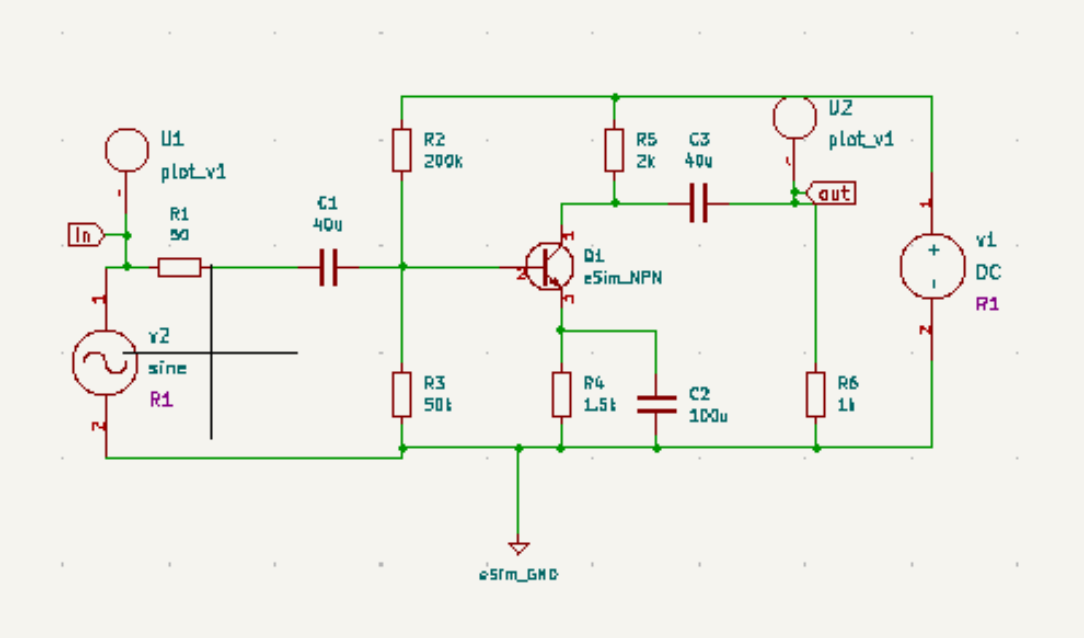


Figure 5.9: Amplifier circuit for Q2N3904

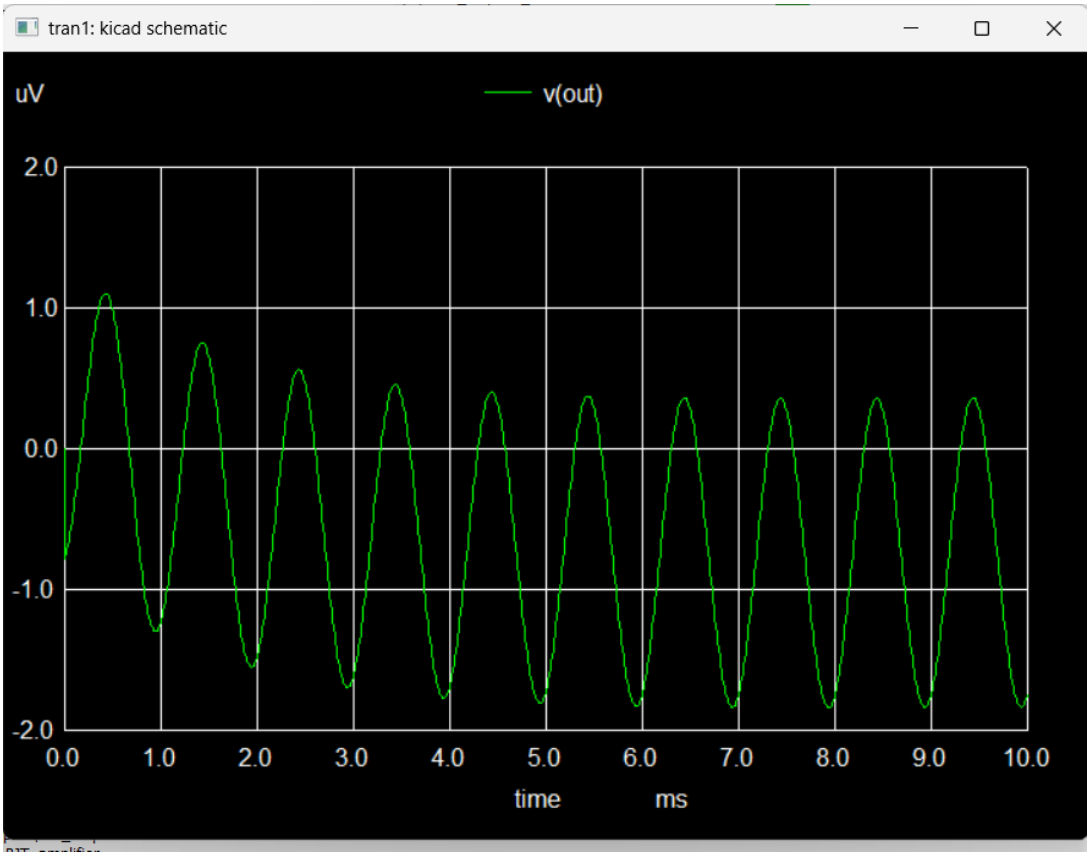


Figure 5.10: Input waveform for Q2N3904 amplifier

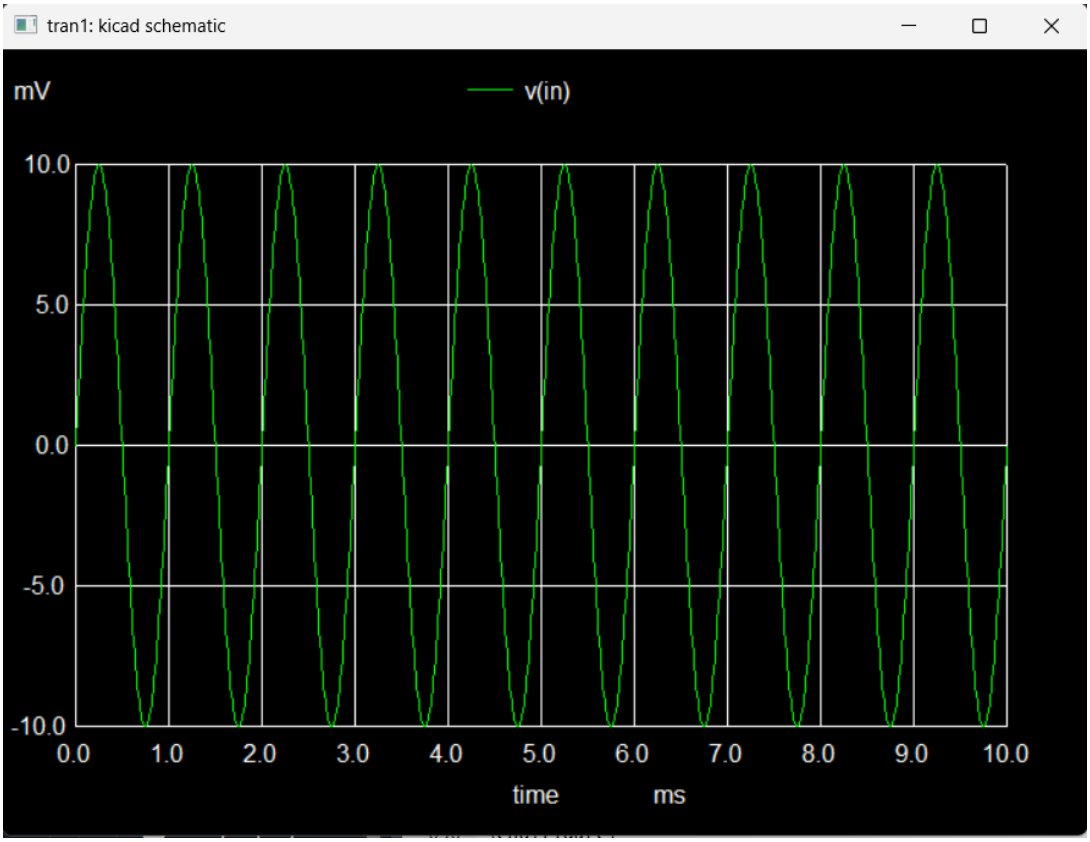


Figure 5.11: Output waveform for Q2N3904 amplifier

Test 3: Frequency Response

The frequency response test characterizes the amplifier's gain behavior across a swept frequency range using an `.ac` analysis, identifying the lower and upper cutoff (-3 dB) frequencies and the resulting bandwidth. This test reveals the effect of the modified junction capacitances (C_{JE}, C_{JC}) and the coupling/bypass capacitors on the amplifier's usable frequency range.

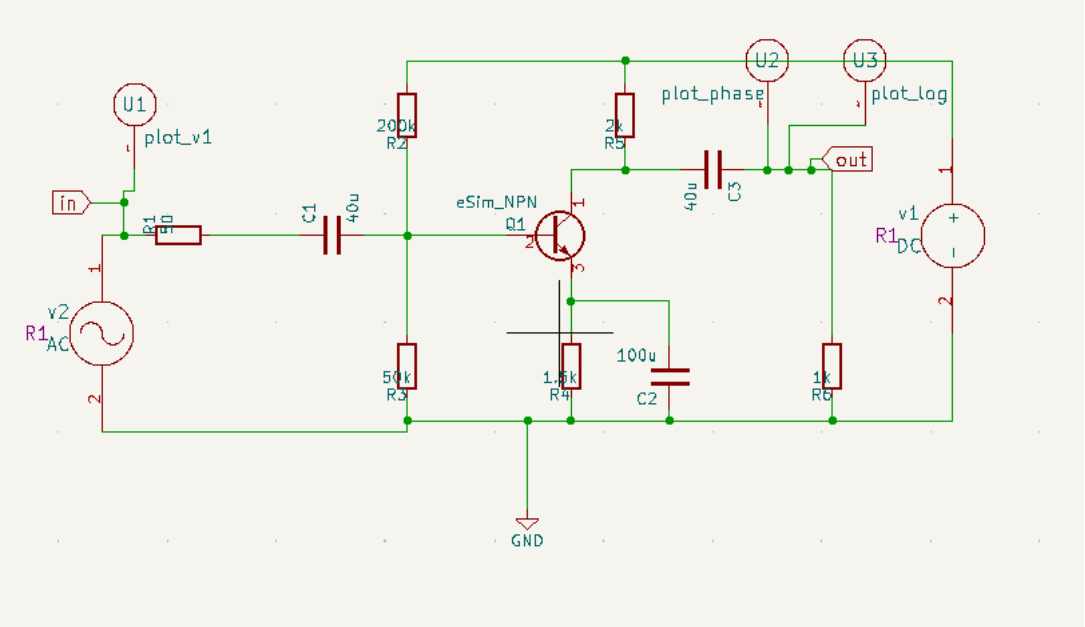


Figure 5.12: Frequency response test circuit for Q2N3904

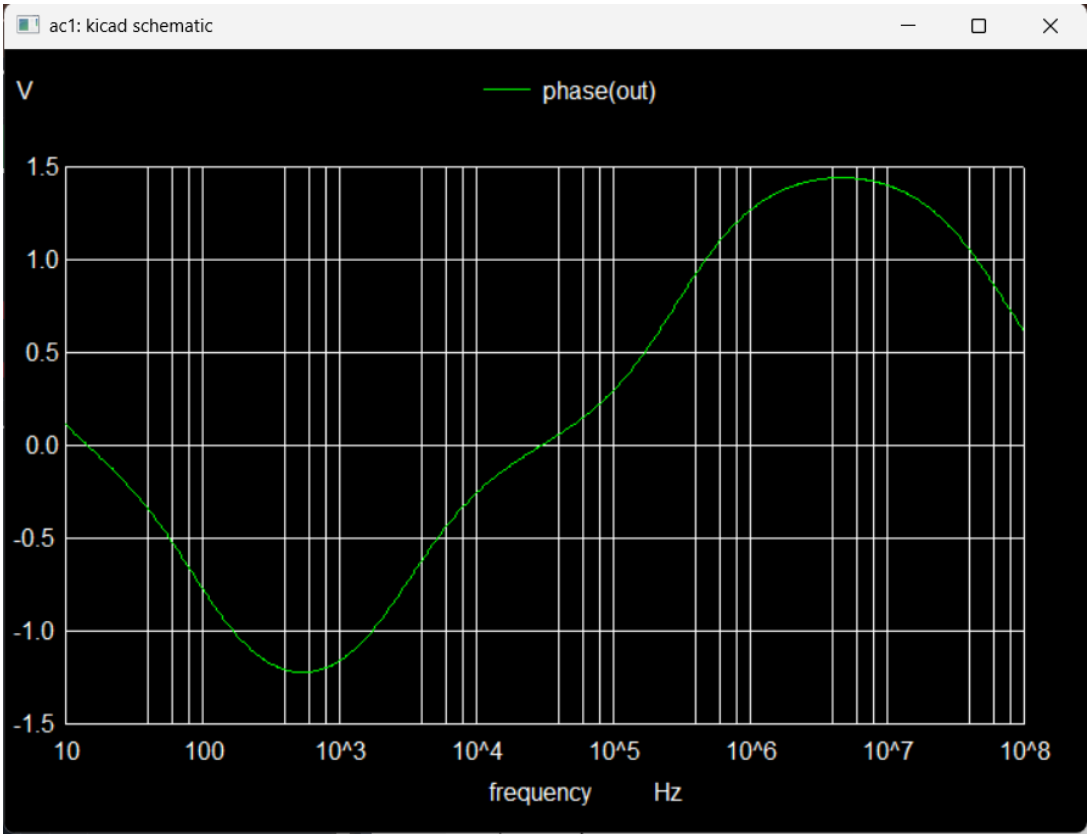


Figure 5.13: Phase Response for Q2N3904 frequency response test

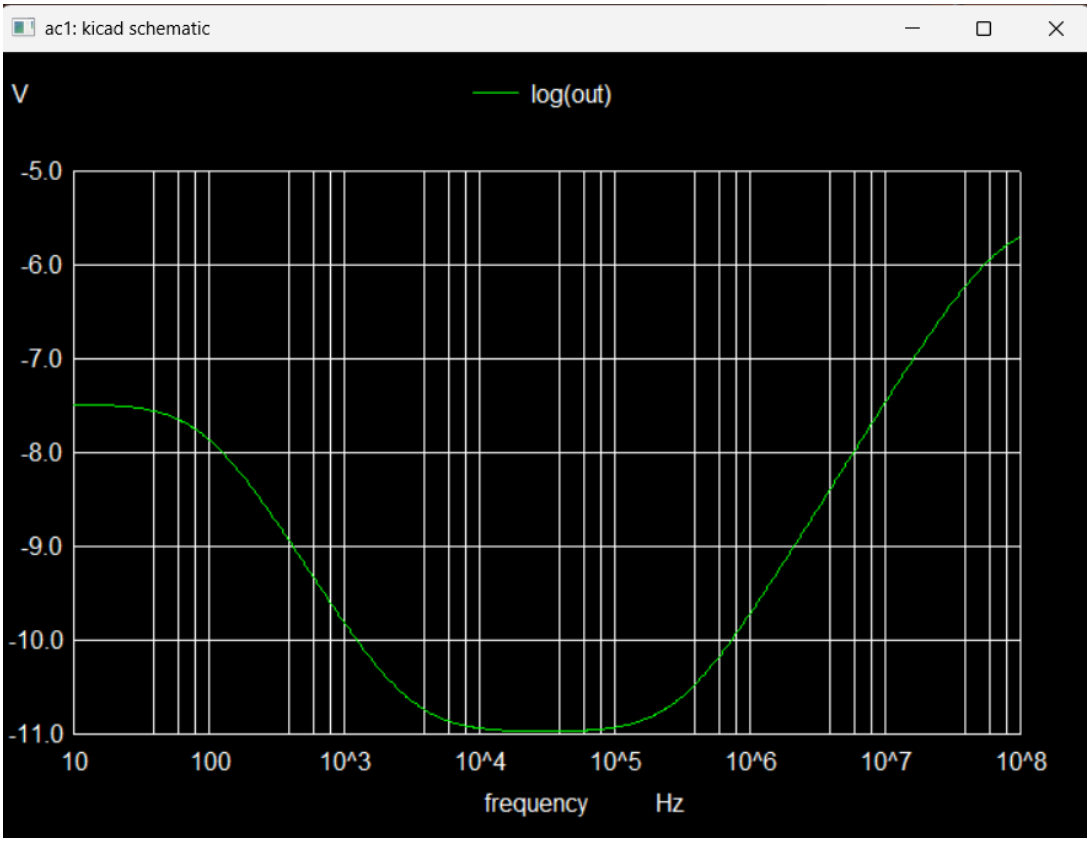


Figure 5.14: Frequency response (gain vs frequency) output for Q2N3904

5.3 Q2N3906: PNP General Purpose Bipolar Junction Transistor

5.3.1 General Description

The Q2N3906 is a widely used **PNP general-purpose bipolar junction transistor (BJT)**, complementary to the NPN Q2N3904 and valued for its low cost, availability, and well-characterized SPICE model. It is designed for small-signal amplification and general-purpose switching applications, offering moderate current gain, adequate frequency response, and low saturation voltage. Its predictable behavior across bias conditions, combined with its complementary relationship to the 2N3904, makes it a standard choice for push-pull output stages, complementary amplifier topologies, and biasing experiments in both academic and practical circuit design.

5.3.2 Typical Applications

- Small-signal audio and general-purpose amplification
- Common-Emitter (CE), Common-Base (CB), and Common-Collector amplifier stages using PNP topology
- Complementary (push-pull) output stages paired with NPN devices such as the Q2N3904
- Biasing network design and stabilization studies
- Switching applications in digital and driver circuits
- Frequency response and bandwidth characterization of amplifier stages
- General-purpose signal conditioning in low-power analog circuits

5.3.3 SPICE Model Implementation

Original SPICE Model Parameters

The table below lists the original 27-parameter Gummel-Poon model obtained from the standard PNP device library.

Table 5.4: Original SPICE Model Parameters of Q2N3906 PNP BJT

Param	Description	Value	Param	Description
IS	Saturation current	650.6E-18	NC	B-C leakage emission coeff.
XTI	Saturation current temp. exp.	3	ISC	B-C leakage saturation current
EG	Energy gap	1.11	IKR	Corner current, reverse beta ro
VAF	Forward Early voltage	115.7	RC	Collector resistance
BF	Ideal max. forward beta	231.7	CJC	B-C zero-bias junction cap.
NE	B-E leakage emission coeff.	1.829	MJC	B-C grading coefficient
ISE	B-E leakage saturation current	54.81f	VJC	B-C built-in potential
IKF	Corner current, forward beta roll-off	1.079	FC	Forward-bias depletion capacit
XTB	Forward/reverse beta temp. exp.	1.5	CJE	B-E zero-bias junction cap.
BR	Ideal max. reverse beta	3.563	MJE	B-E grading coefficient
			VJE	B-E built-in potential
			TR	Ideal reverse transit time
			TF	Ideal forward transit time
			ITF	High-current transit time effec
			VTF	Transit time voltage dependen
			XTF	Transit time bias dependency
			RB	Base resistance

Modified (Optimized) SPICE Model Parameters

To align the simulated device behavior with datasheet-specified characteristics (Motorola 2N3905/2N3906 electrical characteristics table), five parameters were refined and one new parameter (**RE**) was introduced, extending the model to 28 parameters.

Table 5.5: Modified SPICE Model Parameters of Q2N3906 PNP BJT

Parameter	Original	Modified	Change	Justification
BF	231.7	**370**	↑	Raised ideal forward beta above the datasheet-speci
IKF	1.079	**0.08**	↓	Original corner current (>1 A) was non-physical for
CJC	14.76p	**4.3p**	↓	Reduced B-C junction capacitance to match datash
CJE	19.82p	**9.8p**	↓	Reduced B-E junction capacitance to match datash
TR	111.3n	**150n**	↑	Increased reverse transit time to better match datas
RE	—	**0.5**	added	Introduced emitter ohmic (bulk) resistance, previou

All remaining parameters (IS, XTI, EG, VAF, NE, ISE, XTB, BR, NC, ISC, IKR, RC, MJC, VJC, FC, MJE, VJE, TF, ITF, VTF, XTF, RB) were retained unchanged from the original model.

Updated SPICE Model

The modified 28-parameter SPICE model for the Q2N3906 PNP transistor is as follows:

```
.MODEL Q2N3906 PNP( IS=650.6E-18 XTI=3 EG=1.11 VAF=115.7 BF=370
NE=1.829 ISE=54.81E-15 IKF=0.08 XTB=1.5 BR=3.563 NC=2 ISC=0
IKR=0 RC=0.715 CJC=4.3E-12 MJC=0.5383 VJC=0.75 FC=0.5 CJE=9.8E-12
MJE=0.3357 VJE=0.75 TR=150E-9 TF=603.7E-12 ITF=0.65 VTF=5 XTF=1.7
RB=10 RE=0.5 )
```

5.3.4 Device Model Characterization

The Q2N3906, using the optimized 28-parameter model above, is characterized across five distinct test configurations, covering its biasing behavior, amplifier gain characteristics, and frequency response. Each test isolates a specific aspect of PNP transistor operation relevant to analog amplifier design. Unlike the NPN Q2N3904, all supply polarities and current directions are reversed: the emitter is referenced to the positive supply rail, the collector is referenced toward ground, and base current flows out of the base terminal rather than into it.

Test 1: BJT Amplifier

This test evaluates the transistor operating as a complete single-stage RC-coupled common-emitter amplifier with voltage-divider bias, emitter degeneration, and an emitter bypass capacitor. Relative to the NPN amplifier topology, the emitter resistor R_4 is connected to the V_{CC} rail rather than ground, and the collector resistor R_5 is connected to ground rather than V_{CC}, reflecting the reversed current flow direction of the PNP device. A DC supply of $V_1 = 12\,V$ was used, with the bias network sized to place the quiescent collector-emitter voltage V_{CE} near the midpoint of the supply rail for maximum symmetric output swing. An AC input signal of **10–15 mV peak amplitude at 1 kHz** was applied, chosen conservatively below the stage's estimated gain-limited linear range to avoid output clipping. The DC operating point was verified first using `.op`, followed by a `.tran` simulation to observe the amplified waveform.

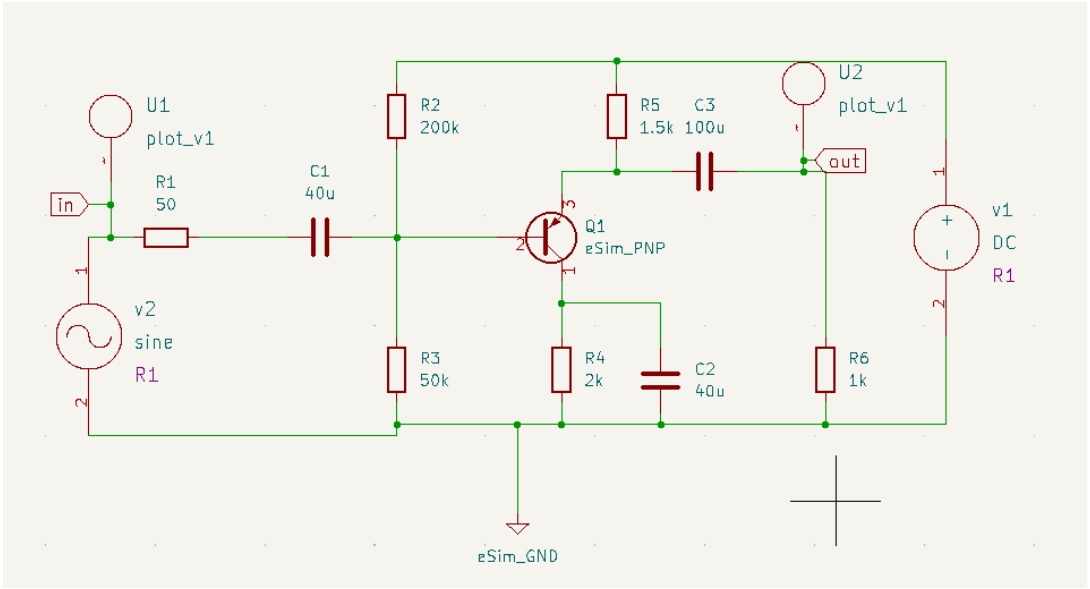


Figure 5.15: Amplifier circuit for Q2N3906

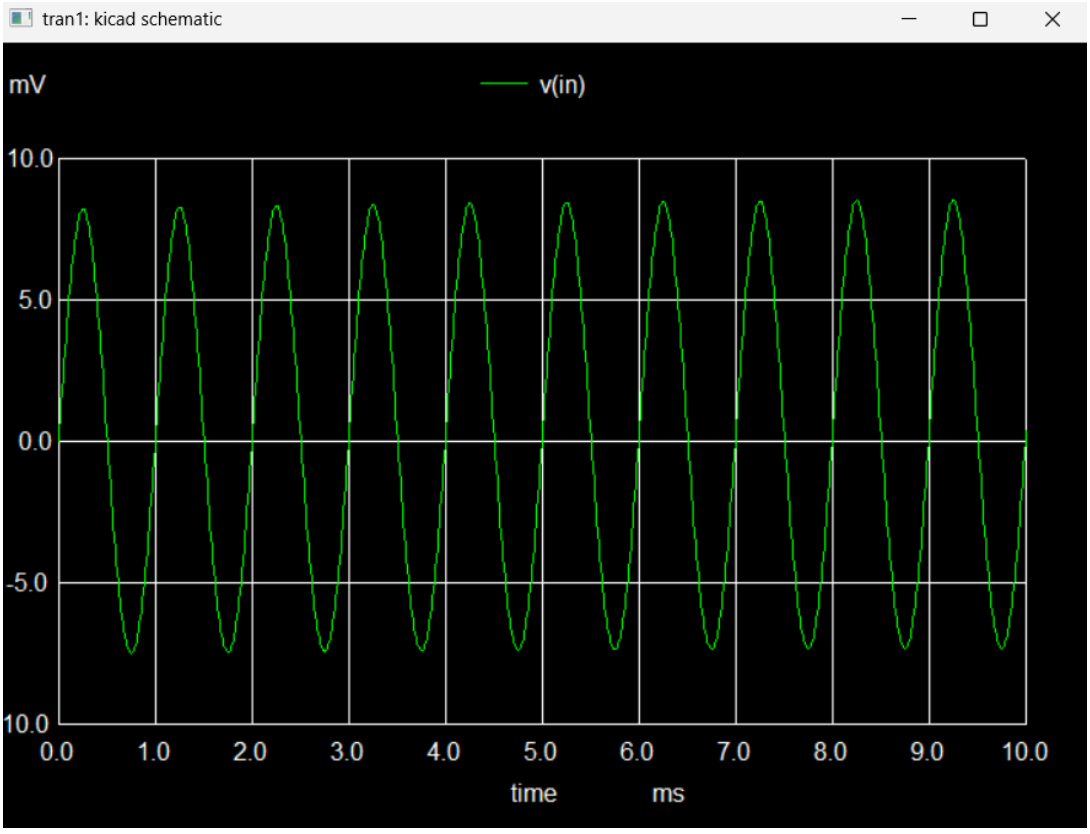


Figure 5.16: Input waveform for Q2N3906 amplifier

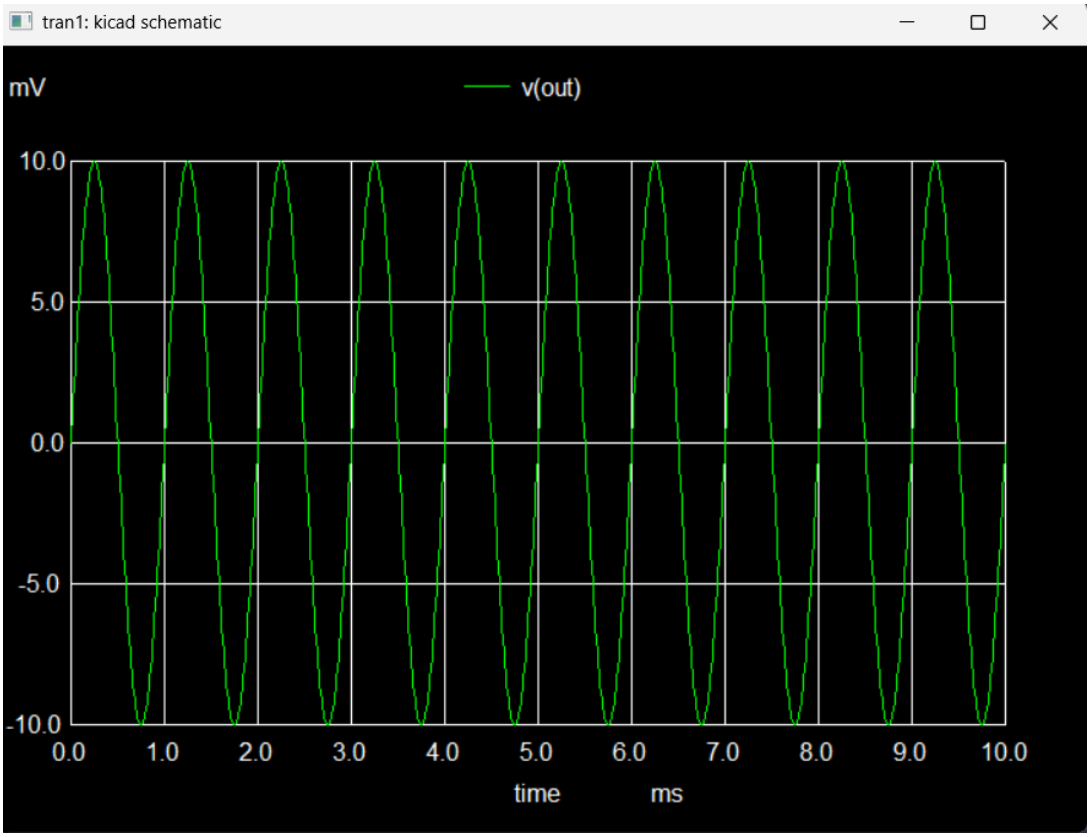


Figure 5.17: Output waveform for Q2N3906 amplifier

Test 3: Frequency Response

The frequency response test characterizes the amplifier's gain behavior across a swept frequency range using an `.ac` analysis, identifying the lower and upper cutoff (-3 dB) frequencies and the resulting bandwidth. This test reveals the effect of the modified junction capacitances (C_{JE}, C_{JC}) and the coupling/bypass capacitors on the amplifier's usable frequency range, and is expected to show a slightly lower upper cutoff frequency than the Q2N3904 amplifier, consistent with the Q2N3906's lower datasheet-specified f_T (250 MHz min vs. 300 MHz min for the 2N3904).

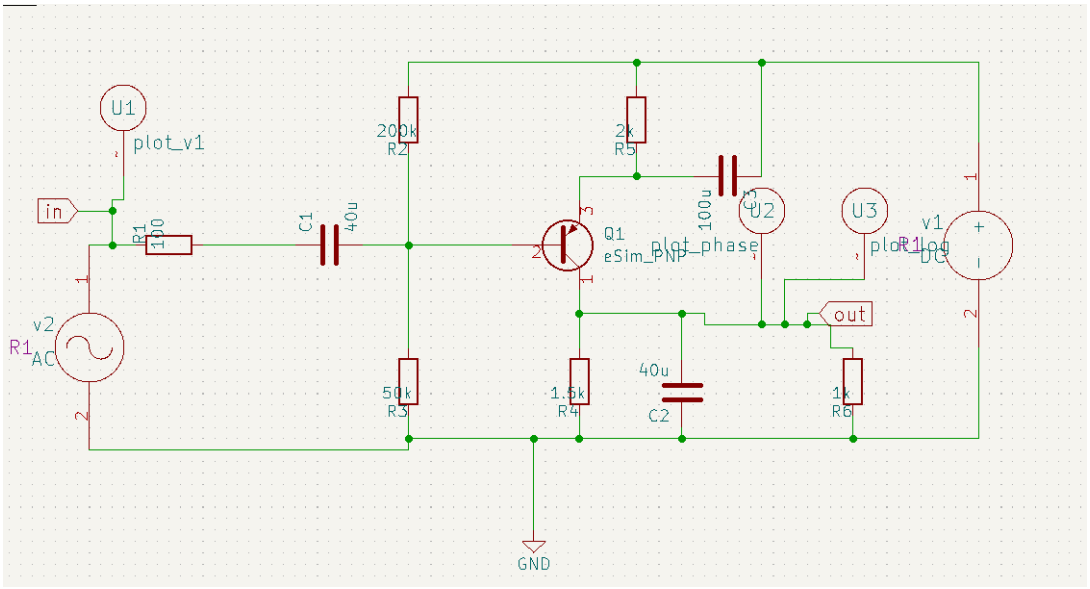


Figure 5.18: Frequency response test circuit for Q2N3906

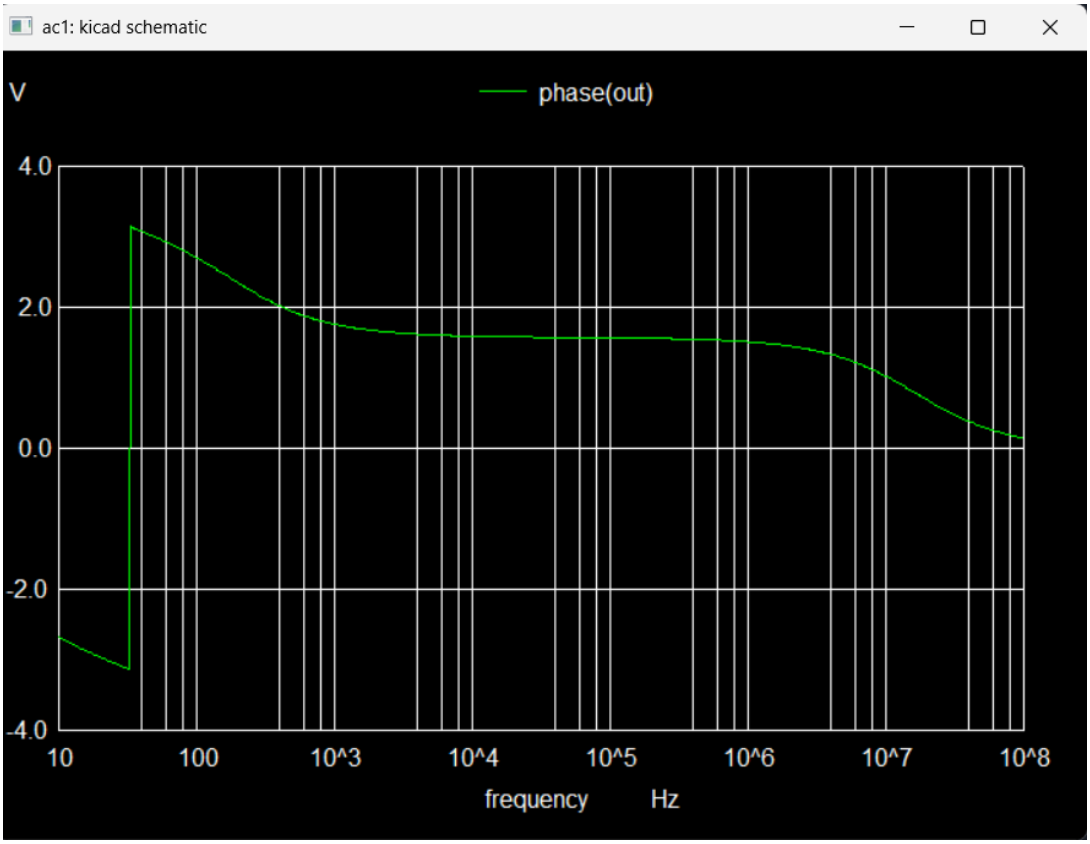


Figure 5.19: Phase Response for Q2N3906 frequency response test

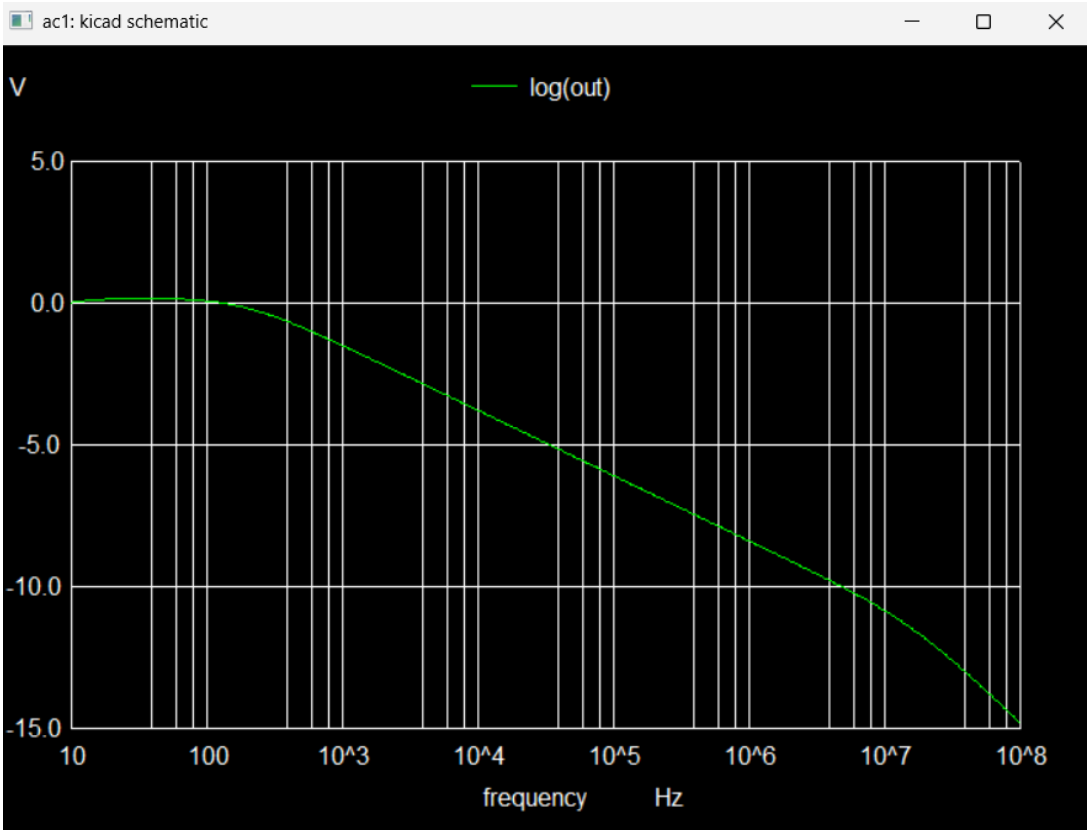


Figure 5.20: Frequency response (gain vs frequency) output for Q2N3906

Chapter 6

Conclusion and Future Scope

We were able to achieve the target of designing and developing various Analog and Digital Integrated Circuits for the eSim library (Subcircuits). IC Subcircuits are designed and also verified based on specifications given in official datasheets. The inclusion of these models in the eSim library will significantly enhance the tool's capabilities, enabling users to easily incorporate these fundamental ICs into their own projects and circuit designs.

Looking ahead, this project sets the foundation for the continued expansion of eSim's device model library. We anticipate that more ready-to-use IC models will be developed, broadening the scope of available components and further empowering the eSim community.

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