Summer Fellowship Report

On

Subcircuit Design using eSim

Submitted by

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Acknowledgement

I take this opportunity to express my heartfelt gratitude to the FOSSEE team at IIT Bombay for granting me the wonderful chance to work on the design and integration of multiple subcircuits in eSim. This experience has offered me invaluable insights into open-source EDA tools for circuit simulation and their practical applications.

I am deeply thankful to Prof. Kannan Moudgalya and the FOSSEE team for placing their trust in me and allowing me to contribute to this meaningful project.

I would also like to thank the entire eSim team for providing a platform that encouraged learning and relearning, and for their consistent guidance and support throughout the journey.

I am especially grateful to my mentors, Mr. Sumanto Kar and Mr. Varad Patil, for their continuous support, knowledge sharing, and for making this fellowship a truly enriching experience.

A special word of thanks goes to Prof. Inderjit Singh Dhanjal, whose mentorship offered me valuable perspectives on the design and implementation of integrated circuits.

Finally, I extend my sincere thanks to my family and friends for their constant encouragement and support throughout this journey.

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Chapter 1

Introduction

FOSSEE which stands for Free/Libre and Open Source Software for Education is an organization, based at IIT Bombay, as a remarkable initiative aimed at promoting the use of open-source software in education and research. It was established with the mission to reduce the dependency on proprietary software and to encourage the adoption of open-source alternatives. FOSSEE offers a wide range of tools and resources that cater to various academic and professional needs.

It provides comprehensive documentation, tutorials, workshops, and hands-on training sessions, for empowering students, educators, and professionals to leverage opensource software for their projects and coursework. The organization's commitment to fostering a collaborative and inclusive environment has significantly contributed to the democratization of technology and has opened up new avenues for innovation and learning. FOSSEE which stands for Free/Libre and Open Source Software for Education is an organization, based at IIT Bombay, as a remarkable initiative aimed at promoting the use of open-source software in education and research.

1.1 eSim

eSim, created by the FOSSEE project at IIT Bombay, is a versatile open-source software tool for circuit design and simulation. It combines various open-source software packages into one cohesive platform, making it easier to design, simulate, and analyze electronic circuits. This tool is particularly useful for students, educators, and professionals who need an affordable and accessible alternative to proprietary software.

eSim offers features for schematic creation, circuit simulation, and PCB design, and includes an extensive library of components. The Subcircuit feature is a significant enhancement, enabling users to design complex circuits by integrating simpler subcircuits. Through eSim, FOSSEE promotes the use of open-source solutions in engineering education and professional fields, encouraging innovation and collaboration.

1.2 NgSpice

NgSpice is an open-source SPICE simulator for electric and electronic circuits. It can simulate various circuit elements, including JFETs, bipolar and MOS transistors, passive elements (R, L, C), diodes and other devices, all interconnected in a netlist.

Digital circuits are also simulated, ranging from single gates to complex circuits, including combinations of analog, digital, and mixed-signal circuits. NgSpice offers a wealth of device models for active, passive, analog, and digital elements. Users input their circuits as netlists, and the output is one or more graphs of currents, voltages, and other electrical quantities, or saved in a data file.

Chapter 2

Features of eSim

The objective behind the development of eSim is to provide an open source EDA solution for electronics and electrical engineers. The software should be capable of performing schematic creation, PCB design and circuit simulation (analog, digital and mixed-signal). It should provide facilities to create new models and components. Thus, eSim offers the following features -

1. **Schematic Creation:** eSim provides an easy-to-use graphical interface for drawing circuit schematics, making it accessible for users of all levels. Users can drag and drop components from the library onto the schematic, simplifying the design process. Comprehensive editing tools allow for easy modification of schematics, including moving, rotating, and labeling components

2. **Circuit Simulation:** eSim supports SPICE (Simulation Program with Integrated Circuit Emphasis), a standard for simulating analog and digital circuits. Users can perform various types of analysis such as transient, AC, and DC, providing insights into circuit behavior over time and frequency.An integrated waveform viewer helps visualize simulation results, aiding in the analysis and debugging of circuit designs.

3. **PCB Design:** The PCB layout editor allows users to place components and route traces with precision. eSim includes DRC (Design Rule Check) capabilities to ensure that the PCB design adheres to manufacturing constraints and electrical rules. Users can generate Gerber files, which are standard for PCB fabrication, directly from their designs.

4. **Subcircuit Feature:** This feature enables users to create complex circuits by integrating smaller, simpler subcircuits, promoting modular and hierarchical design approaches. Subcircuits can be reused in different projects, saving time and effort in redesigning common circuit elements.

5. **Open Source Integration:** eSim integrates several open-source tools like KiCad, Ngspice, and GHDL, providing a comprehensive suite for electronic design automation. Being open-source, eSim is free to use, making advanced circuit design tools accessible without the need for expensive licenses.

Chapter 3

Problem Statement

To design and develop various Analog and Digital Integrated Circuit Models in the form of sub-circuits using device model files already present in the eSim library. These IC models should be useful in the future for circuit designing purposes by developers and users, once they get successfully integrated into the eSim subcircuit Library..

3.1 Approach

Our approach to implementing the problem statement began with examining datasheets from prominent Integrated Circuit (IC) manufacturers such as Texas Instruments, Analog Devices, and NXP Semiconductors. we selected ICs that offer a diverse range of functionalities, including precision amplifiers, comparators, encoders, and audio amplifiers. After building the subcircuits, we tested them to verify basic circuit configurations using NgSpice simulations. The step-by-step roadmap of this process is outlined below :

1. **Analyzing Datasheets:**
   The primary step is to browse through various analog and digital IC datasheets, and hence find suitable circuits to implement in eSim, that are not previously included into the eSim library. Check for the detailed schematic of the IC's and once the component values and the truth table is ascertained, then finalise the IC to be created.

2. **Subcircuit creation:**
   After deciding the IC, we start modeling it as a subcircuit in eSim, using the model files present in the eSim device model library only. The design is strictly according to the information given in the official data-sheets of the ICs.This step also includes building the Symbol/Pin diagram of the IC according to the packaging and pin description given in the data-sheets only.

3. **Text Circuit Design:**
   Once the component of the IC is ready, now we can build the test circuits, according to the data-sheets. In this step we build the test cases and test circuits using the component IC.

4. **Schematic Testing:**
   Once the test circuits are ready, now it's time to simulate the test circuits so that the output can be obtained in the form of wave-forms and 8 plots. Here we take

help of KiCad to NgSpice conversion and Simulation feature in eSim

If the output of the test circuit is not as per expectation, this implies that the test case has failed, and there is some error in the schematic. In such cases we go back to the design phase of the IC or the test circuits, to look for possible errors and then repeat the testing process again after making required changes.

Once the expected output of the test cases are correct and satisfy the expected results, then in such a case the IC is declared successfully working. The test case has been verified and the designing process is complete.

Chapter 4

Analog ICs'

4.1 LH0004

The LH0004 is a general-purpose operational amplifier designed to operate over a wide supply voltage range, typically from ±5V to ±40V. Known for its extremely low quiescent power dissipation—typically around 8mW at ±40V—it is well-suited for low-power applications. It offers a large output voltage swing (up to ±35V into a 2kΩ load) and a low input offset voltage, typically around 0.3mV. The device requires only two small external capacitors for frequency compensation, simplifying circuit design. Its wide operating temperature range makes it reliable for both commercial and rugged environments. With high voltage handling and wide bandwidth, it is commonly used in applications like high-voltage power supplies, wideband amplifiers, resolver excitation, and transducer supply circuits.

4.1.1 IC Layout

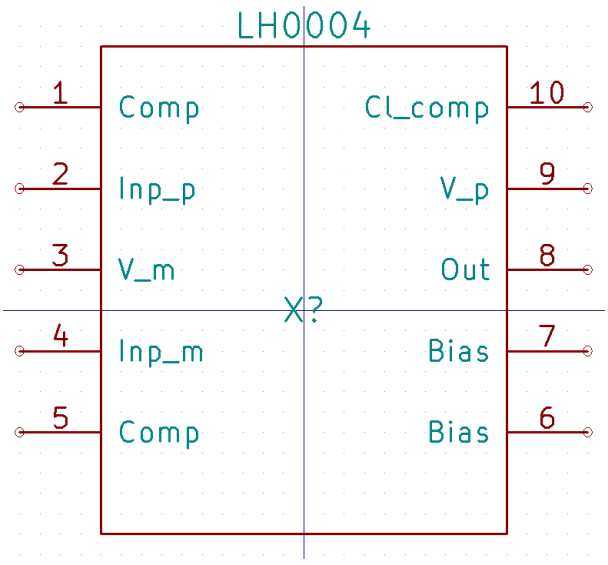

Figure 4.1: Pin Diagram of LH0004

4.1.2 Subcircuit Schematic Diagram

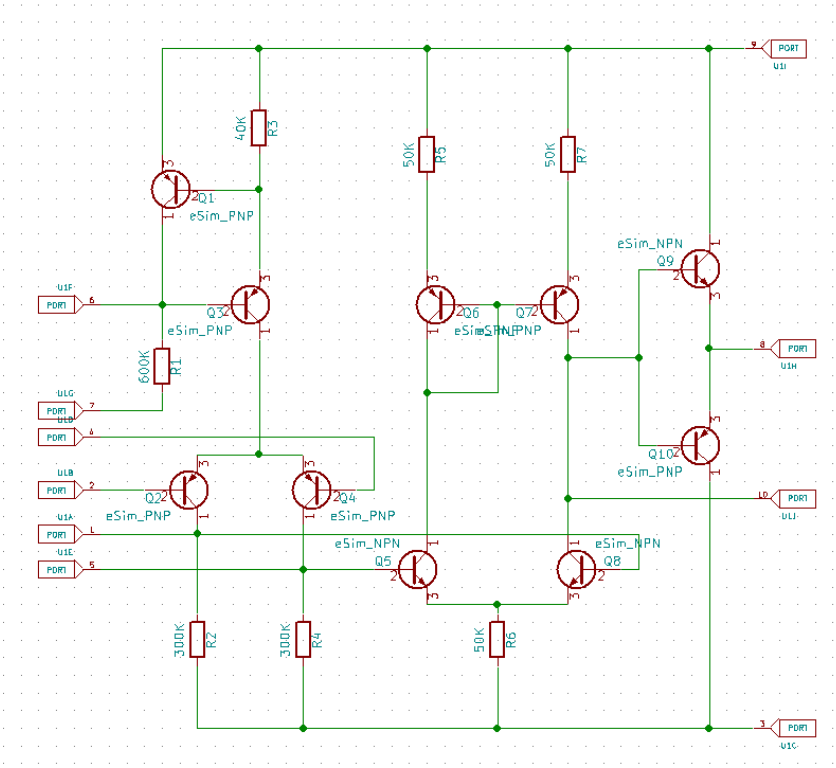

Figure 4.2: Subcircuit Schematic Diagram of LH0004

4.1.3 Test Circuit

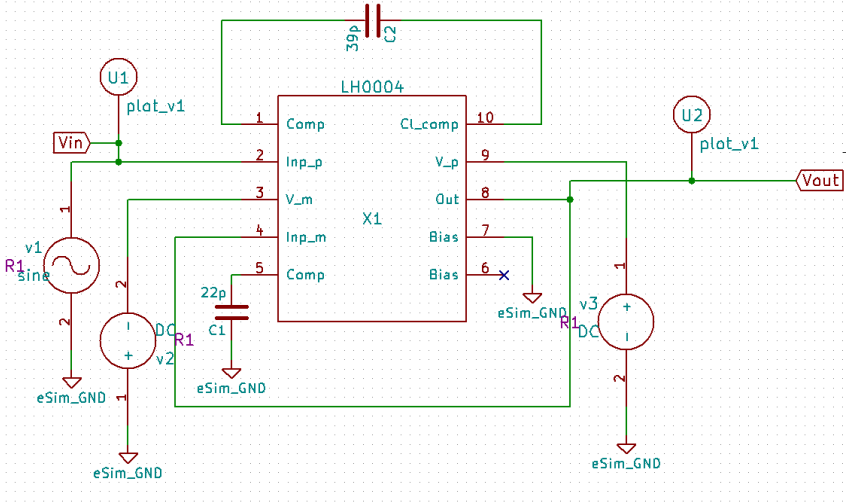

Figure 4.3: Test Circuit of LH0004

4.1.4 Input and Output Plots

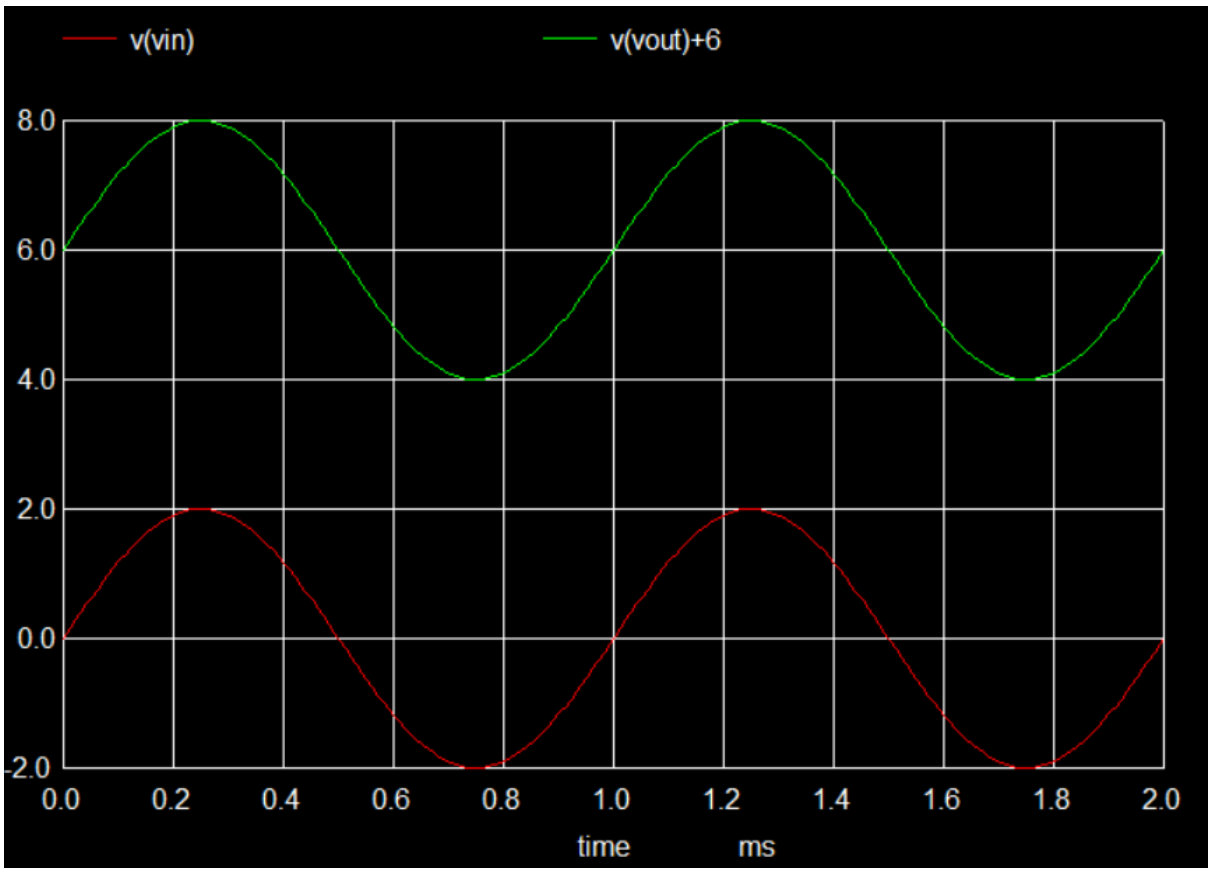

Figure 4.4: Plots of LH0004

Chapter 5

Digital ICs'

5.1 SN74182

The IC 74182 is a look-ahead carry generator designed to improve the speed of binary addition in digital systems. It works by calculating carry signals in advance using the generate and propagate signals provided by adders such as the IC 74181. In typical ripple-carry adders, each bit must wait for the carry to propagate through all the previous stages, which introduces delay. The 74182 eliminates this bottleneck by producing all intermediate carry signals simultaneously, allowing for much faster arithmetic operations, especially in multi-bit adders. It accepts four pairs of generate (G) and propagate (P) inputs from a 4-bit adder, along with an initial carry-in (C0), and produces carry outputs for each bit stage (C1, C2, C3), as well as group generate and propagate outputs. This IC is particularly useful in building high-speed arithmetic logic units (ALUs) and is often cascaded with other 74182 units for wider bit-width operations. Its integration significantly reduces the overall computation time in digital processors and complex arithmetic circuits.

5.1.1 IC Layout

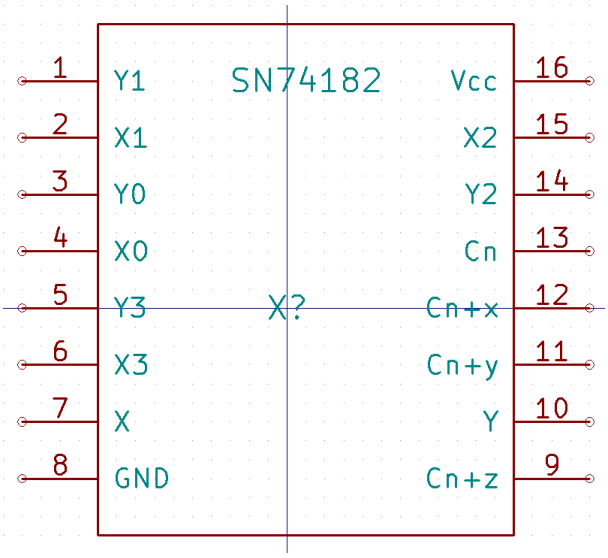

Figure 5.1: Pin Diagram of SN74182

5.1.2 Function Table

FUNCTION TABLE FOR $\overline{G}$ OUTPUT

INPUTS							OUTPUT
$\overline{G}3$	$\overline{G}2$	$\overline{G}1$	$\overline{G}0$	$\overline{P}3$	$\overline{P}2$	$\overline{P}1$	$\overline{G}$
L	X	X	X	X	X	X	L
X	L	X	X	L	X	X	L
X	X	L	X	L	L	X	L
X	X	X	L	L	L	L	L
All other combinations							H

FUNCTION TABLE FOR $\overline{P}$ OUTPUT

INPUTS				OUTPUT
$\overline{P}3$	$\overline{P}2$	$\overline{P}1$	$\overline{P}0$	$\overline{P}$
L	L	L	L	L
All other combinations				H

FUNCTION TABLE FOR C_{n+x} OUTPUT

INPUTS			OUTPUT
$\overline{G}0$	$\overline{P}0$	Cn	C_{n+x}
L	X	X	H
X	L	H	H
All other combinations			L

FUNCTION TABLE FOR C_{n+y} OUTPUT

INPUTS					OUTPUT
$\overline{G}1$	$\overline{G}0$	$\overline{P}1$	$\overline{P}0$	C_n	C_{n+y}
L	X	X	X	X	H
X	L	L	X	X	H
X	X	L	L	H	H
All other combinations					L

FUNCTION TABLE FOR C_{n+z} OUTPUT

INPUTS							OUTPUT
$\overline{G}2$	$\overline{G}1$	$\overline{G}0$	$\overline{P}2$	$\overline{P}1$	$\overline{P}0$	C_n	C_{n+z}
L	X	X	X	X	X	X	H
X	L	X	L	X	X	X	H
X	X	L	L	L	X	X	H
X	X	X	L	L	L	H	H
All other combinations							L

H = high level, L = low level, X = irrelevant
Any inputs not shown in a given table are irrelevant with respect to that output.

Figure 5.2: Function Table of SN74182

5.1.3 Subcircuit Schematic Diagram

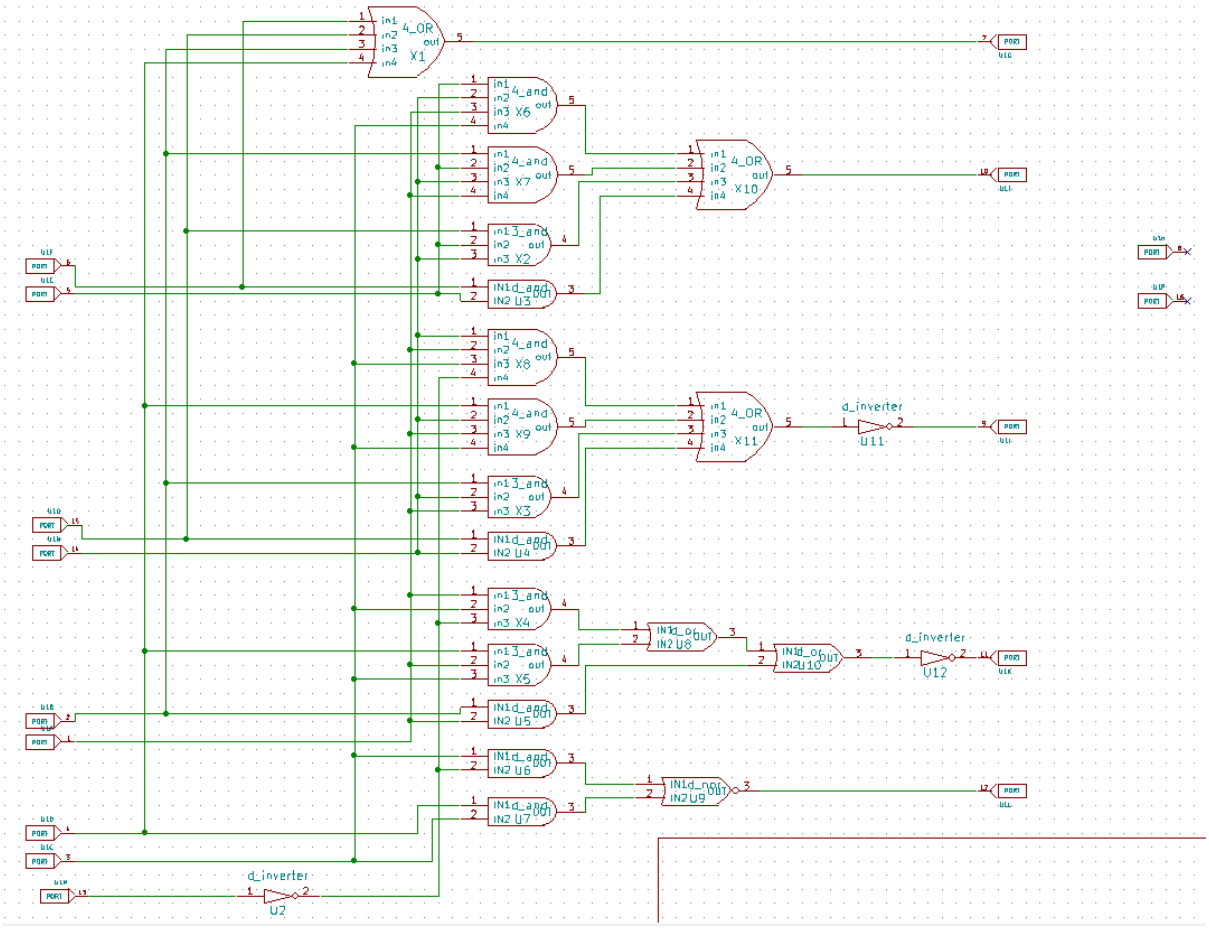

Figure 5.3: Subcircuit Schematic Diagram of SN74182

5.1.4 Test Circuit

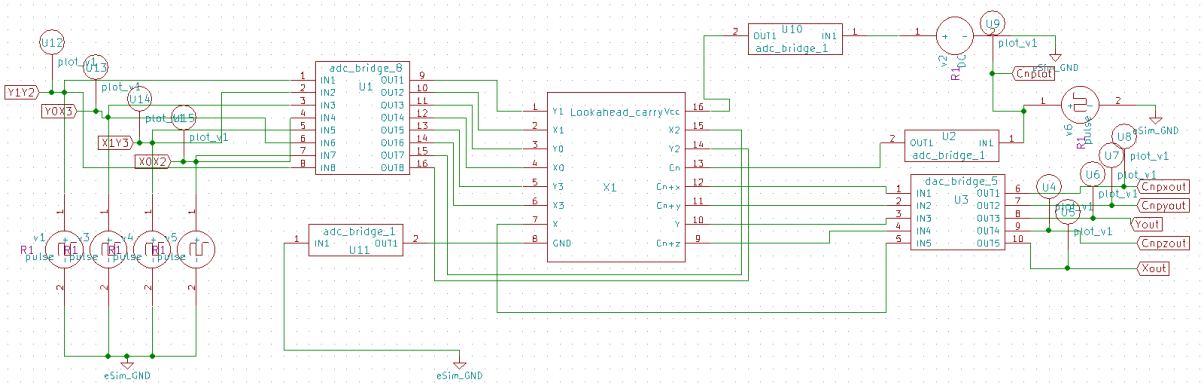

Figure 5.4: Test Circuit of SN74182

5.1.5 Input and Output Plots

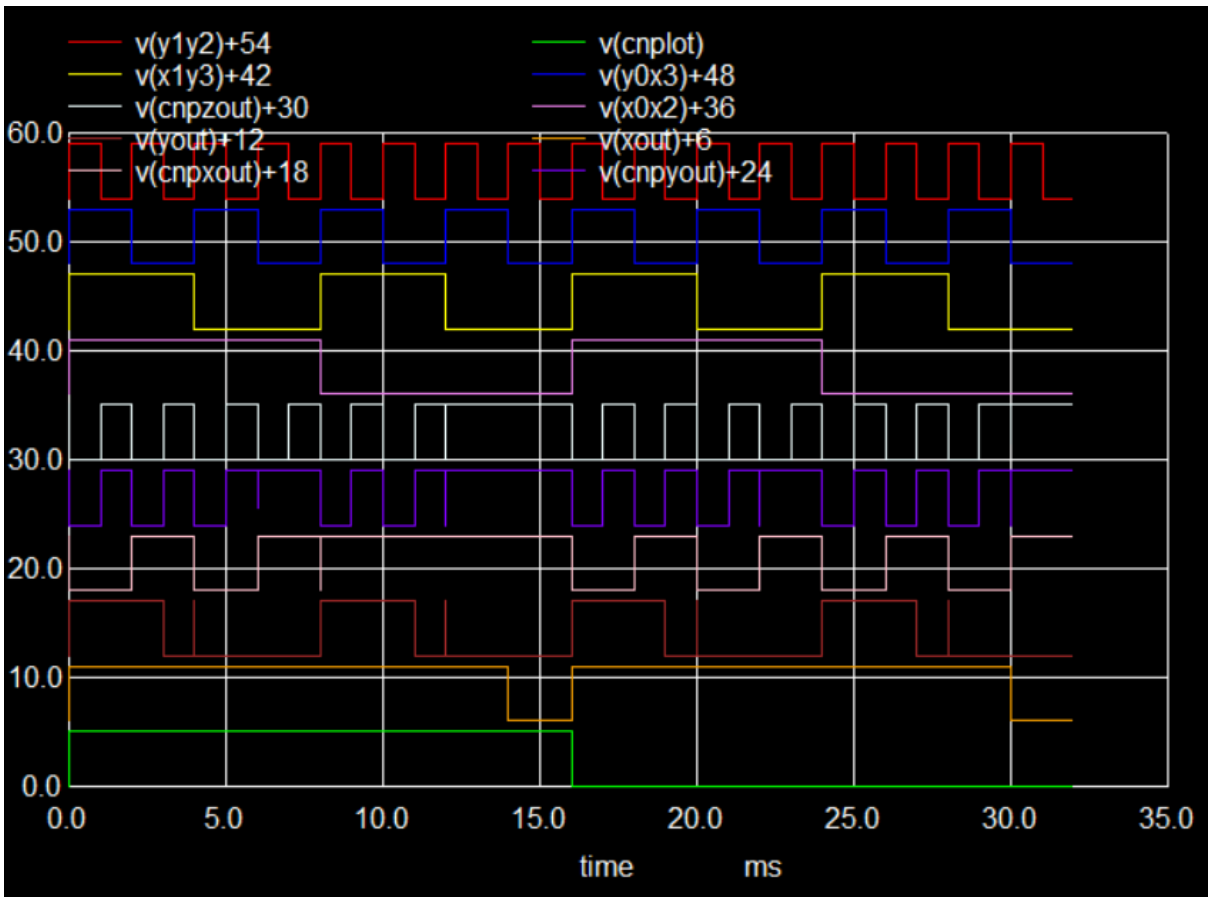

Figure 5.5: Plots of SN74182

5.2 MC10H160

The MC10H160 is a 12-bit parity generator and checker that provides the functionality of detecting or generating parity across up to 12 input lines. It is designed to output a high signal when an odd number of inputs are high, thereby implementing an odd parity function. This makes it especially useful in digital systems where error detection is required, such as in communication protocols or memory systems. One of its practical advantages is that any unconnected inputs default to a logic low state, allowing the device to be used for parity operations with fewer than 12 active inputs. The MC10H160 is also a direct functional replacement for its 10K series predecessor but offers significantly improved performance, with double the speed (i.e., reduced propagation delay) and no increase in power supply current. Owing to these features, it is ideal for high-speed digital applications that demand reliable error-checking capabilities.

5.2.1 IC Layout

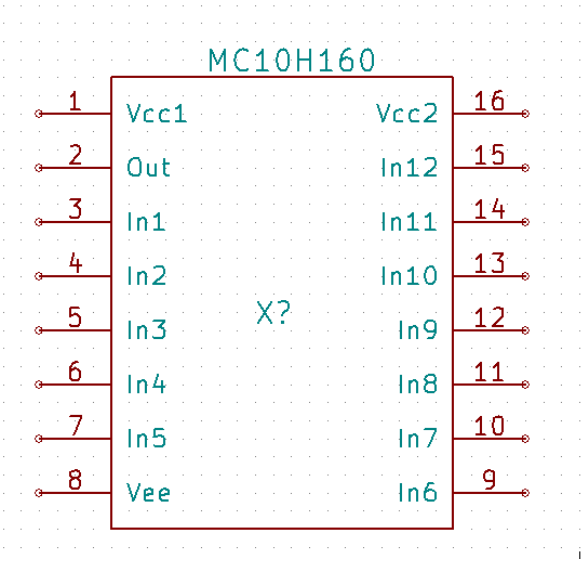

Figure 5.6: Pin Diagram of MC10H160

5.2.2 Subcircuit Schematic Diagram

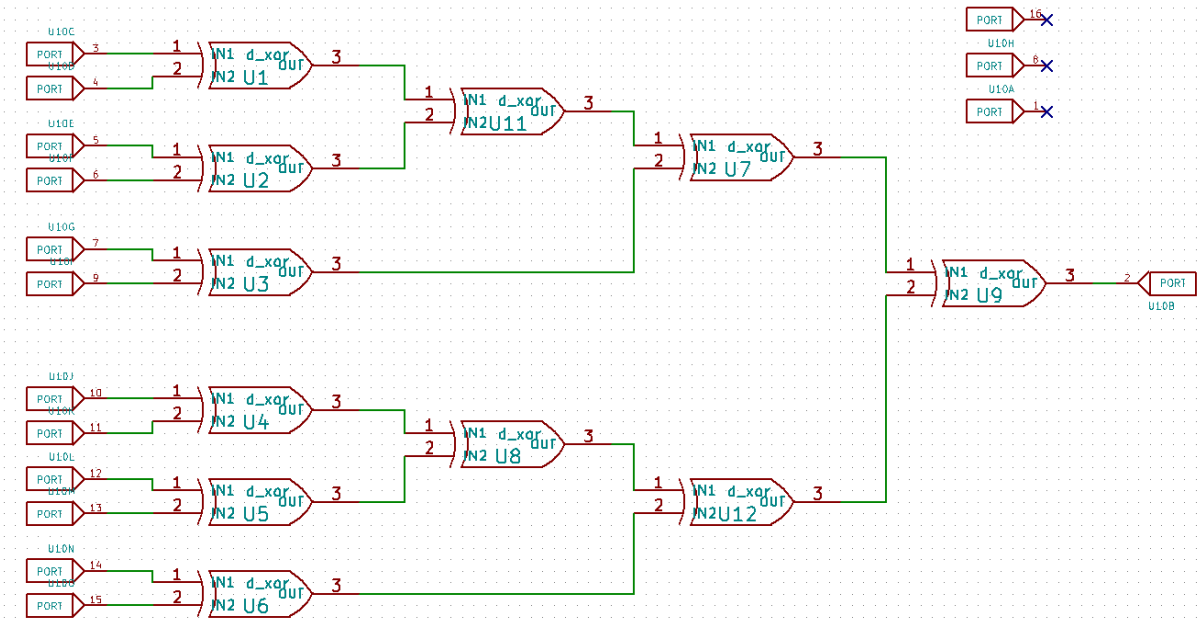

Figure 5.7: Subcircuit Schematic Diagram of MC10H160

5.2.3 Test Circuit

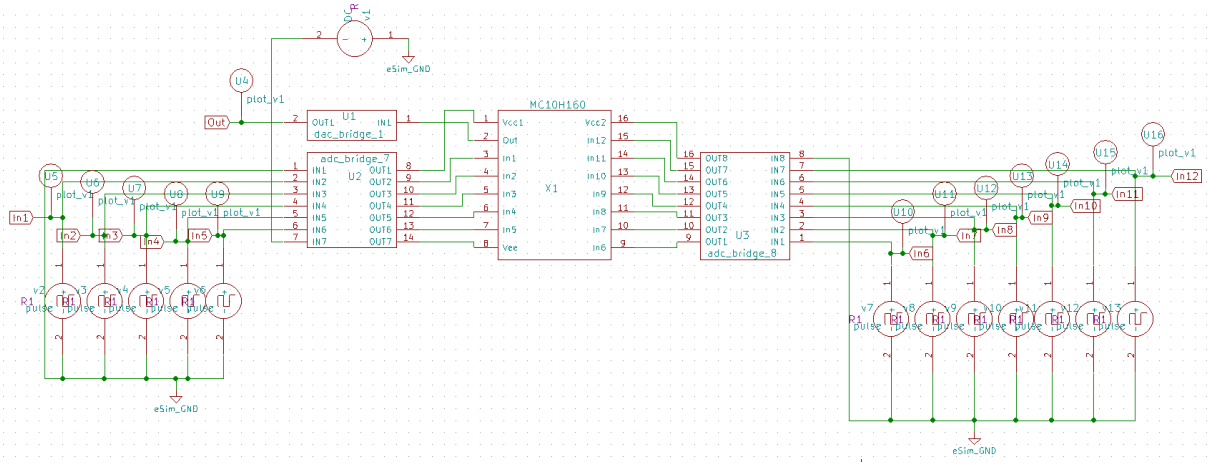

Figure 5.8: Test Circuit of MC10H160

5.2.4 Input and Output Plots

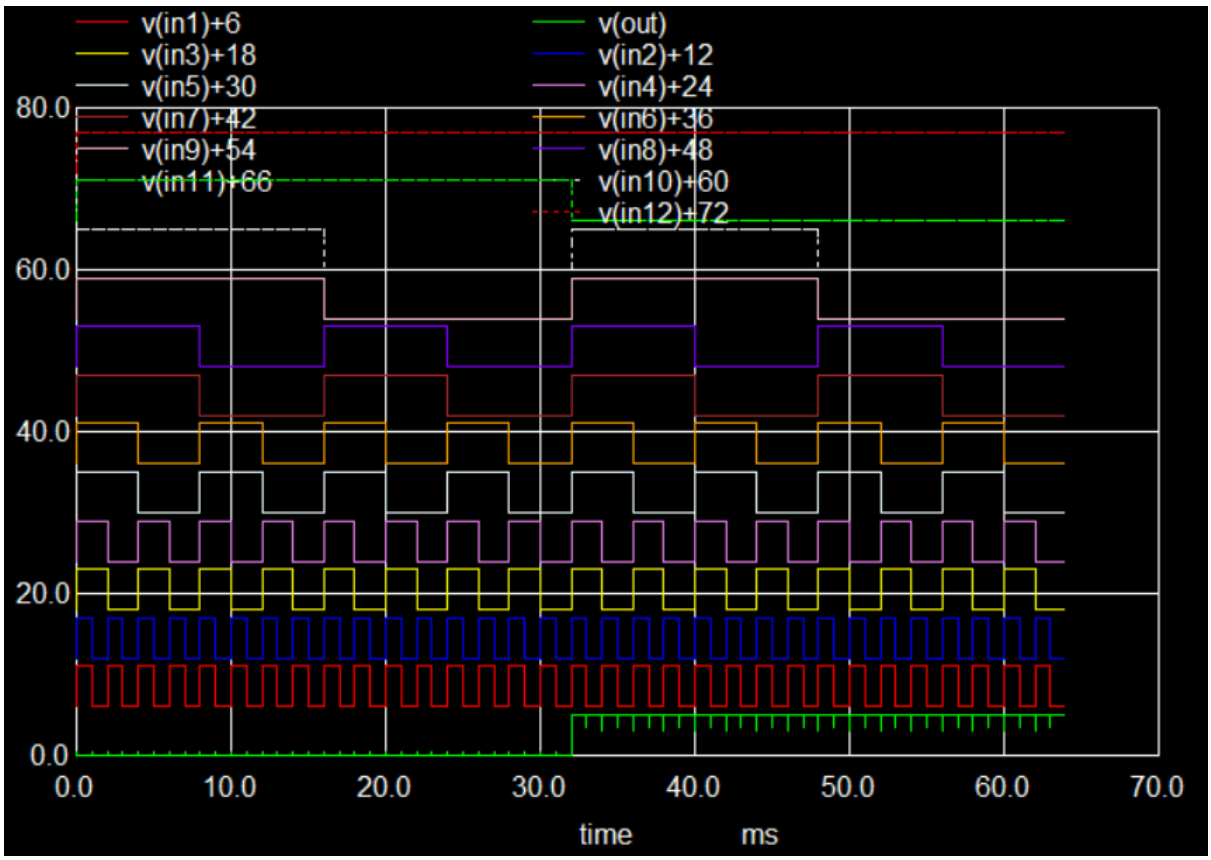

Figure 5.9: Plots of MC10H160

5.3 SN74H60

The SN74H60 is a dual 4-input expander IC that contains two independent 4-input logic functions. It is designed to perform the Boolean operation X = ABCD when connected to X and $\overline{X}$ inputs of compatible logic ICs such as SN7423, SN5450, or SN7450. These expanders are typically used to increase the number of input lines to logic gates without increasing complexity. The SN74H60 is specifically characterized for commercial temperature ranges from 0 ° C to 70 ° C, while its military grade variants like the SN54H60 support a wider range from -55 ° C to 125 ° C. The device is housed in DIP packages and offers dependable logic expansion functionality, commonly used in large-scale digital systems.

5.3.1 IC Layout

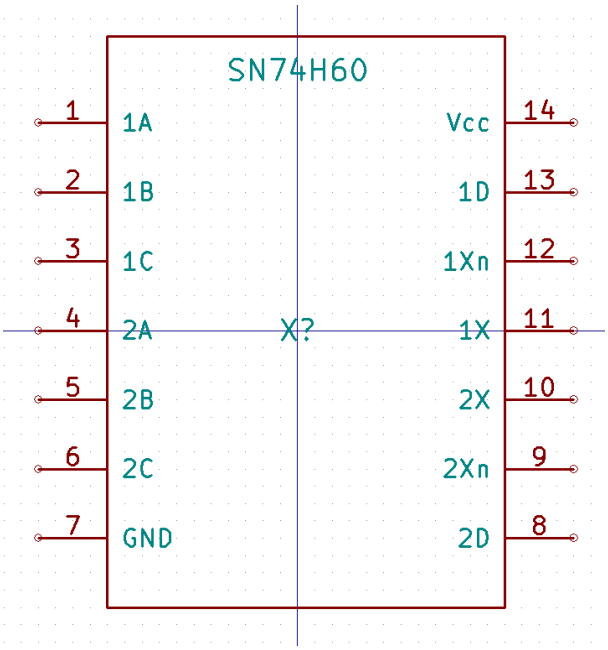

Figure 5.10: Pin Diagram of SN74H60

5.3.2 Subcircuit Schematic Diagram

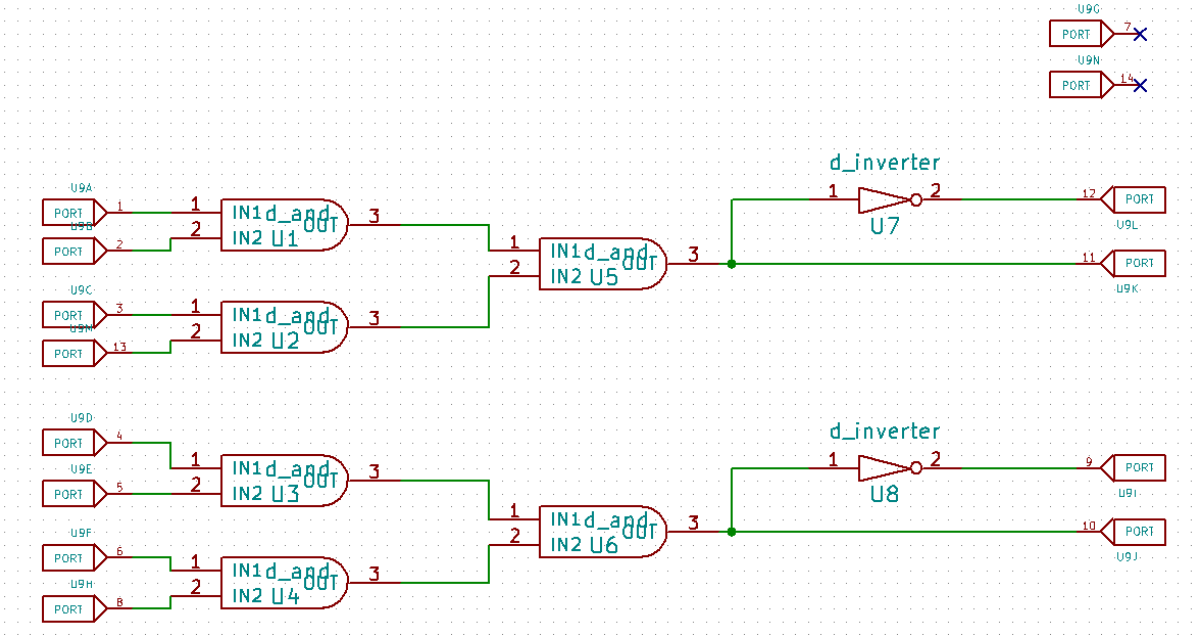

Figure 5.11: Subcircuit Schematic Diagram of SN74H60

5.3.3 Test Circuit

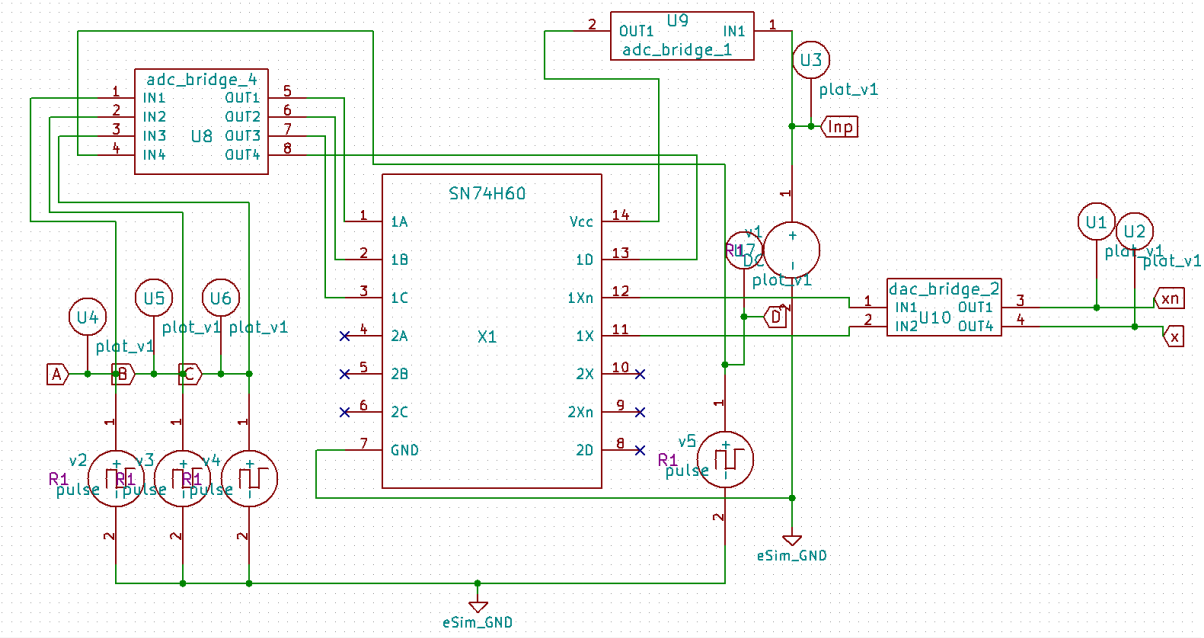

Figure 5.12: Test Circuit of SN74H60

5.3.4 Input and Output Plots

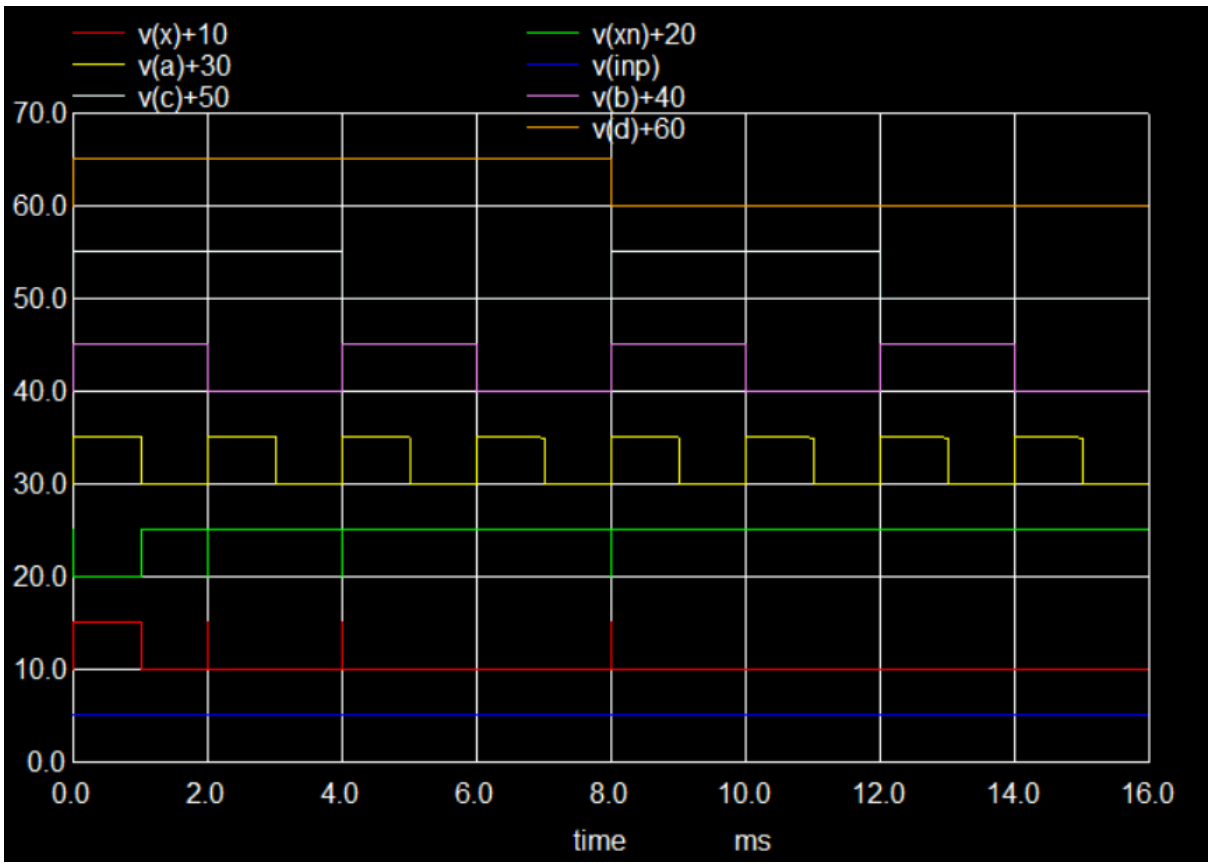

Figure 5.13: Plots of SN74H60

5.4 SN74H62

The SN74H62 is a 4-wide AND-OR expander IC that allows the implementation of complex Boolean expressions using combinations of multiple inputs. It performs the function X = AB + CDE + FGH + IJ, providing flexibility in logic expansion. It is designed to be compatible with other logic families such as SN74H50, SN74H53, and SN74H55 when connected to their respective X and $\overline{X}$ inputs. The SN74H62 is suitable for commercial operating conditions, whereas its military-grade variant SN54H62 supports extended ranges of temperatures. This IC is especially useful in digital systems that require high-density logic processing.

5.4.1 IC Layout

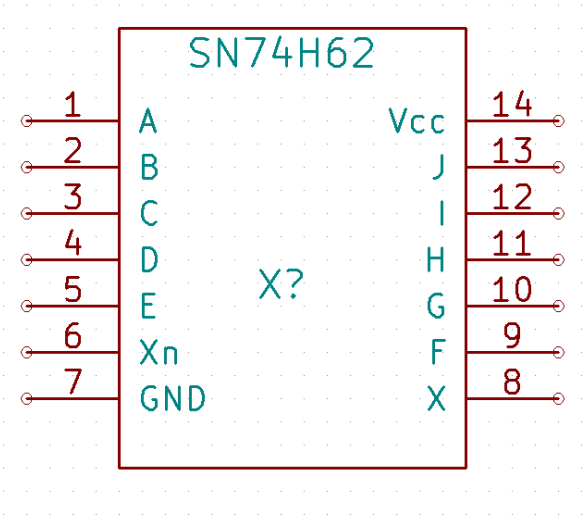

Figure 5.14: Pin Diagram of SN74H62

5.4.2 Subcircuit Schematic Diagram

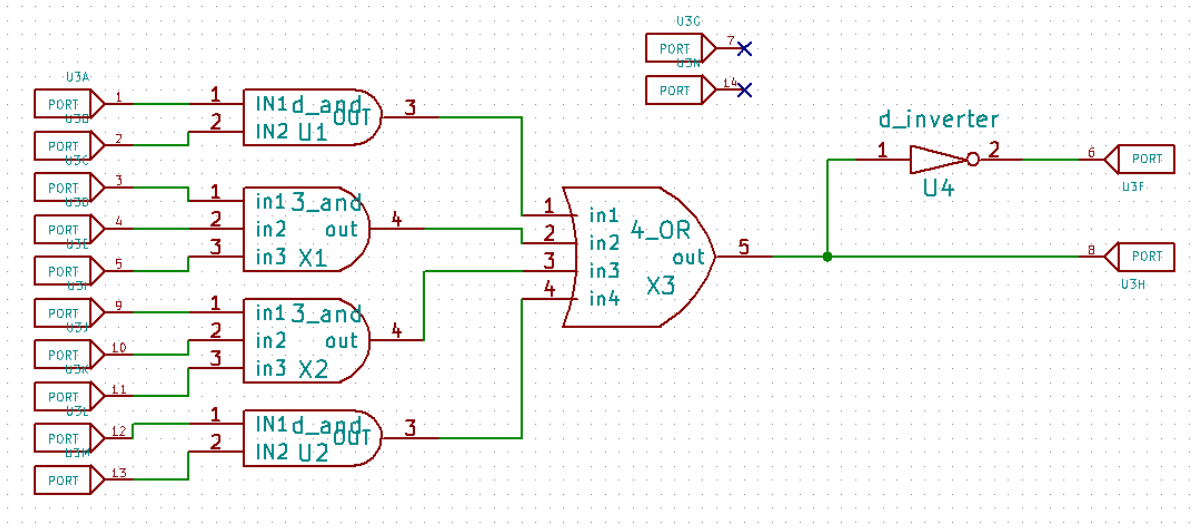

Figure 5.15: Subcircuit Schematic Diagram of SN74H62

5.4.3 Test Circuit

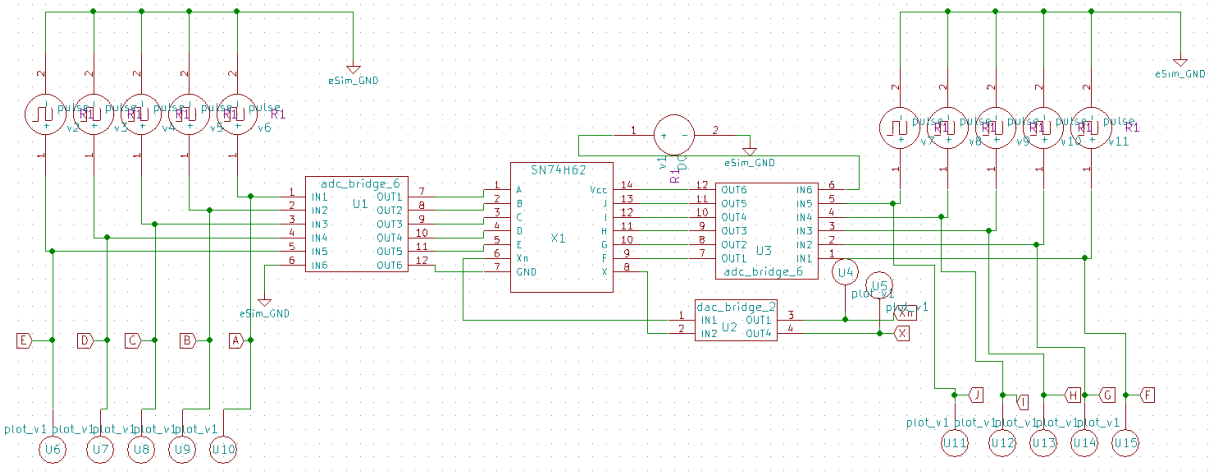

Figure 5.16: Test Circuit of SN74H62

5.4.4 Input and Output Plots

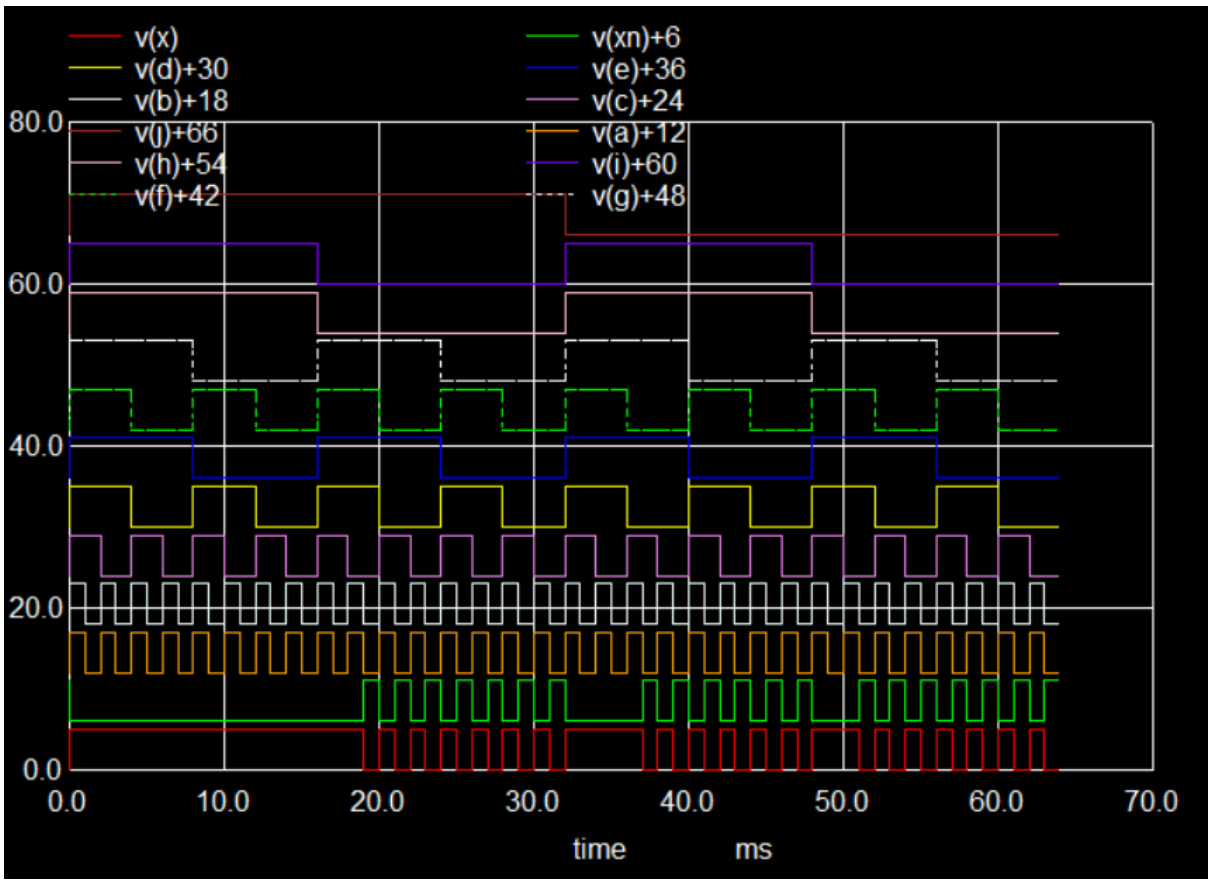

Figure 5.17: Plots of SN74H62

5.5 SN74279

The SN74279 is a quad S-R (Set-Reset) latch IC containing four independent latches, each with a pair of complementary outputs. Each latch features an active-low enable input and operates asynchronously, meaning it responds immediately to changes in the set and reset inputs without requiring a clock. The SN74279 is typically used in applications where temporary data storage, signal synchronization, or logic control is needed. It is ideal for use in sequential logic circuits, timing circuits, and data latching where a simple memory element is required. Its versatility and straightforward logic design make it a fundamental component in digital electronics.

5.5.1 IC Layout

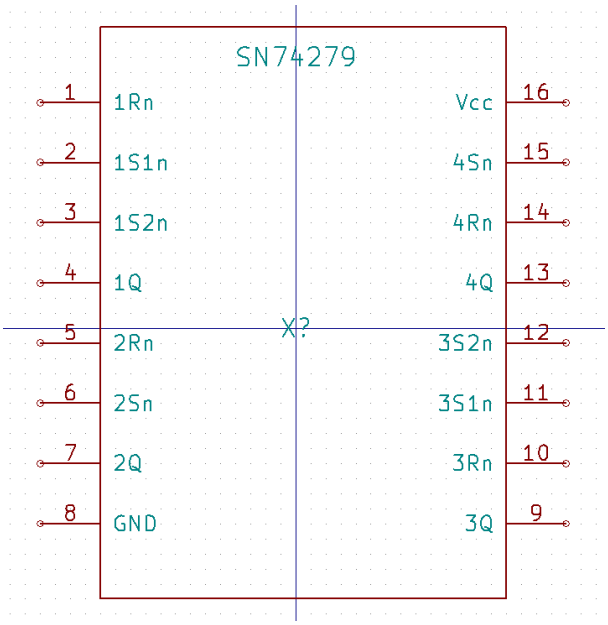

Figure 5.18: Pin Diagram of SN74279

5.5.2 Function Table

FUNCTION TABLE
(each latch)

INPUTS		OUTPUT
$\overline{S}$†	$\overline{R}$	Q
H	H	Q_0
L	H	H
H	L	L
L	L	H‡

H = high level L = low level

†For latches with double S inputs:

Q_0 = the level of Q before the indicated input conditions were established.

‡ This configuration is nonstable: that is, it may not persist when the $\overline{S}$ and $\overline{R}$ inputs return to their inactive (high) level.

H = both $\overline{S}$ inputs high

L = one or both $\overline{S}$ inputs low

Figure 5.19: Function Table of SN74279

5.5.3 Subcircuit Schematic Diagram

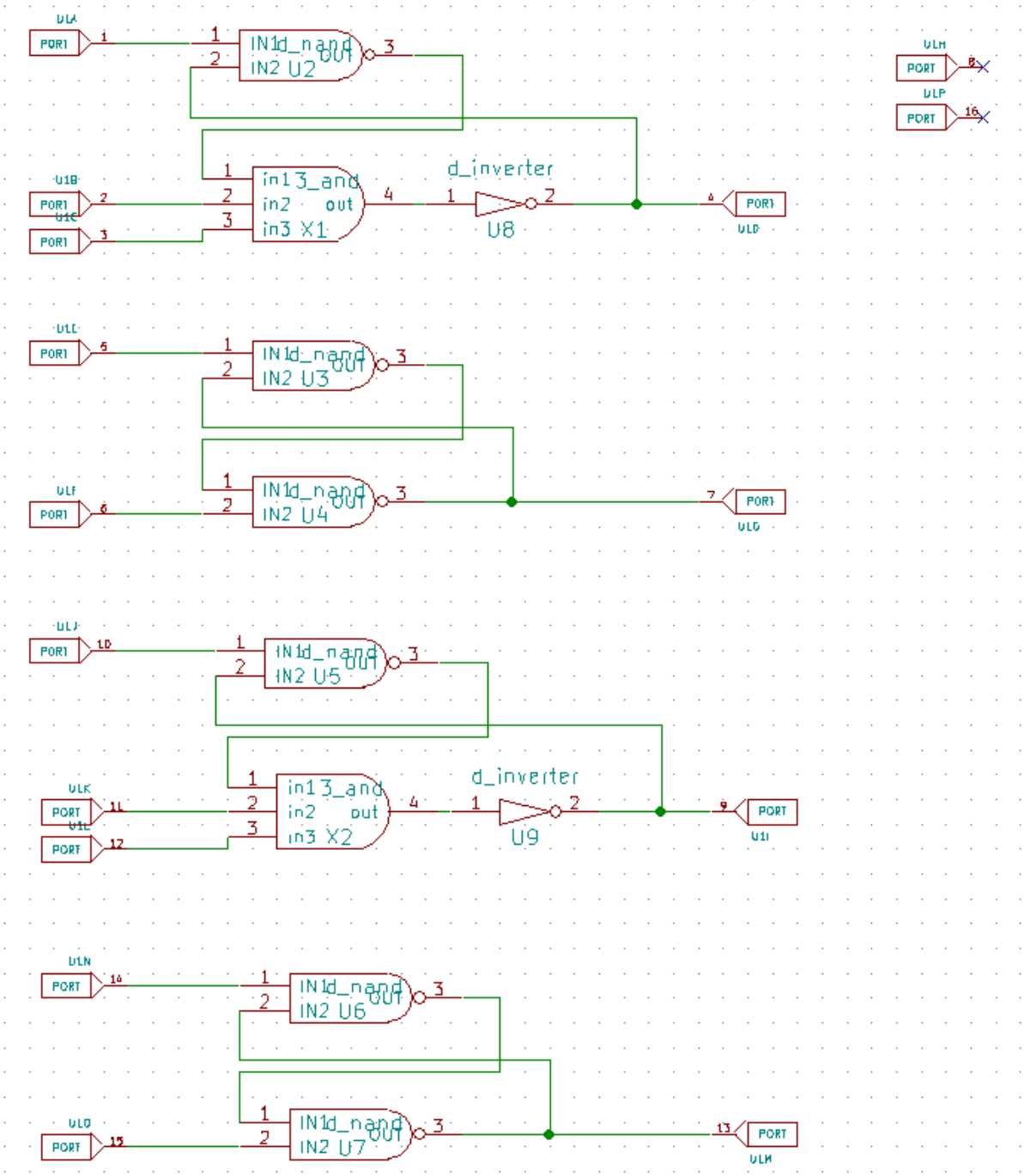

Figure 5.20: Subcircuit Schematic Diagram of SN74279

5.5.4 Test Circuit

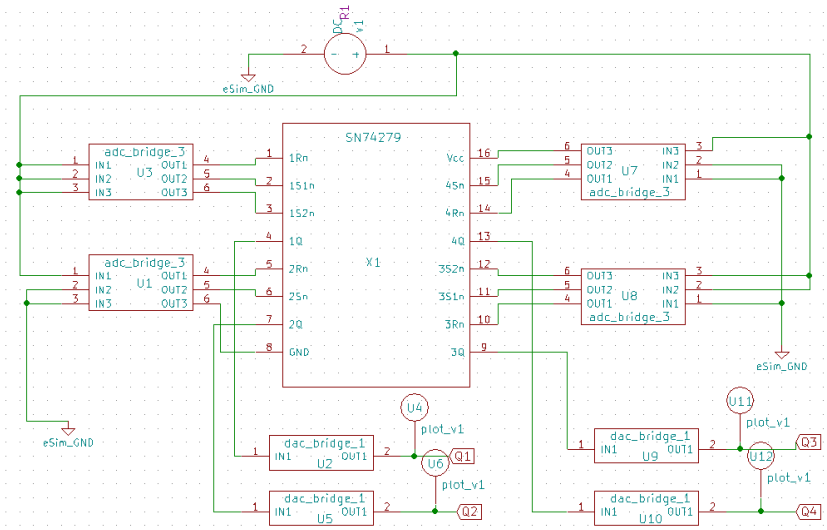

Figure 5.21: Test Circuit of SN74279

5.5.5 Input and Output Plots

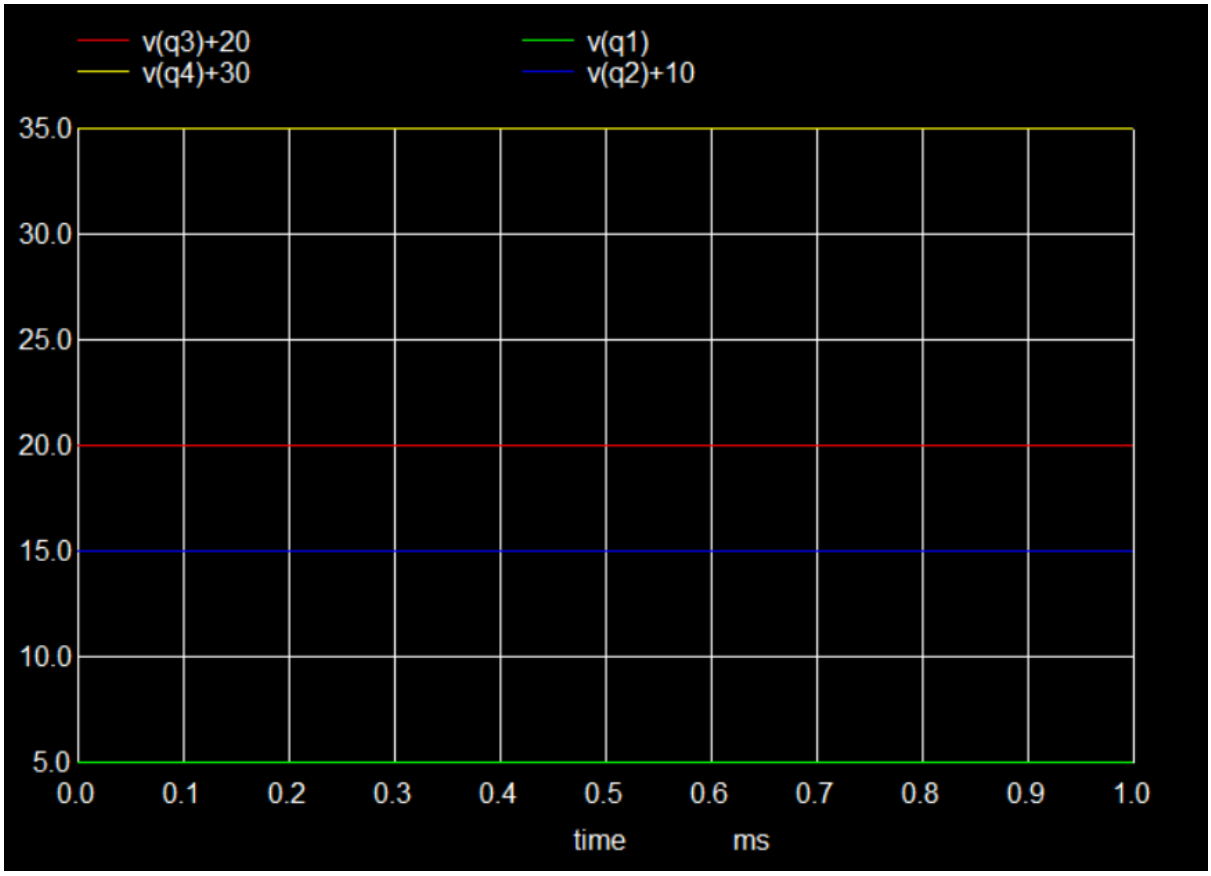

Figure 5.22: Plots of SN74279

5.6 SN74H55

The SN74H55 is a 2-wide, 4-input AND-OR-INVERT (AOI) gate IC, designed to perform complex Boolean functions efficiently. Specifically, it supports the expandable logic function $Y = \overline{ABCD + EFGH + X}$, where X is typically the output from another compatible IC such as the SN54H60 or SN74H60. This structure allows for logic expansion and cascading of gates in larger digital systems. The IC is particularly useful in logic design that requires high-density function implementation using minimal components. It is compatible with a wide range of Texas Instruments logic families and is available in both commercial and military-grade variants, making it suitable for applications demanding reliability across varied temperature ranges.

5.6.1 IC Layout

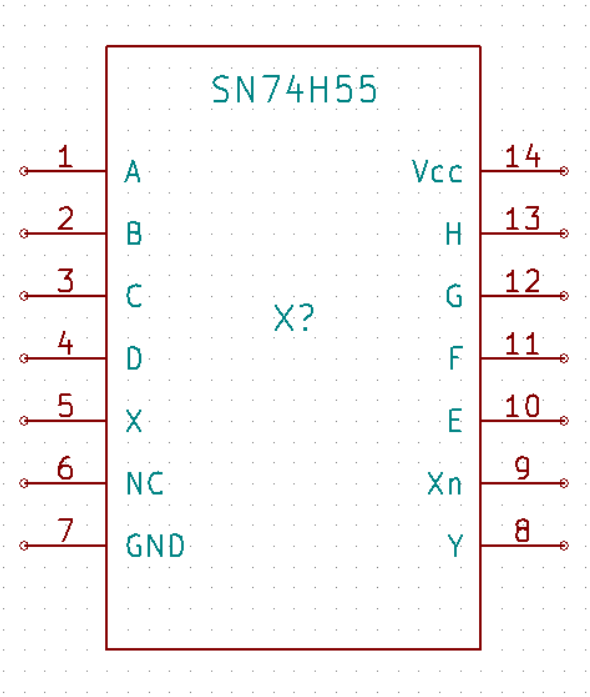

Figure 5.23: Pin Diagram of SN74H55

5.6.2 Subcircuit Schematic Diagram

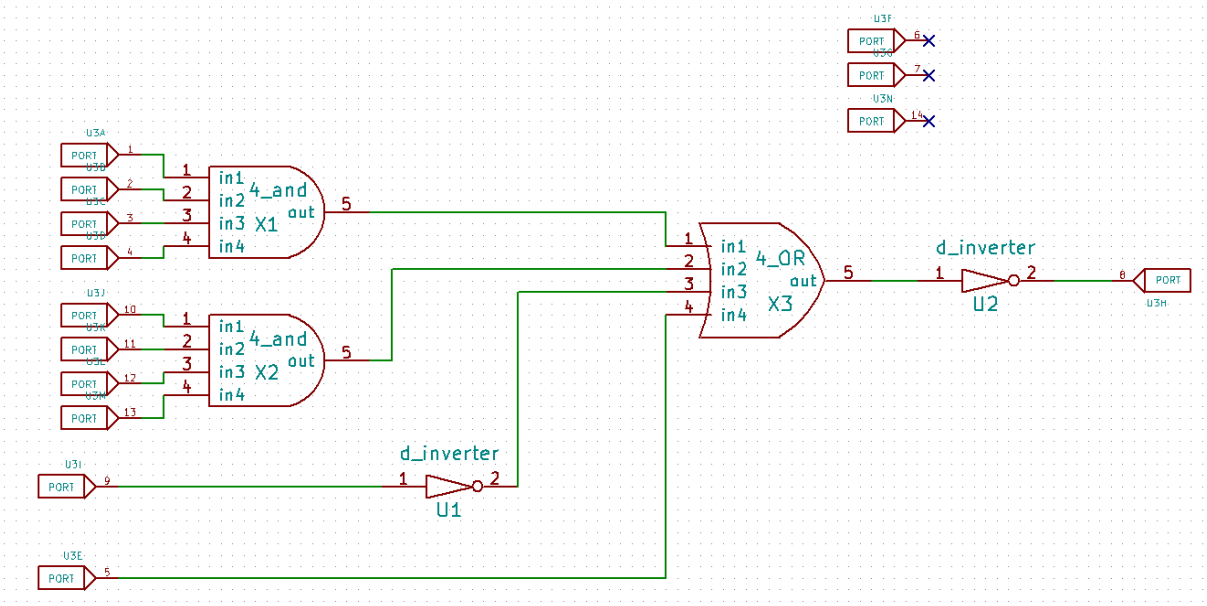

Figure 5.24: Subcircuit Schematic Diagram of SN74H55

5.6.3 Test Circuit

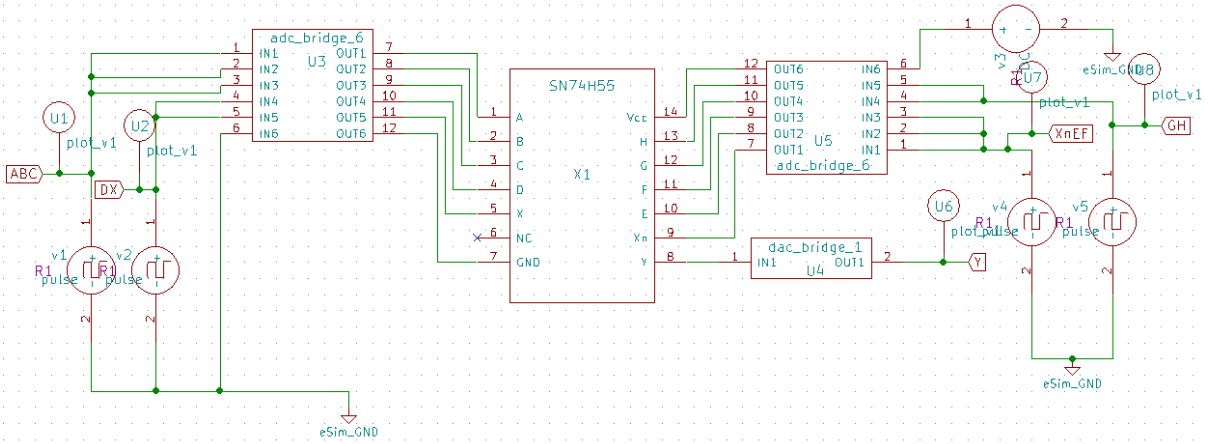

Figure 5.25: Test Circuit of SN74H55

5.6.4 Input and Output Plots

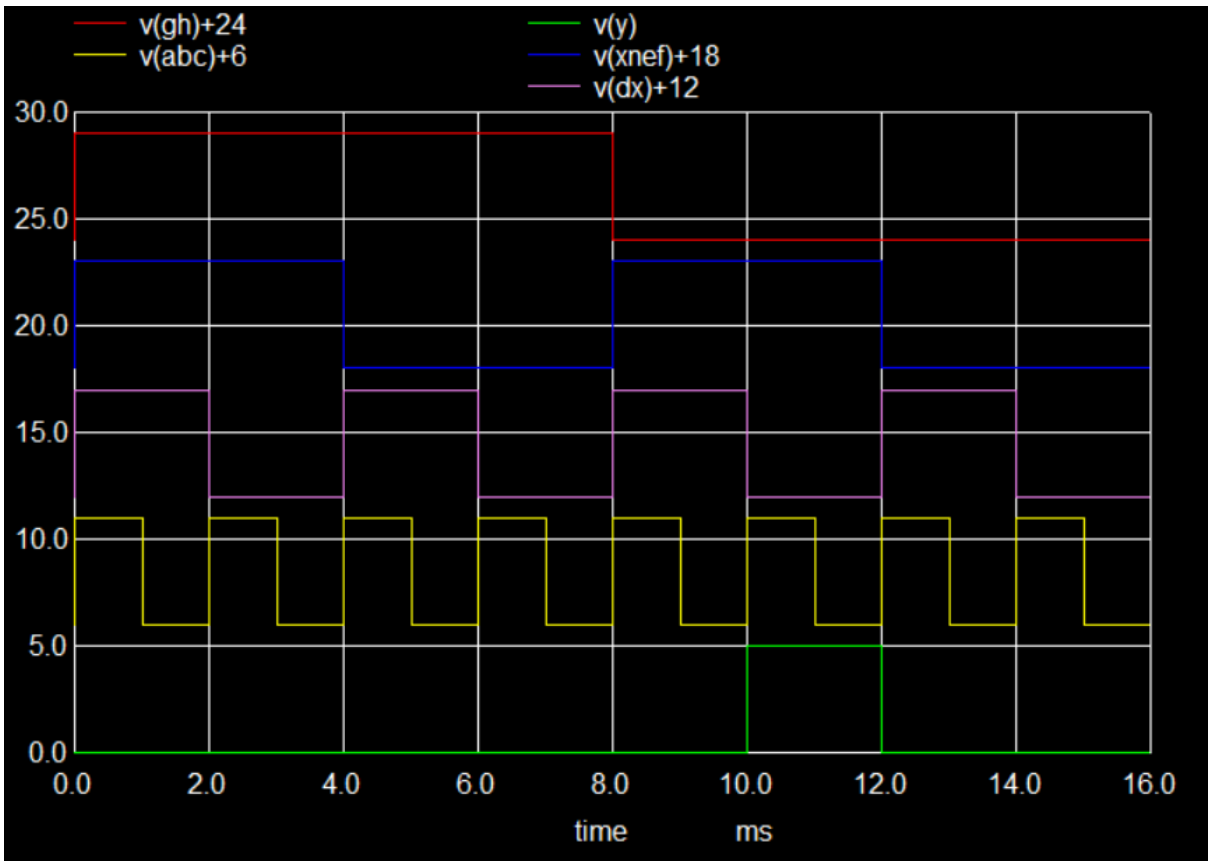

Figure 5.26: Plots of SN74H55

5.7 SN74H53

The SN74H53 is an expandable 4-wide AND-OR-INVERT (AOI) logic gate IC, designed for high-density digital logic systems. It performs the Boolean function $Y = \overline{AB + CD + EFG + HI + X}$, enabling complex logic implementation in a compact form. The variable X typically represents the output of other compatible logic expanders such as SN5460, SN7460, SN54H60, SN74H60, SN54H62, or SN74H62. This expandability makes the SN74H53 ideal for building extended logic circuits. It is available in both military-grade (SN54H53) and commercial-grade (SN74H53) variants, which implies wide temperature range and suitable for applications. Its versatility and robust operating range make it a reliable choice for complex digital applications.

5.7.1 IC Layout

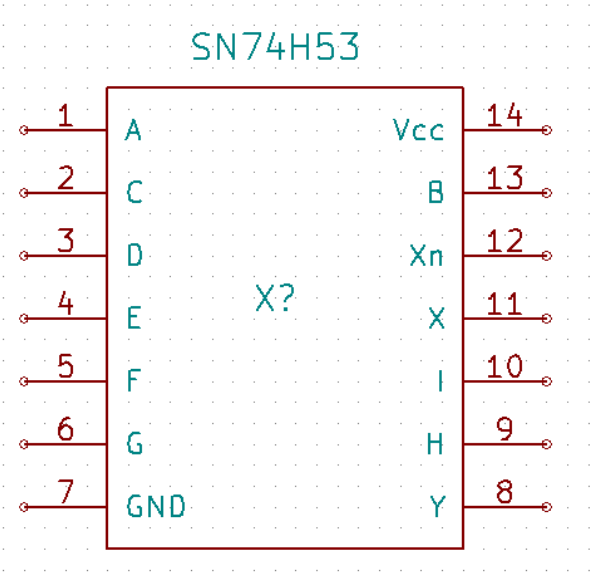

Figure 5.27: Pin Diagram of SN74H53

5.7.2 Subcircuit Schematic Diagram

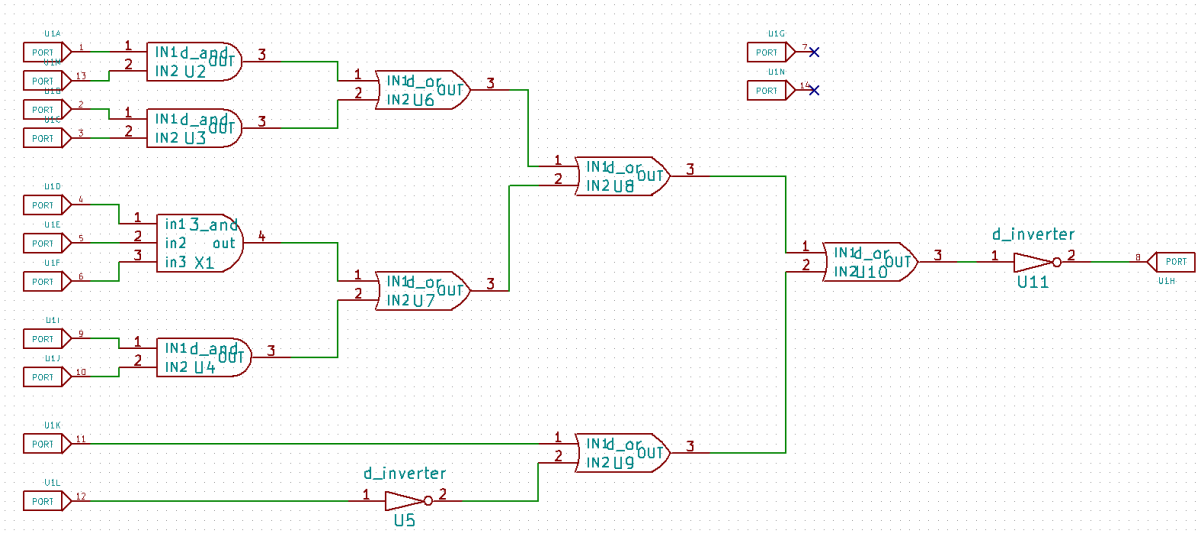

Figure 5.28: Subcircuit Schematic Diagram of SN74H53

5.7.3 Test Circuit

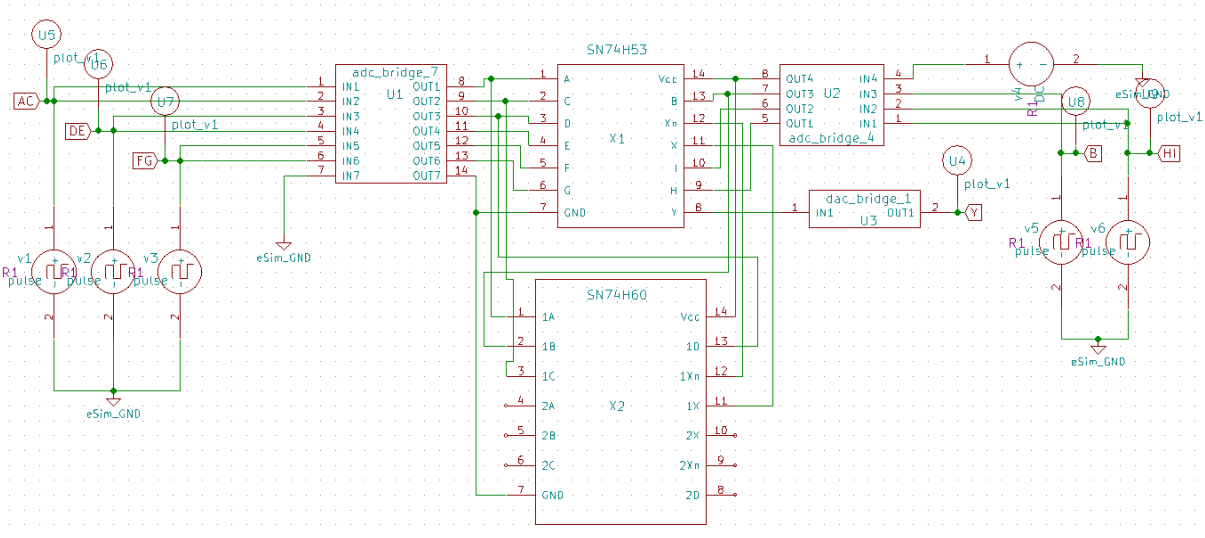

Figure 5.29: Test Circuit of SN74H53

5.7.4 Input and Output Plots

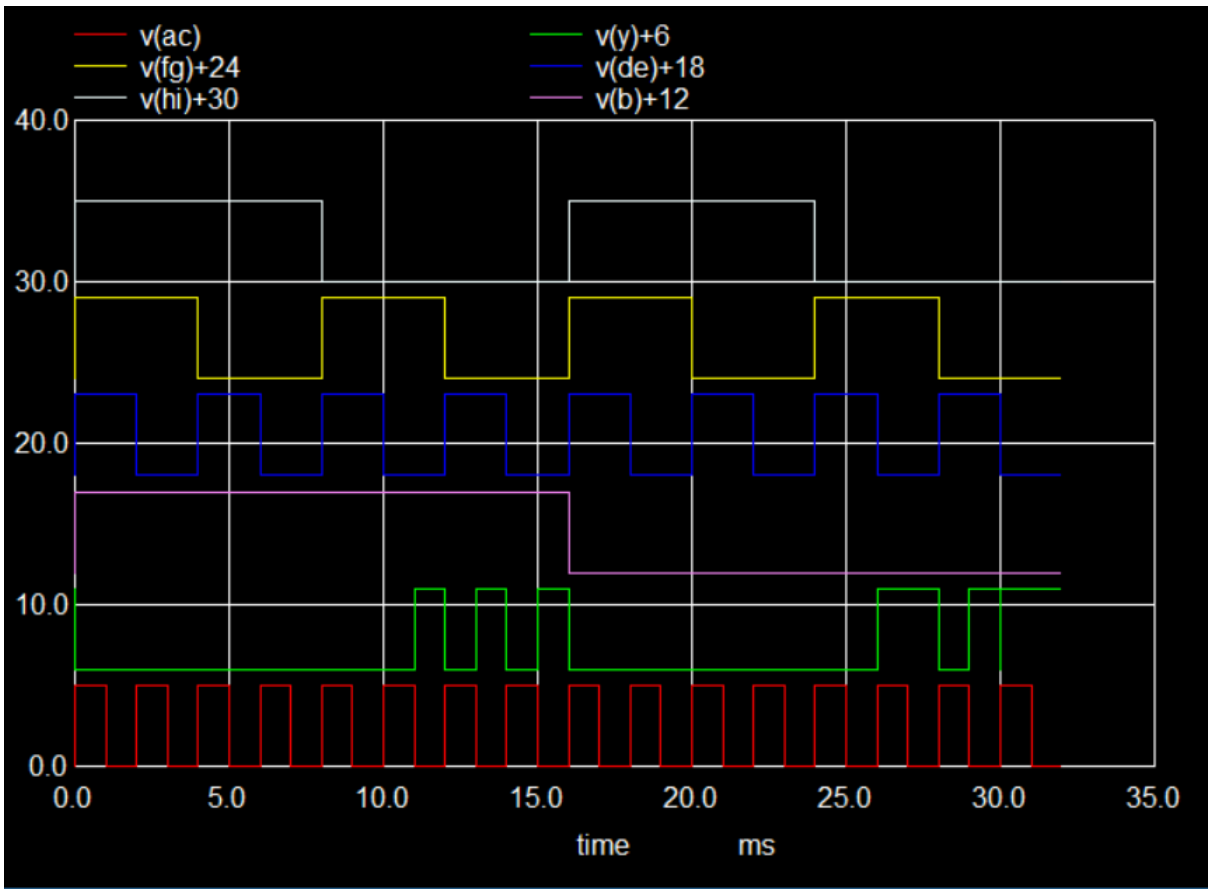

Figure 5.30: Plots of SN74H53

5.8 SN7407

The SN7407 is a TTL hex buffer/driver IC with high-voltage open-collector outputs, designed to interface with high-level circuits such as MOS logic or to drive high-current loads like lamps and relays. It is commonly used as a buffer for TTL inputs and outputs, offering robust sink-current capability. The SN7407 features a minimum breakdown voltage of 30V and supports a maximum sink current of 40mA, making it ideal for driving indicator lamps, relays, and other output devices in digital systems. The device performs the Boolean function $Y = A$ in positive logic, effectively acting as a high-power buffer while ensuring compatibility with most TTL logic levels.

5.8.1 IC Layout

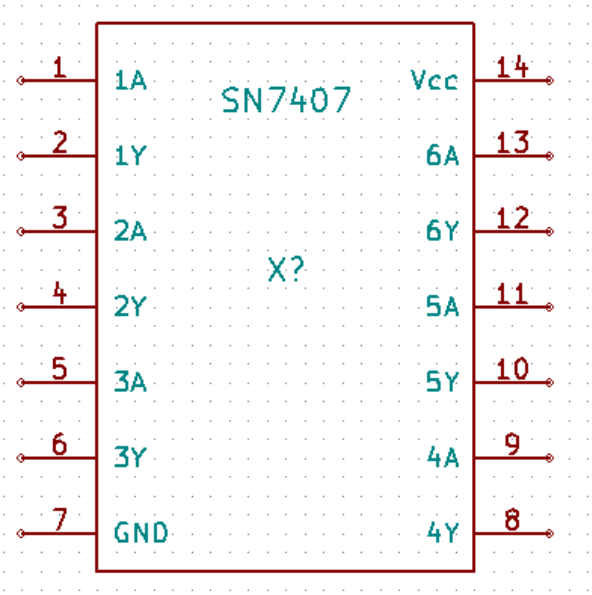

Figure 5.31: Pin Diagram of SN7407

5.8.2 Subcircuit Schematic Diagram

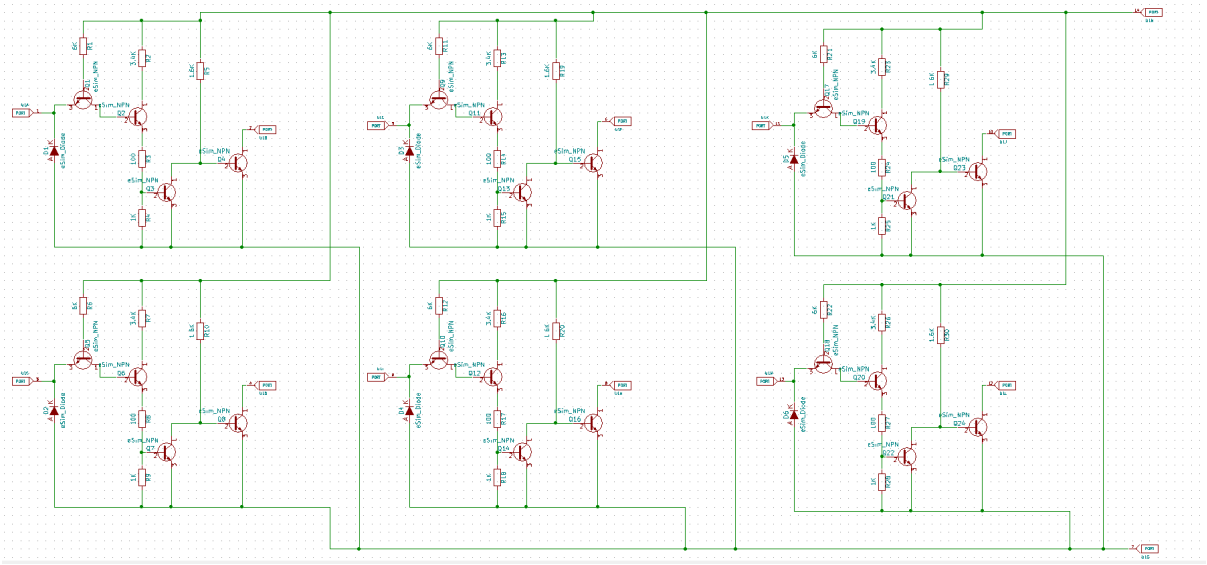

Figure 5.32: Subcircuit Schematic Diagram of SN7407

5.8.3 Test Circuit

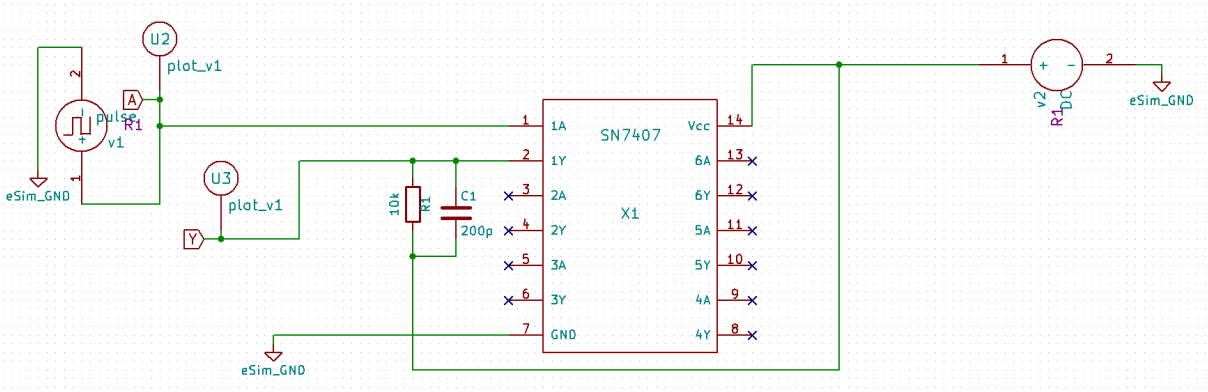

Figure 5.33: Test Circuit of SN7407

5.8.4 Input and Output Plots

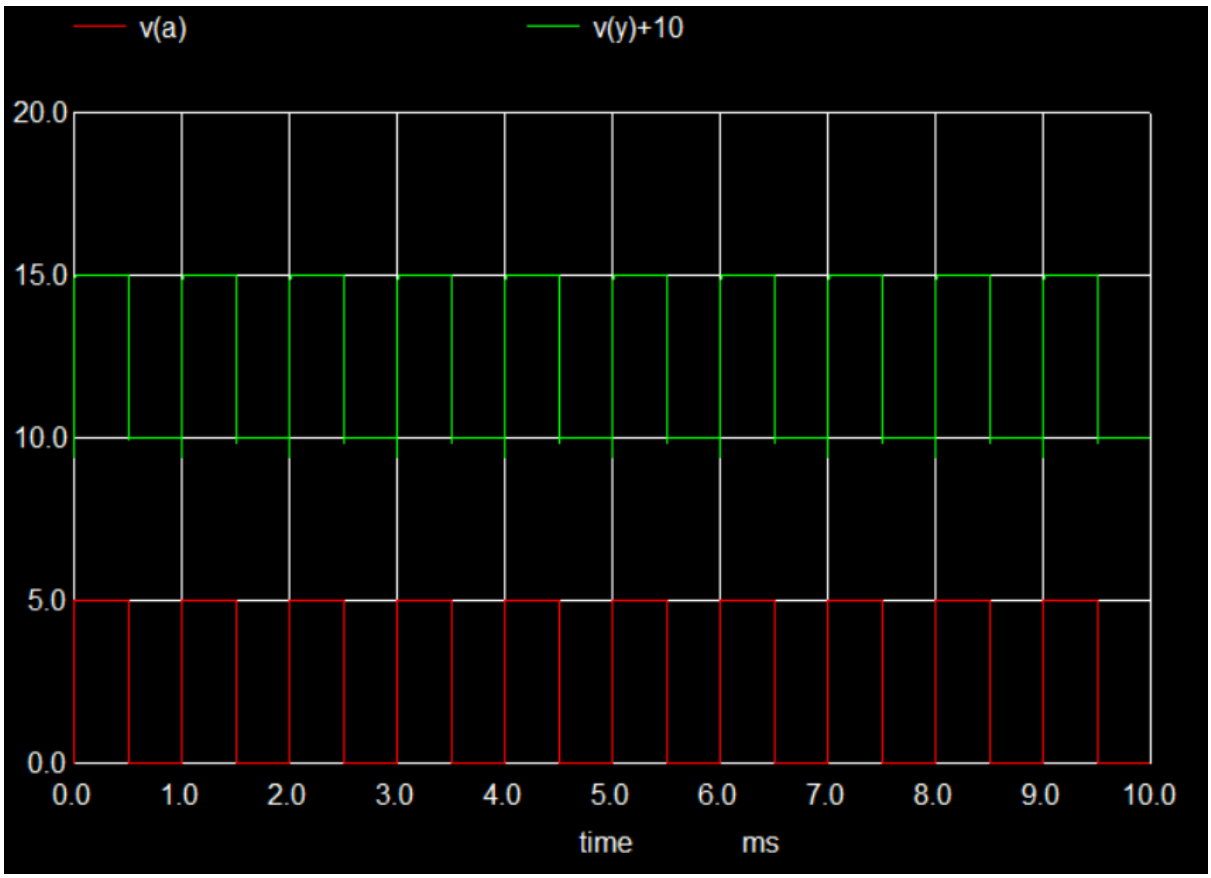

Figure 5.34: Plots of SN7407

5.9 SN74116

The SN74116 is a TTL integrated circuit that features two independent 4-bit D-type latches with asynchronous clear functionality. Each 4-bit latch includes its own clear input and dual-enable inputs, making it highly suitable for cascaded register implementations. When both enable inputs are low, the latch becomes transparent, allowing outputs to follow data inputs. If either enable goes high, the data is latched and further changes in input do not affect the output. The clear input overrides all other functions, resetting all four outputs regardless of the enable states. This IC is commonly used in temporary data storage, buffering, and data synchronization tasks, especially in TTL-based digital systems.

5.9.1 IC Layout

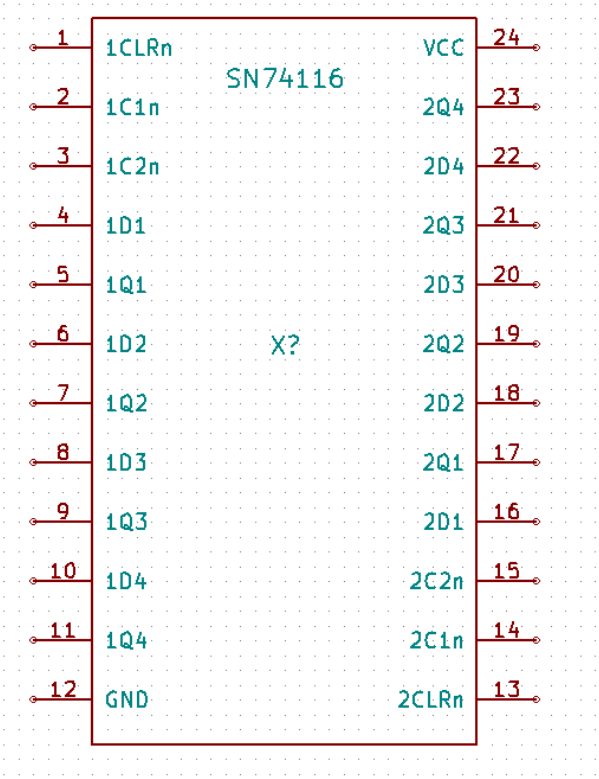

Figure 5.35: Pin Diagram of SN74116

5.9.2 Function Table

FUNCTION TABLE
(EACH LATCH)

INPUTS				OUTPUT
$\overline{\text{CLEAR}}$	ENABLE		DATA	Q
	$\overline{C1}$	$\overline{C2}$		
H	L	L	L	L
H	L	L	H	H
H	X	H	X	Q_0
H	H	X	X	Q_0
L	X	X	X	L

H = high level, L = low level, X = irrelevant
Q_0 = the level of Q before these input conditions were established.

Figure 5.36: Function Table of SN74116

5.9.3 Subcircuit Schematic Diagram

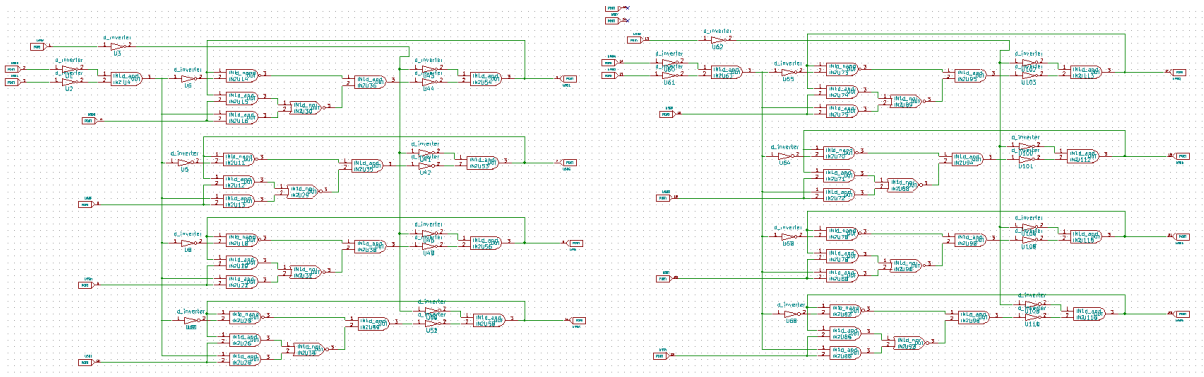

Figure 5.37: Subcircuit Schematic Diagram of SN74116

5.9.4 Test Circuit

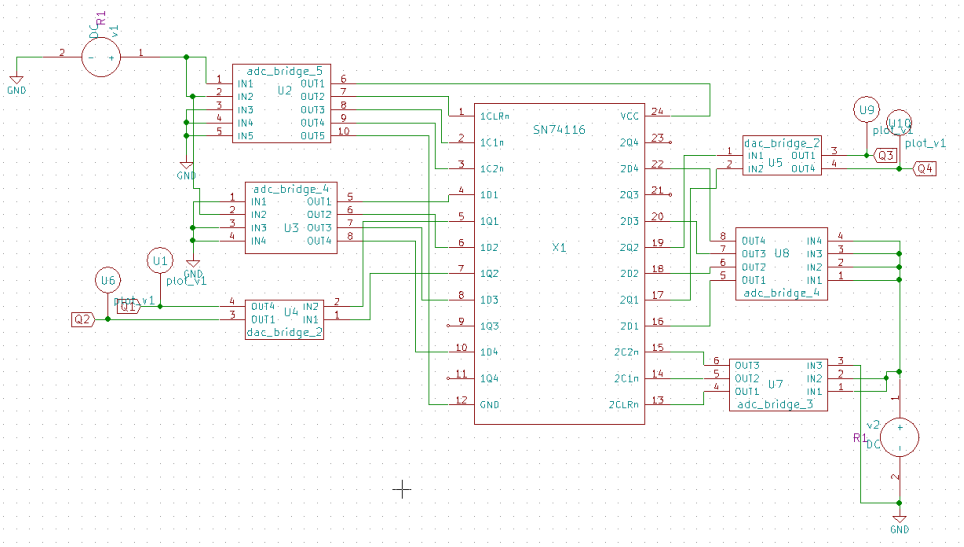

Figure 5.38: Test Circuit of SN74116

5.9.5 Input and Output Plots

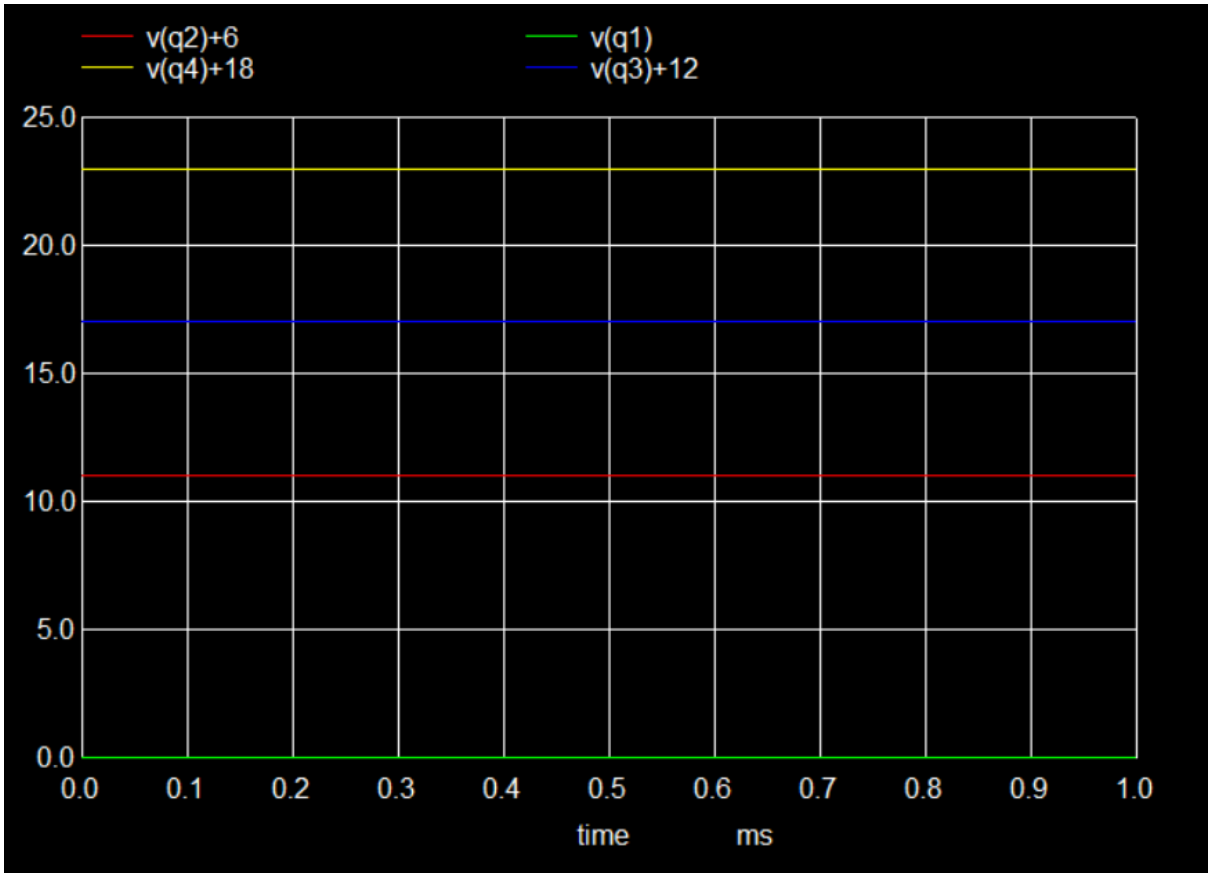

Figure 5.39: Plots of SN74116

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