Summer Fellowship Report

Integrated Circuit Design using Subcircuit feature of eSim

&

Mixed Signal Simulation & Device Modelling in eSim

Submitted by

Pavithra B S

B.Tech (Electronics and Communication Engineering)
SASTRA Deemed University, Thanjavur

Under the guidance of

Mr. Sumanto Kar
Assistant Project Manager, FOSSEE, IIT Bombay

Prof. Kannan M. Moudgalya
Principal Investigator - FOSSEE, IIT Bombay

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Chapter 1

Introduction

The FOSSEE (Free/Libre and Open Source Software for Education) project, an initiative by IIT Bombay, is part of the National Mission on Education through ICT (NMEICT), Ministry of Education, Government of India. The primary goal of FOSSEE is to promote the use of Free and Open Source Software (FOSS) tools in academia and research, offering an affordable and transparent alternative to expen- sive proprietary software. FOSSEE supports a wide range of open-source software including eSim, Scilab, OpenFOAM, Python, R, OpenModelica, DWSIM, and others. Through its various projects, internships, and fellowships, FOSSEE provides students, educators, and researchers an opportunity to contribute to the development and enhancement of these tools. The project not only encourages practical learning and skill development but also aims to foster a collaborative ecosystem where individuals can contribute meaning- fully to the open-source community. By integrating FOSS into academic curricula and research, FOSSEE empowers institutions across India to achieve greater self- reliance and innovation in STEM education.

1.1 eSim

eSim (Electronic Simulation) is a free and open-source Electronic Design Automation (EDA) tool developed as part of the FOSSEE (Free/Libre and Open Source Software for Education) project at IIT Bombay. It is created with the aim of providing a viable open-source alternative to widely used proprietary software in the field of circuit design and simulation, such as OrCAD, PSpice, and LTspice.[1] The tool brings together the power of multiple open-source platforms—most notably KiCad for schematic capture and PCB design, and Ngspice for circuit simulation—into a single integrated environment. eSim is designed to support the entire workflow of electronics development, from circuit design to simulation, offering users a comprehensive platform for learning and innovation. eSim is particularly well-suited for academic institutions, students,

and researchers, as it eliminates the dependency on expensive licensed software. Its development is aligned with the larger objective of the FOSSEE project: to promote self-reliance, accessibility, and transparency in technical education through the use of open-source tools. By adopting eSim, users gain exposure to industry-relevant design processes

using freely available resources. It enables hands-on experience with modern EDA methodologies and encourages active learning and experimentation. Moreover, it supports the open-source philosophy by allowing users to contribute back to its development, ensuring continuous improvement and community-driven innovation. In an educational context, eSim plays a crucial role in fostering practical elec- tronics skills. It enables learners to explore circuit behavior, verify designs through simulation, and even move towards prototyping through PCB layout generation—all within a unified, license-free platform. This makes eSim a valuable asset for engi- neering curricula and student projects.

1.1.1 NgSpice

NgSpice is an open-source circuit simulator integrated into eSim for performing ana- log and mixed-signal simulations. Based on the SPICE simulation engine, NgSpice supports DC, AC, transient, and parametric analyses, making it suitable for ana- lyzing a wide range of circuits. [2] It serves as the simulation backend in eSim, enabling users to simulate circuits de- signed using schematic editors like KiCad.Ngspice has become an essential resource in education and research, enabling learners and engineers to simulate and test cir- cuits efficiently, without relying on proprietary software.

1.1.2 Makerchip

Makerchip is a browser-based integrated development environment (IDE) for design- ing and simulating digital circuits using TL-Verilog (Transaction-Level Verilog). It is a powerful platform that supports modular, scalable, and clean digital design using modern hardware description methodologies. Makerchip enables real-time simula- tion, visualization, and debugging of digital logic, making it highly suitable for both learning and development.[3] As part of its ongoing effort to expand support for open-source tools, FOSSEE, IIT Bombay has integrated Makerchip with eSim. This integration allows users to work with TL-Verilog-based digital components alongside analog subcircuits within the same simulation environment. It bridges the gap between analog and digital design, enabling mixed-signal circuit development in a unified and open-source platform. The integration enhances eSim's capability as a complete circuit design platform—supporting schematic entry, analog simulation, digital design using TL-Verilog, and combined verification workflows. It also aligns with the broader goals of the FOSSEE project to make advanced design and simulation tools freely accessible for academic and professional use.

1.1.3 KiCad

KiCad is an open-source electronic design automation (EDA) tool integrated into eSim, a platform developed by FOSSEE, IIT Bombay, for circuit simulation and PCB design. In eSim, KiCad serves as the primary environment for schematic cap- ture and PCB layout, allowing users to design circuits visually, assign footprints, and generate board layouts with precision. Its integration with eSim enables a seamless workflow from schematic creation to simulation using Ngspice. This allows

users—especially students and educators—to design, simulate, and validate electronic circuits in a free and open-source ecosystem without the need for expensive proprietary software. The inclusion of KiCad in eSim promotes hands-on learning, enhances understanding of electronics, and supports the development of custom ICs and systems using open tools.[4]

1.1.4 GHDL

GHDL is a powerful and open-source VHDL simulator that plays a crucial role in digital system design and verification. Unlike traditional simulators that may rely on proprietary software, GHDL compiles VHDL code directly into native machine code, which makes simulations faster and more efficient. It supports behavioral, structural, and RTL-level modeling, enabling users to simulate complex digital designs, such as processors, communication systems, and finite state machines. In the context of eSim, GHDL is fully integrated to allow users to design circuits using VHDL and verify their functionality through simulation, all within a single unified environment. It also supports waveform generation (via tools like GTKWave), enabling users to analyze signal behavior over time. This integration makes eSim a comprehensive platform for both analog and digital circuit simulation, supporting mixed-mode design and fostering a strong foundation in electronics and hardware description languages for students, researchers, and hobbyists.[5]

Chapter 2

Features of eSim

eSim offers similar capabilities and ease of use as any equivalent proprietary software for schematic creation, simulation, and PCB design, without having to pay a huge amount of money to procure licenses. Hence it can be an affordable alternative to educational institutions and SMEs. It can serve as an alternative to commer- cially available/licensed software tools like OrCAD, PSpice, LTspice, Xpedition, and HSPICE.

- **Schematic Design with KiCad :** Design electronic circuits easily using Ki- Cad's user-friendly schematic capture tool integrated into eSim.
- **Netlist Creation and Circuit Simulation with Ngspice:** Generate netlists from the schematic and simulate the circuit behavior using Ngspice.
- **PCB Design and Gerber File Generation:** Design PCB layouts using KiCad and generate Gerber files required for PCB fabrication.
- **Custom Component Modeling:** Add or modify SPICE models and subcircuits using the built-in Model Builder and Subcircuit Builder tools.
- **Mixed-Signal Circuit Simulation:** Simulate circuits containing both analog and digital components in a single environment.
- **Cross-Platform Compatibility:** Available on both Ubuntu and Windows operating systems for broad accessibility.
- **Integration with OpenModelica:** Enables co-simulation with OpenModelica for system-level modeling and cyber-physical system design.
- **Cost-Effective Alternative to Proprietary Software:** eSim offers capabilities similar to commercial tools like OrCAD, PSpice, LTspice, Xpedition, and HSPICE.
- **No Licensing Cost:** Being open-source, eSim does not require costly licenses, making it highly affordable for educational institutions and small

to medium enterprises (SMEs).

- **Ideal for Learning and Research:** Enables students, educators, and researchers to perform complete circuit design workflows from schematic to simulation and PCB layout in a free and open-source environment.

Chapter 3

Problem Statement

The objective of this project is to design and implement digital integrated circuits utilizing the Subcircuit feature of eSim, develop accurate device models using the Model Editor tool, and conduct mixed-signal simulations through NGVeri. The digital models developed as part of this work will contribute to the enhancement of the eSim component library, thereby expanding its capabilities and applicability in both academic research and industrial design workflows.

3.1 Subcircuit Design

Digital and analog ICs are modeled as subcircuits in eSim based on manufacturer datasheets, incorporating internal schematics, electrical characteristics, and pin con- figurations. These subcircuits are integrated into eSim's library to enable accurate simulation and design of real-world components for academic and industrial appli- cations.

3.1.1 Approach

1. **Analysing Datasheets:** Comprehensive study of datasheets from multiple vendors is conducted to extract detailed internal circuit diagrams, truth tables, logic functionality, pin configurations, and functional block descriptions.
2. **Subcircuit Creation:** The extracted circuit logic is implemented using eSim's schematic editor, leveraging available components and device models from the internal library.
3. **Symbol Creation:** Custom schematic symbols are created based on the IC package type and accurate pin mapping to ensure proper connectivity within user-designed circuits.

4. **Test Circuit Design:** Validation circuits are developed to replicate standard test conditions specified in datasheets, enabling verification of subcircuit behavior.
5. **Simulation and Validation:** Simulations are performed using NgSpice to verify the functional accuracy of each subcircuit. Output waveforms are analyzed and compared with reference data provided in the datasheets to ensure fidelity.

3.2 Mixed-Signal Simulation using NGVeri

This stage involves leveraging eSim's NGVeri feature to perform mixed-signal simu- lation by integrating analog circuits with digital designs written in Verilog. NGVeri enables co-simulation of analog (NgSpice) and digital (Verilator) domains within a unified environment, supporting accurate analysis of mixed-signal systems.

3.2.1 Approach

1. **Verilog Design Implementation:** Digital modules are developed using Verilog, SystemVerilog, or TL-Verilog, depending on the design requirements and complexity.
2. **Functional Verification using Makerchip IDE:** Makerchip IDE is used for writing, debugging, and verifying digital logic to ensure correctness prior to integration with analog circuits.
3. **NGVeri Model Generation:** Verified Verilog or TL-Verilog designs are imported into NGVeri. If TL-Verilog is used, it is first converted into SystemVerilog using SandPiper SaaS. The design is then compiled with Verilator to generate a digital model compatible with mixed-signal simulation.
4. **Analog Circuit Design:** The analog components are designed using eSim's schematic editor via the KiCad interface, utilizing existing component models and custom subcircuits.
5. **Mixed-Signal Co-Simulation:** The analog and digital domains are integrated and simulated simultaneously using NGVeri. NgSpice handles the analog simulation while Verilator executes the digital logic. Simulation results are analyzed using eSim's plotting tools and NgSpice waveform viewer to validate system behavior.

3.3 Device Modeling using Model Editor

When SPICE models are not readily available, eSim's built-in Model Editor enables users to create custom device models. Users can manually define essential

device parameters, either extracted from datasheets or calculated using standard semicon- ductor equations. The Model Editor generates XML-based model files that can be directly integrated into the simulation environment. This capability provides enhanced flexibility, making it possible to simulate and analyze components that are not supported by predefined models or standard libraries.

1. **Parameter Extraction:** Key device parameters such as saturation current, ideality factor, junction capacitances, and breakdown voltage are extracted from datasheets or computed using standard analytical methods.
2. **Model File Creation:** The extracted parameters are manually input into eSim's Model Editor, which generates XML-based model files compatible with the simulation environment.
3. **Test Circuit Design:** Representative test circuits are developed to evaluate the electrical behavior of the modeled device under typical operating conditions.
4. **Simulation and Validation:** The test circuits are simulated using NgSpice, and the results are analyzed by comparing them against manufacturer datasheet specifications to ensure the model's accuracy and reliability.

Chapter 4

Digital IC's

4.1 CD4030 : Quad 2-input Exclusive-OR (XOR) gate

4.1.1 Description

The CD4030 is a CMOS integrated circuit that contains four independent two-input Exclusive-OR (XOR) gates, commonly referred to as a "Quad 2-Input XOR Gate." It is part of the 4000 series of logic ICs and is constructed using complementary MOS (CMOS) technology, which ensures low power consumption and high noise immunity.

Features:

- Quad 2-input XOR gates (Exclusive-OR logic)
- Wide supply voltage range: 3V to 18V
- Low power consumption (CMOS technology)
- High noise immunity
- Available in 14-pin DIP and other packages.

4.1.2 Pin Diagram

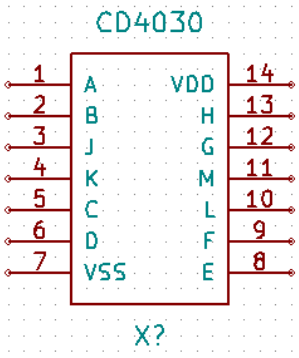

Figure 4.1: Pin Diagram of CD4030

4.1.3 Subcircuit

This subcircuit represents the internal structure of the CD4030 IC, implemented using CMOS logic. It consists of four identical 2-input XOR gates, each constructed using complementary pairs of pMOS and nMOS transistors.

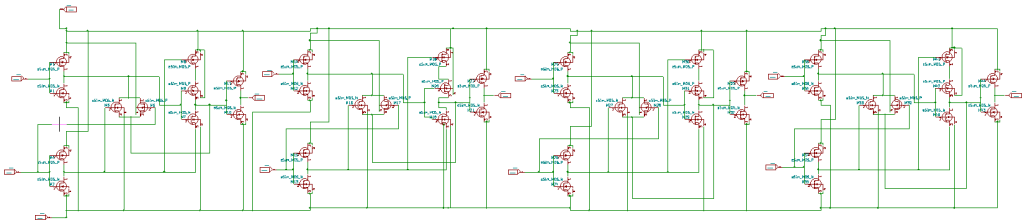

Figure 4.2: Subcircuit Diagram of CD4030

4.1.4 Test Circuit

This is the test circuit to verify the functionality of the CD4030 quad 2-input XOR gate IC . It uses two pulse voltage sources to provide binary test inputs A and B to one of the XOR gates (pins 1 and 2). The corresponding output (pin 3) is monitored using a voltage probe. A DC voltage source provides VDD. This setup allows the observation of the XOR logic behavior over time by visualizing the input-output relationship.

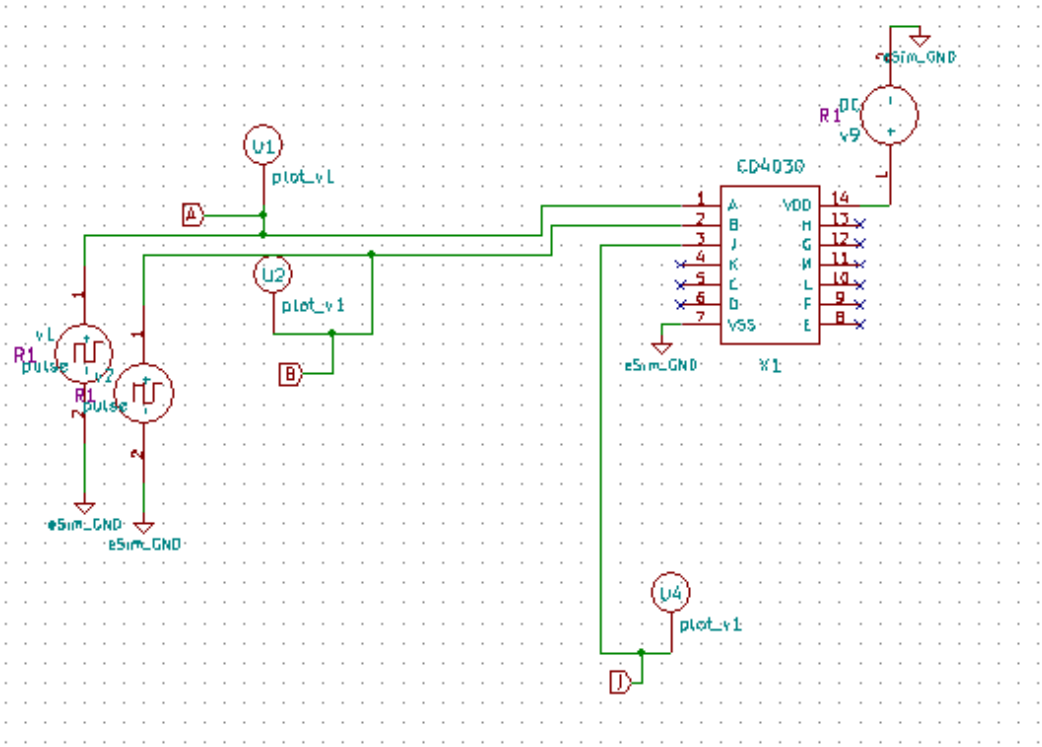

Figure 4.3: Test Circuit for CD4030

4.1.5 Output Waveforms

- When A = 1 (High) and B = 0 (Low), Output = 1
- When A = 0 and B = 1, Output = 1
- When A = B = 0 or A = B = 1, Output = 0

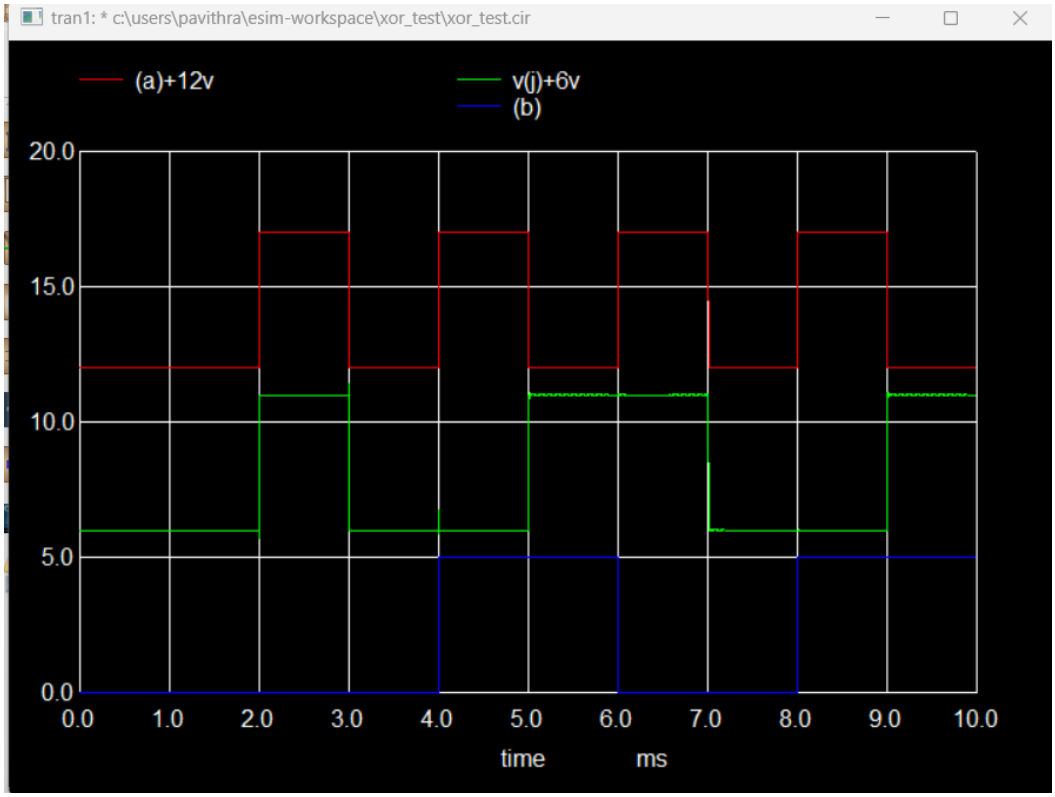

Figure 4.4: Output Waveform of CD4030

4.2 CD4049 : Hex Inverter Buffer

4.2.1 Description

The CD4049 is a CMOS integrated circuit that contains six independent inverter gates, commonly referred to as a "Hex Inverter." It is designed for use as a logic-level converter or general-purpose inverter in digital circuits.

Features:

- Hex inverter: contains six independent NOT gates.
- Wide operating voltage: 3V to 18V.
- High sink current: can drive two TTL loads.
- Allows input voltage higher than supply (V_{DD}).
- Package: Available in 16-pin Dual In-Line Package (DIP) and other package types.

4.2.2 Pin Diagram

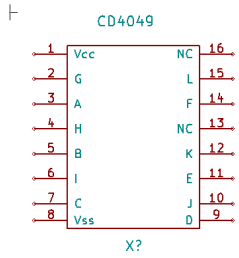

Figure 4.5: Pin Diagram of CD4049 (Top View)

4.2.3 Subcircuit

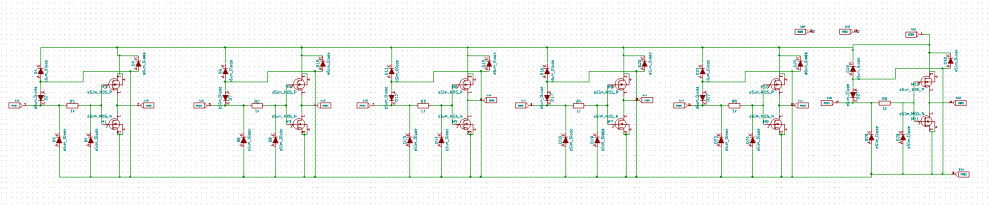

Figure 4.6: Subcircuit Diagram of SN54HC164

4.2.4 Test Circuit

The test circuit shown is used to verify the operation of the CD4049 IC, which is a hex inverter containing six NOT gates. In this setup, a pulse generator provides a square wave input to one of the inverter inputs (pin 3), while the corresponding output (pin 2) is monitored using a voltage probe to observe the waveform. The IC is powered using a DC source connected to VCC (pin 1) and grounded at VSS (pin 8). The expected behavior is that the output will be the logical inversion of the input signal, confirming the correct functionality of the CD4049 inverter gate.

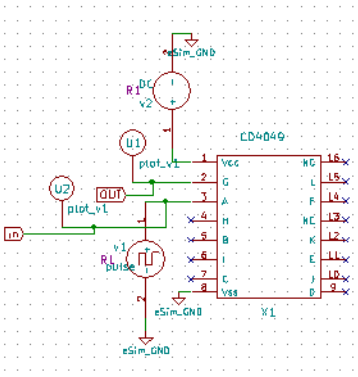

Figure 4.7: Test Circuit for CD4049

4.2.5 Waveforms

From the graph:

- The input is a square wave toggling between approximately 0V and 5V.
- The output is the inverted version of the input: when the input is high (5V), the output goes low (0V), and when the input is low (0V), the output goes high (5V).
- The waveform clearly demonstrates the inverting behavior of the CD4049 gate.

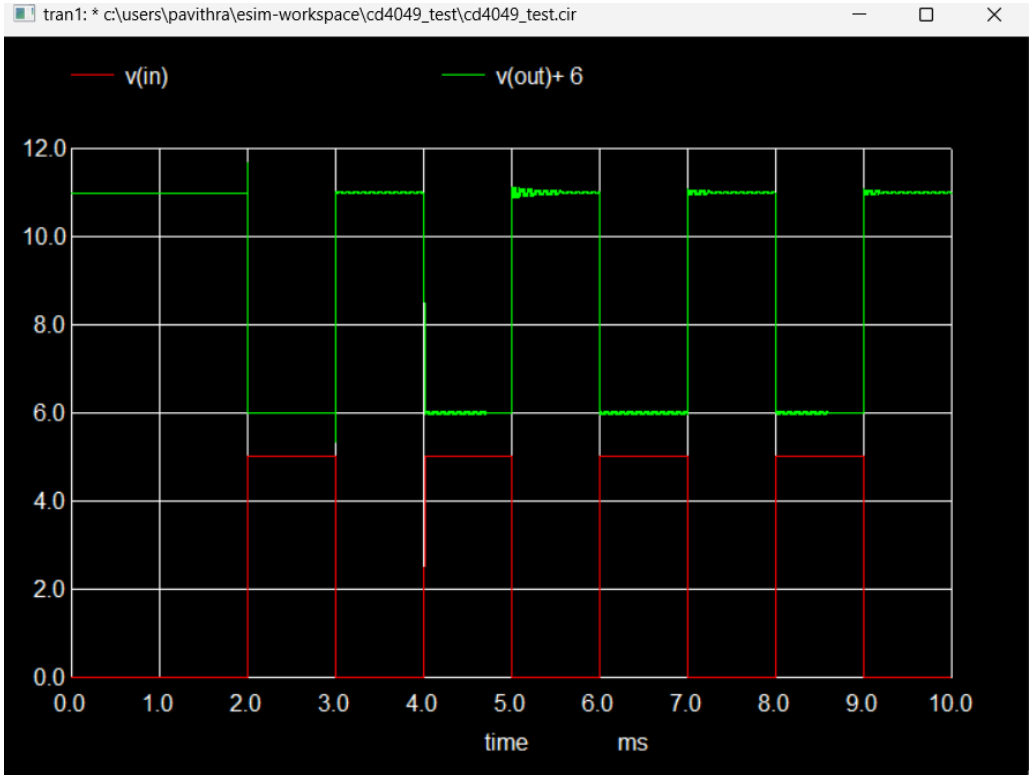

Figure 4.8: Output Waveform of CD4049

4.3 CD4098: Dual Monostable Multivibrator

4.3.1 Description

The CD4098 is a dual retriggerable and resettable monostable multivibrator IC designed for precision timing and pulse generation applications. It features two independent monostable circuits per chip, each capable of being retriggered or reset for flexible control over output pulse width. The duration of the output pulse is accurately set using external resistor and capacitor components, allowing for a wide range of timing intervals. Additionally, the CD4098 operates across a broad supply voltage range (3 V to 20 V), offers both true (Q) and inverted (Q) outputs, and is widely used for pulse shaping, time delay, and edge-conditioning in digital and analog electronic systems.

4.3.2 Pin Diagram

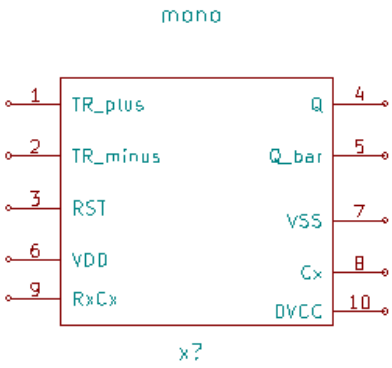

Figure 4.9: Pin Diagram of CD4098(1/2)

4.3.3 Subcircuit

This subcircuit represents one half of the dual CD4098 monostable multivibrator IC. Its primary function is to generate a precise output pulse in response to a trigger input, with the pulse width set by external resistor and capacitor components.

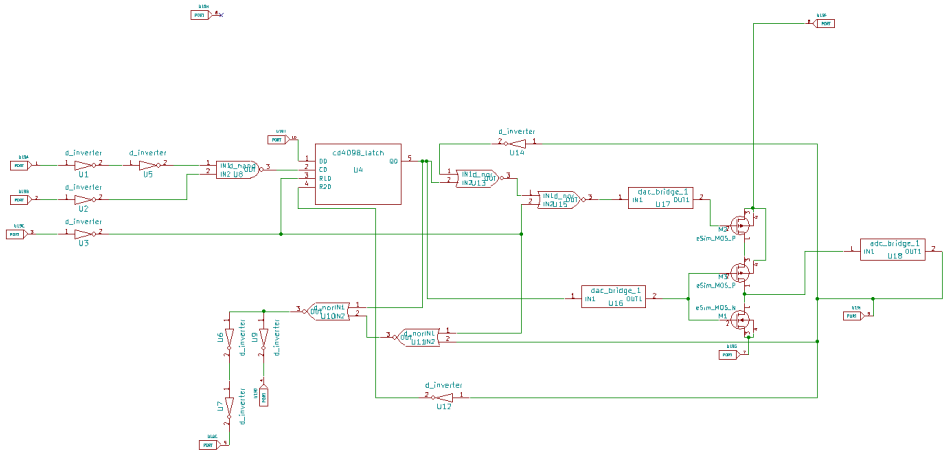

Figure 4.10: Subcircuit Diagram of CD4098(1/2)

4.3.4 Latch used in CD4098

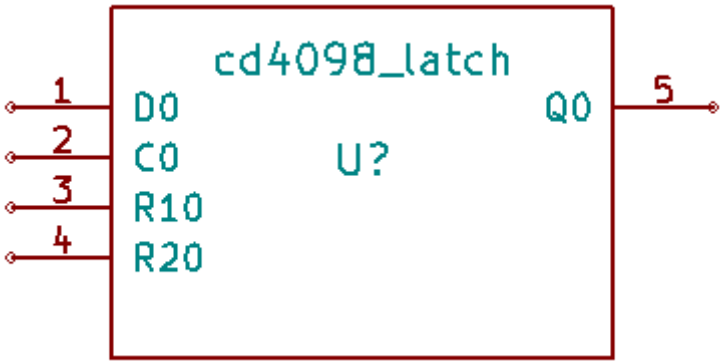

Figure 4.11: Latch used in Subcircuit

4.3.5 Verilog code

```
module CD4098_latch(
    input D,
    input C,
    input R1,
    input R2,
    output reg Q
);

always@(posedge R1 or posedge R2 or posedge C)
begin
    if(R1 || R2)
        Q <= 0;
    else
        Q <= D;
end

endmodule
```

4.3.6 Test Circuit for CD4098 latch

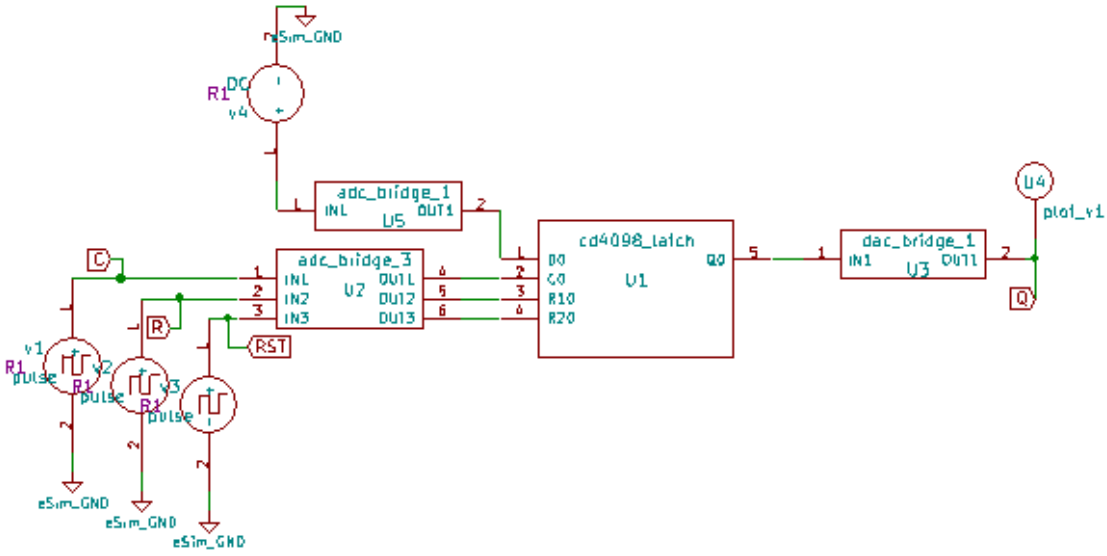

Figure 4.12: Test Circuit for CD4098 latch

4.3.7 Output Waveforms of CD4098 latch

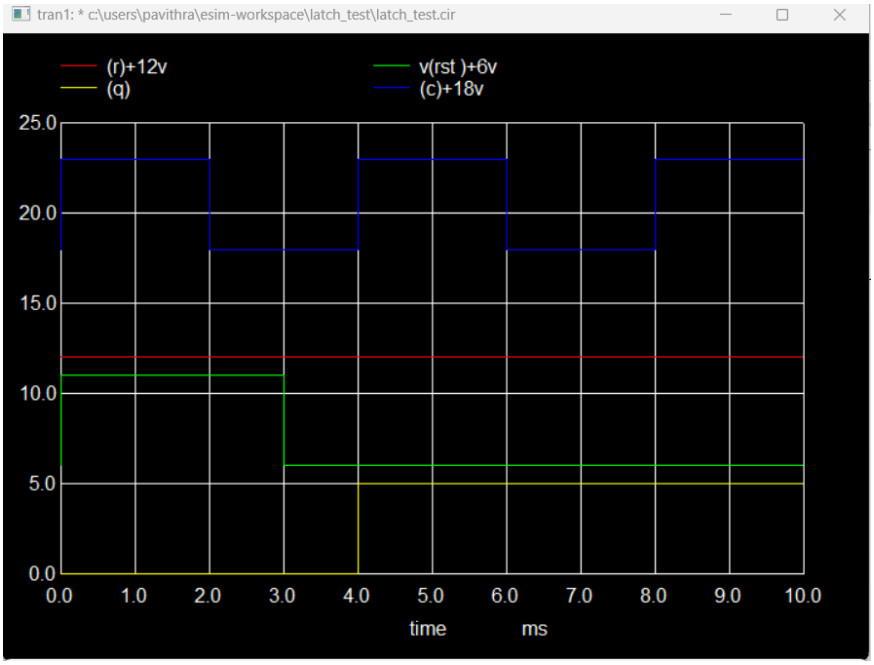

Figure 4.13: Output Waveform of CD4098 latch

4.3.8 Test Circuit

This test circuit demonstrates the operation of a single monostable multivibrator section of the CD4098. When a trigger pulse is applied, the circuit produces a single output pulse at the Q pin with a width determined by the connected timing resistor and capacitor. The reset input allows immediate termination of the output pulse, illustrating precise, retriggerable timing control using just one half of the dual CD4098 IC.

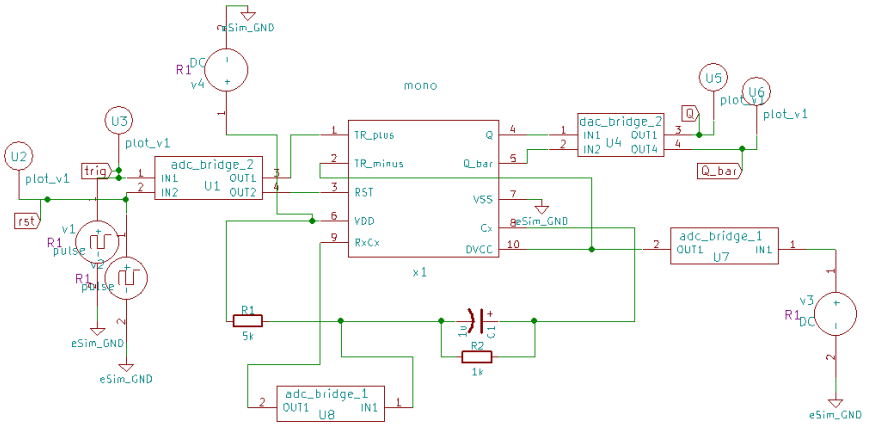

Figure 4.14: Test Circuit for one of the 2 monostable multivibrators

4.3.9 Waveforms

This waveform shows the operation of the CD4098 monostable multivibrator. When a trigger pulse occurs (yellow), the Q output (green) goes high and Q (red) goes low for a fixed period before returning to their original states. The reset signal (blue) can immediately terminate the output pulse, resetting both outputs regardless of timing.

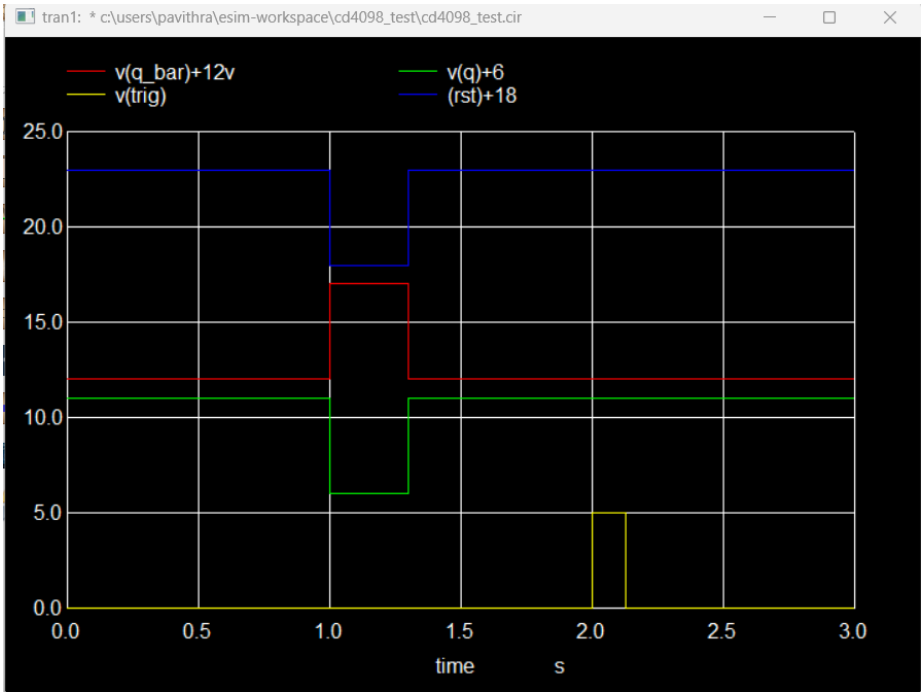

Figure 4.15: Output Waveform of one of the two monostable multivibrators

4.4 MC14076B : 4 bit Register using D-Flip Flop

4.4.1 Description

The MC14076B is a digital integrated circuit designed as a 4-bit register, consisting of four D-type flip-flops operating from a common clock. This IC is used for the storage and transfer of digital data, allowing each flip-flop to store one bit that can be set or cleared synchronously with the clock signal. It features three-state outputs for bus-oriented applications, as well as an asynchronous master reset to clear all stored data. The MC14076B is primarily used in digital systems for buffering, temporary data storage, and parallel data transfer tasks.

Features:

- High noise immunity and low power consumption due to CMOS technology
- Compatible with standard TTL logic levels
- Wide operating voltage range: 3V to 15V
- Individually addressable flip-flops for flexible data handling

4.4.2 Pin Diagram

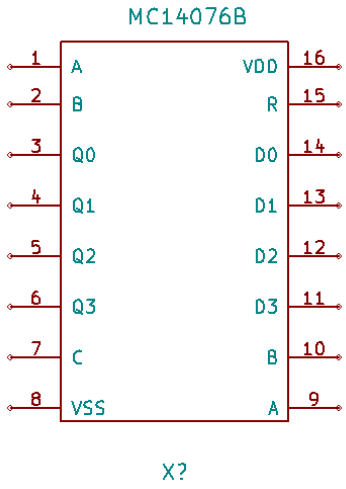

Figure 4.16: Pin Diagram of MC14076B

4.4.3 Subcircuit

The subcircuit of the MC14076B represents the internal logic of a 4-bit register, where four D-type flip-flops are interconnected to store and transfer digital data synchronously with a common clock. Each flip-flop in the subcircuit has its data input (D), clock input, output (Q), and asynchronous master reset, providing the ability to load, clear, and hold binary information in digital systems. The subcircuit also features additional logic for three-state outputs, allowing the stored data to interface directly with system data buses, making the MC14076B suitable for buffering and parallel data transfer applications in digital circuits.

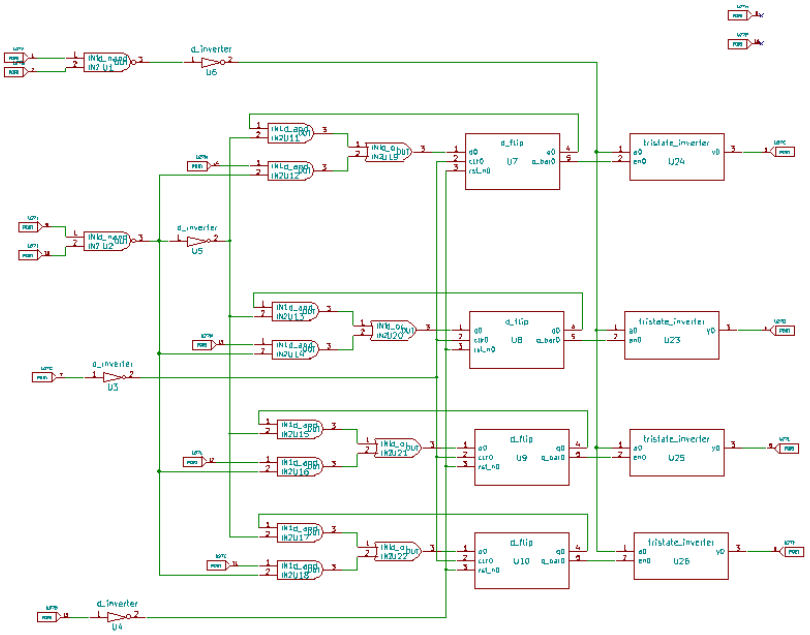

Figure 4.17: Subcircuit of MC14076B

4.4.4 Test Circuit

This test circuit demonstrates the operation of the MC14076B 4-bit register by capturing and storing parallel digital inputs on the rising edge of the clock signal. The output lines display the stored data, which can be asynchronously cleared using the master reset.

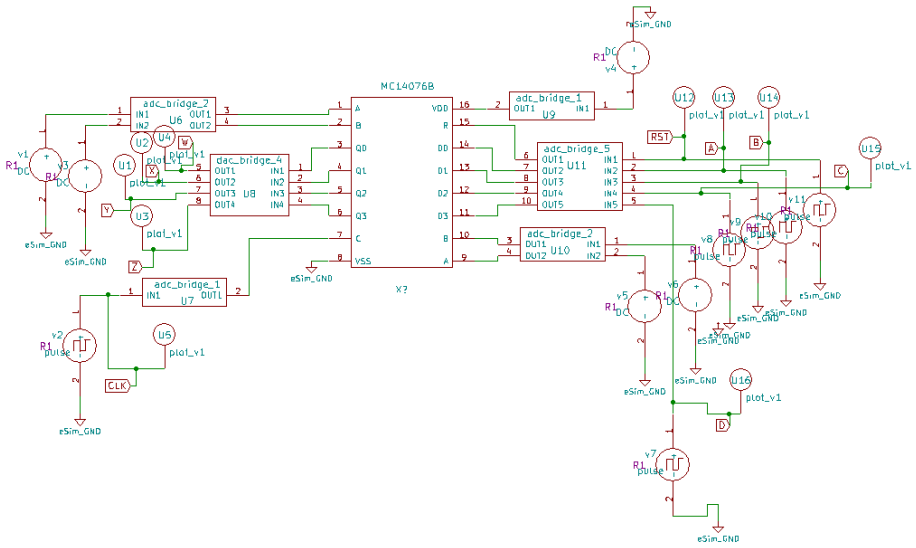

Figure 4.18: Test Circuit for MC14076B

4.4.5 Waveforms

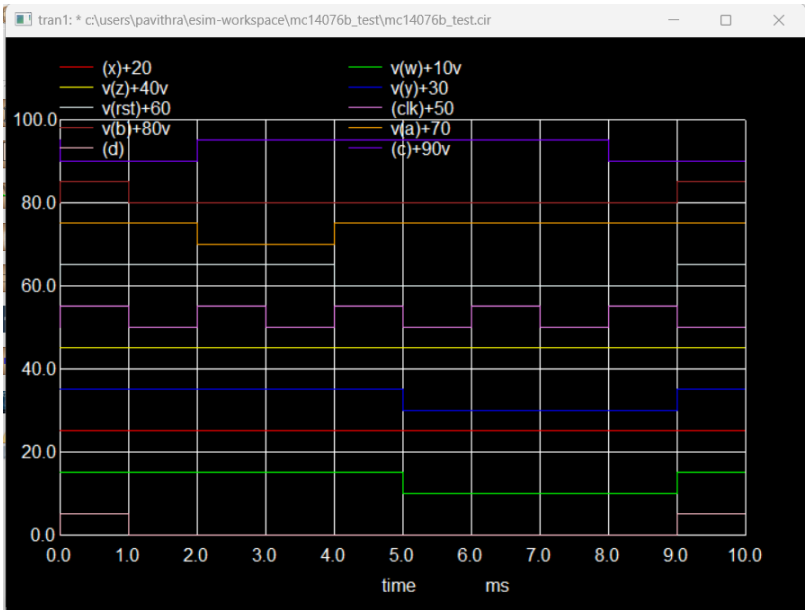

Figure 4.19: Output Waveform of MC14076B

The waveform illustrates:

- Each register output captures and holds its input value on the clock edge, showing correct synchronous data storage.
- The reset signal instantly clears all outputs, demonstrating proper asynchronous reset functionality.
- Outputs remain stable between clock or reset events, confirming correct digital register operation.

4.5 MC14016B : Quad bilateral analog switch IC

4.5.1 Description:

The MC14016B is a quad bilateral analog switch IC designed to route or multiplex both analog and digital signals in electronic systems. It includes four independent switches that can pass signals in either direction, making it highly versatile for applications such as signal gating, multiplexing, and analog/digital switching

Key features:

- **Handles Analog and Digital Signals:** Designed to pass both analog and digital signals, making it useful in mixed-signal systems.
- **Wide Operating Voltage Range:** Operates typically from 3 V to 18 V, compatible with various supply levels.
- **Logic Control:** Switches are controlled by standard logic inputs, allowing easy integration with digital control circuitry.
- **Low On-Resistance:** Offers minimal signal loss and distortion when passing signals, suitable for audio, data, and sensor applications.

4.5.2 Pin Diagram of MC14016B(1/4)

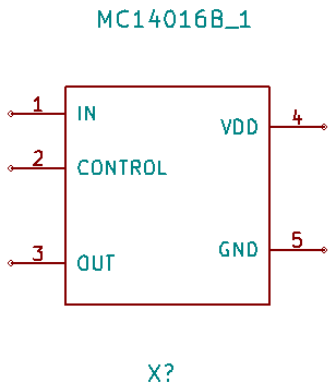

Figure 4.20: Pin Diagram of MC14016B

4.5.3 Subcircuit of MC14016B(1/4)

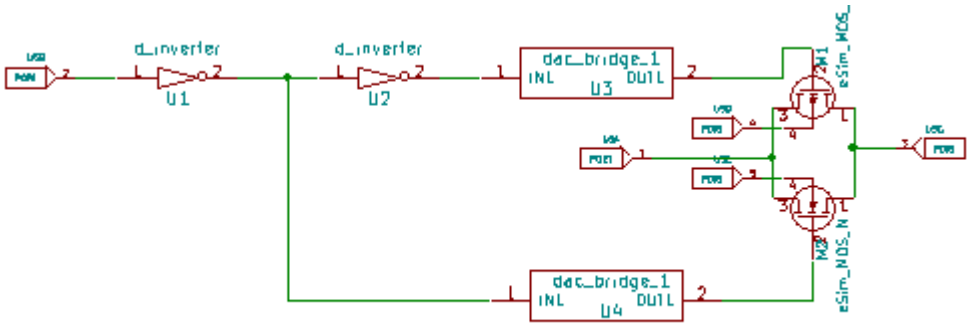

Figure 4.21: Subcircuit of one MC14016B

4.5.4 Test Circuit of MC14016B(1/4)

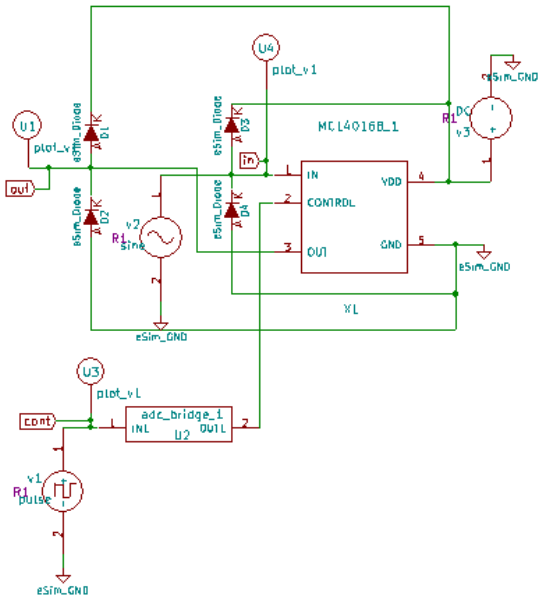

Figure 4.22: Test Circuit of one MC14016B

4.5.5 Waveforms (1/4)

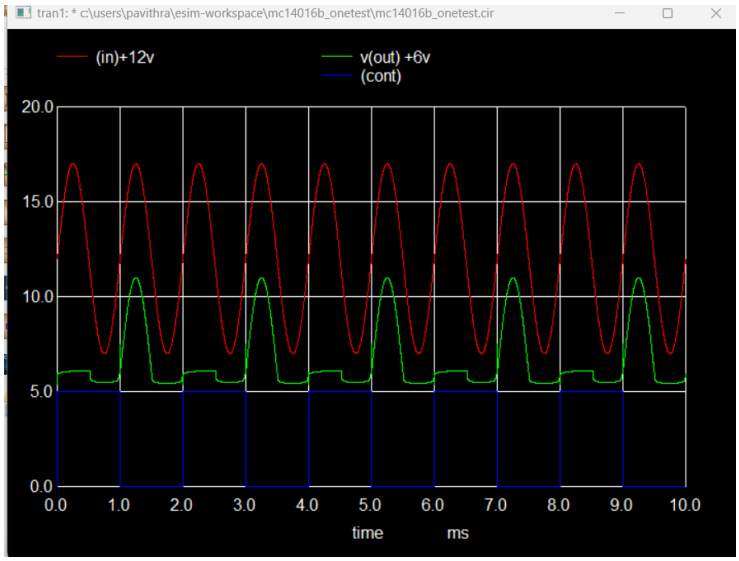

Figure 4.23: Waveform of one MC14016B

4.5.6 Pin Diagram

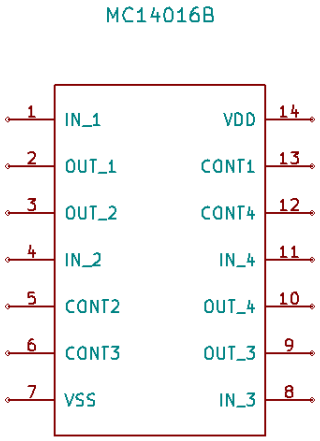

Figure 4.24: Pin Diagram of MC14016B

4.5.7 Subcircuit

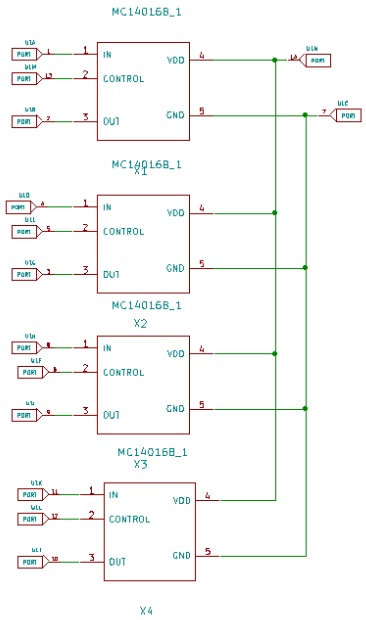

Figure 4.25: Subcircuit of Quad bilateral analog switch

4.5.8 Test Circuit

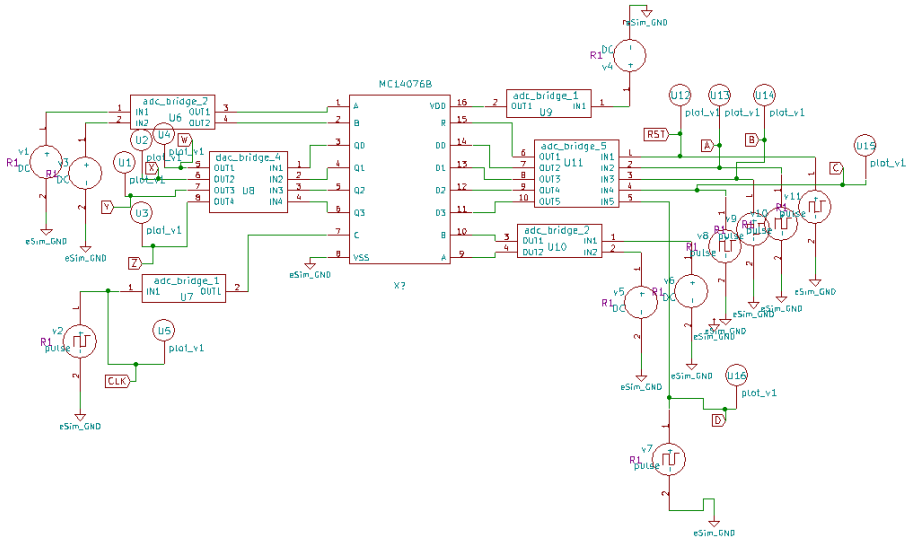

Figure 4.26: Test Circuit for MC14016B

4.5.9 Waveforms

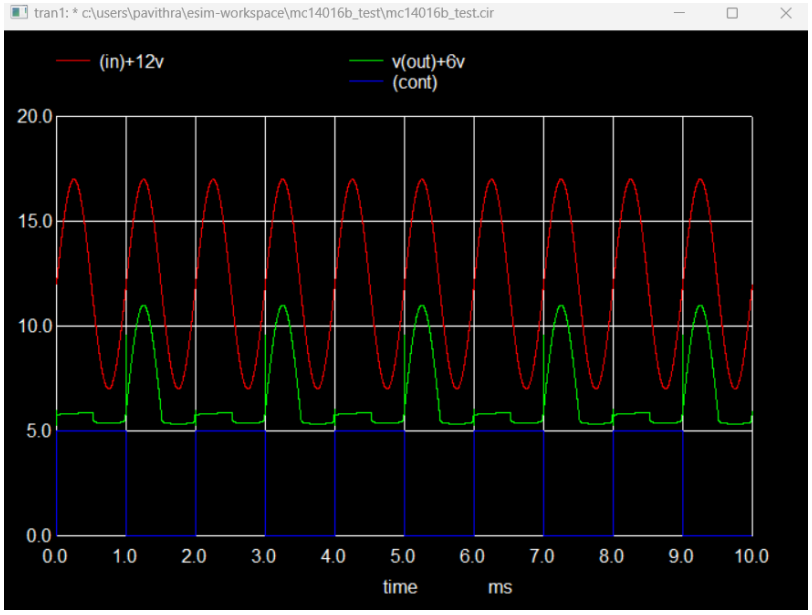

Figure 4.27: Output Waveform of Quad bilateral analog switch

The waveform shows the operation of the MC14016B quad bilateral analog switch. The input signal passes through to the output only when the corresponding control signal is active, resulting in output pulses that match the input during these intervals. When the control is low, the output remains steady, clearly illustrating correct signal routing and isolation behavior for the analog switch IC.

Chapter 5

Analog IC's

5.1 LM3900: Quad Norton Amplifier

5.1.1 Description

The LM3900 is a quad Norton operational amplifier IC, meaning it contains four independent amplifiers in a single package. Unlike standard op-amps, the LM3900 is specifically designed for single-supply operation and can handle input and output voltages very close to ground, making it ideal for low-voltage and single-supply analog circuits.

Features:

- **Single or Dual Supply Operation:** Accepts a wide supply voltage range, typically from 4V to 32V (single supply) or ±2V to ±16V (dual supply), making it highly versatile for different power setups.
- **High Open-Loop Gain & Wide Bandwidth:** Provides a typical open-loop voltage gain of 70dB and a unity-gain bandwidth up to 2.5MHz, suitable for precision amplification.
- **Low Input Bias Current:** Typical input bias current is around 30nA, enabling accurate signal amplification from high-impedance sources.
- **Large Output Voltage Swing:** Can deliver output voltages nearly spanning the entire supply range, useful for single-supply analog circuits.

5.1.2 Pin Diagram

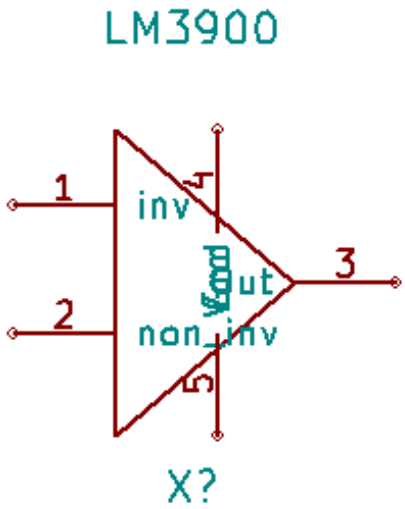

Figure 5.1: Pin Diagram of LM13700MX

5.1.3 Subcircuit

This subcircuit models a single Norton operational amplifier section within the LM3900 IC, showing its core transistor-level building blocks. It processes input currents rather than voltages and enables wide input and output voltage swings relative to ground, making the LM3900 ideal for single-supply analog operations. The arrangement supports high gain, fast response, and low input bias current for versatile signal amplification.

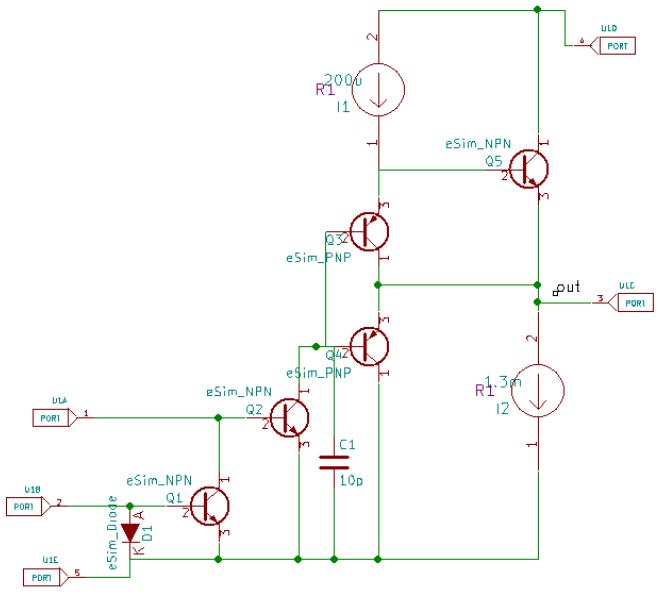

Figure 5.2: Subcircuit Representation single Norton Op-Amp

5.1.4 Test Circuit

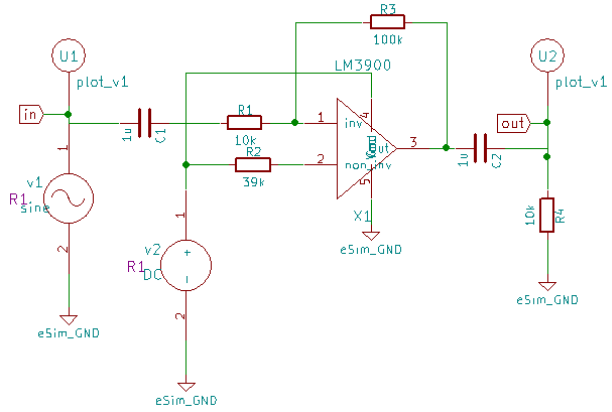

Figure 5.3: LM3900 Configured as Non-inverting Amplifier

5.1.5 Waveforms

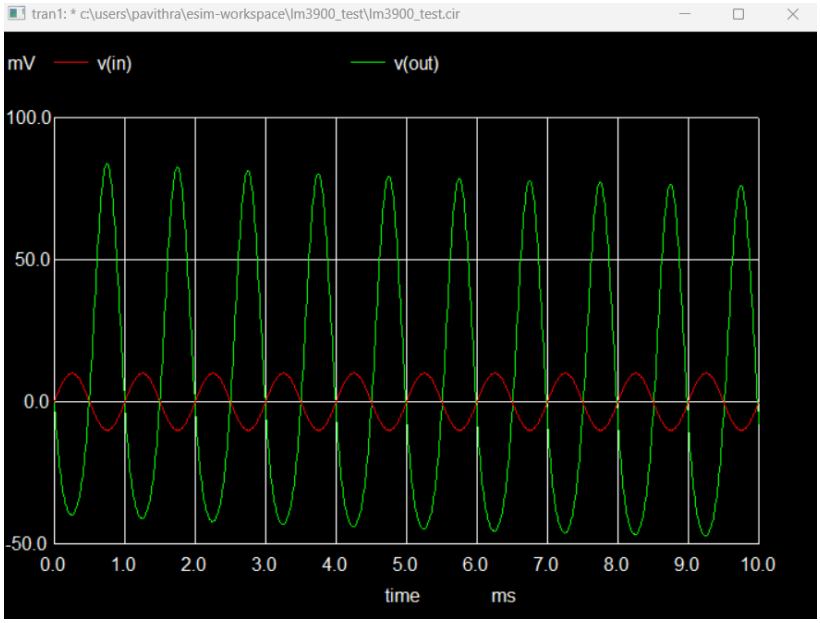

Figure 5.4: Input and Output Signals of LM3900

The waveform shows the operation of a non-inverting amplifier built with the LM3900. The output signal (green) is a sinusoidal wave with much greater amplitude than the input (red), indicating correct amplification and preserved phase. Both signals maintain their shape without distortion, confirming proper linear and in-phase operation of the circuit.

5.2 TA7642 : Monolithic AM Radio IC

5.2.1 Description

The TA7642 is a highly compact, single-chip AM radio integrated circuit housed in a 3-pin TO-92 package designed for low-voltage, battery-operated receivers. It combines RF amplification and detection, operating with minimal external components and a supply as low as 1.2V. Its very low quiescent current and small size make it ideal for building portable AM radios and simple signal-detection circuits

Features:

- **Single-chip AM radio IC:** Comes in a compact 3-pin TO-92 package.

- **Integrated RF amplifier and detector:** Simplifies AM radio circuit design.
- **Low voltage operation:** Can function from as little as 1.2V, making it ideal for battery-powered devices.
- **Low power consumption:** Very low quiescent current, suitable for portable and miniature radios.
- **Minimal external components required:** Enables easy and compact circuit designs.

5.2.2 Pin Diagram

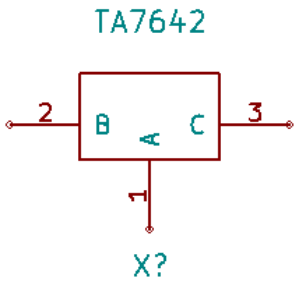

Figure 5.5: Pin Diagram of TA7642

5.2.3 Subcircuit

The internal configuration of the TA7642 can be represented as a subcircuit as shown below.

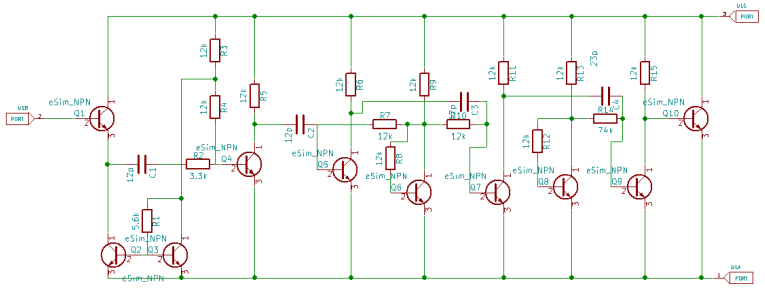

Figure 5.6: Subcircuit Diagram of TA7642

5.2.4 Test Circuit

The following test setup demonstrates the working of TA7642 in a practical configuration.

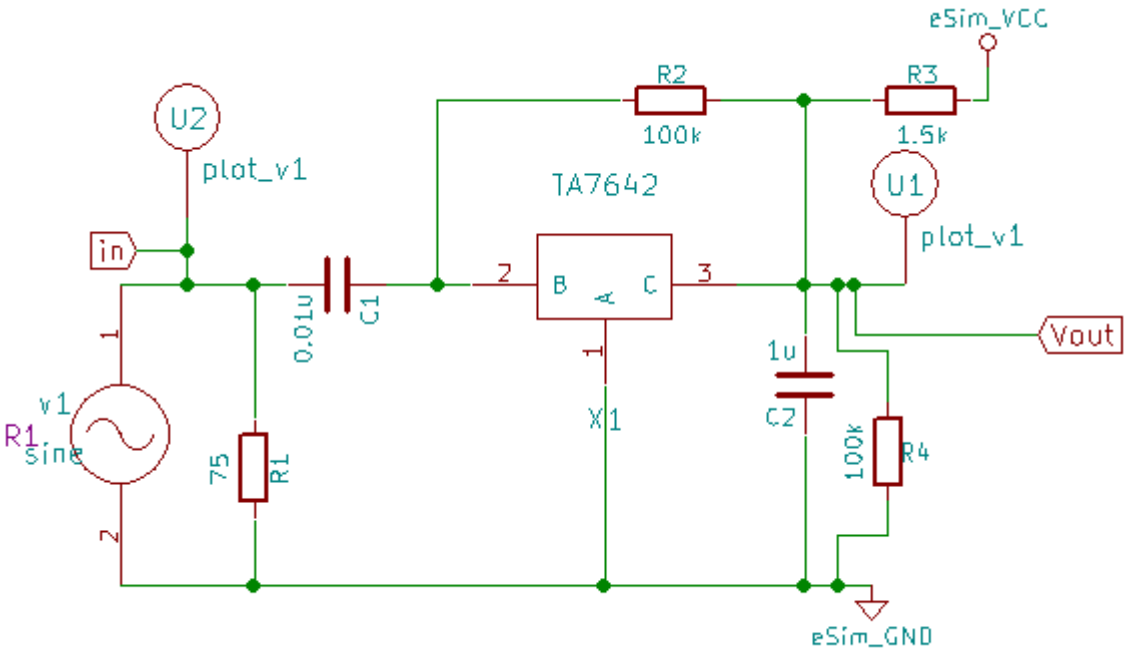

Figure 5.7: Test Circuit for TA7642

5.2.5 Waveforms

The input waveform corresponding to the test circuit is shown below.

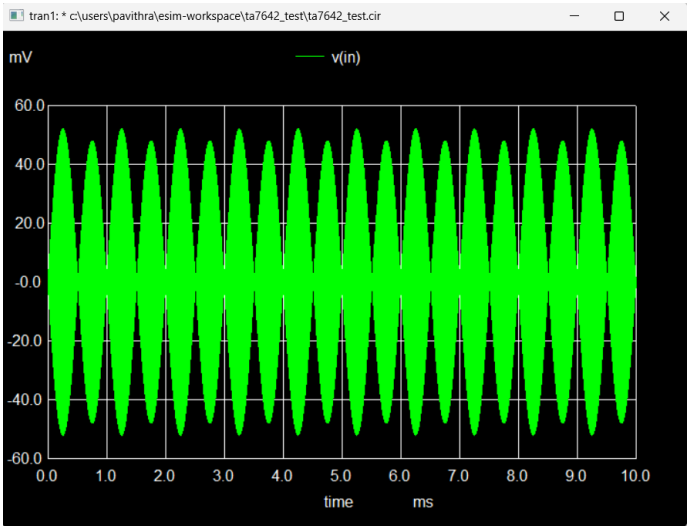

Figure 5.8: Input Waveforms of the Test Circuit (AM signal)

The output waveform corresponding to the test circuit is shown below.

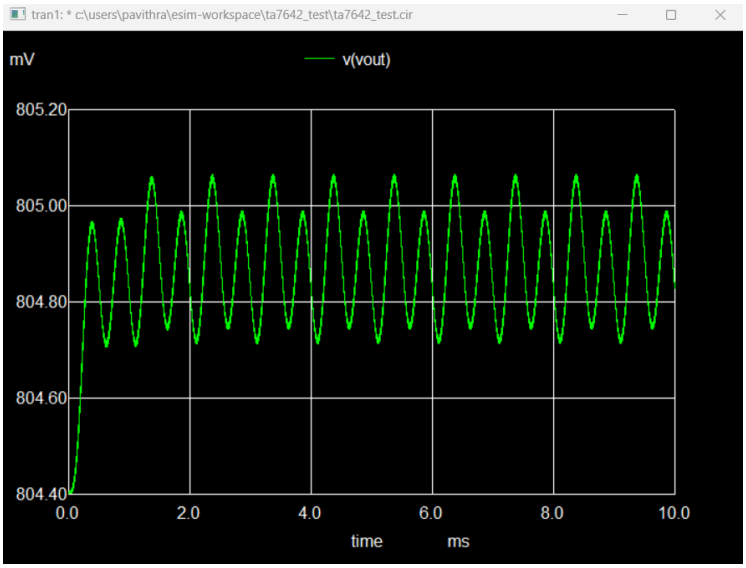

Figure 5.9: Output Waveforms of the Test Circuit

Comparison of obtained output with that of envelope detector

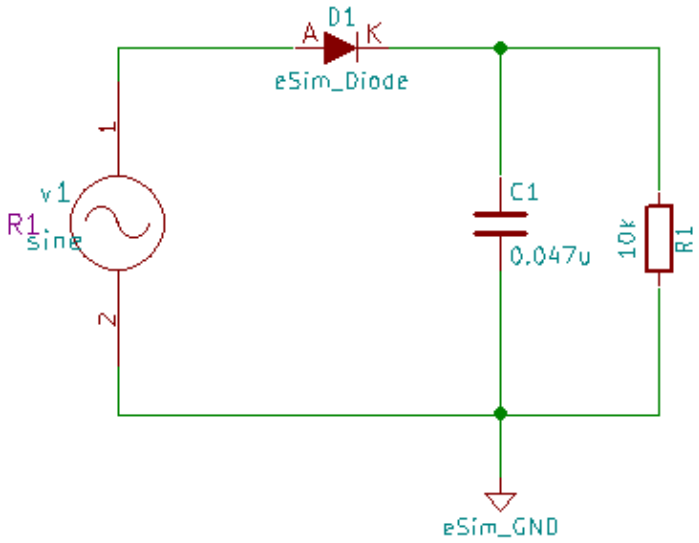

Figure 5.10: Envelope detector with same AM signal as input

Waveforms

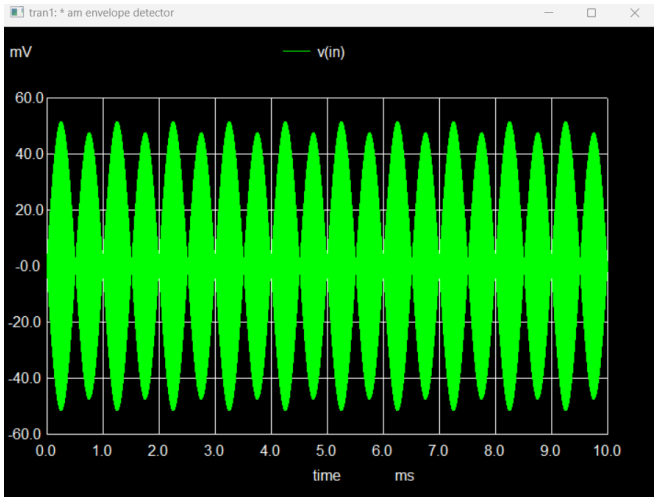

Figure 5.11: Input Waveforms of the envelope detector Circuit

The output waveform corresponding to the envelope detector circuit is shown below.

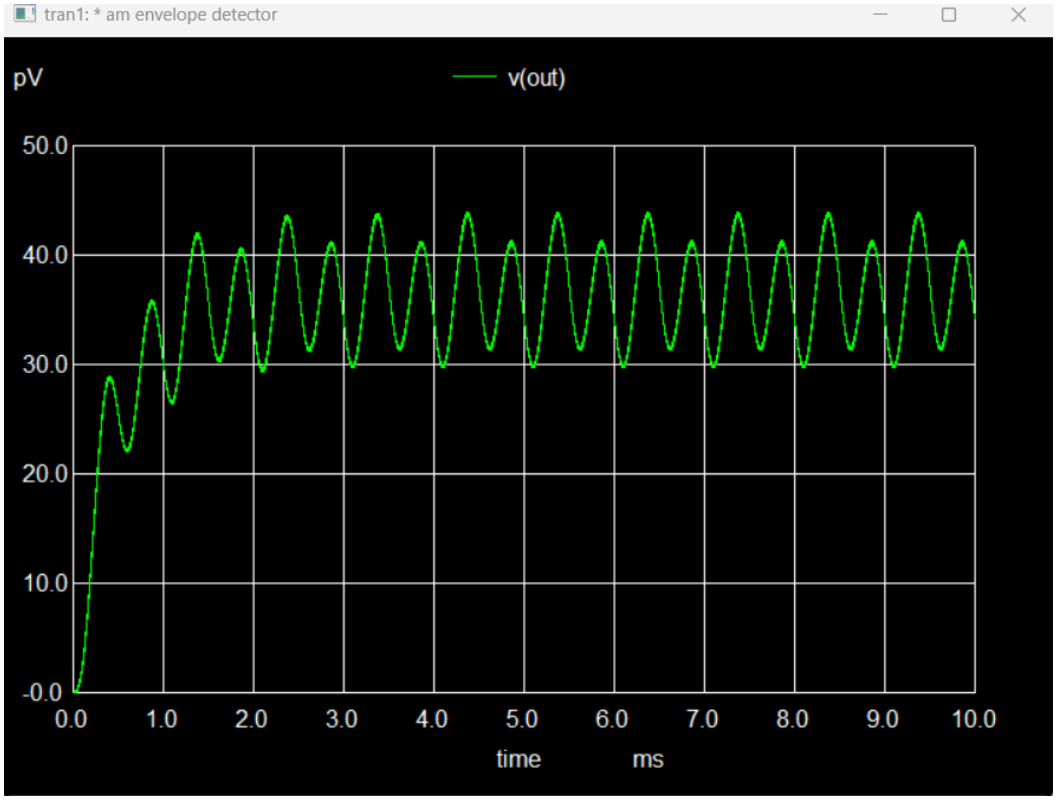

Figure 5.12: Output Waveforms of the envelope detector Circuit

5.3 SN74LVC1G3157 : SPDT Analog Switch

5.3.1 Description

The SN74LVC1G3157 is a single-pole, double-throw (SPDT) analog switch IC designed to route analog or digital signals in electronic systems. It operates over a supply voltage range of 1.65V to 5.5V and features low on-resistance, high speed, and rail-to-rail signal handling. This IC is widely used for signal gating, multiplexing, chopping, and modulation/demodulation applications. Its ability to transmit signals with amplitudes up to the supply voltage in either direction, controlled by standard logic inputs, makes it especially suitable for mixed-signal circuits requiring flexibility and reliable switching performance

Features:

- **SPDT Analog Switch:** Provides single-pole, double-throw switching controlled by digital logic, suitable for passing both analog and digital signals in either direction.
- **Low On-Resistance and High Speed:** Features typical ON-state resistance of 6 ohm and operates at high speed with an operating frequency up to 340MHz.
- **Wide Operating Range and Robustness:** Supports supply voltages from 1.65V to 5.5V, offers rail-to-rail signal handling, ESD protection, and break-before-make switching for reliable performance.

5.3.2 Pin Diagram

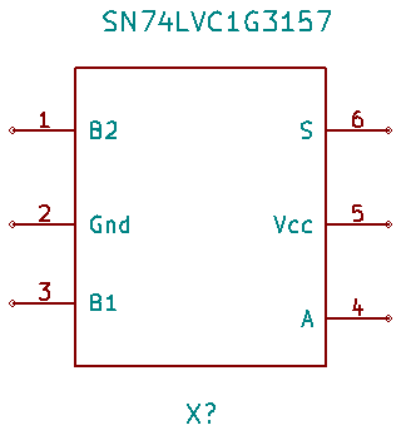

Figure 5.13: Pin diagram of SN74LVC1G3157

5.3.3 Subcircuit

This subcircuit represents the internal logic of the SN74LVC1G3157 SPDT analog switch. It models the switching mechanism that routes one input to either of two outputs under digital control, supporting both analog and digital signals. The design ensures low on-resistance, fast switching, and bidirectional signal flow, reflecting the key operational features of the actual IC.

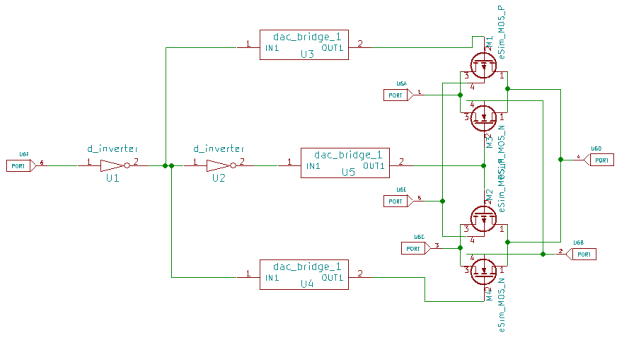

Figure 5.14: Subcircuit of SN74LVC1G3157

5.3.4 Test Circuit

The following test setup demonstrates the working of SN74LVC1G3157 in a practical configuration.

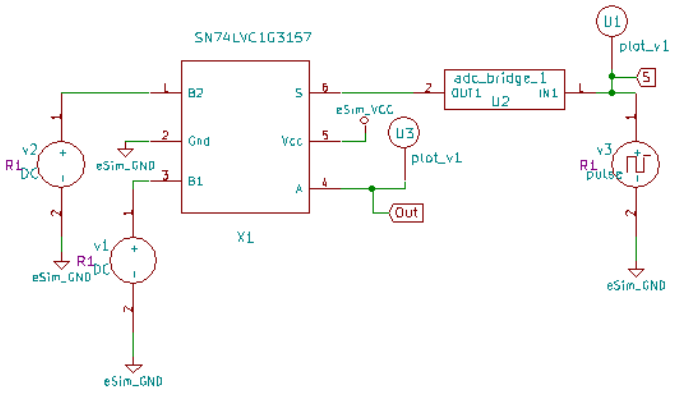

Figure 5.15: Test circuit of Analog Switch

5.3.5 Waveform

The SN74LVC1G3157 analog switch connects the output to either the 1V or 3V input by changing the control (select) signal: when the control is set to one state, it routes the 1V input to the output; when switched, it connects the 3V input instead.

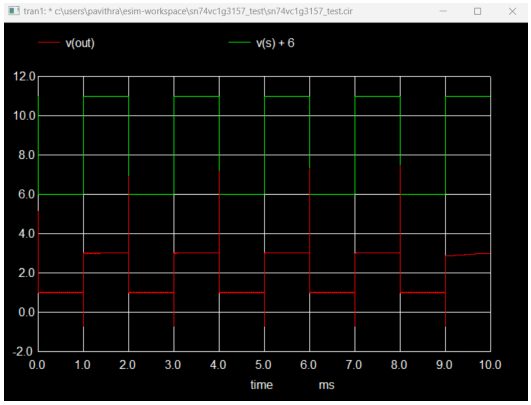

Figure 5.16: Input and Output waveforms of Analog Switch

The SN74LVC1G3157 analog switch connects the output to either the 1 V or 3 V input by changing the control (select) signal: when the control is set to one state, it routes the 1 V input to the output; when switched, it connects the 3 V input instead.

5.4 MC3340 : Voltage controlled electronic Attenuator

5.4.1 Description

The MC3340 is an analog integrated circuit designed as a voltage-controlled electronic attenuator, commonly used for audio volume control and other analog signal level adjustments. It enables smooth, continuous attenuation of input signals in response to a control voltage, making it ideal for automated or remote-controlled audio devices. With a simple application circuit, the MC3340 delivers low distortion, wide attenuation range, and high linearity, making it a preferred choice in both consumer and professional audio equipment.

Features:

- **Voltage-Controlled Analog Attenuator:** Offers up to 80dB of smooth, continuous attenuation for frequencies up to 1MHz, controlled by an external DC voltage or variable resistor.
- **Low Distortion:** Maintains low total harmonic distortion, typically less than 1% at up to 15dB attenuation and less than 3% up to 40dB attenuation.
- **Ideal for Audio and Instrumentation:** Commonly used in remote-controlled audio volume circuits and dynamic range control due to its wide attenuation range, compact 8-pin package, and high linearity.

5.4.2 Pin Diagram

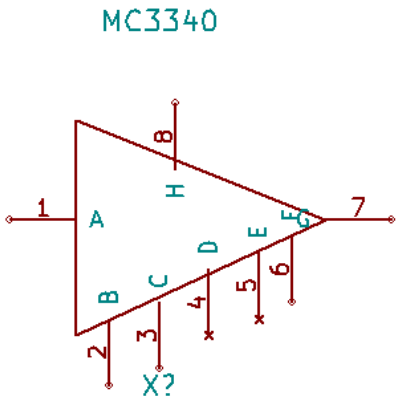

Figure 5.17: Pin Diagram of MC3340

5.4.3 Subcircuit

This subcircuit models the core of the MC3340, a voltage-controlled analog attenuator designed for smooth, linear adjustment of audio or signal levels. It electronically varies signal attenuation in response to a control voltage, enabling remote or automatic volume and amplitude control in analog circuits. The design ensures low distortion and a wide dynamic range, making it ideal for audio and instrumentation applications.

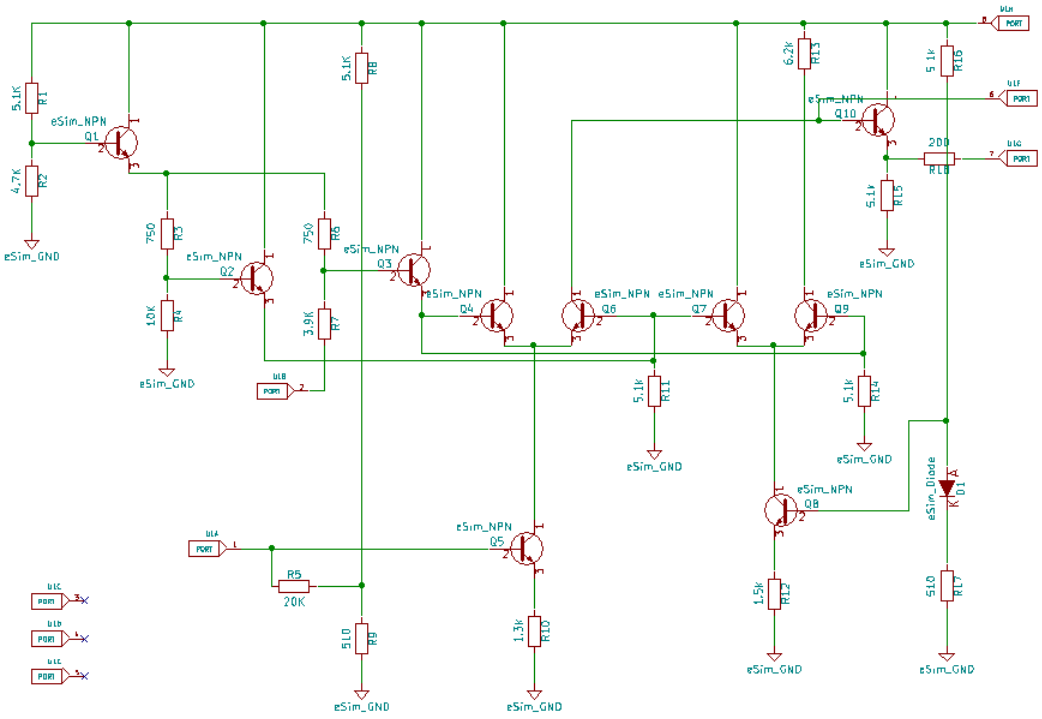

Figure 5.18: Subcircuit of MC3340

5.4.4 Test Circuit

The following test setup demonstrates the working of MC3340 in a practical configuration.

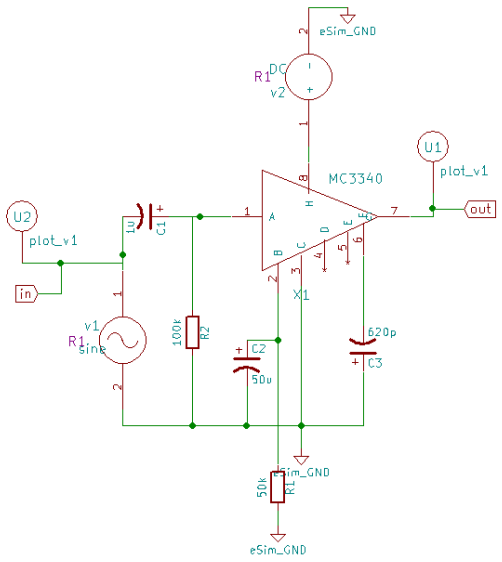

Figure 5.19: Test Circuit of MC3340

5.4.5 Waveform

- The input waveform is a sinusoidal signal applied to the attenuator; the output waveform is the same sine wave but with noticeably reduced amplitude, illustrating the effect of attenuation.
- The degree of attenuation (output signal level) is directly controlled by the DC voltage applied to the MC3340's control input—raising or lowering this voltage smoothly increases or decreases the output amplitude.
- This behavior shows that the MC3340 provides precise, linear, and low-distortion volume or signal level control in analog circuits by varying a simple control voltage.

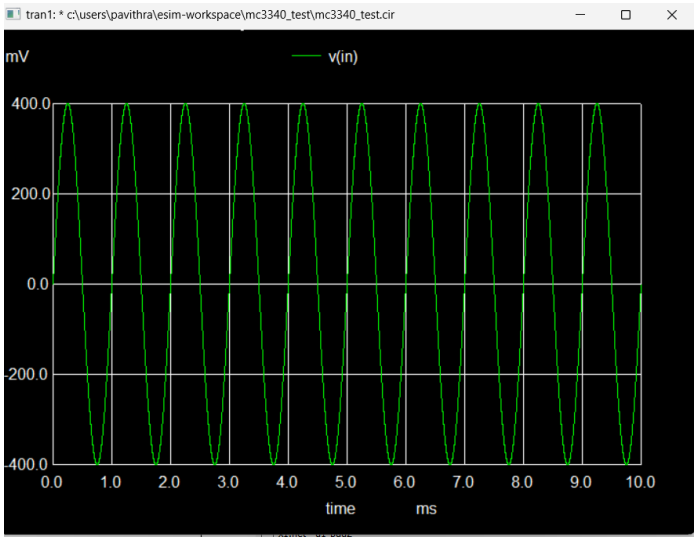

Figure 5.20: Input waveform of the test circuit

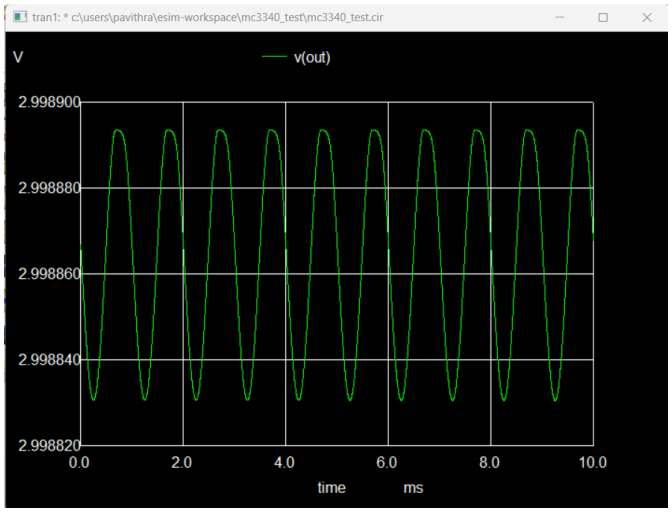

Figure 5.21: Output waveform of the test circuit

Chapter 6

Mixed-Signal Simulation

The Mixed-Signal Simulation capability in eSim enables the co-simulation of analog and digital domains by integrating SPICE-based analog circuits with Verilog-based digital logic. This is facilitated through the NgVeri interface, which combines the simulation strengths of NgSpice for analog behavior and Verilator for digital logic. By allowing simultaneous simulation of both domains, mixed-signal co-simulation supports comprehensive analysis of systems where analog and digital components in- teract—such as ADCs, DACs, and sensor interfaces—ensuring accurate and efficient system-level verification.

6.1 AM29112 : Microprogram Sequencer

6.1.1 Description

The AM29112 is a high-performance, interruptible microprogram sequencer developed by Advanced Micro Devices (AMD). Designed as an 8-bit slice component, it is intended for use in very high-speed microprogrammed systems and optimized to work with advanced arithmetic logic units (ALUs) and processing components. Key features include support for microprogram-level interrupts (both maskable and unmaskable), a 33-level deep on-chip stack for efficient subroutine and interrupt handling, powerful loop and addressing controls, and the ability to cascade for wider data paths. The AM29112 is commonly used to manage control flow in pipelined and microprogrammed computing architectures, operating at speeds up to 10 MHz

Key features:

- Supports microprogram-level interrupts, including maskable and non-maskable types, for enhanced control flow flexibility.
- Built-in 33-level microstack for efficient subroutine and interrupt nesting.

- High-speed operation up to 10MHz, suitable for advanced microprogrammed control units.

6.1.2 Block Diagram

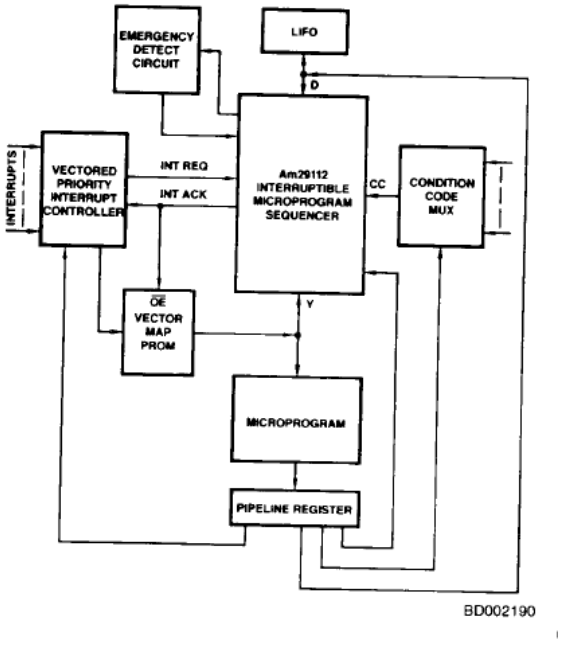

Figure 6.1: Block Diagram of AM29112

6.1.3 Verilog Code

The Verilog code below implements AM29112.

```
module AM29112(

    inout [7:0] D,


    output [7:0] Y,


    input [4:0] I,
    input [1:0] MODE,
```

```
    input [3:0] M,


    input CP,
    input RST,
    input HOLD,
    input CC,
    input CCEN,
    input POL,
    input UINTR,
    input MINTR,
    input INTD,
    input LSS,


    inout ACIO,
    inout PCIO,
    inout CIO,
    inout CZIO,


    output reg MINTA,
    output reg STKERR
);


    reg [7:0] PC;
    reg [7:0] stack [0:7];
    reg [2:0] SP;
    reg [7:0] D_out;
    reg D_drive;


    wire [7:0] pc_plus_1 = PC + 1;
    wire condition_met;
    wire interrupt_req;
    wire Y_drive;


    reg pc_load, pc_increment;
    reg stack_push, stack_pop;
    reg branch_enable, call_enable, ret_enable;
    reg [7:0] next_addr;


    localparam INST_CONTINUE    = 5'b00000;
```

```
localparam INST_JUMP        = 5'b00001;
localparam INST_CALL        = 5'b00010;
localparam INST_RETURN      = 5'b00011;
localparam INST_COND_JUMP   = 5'b00100;
localparam INST_MULTIWAY    = 5'b01000;


assign condition_met = CCEN ? (POL ? ~CC : CC) : 1'b1;


assign interrupt_req = UINTR || (MINTR && !INTD);


assign Y_drive = !HOLD;
assign Y = Y_drive ? PC : 8'bz;


assign D = D_drive ? D_out : 8'bz;


always @(*) begin

    pc_load = 0;
    pc_increment = 0;
    stack_push = 0;
    stack_pop = 0;
    branch_enable = 0;
    call_enable = 0;
    ret_enable = 0;
    next_addr = 8'b0;
    D_drive = 0;
    D_out = 8'b0;


    case (I)
        INST_CONTINUE: begin
            pc_increment = 1;
        end

        INST_JUMP: begin
            pc_load = 1;
            next_addr = D;
        end

        INST_CALL: begin
            call_enable = 1;
```

```
            stack_push = 1;
            pc_load = 1;
            next_addr = D;
        end

        INST_RETURN: begin
            ret_enable = 1;
            stack_pop = 1;
            pc_load = 1;
            next_addr = (SP > 0) ? stack[SP-1] : 8'b0;
        end

        INST_COND_JUMP: begin
            if (condition_met) begin
                pc_load = 1;
                next_addr = D;
            end else begin
                pc_increment = 1;
            end
        end

        INST_MULTIWAY: begin

            pc_load = 1;
            next_addr = D;
        end

        default: begin
            pc_increment = 1;
        end
    endcase
end


always @(posedge CP or posedge RST) begin
    integer i;
    if (RST) begin

        PC <= 8'b0;
        SP <= 3'b0;
        STKERR <= 1'b0;
        MINTA <= 1'b0;
        for (i = 0; i < 8; i = i + 1)
            stack[i] <= 8'b0;
    end else begin
        STKERR <= 1'b0;
```

```
        MINTA <= 1'b0;


        if (interrupt_req) begin
            if (SP < 8) begin
                stack[SP] <= pc_plus_1;
                SP <= SP + 1;
                PC <= D; // Interrupt vector from D bus
                if (MINTR && !INTD) MINTA <= 1'b1;
            end else begin
                STKERR <= 1'b1;
            end
        end

        else begin

            if (stack_push && call_enable) begin
                if (SP < 8) begin
                    stack[SP] <= pc_plus_1;
                    SP <= SP + 1;
                end else begin
                    STKERR <= 1'b1;
                end
            end

            if (stack_pop && ret_enable) begin
                if (SP > 0) begin
                    SP <= SP - 1;
                end else begin
                    STKERR <= 1'b1;
                end
            end


            if (pc_load) begin
                PC <= next_addr;
            end else if (pc_increment) begin
                PC <= pc_plus_1;
            end
        end
    end
end


assign ACIO = 1'bz;
assign PCIO = 1'bz;
```

```
    assign CIO = 1'bz;
    assign CZIO = 1'bz;

endmodule
```

6.1.4 Pin Diagram

Figure 6.2: Pin Diagram of AM29112

This pin diagram shows the AM29112 microprogram sequencer chip, featuring an 8-bit bidirectional data bus (D0–D7), 8-bit address outputs (Y0–Y7), instruction and mode inputs, control and status signals, as well as cascade and interrupt handling pins. The arrangement supports complex microprogram control, stack operations, and flexible interrupt and branching logic for use in high-speed microprogrammed systems.

6.1.5 Test Circuit

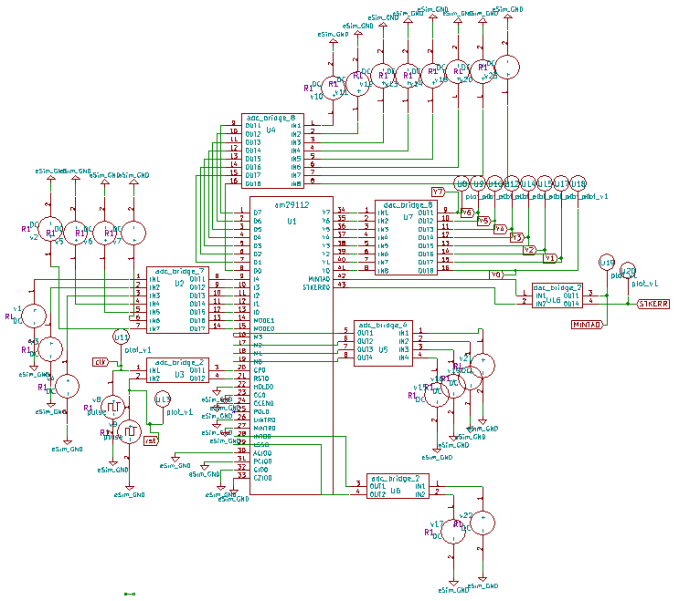

Figure 6.3: Test Circuit for AM29112

This test circuit showcases the AM29112 microprogram sequencer at the center, interfacing with address and data buses, control logic, analog-to-digital and digital-to-analog bridges, and various status/interrupt lines. It is designed to evaluate the chip's sequencing, branching, stack, and interrupt handling features within a simulated microprogrammed system environment.

6.1.6 Waveforms

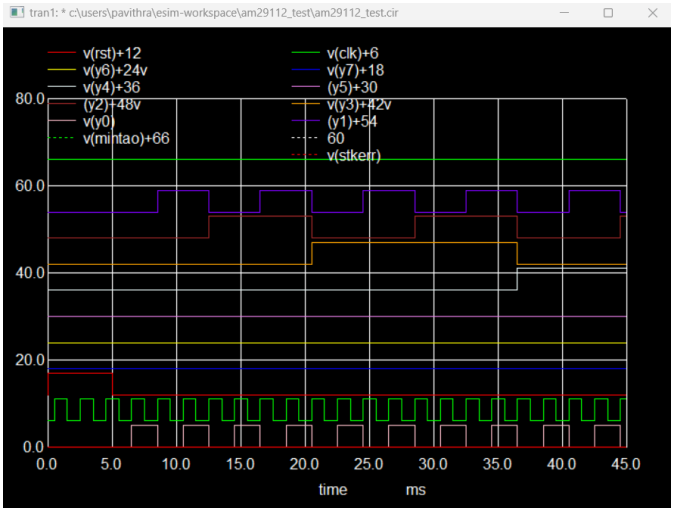

Figure 6.4: Output Waveform of AM29112 Test circuit

- **Clock (v(clk))**: A periodic square wave, serving as the system heartbeat and timing reference for state changes.
- **Reset (v(rst))**: High at initialization, dropping low after the system starts.
- **Counters and Outputs (v(y#), v(x#))**: Stepwise changes in these signals indicate sequencer progress through address or instruction cycles, as outputs change in response to clock and control events.
- **Interrupt and Stack Error**: Digital status lines, including interrupt acknowledge and stack error, transition high or low to indicate status and fault events as the microprogram executes.
- **General Trend**: The digital signals maintain stable logic levels, shifting state primarily at clock edges, as required in pipelined, synchronous digital control logic.

6.1.7 NgSpice Output

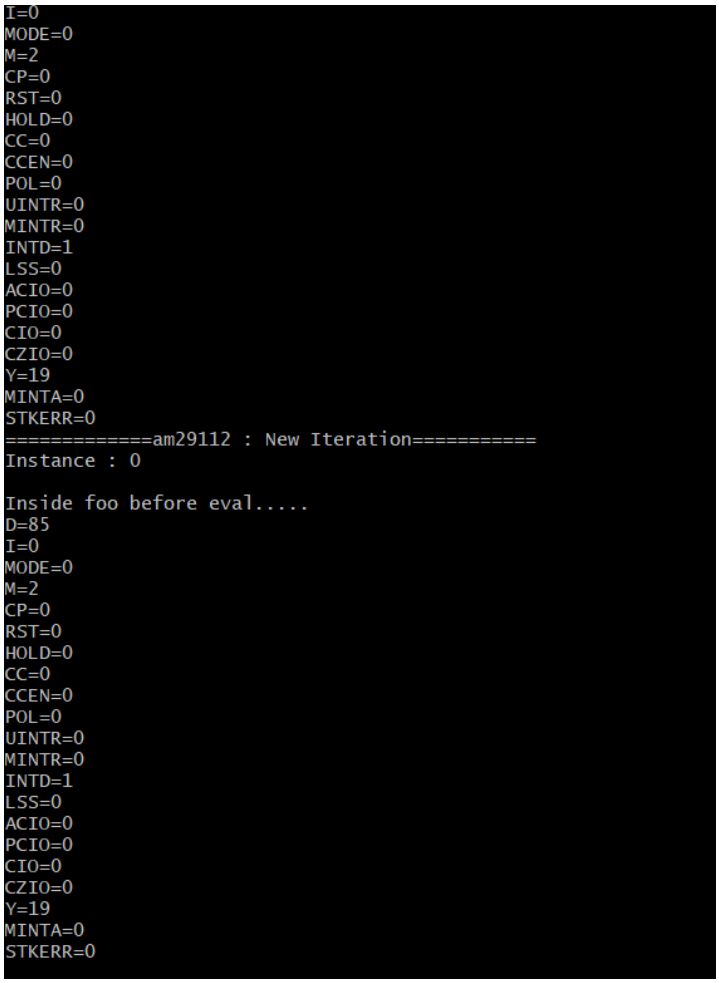

Figure 6.5: NgSpice Simulation Output for 82S126 PROM

The ngspice terminal output shows the AM29112 microprogram sequencer initializing and running with all control, data, and status signals correctly set for normal operation.

Chapter 7

Device Modeling

Device modelling in eSim refers to the process of designing fundamental semiconduc- tor devices such as BJTs, MOSFETs, and diodes through physics-based SPICE-level modelling.This approach involves formulating accurate .model statements that en- capsulate key parameters—such as threshold voltage, saturation current, mobility factors, and junction capacitances—governing the device's operation. These models are grounded in semiconductor physics and are essential for reproducing real-world phenomena like switching behavior, biasing characteristics, and nonlinearities under various operating conditions

7.1 2N3903 : NPN Silicon Transistor

7.1.1 Description

The 2N3903 is a general-purpose NPN silicon transistor commonly used for amplification and switching applications in electronic circuits. It is housed in a compact TO-92 plastic package and designed to handle maximum collector-emitter voltages of 40V, collector currents up to 200mA, and can dissipate up to 625mW of power. With a transition frequency of around 250MHz and typical DC current gain (hFE) ranging from 50 to 150 at 10mA, the 2N3903 is suitable for low-power, high-speed signal amplification in analog circuits and digital switching. Its complementary PNP counterpart is the 2N3905, making it useful in push-pull amplifier stages and other complementary designs

7.1.2 SPICE Model

.model 2N3903 NPN(Is=6.734f Xti=3 Eg=1.11 Vaf=74 Bf=200 Ne=1.5 + Ise=6.734f Ikf=0.284 Xtb=1.5 Br=3 Nc=2 Isc=0 Ikr=0 Rc=1 Cjc=3p + Mjc=0.33 Vjc=0.75 Fc=0.5 Cje=4p Mje=0.33 Vje=0.75 Tr=100n Tf=350p + Itf=0.1 Vtf=10 Xtf=1 Rb=0.56)

7.1.3 Common Emitter Configuration

The following circuit demonstrates the common emitter configuration of 2N3903

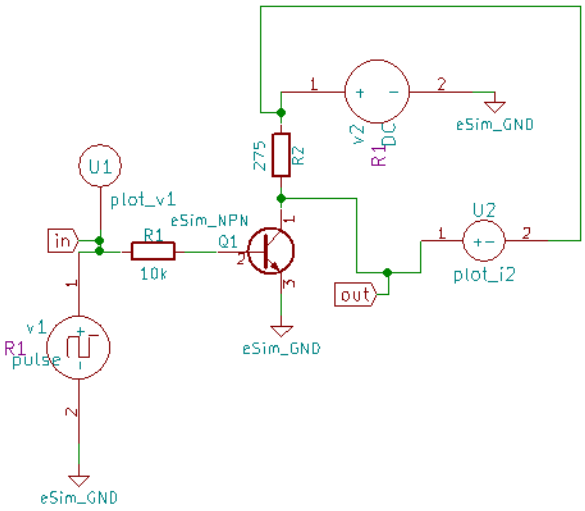

Figure 7.1: 2N3903 Common emitter configuration

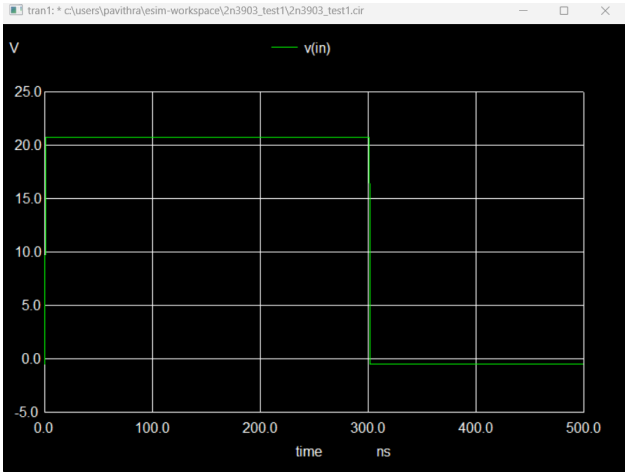

Figure 7.2: Input voltage pulse applied to base

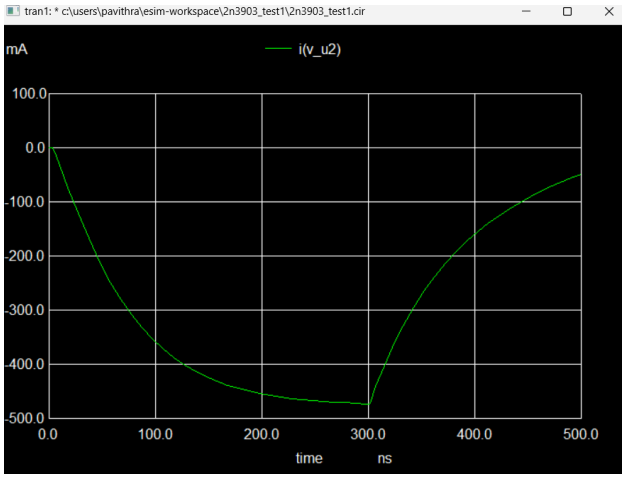

Figure 7.3: Collector current through the transistor

- When the input pulse is high, the transistor enters saturation, and a substantial collector current flows, observed as a sharp downward curve (indicating current direction in simulation).
- The collector current quickly reaches a peak negative value due to the applied input, then decays as the circuit elements respond.
- When the pulse drops back to its low state, the collector current returns toward zero, representing the switch-off sequence of the transistor.

7.1.4 Frequency Response Analysis

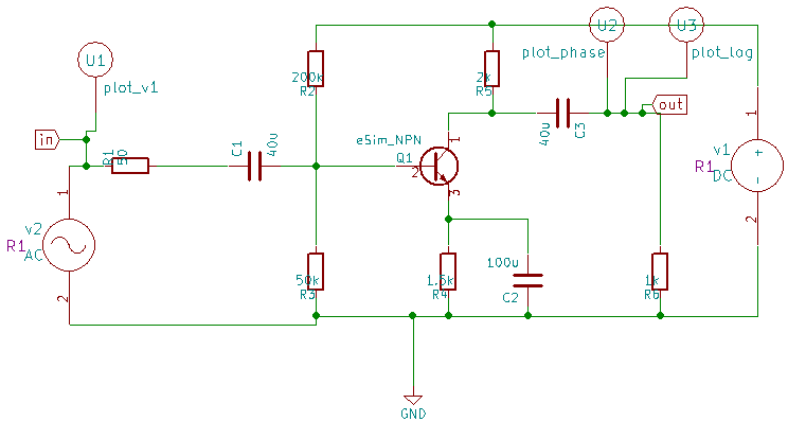

Figure 7.4: Frequency Response Measurement Circuit

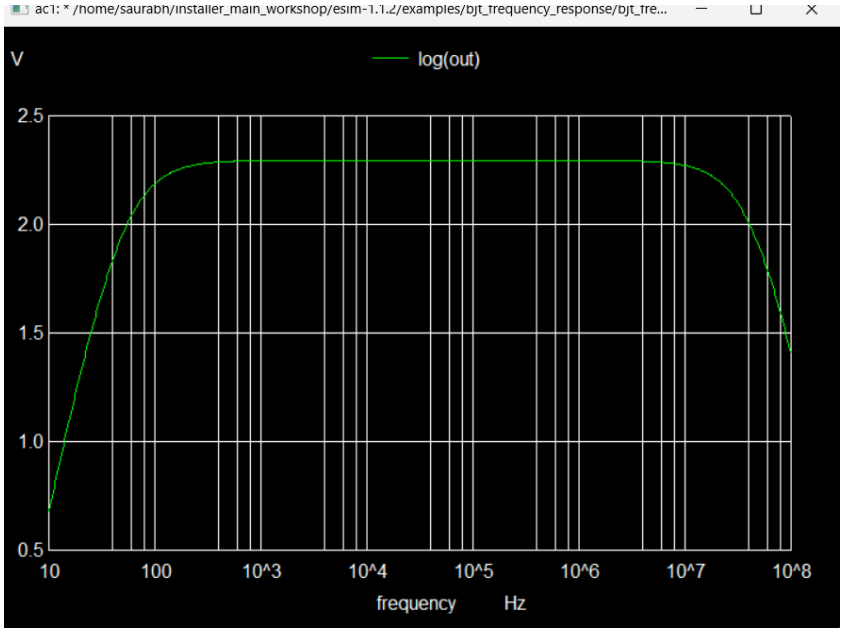

Figure 7.5: Frequency Response – log(out)

This plot represents the frequency-dependent voltage gain of the 2N3903 amplifier. It shows a flat midband gain of 2.3 V/V and a high-frequency roll-off beyond 10 MHz, indicating the transistor's bandwidth limit.

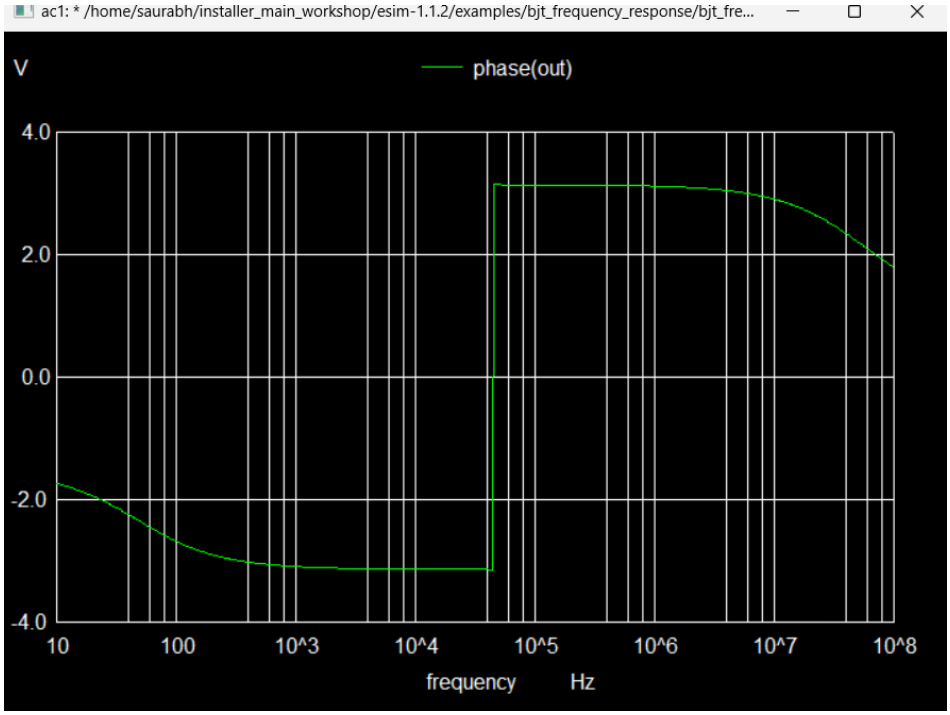

Figure 7.6: Frequency Response – Phase plot

This plot shows how the phase of the output signal shifts with increasing frequency. The 2N3903 exhibits typical phase lag behavior, with phase becoming more negative near the cutoff region, indicating capacitive effects.

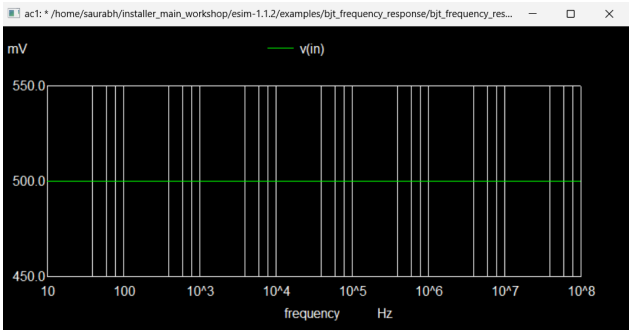

Figure 7.7: Frequency Response – Magnitude plot(V(in))

The input signal is held constant at 500 mV AC across all frequencies. This flat line confirms that the frequency sweep is applied uniformly, ensuring valid gain and phase analysis for the 2N3903 amplifier.

7.1.5 Amplifier Characteristics

This is a common-emitter amplifier circuit using the 2N3903 NPN transistor. It amplifies small AC input signals, producing a larger, phase-inverted output voltage suitable for analog signal processing. The use of coupling and bypass capacitors ensures effective signal amplification across the desired frequency range.

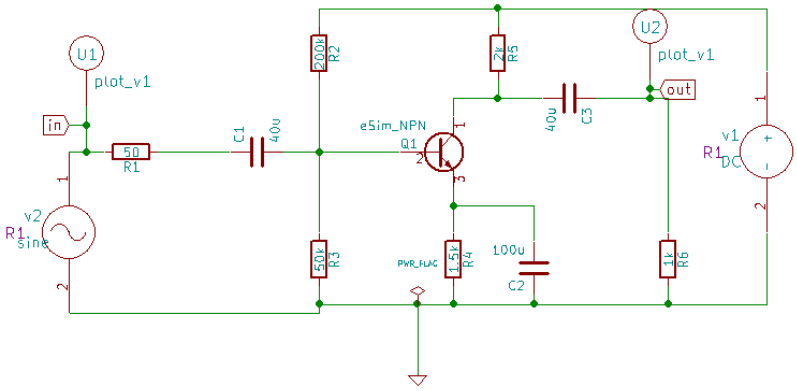

Figure 7.8: 2N3903 BJT Amplifier Circuit

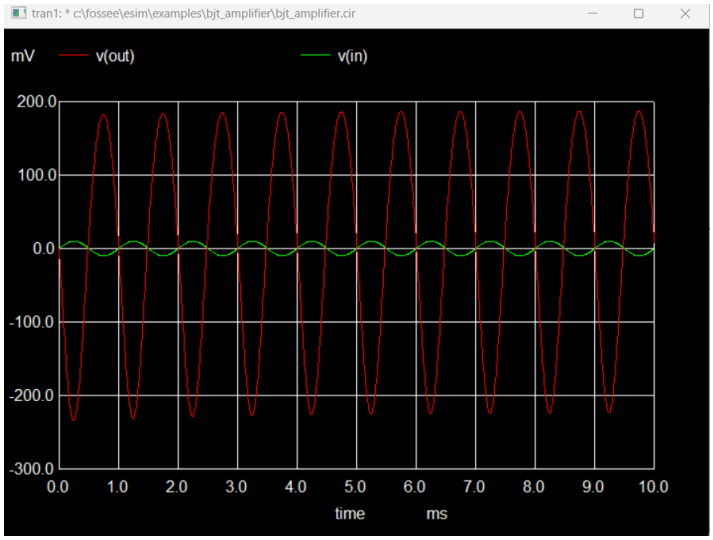

Figure 7.9: Input and Output Characteristics of 2N3903 Amplifier circuit

The displayed plot demonstrates the typical behavior of a BJT amplifier using the 2N3903 transistor. A small AC input (green) is applied, and the resulting

output (red) shows strong amplification with phase inversion—evidence of correct common-emitter amplifier operation. This matches the expected characteristic for small-signal NPN transistors like the 2N3903, confirming its suitability for signal amplification in analog circuits.

7.2 2N4393 : N-Channel JFET

7.2.1 Description

The 2N4393 is a general-purpose, low-noise N-channel junction field-effect transistor (JFET) commonly used for signal amplification and switching in electronic circuits. Housed in a TO-18 metal package, it features high input impedance, low gate leakage current, and good transconductance, making it suitable for sensitive analog applications such as audio preamplifiers, low-level signal amplifiers, and RF circuits. The 2N4393 is valued for its stability, low noise, and versatility in both amplification and switching roles.

7.2.2 SPICE Model

.MODEL 2N4393 NJF (VTO=-1.4 BETA=0.0091 LAMBDA=0.006 RD=1 RS=1 CGS=4.1p CGD=4.6p PB=1 IS=205f AF=1 FC=0.5 BETATCE=-0.5 N=1 NR=2 XTI=3 VTOTC=-2.5m ALPHA=21u VK=1 ISR=10f KF=0.001f M=0.5)

7.2.3 Amplifier Configuration

This circuit is a common-source amplifier utilizing the 2N4393 N-channel JFET. It amplifies small input AC signals, providing high input impedance and excellent signal fidelity—ideal for low-noise amplification in sensitive analog applications. Coupling and bypass capacitors ensure stable operation and bandwidth.

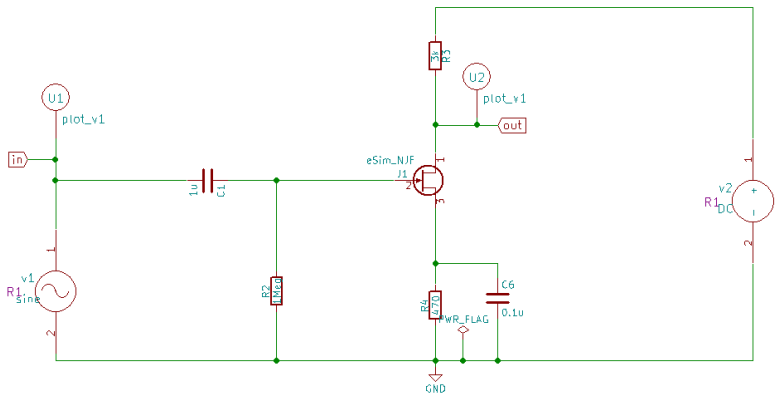

Figure 7.10: Amplifier Test Circuit using 2N4393

7.2.4 Input Waveform

- This is a sinusoidal input signal with a peak amplitude of $\pm 10\,\text{mV}$.
- The frequency is consistent and the waveform is clean.
- It represents a small AC signal applied to the gate of the FET.

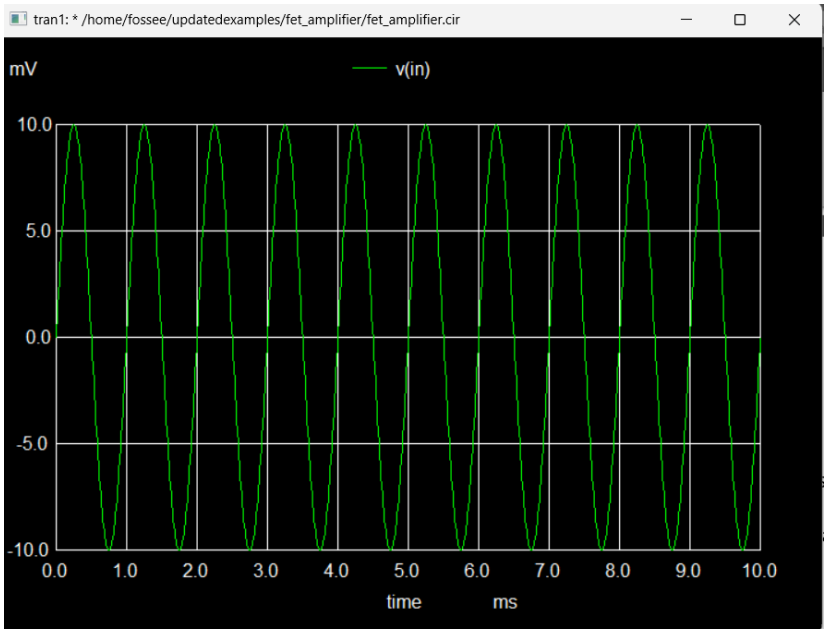

Figure 7.11: Input Waveform of the 2N4393 Amplifier

7.2.5 Output Waveform

- This is the amplified output voltage, taken from the drain.
- The waveform is sinusoidal and follows the same frequency as the input.
- The output signal is centered around $\sim 4\,\text{V}$ and has an amplitude of about $\pm 0.08\,\text{V}$, showing voltage gain.
- Since the FET amplifier is typically common-source, the output is also inverted in phase relative to the input (not clearly visible unless overlaid, but expected behavior).

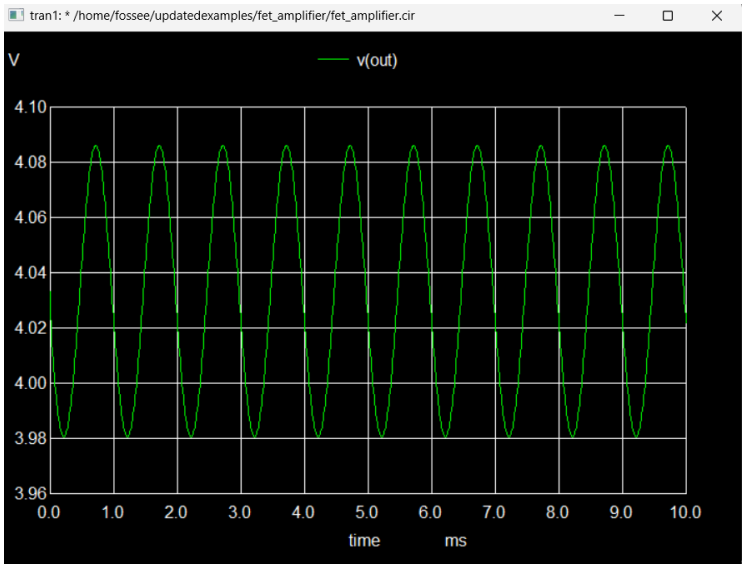

Figure 7.12: Output Waveform of the 2N4393 Amplifier

7.2.6 Frequency Response Analysis

This is a frequency response test circuit for a common-source JFET amplifier using the 2N4393 transistor. An AC input signal is coupled through capacitor C1 to the gate of the JFET (J1), while the output is taken from the drain through R2. Capacitor C6 provides source bypassing to improve gain. The circuit analyzes how the amplifier's gain and phase vary with frequency, helping plot Bode characteristics.

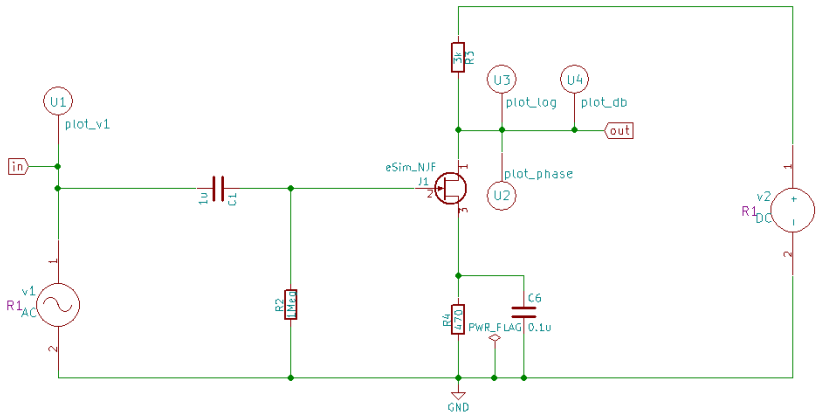

Figure 7.13: Frequency Response Test Circuit using 2N4393

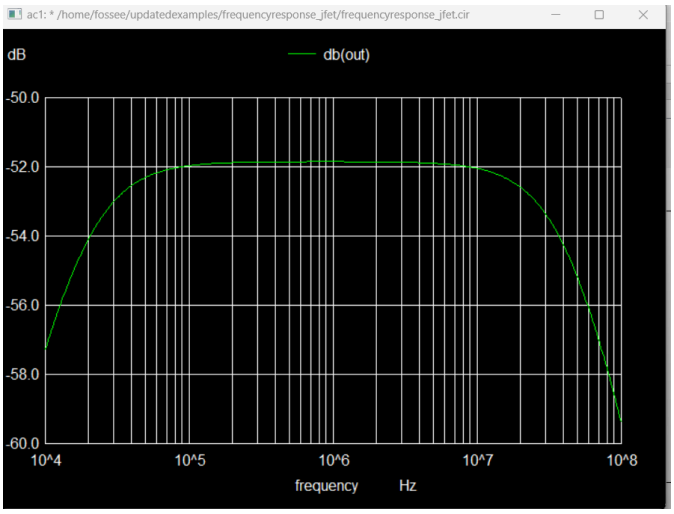

Figure 7.14: Log-Magnitude Plot of Amplifier Output (Gain vs Frequency)

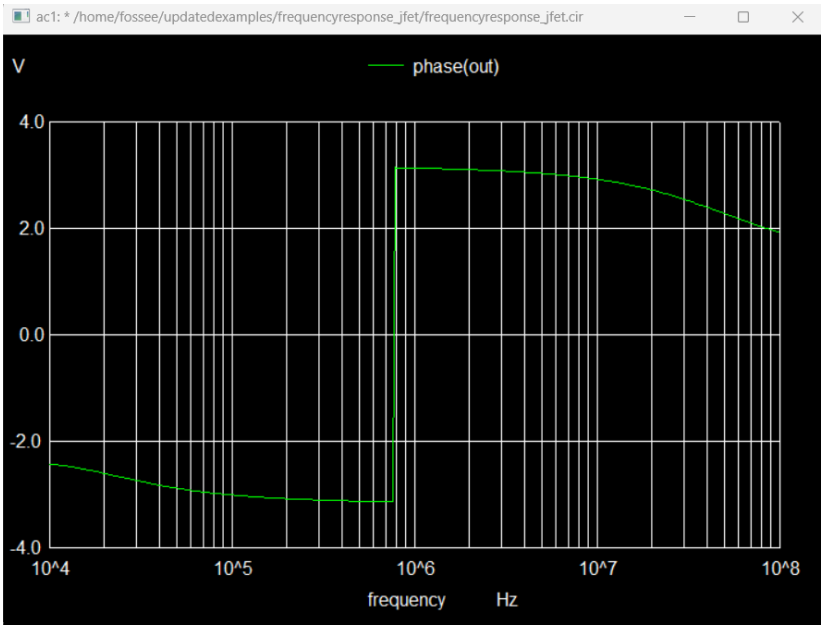

Figure 7.15: Phase Plot of Amplifier Output (Phase vs Frequency)

Log Plot (Gain vs Frequency): The frequency response plot of the 2N4393-based JFET amplifier shows a flat gain of around -52 dB in the mid-frequency range, indicating stable amplification. The gain drops off at low and high frequencies

due to coupling/bypass capacitors and parasitic capacitances, defining the amplifier's bandwidth limits.

Phase Plot (Phase vs Frequency): The phase response shows a sharp phase shift near the amplifier's lower cutoff frequency and a gradual phase lag as frequency increases, typical of a common-source amplifier. This behavior is due to the reactive elements (capacitors and intrinsic capacitances) affecting signal phase. The sudden jump around 10610**6106 Hz reflects a -180° to +180° phase wrap, which is normal in such logarithmic phase plots.

7.2.7 Digital Switching test circuit

This is a digital switching test circuit for the 2N4393 N-channel JFET. A pulse input is applied to the gate through a resistor network, controlling the JFET's conduction. The drain is connected to a DC supply through a 3.2k ohm load resistor, and the output is taken at the drain. This setup helps observe the JFET's switching behavior, such as how it turns ON and OFF with gate voltage variations.

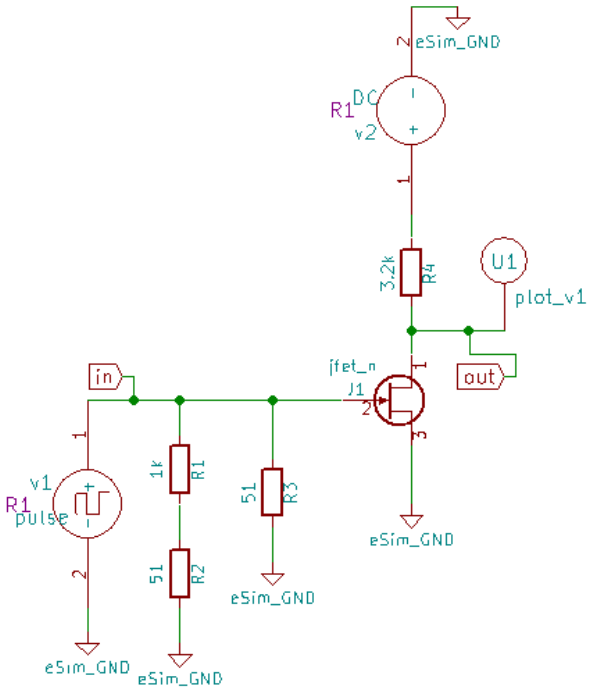

Figure 7.16: Switching circuit using 2N4393

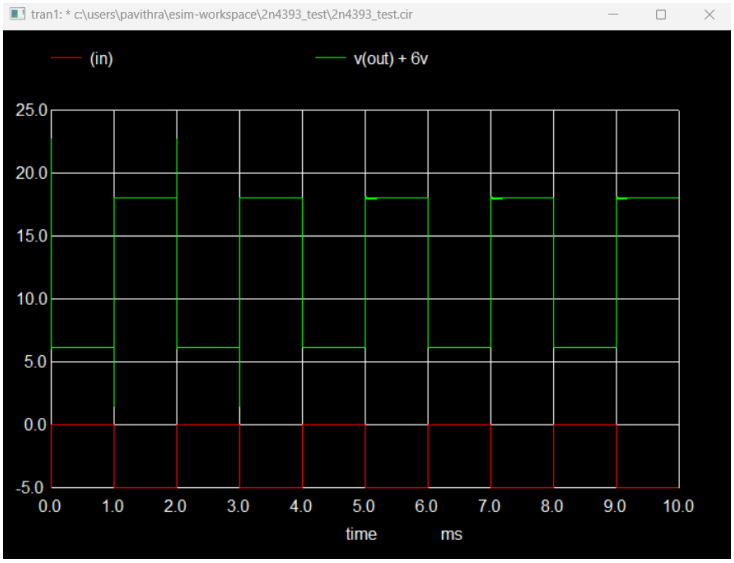

Figure 7.17: Input and Output Waveforms

The output waveform shows proper switching of the 2N4393 JFET. The output goes low when the JFET conducts and high when it turns off, matching the input pulse.

7.3 1N34A : Germanium Diode

7.3.1 Description

The 1N34A is a point-contact germanium diode known for its very low forward voltage drop (typically 0.1–0.3V) and high sensitivity, making it ideal for detecting and demodulating weak signals in crystal radios, AM/FM detectors, and other RF applications. It features a peak reverse voltage of up to 65V and an average forward current rating of 50mA, and is valued for its linearity and reliable performance in audio and radio frequency circuits

7.3.2 SPICE Model

.model 1N34A D(IS=2.6u RS=6.5 N=1.6 CJO=0.8p EG=0.67 BV=75 IBV=1m)

7.3.3 Forward Bias Characteristics

The following test circuit is used to observe the forward bias behavior of the 1N34A diode. A DC voltage source is applied in series with a current-limiting resistor and the diode under test.

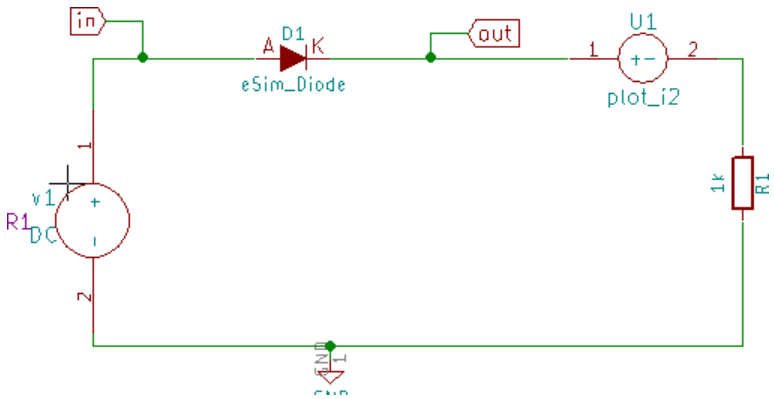

Figure 7.18: Forward Bias Test Circuit for 1N34A

Forward Bias Characteristics – Waveform

The forward bias characteristics of the 1N34A germanium diode show that it begins conducting current at a very low forward voltage—typically around 0.2V. As the voltage increases, the current rises rapidly, making the 1N34A highly sensitive and ideal for signal detection in low-voltage applications. This behavior is due to its low forward voltage drop and high sensitivity compared to silicon diodes.

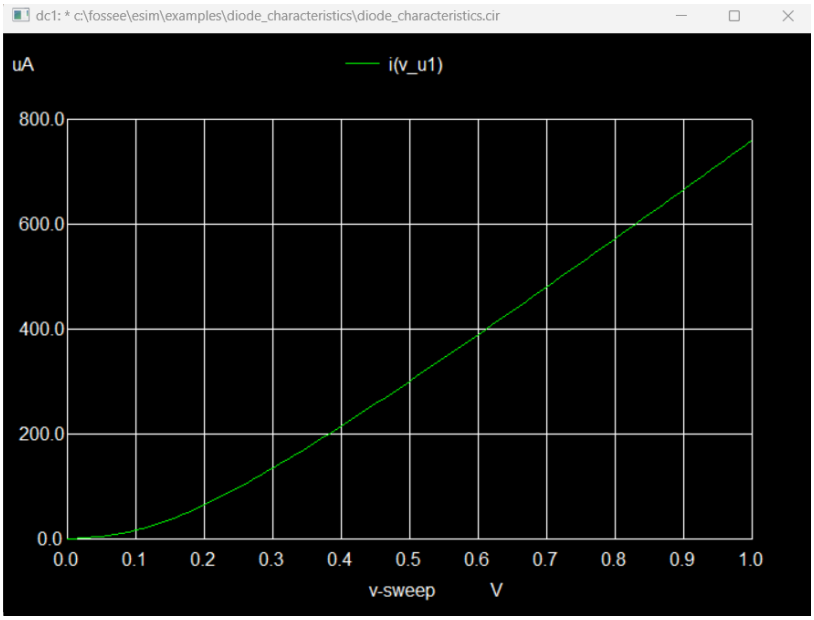

Figure 7.19: Forward Bias Characteristics (V F vs I F)

7.3.4 Reverse Bias Characteristics

To test the reverse bias response, a DC source is connected with polarity reversed across the diode along with a current measurement setup. The reverse current observed is typically very small,indicating high resistance to reverse conduction and confirming the diode's rectifying behavior.

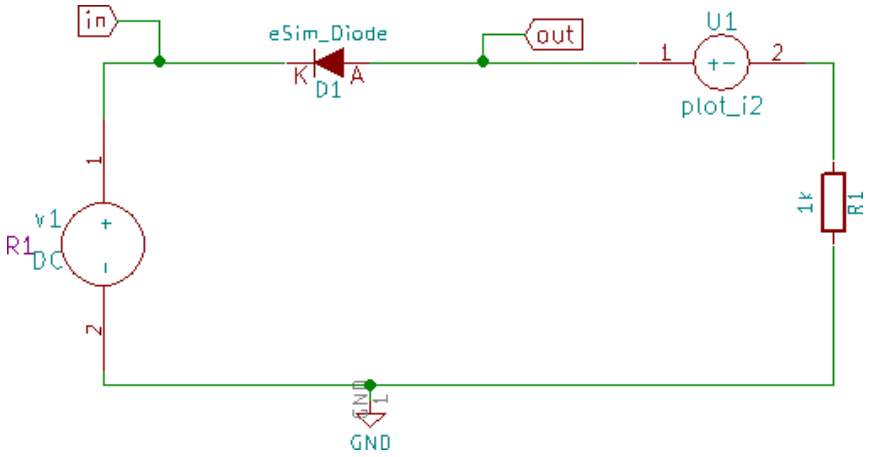

Figure 7.20: Reverse Bias Test Circuit for MUR406

Reverse Bias Characteristics Waveform

When the 1N34A germanium diode is reverse biased, it allows only a very tiny leakage current to flow—often measured in microamperes or less. As the reverse voltage increases, the current remains nearly constant and very low until the breakdown voltage is reached, at which point the current rises sharply. This high reverse resistance and minimal leakage make the 1N34A suitable for signal detection where low reverse current is essential.

7.4 Half-Wave Rectifier using 1N34A

A half wave rectifier with a 1N34A germanium diode converts AC to pulsating DC by allowing only the positive half-cycles of the input signal to reach the output. The 1N34A's low forward voltage drop ensures efficient rectification, making it ideal for detecting and rectifying low-level signals.

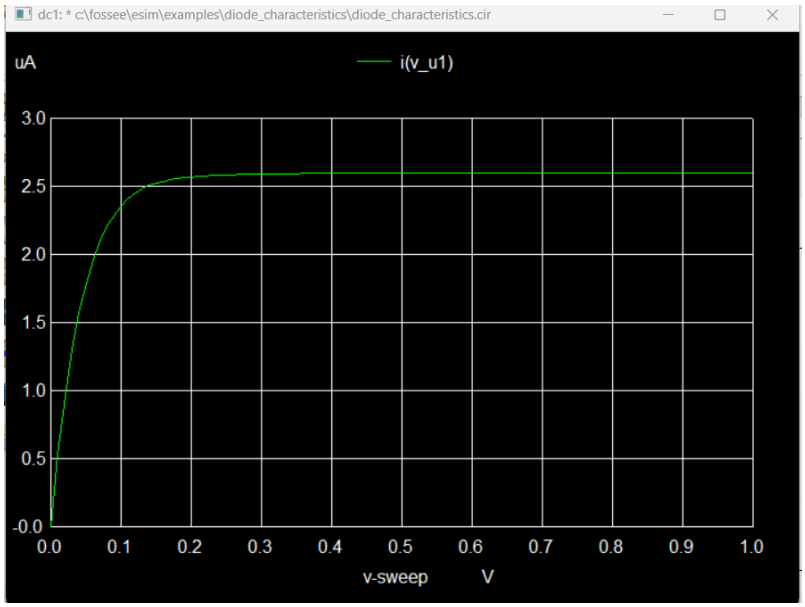

Figure 7.21: Reverse Bias Characteristics (I R vs V R)

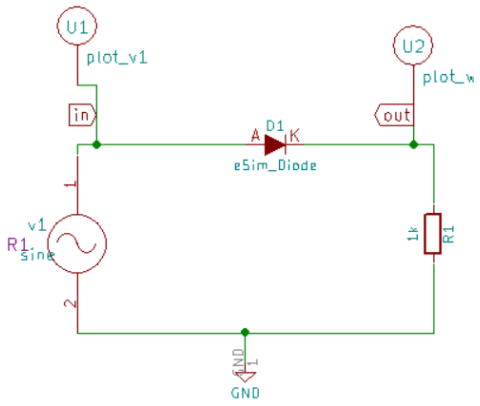

Figure 7.22: Half wave rectifier circuit using 1N34A

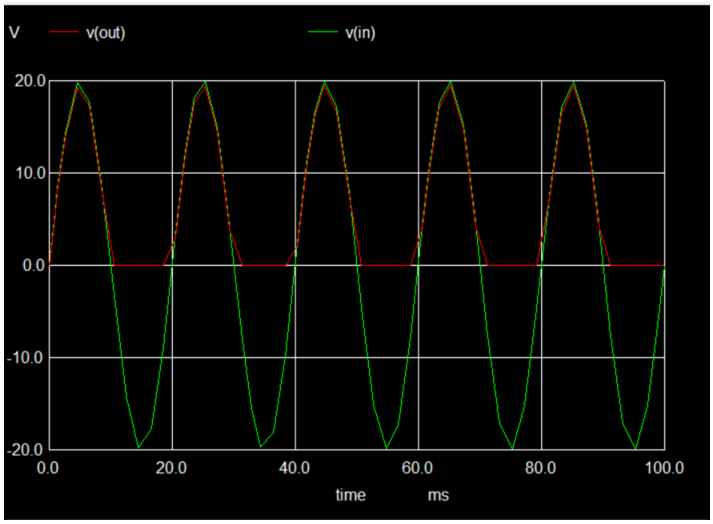

Figure 7.23: Input and Output waveforms of Half wave rectifier using 1N34A

7.5 TIP41C : NPN Silicon Transistor

7.5.1 Description

The TIP41C is a medium-power NPN silicon transistor widely used for amplification and switching applications. Housed in a TO-220 package, it features a maximum collector-emitter voltage of 100V, a collector current rating of up to 6A, and power dissipation capability of 65W. Its robust design, moderate gain, and high current handling make it suitable for audio amplifiers, power regulators, motor control, and other general-purpose circuits where reliable amplification or switching is required

7.5.2 SPICE Model

.model TIP41C NPN (+ IS=1.0E-10 BF=100 NF=1.0 VAF=50 IKF=1.0 + ISE=1.0E-11 NE=2.0 BR=1.0 NR=1.0 VAR=10 IKR=0.5 + RE=0.5 RC=1.0 RB=1.0 + CJE=30p VJE=0.75 MJE=0.33 + CJC=10p VJC=0.5 MJC=0.33 + TF=0.5n TR=1n)

7.5.3 Amplifier Configuration

The amplifier circuit shown below uses the TIP41C in a common-emitter configuration, suitable for inverting signal amplification.

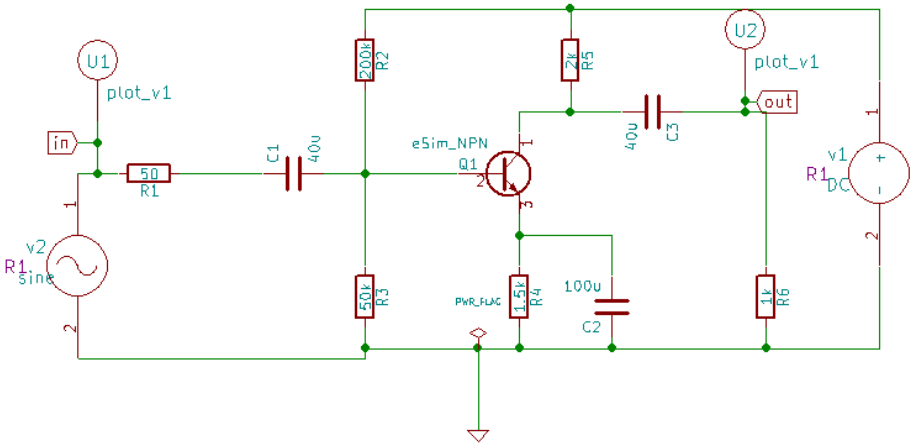

Figure 7.24: Amplifier Circuit Using TIP41C in Common-Emitter Configuration

Amplifier Output Waveform

The amplifier using the TIP41C transistor produces an output waveform with a significantly greater amplitude and an inverted phase compared to the input. This demonstrates strong voltage gain and correct operation as a common-emitter amplifier, making it suitable for applications requiring robust signal amplification.

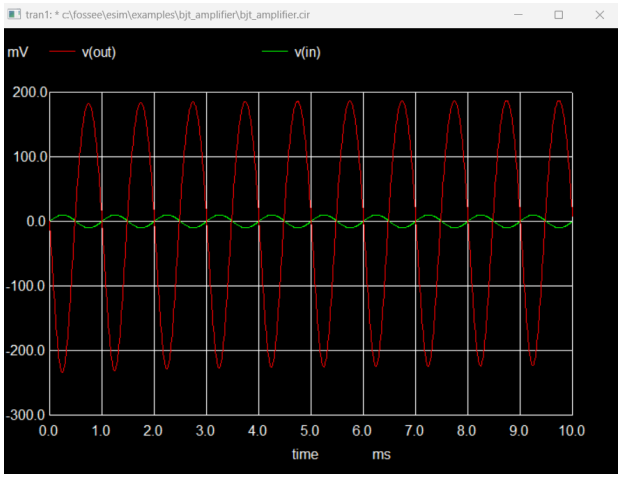

Figure 7.25: Output Waveform of TIP41C Amplifier

7.5.4 Common-Base Configuration

Common-Base output Characteristics

This circuit uses the TIP41C power transistor in a common-base (CB) configuration. It provides current gain and low input impedance, making it effective for applications requiring high-frequency signal amplification and stable operation. The configuration also exhibits low voltage gain with nearly unity output phase, which is useful for specific analog circuit application

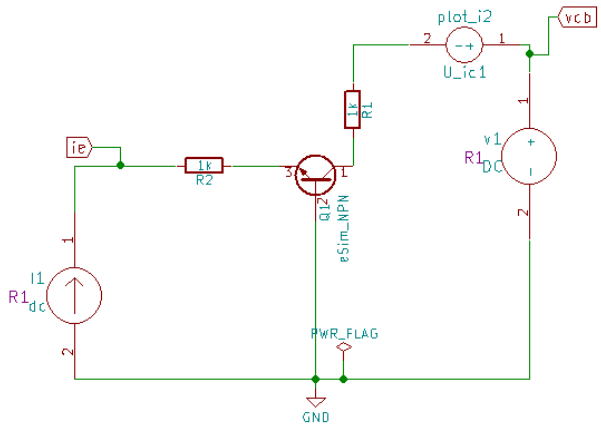

Figure 7.26: Common-Base Characteristic Circuit

The graph shows collector current increasing linearly with collector-base voltage for various emitter currents, which is typical of proper CB operation. It demonstrates stable current control by the emitter and shows the expected Early effect, confirming correct active region behavior for the TIP41C in this configuration.

7.5.5 Frequency Response Analysis

To evaluate high-frequency performance, the amplifier is subjected to a frequency sweep. Gain and phase shift are analyzed to determine bandwidth and stability.

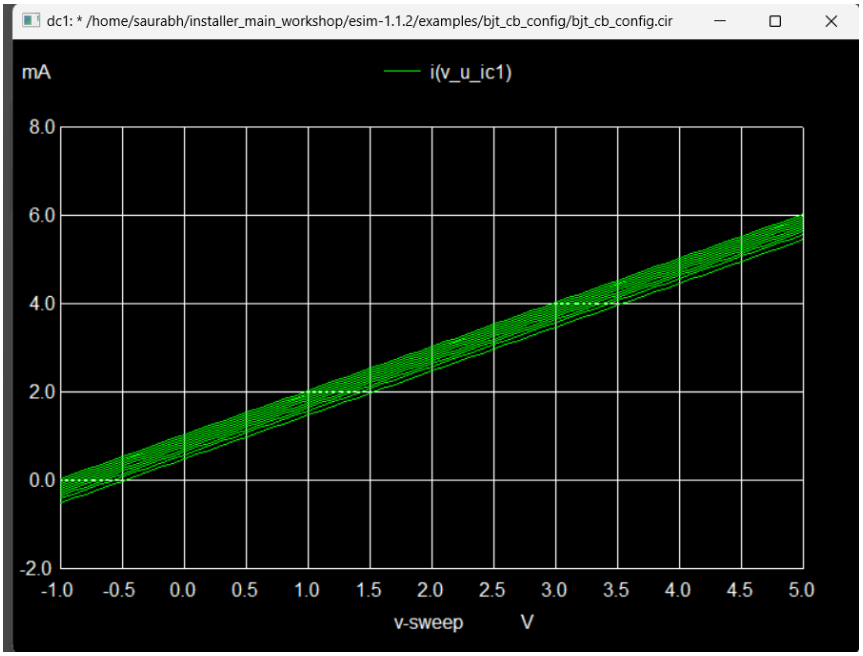

Figure 7.27: Common-Base Output Characteristics

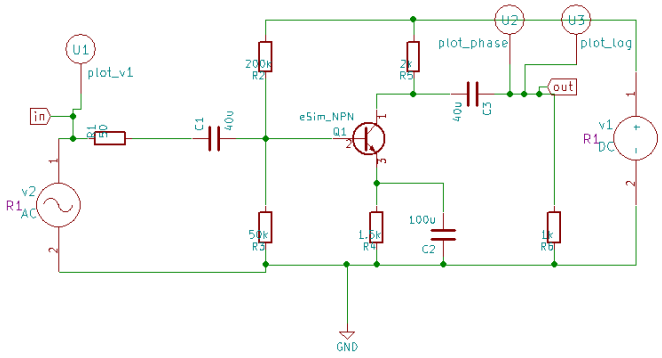

Figure 7.28: Frequency Response Test Circuit for Common-Emitter Amplifier

Log-Magnitude Plot: The amplifier maintains a consistent gain across a wide mid-frequency range, with roll-off (attenuation) at both low and high frequencies. This band-pass behavior is typical due to the device's inherent limitations and coupling capacitance

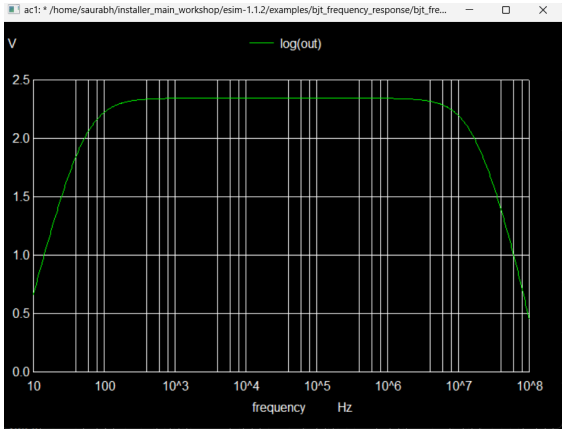

Figure 7.29: Log-Magnitude Plot (Gain vs Frequency)

Phase Plot: The phase plot shows the variation of output signal phase relative to the input signal as the frequency increases. It helps assess phase margin and feedback system stability.

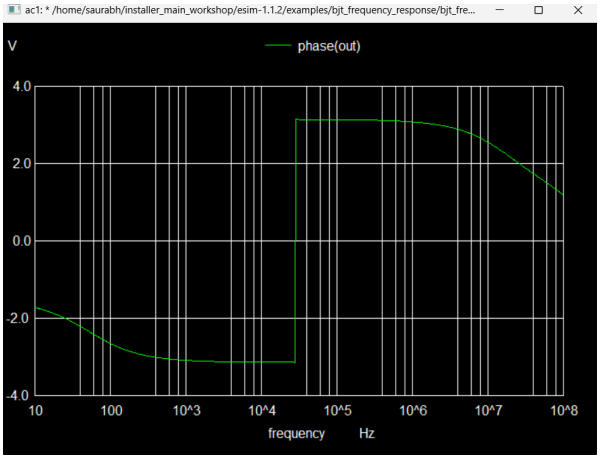

Figure 7.30: Phase Plot (Phase vs Frequency)

Chapter 8

Failed ICs

In this section, we discuss circuits that did not perform as expected during testing. Understanding the reasons for these failures helps in diagnosing issues and improving circuit design.

8.1 MC1556:Operational Amplifier

- The subcircuit for the MC1556 IC was implemented, closely following its datasheet specifications.
- A standard test circuit was created with the op-amp in the non-inverting configuration, including power supply connections and a resistive load.
- The output waveform does not match the expected op-amp response, likely due to incorrect circuit connections, supply voltages, or component values in the simulation.
- It's possible that the subcircuit model for the MC1556 contains errors or is not fully compatible with the simulation tool.
- Mismatches like offset errors or limited slew rate, or issues with biasing, can also cause deviations from ideal output.

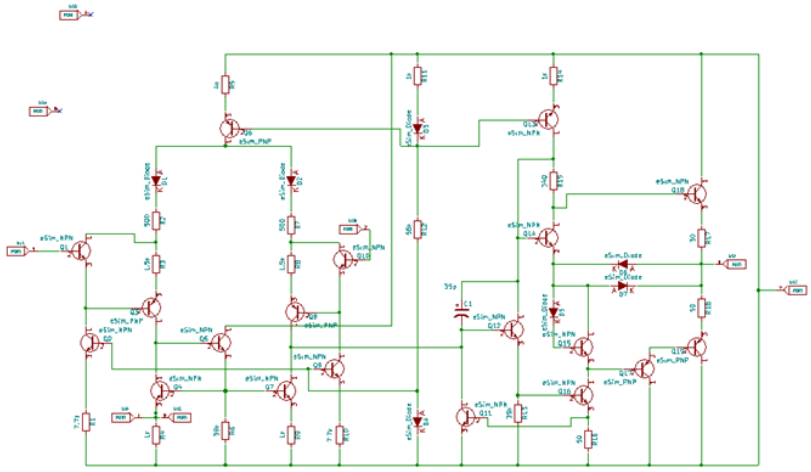

Figure 8.1: Subcircuit of MC1556

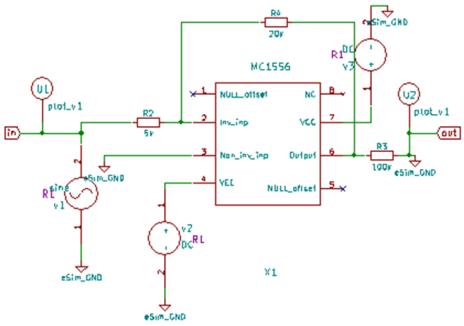

Figure 8.2: Test circuit of MC1556

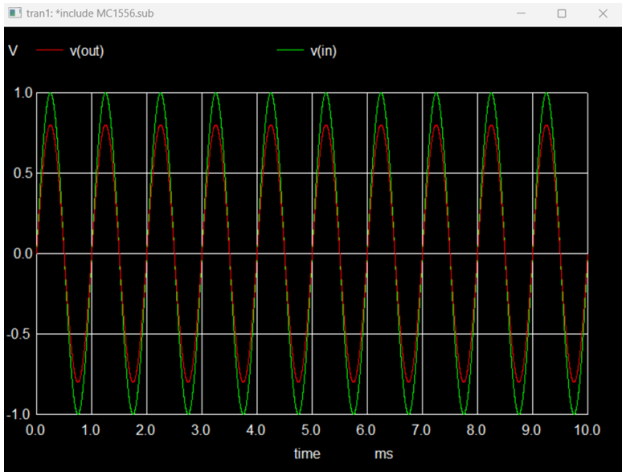

Figure 8.3: Input and Output waveform obtained

8.2 Ml1490: RF/IF Amplifier

- The ML1490 subcircuit was implemented using its typical internal schematic.
- A test circuit was set up with the ML1490 configured for AC signal amplification.
- A sinusoidal input (V_in) was applied and the corresponding output (V_out) was measured.
- Input and output voltage waveforms were captured for analysis.

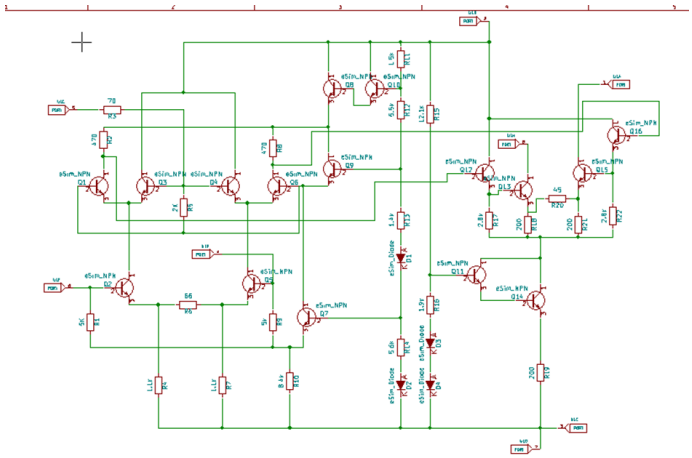

Figure 8.4: Subcircuit of ML1490

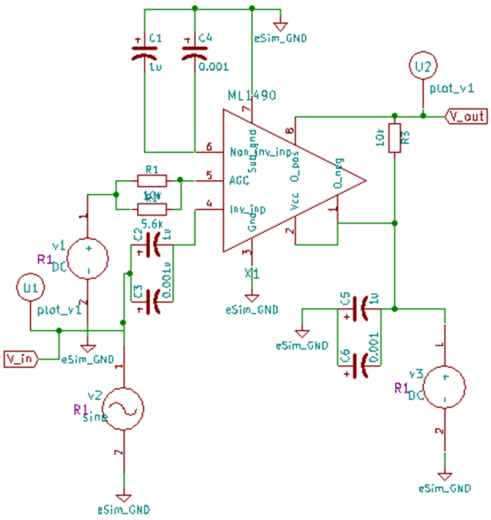

Figure 8.5: Video Amplifier test circuit using ML1490

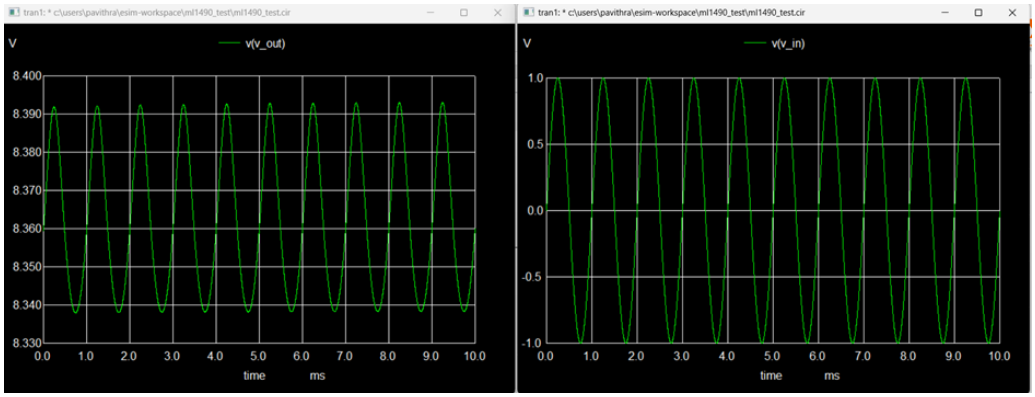

Figure 8.6: Input and output waveforms of ML1490

Output waveform is not as expected: The output voltage is nearly flat with only a small oscillation superimposed, while the input is a full-amplitude sine wave. Ideally, there should be a significant amplification and/or gain-controlled output.

Possible reasons for failure:

- The ML1490 is primarily intended for RF/IF or audio AGC amplification, not as a standard op-amp, so using it directly as a general amplifier might not yield expected results.
- There may be mistakes in circuit connections, AGC biasing, or load configuration, leading to improper operation.

8.3 TDA2320:PreAmplifier for Infrared remote control systems

The internal subcircuit of the TDA2320 was constructed as per standard references. A typical test setup was assembled for basic amplification, but choosing suitable resistor and capacitor values was challenging due to the lack of recommended values in the datasheet.

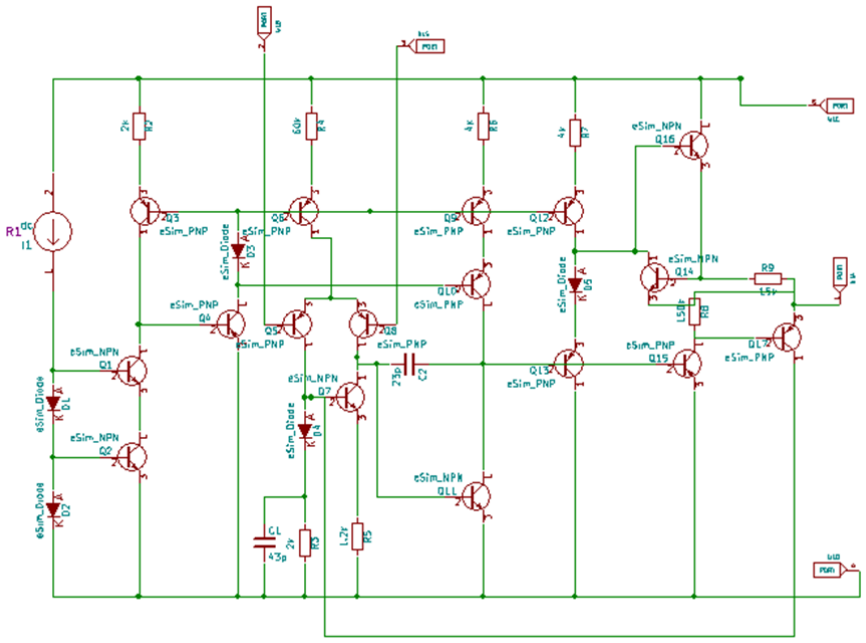

Figure 8.7: Subcircuit of TDA2320

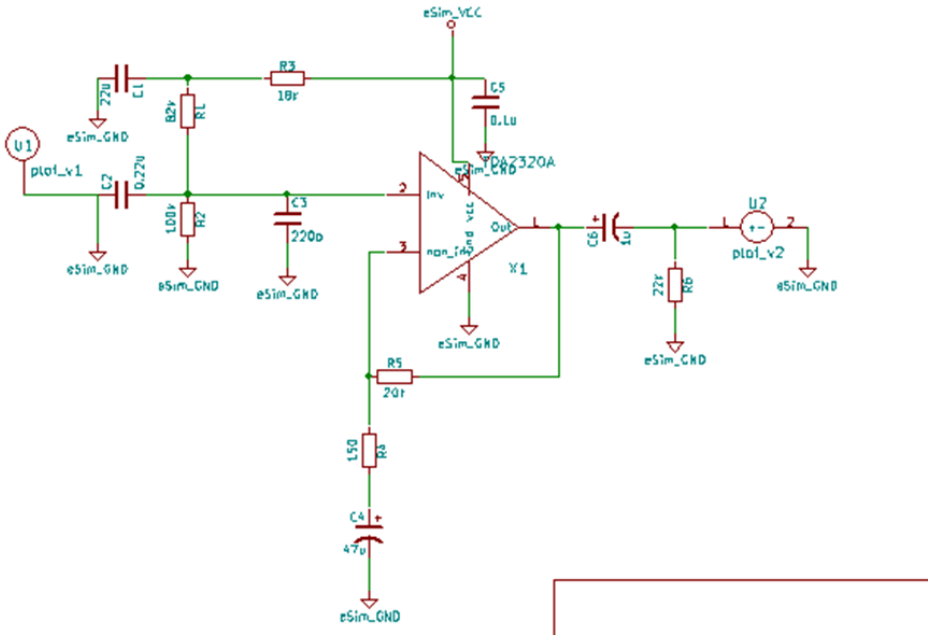

Figure 8.8: Stereo amplifier test circuit using TDA2320

- The datasheet did not provide explicit values for all required resistors and capacitors, making it difficult to ensure correct biasing and frequency response.
- The simulation produced an error indicating “iteration limit reached," zero length vector error.

Chapter 9

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