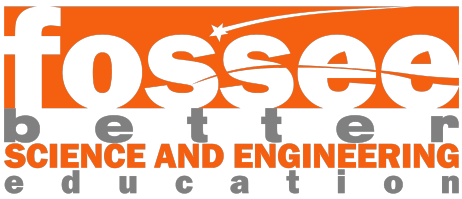

Summer Fellowship Report

On

FreeCAD based Modelling and 4-layer PCB Design using eSim

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I also sincerely appreciate the entire FOSSEE initiative for its efforts in empowering students and researchers by making tools freely accessible, thus removing the barriers imposed by costly commercial software. This mission not only fosters innovation but also strengthens the open-source ecosystem, allowing young learners to actively contribute and grow.

This internship has been a memorable and rewarding phase of my academic journey. The knowledge, skills, and experiences I have gained will undoubtedly serve as a strong foundation as I move forward in my career in the electronics domain.

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Chapter 1

Introduction

The advancement of Electronic Design Automation (EDA) tools has revolutionized the way electronic circuits are designed, simulated, and verified. Among these, open-source tools play a crucial role in making advanced EDA capabilities accessible to students, educators, and researchers without the burden of expensive licenses. The FOSSEE project at IIT Bombay has taken significant steps to promote such open-source tools globally.

One of the key open-source tools developed and promoted under FOSSEE is **eSim**, which integrates multiple open-source EDA tools to provide a unified platform for circuit design, simulation, and PCB layout. Various tools like NgSpice, Makerchip, and KiCad work together under eSim to offer a complete design environment.

1.1 eSim

eSim is an open-source Electronic Design Automation (EDA) tool developed by FOSSEE, IIT Bombay. The primary objective of eSim is to provide a completely free and open-source alternative to commercial circuit design and simulation software, thereby reducing dependency on expensive proprietary tools in academia and research.

eSim integrates multiple open-source tools to provide a comprehensive design and simulation environment. **KiCad** is used for schematic capture and PCB design, while **NgSpice** performs analog circuit simulation. For digital simulation, **GHDL** is integrated, supporting VHDL based designs, and **Makerchip** enables online Transaction Level Verilog (TL-Verilog) based digital design and verification. Python sup-

port is also available in eSim, allowing users to perform customized simulations, generate netlists.

One of the key features of eSim is its **Subcircuit feature**, which allows complex designs to be modularized into reusable blocks, simplifying the design of large systems. Additionally, eSim supports device modeling, enabling users to define and simulate custom semiconductor devices using real-world parameters. As part of its continuous development, eSim also supports **SkyWater SKY130 PDK**, allowing users to perform simulations using an open-source 130nm Process Design Kit, which is widely used for analog, mixed-signal, and digital IC design research.

By supporting a fully open-source toolchain, eSim empowers students, educators, and researchers to gain hands-on experience with industry-relevant EDA tools and contribute actively to the open-source hardware ecosystem.

1.1.1 NgSpice

NgSpice is an open-source circuit simulator integrated into eSim for performing analog and mixed-signal simulations. Based on the SPICE simulation engine, NgSpice supports DC, AC, transient, and parametric analyses, making it suitable for analyzing a wide range of circuits.

It allows users to simulate circuit behavior using industry-standard SPICE models, including support for subcircuits and behavioral modeling. In eSim, NgSpice works as the backend simulator for schematics created using KiCad, providing waveform outputs for voltage, current, and frequency responses. Its flexibility and accuracy make it a powerful tool for verifying designs before hardware implementation.

1.1.2 Makerchip

Makerchip is an integrated platform designed to simplify digital circuit design by offering both browser-based and desktop-based environments for coding, simulating, and debugging digital hardware designs. It supports multiple hardware description languages including Verilog, SystemVerilog, and Transaction-Level Verilog (TL-Verilog), allowing

flexibility for users at various levels of expertise.

In eSim, Makerchip is interfaced through a Python-based application called Makerchip-App, which seamlessly launches the Makerchip IDE for digital design and verification. The platform integrates several open-source and proprietary tools to provide a rich set of features such as real-time simulation, waveform viewing, and code linting, thereby improving design accuracy and productivity.

1.1.3 KiCad

KiCad is an open-source PCB design and schematic capture tool integrated within eSim for creating circuit schematics and generating PCB layouts. It allows users to design multi-layer boards, define custom footprints, and perform design rule checks to ensure design correctness before fabrication.

In eSim, KiCad acts as the primary schematic editor, allowing users to graphically build circuits by placing and interconnecting components from extensive open-source libraries. The designed schematics can directly be used for both simulation and PCB layout generation. KiCad also supports features such as 3D visualization of PCBs, Gerber file export for manufacturing, and electrical rule checking to identify design issues early. Its seamless integration within eSim enables a smooth transition from schematic design to simulation and physical realization, offering a complete design-to-fabrication workflow entirely within an open-source environment.

1.1.4 GHDL

GHDL is an open-source simulator for VHDL, a hardware description language widely used in digital circuit design. It supports the complete IEEE VHDL standard, allowing designers to simulate, verify, and debug VHDL-based digital systems effectively.

In eSim, GHDL is integrated to enable digital simulation alongside analog simulation provided by NgSpice. Users can model digital circuits using VHDL, which are then simulated using GHDL to verify logical functionality and timing behavior. This integration allows eSim to handle mixed-signal designs, where the analog components are simulated by NgSpice and the digital components by GHDL, providing

a comprehensive platform for complex system design. The combination of these tools allows designers to validate both analog and digital subsystems within a unified simulation environment.

1.2 FreeCAD

FreeCAD is an open-source parametric 3D CAD modeling software developed to cater to a wide range of engineering and design applications, particularly in mechanical engineering and product design. With its robust parametric modeling capabilities, FreeCAD allows users to modify designs by going back into their model history and changing parameters, making it ideal for iterative design processes.

FreeCAD is modular in nature, featuring multiple **workbenches** such as Part Design, Sketcher, Draft, Arch, FEM (Finite Element Method), and Path for CAM operations. Each workbench provides specific tools tailored to a particular aspect of design, simulation, or manufacturing. The **Sketcher** workbench allows constraint-based 2D sketching, which forms the basis for creating complex 3D models in the Part Design workbench.

A major strength of FreeCAD is its scripting support using **Python**, enabling automation, custom macro development, and advanced modeling workflows. The software is also compatible with a variety of industry-standard file formats such as STEP, IGES, STL, SVG, DXF, and OBJ, allowing seamless integration with other CAD and simulation tools.

FreeCAD also supports external modules and plugins, extending its capabilities for domains like architecture (through BIM tools), mechanical simulation, electronics (with PCB importers), and technical drawing generation. Its active development community and integration with open-source platforms make it a powerful and flexible tool for students, researchers, hobbyists, and professionals alike.

Chapter 2

Problem Statement

To design, develop, and test a compact electro-mechanical setup by miniaturizing a roller mechanism using FreeCAD, and to integrate it with an embedded system centered around the ESP32-S3 Sense microcontroller. The actuation is provided by a 28BYJ-48 stepper motor controlled through a ULN2003A driver IC. A custom-designed, multi-layer PCB consolidates the microcontroller, motor driver, power regulation circuits—including both LM7805 linear and advanced BQ25185/TPS61023 modules—and the SX1262 LoRa communication module for low-power, long-range wireless connectivity. This integrated hardware platform offers a reliable and modular solution suitable for automation and control applications in compact embedded systems.

2.1 Mechanical Design and Actuation System

The mechanical subsystem was developed using FreeCAD to achieve a compact, reliable roller mechanism optimized for controlled linear motion and ease of integration. Key mechanical components modeled and incorporated include the 28BYJ-48 stepper motor, precision gears, motor coupling assemblies, and support guides to maintain proper strip tensioning and alignment within tight tolerances.

- The miniaturized roller mechanism is tailored for precise movement of thin media, supported by accurately positioned stepper motor and gear assemblies.

- The 28BYJ-48 stepper motor is utilized for its affordability and precise step control, interfaced via the ULN2003A driver.
- The motor-driver coupling, as well as gear and support structures, were modeled carefully in FreeCAD to optimize space while maintaining robustness and smooth operation.
- Mechanical tolerances and alignment considerations were rigorously addressed to minimize operational backlash and ensure reliability.

This mechanical configuration guarantees smooth, repeatable actuation, aligning with the compact embedded control requirements imposed by the overall system design.

2.2 Embedded System Integration and Communication

The embedded control system leverages the ESP32-S3 Sense microcontroller for high-performance computation, extensive peripheral interfacing, and onboard sensor functionalities. Two iterations of custom PCB designs were developed to realize the system hardware integration.

- The initial PCB design employs the LM7805 linear regulator along with the ULN2003A driver IC, providing a simple and effective foundation for motor control, power regulation, and peripheral connections.
- The advanced PCB iteration features a four-layer stackup integrating discrete BQ25185 battery management and TPS61023 synchronous boost converter circuits, enabling efficient solar and USB Type-C power pathways alongside an expanded feature set.
- The SX1262 LoRa module is seamlessly integrated into both PCB versions for reliable, low-power long-range wireless communication.
- The ESP32-S3 Sense microcontroller and SX1262 modules are stacked vertically on the optimized PCB, minimizing footprint

and enhancing modularity. The ESP32-S3 module footprint follows the Seeed Studio Xiao standard, with the MCU positioned at the bottom to ensure unobstructed camera functionality.

- The consolidated PCBs integrate motor driver control, power regulation, MCU, and LoRa communication interfaces into compact, robust hardware suitable for field deployment.

This multiphase embedded platform offers a versatile and scalable foundation for automation and wireless control applications, addressing both prototyping simplicity and advanced power management for long-term reliability.

Chapter 3

Roller Feed Mechanism Design

This chapter presents the design and working principle of a custom roller feed mechanism. The system is designed to transport flexible material in a controlled manner using a motorized gear system and a dual-roller guide. The architecture is modular, 3D-printable, and suitable for experimentation or integration into broader automation systems. The key features include a geared roller pulling system, a passive guiding roller, and a sensor integration slot for real-time material monitoring.

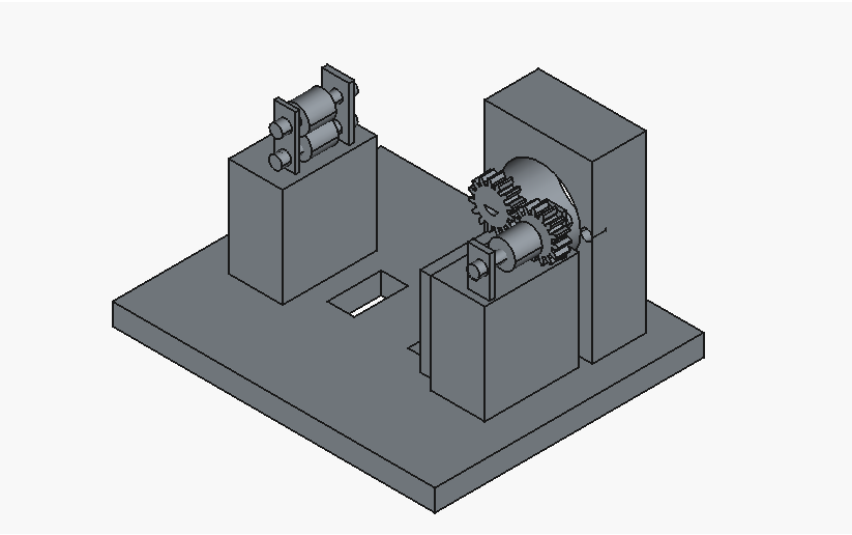

Figure 3.1: Isometric View of the Roller Feed Mechanism

3.1 Overview of the Mechanism

The mechanism is constructed on a solid rectangular baseplate with multiple vertical support blocks that house the rollers, gear train, and motor. Material enters through the guiding roller on the left and is pulled across the structure by a motor-driven pulling roller on the

right. The system ensures linear motion with minimal deviation, suitable for strip-based transport and scanning mechanisms.

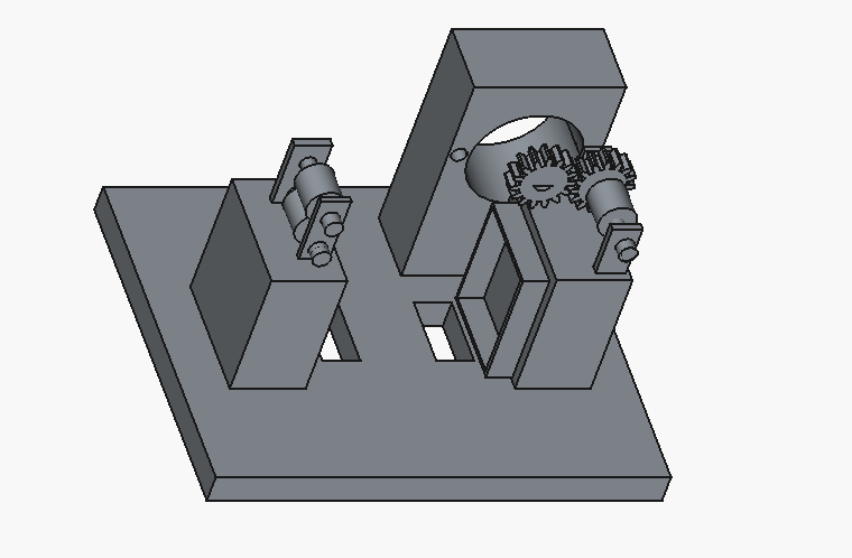

Figure 3.2: Top View Showing Alignment and Roller Placement

3.2 Roller Assembly Design

The system features two roller subassemblies:

- **Guiding Roller Assembly**: Positioned on the left, it comprises two vertically stacked cylindrical rollers. These passively grip and guide the material through the setup. The roller bracket allows tool-free maintenance and roller replacement.
- **Pulling Roller Assembly**: Located on the right, this set of rollers performs active material pulling. The bottom roller is driven by a gear mechanism connected to a motor. The upper roller provides counter-pressure to ensure effective traction.

Both roller systems use fixed brackets mounted on raised supports to ensure parallelism and consistent pressure during rotation.

3.3 Motor and Gear Mechanism Integration

The mechanism includes a large circular housing intended for a compact stepper or DC motor. A gear mounted on the motor shaft engages

with a secondary gear attached to the pulling roller shaft. This gear pair forms a simple spur gear train that translates motor torque into roller rotation. Gear teeth are matched for synchronized engagement, and the entire system is aligned for low-friction transmission.

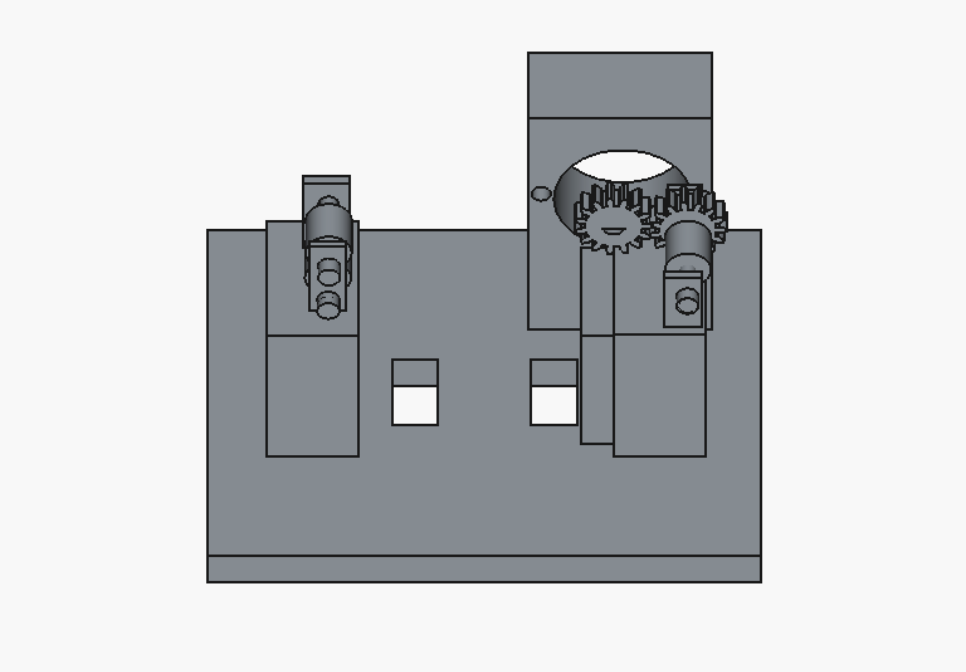

Figure 3.3: Oblique View Showing Gear Train and Motor Slot

3.4 Sensor Integration Slot

A dedicated rectangular chassis is incorporated adjacent to the pulling roller assembly to accommodate a color-based sensor module. This slot is strategically positioned to align directly with the material strip's path as it moves through the rollers, enabling accurate, real-time detection of color patterns, markings, or variations on the surface.

The cavity is designed to fit compact sensor modules such as the **TCS34725** or **APDS-9960**, which offer digital color sensing capabilities. These sensors can be used for a range of purposes—such as detecting color-coded tags, classifying samples based on color intensity, or triggering events based on predefined color thresholds.

To minimize optical distortion or interference, the sensor window faces the strip through a clear, sealed opening. This ensures reliable sensing while protecting the electronics from environmental exposure. Provision has been made within the chassis to accommodate sensor PCBs, and wire routing channels are embedded in the baseplate to

streamline connections to the processing unit or microcontroller.

The integration of such a sensor enhances the mechanism's potential for automation and intelligent decision-making, making it suitable for applications involving quality inspection, sample classification, or closed-loop feedback control.

3.5 Baseplate and Mounting Slots

The baseplate not only provides structural support but also offers functional features like:

- Cutouts beneath the roller path for sensor exposure or strip exit.
- Slits and holes for clamping the entire assembly to an external rig or enclosure.
- Raised motor and roller platforms for mechanical stability and vibration isolation.

The design is highly symmetric and compact, allowing it to be embedded easily into larger mechanical or test setups.

3.6 Modularity and Expandability

The roller feed mechanism is designed with flexibility in mind. Some of its customizable aspects include:

- **Roller Dimensions**: Adjustable diameter and width to accommodate varying material sizes.
- **Motor Type**: Supports DC, stepper, or servo motors with matching mounts and gear interfaces.
- **Sensor Type**: Adaptable sensor slot for optical, magnetic, or proximity sensing.
- **Gear Ratios**: Swappable gear pairs to modify torque and speed based on application.

All parts can be manufactured via 3D printing, CNC milling, or laser cutting, making this a versatile platform for experimental setups or small-scale automation.

3.7 Conclusion

This chapter detailed the structural and functional aspects of a modular roller feed mechanism. By combining a driven pulling system, passive guiding rollers, and an integrated sensing slot, the setup achieves precise and controlled strip movement. The design is open to mechanical and electrical customizations, making it ideal for prototyping, research, or educational applications.

Chapter 4

Circuit Architecture and Component Overview

This chapter presents a detailed examination of the architectural design and key components employed in the two successive PCB versions—the Basic LM7805 Regulated Board and the Advanced BQ25185 Based Optimized Board. A comprehensive understanding of each component's role, specifications, and integration rationale provides important context for appreciating the system design complexities, power management strategies, and functional capabilities achieved.

4.1 Seeed Studio XIAO ESP32-S3 Sense Microcontroller Module

At the core of the system is the Seeed Studio XIAO ESP32-S3 Sense microcontroller module, a compact yet powerful solution designed specifically for high-performance IoT and embedded vision applications. This module was chosen for its unique combination of advanced processing capabilities, flexible peripheral integrations, and onboard sensor support, making it a versatile platform for a wide range of embedded systems.

- **Processor Architecture:** This module utilizes dual-core Xtensa LX7 processors running at up to 240 MHz, offering substantial compute resources for real-time signal processing, sensor fusion, and wireless protocol stack execution. The architecture supports branch predication, SIMD instructions, and hardware loops, which boost performance in intensive tasks like machine learning inference.

- **Memory Resources:** On-chip SRAM combined with external SPI flash support provides ample space for firmware, buffers, and sophisticated application code, enabling local data processing and reducing cloud dependency.
- **Communication Interfaces:** Rich connectivity options include SPI, I2C, UART, PWM, and ADCs. This flexibility facilitates direct integration with peripheral devices such as the SX1262 LoRa transceiver (via SPI), sensor arrays (via I2C/ADC), and actuator controllers (via PWM or GPIO).
- **Wireless Capabilities:** Native Wi-Fi 6 and Bluetooth 5.0 support enhance local and mesh network communications, complementing the long-range LoRa capabilities, making the device ideal for hybrid connectivity scenarios.
- **Onboard Sensors and Camera Interface:** The "Sense" variant is equipped with capacitive touch sensors and a dedicated camera interface (DVP). This enables direct connection of image sensors, supporting applications like visual recognition, environmental monitoring, and smart surveillance.
- **Modular Footprint Compatibility:** The Xiao ESP32-S3 Sense standard footprint enables compatibility with popular off-the-shelf modules, easing prototyping and supply chain considerations. The optimized PCB design mounts the MCU on the bottom layer, ensuring the camera lens has an unobstructed field of view through the enclosure.

4.2 SX1262 LoRa Communication Module

The Semtech SX1262 serves as the wireless transceiver for long-range low-power communication, critical for remote sensing and telemetry:

- **Modulation and Range:** Supports LoRa modulation, offering kilometers of range with low power consumption, enabling applications in rural, industrial, and expansive area networks.
- **Frequency Bands:** Operates in global ISM bands (e.g., 868 MHz, 915 MHz), compliant with regional regulations.

- **SPI Interface and Control Pins:** Connected to the ESP32-S3 via SPI for data and configuration with dedicated GPIO lines managing interrupts (DIO1), reset (RST), and status (BUSY) signals essential for synchronous communication and power management.
- **Stacked Mounting:** Physically stacked atop the ESP32-S3 module in the optimized design to minimize PCB footprint and signal interference.

4.3 Power Regulation and Management

Power efficiency and reliability are addressed through two distinct approaches reflecting the project's evolving complexity:

4.3.1 LM7805 Linear Regulator (Basic Design)

The classic LM7805 linear voltage regulator offers a straightforward solution to supply a clean 5V rail from a higher DC voltage source. Paired with input and output decoupling capacitors (C3 and C4), it reduces ripple and transient noise. Though cost-effective and simple, the LM7805 dissipates excess voltage as heat, lowering efficiency especially in battery-powered or solar-powered environments.

4.3.2 BQ25185 Battery Management and TPS61023 Boost Converter (Optimized Design)

The advanced power system integrates:

- **BQ25185:** A comprehensive battery management solution that supports single-cell Li-ion/Li-Po charging with power-path management. It accommodates dual power inputs (solar panel and USB Type-C), performing automatic source selection, overcharge/discharge protection, and temperature monitoring. Maximum Power Point Tracking (MPPT) algorithms improve solar charging efficiency, crucial for off-grid deployments.
- **TPS61023:** A synchronous boost converter that raises battery voltage to a consistent 5V output, enabling system operation even when battery voltage falls below the required threshold. This

converter maintains high efficiency and reduces electromagnetic interference through controlled switching and integrated compensation.

This power subsystem enables dynamic, safe, and efficient energy management suited for portable, solar-powered, and battery-backed embedded applications.

4.4 High-Current Driver and Switching Components

- **ULN2003A Darlington Driver:** Provides a reliable interface for driving inductive loads such as stepper motors, relays, and solenoids using low-current control signals from the microcontroller. It includes internal clamp diodes to suppress voltage spikes, protecting device longevity and ensuring safe operation.
- **N-Channel MOSFET Switching:** Implemented as low-side switches in several control circuits, MOSFETs enable efficient, high-speed switching with low voltage drop and heat dissipation. Their gate terminals are driven by MCU GPIOs, allowing flexible load control.

4.5 Connector Interfaces and Expandability

Connectors are strategically placed and specified to promote modularity and testing convenience:

- **USB Type-C Port:** Consolidates charging, programming, and data transfer via a single compact USB-C interface. This standardization simplifies user interaction and reduces board complexity.
- **Test and Expansion Headers:** Multiple pin headers expose MCU control lines, power rails, and sensor signals, facilitating prototyping, debugging, and integration with other modules or external circuitry.

- **Power Input Connectors:** Support solar panels, battery packs, or wall adapters, maintaining flexibility for diverse deployment environments.

4.6 Mechanical Design and Layer Stackup

Mechanical and manufacturing considerations are paramount, especially in the optimized PCB:

- **Four-Layer PCB Stackup:** The optimized design employs a four-layer PCB with dedicated inner layers for power and ground planes. This multilayer configuration dramatically improves signal integrity, reduces electromagnetic interference, and provides low-impedance paths for current flow.
- **Component Placement:** The ESP32-S3 module is positioned on the bottom side for camera accessibility, while the SX1262 module is stacked directly above, conserving board space and enhancing signal coupling. Headers and connectors are positioned for easy cable management and mechanical robustness within enclosures.
- **Thermal Management:** Careful copper pours and trace widths ensure heat dissipation from high-current components, particularly in the power regulation circuit.

4.7 Summary

By carefully selecting and arranging high-performance components—ranging from the advanced ESP32-S3 Sense MCU and SX1262 LoRa transceiver to sophisticated power management ICs and robust drivers—these designs embody the balance between functionality, reliability, and scalability. The architectural choices underpin the two-stage design approach: starting from a foundational LM7805-based board and progressing towards a feature-rich, modular, four-layer optimized PCB capable of addressing complex, real-world embedded sensing and control challenges.

Chapter 5

Basic PCB Design with LM7805

This chapter details the development of a foundational printed circuit board (PCB) design featuring core components for regulated power delivery, robust driver interfacing, and clear signal routing. The board integrates the LM7805 voltage regulator for stable 5V power and the ULN2003A driver IC to safely interface digital logic with relays, indicators, or other higher-current loads. The design was executed in eSim, following best practices in schematic capture, footprint mapping, layout, and validation.

5.1 Schematic Design and Circuit Overview

The schematic for the basic board, constructed in eSim, includes:

- **Power Regulation (X1):** The LM7805 voltage regulator is responsible for converting a higher, variable DC input to a fixed 5V output, supplying power to all onboard circuits. Capacitors C3 (0.33uF) and C4 (0.1uF) are positioned at the regulator's input and output, respectively, to stabilize voltage and suppress high-frequency noise, ensuring reliable performance.
- **ULN2003A Driver (U2):** The ULN2003A provides a buffer between microcontroller GPIOs and external actuators. It allows small control currents to switch high or inductive loads by means of its internal darlington transistor arrays and integrates flyback diodes for inductive load protection, preventing voltage spikes that could otherwise damage circuitry.
- **Connectors and Headers:** The POWER1 connector supplies raw input voltage to the regulator, while DRIVERCONTROL1 and LEDCONTROL1 headers facilitate organized wiring between

the microcontroller and the driver or indicators. This structure supports practical bench testing and simplifies integration in broader systems.

- **Low-side NMOS Switch (MN1):** Used for efficient switching of output loads to ground from logic signals, the NMOS enables rapid and reliable on/off control of LEDs or other low-power loads, neatly interfacing logic to the power side of the circuit.

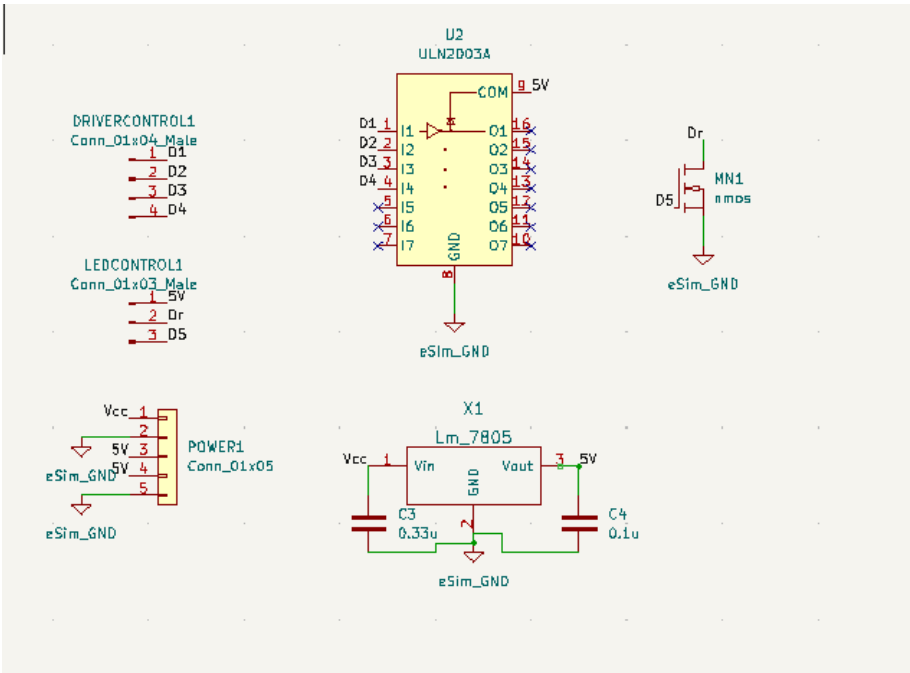

Figure 5.1: Schematic diagram of the basic PCB design, including LM7805 regulator, ULN2003A driver, and connector arrangement as created in eSim.

5.2 Symbol-to-Footprint Assignment

Each component in the schematic is mapped to a precise physical footprint, ensuring that device pins correspond correctly to PCB pads. For this board, standard through-hole parts (DIP for ULN2003A, TO-220 for LM7805, and 0.1" or 0.2" headers) were selected, supporting reliable manual soldering and mechanical durability. eSim's library was utilized to reduce footprints errors and to streamline the board fabrication process.

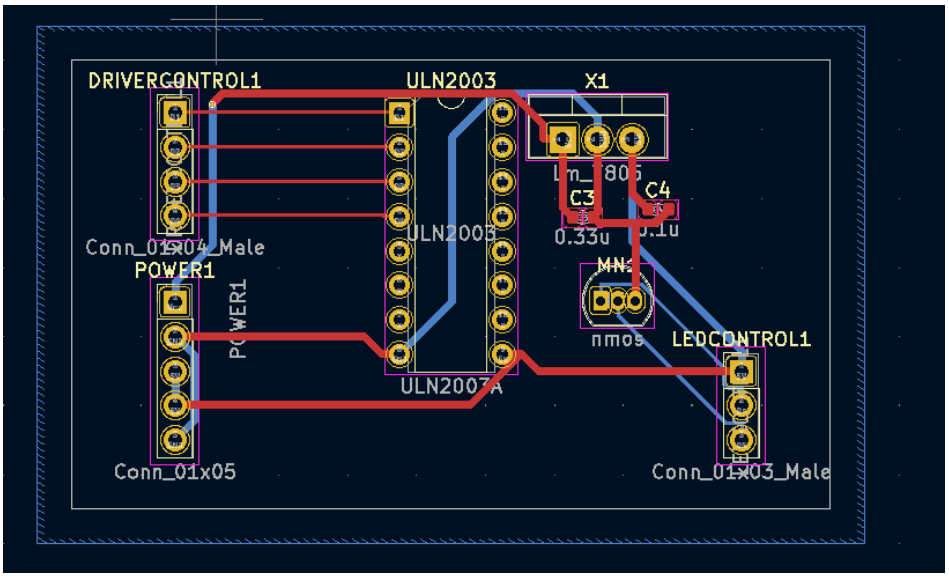

Figure 5.2: Example of symbol-to-footprint assignment used for the basic PCB, supporting accessible prototyping and assembly.

5.3 PCB Layout and Routing

The layout was crafted to produce a logical, uncluttered, and electrically robust design.

5.3.1 Component Placement

The LM7805 regulator and its bypass capacitors are placed close to the power entry to minimize voltage drops and maximize filtering effectiveness. The ULN2003A is centrally located, with its input pins facing the DRIVERCONTROL1 header and outputs routed efficiently to the corresponding header or load.

5.3.2 Routing Strategy

Wider traces are used for the primary 5V and ground nets, supporting higher current without excessive heating or voltage sag. Signal traces are routed to avoid crosstalk and noise, with explicit separation between input controls, output loads, and power traces. Cornering is minimized to reduce impedance discontinuities.

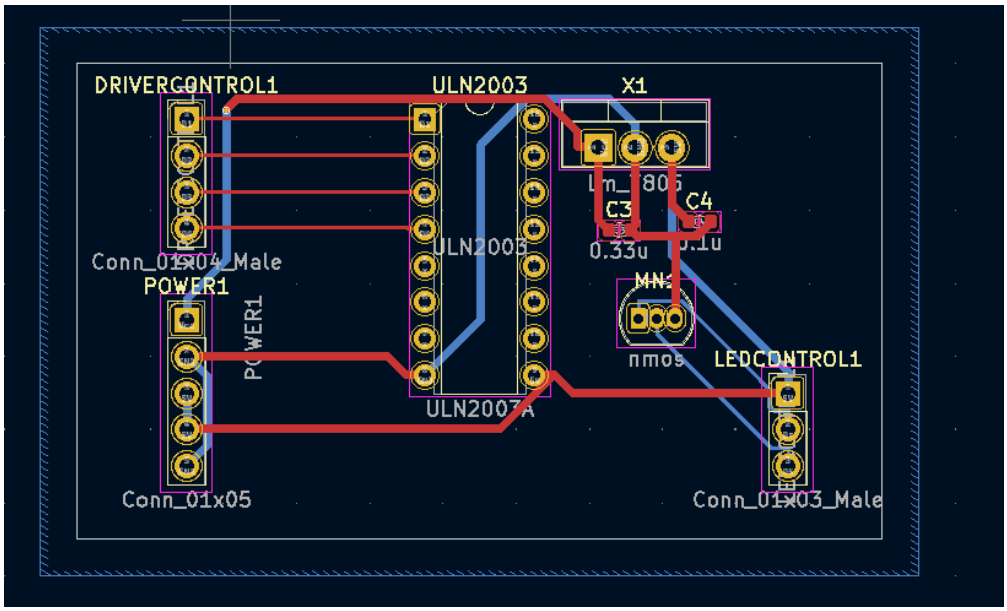

Figure 5.3: PCB top and bottom copper layer routing as visualized in eSim, highlighting organized paths for all signals and power lines.

5.3.3 Copper Layer and Net Analysis

Copper traces are displayed in the layout to verify the continuity of all nets and to confirm there are no unintentional shorts between signal layers. Traces serving higher loads are thickened, and polygonal fills are used for ground to lower resistance and improve EMC.

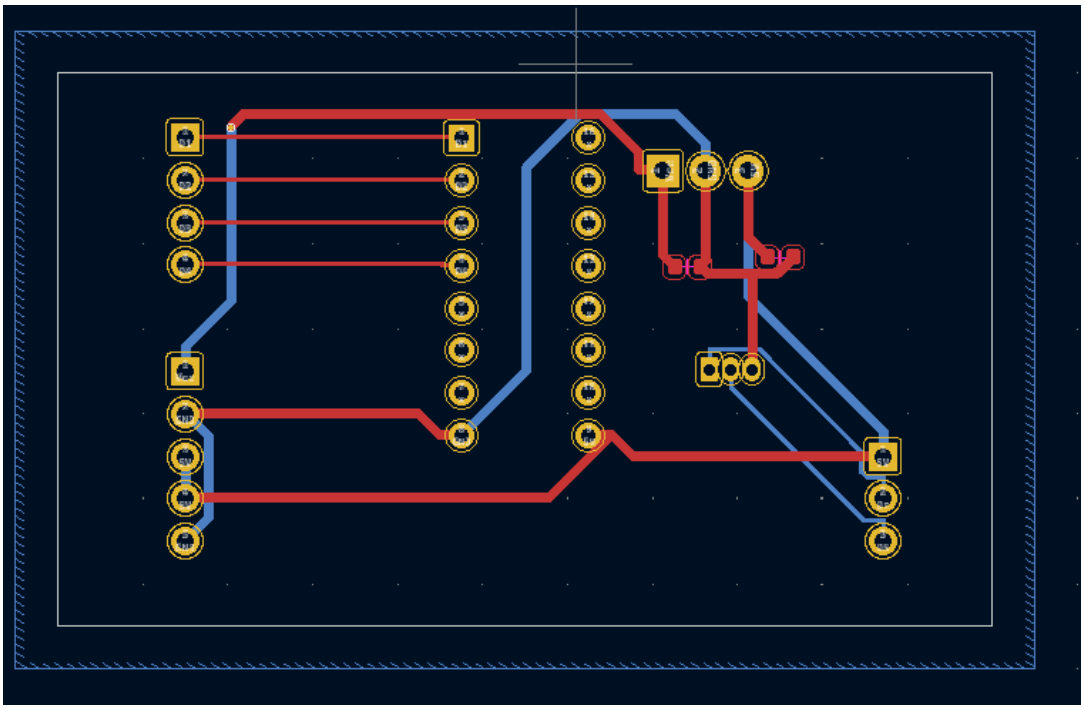

Figure 5.4: Copper layer visualization from eSim, showing detailed trace routing for both power and signal paths.

5.4 3D Board Visualization

A 3D rendering of the finished layout is generated in eSim to inspect correct pin header orientation, mechanical clearances, and the insertion heights of through-hole devices. This model allows for pre-assembly verification, reducing risks of assembly errors or mechanical interference in the final enclosure.

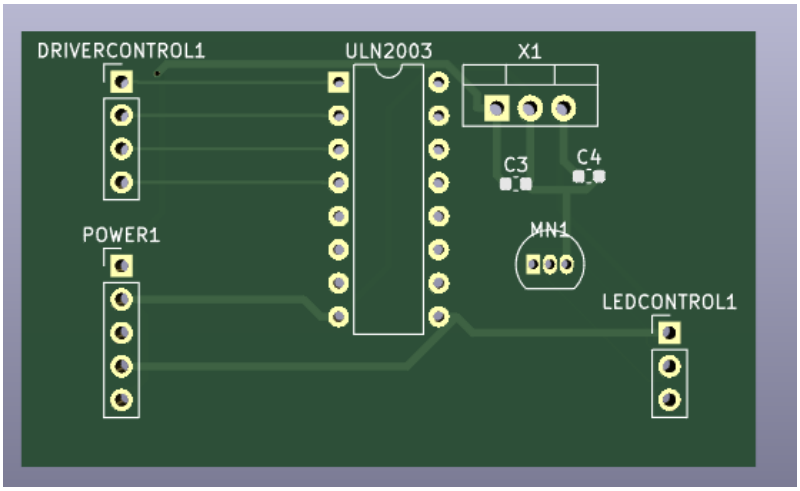

Figure 5.5: 3D view of the basic PCB design from eSim, useful for verifying mechanical and assembly constraints.

5.5 Design Rule Checking (DRC)

A comprehensive DRC was performed within eSim to catch violations such as trace clearance, minimum feature size, and other fabrication constraints prior to Gerber export and manufacturing.

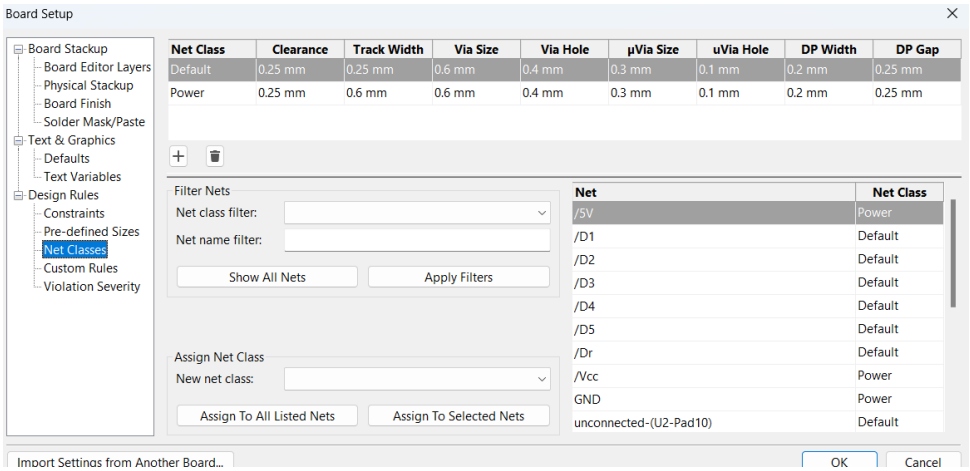

Figure 5.6: Design Rule Check (DRC) results for the basic PCB, confirming compliance with fabrication requirements.

5.6 Summary

This basic PCB chapter provided a reliable introduction to core embedded hardware principles using the LM7805 and ULN2003A, while following good practices in schematic capture, footprint assignment, layout, and design validation. The confidence and lessons from this prototype informed the evolution toward the advanced, optimized PCB designs described in the subsequent chapter.

Chapter 6

Optimized PCB Design using BQ25185 and TPS61023

This chapter provides a comprehensive account of the design, verification, and realization of a printed circuit board (PCB) for an integrated ESP32-S3 microcontroller and LoRa SX1262 communication system. The entire PCB development workflow—from schematic design to 3D board visualization—was completed using the open-source eSim EDA suite. This modular and space-efficient architecture is intended for embedded sensor and control applications requiring wireless connectivity, robust power management, and peripheral control.

6.1 Schematic Design and Circuit Integration

The circuit schematic, meticulously drawn in eSim, serves as the backbone for the entire hardware system. The design is centered around the ESP32-S3 microcontroller and SX1262 LoRa module, which are physically stacked, with the SX1262 positioned directly above the ESP32-S3. The standardized Seeed Studio Xiao ESP32-S3 Sense footprint is adopted for the MCU, allowing for compatibility with widely available modules and simplified integration.

Special consideration is given to component placement: the MCU is deliberately mounted on the bottom side of the PCB. This orientation ensures the onboard camera has an unobstructed field of view, critical for applications involving imaging, visual feedback, or sensor fusion. Additionally, THT (Through-Hole Technology) pads are provided, facilitating robust electrical and mechanical connections as well as user modifications or system expansion.

The schematic reflects a single USB Type-C port for both programming and charging, providing a cost-effective and straightforward interface. Peripheral connections are kept accessible, while high-quality layout practices—such as careful decoupling, clear net labeling, and functional clustering—optimize both signal integrity and ease of debugging.

6.2 Advanced Power Management: Mimicking the Adafruit BQ25185+5V Boost Board

A significant aspect of this board's design is its advanced power management subsystem, drawing inspiration from the Adafruit BQ25185+5V Boost board. This functionality is implemented and further enhanced by the manual integration of the BQ25185 battery management IC and the TPS61023 boost converter directly within the schematic.

6.2.1 Integration of BQ25185 and TPS61023

- **BQ25185:** This highly integrated battery management IC performs efficient charging and protection for a single-cell Li-ion or Li-Po battery. It manages power path control, monitors charging status, and implements safety features including overvoltage, overcurrent, and thermal protection. Its versatile input allows for both solar panel and USB Type-C energy sources, as reflected in the schematic's port configuration.
- **TPS61023:** Serving as a synchronous boost converter, the TPS61023 elevates the battery voltage to a steady 5V output—crucial for reliable system operation, even when battery voltage falls below nominal. This ensures uninterrupted power for the ESP32-S3, SX1262, sensor payloads, and user interface circuits.

6.2.2 Solar Power and USB Type-C Charging

The power architecture efficiently supports both solar energy harvesting and USB Type-C based direct charging:

- **Solar Input:** The BQ25185 dynamically manages fluctuating solar panel voltages, leveraging its high-input-voltage tolerance and maximum power point tracking (MPPT) capabilities. This integration enables sustainable off-grid deployments and uninterrupted field operation.
- **Type-C Charging:** The single Type-C connector simplifies user interface and system cost by combining data and power roles. The power path logic ensures seamless handover between USB and solar input sources based on dynamic availability.

6.2.3 System Capabilities and Reliability

By directly integrating the BQ25185 and TPS61023 functions, this custom board matches and extends the Adafruit BQ25185+5V Boost's capabilities:

- Robust and continuous 5V supply for all onboard and auxiliary modules
- Safe, adaptive Li-ion/Li-Po charging from both solar and USB sources
- Reliable system behavior in portable, remote, or mobile deployments
- Seamless and safe power bank charging via the streamlined Type-C interface

These enhancements make the board ideal for operation in advanced sensor platforms, IoT deployments, and autonomous edge computing scenarios.

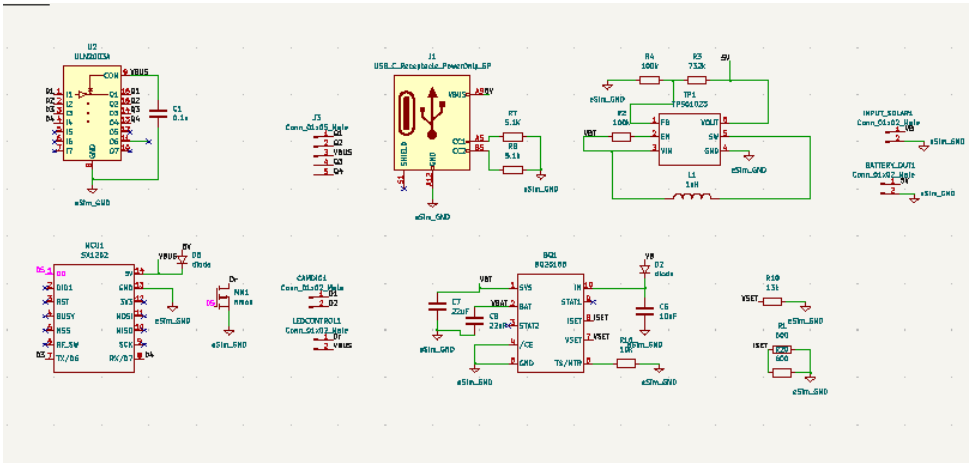

Figure 6.1: Schematic diagram of the integrated ESP32-S3 and LoRa sensor-control PCB as designed in eSim.

6.3 Symbol-to-Footprint Assignment

Careful symbol-to-footprint assignment is fundamental for accurate PCB realization. Each circuit symbol—including the ESP32-S3 (standard Xiao Sense footprint), SX1262, Type-C port, and passive and active components—is paired with a precise mechanical footprint from the eSim library or custom-built for the application. THT footprints are used for key connection pads to enhance board durability and offer easier prototyping/fabrication.

Symbol : Footprint Assignments

1	BATTERY_OUT1	Conn_01x02_Male	Connector_PinHeader_2.54mm:PinHeader_1x02_P2.54mm_Vertical
2	BQ1	BQ25185	Package_SON:WSON-10-1EP_4x3mm_P0.5mm_EP2.2x2mm
3	C1	0.1u	Capacitor_SMD:C_0603_1608Metric
4	C6	10uF	Capacitor_SMD:C_0603_1608Metric
5	C7	22uF	Capacitor_SMD:C_0603_1608Metric
6	C8	22uF	Capacitor_SMD:C_0603_1608Metric
7	CAMDIG1	Conn_01x02_Male	Connector_PinHeader_2.54mm:PinHeader_1x02_P2.54mm_Vertical
8	D2	diode	Diode_SMD:D_SOD-123
9	INPUT_SOLAR1	Conn_01x02_Male	Connector_PinHeader_2.54mm:PinHeader_1x02_P2.54mm_Vertical
10	J1	USB_C_Receptacle_PowerOnly_6P	Connector_USB:USB_C_Receptacle_GCT_USB4085
11	J2	USB_C_Receptacle_PowerOnly_6P	Connector_USB:USB_C_Receptacle_GCT_USB4085
12	J3	Conn_01x05_Male	Connector_PinHeader_2.54mm:PinHeader_1x05_P2.54mm_Vertical
13	L1	1uH	Inductor_SMD:L_1008_2520Metric
14	LEDCONTROL1	Conn_01x02_Male	Connector_PinHeader_2.54mm:PinHeader_1x02_P2.54mm_Vertical
15	MCU1	SX1262	xiao ESP32S3_PCB:MOUDLE14P-SMD-2.54-21X17.8MM
16	MN1	nmos	Package_TO_SOT_THT:TO-92_Inline
17	R1	600	Resistor_SMD:R_0603_1608Metric
18	R2	100k	Resistor_SMD:R_0603_1608Metric
19	R3	732k	Resistor_SMD:R_0603_1608Metric
20	R4	100k	Resistor_SMD:R_0603_1608Metric
21	R5	5.1K	Resistor_SMD:R_0603_1608Metric
22	R6	5.1k	Resistor_SMD:R_0603_1608Metric
23	R7	5.1K	Resistor_SMD:R_0603_1608Metric
24	R8	5.1k	Resistor_SMD:R_0603_1608Metric
25	R16	10k	Resistor_SMD:R_0603_1608Metric
26	R19	13k	Resistor_SMD:R_0603_1608Metric
27	R20	600	Resistor_SMD:R_0603_1608Metric
28	TP1	TPS61023	Package_TO_SOT_SMD:SOT-563
29	U2	ULN2003A	Package_DIP:DIP-16_W7.62mm

Figure 6.2: Symbol-to-footprint assignment table for all components in the PCB project, generated using eSim.

6.4 PCB Layout

The layout effort transforms schematic intent and mechanical constraints into a manufacturable, high-performance hardware product. This version advances the previous design by deploying a four-layer stackup. The four-layer approach enables dedicated power and ground planes, providing superior noise suppression, improved EMI shielding, and robust high-current delivery, which is essential for RF modules and high-speed MCUs.

6.4.1 Signal Integrity and Segregation

High-frequency signal lines used for SPI between the ESP32-S3 and SX1262, as well as power traces and control lines, are carefully segregated to minimize crosstalk and EMI. The use of a four-layer board allows sensitive analog, RF, and power domains to be isolated by internal planes, and critical nets to be routed with controlled impedance.

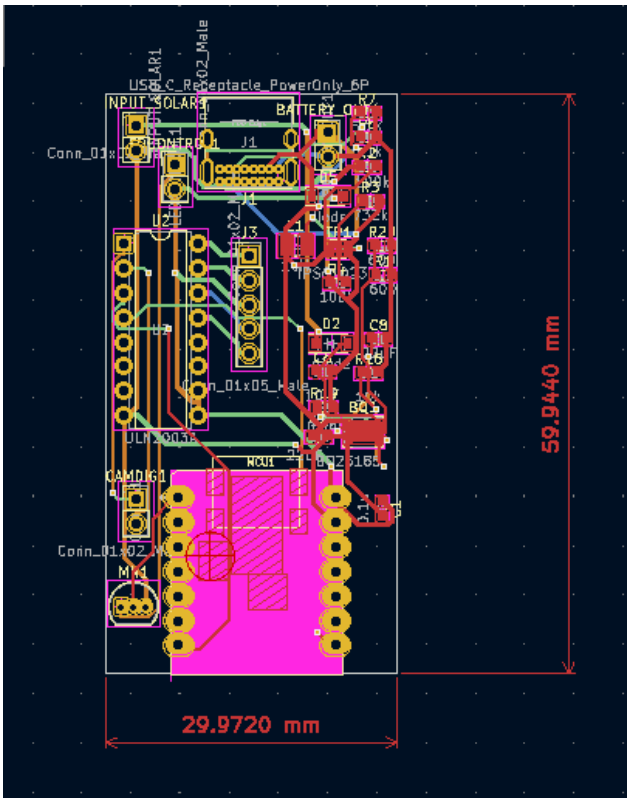

Figure 6.3: PCB layout view showing the organized component arrangement and optimized routing in eSim.

6.4.2 Routing Optimization

Advanced routing in four layers provides both signal and power integrity, with the internal layers primarily dedicated to power (solid 5V) and ground returns, and the outer layers used for signals and compact component connections. Length-matched, impedance-controlled routing techniques are used for timing-critical and RF nets.

6.4.3 Ground Plane and Power Management

A solid ground plane is maintained throughout the board for minimal ground bounce and maximum EMC performance. Power distribution is stabilized with low-impedance paths across the plane, and decoupling capacitors are strategically populated close to all ICs, not just the MCU, to suppress high-frequency noise and voltage dips.

6.4.4 Component Placement and Modular Stacking

With the MCU at the base and the SX1262 mounted directly above, board stacking is optimized for compactness and functional accessibility. Camera functionality is prioritized by ensuring the ESP32-S3 (Xiao Sense) footprint's aperture aligns with the enclosure's camera window, preventing obstructions. THT pads remain accessible at the board's periphery for expandability and manual assembly.

6.4.5 Mechanical Considerations

Connectors, mounting holes, and expansion headers are carefully aligned for robust mechanical integrity. The single Type-C port is optimally placed for easy cable management and secure attachment, reducing risk of physical damage over repeated usage.

Collectively, these features yield a reliable, scalable PCB ready for demanding modular wireless sensing, imaging, and control applications.

6.5 Design Rule Checking (DRC) and Net Class Validation

A thorough DRC was performed, taking full advantage of the four-layer architecture to enforce spatial and electrical design rules:

- **Clearances:** Enhanced for tighter four-layer geometries, ensuring compliance with advanced fabrication standards.
- **Trace Widths:** Optimized per net class—power traces are especially robust to carry higher currents with minimal temperature rise.
- **Via and Pad Sizes:** Verified for mechanical/routing reliability, accounting for stacked vias and internal layer transitions.
- **Net Classes:** Defined for core power, ground, and all signal domains with dedicated rules to handle high-speed data and RF performance.

These DRC and net class checks ensure that the design is not only functional but manufacturable, mitigating risks of shorts, opens, or signal/power integrity violations. Layer stackup and net assignments are aligned with modern EMS fabrication capabilities for long-term reliability.

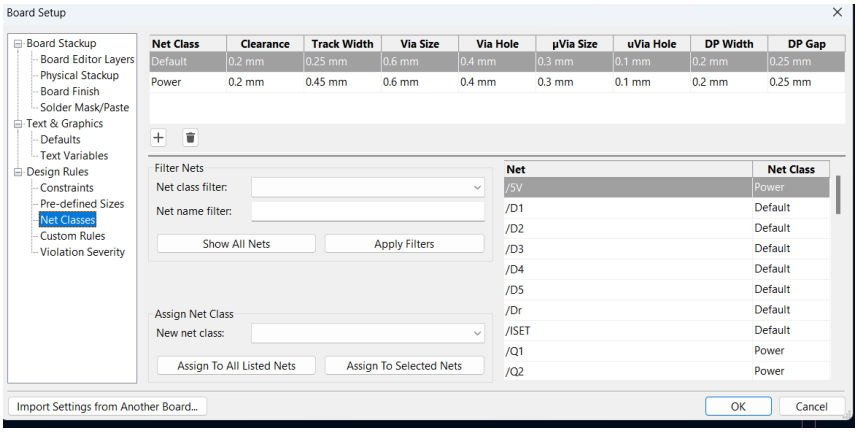

Figure 6.4: Results of the Design Rule Check (DRC) and net class settings for different functional domains within the board.

6.6 3D Board Visualization

A 3D rendering of the complete, assembled board is generated in eSim. This visualization is crucial for confirming mechanical compat-

ibility—verifying that the camera and connectors align as intended, the stacking position of the SX1262 does not interfere with the camera's field of view, and that all THT pads and expansion headers are accessible for downstream assembly.

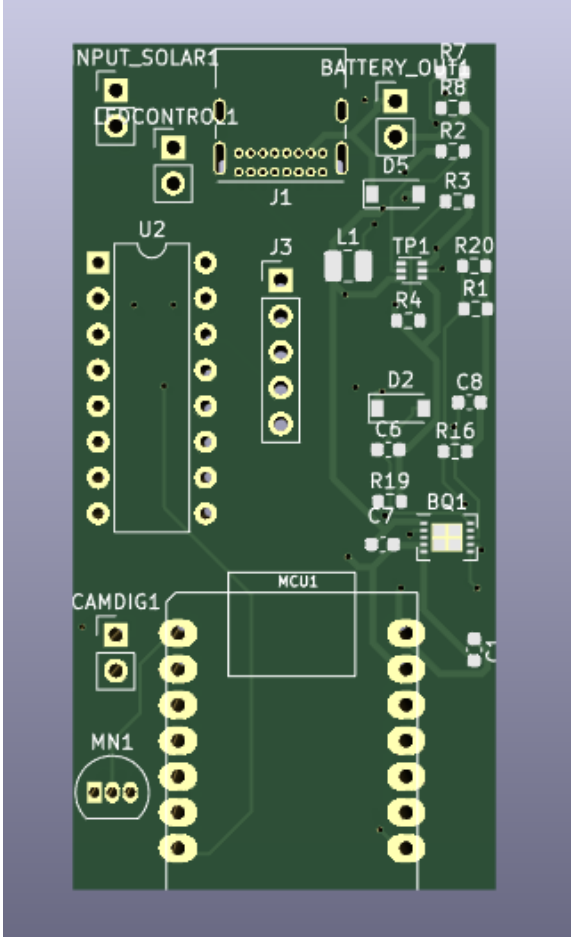

Figure 6.5: 3D rendered view of the PCB, showing actual component heights, placement, and physical clearances.

6.7 Copper Layer Visualization

Copper layer visualization in eSim highlights the clean separation and management of signals, uninterrupted ground planes, and distributed power nets. The four-layer stackup is evident, with distinct layers for high-speed signals, power planes, and shielding. These views ensure that the final physical board strictly matches the intended logical and functional architecture, supporting rigorous design-for-manufacturing goals and high-speed circuit requirements.

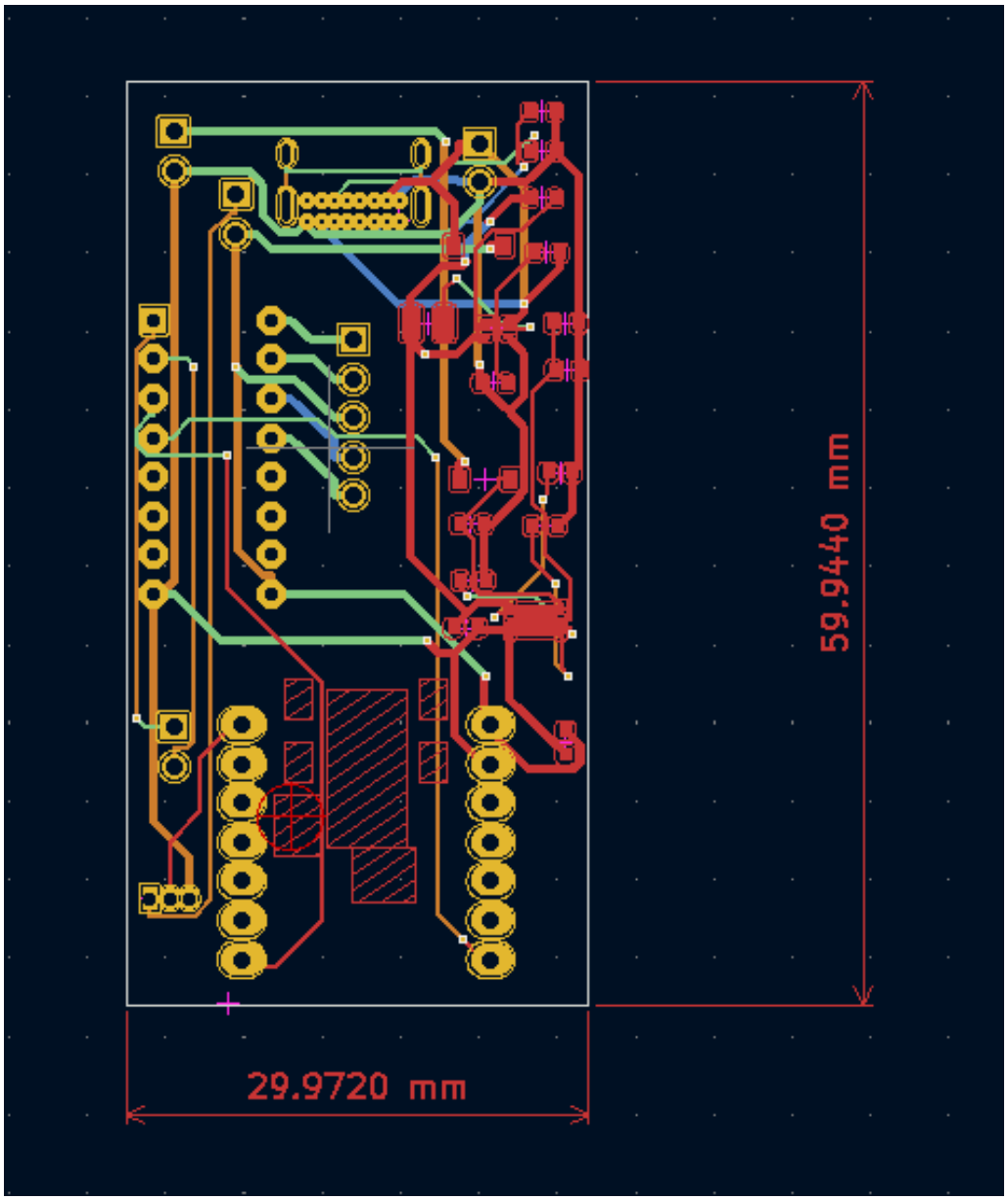

Figure 6.6: Copper layer visualization from eSim, highlighting signal traces, power planes, and critical pours for thermal and electrical performance.

6.8 Summary

This optimized PCB design incorporates a high degree of mechanical and electrical integration by adopting advanced power management, a four-layer stackup, precision module stacking, and strong DRC/net class compliance. These enhancements markedly improve scalability, noise immunity, power delivery, and physical robustness—culminating in a professionally engineered platform for demanding embedded sensing and control solutions.

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