Summer Fellowship Report

On

Integrated Circuit Design using Subcircuit feature of eSim

Submitted by

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I take this opportunity to express my deepest gratitude to the entire FOSSEE team at IIT Bombay for providing me with this wonderful opportunity to work on the design and integration of sub-circuits using eSim . The internship has given me valuable exposure to open-source tools, their real-world applications, and a deeper understanding of electronic design and simulation.

I am especially grateful to Prof. Kannan M. Moudgalya for his constant inspiration and vision behind the FOSSEE initiative. His commitment towards promoting open-source software for education and research has created numerous opportunities for students like me to gain hands-on experience and contribute to the open-source community. His farsighted leadership and encouragement have been truly motivating throughout this journey.

I would like to convey my heartfelt thanks to Mr. Sumanto Kar for his constant support, guidance, and encouragement throughout the internship. His valuable insights, timely feedback, and patient mentoring have been instrumental in helping me overcome challenges and successfully complete my project objectives. His dedication towards guiding interns like me has made this journey both enlightening and enjoyable.

I also sincerely appreciate the entire FOSSEE initiative for its efforts in empowering students and researchers by making tools freely accessible, thus removing the barriers imposed by costly commercial software. This mission not only fosters innovation but also strengthens the open-source ecosystem, allowing young learners to actively contribute and grow.

This internship has been a memorable and rewarding phase of my academic journey. The knowledge, skills, and experiences I have gained will undoubtedly serve as a strong foundation as I move forward in my career in the semiconductor and VLSI domain.

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Chapter 1

Introduction

1.1 eSim

eSim (Electronic Simulation) is an open-source Electronic Design Automation (EDA) tool developed by the FOSSEE (Free/Libre and Open Source Software for Education) project at IIT Bombay. It is an initiative supported by the Ministry of Education, Government of India, aimed at promoting the use of open-source software in academia and industry.

One of the key strengths of eSim lies in its user-friendly interface and support for customized subcircuit development, making it ideal for educational institutions and research-based applications. It enables students, educators, and engineers to model real-world systems, verify circuit behavior, and perform parameter sweeps or transient analysis efficiently. Moreover, eSim includes Python-based simulation capabilities and Scilab integration, enhancing its computational power and flexibility for system-level design.

1.2 Ngspice

Ngspice is an open-source mixed-level/mixed-signal circuit simulator based on the original SPICE (Simulation Program with Integrated Circuit Emphasis) engine developed at the University of California, Berkeley. As a part of the GNU project, Ngspice extends the capabilities of its predecessors by incorporating advanced simulation features, support for digital and behavioral modeling, and enhanced convergence algorithms. It is widely used for simulating analog, digital, and mixed-signal circuits, making it a valuable tool in both academic and professional electronics design environments.

1.3 Ki-Cad

Ki-Cad is an open-source electronics design automation (EDA) software suite used for schematic capture and printed circuit board (PCB) layout design. Originally developed by Jean-Pierre Charras and now maintained by an active global commu-

nity, KiCad has grown into one of the most powerful free alternatives to proprietary PCB design tools.

It allows users to design multi-sheet schematics, create custom libraries, and route multilayer PCBs with precision. The software also supports 3D visualization of PCB layouts, giving designers a realistic view of the final board before fabrication.

1.4 GHDL

GHDL is an open-source VHDL (VHSIC Hardware Description Language) simulator that enables the analysis, compilation, and simulation of digital circuit designs entirely within a command-line or scriptable environment. Unlike many commercial VHDL tools, GHDL supports a complete simulation flow without relying on external graphical interfaces, making it lightweight, efficient, and highly suited for automated workflows. It adheres to the IEEE 1076 VHDL standard, allowing users to write synthesizable and testbench code for complex digital systems and verify their behavior through waveform generation and signal tracing.

GHDL is widely used in academic, research, and open-source hardware communities for its reliability, performance, and full compatibility with common digital design workflows. It can be easily integrated with tools like GTKWave for waveform viewing and with open-source EDA platforms such as eSimfor co-simulation and testing. GHDL also supports mixed-language simulation when combined with tools like Yosys and Verilator, enabling seamless integration of VHDL and Verilog modules. As a fully free and open-source tool, GHDL empowers students and developers to prototype, test, and validate digital circuits without the limitations of costly commercial licenses.

Chapter 2

Features of eSim

The objective behind the development of eSim is to provide an open source EDA solution for electronics and electrical engineers. The software should be capable of performing schematic creation, PCB design and circuit simulation (analog, digital and mixed-signal). It should provide facilities to create new models and components. Thus, eSim offers the following features -

1. Schematic Creation: eSim provides an easy-to-use graphical interface for drawing circuit schematics, making it accessible for users of all levels. Users can drag and drop components from the library onto the schematic, simplifying the design process. Comprehensive editing tools allow for easy modification of schematics, including moving, rotating, and labeling components.

2. Circuit Simulation: eSim supports SPICE (Simulation Program with Integrated Circuit Emphasis), a standard for simulating analog and digital circuits. Users can perform various types of analysis such as transient, AC, and DC, providing insights into circuit behavior over time and frequency.An integrated waveform viewer helps visualize simulation results, aiding in the analysis and debugging of circuit designs.

3. PCB Design: The PCB layout editor allows users to place components and route traces with precision. eSim includes DRC capabilities to ensure that the PCB design adheres to manufacturing constraints and electrical rules. Users can generate Gerber files, which are standard for PCB fabrication, directly from their designs.

4. Subcircuit Feature This feature enables users to create complex circuits by integrating smaller, simpler subcircuits, promoting modular and hierarchical design approaches. Subcircuits can be reused in different projects, saving time and effort in redesigning common circuit elements.

5. Open Source IntegrationeSim integrates several open-source tools like KiCad, Ngspice, and GHDL, providing a comprehensive suite for electronic design automation. Being open-source, eSim is free to use, making advanced circuit design tools accessible without the need for expensive licenses.

Chapter 3

Problem Statement

To design and develop various Analog and Digital Integrated Circuit Models in the form of sub-circuits using device model files already present in the eSim library. These IC models should be useful in the future for circuit designing purposes by developers and users, once they get successfully integrated into the eSim subcircuit Library.

3.1 Approach

Our approach to implementing the problem statement began with examining datasheets from prominent Integrated Circuit (IC) manufacturers such as Texas Instruments, Analog Devices, and NXP Semiconductors. we selected ICs that offer a diverse range of functionalities, including precision amplifiers, comparators, encoders, and audio amplifiers. After building the subcircuits, we tested them to verify basic circuit configurations using NgSpice simulations. The step-by-step roadmap of this process is outlined below :

1. Analyzing Datasheets : The primary step is to browse through various analog and digital IC datasheets, and hence find suitable circuits to implement in eSim, that are not previously included into the eSim library. Check for the detailed schematic of the IC's and once the component values and the truth table is ascertained, then finalise the IC to be created.

2. Subcircuit Creation : After deciding the IC, we start modeling it as a sub-circuit in eSim, using the model files present in the eSim device model library only. The design is strictly according to the information given in the official data-sheets of the ICs.This step also includes building the Symbol/Pin diagram of the IC according to the packaging and pin description given in the data-sheets only.

3. Test Circuit Design : Once the component of the IC is ready, now we can build the test circuits, according to the data sheets. In this step we build the test cases and test circuits using the component IC.

4. Schematic Testing : Once the test circuits are ready, now it's time to simulate the test circuits so that the output can be obtained in the form of wave-forms and

plots. Here we take help of KiCad to NgSpice conversion and Simulation feature in eSim

If the output of the test circuit is not as per expectation, this implies that the test case has failed, and there is some error in the schematic. In such cases we go back to the design phase of the IC or the test circuits, to look for possible errors and then repeat the testing process again after making required changes.

Once the expected output of the test cases are correct and satisfy the expected results, then in such a case the IC is declared successfully working. The test case has been verified and the designing process is complete.

Chapter 4

Integrated Circuit Design

4.1 SN54H87- 4 bit True/Compliment, Zero/One Elements

Operation of these monolithic 4-bit true/complement elements is controlled by the B and C inputs. With the B input low, the 4-bit binary input (A) is transferred to the output (Y) in either complementary form (with C low) or true form (with C high). When the B input is high, the output will be at the complementary level of the C input regardless of the levels of the data inputs. These circuits are fully compatible for use with other TTL circuits. Input clamping diodes are provided to minimize transmission line effects and thereby simplify system design. Each input represents only one normalized series 54H/74H load, and full fan-out to 10 series 54H/74H loads is available from each of the outputs in the low-level condition. Power dissipation is 270 mW typically with an average propagation delay of 14 ns from data inputs to output.

Truth Table:

FUNCTION TABLE

CONTROL INPUTS		OUTPUTS			
B	C	Y1	Y2	Y3	Y4
L	L	$\overline{A1}$	$\overline{A2}$	$\overline{A3}$	$\overline{A4}$
L	H	A1	A2	A3	A4
H	L	H	H	H	H
H	H	L	L	L	L

H high level, L low level

A1, A2, A3, A4 the level of the respective A input.

Figure 4.1: Truth table of SN54H87 IC

4.1.1 Pin Diagram

The below figure shows the pin diagram of IC SN54H87. This IC is designed in J or W package with 14 pins. it comprises of 2 control pins A and B, 4 data input pins named A1, A2,A3,A4 , 4 output pins Y1,Y2,Y3,Y4 , and 2 pins which are named as NC meanis that they dont have any internal connection linked to them and 2 pins names VCC and GND.

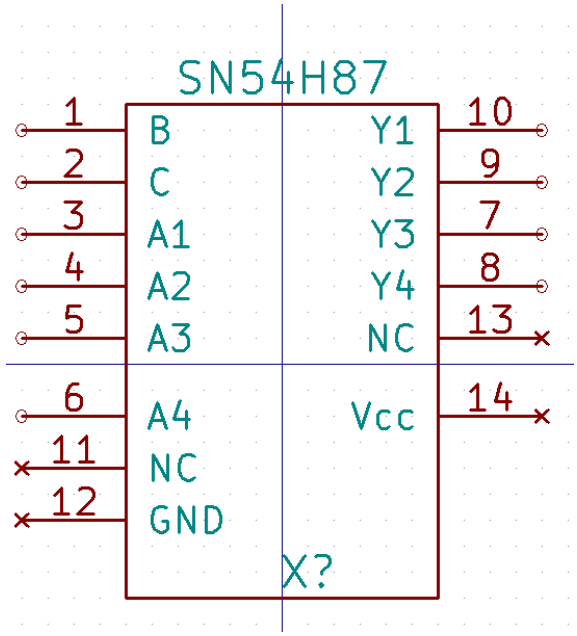


Figure 4.2: Pin Diagram of SN54H87 IC

4.1.2 Subcircuit Schematic Diagram

The figure below shows the schematic of the IC SN54H87.

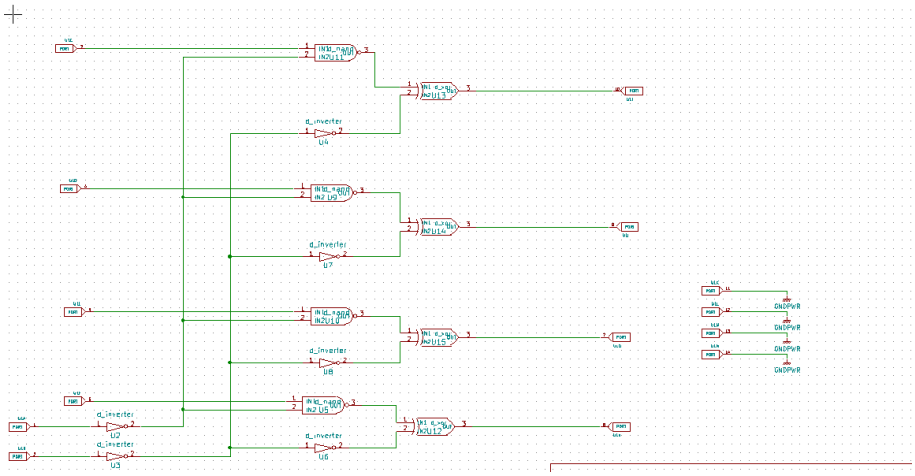
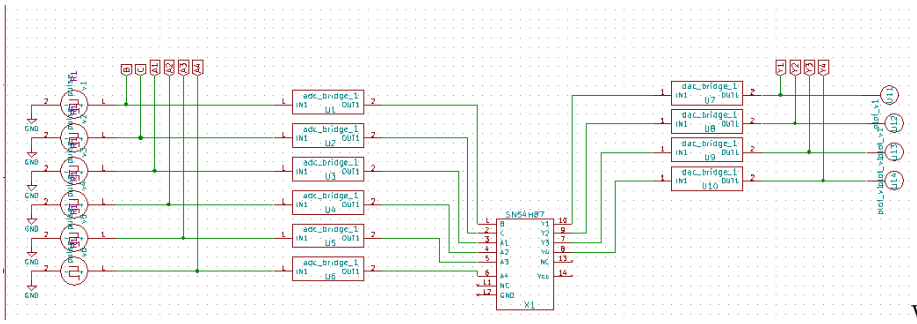


Figure 4.3: Subcircuit schematic of SN54H87 IC

4.1.3 Test Circuit

The figure below shows the test circuit of the IC SN54H87, to test the operation of the IC.



waveforms

Figure 4.4: Test circuit of SN54H87 IC

4.1.4 Input Waveforms

The figure below shows the input wavefoms which is given as per the truth table in the form of pulse waveforms.

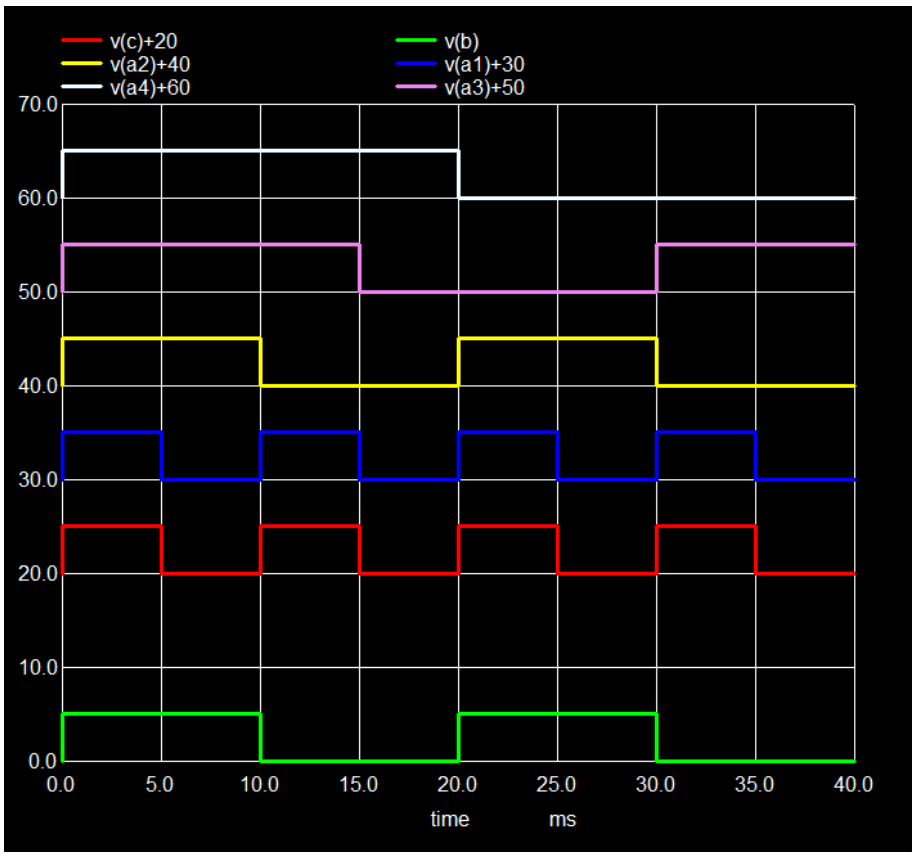


Figure 4.5: Input waveform of SN54H87 IC

4.1.5 Output Waveforms

The figure below shows the output signal received at the output pins of SN54H87 IC after processing the input signals.

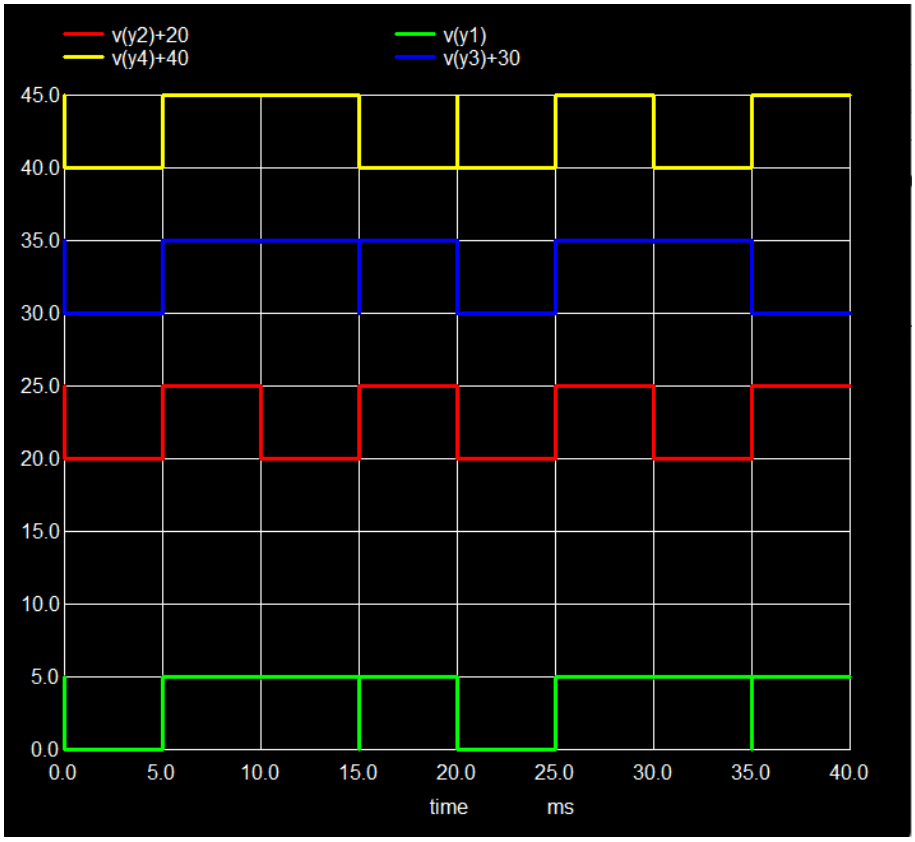


Figure 4.6: Output waveform of SN54H87 IC

4.2 MC1445- Gate Controlled Two Channel Input Wideband Amplifier

The MC1445/1545 was designed for use as a general purpose gated wideband amplifier, video switch, sense amplifier, multiplexer, modulator, FSK circuit, limiter, AGC circuit, or pulse amplifier.

- Large Bandwidth: 50 MHz Typical
- Channel Select Time: 20 ns Typical
- Differential Inputs and Differential Output

4.2.1 Pin Diagram

The IC MC1445 comprises of 9 pins. It include 2 pairs of pins , with each pair allocated to A and B respectively , depictinf inverting and non-inverting inputs. It

also includes a GATE pin, 1 pin for VCC and 1 pin for VEE. It includes 2 output pins : one is for invertinf and other is for non-inverting outputs.

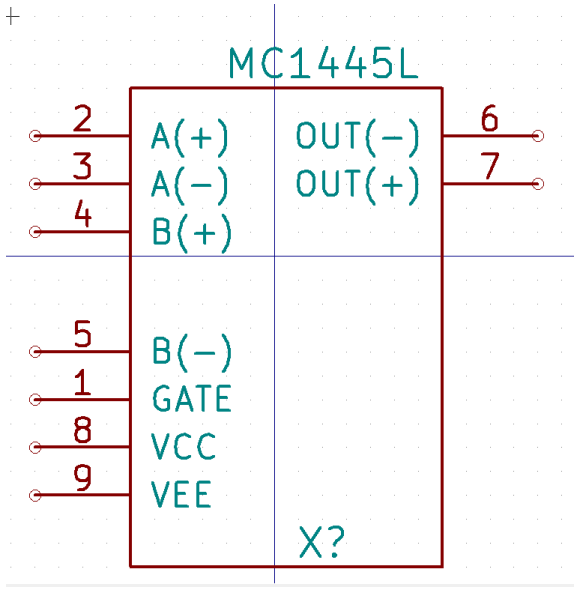


Figure 4.7: Pin Diagram of MC1445 IC

4.2.2 Subcircuit Schematic Diagram

The figure below shows the schematic of the IC MC1445.

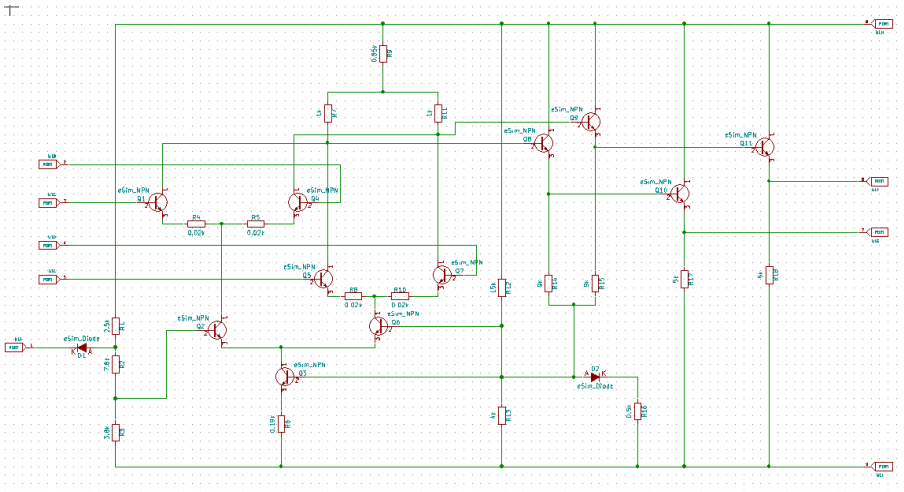


Figure 4.8: Subcircuit Schematic of MC1445 IC

4.2.3 Test Circuit

The figure below shows the test circuit of the IC MC1445 to test the operation of the IC.

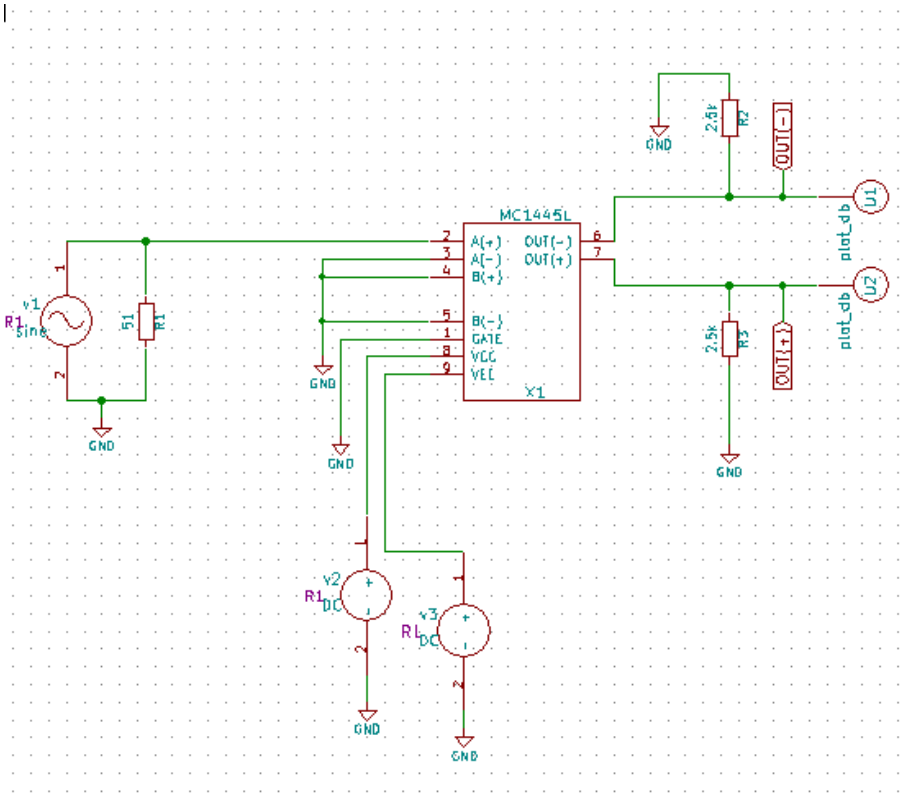


Figure 4.9: Test circuit of MC1445 IC

4.2.4 Input Values

The figure below represents the input values that we have inserted as per the datasheet of MC1445 IC

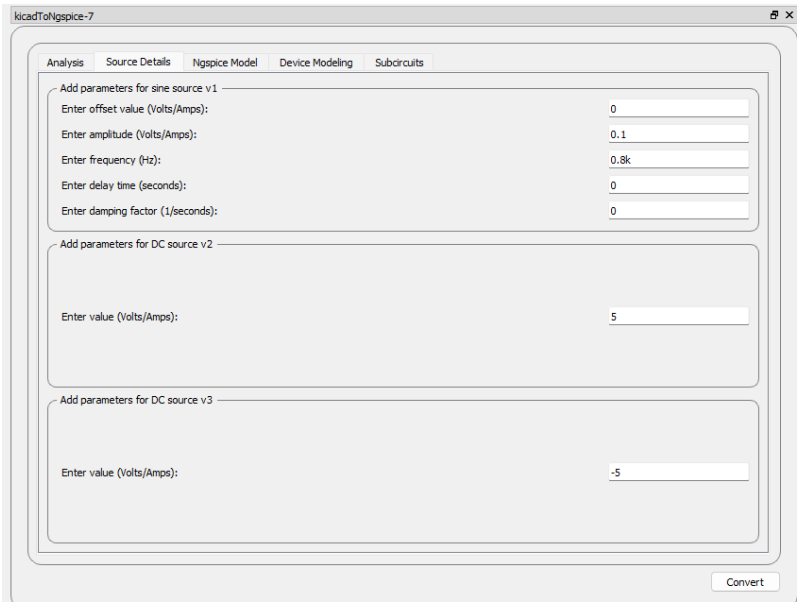


Figure 4.10: Input Values of MC1445 IC

4.2.5 Output Waveforms

The figure below shows the output signal received at the output pins of SN54H87 IC after processing the input signals.

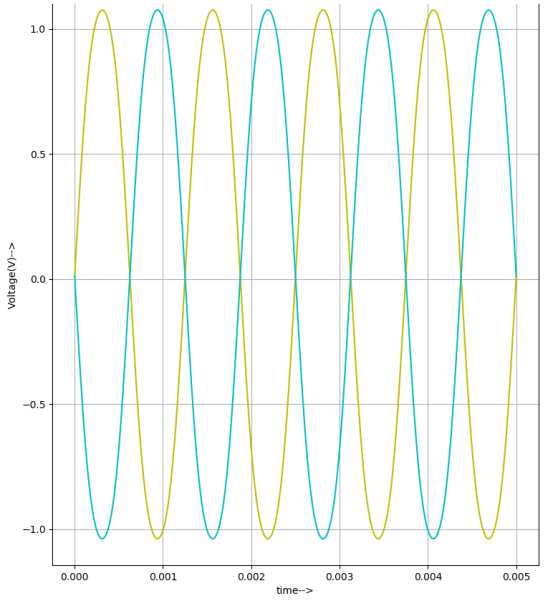


Figure 4.11: Output Waveform of MC1445 IC

4.3 CD4019- CMOS Quad AND/OR Select Gate

CD4019 types consist of four AND/OR select gate configurations, each consisting of two 2-input AND gates driving a single 2-input OR gate. Selection is accomplished by control bits Ka and Kb. In addition to selection of either channel A or channel B information,the contol bits can be applied simultaneously to accomplish the logical A+B function. **Truth Table:**

TRUTH TABLE

Ka	Kb	An	Bn	Dn
1	0	1	X	1
1	0	0	X	0
0	1	X	1	1
0	1	X	0	0
0	0	X	X	0
1	1	0	0	0
1	1	0	1	1
1	1	1	0	1
1	1	1	1	1

X = Don't Care

Figure 4.12: Truth table of CD4019 IC

4.3.1 Pin Diagram

The below figure shows the pin diagram of IC CD4019. This IC is designed in hermetic dual-in-line ceramic packages (F3A suffix) with 14 pins. It comprises of 2 control pins Ka and Kb, 4 pairs data input pins named A1 B!, A2 B2,A3 B3,A4 B4 , and 4 output pins D1 , D2, D3, D4.

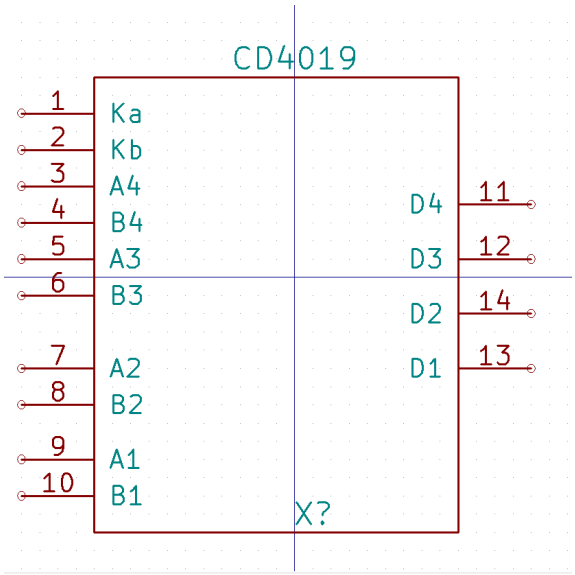


Figure 4.13: Pin Diagram of IC CD4019 IC

4.3.2 Subcircuit Schematic Diagram

The figure below shows the schematic of the IC CD4019.

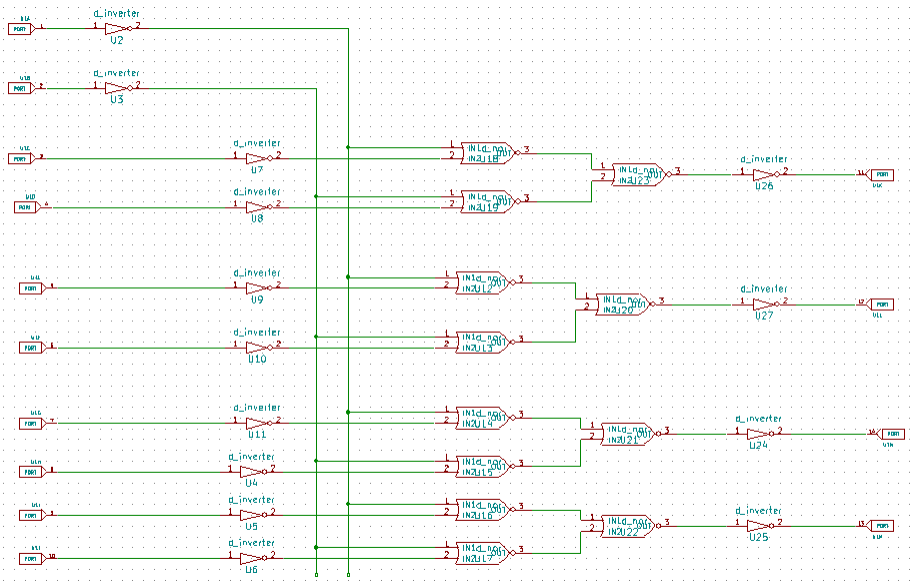


Figure 4.14: Subcircuit of IC CD4019

4.3.3 Test Circuit

The figure below shows the test circuit of the IC CD4019 to test the operation of the IC.

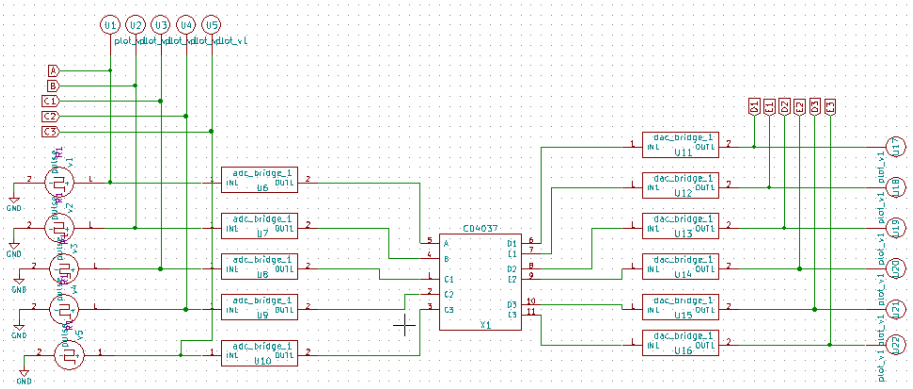


Figure 4.15: Test Circuit of IC CD4019

4.3.4 Input Waveforms

The figure below shows the input wavefoms which is given as per the truth table in the form of pulse waveforms,

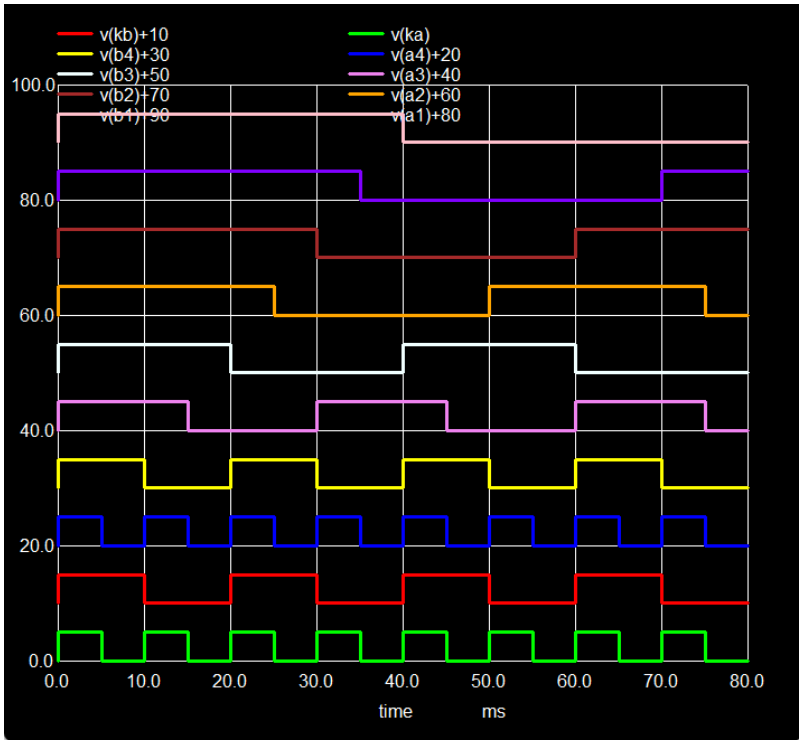


Figure 4.16: Input Waveform of CD4019 IC

4.3.5 Output Waveforms

The figure below shows the output signal received at the output pins of CD4019 IC after processing the input signals.

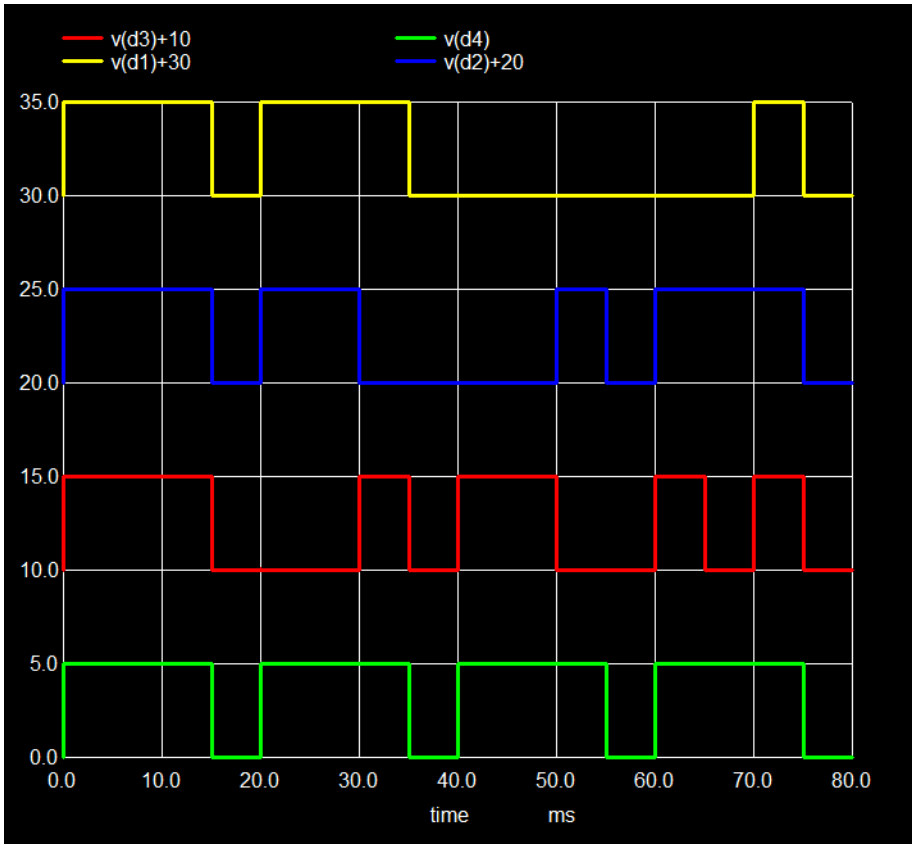


Figure 4.17: Output Wavefom of CD4019 IC

4.4 TL811M- Dual Channel Differential Comparators with strobes

The TL811 is an improved version of the TL711 high speed dual-channel voltage comparator. Voltage amplification is higher due to an extra stage, increasing the tempearture accuracy . The output pulse width may be "stretched" by varying the capacitive loading.
Each channel has different inputs, a strobe input, and an output in common with the other channel. When either strobe is taken low , it inhibits the associated channel. If both strobes are simulatneously low , the output will be low regardless of the conditions applied to the differential inputs.
These dual-channel voltage comparators are particularly attractive for applications requiring an amplitude-descriminating sense amplifier with an adjustbale threshold voltage.

4.4.1 Pin Diagram

The below figure shows the pin diagram of IC TL811M. This IC is designed in J Dual in-Line Package with 10 pins. It comprises of 2 pairs of inverting and non-inverting inputs, 1 GND (ground) pin, 2 pins for strobes , 1 output pin, and 2 pins named as VCC+ and VCC-.

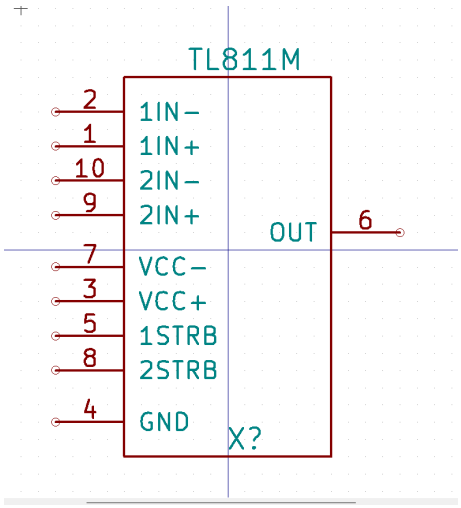


Figure 4.18: Pin Diagram of TL811M IC

4.4.2 Subcircuit Schematic Diagram

The figure below shows the schematic of the IC TL811M.

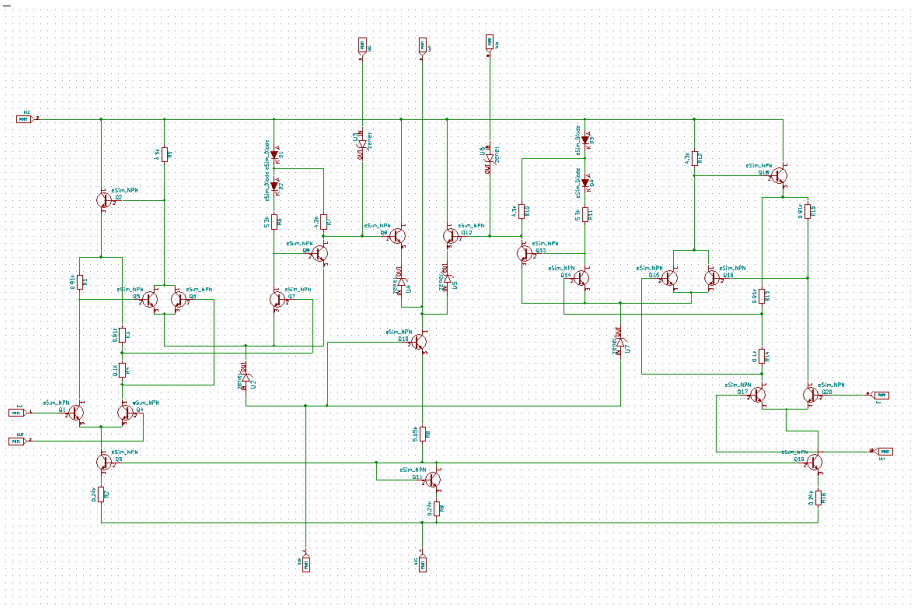


Figure 4.19: Subcircuit of TL811M IC

4.4.3 Test Circuit

The figure below shows the test circuit of the IC TL811M to test the operation of the IC.

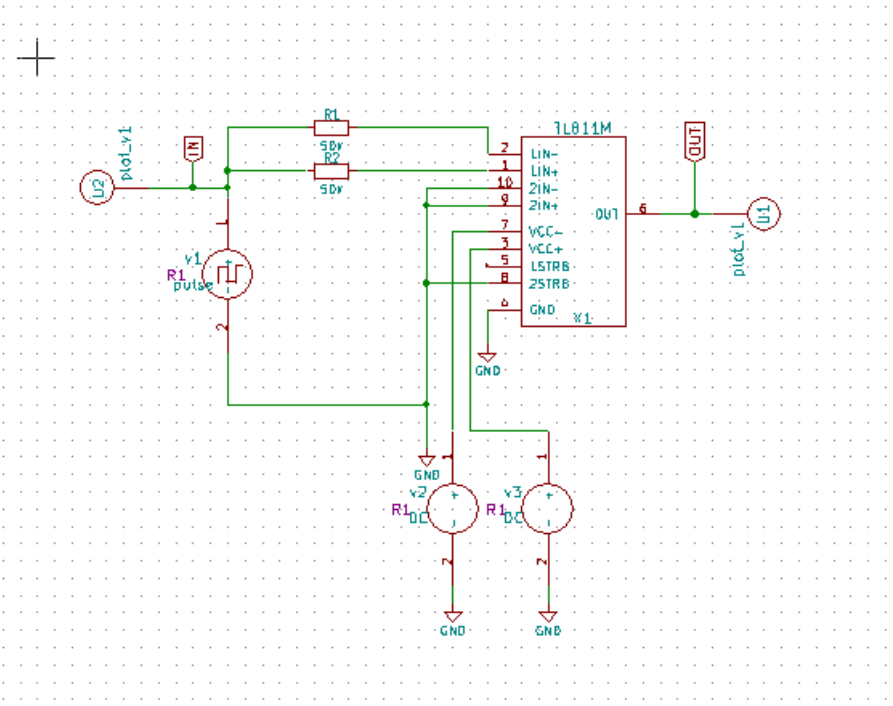


Figure 4.20: Test circuit of IC TL811M

4.4.4 Input Waveforms

The figure below shows the input wavefoms which is in the form of pulse waveforms,

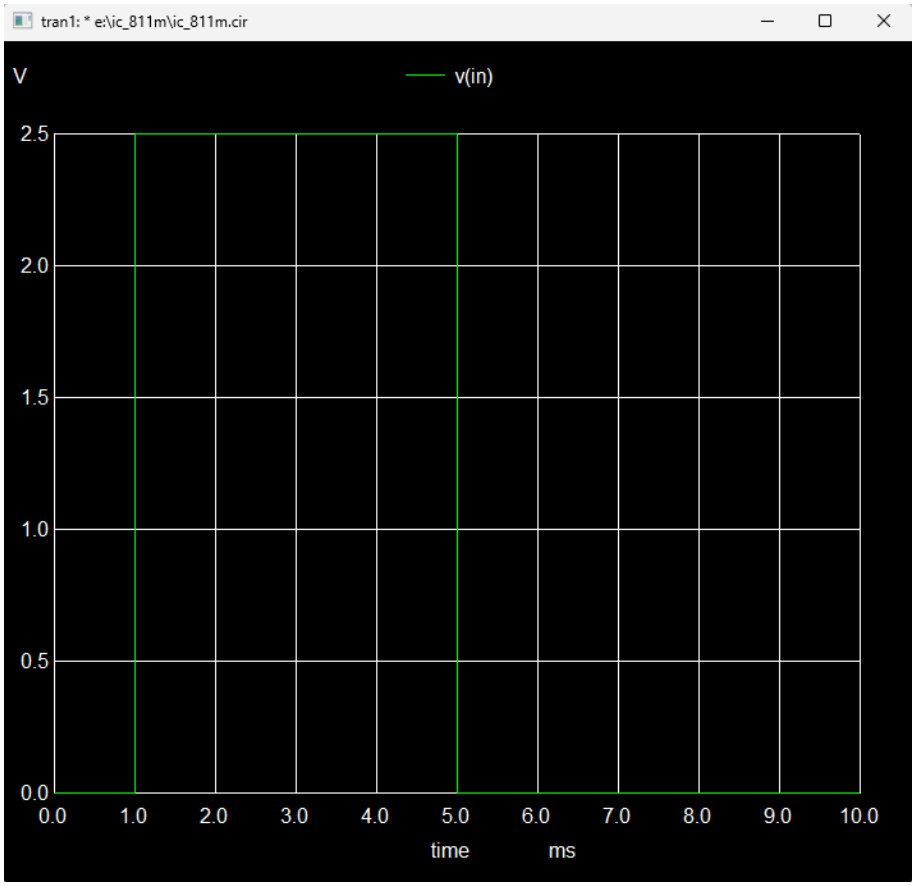


Figure 4.21: Input Waveform of TL811M IC

4.4.5 Output Waveforms

The figure below shows the output signal received at the output pin of TL811M IC after processing the input signals.

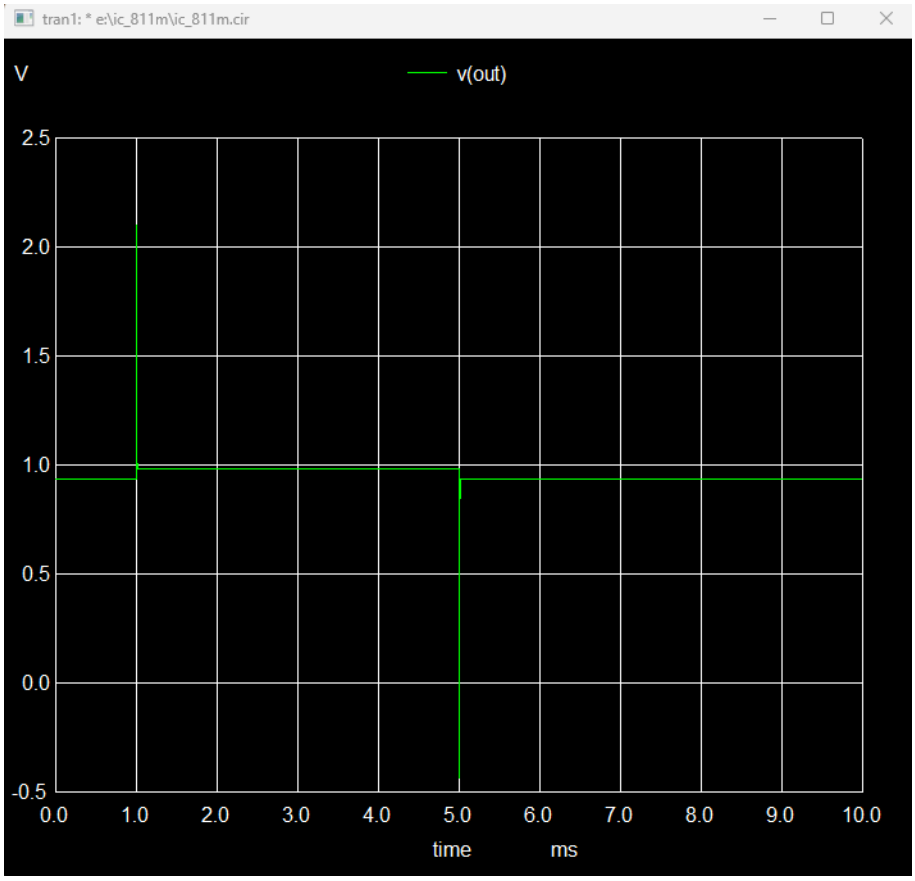


Figure 4.22: Output Waveform of TL811M IC

4.5 IC TL560C- Precision Level Detector

The TL560C is precision level Detector intended for applications that require a Schmitt Trigger function. The detector has excellent voltage and temperature stability and an internal voltage reference for the input threshold level. The reference-voltage pin is available for external adjustment of the positive-going threshold voltage level.The TL560C is characterized for operation from 0 °C to 70 °C.

4.5.1 Pin Diagram

The below figure shows the pin diagram of IC TL560C. This IC is designed in JG or P Dual in-Line Package with 5 pins. It comprises of 1 input and 1 output pins, 1 pin for VCC, 1 pin for GND(Ground) and 1 pin named as REF(Reference).

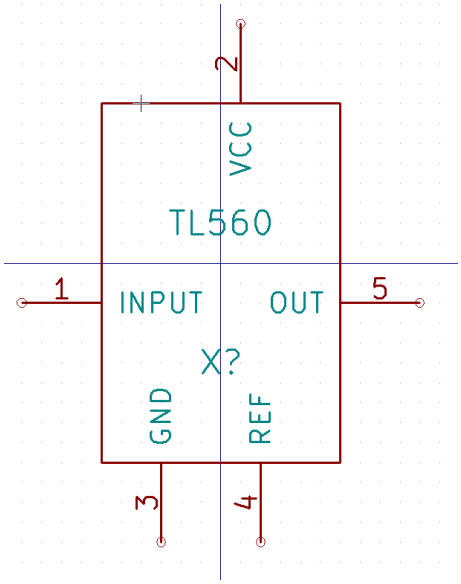


Figure 4.23: Pin Diagram of TL560C IC

4.5.2 Subcircuit Schematic Diagram

The figure below shows the schematic of the IC TL560C.

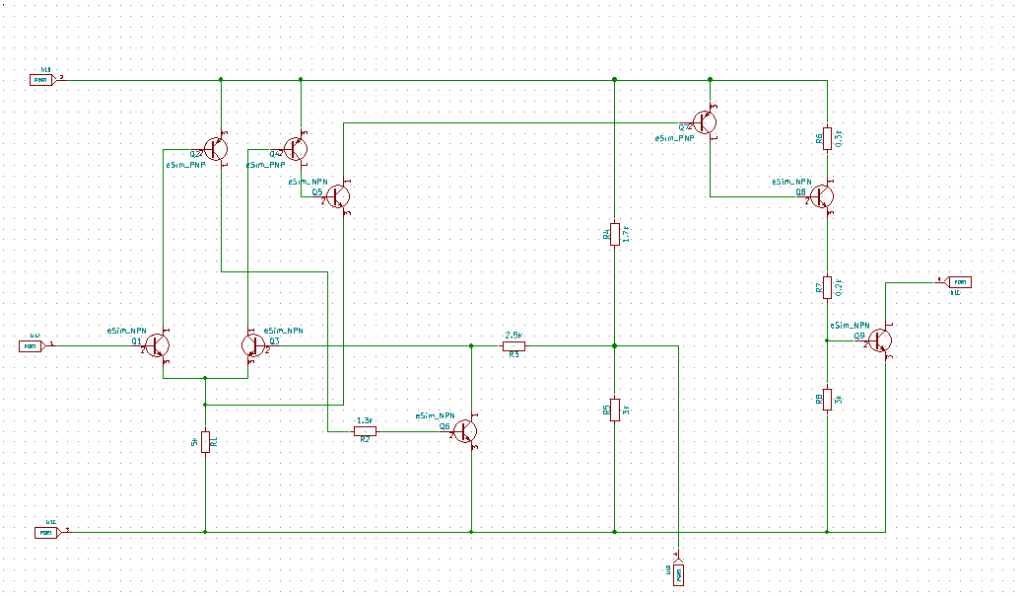


Figure 4.24: Subcircuit of TL560C IC

4.5.3 Test Circuit

The figure below shows the test circuit of the IC TL560C to test the operation of the IC.

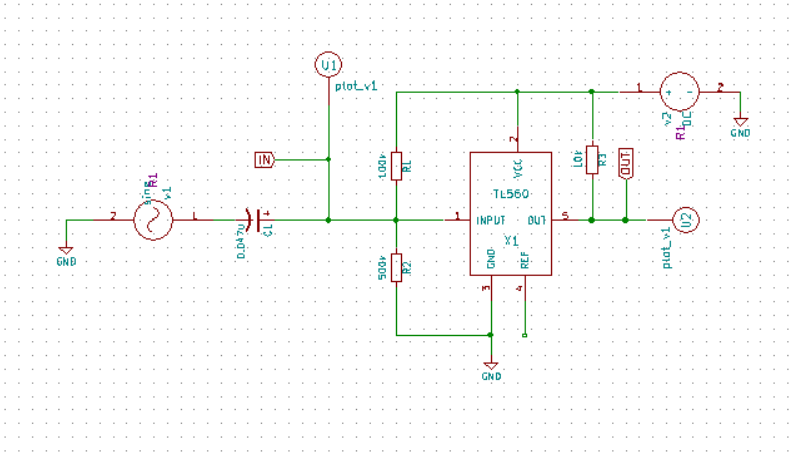


Figure 4.25: Test circuit of TL560C IC

4.5.4 Input Waveforms

The figure below shows the input waveform, which is in the form of a sinusodial wave.

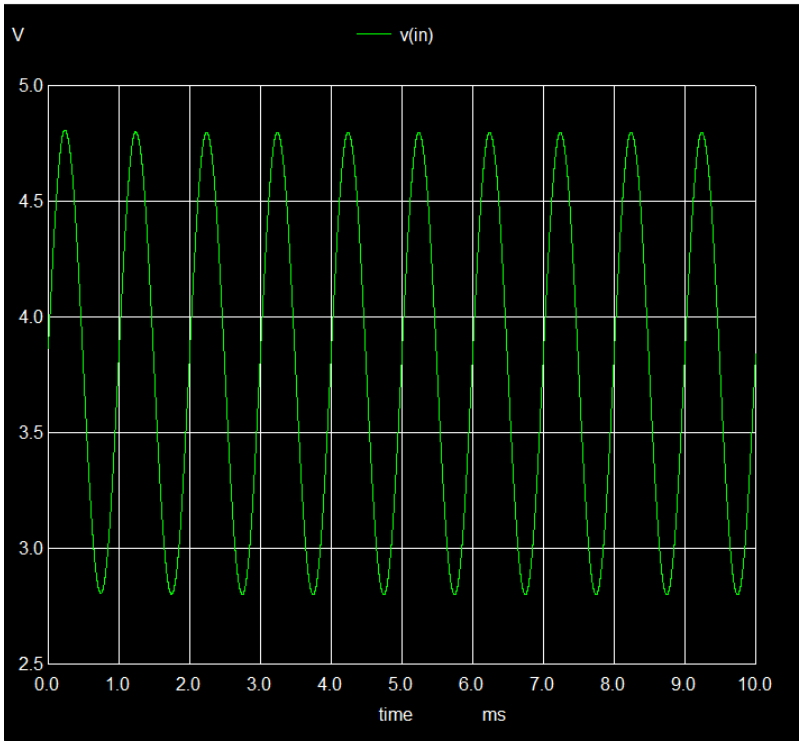


Figure 4.26: Input Waveform of TL560C IC

4.5.5 Output Waveforms

The figure below shows the output signal received at the output pin of TL560C IC after processing the input signals.

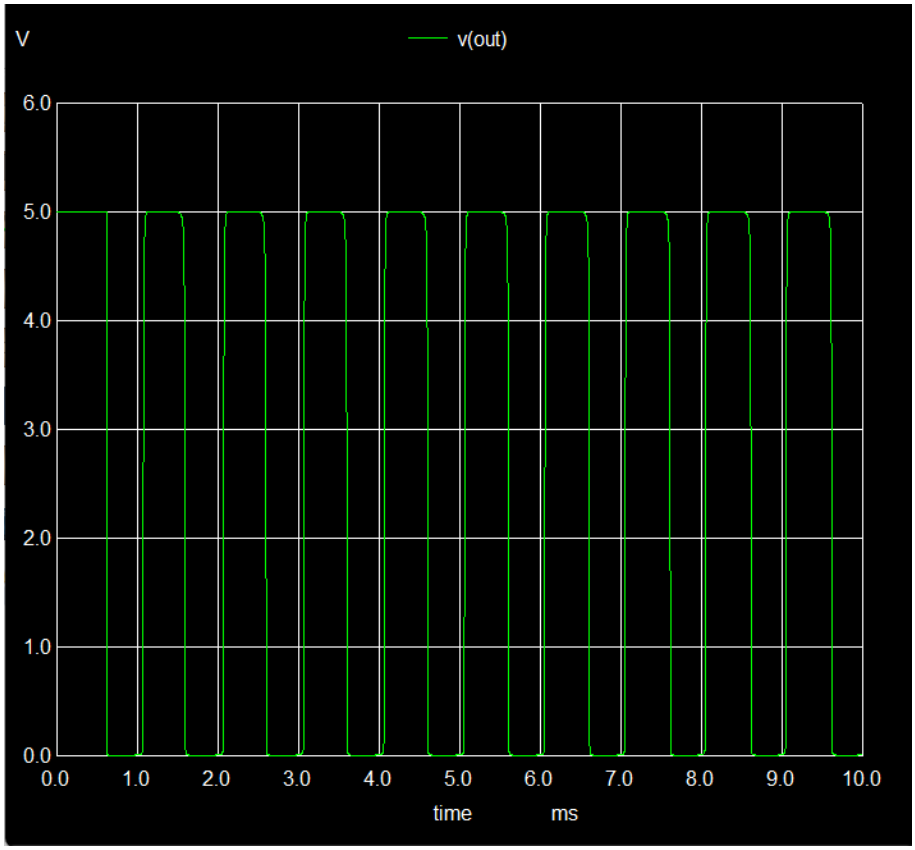


Figure 4.27: Ouput Waveform of TL560C IC

4.6 CD4037A-CMOS Triple AND/OR Bi-Phase Pairs

The CD4037A consists of three AND/OR pairs Driven by common control signals A and B. Each circuit has a data input(C) , and two output terminals D and E that provide output in accordance with the truth table shown below. The circuit is useful for coding and decoding of signals and split-phase(Bi-phase) communicatons systems, magnetic recording , and plated wire and core memory systems. A separate VCC terminal is provided to allow level conversion to any voltage from 3 volts to VDD. These types are supplied in 14-lead hermetic Dual-in-line ceramic packages(D and F suffixes) , 14-lead dual-in-line plastic package(E suffix), 14-lead ceramic flat package (K suffix), and in chip form(H suffix).
Truth Table:

TRUTH TABLE

INPUT		OUTPUT	
A	B	D	E
0	0	1	1
1	0	C	$\overline{C}$
0	1	$\overline{C}$	C
1	1	0	0

Figure 4.28: Truth Table of CD4037 IC

4.6.1 Pin Diagram

The below figure shows the pin diagram of IC CD4037. It comprises of 2 control pins A and B , 3 set of input pins named as C1, C2, C3 and 3 pairs of output pins which is D1 E1, D2 E2 and D3 E3.

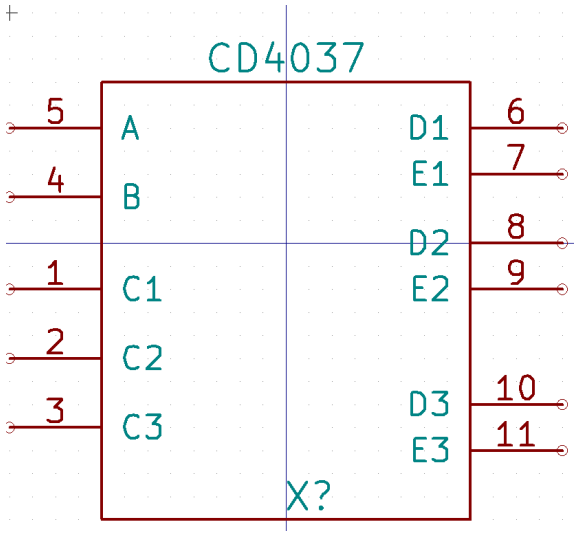


Figure 4.29: Pin Diagram of CD4037 IC

4.6.2 Subcircuit Schematic Diagram

The figure below shows the schematic of the IC CD4037.

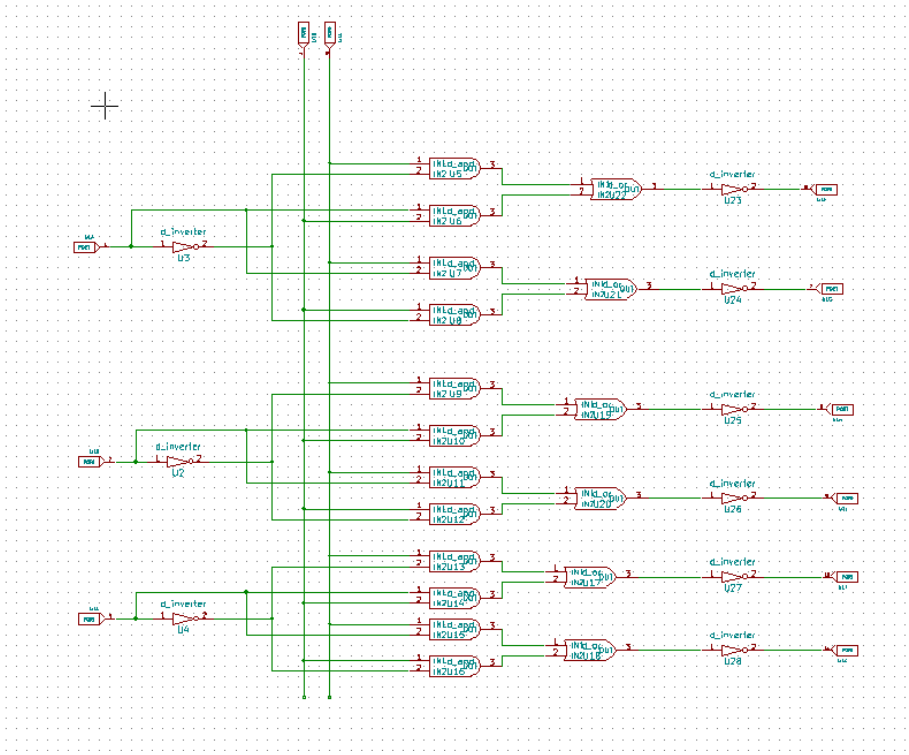


Figure 4.30: Subcircuit of CD4037 IC

4.6.3 Test Circuit

The figure below shows the test circuit of the IC CD4037 to test the operation of the IC.

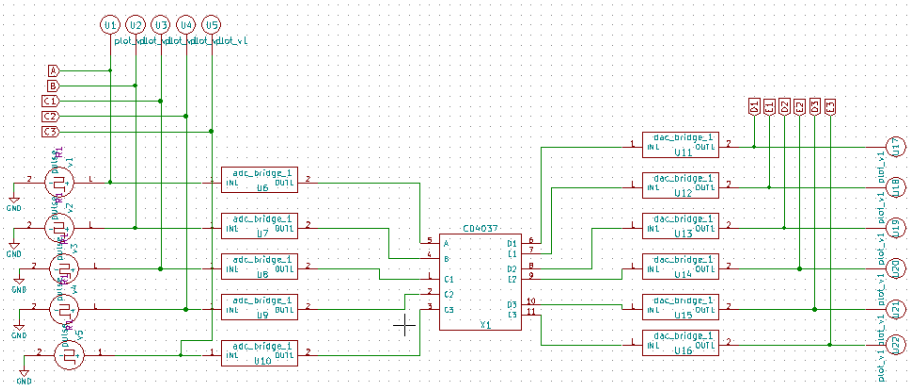


Figure 4.31: Test Circuit of CD4037 IC

4.6.4 Input Waveforms

The figure below shows the input waveform, which is in the form of a pulse wave.

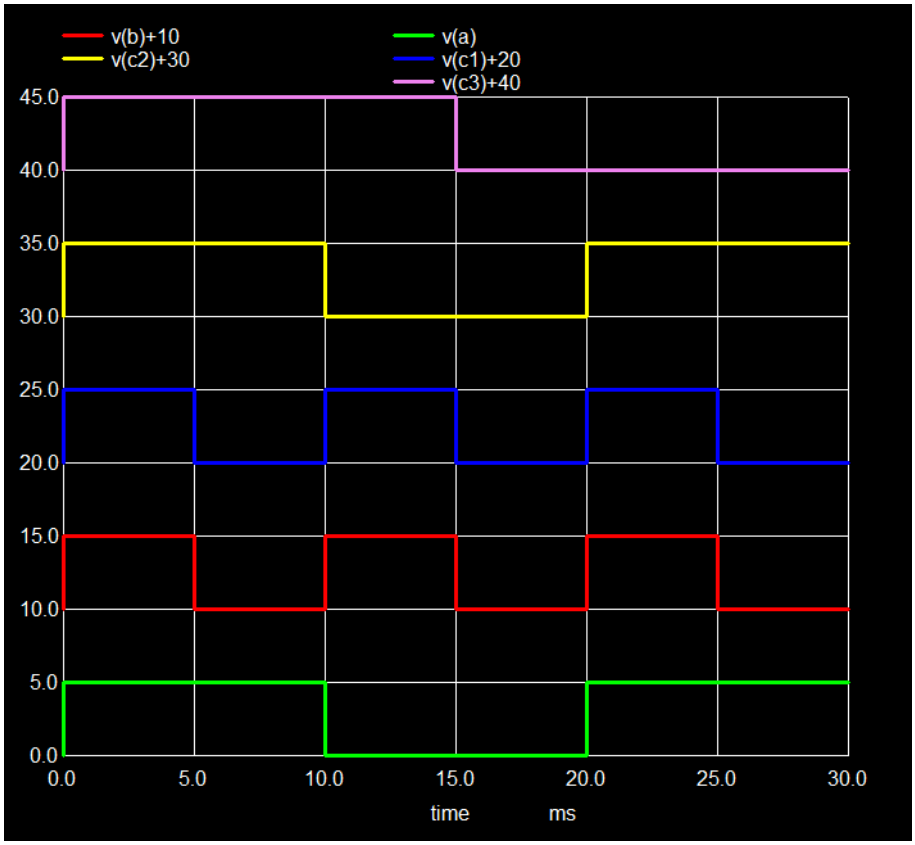


Figure 4.32: Input Waveform of CD4037 IC

4.6.5 Output Waveforms

The figure below shows the output signal received at the output pin of IC after processing the input signals.

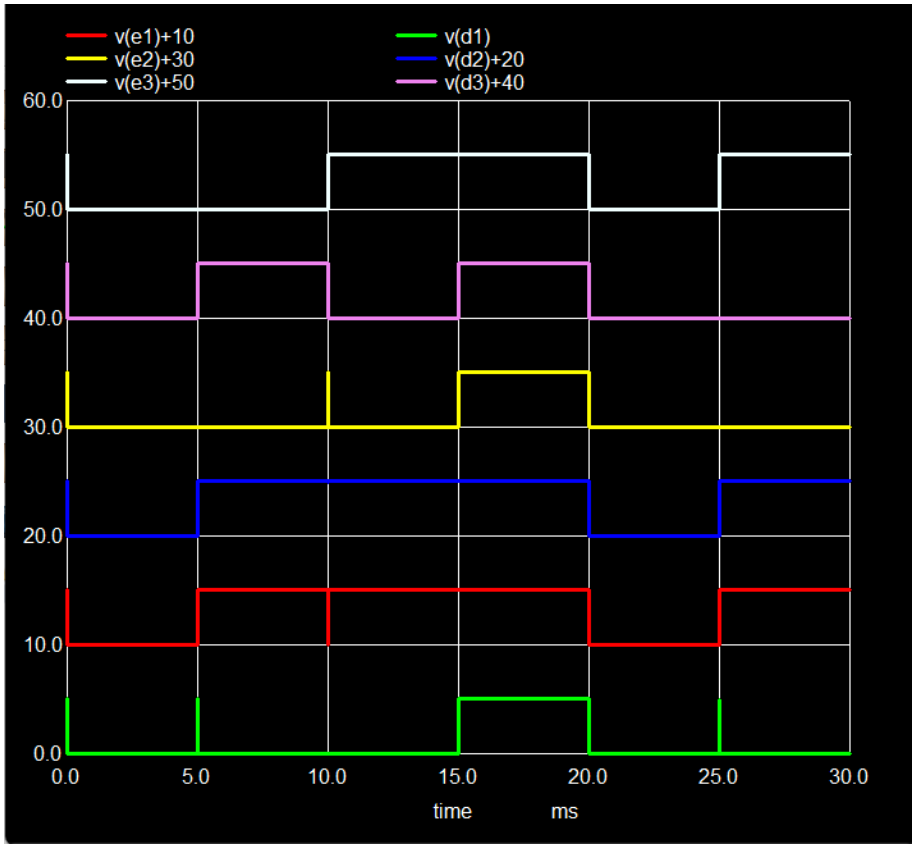


Figure 4.33: Output Waveform of CD4037 IC

4.7 SN74128-Line Drivers

These devices contain four independent 2-input NOR line drivers. They perform the boolean function Y = A+B or Y = A.B. The SN54128 is designed to drive 75 ohms lines. The SN74128 is designed to drive 50 ohms lines. The SN54128 is characterized for operation over the full military range −55 °C to 125 °C. The SN74128 is characterized for operation from 0 °C to 70 °C.

4.7.1 Pin Diagram

The below figure shows the pin diagram of IC CD4037. It comprises of 2 control pins A and B , 3 set of input pins named as C1, C2, C3 and 3 pairs of output pins which is D1 E1, D2 E2 and D3 E3.

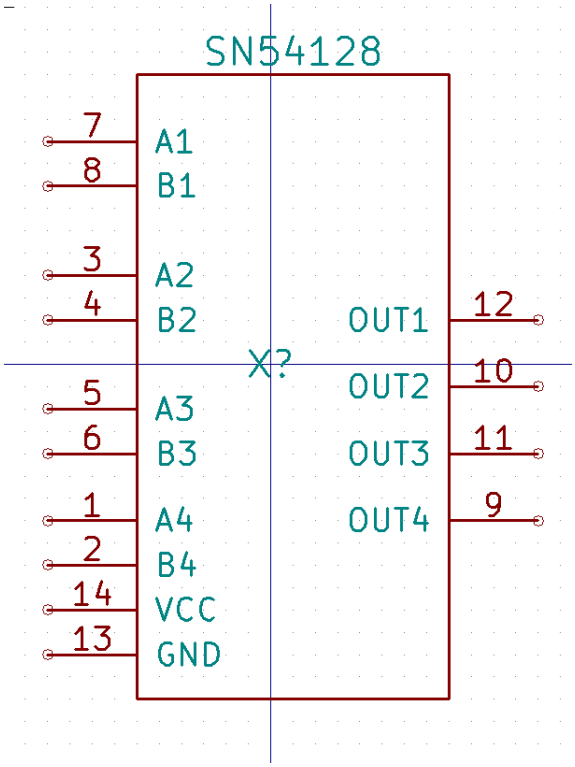


Figure 4.34: Pin Diagram of SN74128

4.7.2 Subcircuit Schematic Diagram

The figure below shows the schematic of the IC SN74128.

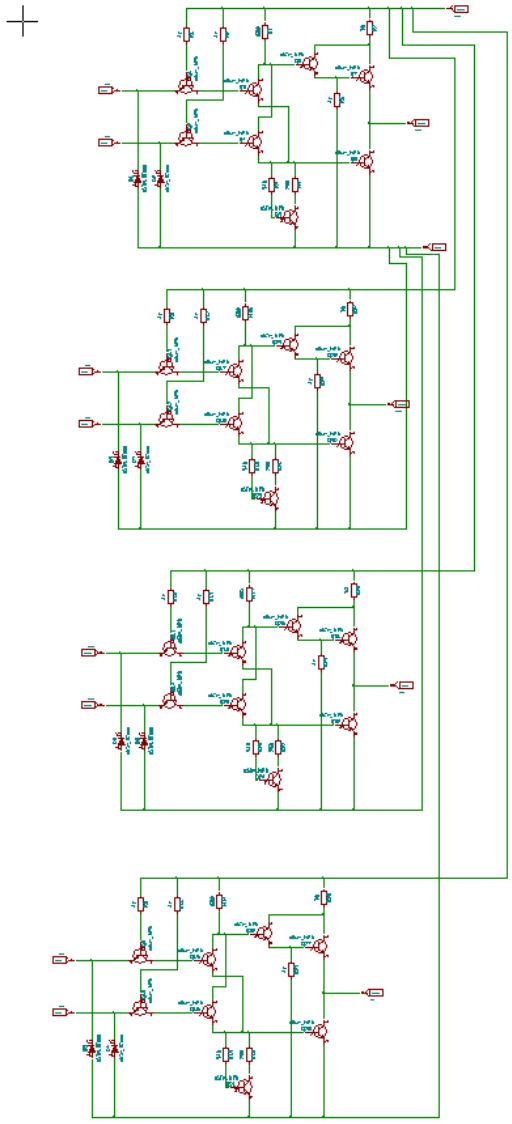


Figure 4.35: Subcircuitof SN74128 IC

4.7.3 Test Circuit

The figure below shows the test circuit of the IC SN74128 to test the operation of the IC.

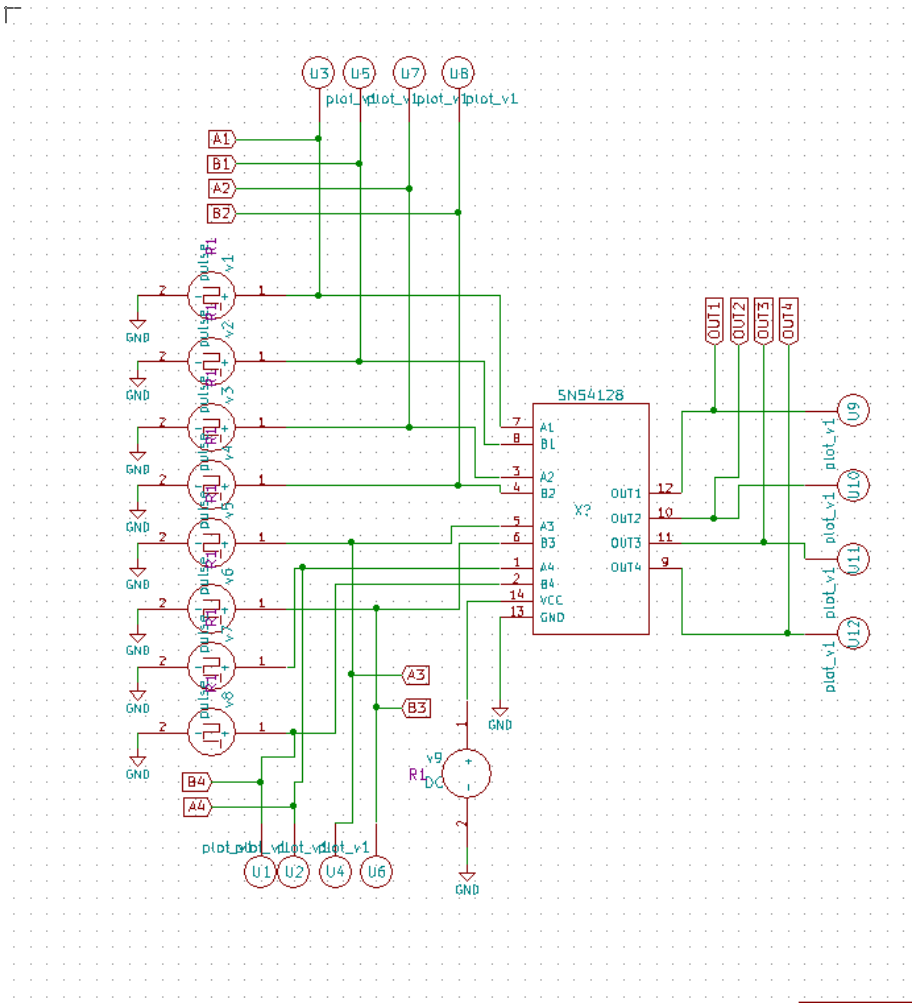


Figure 4.36: Test Circuit of SN74128 IC

4.7.4 Input Waveforms

The figure below shows the input waveform, which is in the form of a pulse wave.

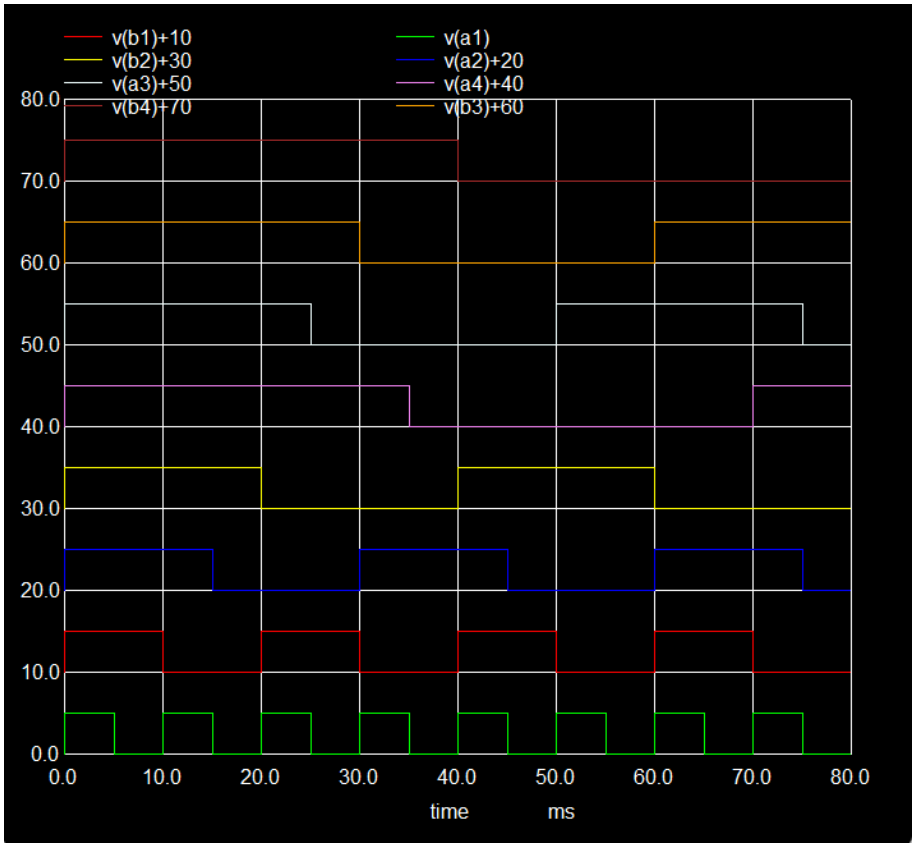


Figure 4.37: Input Waveform of SN74128 IC

4.7.5 Output Waveforms

The figure below shows the output signal received at the output pin of SN74128 IC after processing the input signals.

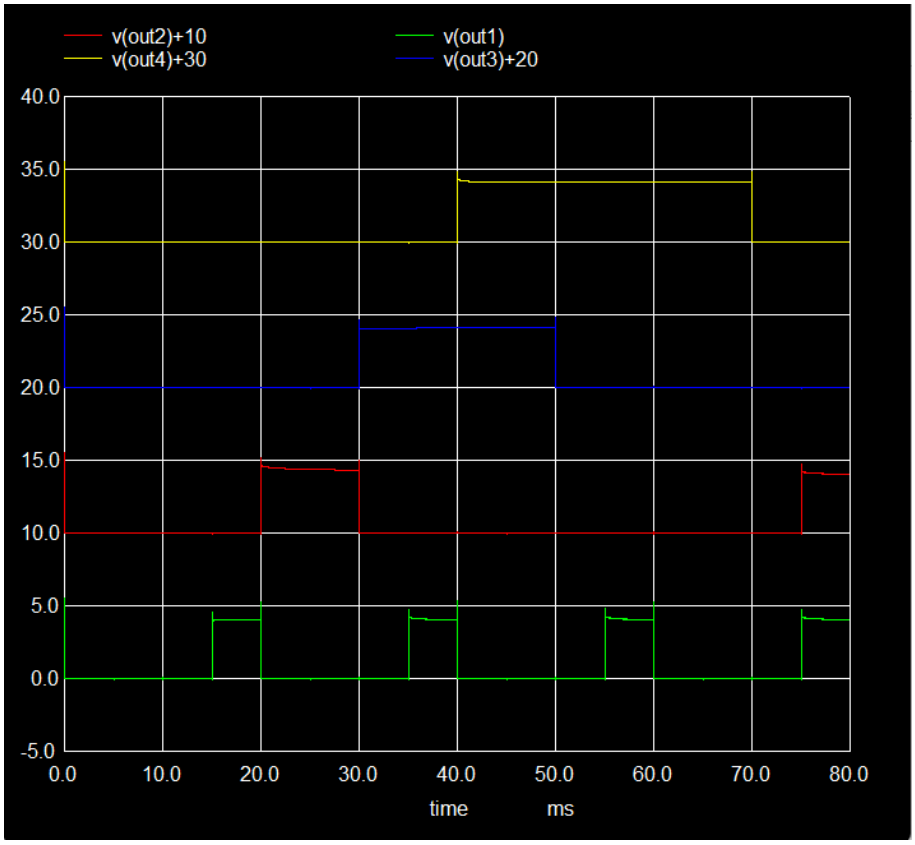


Figure 4.38: Output Waveform of SN74128 IC

4.8 HEF4531B-13 input Parity Checker/Generator

The HEF4531B is a parity checker/generator with 13 inputs (I0 to I12) and a parity output (O). When the number of parity inputs that are HIGH is even, the output is LOW. When the number of parity inputs that are HIGH is odd, the output is HIGH. For words of 12 bits of less, the output can be used to generate either odd or even parity by appropriate termination of the unused parity input(s). For words of 14 or more bits, the devices can be cascaded by connecting the output of one device to any parity input of another device. When cascading devices, it is recommended that the output of one device be connected to the I12 input of the other device since there is less delay to the output from the I12 input from any other input(I0 to I11).

Truth Table:

INPUTS													OUTPUT
I_0	I_1	I_2	I_3	I_4	I_5	I_6	I_7	I_8	I_9	I_{10}	I_{11}	I_{12}	O
L	L	L	L	L	L	L	L	L	L	L	L	L	L
any odd number of inputs HIGH													H
any even number of inputs HIGH													L
H	H	H	H	H	H	H	H	H	H	H	H	H	H

Figure 4.39: Truth table of HEF4531B IC

4.8.1 Pin Diagram

The below figure shows the pin diagram of IC HEF4531B. It comprises of 13 input pins labelled from I0 to I12, 2 pins representing VDD and VSS and 1 output pin.

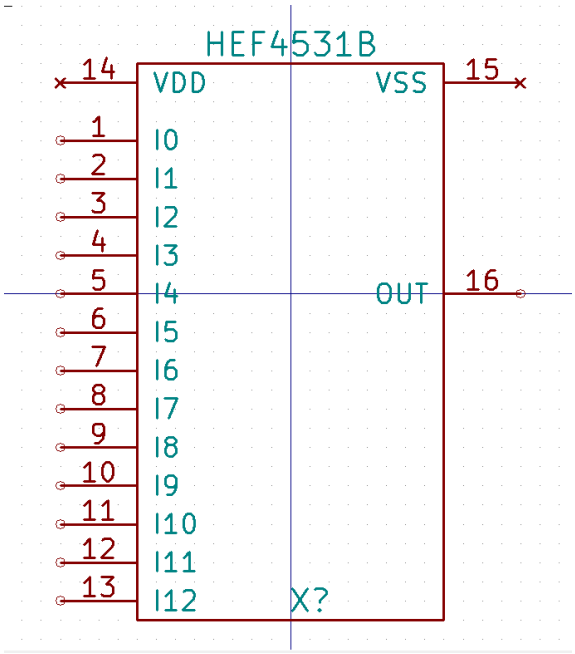


Figure 4.40: Pin Diagram of HEF4531B IC

4.8.2 Subcircuit Schematic Diagram

The figure below shows the schematic of the IC HEF4531B.

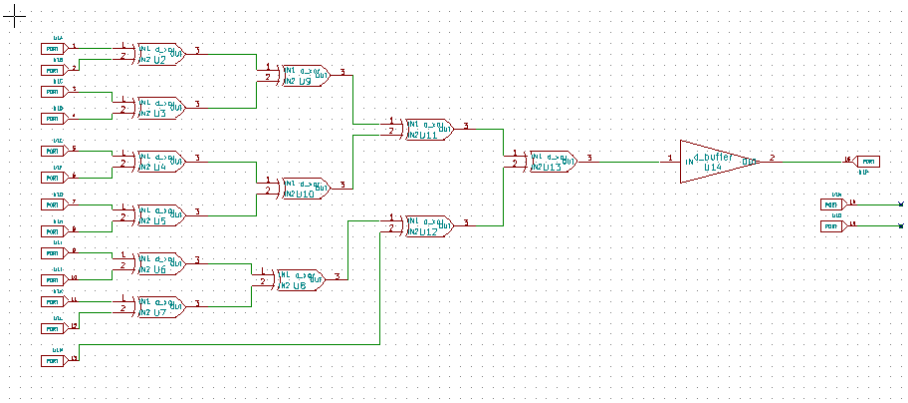


Figure 4.41: Subcircuit of HEF4531B IC

4.8.3 Test Circuit

The figure below shows the test circuit of the IC HEF4531B to test the operation of the IC.

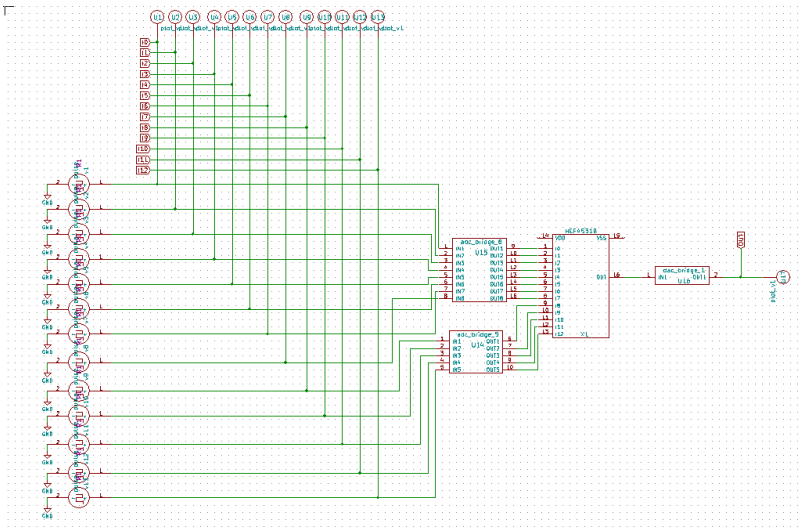


Figure 4.42: Test Circuit of HEF4531B IC

4.8.4 Input Waveforms

The figure below shows the input waveform, which is in the form of a pulse wave.

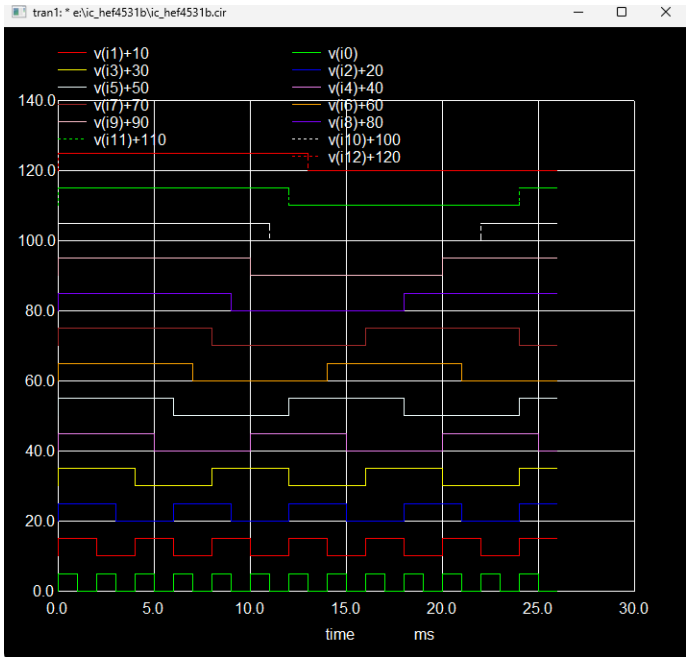


Figure 4.43: Input Waveforms of HEF4531B IC

4.8.5 Output Waveforms

The figure below shows the output signal received at the output pin of HEF4531B IC after processing the input signals.

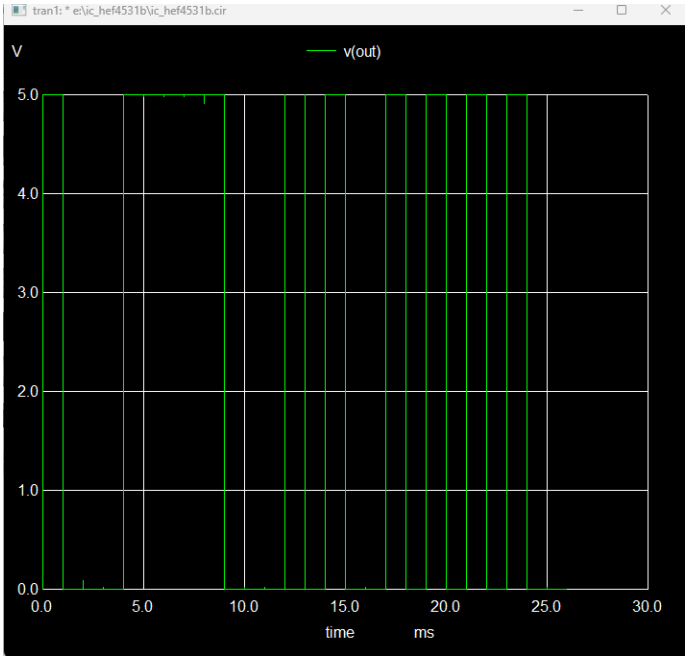


Figure 4.44: Output Waveforms of HEF4531B IC

4.9 74HC58- Dual AND/OR

The 74HC58 is a high-speed Si-gate CMOS device and is pin compatible with low power Schottky TTL (LSTTL). It is specified in compliance with JEDEC standard no. 7A. The "58" provides two sections of AND-OR gates. One section contains a 2-wide, 3-input (1A to 1F) AND-OR gate and the second section contains a 2-wide, 2-input (2A to 2D) AND-OR gate.

Truth Table:

INPUTS						OUTPUT
1A	1B	1C	1D	1E	1F	1Y
L	X	X	L	X	X	L
L	X	X	X	L	X	L
L	X	X	X	X	L	L
X	L	X	L	X	X	L
X	L	X	X	L	X	L
X	L	X	X	X	L	L
X	X	L	L	X	X	L
X	X	L	X	L	X	L
X	X	L	X	X	L	L
X	X	X	H	H	H	H
H	H	H	X	X	X	H

Figure 4.45: Truth Table of 74HC58 IC

INPUTS				OUTPUT
2A	2B	2C	2D	2Y
L	X	L	X	L
L	X	X	L	L
X	L	L	X	L
X	L	X	L	L
X	X	H	H	H
H	H	X	X	H

Figure 4.46: Truth Table of 74HC58 IC

4.9.1 Pin Diagram

The below figure shows the pin diagram of IC 74HC58. It comprises of 10 input pins among which 6 input pins represents the AND gate operation labelled from (1A to 1F) and 4 input pins represents the OR gate operation labelled from (2A to 2D) and there is 2 output pins.

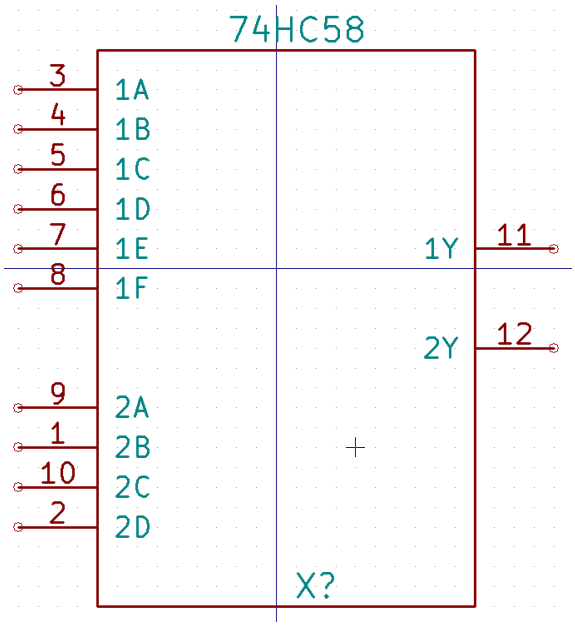


Figure 4.47: Pin Diagram of 74HC58 IC

4.9.2 Subcircuit Schematic Diagram

The figure below shows the schematic of the IC 74HC58.

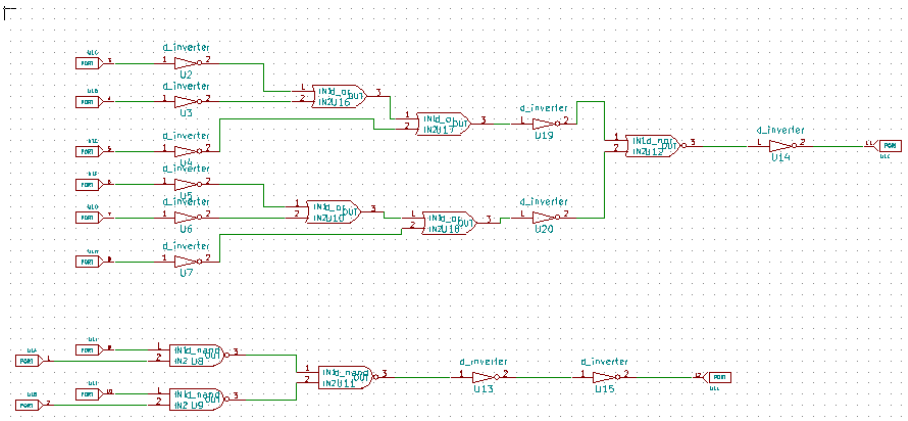


Figure 4.48: Subcircuit Schematic of 74HC58 IC

4.9.3 Test Circuit

The figure below shows the test circuit of the IC 74HC58 to test the operation of the IC.

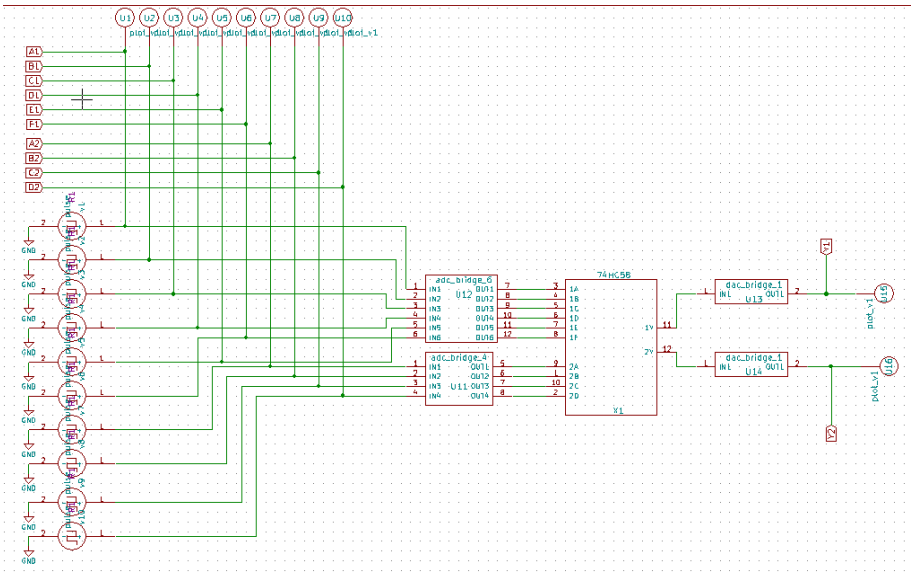


Figure 4.49: Test Circuit of 74HC58 IC

4.9.4 Input Waveforms

The figure below shows the input waveform, which is in the form of a pulse wave.

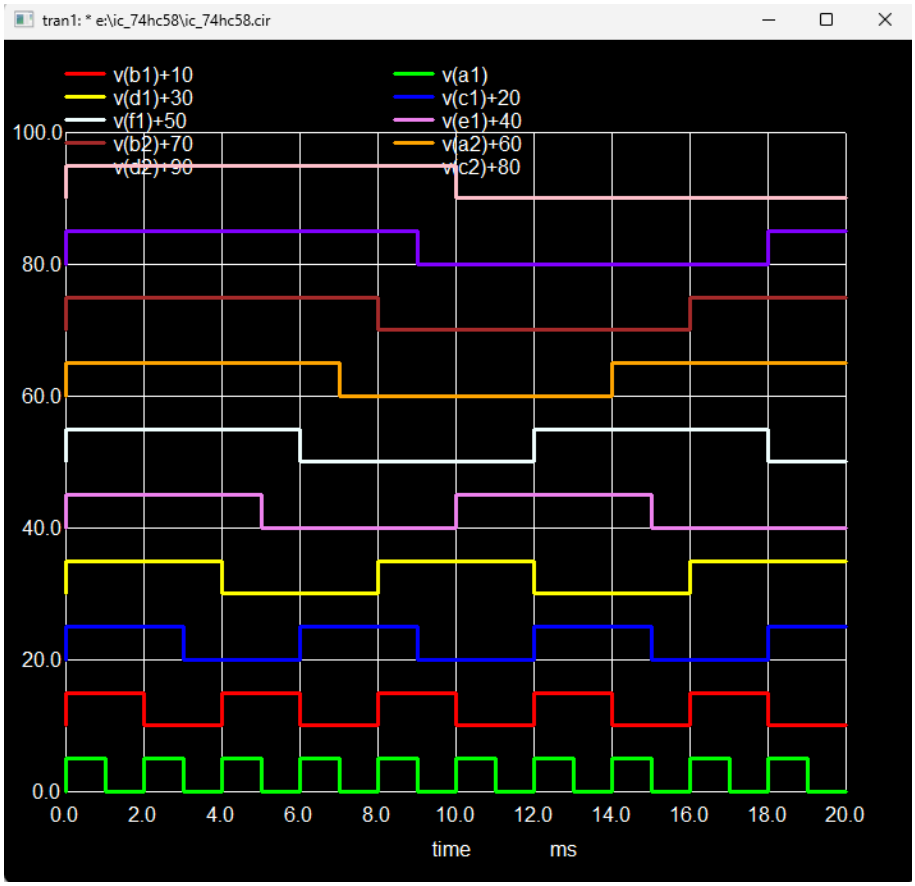


Figure 4.50: Input Waveform of 74HC58 IC

4.9.5 Output Waveforms

The figure below shows the output signal received at the output pin of 74HC58 IC after processing the input signals.

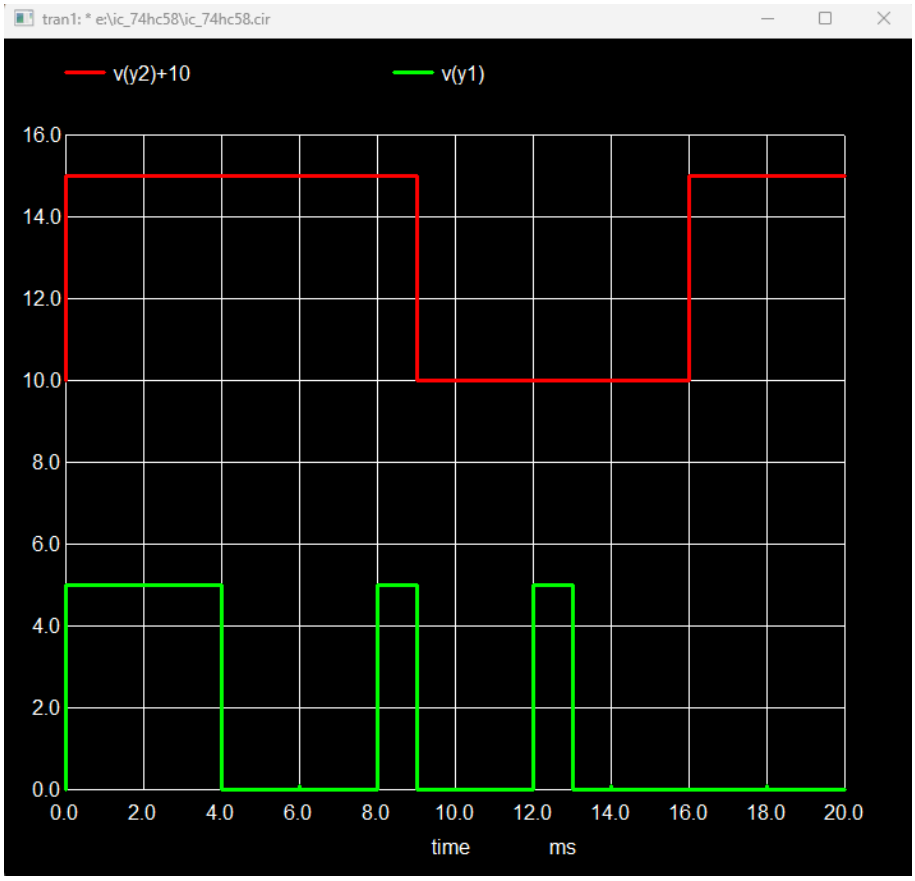


Figure 4.51: Output Waveform of 74HC58 IC

4.10 SN74ALS679- 12 Bit Address Comparator

This 12-bit address comparator simplifies addressing of memory boards and/or other peripheral devices. The four P inputs are normally hardwired with a preprogrammed address. An internal decoder determines what input information applied to the A inputs must be low or high to cause a low state at the Y output. For example, a positive-logic bit combination of 0111 (decimal 7) at the P input determines that inputs A1 through A7 must be low and that inputs A8 through A12 must be high to cause the output to go low. Equality of the address applied at the A inputs to the preprogrammed address is indicated by the output being low. This device features an enable (G) input. When G is low, the device is enabled. When G is high, the device is disabled and the output is high, regardless of the A and P inputs.
Truth Table:

FUNCTION TABLE

INPUTS																OUTPUT
$\overline{G}$	P3	P2	P1	P0	A1	A2	A3	A4	A5	A6	A7	A8	A9	A10	A11	A12	Y
L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	L
L	L	L	L	H	L	H	H	H	H	H	H	H	H	H	H	H	L
L	L	L	H	L	L	L	H	H	H	H	H	H	H	H	H	H	L
L	L	L	H	H	L	L	L	H	H	H	H	H	H	H	H	H	L
L	L	H	L	L	L	L	L	L	H	H	H	H	H	H	H	H	L
L	L	H	L	H	L	L	L	L	L	H	H	H	H	H	H	H	L
L	L	H	H	L	L	L	L	L	L	L	H	H	H	H	H	H	L
L	L	H	H	H	L	L	L	L	L	L	L	H	H	H	H	H	L
L	H	L	L	L	L	L	L	L	L	L	L	L	H	H	H	H	L
L	H	L	L	H	L	L	L	L	L	L	L	L	L	H	H	H	L
L	H	L	H	L	L	L	L	L	L	L	L	L	L	L	H	H	L
L	H	L	H	H	L	L	L	L	L	L	L	L	L	L	L	H	L
L	H	H	L	L	L	L	L	L	L	L	L	L	H	H	H	L	L†
L	H	H	L	H	L	L	L	L	L	L	L	L	L	H	H	L	L†
L	H	H	H	L	L	L	L	L	L	L	L	L	L	L	H	L	L†
L	H	H	H	H	L	L	L	L	L	L	L	L	L	L	L	L	L
L	All other combinations																H
H	Any combination																H

Figure 4.52: Truth Table of SN74ALS679 IC

4.10.1 Pin Diagram

The below figure shows the pin diagram of IC SN74ALS679. It comprises of a total of 17 input pins which are labelled as A1-A12, P0-P3 and G. 2 pins represent VCC and GND ad it has 1 output pin.

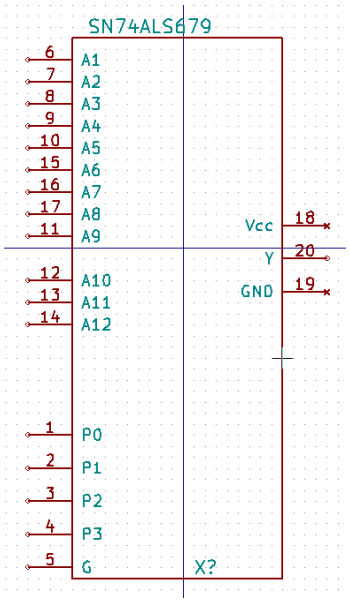


Figure 4.53: Pin Diagram of SN74ALS679 IC

4.10.2 Subcircuit Schematic Diagram

The figure below shows the schematic of the IC SN74ALS679.

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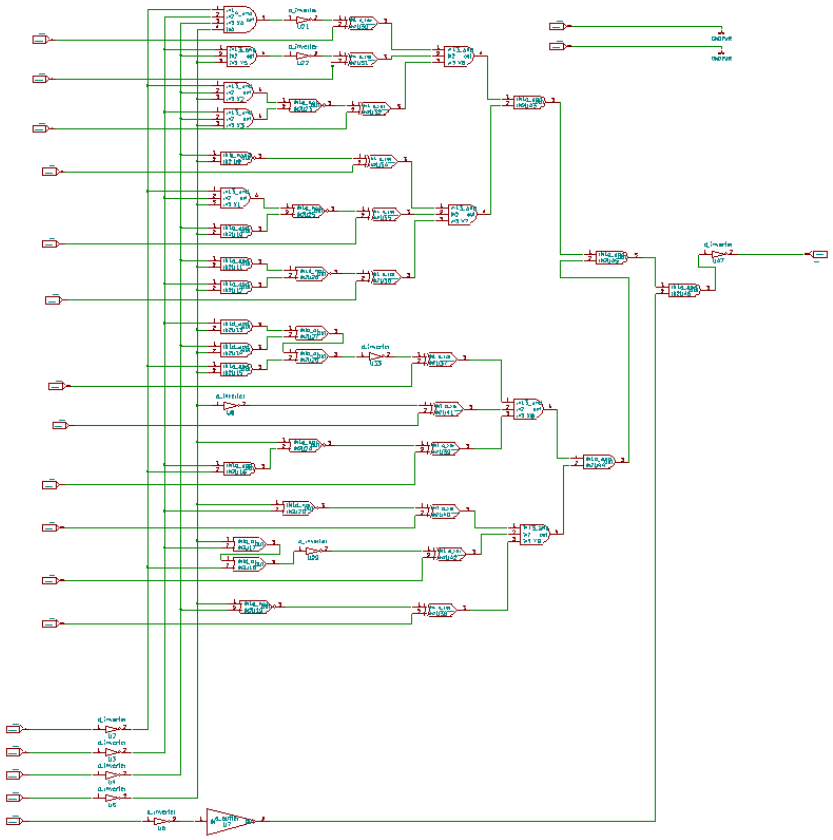

Figure 4.54: Subcircuit of SN74ALS679 IC

4.10.3 Test Circuit

The figure below shows the test circuit of the IC SN74ALS679 to test the operation of the IC.

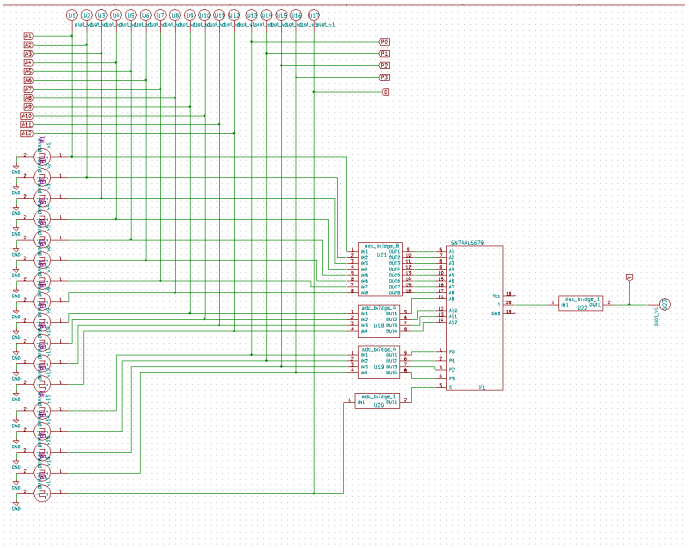

Figure 4.55: Test Circuit of SN74ALS679 IC

4.10.4 Input Waveforms

The figure below shows the input waveform, which is in the form of a pulse wave.

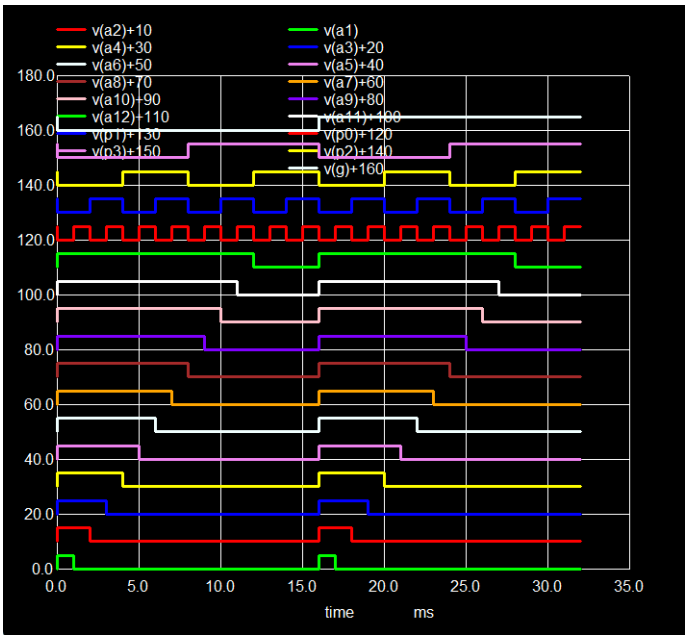

Figure 4.56: Input Waveform of SN74ALS679 IC

4.10.5 Output Waveforms

The figure below shows the output signal received at the output pin of SN74ALS679 IC after processing the input signals.

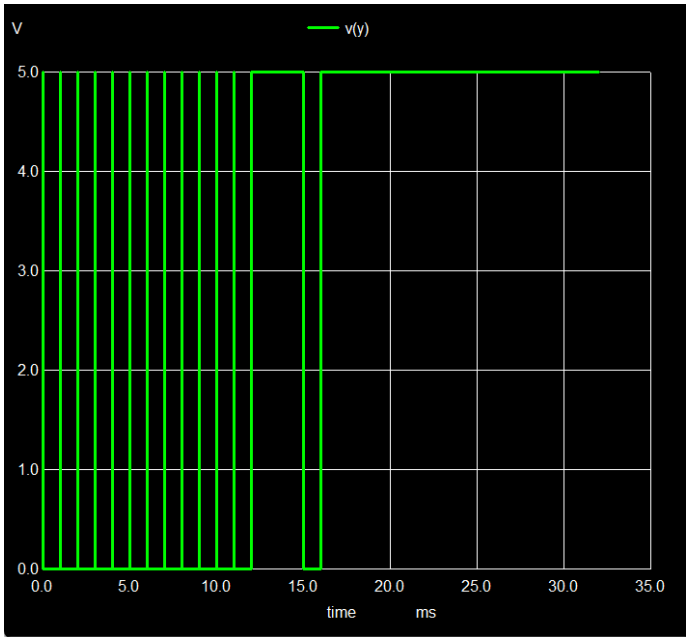

Figure 4.57: Output Waveform of SN74ALS679 IC

Chapter 5

Conclusion and Future Scope

We successfully met our goal of developing various subcircuits for both Analog and Digital Integrated Circuits. Each IC model was meticulously created based on the specifications provided in their official datasheets. The output of each IC was thoroughly verified and tested using their respective test circuits. The IC models developed during this fellowship include fundamental circuit components such as Precision level Detector, Comparators, Wideband Amplifier, Line Drivers, and various Logic Gate ICs. These models are now ready to be incorporated into the subcircuit library of eSim, allowing developers and students to utilize them as building blocks in their projects and circuit designs. As the device model library in eSim continues to grow, we anticipate the development of more such ready-to-use IC models for use in eSim.

Chapter 6

Reference

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