Summer Fellowship Report

On

Integrated Circuit Design using Subcircuit Feature of eSim

Submitted by

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I would like to give my heartfelt appreciation to FOSSEE, IIT Bombay for giving me the amazing chance to work on the design and integration of various sub-circuits in eSim. This internship has been an enriching experience, providing in-depth exposure to open-source EDA tools and their importance in circuit simulation and design, thus enriching my knowledge in circuit modeling, simulation, and verification and so allowing me to acquire the expertise to handle subsequent challenges in electronics and semiconductor design.

I am particularly grateful to Prof. Kannan M. Moudgalya for his visionary guidance and support. His commitment to fostering open-source innovation has been incredibly inspiring, and I am privileged to have been a part of a mission that so mirrors the future of collaborative technology.

A word of thanks to my mentor, Mr. Sumanto Kar, and his team whose technical expertise, perceptive comments, and constant motivation played a pivotal role in this internship experience.

As I continue on my learning journey in the vast field of Electronics, the skills, understanding, and experience obtained within this time frame will most surely be a foundation upon which to build my professional career.

I am deeply grateful for this experience and will work to implement what I have learned in useful and positive ways in the future.

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Chapter 1

Introduction

1.1 FOSSEE

The FOSSEE (Free/Libre and Open Source Software for Education) initiative is a part of the National Mission on Education through Information and Communication Technology (ICT), Ministry of Human Resource Deveopment (MHRD), Government of India. It advocates for adopting open-source solutions to enhance learning standards across India. By shifting away from paid proprietary software, the project supports educational institutions in transitioning to free and open-source alternatives with comparable tools. Additionally, the project focuses on creating new open-source applications and improving existing ones to better serve academic and research needs.

1.2 eSim

eSim, formerly known as OSCAD/FreeEDA, is a free/libre and open-source Electronic Design Automation (EDA) tool that supports circuit design, simulation, analysis, and PCB layout development. Built on open-source technologies such as KiCad, Ngspice, GHDL, OpenModelica, Verilator, Makerchip, and the SkyWater SKY130 PDK, eSim provides a powerful, integrated platform for engineers and educators. Released under the GNU General Public License, it ensures accessibility and freedom for users.

One of the key feature is its Subcircuit functionality, which allows users to build complex circuits by combining reusable modular blocks.

With capabilities comparable to proprietary tools like OrCAD, PSpice, LTspice, Xpedition, and HSPICE, eSim eliminates the need for expensive licenses, making it a cost-effective alternative for educational institutions, researchers, and small-to-medium enterprises (SMEs).

As part of the FOSSEE initiative, eSim promotes open-source adoption in engineering education and industry, fostering innovation, collaboration, and accessibility in electronics design.

1.3 Ngspice

NgSpice is a free and open-source circuit simulation tool based on the SPICE (Simulation Program with Integrated Circuit Emphasis) framework. It supports the analysis of analog, digital, and mixed-signal circuits, making it a versatile solution for electronics design and education. A comprehensive component support exist which provides a wide ranges of cirucit elements along with in-built models, the circuits are defined using Netlists and results are visualised as waveforms (voltage, current, etc.) THus providing a high-performance simulation capabilities without licensing costs.

1.4 KiCad

KiCad is an open-source, free Electronic Design Automation (EDA) solution for printed circuit board (PCB) and schematic design. It offers professional-level tools for designing circuit schematics, PCB layout, generating manufacturing files (Gerber), and library management. It serves as the foundation for schematic capture and PCB design, offering a professional-grade environment with features such as hierarchical schematics, custum symbol creation, and design rule checking. Combined with eSim, it extends the capabilities of KiCad by providing advanced simulation tools for analog, digital, and mixed-signal circuits. Enabling users to conduct transient, AC, DC analysis with real time waveform visualization.

Chapter 2

Features of eSim

The primary objective of eSim is to offer an open-source Electronic Design Automation (EDA) solution for electronics and electrical engineers. The software is designed to facilitate schematic creation, printed circuit board (PCB) design, and circuit simulation (analog, digital, and mixed-signal). Additionally, it provides tools for creating custom models and components.
Some of its Key Characteristics include:

1. **Open-Source Platform Integration:**
   eSim integrates multiple open-source EDA tools, including KiCad (for PCB design), Ngspice (for circuit simulation), and GHDL (for digital simulation). By leveraging open-source software, eSim eliminates licensing costs, making professional-grade circuit design tools widely accessible.

2. **Printed Circuit Board (PCB) Layout Design:**
   The software includes a dedicated PCB editor with features for component placement, trace routing, and layer management. Design Rule Checking (DRC) ensures manufacturability, while Gerber file export enables seamless fabrication. This functionality supports both novice and advanced users in developing industry-standard PCB designs.

3. **Hierarchical Circuit Design with Subcircuits:**
   To enhance modularity, eSim allows users to construct complex circuits by embedding reusable subcircuits. This hierarchical approach improves design efficiency, as commonly used circuit blocks can be stored in libraries and redeployed across projects without redundant redesign efforts.

4. **Circuit Simulation and Analysis:**
   eSim employs SPICE-based simulation for analog, digital, and mixed-signal circuits. Users can perform transient, AC, and DC analyses to assess circuit performance under different conditions. An integrated waveform viewer aids in visualizing results, simplifying debugging and optimization processes.

5. **Schematic Capture and Editing:**
   The software provides a user-friendly interface for schematic entry, featuring drag-and-drop component placement from an extensible library. Editing

tools allow for easy modifications, including component rotation, labeling, and connectivity adjustments, streamlining the initial design phase.

Chapter 3

Task Chosen

To develop a set of analog and digital IC models as modular subcircuits. Once incorporated into eSim's subcircuit repository, these models will provide a foundation for streamlined circuit design by users and developers.

3.1 Approach

The general approach taken involved selecting datasheets of developed ICs from establised Semiconductor companies such as Analog Devices, Texas Instruments, be it analog or digital whose functionalities may range from power amplifiers, logic gates to specially designed ICs. Then the design of the circuit is carried out, after which the validity and testing of the circuit is done through test circuits.

Methodology:

1. **IC Selection and Datasheet Analysis:**
   The implementation process commenced with a comprehensive review of datasheets from leading semiconductor manufacturers, including Texas Instruments, Analog Devices, and NXP Semiconductors. We identified a diverse set of integrated circuits (ICs) encompassing key functionalities such as precision amplifiers, comparators, encoders, and audio amplifiers. Selection criteria prioritized ICs that were not previously available in the eSim library while ensuring representation across both analog and digital domains (e.g., power amplifiers, logic gates, and application-specific ICs).

2. **Subcircuit Development:**
   For each selected IC, we constructed a corresponding subcircuit model using only the device model files available in the eSim library. The design process strictly adhered to manufacturer datasheet specifications, including:
   Schematic Implementation: Translating the IC's internal circuitry into a subcircuit netlist.
   Symbol Generation: Creating standardized symbols with pin configurations matching the IC's packaging (e.g., DIP, SOIC).

3. **Test Circuit Design and Validation:**
   To verify functionality, we designed test circuits for each subcircuit based on

datasheet-recommended configurations. The validation workflow involved:
Simulation: Using eSim's KiCad-to-NgSpice integration to simulate test cases and generate output waveforms.
Iterative Debugging: Comparing results against datasheet expectations; discrepancies triggered redesign of either the subcircuit or test circuit until outputs matched theoretical behavior.

4. **Library Integration:**
   Successfully validated subcircuits were added to eSim's library, ensuring future accessibility for users. This modular approach enhances the tool's versatility for circuit design tasks.

Chapter 4

ICs Implemented

4.1 Contibutions

These are the Integrated Circuits ICs that I have implemented throughout my time as an Intern at FOSSEE eSim:

1. **HD74HC30** : 8-input NAND Gates
2. **SN54S64** : 4-2-3-2 Input AND-OR-invert Gates
3. **SN74ACT86** : Quadruple 2-Input Exclusive-OR Gates
4. **CD54HC7266** : Quadruple 2-Input XNOR Gates
5. **SLOA024B_LowPass** : Sallen Key Low Pass Configuration
6. **SLOA024B_HighPass** : Sallen Key High Pass Configuration
7. **MM54C42** : BCD-to-Decimal Decoder
8. **CD4555** : Dual Binary to 1 of 4 Demultiplexers
9. **CA3045** : General Purpose NPN Transistor Arrays

4.2 HD74HC30

4.2.1 Description

The HD74HC30 is am integrated circuit that implements an 8-input NAND gate. Fabricated using advanced silicon-gate technology, it combines the low power consumption of CMOS with the operational speed comparable to LSTTL (Low-Power Schottky Transistor-Transistor Logic) devices.
Its basic function is as a Single 8-input NAND gate which gives outputs LOW only when all inputs are HIGH.Its operating voltages ranges from 2V to 6V.
Truth Table:

Inputs								Output
A	B	C	D	E	F	G	H	Y
H	H	H	H	H	H	H	H	L
L	X	X	X	X	X	X	X	H
X	L	X	X	X	X	X	X	H
X	X	L	X	X	X	X	X	H
X	X	X	L	X	X	X	X	H
X	X	X	X	L	X	X	X	H
X	X	X	X	X	L	X	X	H
X	X	X	X	X	X	L	X	H
X	X	X	X	X	X	X	L	H

H : High level
L : Low level
X : Irrelevant

Figure 4.1: Truth Table for the NAND 8 x 1

4.2.2 Applications

1. Address Decoding
   Used in memory systems to activate specific chips/modules only when all address lines match (all inputs HIGH).

2. Glitch Detection
   Monitors multiple signals simultaneously; triggers an alert (LOW output) if any input deviates unexpectedly.

3. Power Management
   Combines multiple enable signals in low-power devices to control power gating.

4.2.3 PIN Configuration

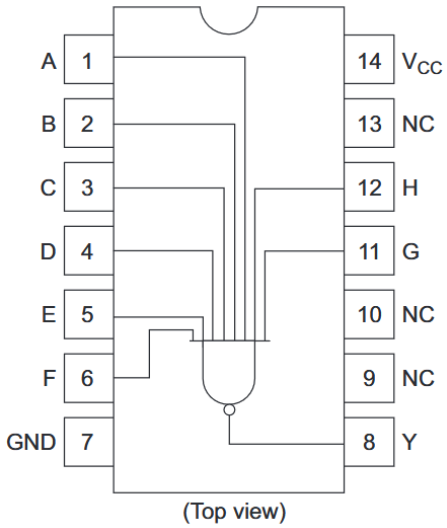

Figure 4.2: Pin Configuration

4.2.4 SubCircuit Schematic

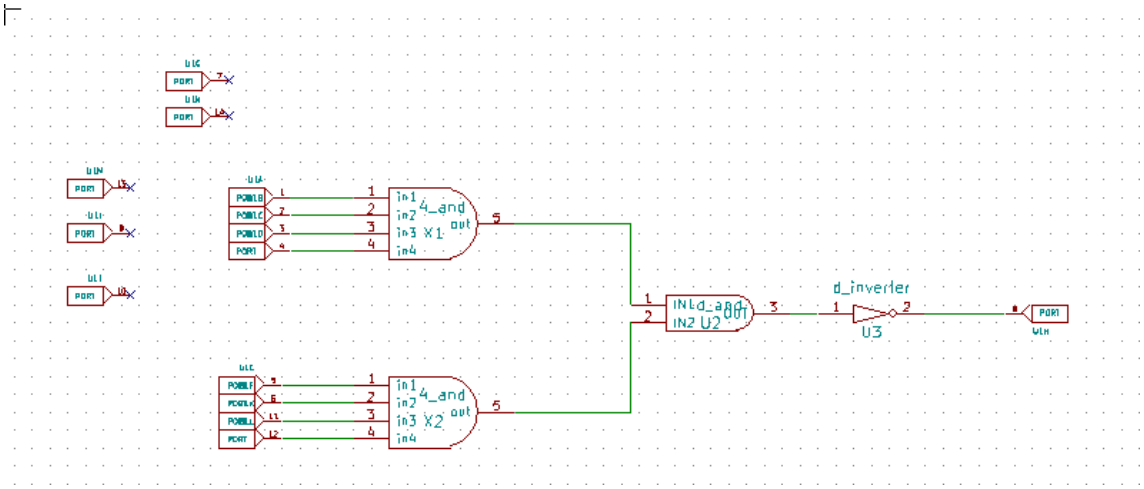

Figure 4.3: Subcircuit Schematic Layout of HD74HC30

4.2.5 IC Layout

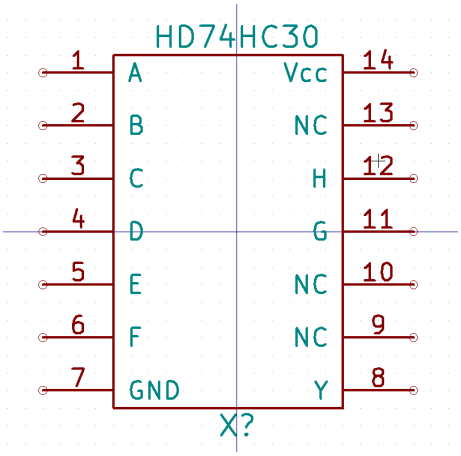

Figure 4.4: IC for HD74HC30

4.2.6 Test Circuit

This is the circuit made to verify and check the working of the implemented IC:

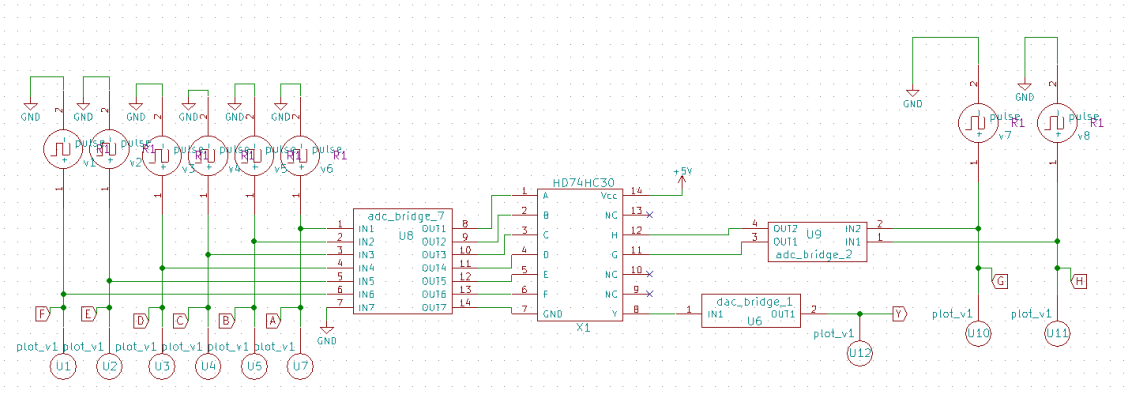

Figure 4.5: Test Circuit for HD74HC30

4.2.7 Output Waveforms

Here follows the waveform of the various inputs along with their corresponding outputs of the 8 x 1 NAND:

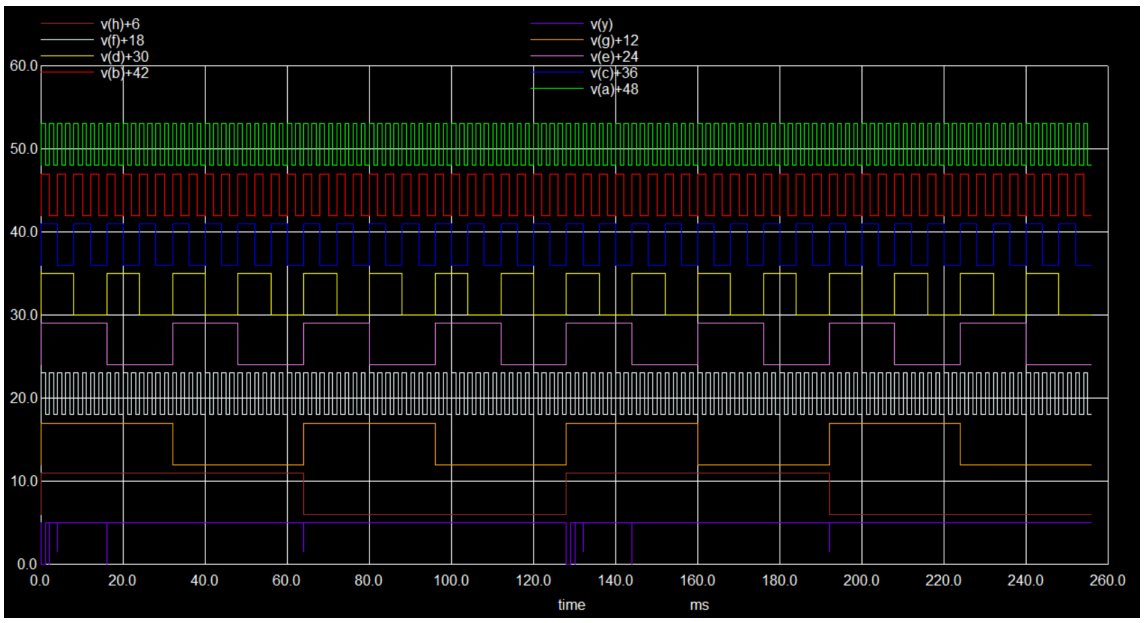

Figure 4.6: Output Waveforms of HD74HC30

4.3 SN54S64

4.3.1 Description

The SN54S64 from Texas Instruments is a 4-2-3-2 AND-OR-INVERT gate, performing the Boolean function:

$$Y = \overline{ABCD + EF + GHI + JK}$$

The SN54S64 (as opposed to the commercial SN74 series) is rated for military temperature ranges and rugged environments, making it suitable for mission-critical systems.

4.3.2 Applications

This IC has its uses for the following:

1. **Arithmetic Logic Units (ALUs):**
   Used to implement complex logic functions like partial sums, carry generation, and logical comparison.

2. **Data Path Optimization:**
   Helps reduce the number of discrete gates by combining logic expressions into a single gate, reducing propagation delay.

3. **Control Logic Circuits:**
   Ideal for state machines, instruction decoding, and control signal generation where compact logic combinations are needed.

4.3.3 PIN Configuration

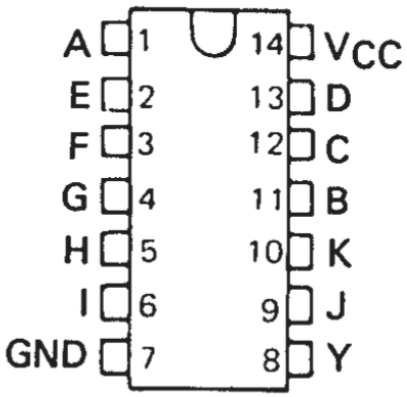

Figure 4.7: Pin Configuration

4.3.4 SubCircuit Schematic

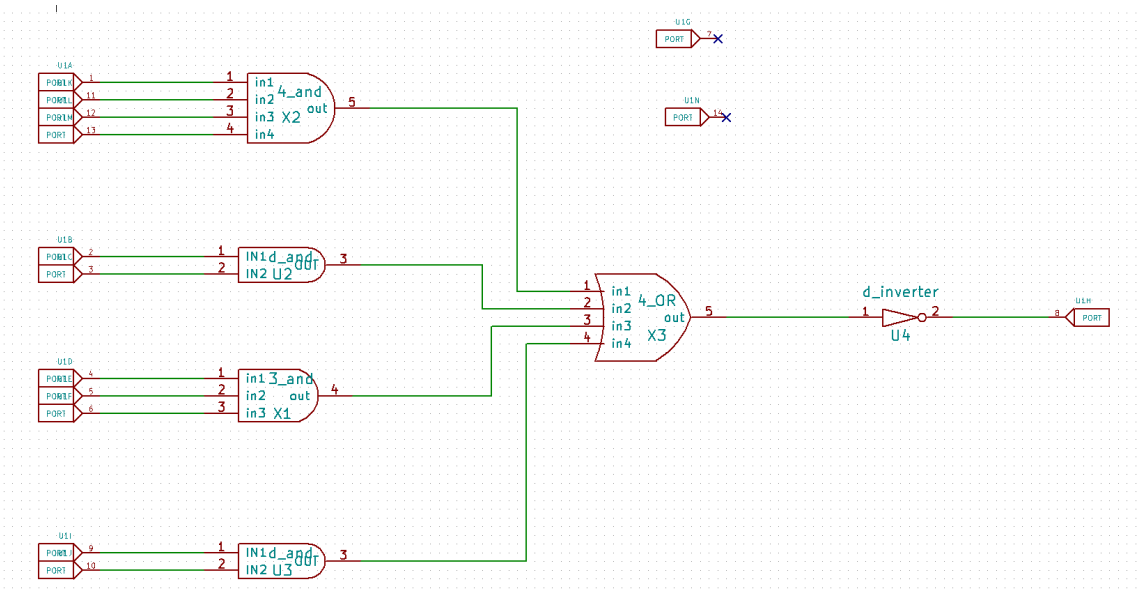

Figure 4.8: Subcircuit Schematic Layout of SN54S64

4.3.5 IC Layout

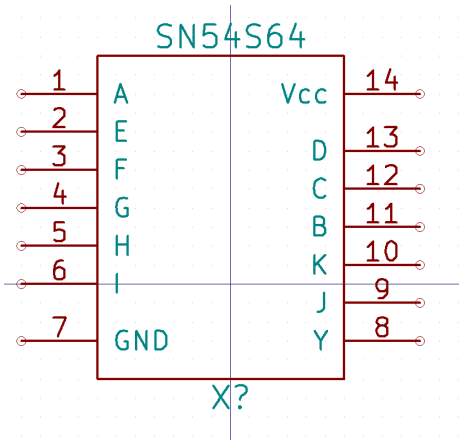

Figure 4.9: IC for SN54S64

4.3.6 Test Circuit

This is the circuit made to verify and check the working of the implemented IC:

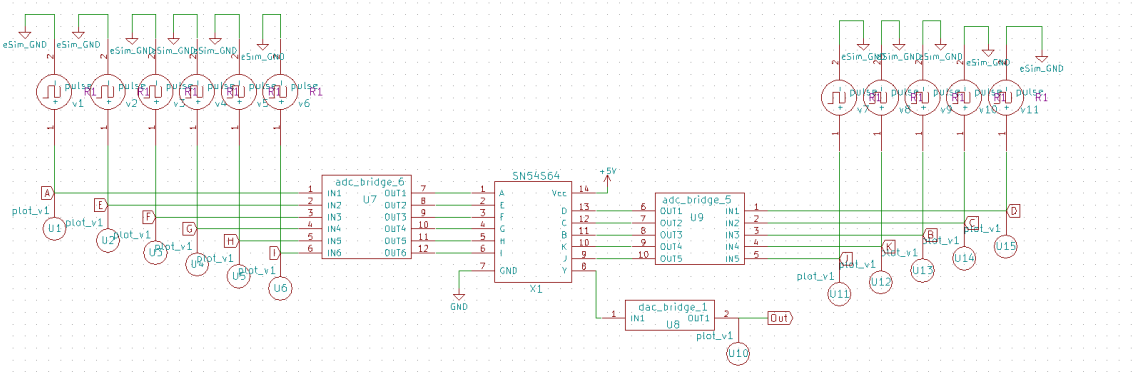

Figure 4.10: Test Circuit for SN54S64

4.3.7 Output Waveforms

Here follows the waveform of the various inputs along with their corresponding outputs of the 4-2-3-2 AND-OR-INVERT:

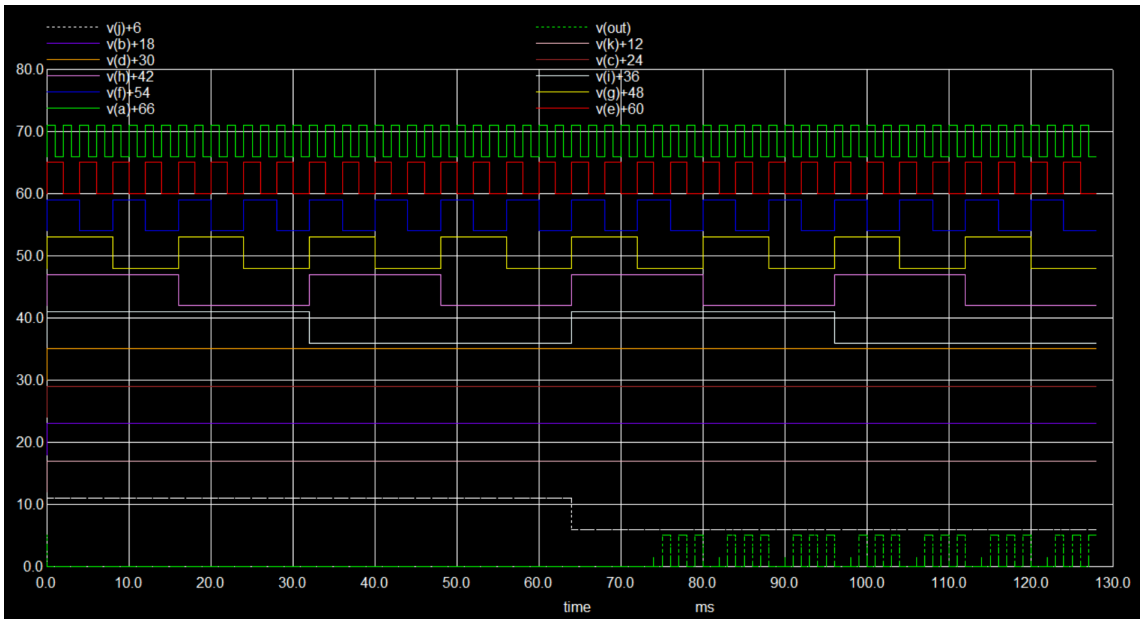

Figure 4.11: Output Waveforms of SN54S64

4.4 SN74ACT86

4.4.1 Description

The SN74ACT86 is a quad 2-input XOR (exclusive-OR) gate IC from Texas Instruments, built using Advanced CMOS technology with TTL-compatible inputs. It contains four independent XOR gates that perform the logic function:

$$Y = A \oplus B$$

INPUTS		OUTPUT Y
A	B	
L	L	L
L	H	H
H	L	H
H	H	L

Figure 4.12: Truth Table of XOR

4.4.2 Applications

This IC has its uses for the following:

1. **Data Encryption (Simple XOR Cipher)**:
   This gate is used for a lightweight encryption.

   $$Encrypted = Data \oplus Key$$

   Same operation used for decryption.

2. **Phase Detection in PLLs:**
   XOR gates detect phase difference between clock signals (square waves). Useful in synchronization and frequency control.

3. **Parity Generators and Checkers:**
   Used to detect errors in data transmission or storage.Parity bit is generated using XOR across all data bits.

4.4.3 PIN Configuration

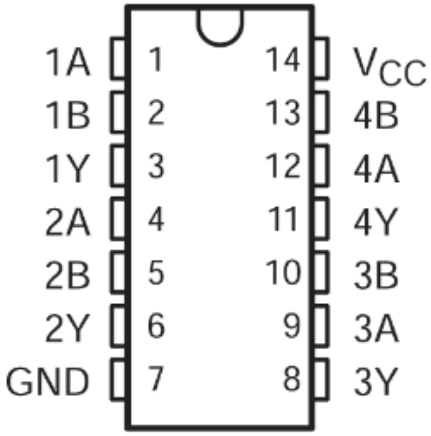

Figure 4.13: Pin Configuration

4.4.4 SubCircuit Schematic

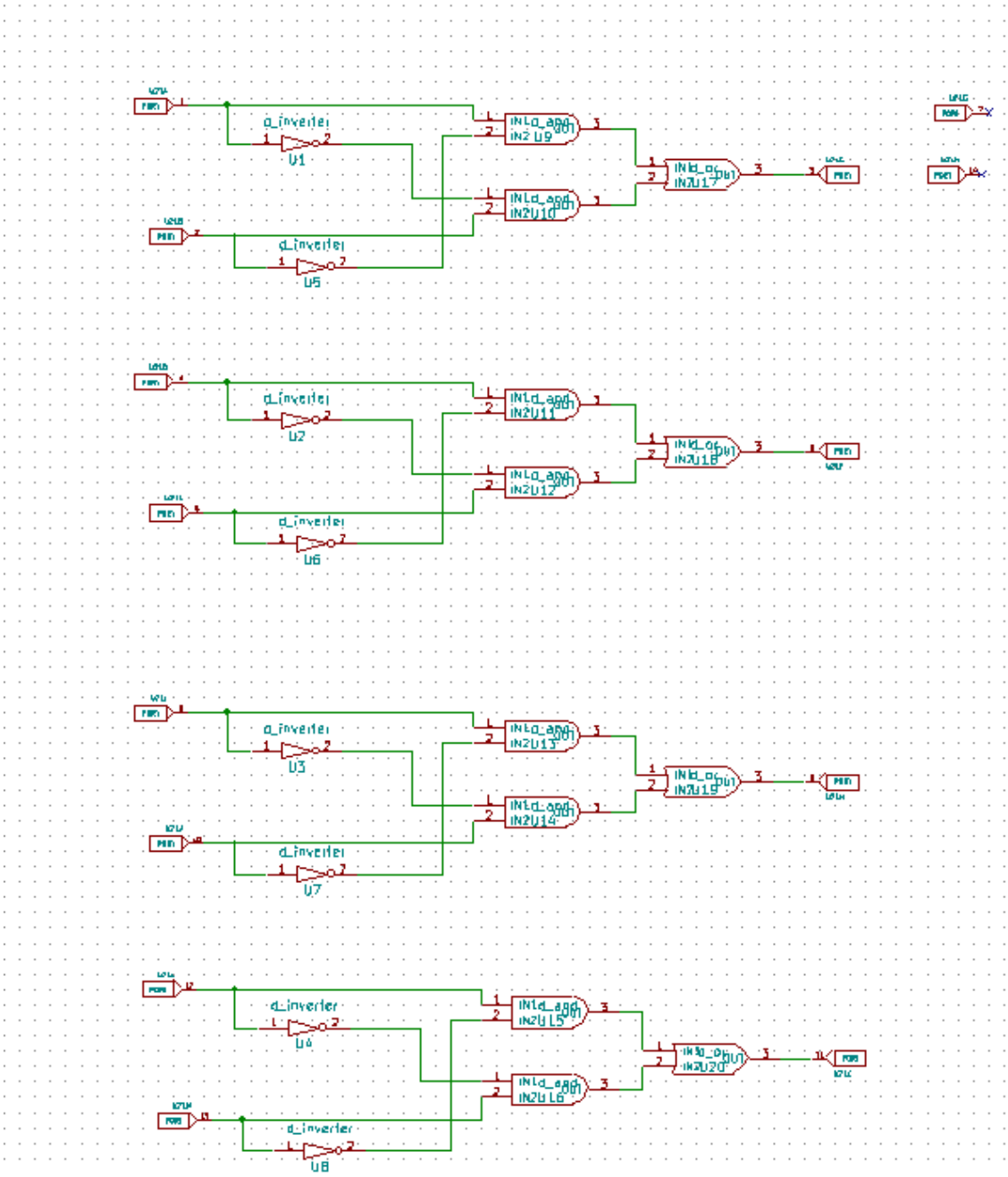

Figure 4.14: Subcircuit Schematic Layout of SN74ACT86

4.4.5 IC Layout

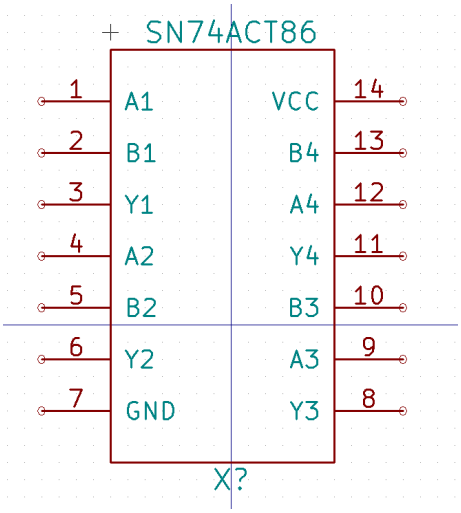

Figure 4.15: IC for SN74ACT86

4.4.6 Test Circuit

This is the circuit made to verify and check the working of the implemented IC:

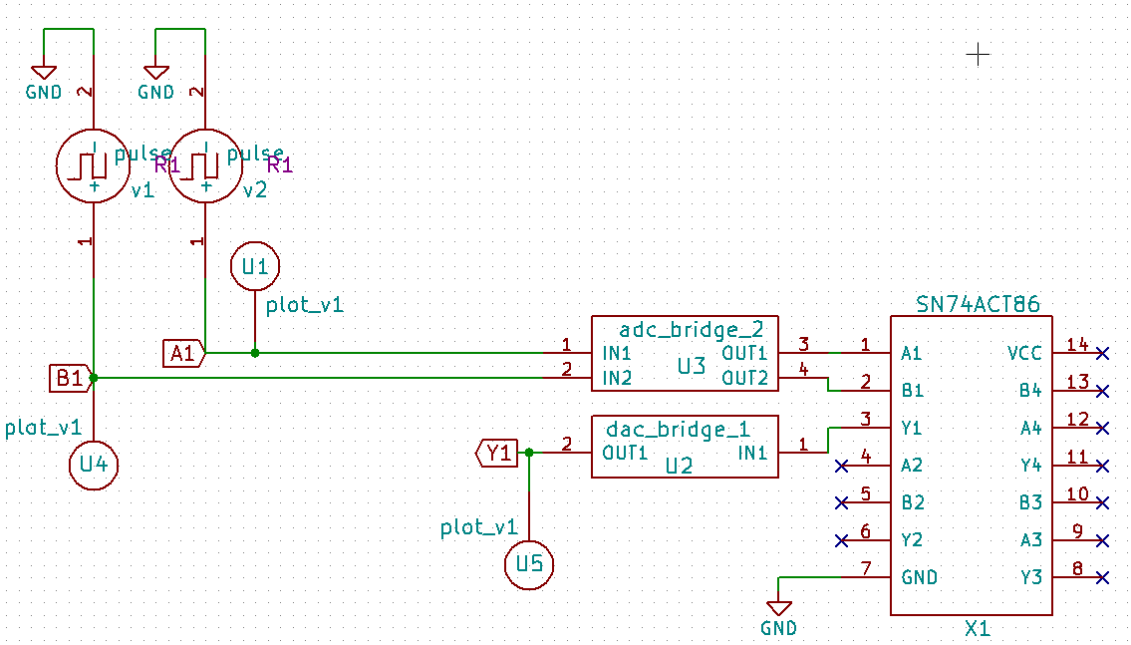

Figure 4.16: Test Circuit for SN74ACT86

4.4.7 Output Waveforms

Here follows the waveform of the various inputs along with their corresponding outputs of the SN74ACT86:

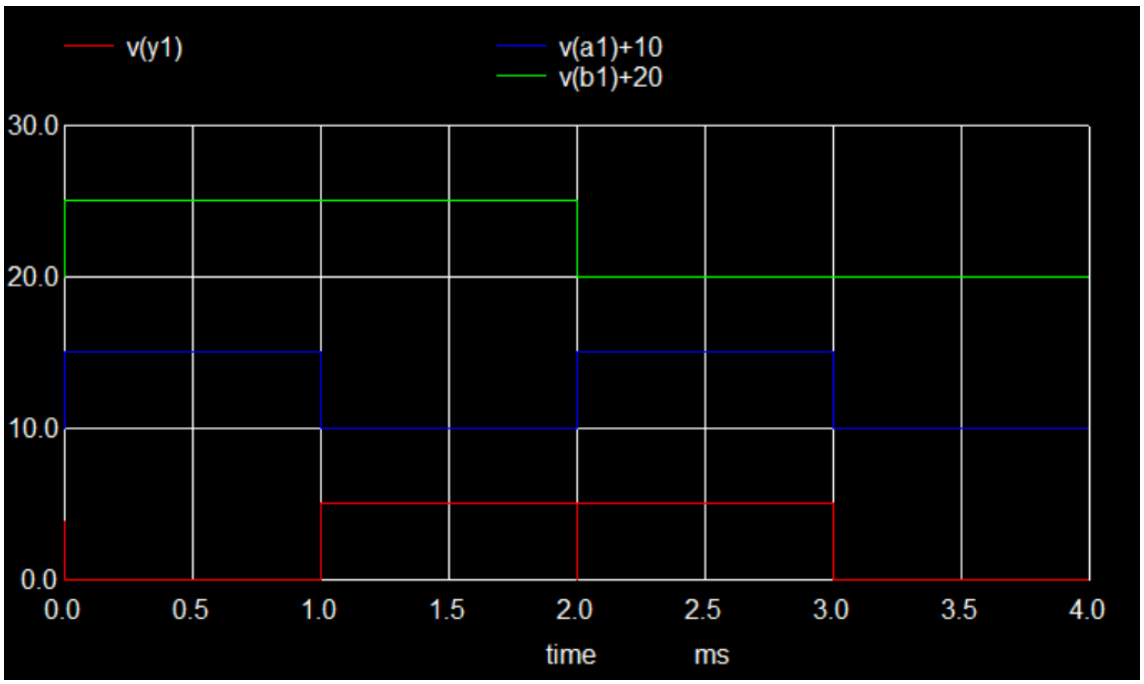

Figure 4.17: Output Waveforms of SN74ACT86

4.5 CD54HC7266

4.5.1 Description

The CD54HC7266 is a high-speed CMOS logic integrated circuit comprising four independent 2-input XNOR gates. Each gate implements the exclusive-NOR (XNOR) logic function, which produces high (logic 1) only when the inputs are identical (either both high or both low). The CD54 prefix specifying extended temperature and reliability ratings. Each gate performs the Boolean function:

$$Y = \overline{A \oplus B}$$

Truth Table:

INPUTS		OUTPUT
A	B	Y
L	L	H
L	H	L
H	L	L
H	H	H

Figure 4.18: Truth Table for XNOR gate

4.5.2 Applications

1. **Memory Address Decoding:**
   XNOR gates help in building address comparators in cache controllers and memory-mapped I/O systems.

2. **Cryptographic Logic:**
   XNORs are sometimes used in basic encryption/decryption logic for creating predictable inverse operations.

3. **Digital Matching Circuits:**
   Used in pattern recognition or address matching circuits where you need to check if input patterns match a reference.

4. **Parity Generators and Checkers:**
   XNOR gates can help generate and verify even parity, useful in error detection in data transmission and memory systems.

4.5.3 PIN Configuration

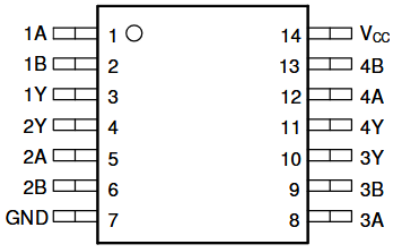

Figure 4.19: Pin Configuration

4.5.4 SubCircuit Schematic

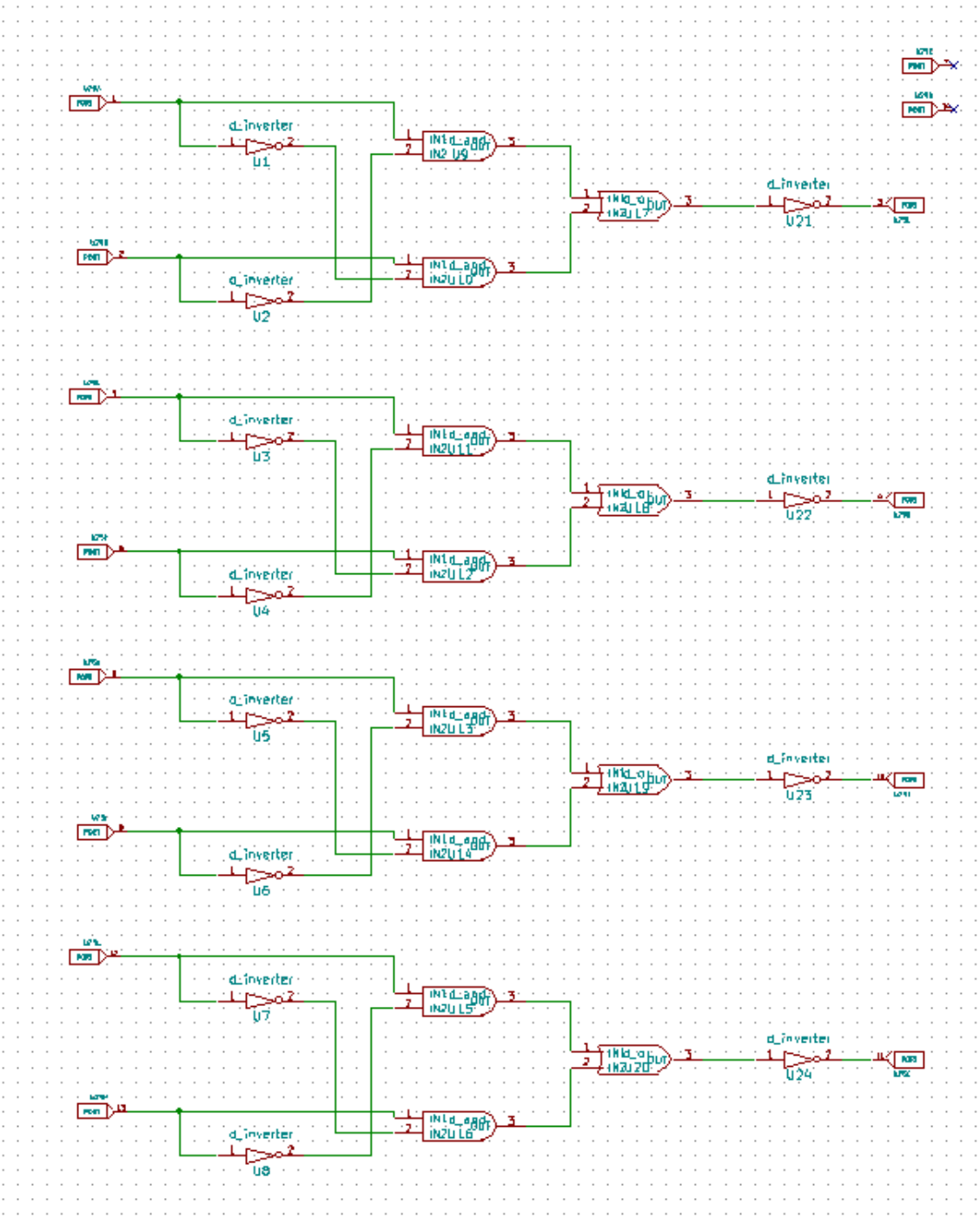

Figure 4.20: Subcircuit Schematic Layout of CD54HC7266

4.5.5 IC Layout

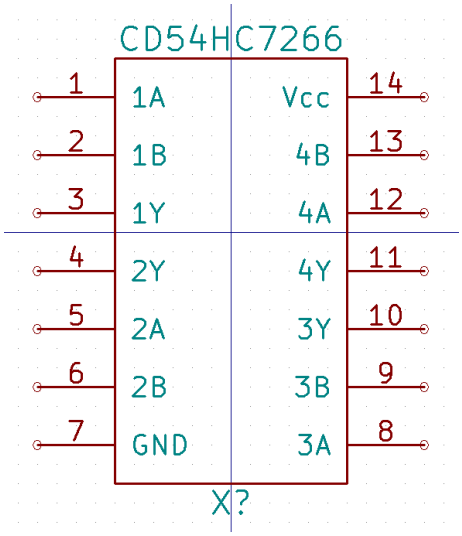

Figure 4.21: IC for CD54HC7266

4.5.6 Test Circuit

This is the circuit made to verify and check the working of the implemented IC:

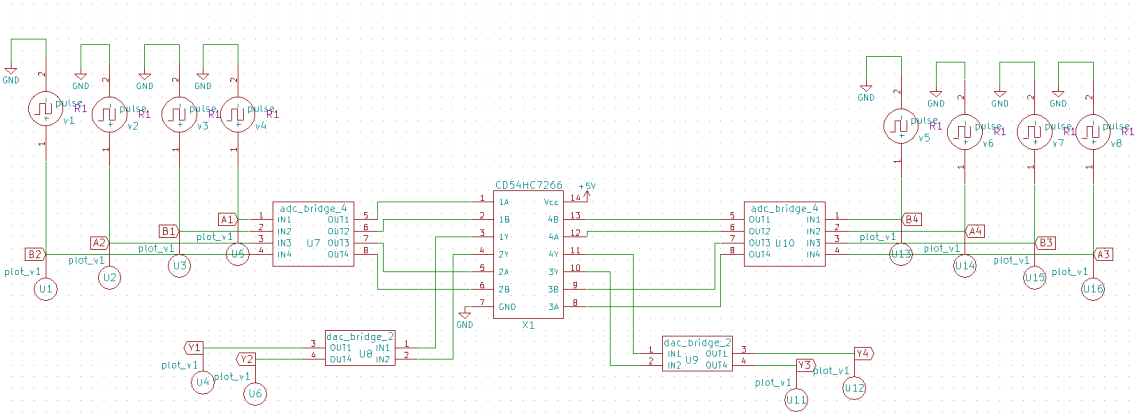

Figure 4.22: Test Circuit for CD54HC7266

4.5.7 Output Waveforms

Here follows the waveform of the various inputs along with their corresponding outputs of the CD54HC7266:

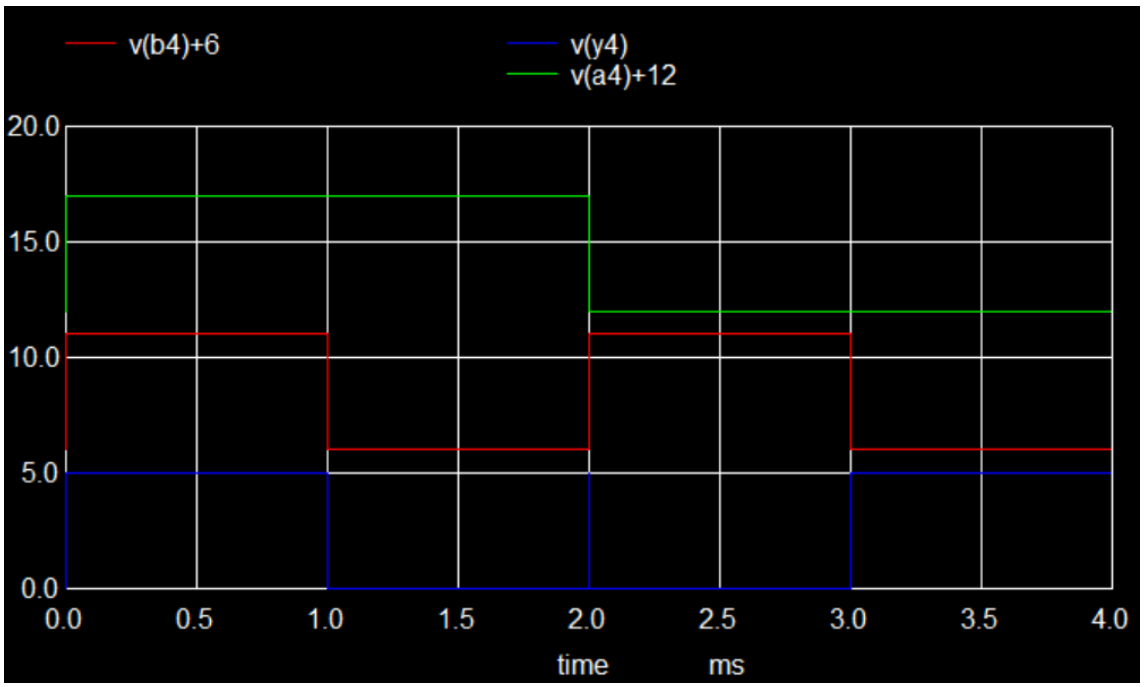

Figure 4.23: Output Waveforms of CD54HC7266

4.6 SLOA024B_LowPass OP AMP

4.6.1 Description

The SLOA024B application report by Texas Instruments provides a detailed explanation of low-pass filters using operational amplifiers. A low-pass filter is designed to allow signals with frequencies below a certain cutoff frequency (fcfc) to pass through while attenuating higher-frequency signals. The report explains both passive and active low-pass filters, emphasizing the advantages of active designs using op amps, such as improved performance, buffering capability, and gain control.
The Sallen-Key topology is a popular active filter configuration that uses an op amp, two resistors, and two capacitors to form a second-order low-pass filter. It provides a simple, stable, and cost-effective solution for achieving sharper roll-off compared to first-order designs.
The cutoff frequency fc:

$$f_c = \frac{1}{2\pi\sqrt{R_1 R_2 C_1 C_2}}$$

This architecture is well-suited for audio filters, signal conditioning, and sensor interface circuits, due to its simplicity and low component count.

4.6.2 Applications

1. **Audio Signal Processing:**
   Used to remove high-frequency noise and unwanted components from audio signals, especially in equalizers, tone controls, and amplifiers.

2. **Sensor Signal Conditioning:**
   Smooths out noisy or fluctuating signals from sensors (like temperature or pressure sensors) to ensure clean and stable input to microcontrollers or data acquisition systems.

3. **Communication Systems:**
   Used to limit signal bandwidth and reduce interference in modulation/demodulation circuits and receiver front ends.

4. **Anti-Aliasing Filters:**
   Placed before analog-to-digital converters (ADCs) to eliminate high-frequency signals that could cause aliasing and distort digital representations.

4.6.3 SubCircuit Schematic

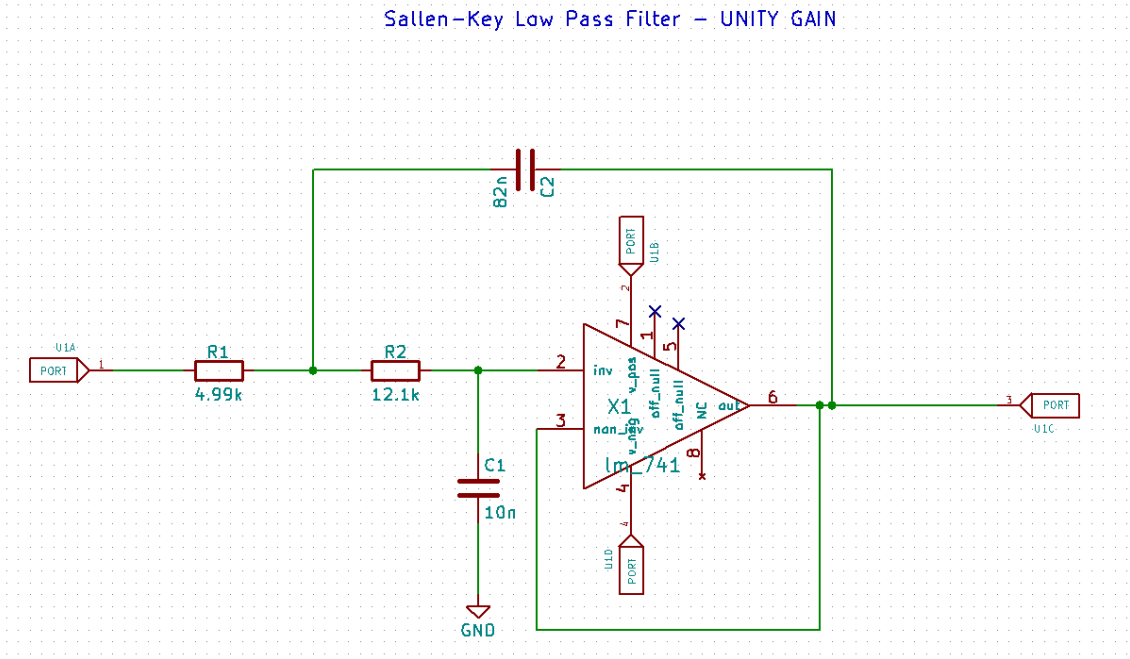

Figure 4.24: Subcircuit Schematic Layout of SLOA024B for Low Pass Sallen-Key Configuration.

4.6.4 IC Layout

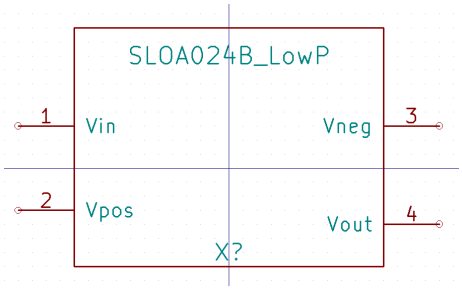

Figure 4.25: IC for SLOA024B for Low Pass Sallen-Key Configuration

4.6.5 Test Circuit

This is the circuit made to verify and check the working of the implemented IC:

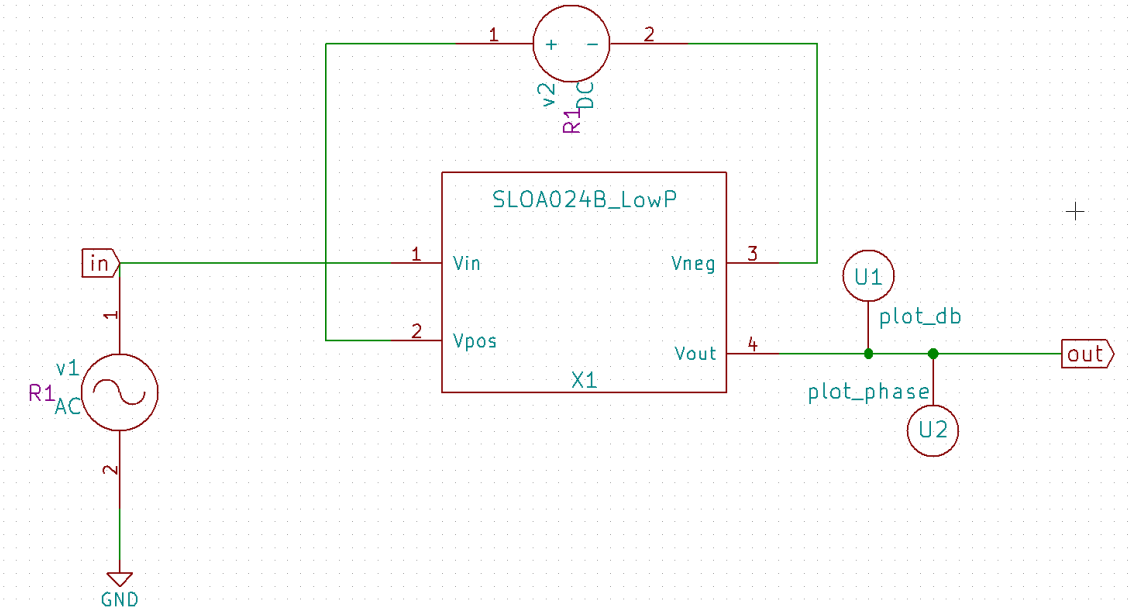

Figure 4.26: Test Circuit for SLOA024B for Low Pass Sallen-Key Configuration

4.6.6 Output Waveforms

Here follows the AC analysis of the SLOA024B for Low Pass Sallen-Key Configuration:

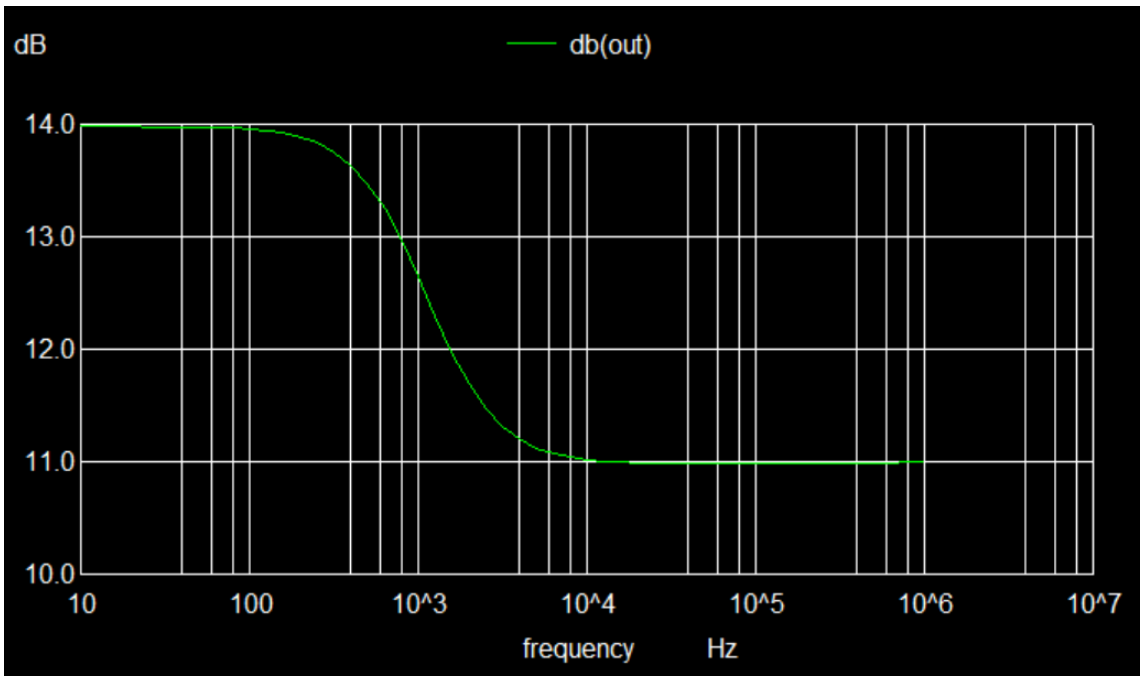

Figure 4.27: Manitude Plot of SLOA024B Low Pass Sallen-Key Configuration

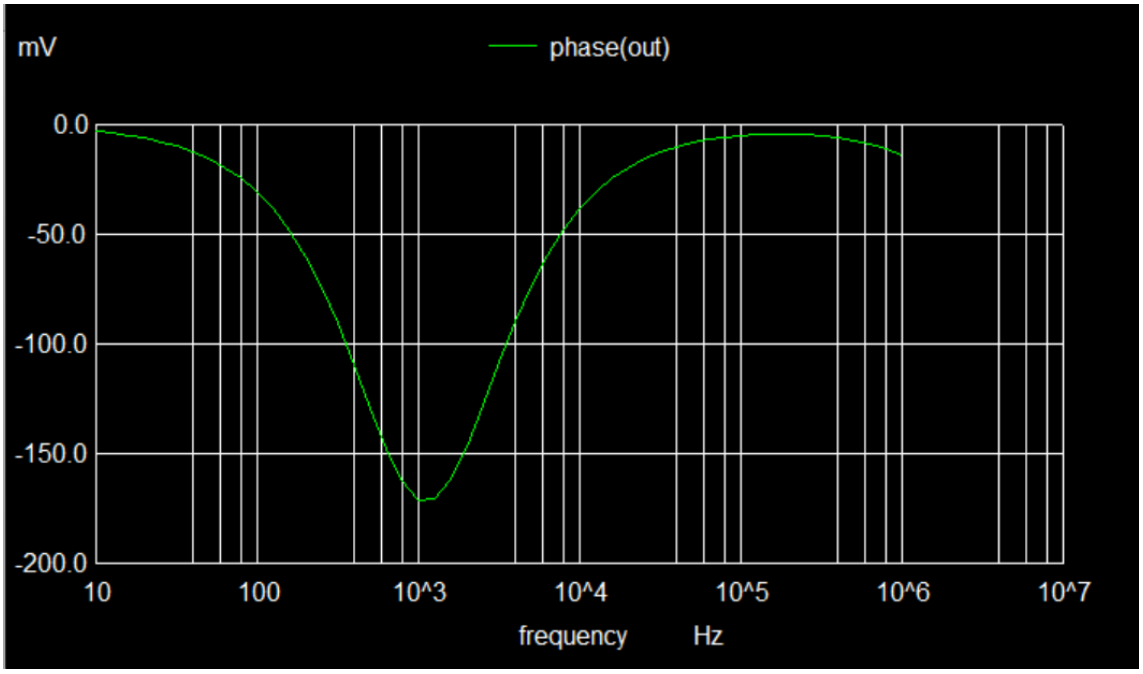

Figure 4.28: Phase Plot of SLOA024B Low Pass Sallen-Key Configuration

4.7 SLOA024B_HighPass

4.7.1 Description

In SLOA024B, high-pass filters are explained as circuits that allow high-frequency signals to pass while attenuating low-frequency components. The Sallen-Key high-pass filter is presented as a simple and effective active filter topology using an op amp, two capacitors, and two resistors to form a second-order high-pass filter. It allows signals above a certain cutoff frequency (fcfc) to pass while attenuating lower frequencies.
The cutoff frequency is given by:

$$f_c = \frac{1}{2\pi\sqrt{R_1 R_2 C_1 C_2}}$$

This configuration provides a sharper roll-off than first-order filters and offers good stability and performance with minimal components. It's especially useful when a flat passband and predictable frequency response are required.

4.7.2 Applications

1. **AC Coupling in Audio Systems:**
   Blocks DC offset from audio signals and ensures clean transmission of audible frequencies in amplifiers and mixers.

2. **Communication Systems:**
   Removes low-frequency interference and hum. It acts as a pre-emphasis filter in FM transmitters.

3. **Modular Synths and Audio Effects:**
   Shapes sound in analog synths or effects pedals by removing subsonic content.

4. **Power Line Noise Rejection:**
   Removes low-frequency interference such as 50/60 Hz hum from power lines in analog circuits.

4.7.3 SubCircuit Schematic

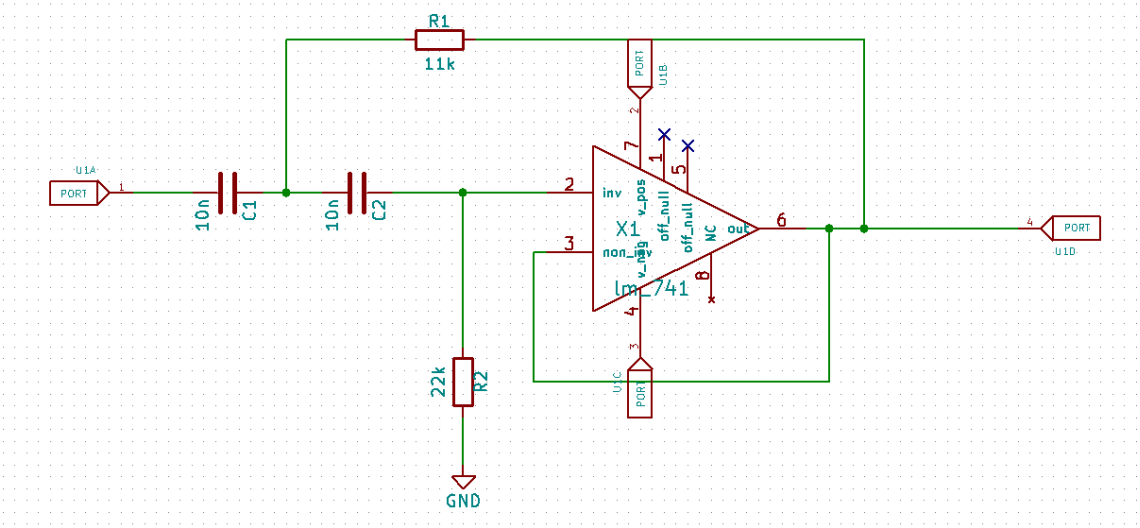

Figure 4.29: Subcircuit Schematic Layout of SLOA024B for High Pass Sallen-Key Configuration.

4.7.4 IC Layout

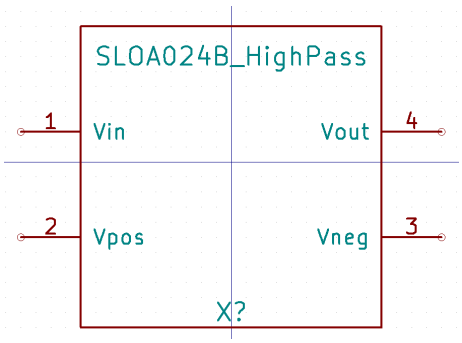

Figure 4.30: IC for SLOA024B for High Pass Sallen-Key Configuration

4.7.5 Test Circuit

This is the circuit made to verify and check the working of the implemented IC:

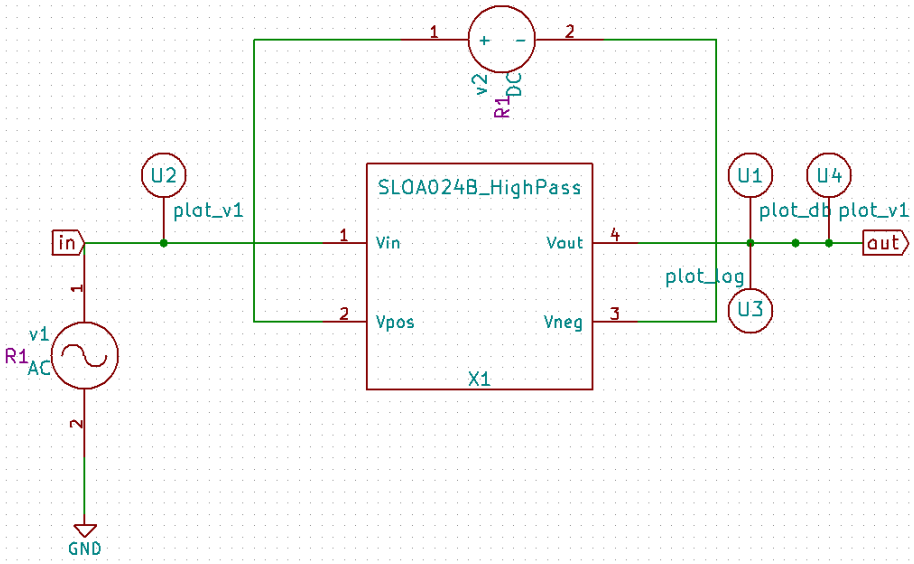

Figure 4.31: Test Circuit for SLOA024B for High Pass Sallen-Key Configuration

4.7.6 Output Waveforms

Here follows the AC analysis of the SLOA024B for High Pass Sallen-Key Configuration:

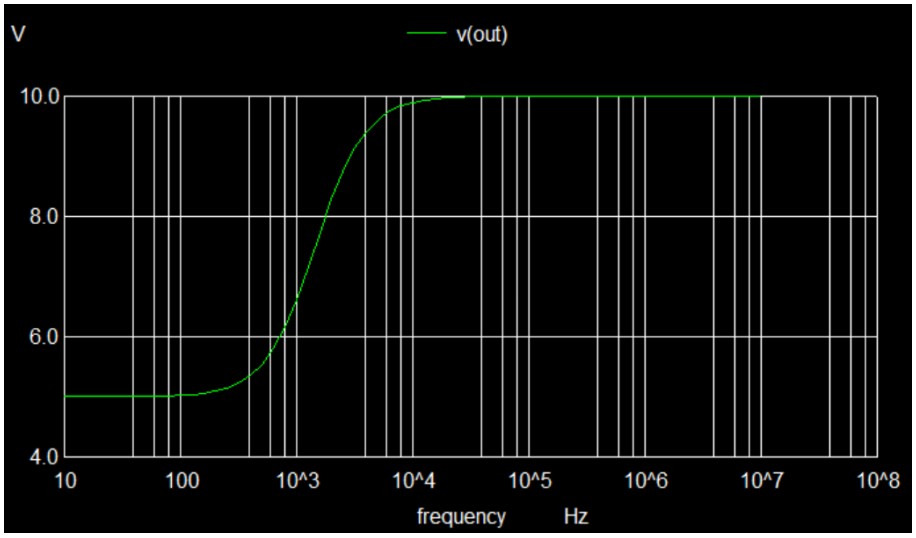

Figure 4.32: Manitude Plot of SLOA024B High Pass Sallen-Key Configuration

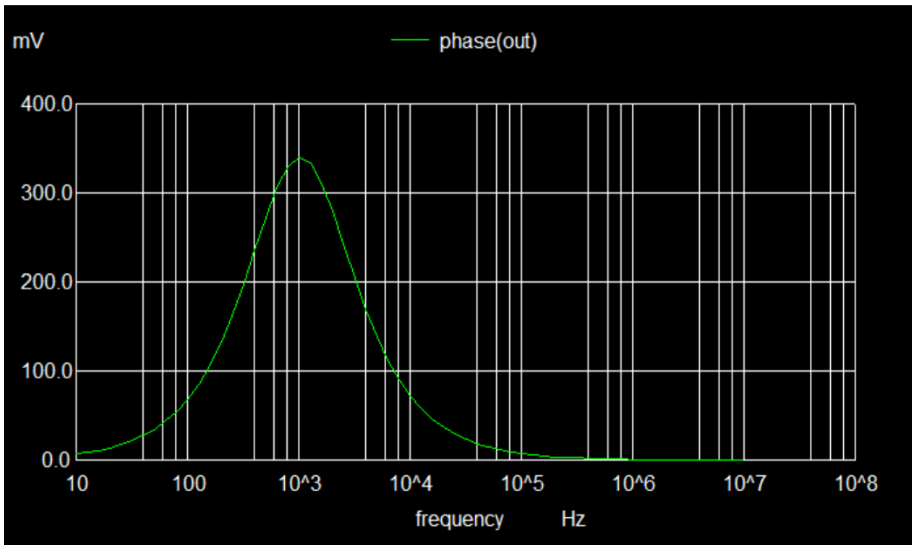

Figure 4.33: Phase Plot of SLOA024B High Pass Sallen-Key Configuration

4.8 MM54C42

4.8.1 Description

The MM54C42 is a one-of-ten decoder built using CMOS technology with N- and P-channel enhancement-mode transistors. It accepts a 4-bit binary input and decodes it into one active-low output (logic '0') among ten outputs (Y0–Y9). For valid inputs from 0 to 9, only the corresponding output goes low, while all others stay high. For inputs from 10 to 15, all outputs remain high, indicating invalid input.
Truth Table:

Inputs				Outputs									
D	C	B	A	0	1	2	3	4	5	6	7	8	9
0	0	0	0	0	1	1	1	1	1	1	1	1	1
0	0	0	1	1	0	1	1	1	1	1	1	1	1
0	0	1	0	1	1	0	1	1	1	1	1	1	1
0	0	1	1	1	1	1	0	1	1	1	1	1	1
0	1	0	0	1	1	1	1	0	1	1	1	1	1
0	1	0	1	1	1	1	1	1	0	1	1	1	1
0	1	1	0	1	1	1	1	1	1	0	1	1	1
0	1	1	1	1	1	1	1	1	1	1	0	1	1
1	0	0	0	1	1	1	1	1	1	1	1	0	1
1	0	0	1	1	1	1	1	1	1	1	1	1	0
1	0	1	0	1	1	1	1	1	1	1	1	1	1
1	0	1	1	1	1	1	1	1	1	1	1	1	1
1	1	0	0	1	1	1	1	1	1	1	1	1	1
1	1	0	1	1	1	1	1	1	1	1	1	1	1
1	1	1	0	1	1	1	1	1	1	1	1	1	1
1	1	1	1	1	1	1	1	1	1	1	1	1	1

Figure 4.34: Truth Table for MM54C42

4.8.2 Applications

1. **Automotive:**
   Used in dashboard display control, sensor addressing, and diagnostic systems to select and activate specific circuits or indicators based on digital input codes.

2. **Alarm Systems:**
   Helps manage zone selection in multi-zone security systems, enabling the controller to monitor or activate alarms for specific areas using binary input control.

3. **Remote Metering:**
   Supports data selection and routing in remote monitoring systems (e.g., water, gas, electricity meters), enabling selection of one sensor or meter from many.

4. **Data Terminals:**
   Facilitates device addressing, keyboard decoding, and input/output management in terminals that communicate digital data between systems.

4.8.3 PIN Configuration

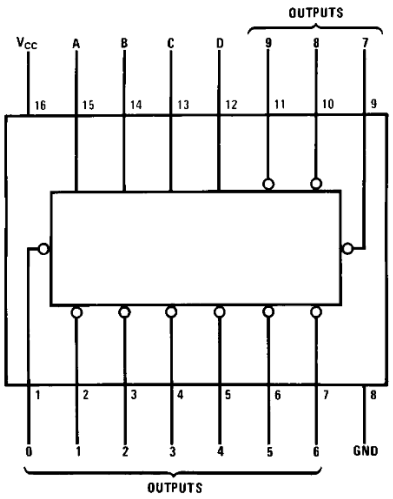

Figure 4.35: Pin Configuration

4.8.4 SubCircuit Schematic

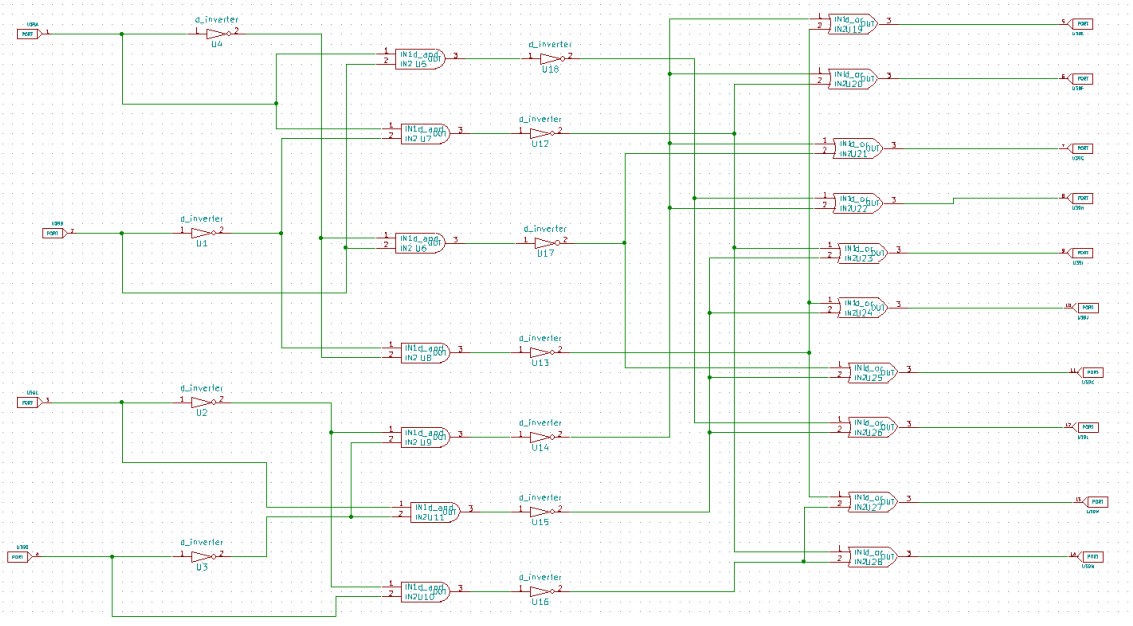

Figure 4.36: Subcircuit Schematic Layout of MM54C42

4.8.5 IC Layout

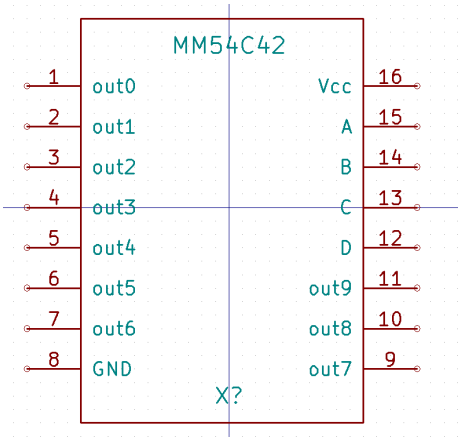

Figure 4.37: IC for MM54C42

4.8.6 Test Circuit

This is the circuit made to verify and check the working of the implemented IC:

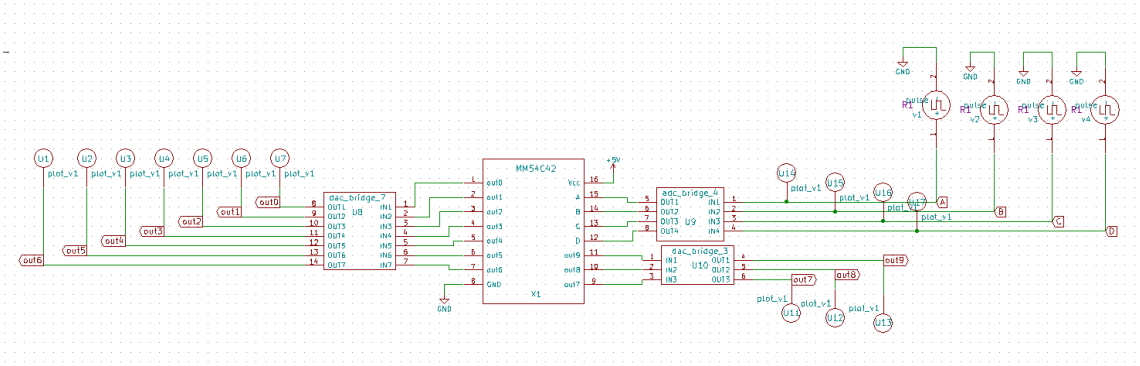

Figure 4.38: Test Circuit for MM54C42

4.8.7 Output Waveforms

Here follows the waveform of the various inputs along with their corresponding outputs of the MM54C42:

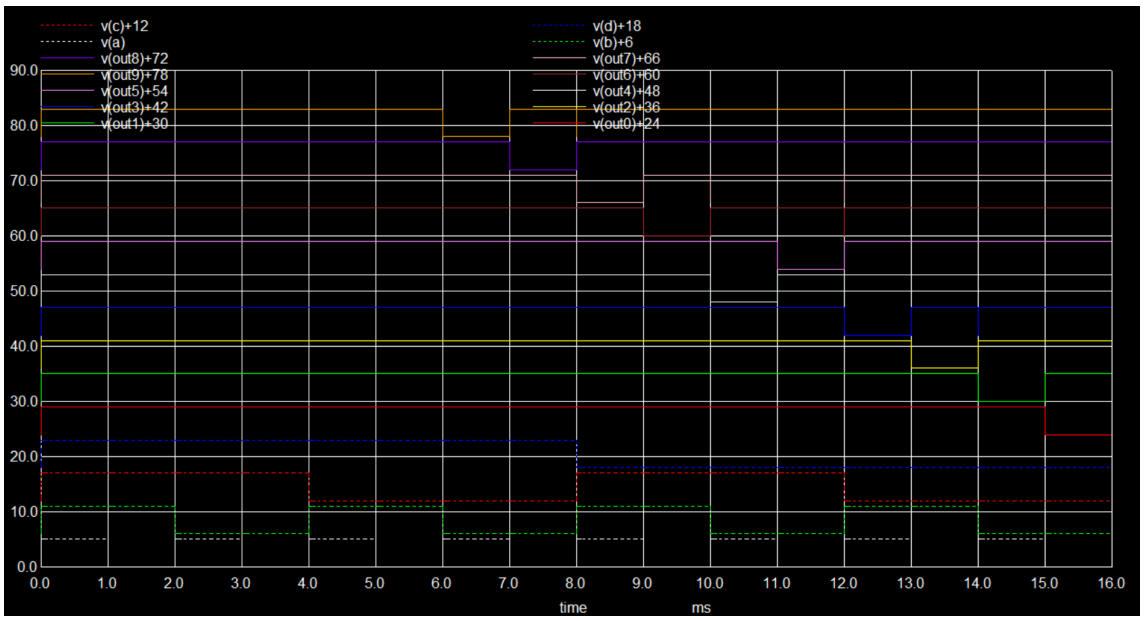

Figure 4.39: Output Waveforms of MM54C42

4.9 CD4555

4.9.1 Description

The CD4555 is a dual 1-of-4 decoder/demultiplexer designed to decode two 2-bit binary inputs into four mutually exclusive outputs each. It features separate enable inputs for each decoder, allowing flexible control and demultiplexing operations. When enabled, the selected output goes low (logic 0) while all others remain high.
Truth Table:

INPUTS			OUTPUTS CD4555B			
ENABLE	SELECT					
$\overline{E}$	B	A	Q3	Q2	Q1	Q0
0	0	0	0	0	0	1
0	0	1	0	0	1	0
0	1	0	0	1	0	0
0	1	1	1	0	0	0
1	X	X	0	0	0	0

X = DON'T CARE

LOGIC 1 ≡ HIGH
LOGIC 0 ≡ LOW

Figure 4.40: Truth Table for CD4555

4.9.2 Applications

1. **Data Routing and Demultiplexing:**
   Used to route a single data input to one of multiple outputs, such as in communication systems or digital buses.

2. **Memory Address Decoding:**
   Helps select specific memory locations or blocks by decoding address lines, especially in small-scale memory systems.

3. **Alarm and Monitoring Systems:**
   Used to activate specific indicators, alarms, or sensors depending on control logic inputs.

4.9.3 PIN Configuration

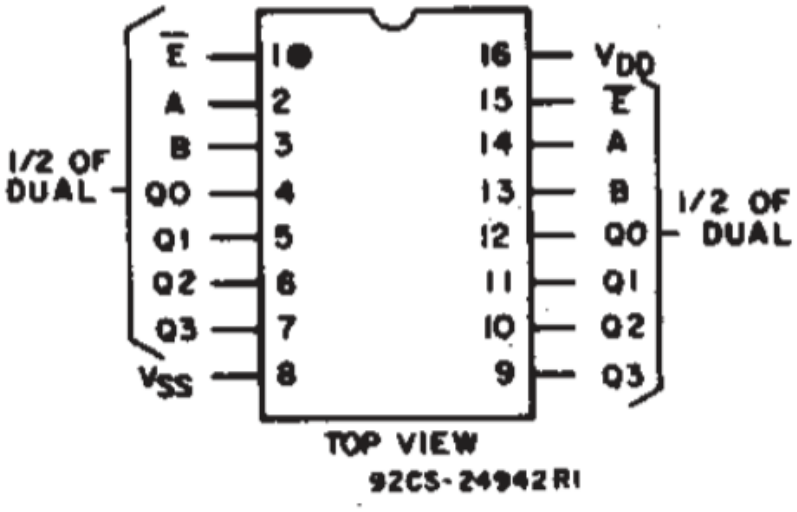

Figure 4.41: Pin Configuration

4.9.4 SubCircuit Schematic

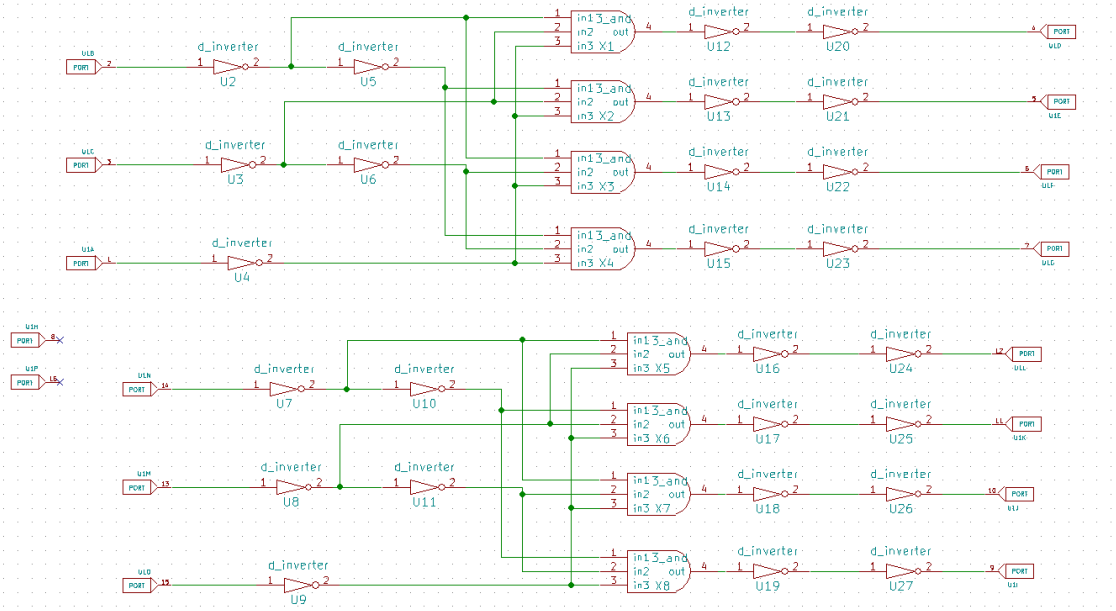

Figure 4.42: Subcircuit Schematic Layout of CD4555

4.9.5 IC Layout

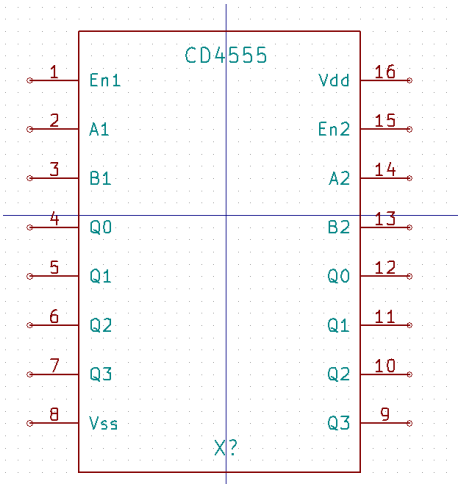

Figure 4.43: IC for CD4555

4.9.6 Test Circuit

This is the circuit made to verify and check the working of the implemented IC:

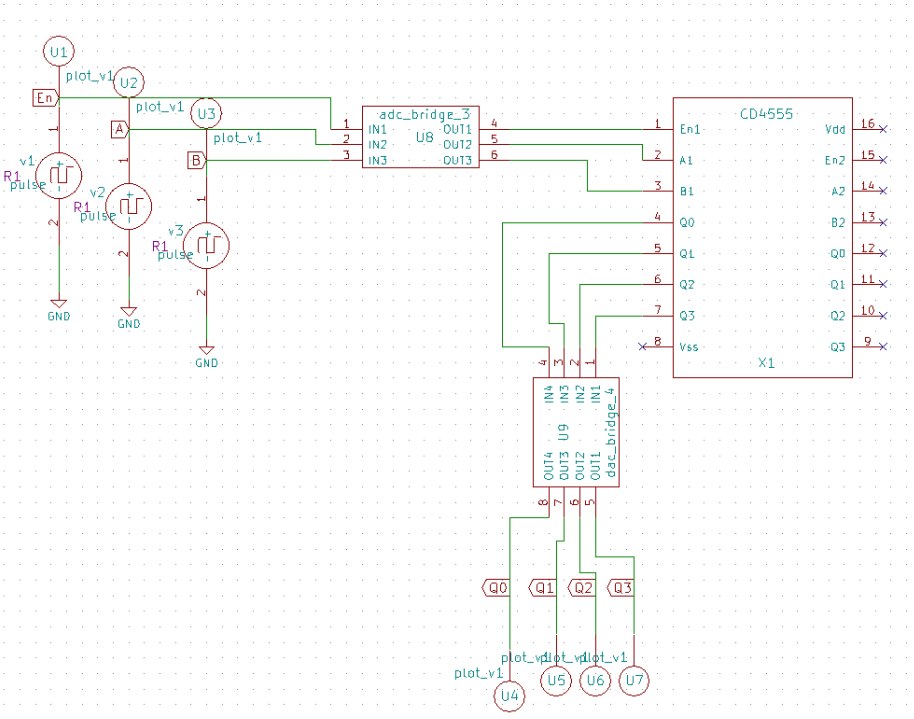

Figure 4.44: Test Circuit for CD4555

4.9.7 Output Waveforms

Here follows the waveform of the various inputs along with their corresponding outputs of the CD4555:

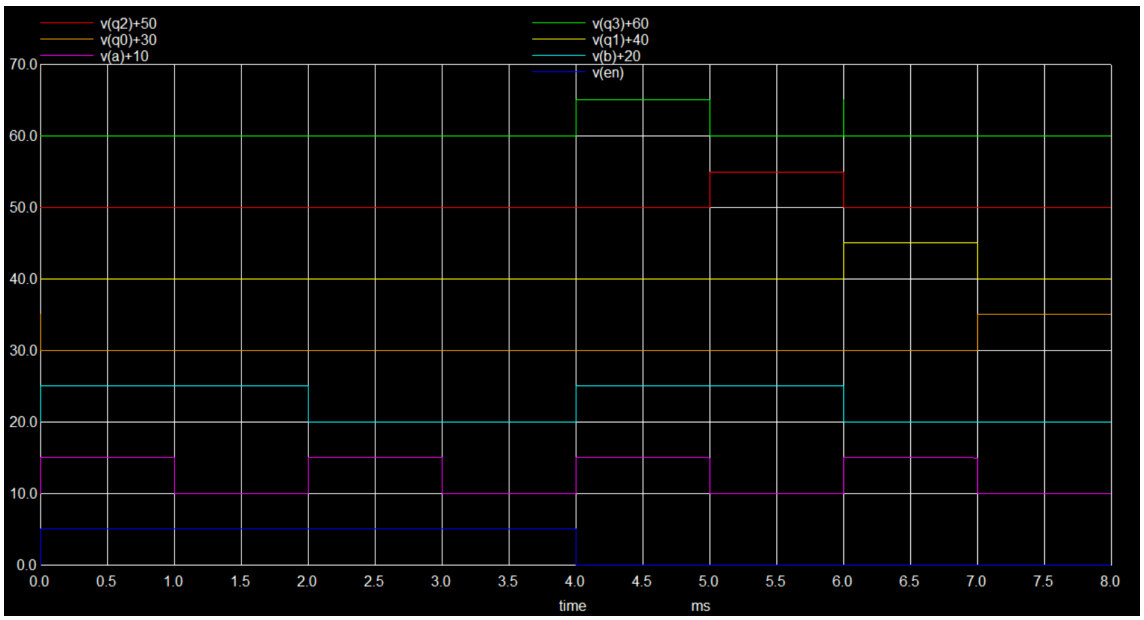

Figure 4.45: Output Waveforms of CD4555

4.10 CA3045

4.10.1 Description

The CA3045 is a monolithic general-purpose NPN transistor array, typically containing five independent NPN transistors on a single chip. It is designed for use in applications where matched transistor characteristics and thermal tracking are important. The array ensures excellent electrical matching between transistors and low thermal drift, making it suitable for analog circuits such as differential amplifiers, current mirrors, and analog switches.

4.10.2 Applications

1. **Low-Power Amplifier Circuits:**
   Ideal for use in circuits operating from DC up to the VHF range due to its high-frequency response.

2. **Temperature-Compensated Amplifiers:**
   The monolithic construction ensures close thermal coupling, which helps maintain performance over a wide temperature range.

3. **Instrumentation and Signal Processing:**
   Used in precision analog systems for tasks like signal amplification, current mirroring, and switching.

4.10.3 PIN Configuration

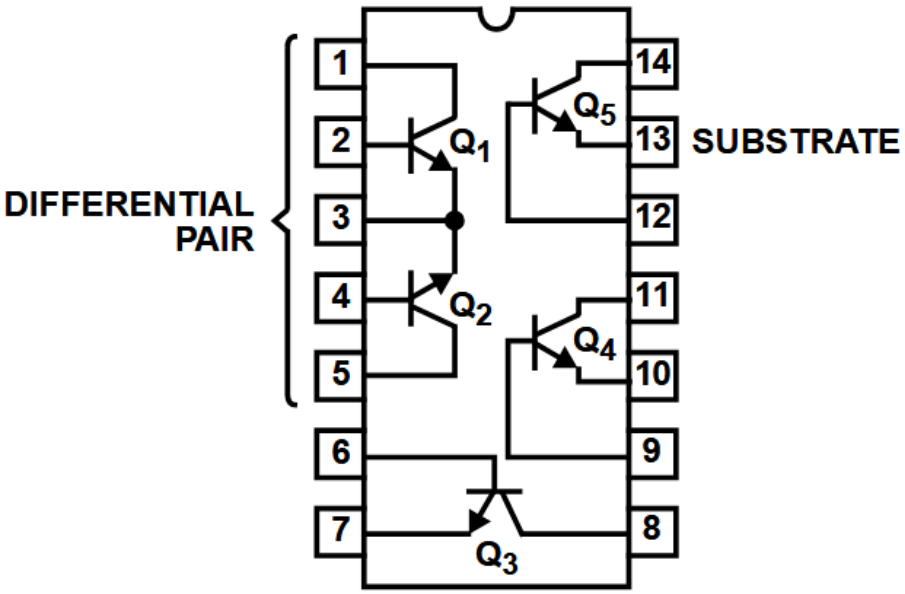

Figure 4.46: Pin Configuration

4.10.4 SubCircuit Schematic

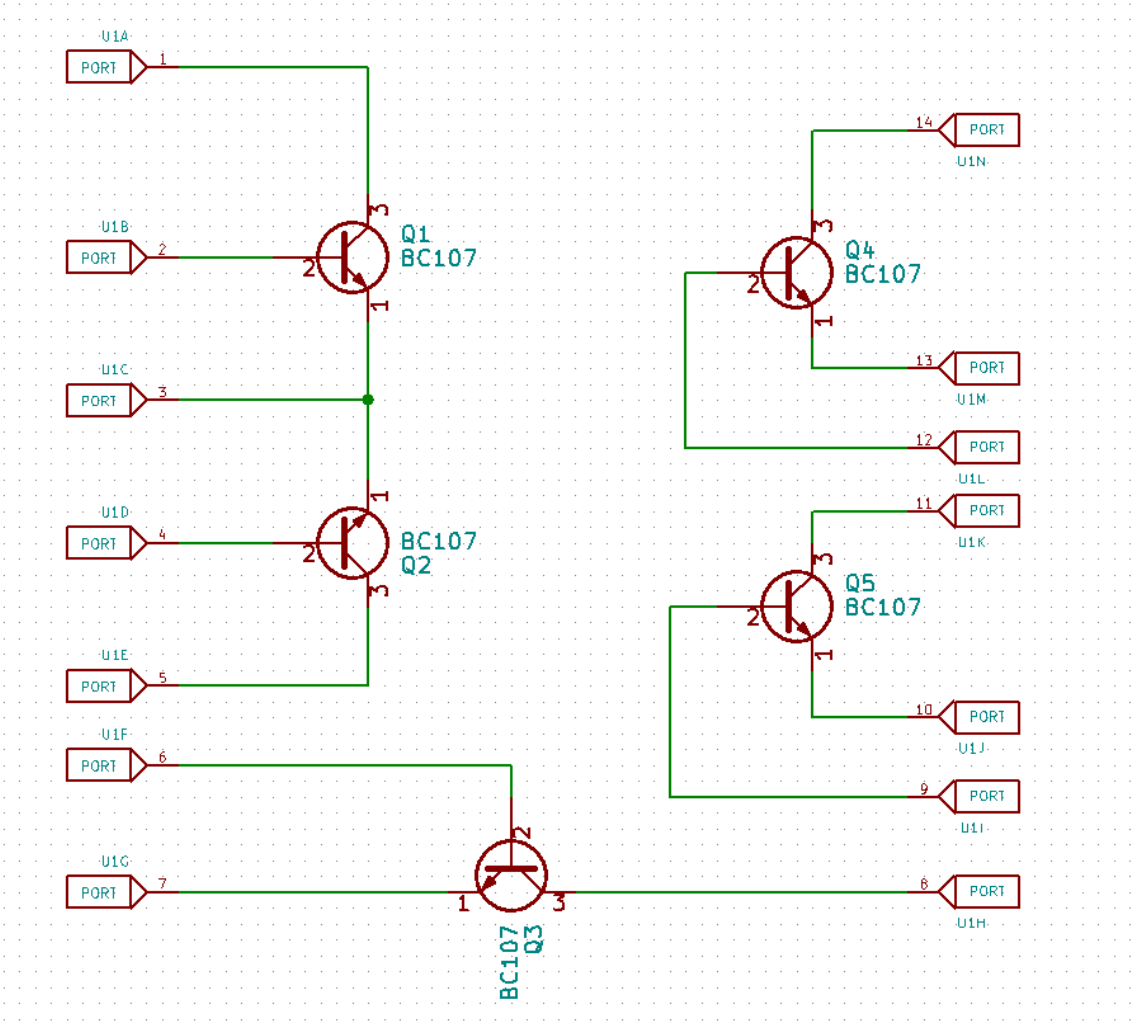

Figure 4.47: Subcircuit Schematic Layout of CA3045

4.10.5 IC Layout

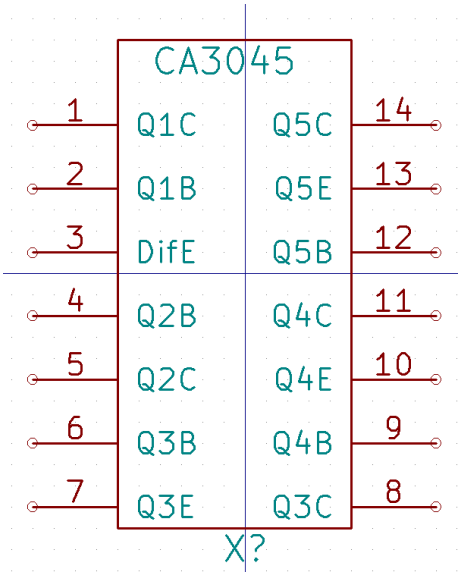

Figure 4.48: IC for CA3045

4.10.6 Test Circuit

This is the circuit made to verify and check the working of the implemented IC:

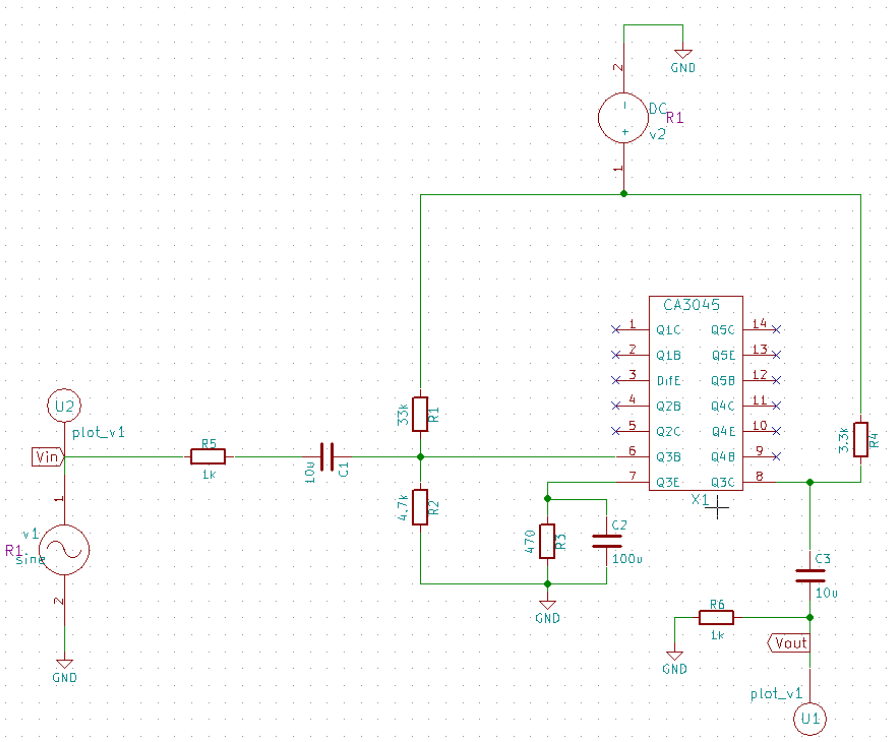

Figure 4.49: Test Circuit for CA3045

4.10.7 Output Waveforms

Here follows the waveform of the various inputs along with their corresponding outputs of the CA3045:

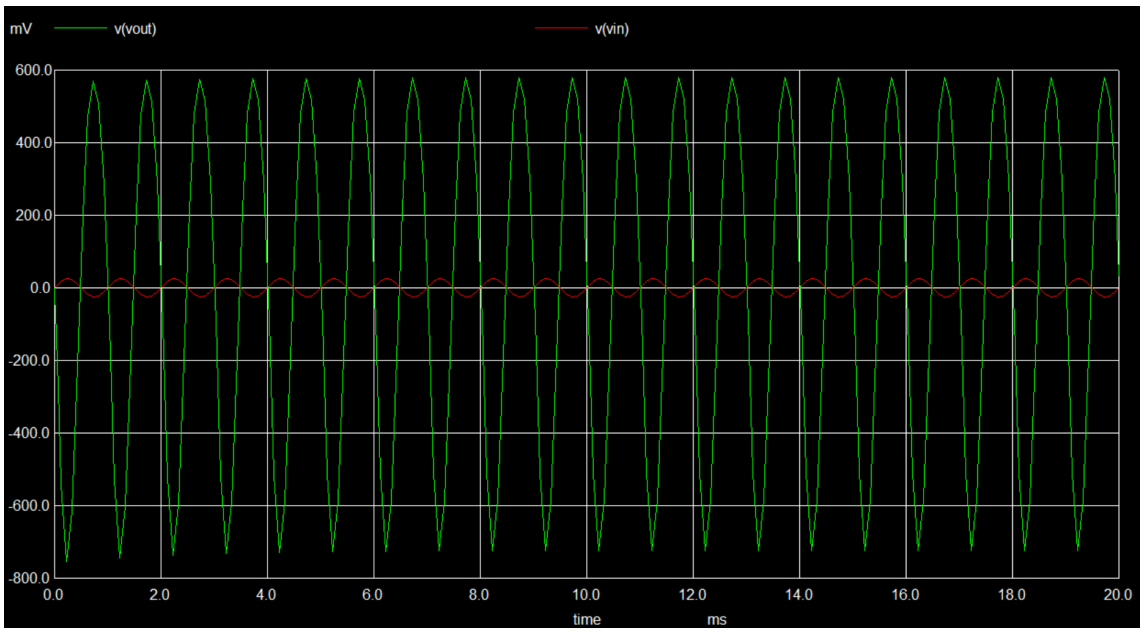

Figure 4.50: Output Waveforms of CA3045

Chapter 5

Failed IC

This section covers the IC that was unsuccessfully implemented.

5.1 NJM4151: Voltage to Frequency Converter/ Frequency to Voltage Converter

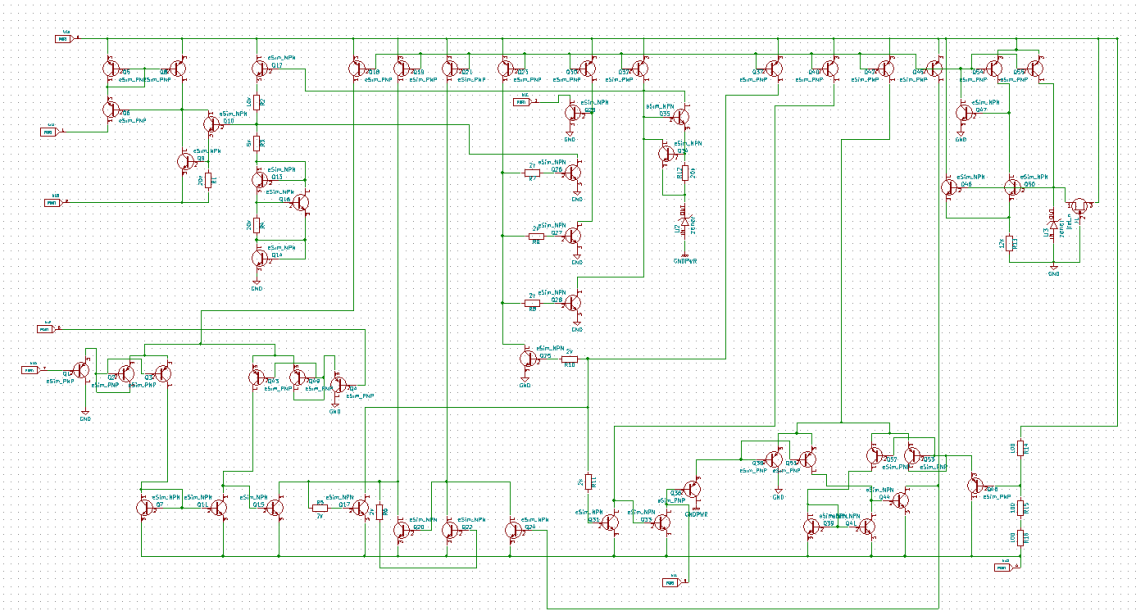

Figure 5.1: Schematic Layout of NJM4151

During testing of the NJM4151 IC, the expected output waveforms did not appear. Instead, distorted and unstable signals were observed, indicating possible issues in circuit configuration, component values, or simulation model limitations.
Further investigation and refinements are needed. Community feedback and suggestions are welcome to help improve the design and achieve clean, reliable outputs.

Chapter 6

Conclusion and Future Scope

The project was successfully completed with its purpose of designing and verifying a set of analog and mixed-signal IC subcircuits, modeled in exact detail from official datasheets. Every IC—be it a function generator or a multivibrator—was meticulously built with discrete components and validated with canonical circuits in the eSim platform. In spite of some setbacks like waveform distortion and less-than-perfect simulation behavior in some instances (like NJM4151), every setback proved the subtleties of real-world analog behavior and model constraints.

This activity not only deepened my knowledge of analog circuit design but also emphasized iterative testing, simulation precision, and physical limitations in open-source EDA tools. All tested IC models are now available to be added to the eSim subcircuit library, providing a useful resource for future designers and students designing analog and hybrid systems.

In the future, the models can be upgraded with higher transistor-level accuracy, further parameter tuning, and potentially Spice-compatible macromodels. The project opens the door to upgrading eSim's analog IC support and inspiring collaborative contributions toward the evolution of a solid, open-source collection of IC models for teaching and prototyping.

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