Summer Fellowship Report

On

Integrated Circuit Design using Subcircuit feature of eSim

Submitted by

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Acknowledgment

I would like to express my heartfelt gratitude to the **FOSSEE team at IIT Bombay** for giving me the opportunity to work on the design and integration of multiple sub-circuits using **eSim**, an open-source EDA tool. This internship has been an enriching experience that significantly enhanced my technical knowledge, practical skills, and understanding of circuit simulation using open-source platforms.

I am especially indebted to my mentor, **Mr. Sumanto Kar**, for his continuous support, expert guidance, and invaluable mentorship throughout the course of this project. His encouragement, attention to detail, and willingness to clarify complex technical concepts helped me navigate every challenge with confidence and precision. His role in shaping both the technical and professional aspects of this internship has been truly instrumental, and I am immensely thankful for his dedication and commitment.

I would also like to extend my sincere appreciation to **Prof. Kannan M. Moudgalya** for his visionary leadership and for fostering such impactful learning opportunities through the FOSSEE initiative. His efforts in promoting open-source tools for education and research have created a platform for aspiring engineers like me to learn, explore, and contribute meaningfully.

I am also thankful to **Varad Patil** for his timely assistance, insightful inputs, and collaborative spirit during the course of the project. His support played a valuable role in achieving project milestones efficiently.

This internship has been a significant milestone in my academic journey, deepening my passion for electronics and circuit design. The experience has not only broadened my technical perspective but also strengthened my confidence as an aspiring engineer. I look forward to applying the knowledge and skills gained during this internship in future academic and professional endeavors.

Contents

Chapter 1

Introduction

FOSSEE which stands for Free/Libre and Open Source Software for Education is an organization, based at IIT Bombay, as a remarkable initiative aimed at promoting the use of open-source software in education and research. It was established with the mission to reduce the dependency on proprietary software and to encourage the adop- tion of open-source alternatives. FOSSEE offers a wide range of tools and resources that cater to various academic and professional needs.

It provides comprehensive documentation, tutorials, workshops, and hands-on train- ing sessions, for empowering students, educators, and professionals to leverage open- source software for their projects and coursework. The organization's commitment to fostering a collaborative and inclusive environment has significantly contributed to the democratization of technology and has opened up new avenues for innovation and learning.

1.1 eSim

eSim, created by the FOSSEE project at IIT Bombay, is a versatile open-source soft- ware tool for circuit design and simulation. It combines various open-source software packages into one cohesive platform, making it easier to design, simulate, and ana- lyze electronic circuits. This tool is particularly useful for students, educators, and professionals who need an affordable and accessible alternative to proprietary software.

eSim offers features for schematic creation, circuit simulation, PCB design, and includes an extensive library of components. The Subcircuit feature is a significant enhancement, enabling users to design complex circuits by integrating simpler subcir- cuits. Through eSim, FOSSEE promotes the use of open-source solutions in engineer- ing education and professional fields, encouraging innovation and collaboration.

1.2 NgSpice

NgSpice is the open-source spice simulator for electric and electronic circuits. Such a circuit may comprise JFETs, bipolar and MOS transistors, passive elements like R, L, or C, diodes, transmission lines and other devices, all interconnected in a netlist.

Digital circuits are simulated as well, event-driven and fast, from single gates to complex circuits and the combination of both analog and digital as well as a mixed- signal circuits. NgSpice offers a wealth of device models for active, passive, analog, and digital elements. Model parameters are provided by our collections, by the semi- conductor device manufacturers, or from semiconductor foundries. The user adds her circuits as a netlist, and the output is one or more graphs of currents, voltages and other electrical quantities or is saved in a data file.

1.3 Makerchip

Makerchip is a platform that offers convenient and accessible access to various tools for digital circuit design. It provides both browser-based and desktop-based environments for coding, compiling, simulating, and debugging Verilog designs. Makerchip supports a combination of open-source tools and proprietary ones, ensuring a comprehensive range of capabilities.

One can simulate Verilog/SystemVerilog/Transaction-Level Verilog code in Makerchip. eSim is interfaced with Makerchip using a Python based application called Makerchip-App which launches the Makerchip IDE. Makerchip aims to make circuit design easy and enjoyable for users of all skill levels. The platform provides a user-friendly interface, intuitive workflows, and a range of helpful features that simplify the design process and enhance the overall user experience.

The main drawback of these open source tools is that they are not comprehensive. Some of them are capable of PCB design (e.g. KiCad) while some of them are capable of performing simulations (e.g. gEDA). To the best of our knowledge, there is no open source software that can perform circuit design, simulation and layout design together. eSim is capable of doing all of the above.

Chapter 2

Features Of

eSim

The objective behind the development of eSim is to provide an open source EDA solution for electronics and electrical engineers. The software should be capable of performing schematic creation, PCB design and circuit simulation (analog, digital and mixed-signal). It should provide facilities to create new models and components. Thus, eSim offers the following features -

1. Schematic Creation: eSim provides an easy-to-use graphical interface for drawing circuit schematics, making it accessible for users of all levels. Users can drag and drop components from the library onto the schematic, simplifying the design pro- cess. Comprehensive editing tools allow for easy modification of schematics, including moving, rotating, and labeling components.

2. Circuit Simulation: eSim supports SPICE (Simulation Program with Integrated Circuit Emphasis), a standard for simulating analog and digital circuits. Users can perform various types of analysis such as transient, AC, and DC, providing insights into circuit behavior over time and frequency.An integrated waveform viewer helps vi- sualize simulation results, aiding in the analysis and debugging of circuit designs.

3. PCB Design: The PCB layout editor allows users to place components and route traces with precision. eSim includes DRC capabilities to ensure that the PCB design adheres to manufacturing constraints and electrical rules. Users can generate Gerber files, which are standard for PCB fabrication, directly from their designs.

4. Subcircuit Feature: This feature enables users to create complex circuits by integrating smaller, simpler subcircuits, promoting modular and hierarchical design approaches. Subcircuits can be reused in different projects, saving time and effort in redesigning common circuit elements.

5. Open Source Integration: eSim integrates several open-source tools like KiCad, Ngspice, and GHDL, providing a comprehensive suite for electronic design automation. Being open-source, eSim is free to use, making advanced circuit design tools accessible without the need for expensive licenses.

Chapter 3

Problem Statement

To design and develop various Analog and Digital Integrated Circuit Models in the form of sub-circuits using device model files already present in the eSim library. These IC models should be useful in the future for circuit designing purposes by developers and users, once they get successfully integrated into the eSim subcircuit Library.

3.1 Approach

Our approach to implementing the problem statement began with examining datasheets from prominent Integrated Circuit (IC) manufacturers such as Texas Instruments, Analog Devices, and NXP Semiconductors. we selected ICs that offer a diverse range of functionalities, including precision amplifiers, comparators, encoders, and audio amplifiers. After building the subcircuits, we tested them to verify basic circuit configurations using NgSpice simulations. The step-by-step roadmap of this process is outlined below :

1. **Analyzing Datasheets :** The primary step is to browse through various analog and digital IC datasheets, and hence find suitable circuits to implement in eSim, that are not previously included into the eSim library. Check for the detailed schematic of the IC's and once the component values and the truth table is ascertained, then finalise the IC to be created.

2. **Subcircuit Creation :** After deciding the IC, we start modeling it as a subcircuit in eSim, using the model files present in the eSim device model library only. The design is strictly according to the information given in the official data-sheets of the ICs.This step also includes building the Symbol/Pin diagram of the IC according to the packaging and pin description given in the data-sheets only.

3. **Test Circuit Design :** Once the component of the IC is ready, now we can build the test circuits, according to the data-sheets. In this step we build the test cases and test circuits using the component IC.

4. **Schematic Testing :** Once the test circuits are ready, now it's time to simulate the test circuits so that the output can be obtained in the form of wave-forms and

plots. Here we take help of KiCad to NgSpice conversion and Simulation feature in eSim

If the output of the test circuit is not as per expectation, this implies that the test case has failed, and there is some error in the schematic. In such cases we go back to the design phase of the IC or the test circuits, to look for possible errors and then repeat the testing process again after making required changes.

Once the expected output of the test cases are correct and satisfy the expected results, then in such a case the IC is declared successfully working. The test case has been verified and the designing process is complete.

Chapter 4

4.1 MCT7800

The **MCT7800** is a fixed-voltage linear regulator IC designed to provide a **stable and reliable DC output voltage** from a higher input voltage source. It is commonly used for **local on-board regulation** in electronic circuits where consistent voltage is critical for performance.This IC is available in multiple fixed output voltage options, including **5V, 6V, 8V, 9V, 12V, 15V, 18V,** and **24V**, making it versatile for a wide range of applications. It can supply an output current of **over 1 ampere**, provided adequate heat dissipation is ensured.
The series integrates key protection features such as **internal current limiting**, **thermal shutdown**, and **safe-area compensation**, which safeguard both the regulator and the connected load from faults like **overheating** or **short circuits**. In addition to its robust protection, the series provides **excellent line and load regulation**, **low output noise**, and **high ripple rejection**, making it highly suitable for applications in **embedded systems**, **power supplies**, **instrumentation circuits**, and **consumer electronics**.

4.1.1 Pin Diagram

Below is the pin diagram of MCT7800 Voltage regulator that provides a stable regulated voltage. It is a 3-terminal IC consisting of Input ,Ground and Output terminal for regulated voltage.

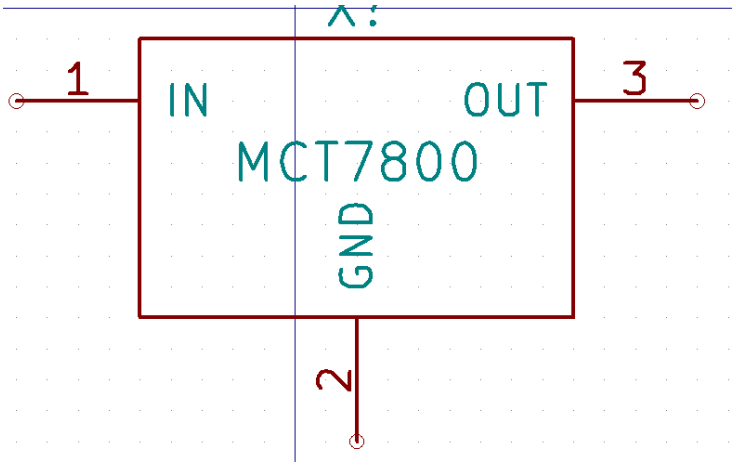

Figure 4.1.1.1: Pin configuration of the LM342 voltage regulator.

4.1.2 Sub Circuit Layout

The MCT7800 voltage regulator integrates 19 transistors with supporting resistors and capacitors to provide precise and stable voltage regulation. It uses a **bandgap reference**, **differential amplifier**, and a **series pass transistor** to maintain a constant output, even under varying load or input conditions. Built-in features like **current limiting**, **thermal shutdown**, and **safe-area protection** enhance reliability, especially in demanding environments. A small internal capacitor ensures stable operation without external compensation. This practical design allows the MCT7800 to be directly used in **power supplies, embedded systems, and consumer devices**, offering **plug-and-play voltage regulation** with minimal external components.

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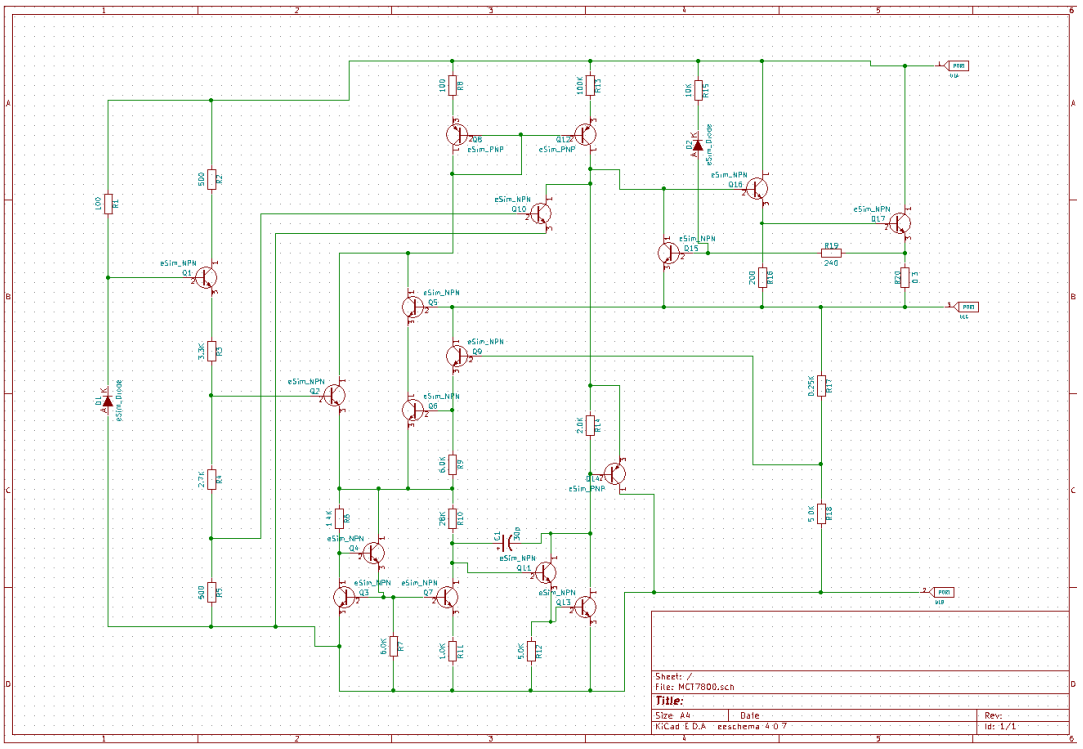

Figure 4.1.2.1: Subcircuit layout of the MCT7800 voltage regulator.

4.1.3 Test Circuit

This test setup for the **MCT7800 voltage regulator** is developed to observe and validate the regulator's electrical characteristics through simulation. Using the subcircuit model of the IC, the configuration allows for easy integration into circuit simulation tools to assess performance parameters like output stability, regulation accuracy, and fault response. Capacitors connected at the input and output help filter noise and stabilize the system, ensuring realistic testing conditions.

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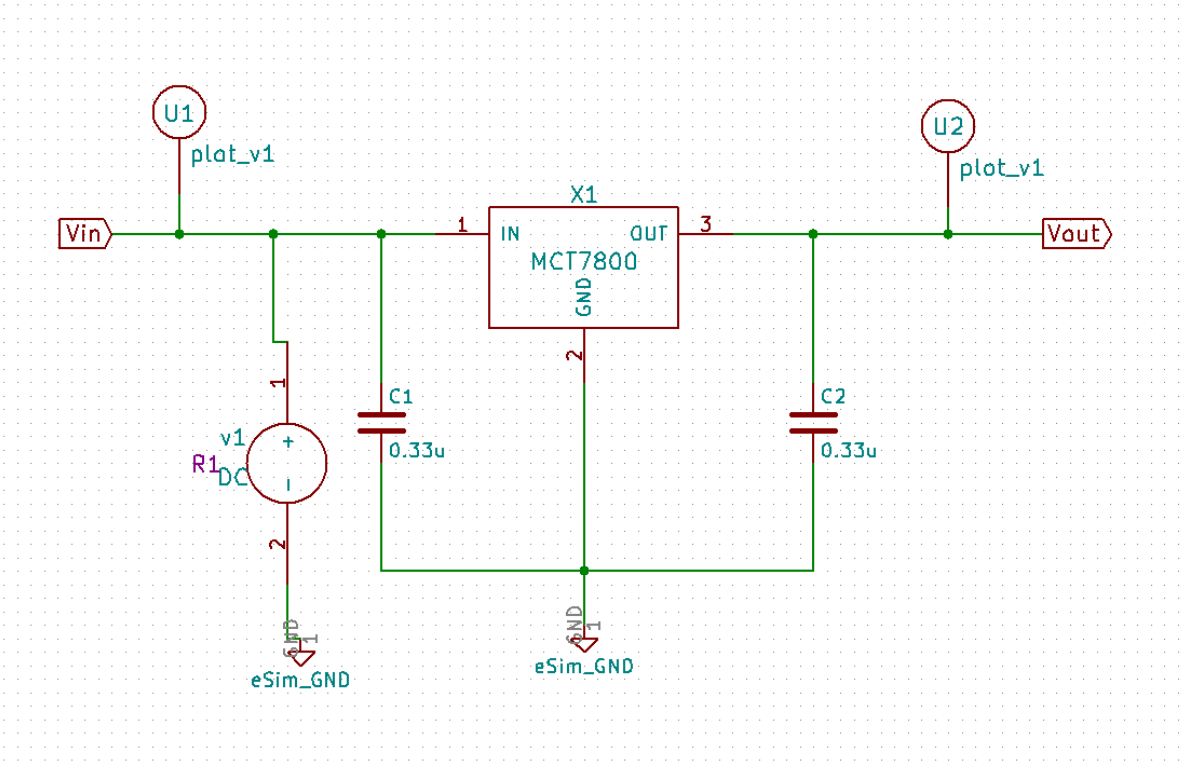

Figure 4.1.3.1: Test circuit setup for the MCT7800 voltage regulator.

4.1.4 Input Waveform

In this test circuit, the MCT7800 voltage regulator is applied with 50V DC input. This input voltage is regulated to obtain low regulated voltage. The use of a 50 V DC input lies within the designed input range, providing stable regulated output voltage for practical use.

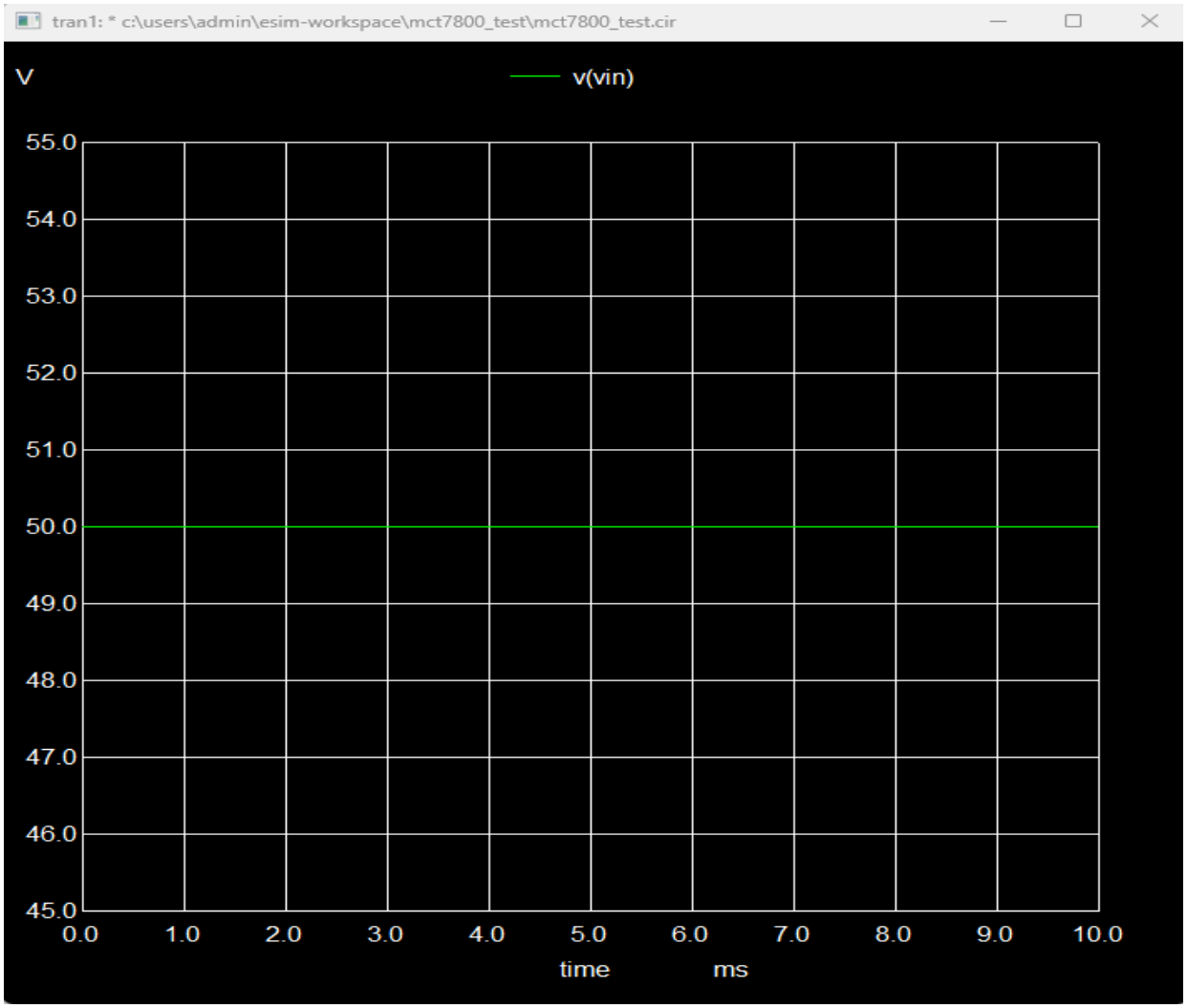

Figure 4.1.4.1: Input waveform for the MCT7800 voltage regulator.

4.1.5 Output Waveform

The MCT7800 voltage regulator delivers a regulated output voltage of approximately 5V. In the test circuit, we observe that MCT7800 is capable of providing a steady stable regulated output of 4.8V which is approximated to 5V. This regulated output is crucial for applications that require a stable 5 V power supply, ensuring reliable operation of connected electronic components.

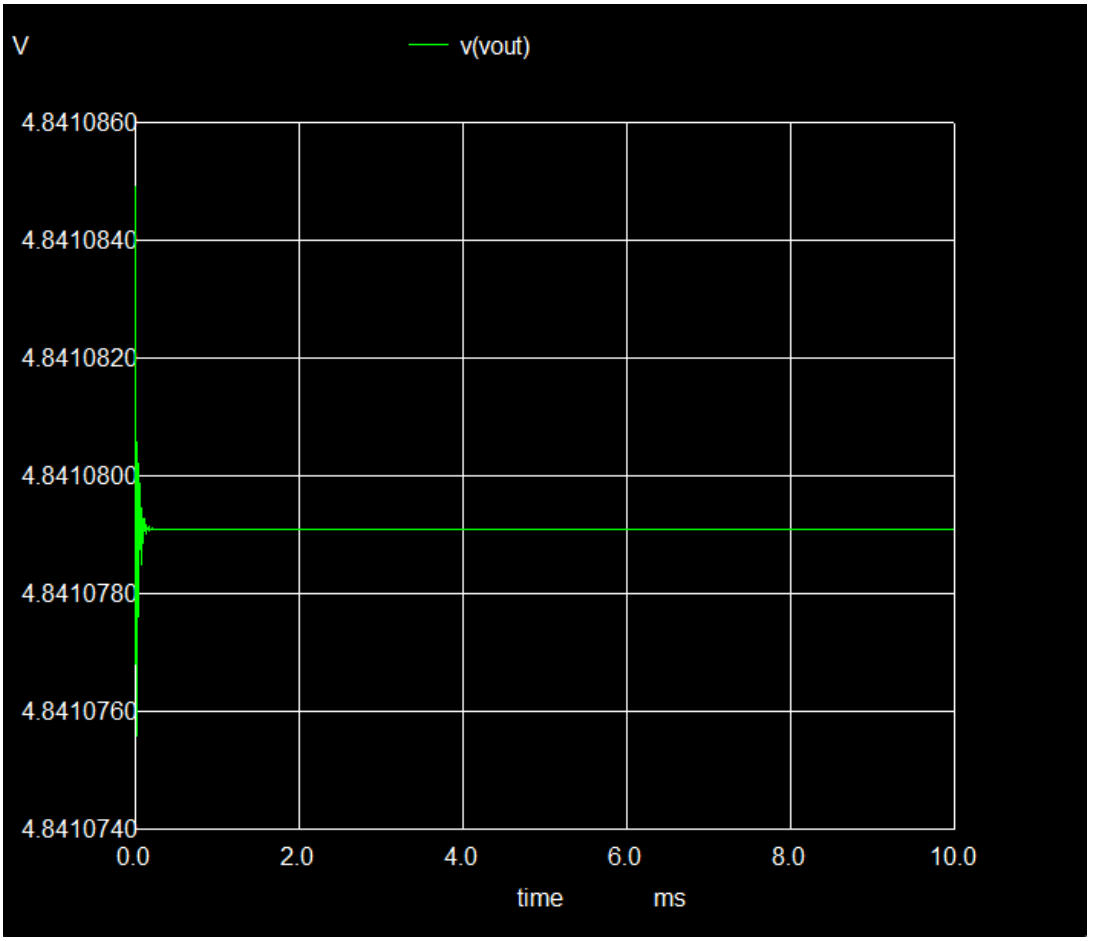

Figure 4.1.5.1: Output waveform of the MCT7800 voltage regulator.

4.2 MMC4011

The MMC4011 is a CMOS-based quad 2-input NAND gate IC, constructed using complementary p-channel and n-channel MOS transistors. It delivers reliable digital logic operation with high noise immunity, low static power consumption, and a wide operating voltage range from 3V to 15V. Each of the four independent gates in the package performs the NAND logic function, making it a fundamental component in digital logic design. Its compatibility with both TTL and CMOS logic levels makes it suitable for a variety of low-power applications.

Key features of the MMC4011 include a maximum input current of ±1 µA at 18V, a typical propagation delay of 60 ns at 10V, and an extremely low power dissipation per gate—typically in the nanowatt range. The IC supports symmetrical output drive (equal source and sink current capabilities), and the inputs are protected against static discharge. It comes in a standard 14-pin DIP package, with clearly defined pinouts for each NAND gate. Its wide supply voltage range, low power draw, and reliable logic operation make it ideal for use in timers, logic control units, signal inverters, and combinational logic circuits.

4.2.1 Pin Diagram

The MMC4011 is a quad 2-input NAND gate IC with 14 pins. It contains four independent NAND gates. Each gate has two inputs and one output. Pins 1–6 and 8–13 are used for inputs and outputs of the gates, while pin 14 is VDD (power supply) and pin 7 is VSS (ground). This IC is widely used in digital logic circuits for basic logic operations.

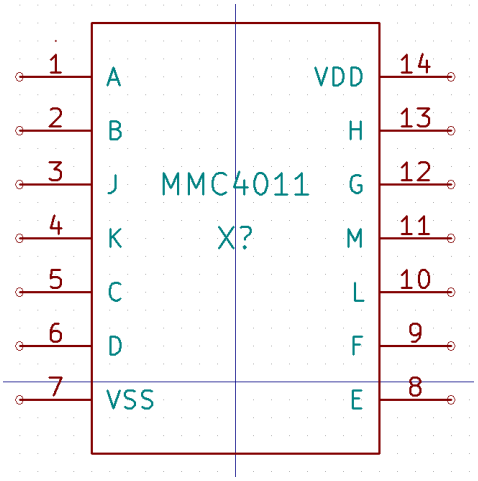

Figure 4.2.1.1: Pin Configuration of LM109

4.2.2 Sub Circuit Layout

(Fig-4.2.2.1) illustrates the single internal design of the MMC4011 and (Fig 4.2.2.2) Shows the entire sub circuit of MMC4011, Each gate uses a pull-up and pull-down network to perform the NAND function efficiently with low power consumption. The design includes input protection circuitry for ESD resistance and offers balanced switching characteristics suitable for digital logic applications

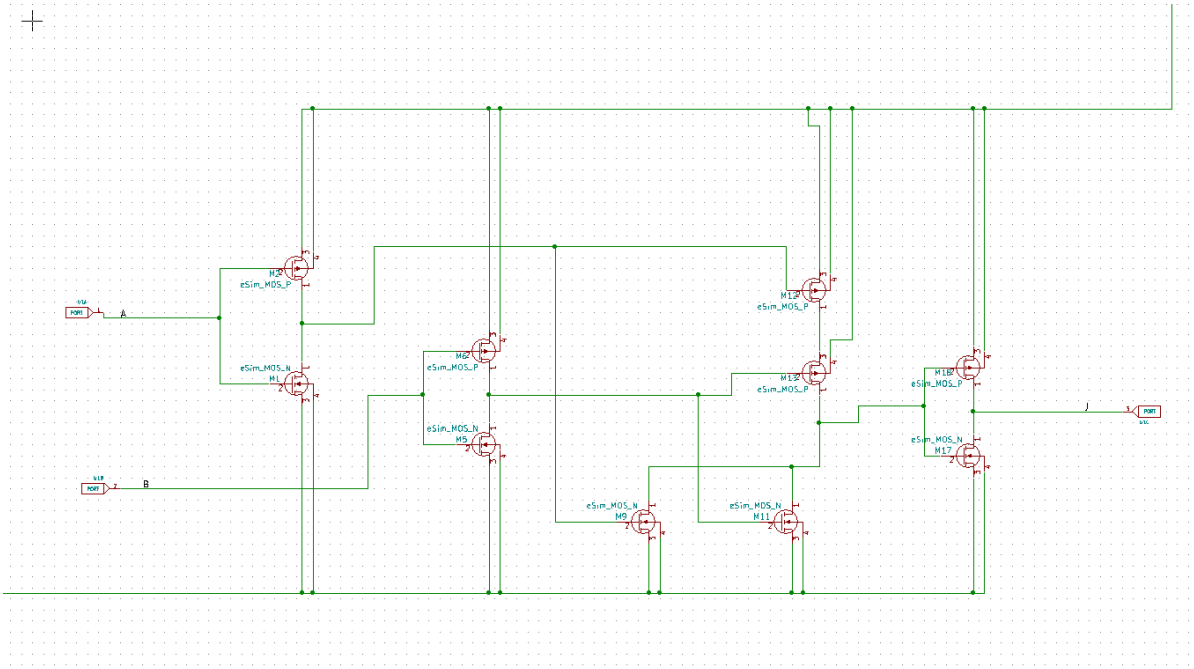

Figure 4.2.2.1: Subcircuit layout of single gate of MMC4011

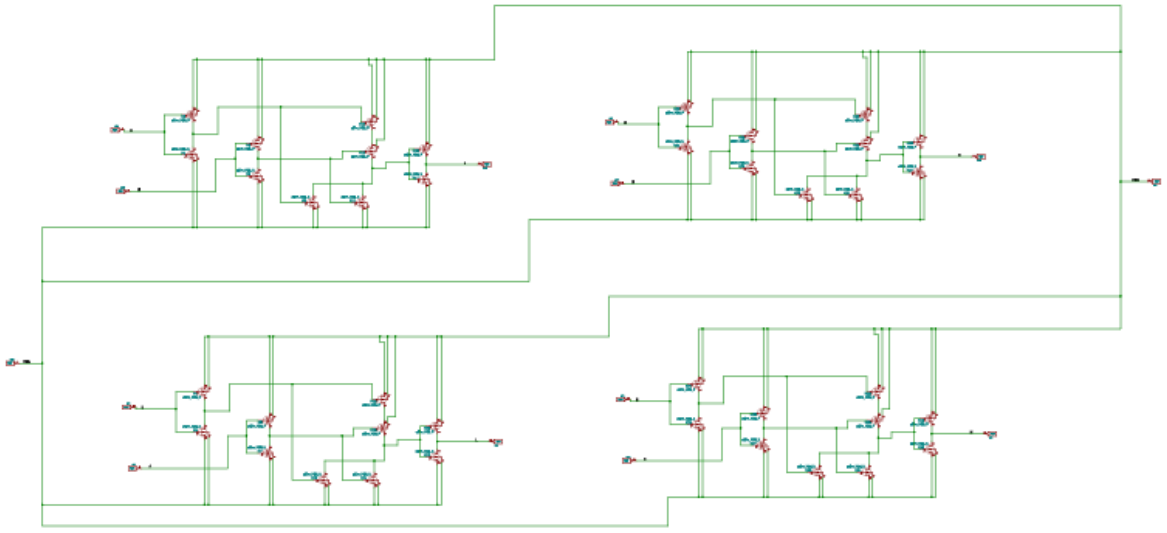

Figure 4.2.2.2: Subcircuit layout of MMC4011

4.2.3 Test Circuit

Provides a test circuit setup for evaluating the LM109's performance, showing the correct connection of input voltage, output load, and ground to verify stable operation under various conditions.

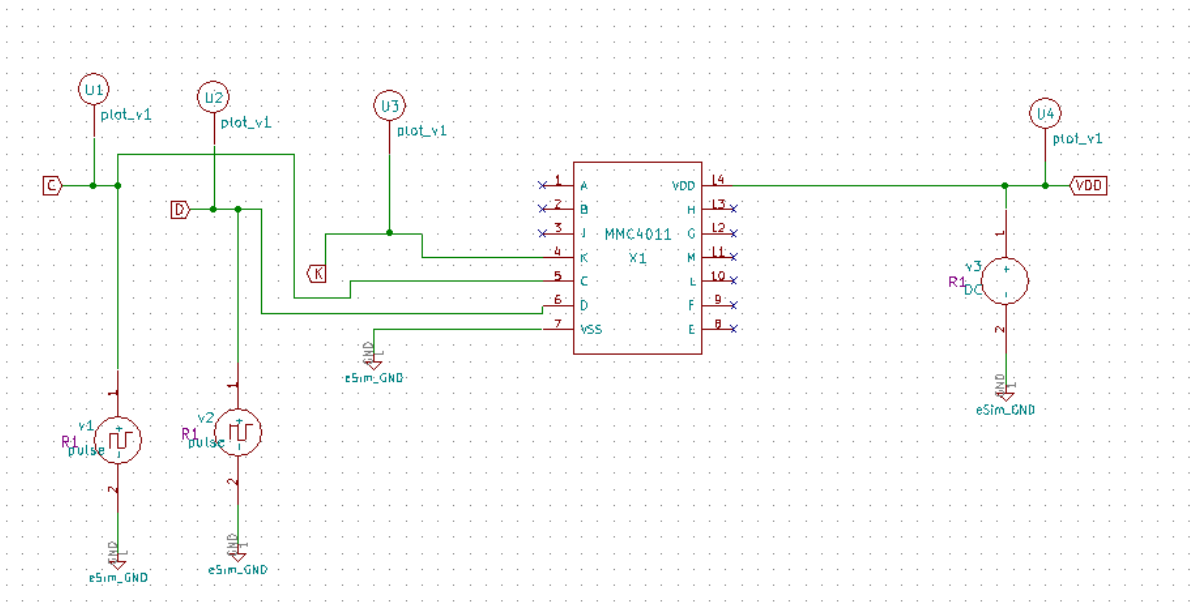

Figure 4.2.3.1: Test Circuit of the MMC4011

4.2.4 Waveform

The waveform shows the output response of the MMC4011 quad NAND gate IC for varying digital inputs. Signals v(c) and v|(d) represents input pulse trains, while the corresponding output v(k) toggles as expected for a NAND function—only going LOW when both inputs are HIGH. The logic transitions are clean, and timing alignment confirms proper NAND gate behavior under pulsed conditions with VDD held constant at 10 V

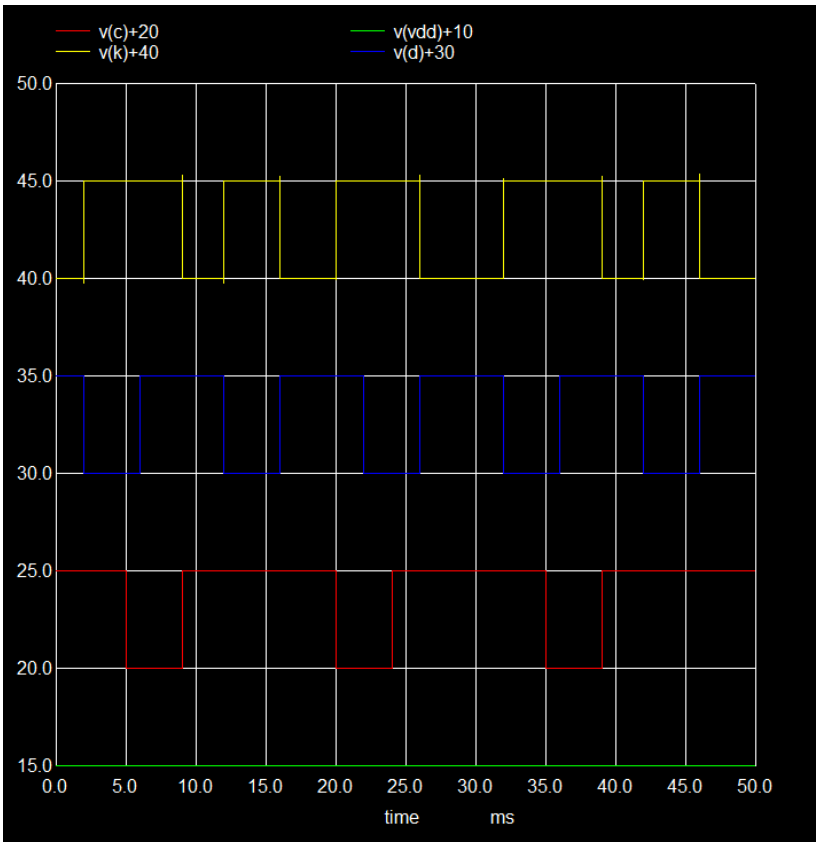

Figure 4.2.3.1: Test Circuit of the MMC4011

4.3 CD4085B

The CD4085B is a CMOS-based dual 4-input **AND-OR-INVERT (AOI)** gate IC. Each gate performs the logic function: $E1 = \overline{INH1 + A1B1 + C1D1}$, $E2 = \overline{INH2 + A2B2 + C2D2}$, meaning it combines two pairs of AND gates, feeds their outputs into an OR gate, and then inverts the final result. This compact logic configuration is widely used in arithmetic logic units, multiplexers, and control logic designs. The IC operates over a wide voltage range of 3V to 15V and offers high noise immunity and low static power consumption, making it suitable for both TTL-compatible systems and low-power applications.

Key features of the CD4085B include its symmetrical drive capability, high input impedance, and standard CMOS output levels. The device is available in multiple 14-pin package types such as DIP, SOIC, and TSSOP, supporting various design requirements. It offers robust performance across a wide temperature range (–55°C to 125°C) and includes input protection against electrostatic discharge. With its integrated AOI functionality, the CD4085B simplifies logic circuit design by reducing gate count and layout complexity in combinational digital systems.

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4.3.1 Pin Diagram

Shows the pin configuration of the CD4085B, indicating the four inputs [(A1,B1,C1,D1)/(A2,B2,C2,D2) and Active low inhibit pins (INHIB 1/INHIB2) and output is obtained at E1 for set (A1,B1,C1,D1) input and Inhibit pin1and at E2 for set (A2,B2,C2,D2) input and Inhibit pin2 respectively. Therefore correct connections must be made inorder to achieve correct output.

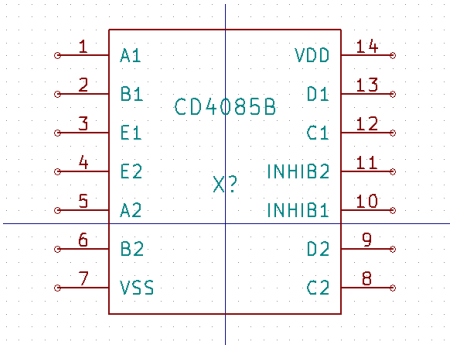

Figure 4.3.1.1: Pin Configuration of CD4085B

4.3.2 Sub Circuit Layout

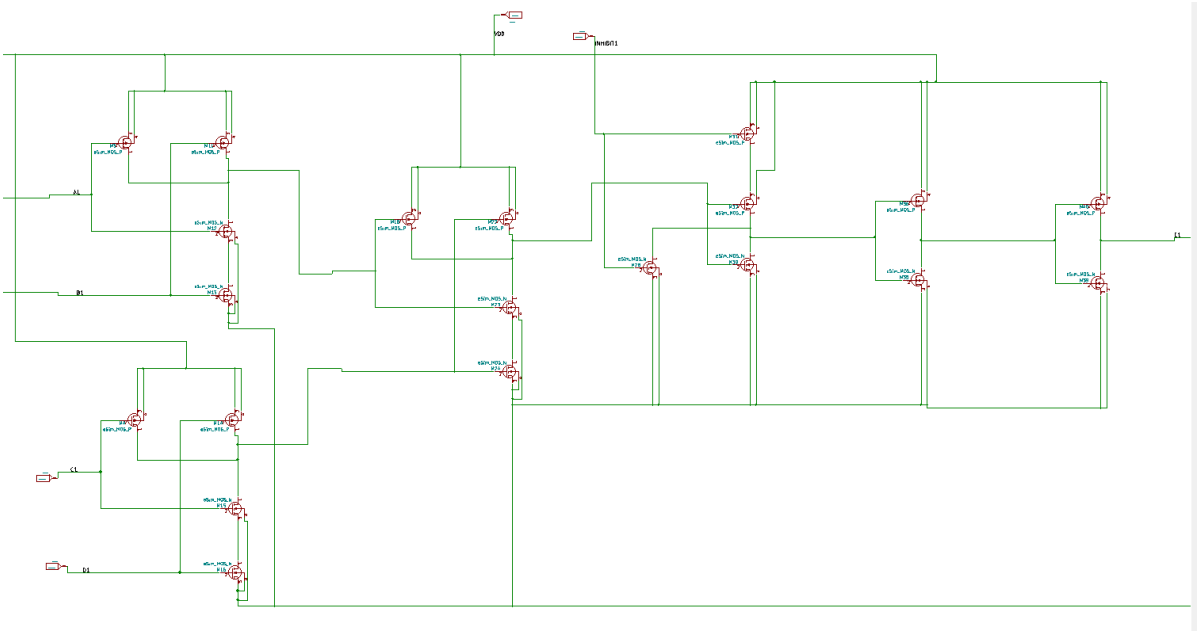

Figure 4.3.2.1: Single Subcircuit logic layout of the CD4085B

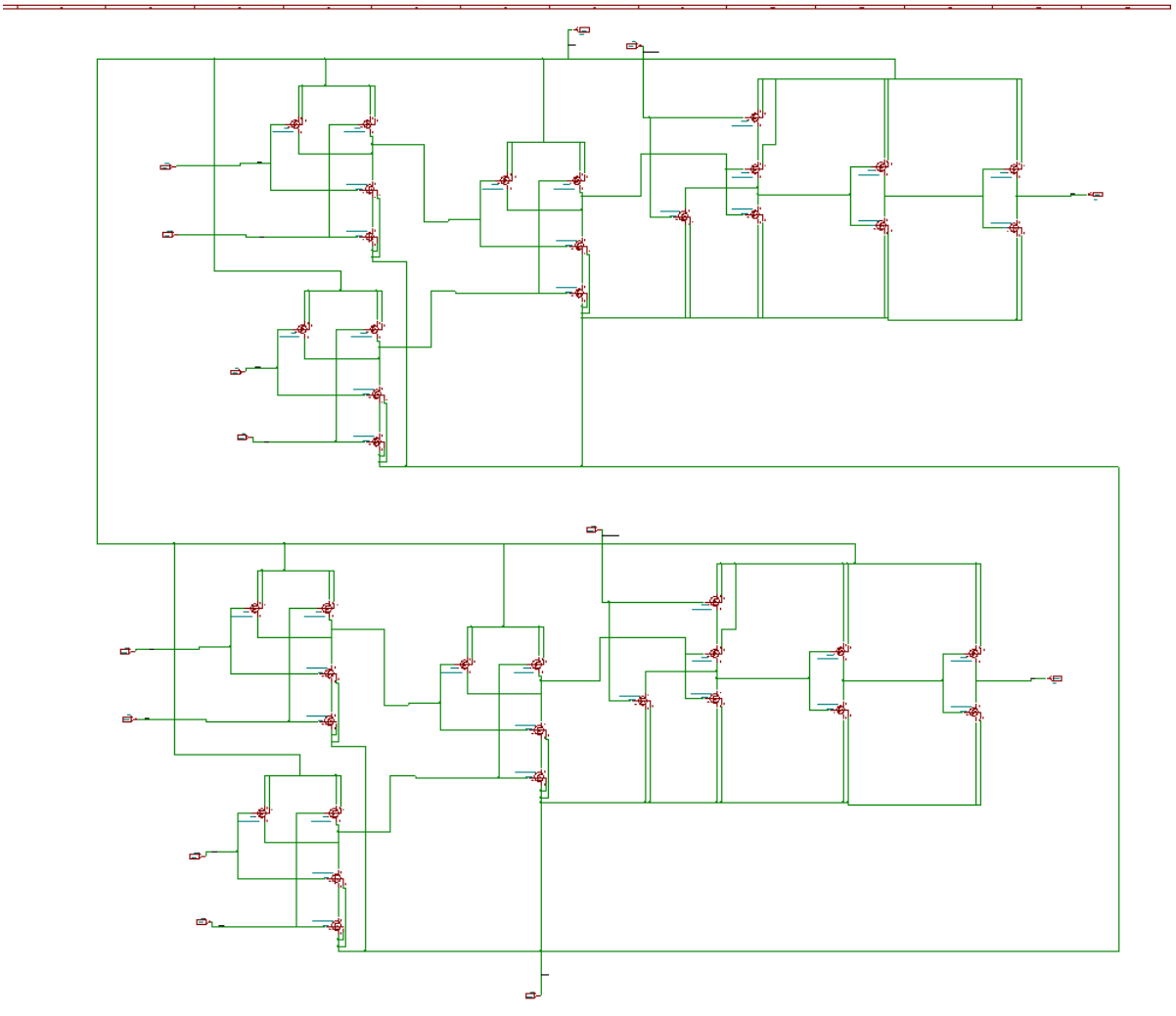

Figure 4.3.2.2: Subcircuit layout of CD4085B

The Subcircuit consists of two independent 4-input **AND-OR-INVERT** (AOI) gates, each formed by combining basic CMOS logic building blocks—AND, OR, and NOT gates—using complementary p-channel and n-channel MOSFETs. In each gate, two pairs of inputs are first processed by two separate 2-input AND gates. The outputs of these AND gates are then fed into a 2-input OR gate, and the result is inverted using a CMOS inverter to produce the final AOI logic output. This internal arrangement ensures reliable logic operation with low power consumption, high noise margin, and balanced output transitions, characteristic of CMOS technology.

4.3.3 Test Circuit

This circuit tests the **CD4085B** AOI gate with four pulse inputs and two active-low **inhibit controls** (Inhib1, Inhib2). The gate outputs follow the logic only when the corresponding inhibit input is LOW. When inhibit is HIGH, the output is disabled. Pulse sources and probes are used to observe the gate's logic response under different conditions.

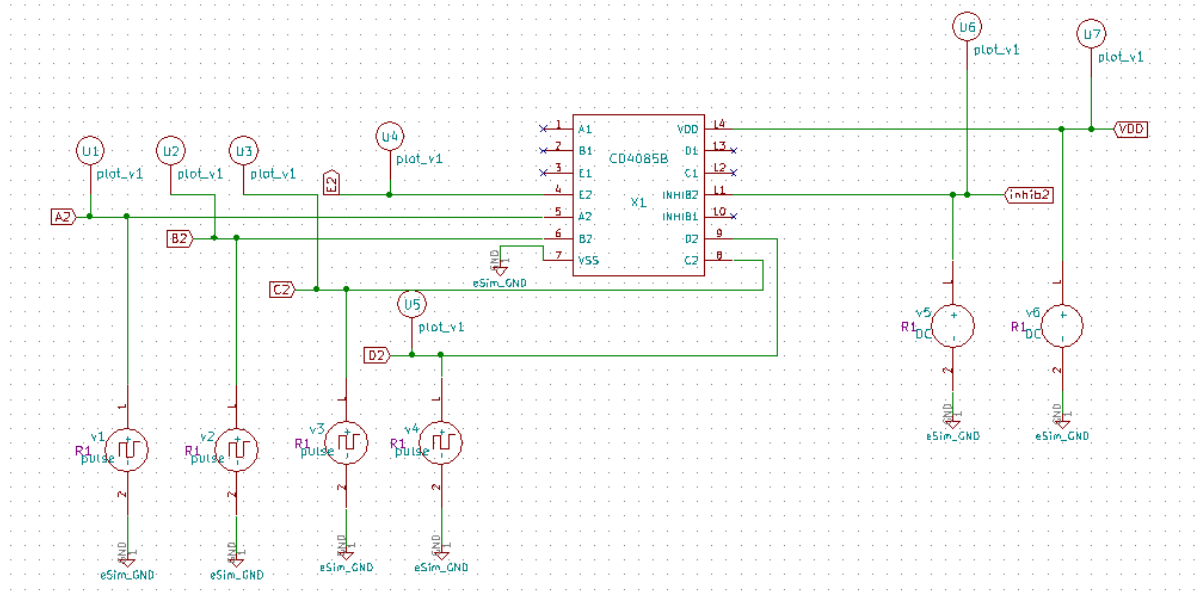

Figure 4.3.3.1: Test Circuit of CD4085B

4.3.4 Waveform

This waveform illustrates the behavior of the **CD4085B** AND-OR-INVERT gate with **active-low inhibit (inhib2)**. Inputs A2, B2, C2, and D2 are shown as distinct pulse signals, while **inhib2** remains LOW throughout, enabling normal gate operation.
The output **E2** (topmost trace) toggles LOW only when the condition (A2·B2)+(C2·D2) is HIGH, due to the inverting nature of the gate. When this logic expression is LOW, the output stays HIGH. The waveform confirms proper AOI functionality—E2 only dips LOW when the correct input combinations are satisfied and inhibit2 is active (LOW), validating the IC's logic under dynamic pulse conditions

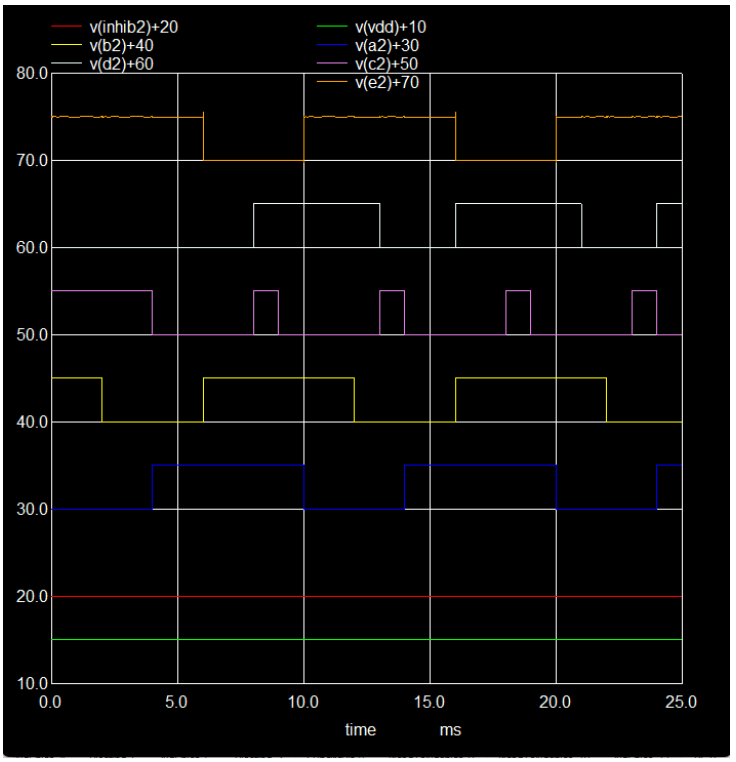

Figure 4.3.4.1: OUTPUT waveform of CD4085

4.4 ICL7611

The ICL7611 is a low-power, monolithic CMOS operational amplifier (op-amp) designed for precision analog signal processing tasks. Manufactured originally by Intersil , this IC is part of the ICL76xx family and is known for operating efficiently at very low supply currents—making it suitable for battery-powered or portable applications. The device operates with a single supply voltage as low as +3V (and up to +16V) or a dual supply of ±1.5V to ±8V, offering flexibility in low-voltage designs.

Key factor is its extremely low input bias current, low offset voltage, and high input impedance, making it suitable for sensor interfacing, instrumentation, and precision signal conditioning in applications such as medical equipment, handheld devices, and environmental monitoring systems. The op-amp provides a good balance of power efficiency and analog accuracy in compact packages like 8-pin DIP or SOIC.

4.4.1 Pin Diagram

This is the pin configuration of ICL7611. It shows the necessary pins as 2 balance inputs, IN+ and IN- as non-inverting and inverting inputs respectively, V+ and V- being the positive and negative power inputs respectively along with 1 output pin and Iq(quiescent current) setup. This ensures correct working of IC.

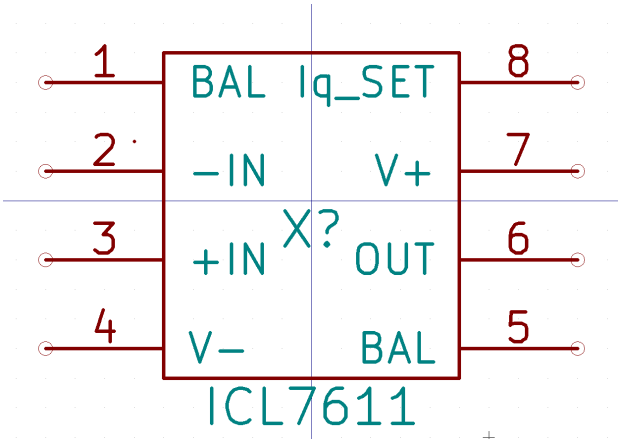

Figure 4.4.1.1: Pin Configuration of ICL7611

4.4.2 Sub Circuit Layout

The internal structure of the **ICL7611** illustrates that CMOS op-amp is based on a **low-power, high-impedance differential input stage**, followed by a **gain stage** and an **output buffer**. The input stage uses **MOSFET differential pairs**, which contribute to its ultra-low input bias current and high input impedance. This stage is optimized for precision and low leakage, making the device suitable for interfacing with high-impedance sensors. The second stage is a high-gain amplifier that boosts the differential signal, and the final stage is a **class AB output driver**, capable of rail-to-rail output swing. The op-amp also includes **biasing circuits**, **quiescent current control logic**, and **short-circuit protection circuits**. The internal biasing allows the user to program the current consumption using a control pin without external resistors, which is key to its ultra-low power operation

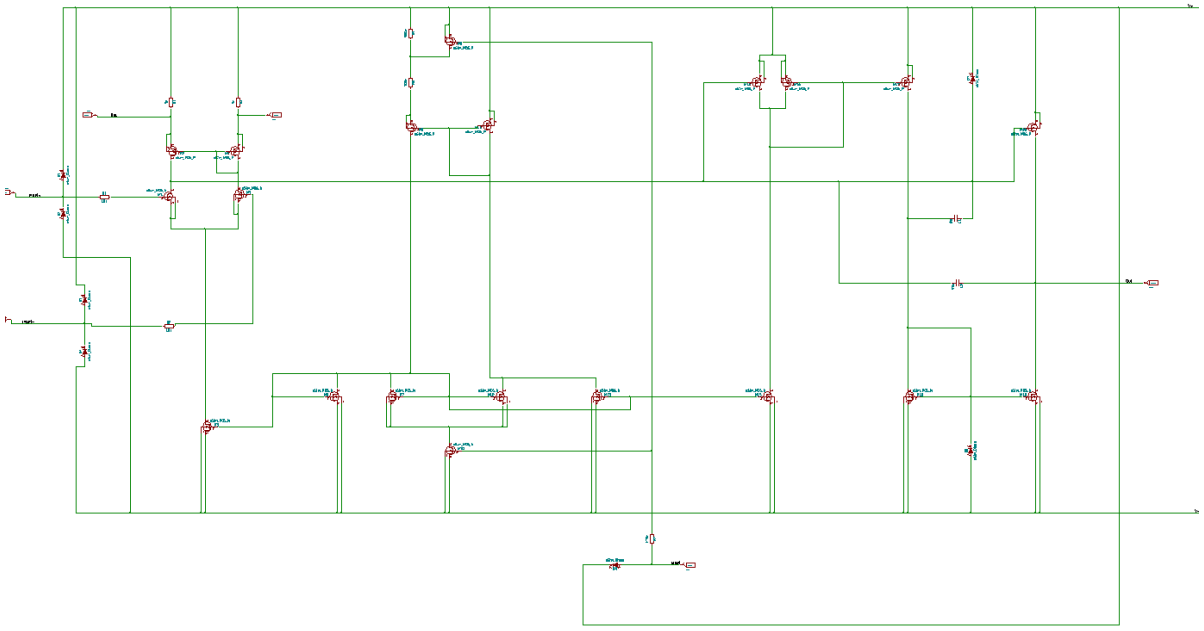

Figure 4.4.2.1: Subcircuit layout of the ICL7611

4.4.3 Test Circuit

The test circuit is an implementation of a voltage follower using the ICL7611 op-amp, where the **non-inverting input (IN+)** is applied with a sinusoidal signal and the **inverting input (IN–)** is connected to the output through a **10kΩ feedback resistor**. The op-amp is powered using **V+** as the positive supply and negative supply **V–** grounded, with both **balance pins left unconnected**. A **100kΩ load** is connected at the output, and the **quiescent current is internally set to 100µA**. The circuit provided accurate voltage tracking with low power consumption, suitable for high-impedance and low-power applications.

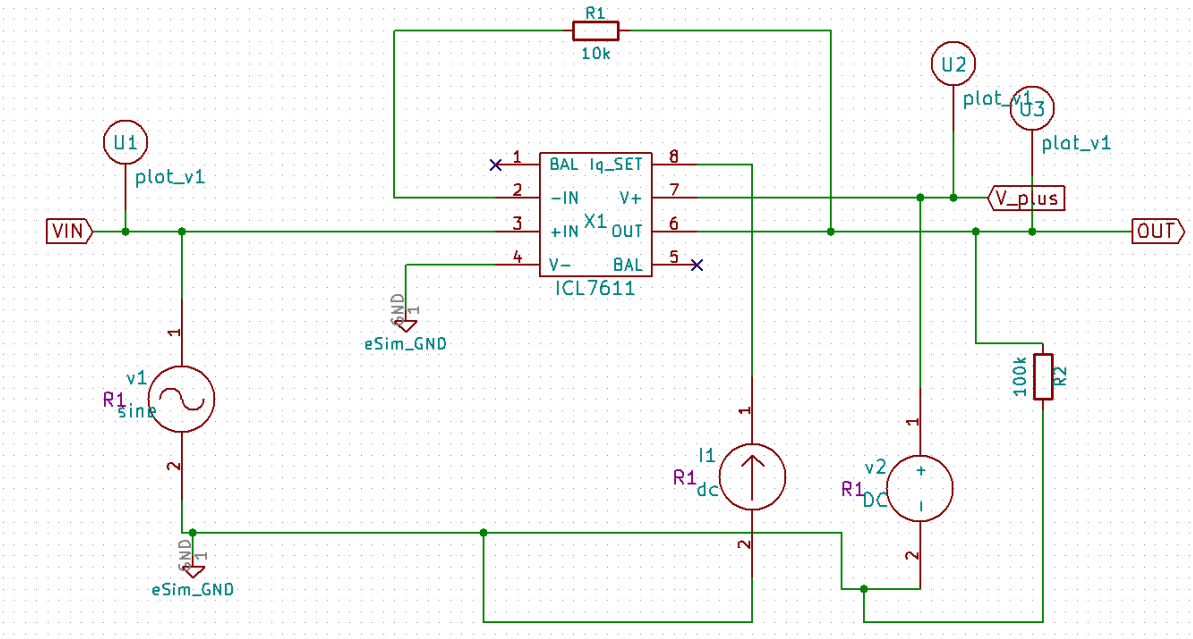

Figure 4.4.3.1: Test Circuit Layout of the ICL7611

4.4.4 Input Waveform

The input waveform depicts a **1kHz sinusoidal signal** with a **5V DC offset** and **5V amplitude**, resulting in a smooth waveform oscillating between **0V and 10V**. This ensures compatibility with single-supply operation and tests the op-amp's ability to handle full-range positive input signals.

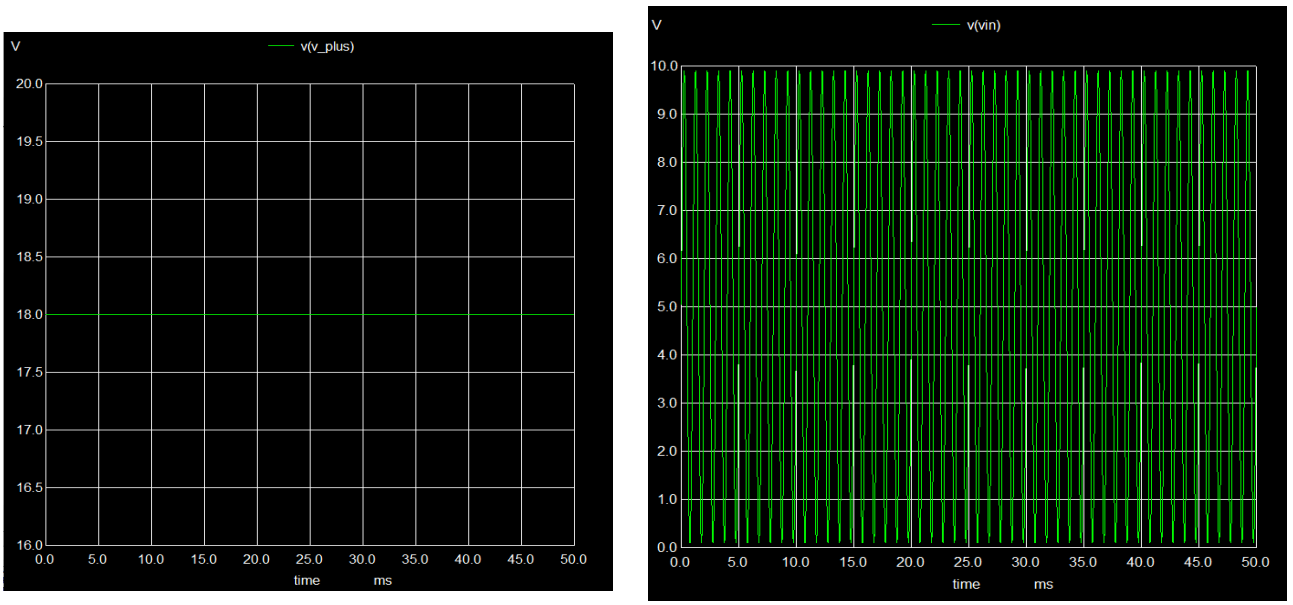

Figure 4.4.4.1: Input Wave form of 7611

4.4.5 Output Waveform

The output waveform depicts a sinusoidal signal closely following the input, with an approximate output swing of 4.9V, slightly less than the full 5V amplitude. This minor drop indicates the op-amp's near rail-to-rail performance, typical in low-power CMOS designs, and confirms effective voltage following within practical output limits.

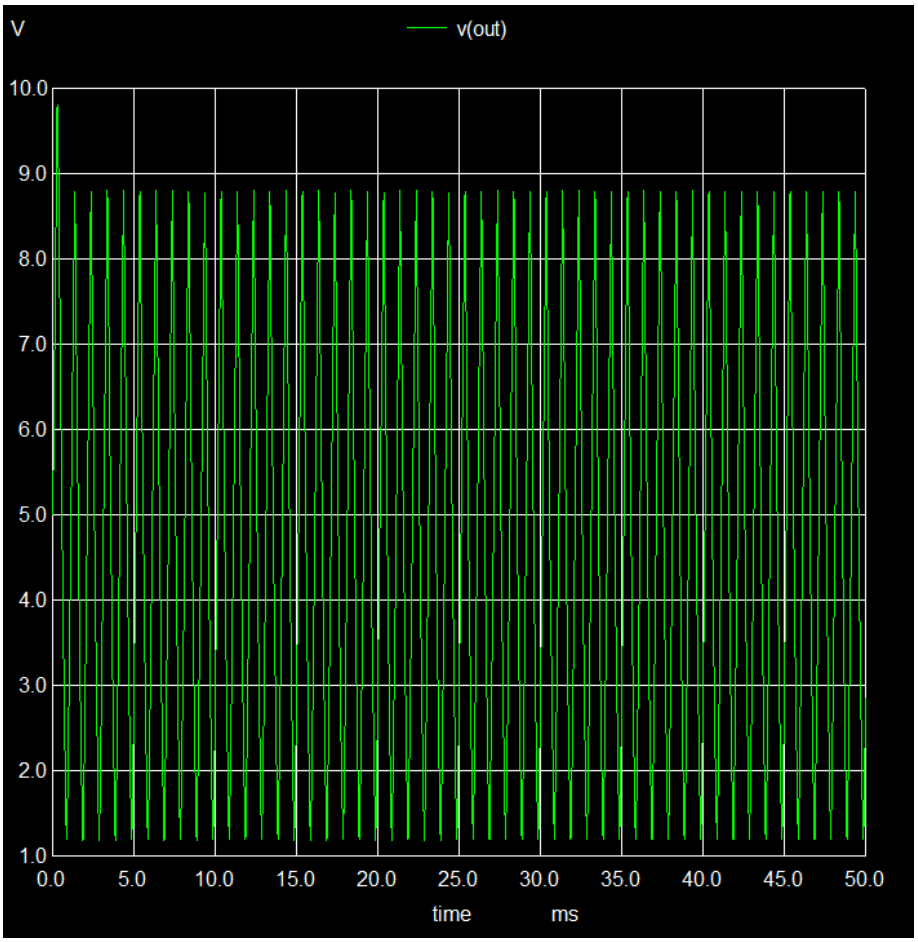

Figure 4.4.5.1: Output Wave form of ICL7611

4.5 CD74HC4050

The CD74HC4050 is a hex non-inverting buffer from the high-speed CMOS logic family, designed primarily for voltage level shifting and signal buffering applications. It features six independent buffer gates capable of accepting high-voltage input signals up to 15V, even when the device operates at a lower supply voltage like 3V or 5V. This makes it ideal for interfacing high-voltage CMOS or analog outputs with low-voltage digital systems such as microcontrollers or logic ICs. The IC operates over a wide supply range of 2V to 6V, and its CMOS design ensures low power consumption and high noise immunity. The device is commonly used in sensor interfacing, signal isolation, and protection of sensitive microcontroller inputs.

4.5.1 Pin Diagram

It is 16 package (pin1-VCC and pin 8 – GND and pin16 not connected). The rest is the input and output pins of 6 buffers of CD74HC4050.

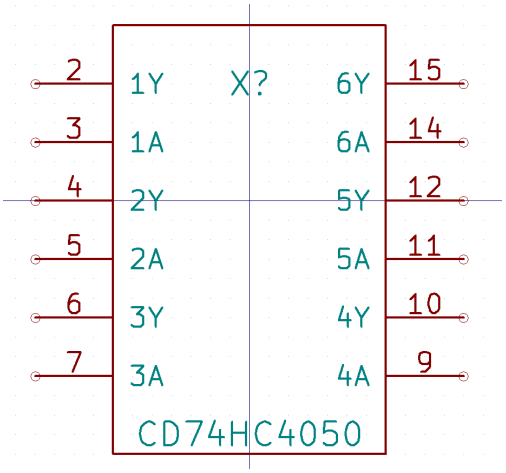

Figure 4.5.1.1: Pin configuration of CD74HC4050

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4.5.2 Sub Circuit Layout

The CD74HC4050 integrates six independent non-inverting buffer stages, implemented using advanced high-speed CMOS logic technology. Each buffer features a high input impedance and is equipped with integrated input protection circuitry, enabling it to reliably accept input voltages of up to 15V, regardless of the device's operating supply voltage (as low as 5V). This makes it particularly suitable for interfacing high-voltage signals with low-voltage digital systems in mixed-signal or level-shifting applications.

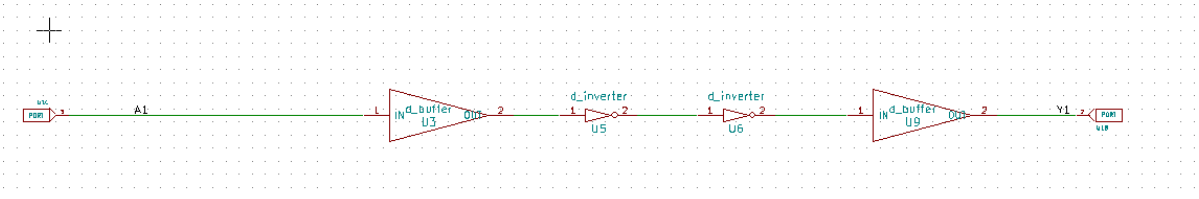

Figure 4.5.2.1: Single Buffer subcircuit of CD74HC4050

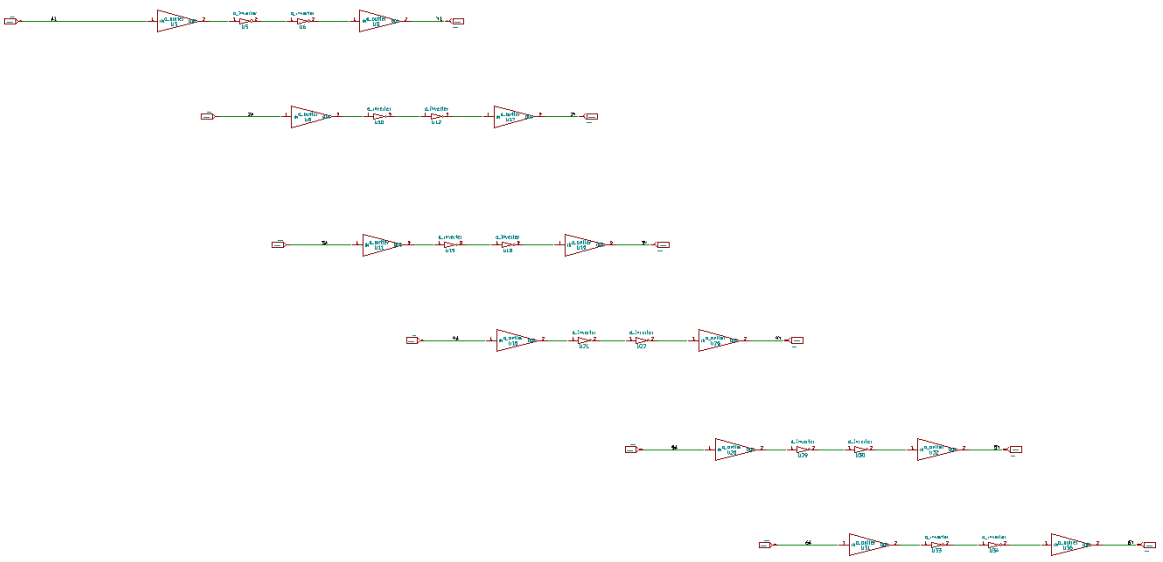

Figure 4.5.2.1: Subcircuit of CD74HC4050

4.5.3 Test Circuit

The test circuit is designed to verify the Output logic levels form 0V–5V, Hence it is designed such that the **15V input pulse** is applied to the input (2A) of the **CD74HC4050**, and a **10kΩ resistor** is connected at the output (2Y) as the load.

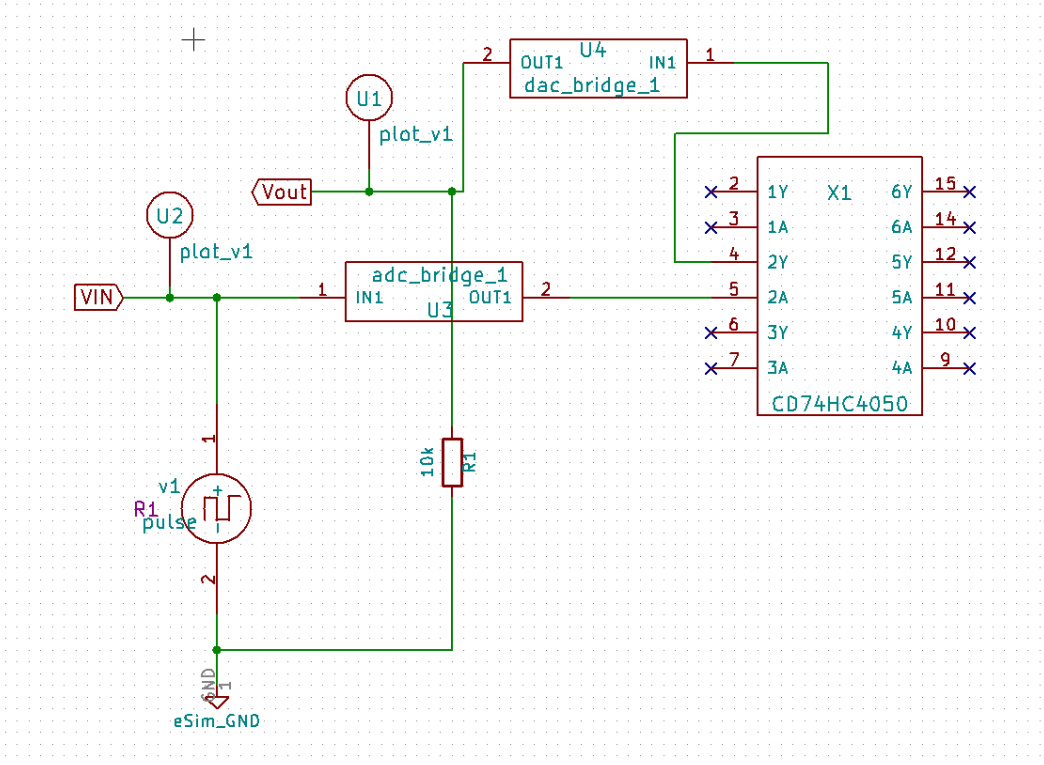

Figure 4.5.3.1: Test circuit setup for CD74HC4050.

4.5.4 Input and Output Waveform

The input and output waveforms are represented on a single plot to simultaneously verify the correct operation of the implemented IC. As observe (fig 4.5.4.1), the input (VIN) is a pulsed signal ranging from 0V - 15V, while the output (VOUT) switches cleanly between 0V- 5V. This confirms the proper level shifting and functional correctness of the CD74HC4050 buffer.

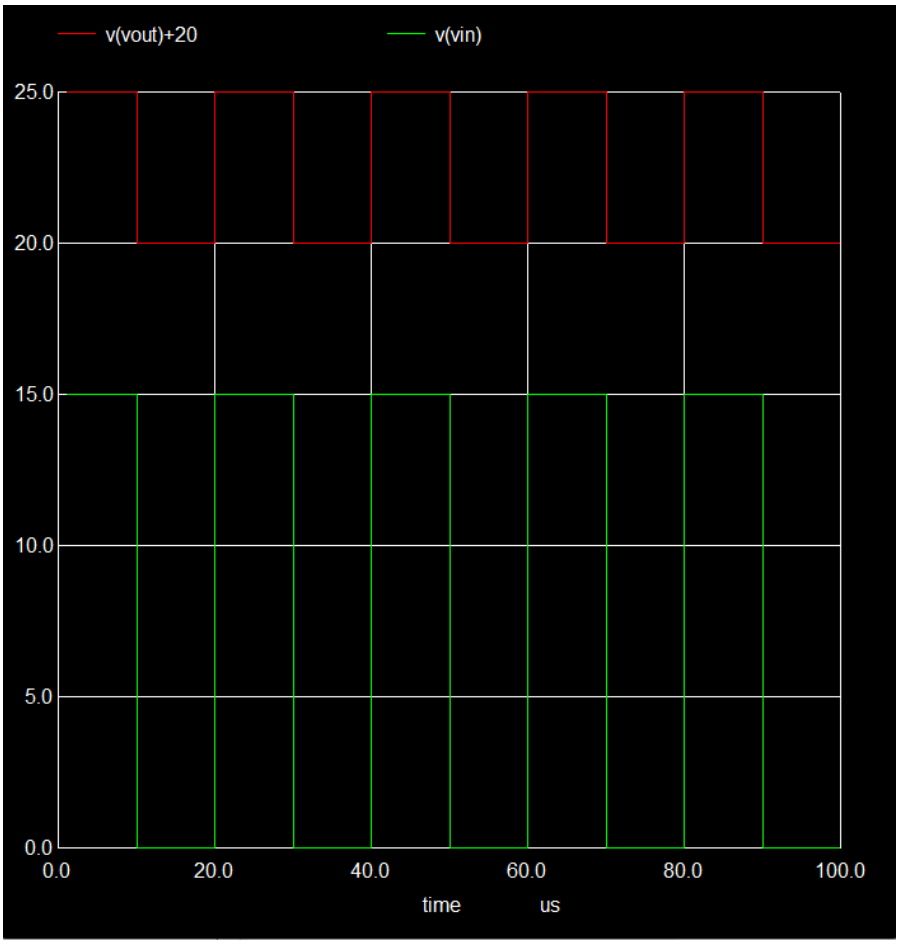

Figure 4.5.4.1: Input/output waveform of CD74HC4050.

4.6 MC1723

The **MC1723** is a versatile monolithic voltage regulator IC widely used for adjustable power supply applications. Originally developed by Motorola, it allows precise regulation over a wide output voltage range (2 V to 37 V) with the help of external resistors. The IC features excellent line and load regulation, internal current limiting, thermal shutdown, and the capability to drive external pass transistors for higher current requirements. It is commonly packaged in a 14-pin DIP and is electrically equivalent to the widely known LM723 regulator.

Internally, the MC1723 consists of a reference voltage generator, error amplifier, series pass transistor, and current limiting circuitry. Its architecture supports both series and shunt regulator configurations, making it suitable for custom power supplies, battery chargers, and industrial applications. Despite the rise of modern regulators, the MC1723 remains a valuable component in analog design education and legacy system maintenance due to its flexibility and reliability.

4.6.1 Pin Diagram

The MC1723 IC features essential pins for voltage regulation. Pin 2 (CURR_LIM) and Pin 3 (CURR_SENSE) are used for setting and sensing current limit. Pin 4 (INV_IN) and Pin 5 (NON_INV_IN) serve as the inputs to the error amplifier. Pin 6 (VREF) provides a stable 7 V reference, while Pin 7 is the ground (GND). Pin 9 (VZ) is used for startup or zener connection. Pin 10 (VO) gives the regulated output, and Pin 11 (VC) connects to the collector of an external pass transistor. Pin 12 (VCC) is the main supply input, and Pin 13(COMP) is used for frequency compensation.

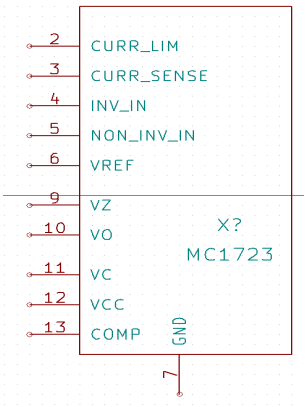

Figure 5.1.1.1: Pin Configuration of MC1723

4.6.2 Sub Circuit Layout

The internal structure of the MC1723 includes a precision voltage reference, an error amplifier, a series pass transistor, and current limiting circuitry. The voltage reference provides a stable 7.15 V output, which is compared by the error amplifier with a portion of the output voltage set by external resistors. The amplifier controls the pass transistor to regulate the output. Current limiting is achieved through a comparator and an external sense resistor. The IC also includes a compensation terminal for frequency stability and allows connection of an external pass transistor for higher current applications.

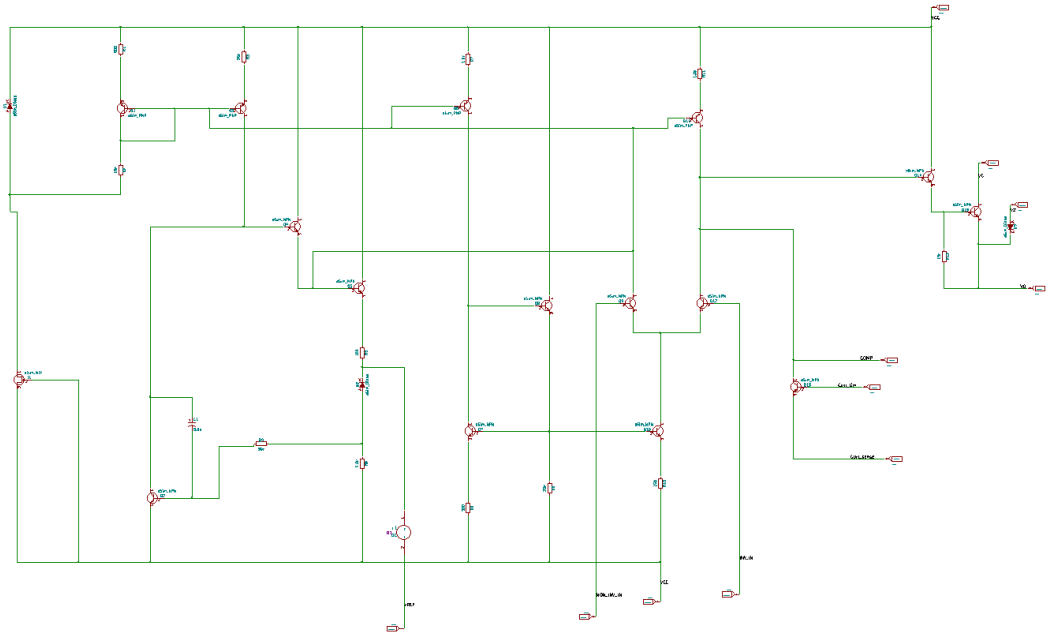

Figure 4.6.2.1: Subcircuit layout of the MC1723

4.6.3 Test Circuit

The test circuit demonstrates the MC1723 as an adjustable voltage regulator using an external pass transistor for higher current output. A resistor divider sets the output voltage by comparing it with the internal reference. Current limiting is implemented via a sense resistor between CURR_SENSE and CURR_LIM. Capacitors ensure stability and filtering, while the external transistor regulates VOUT based on the error amplifier's control, effectively showcasing the IC's voltage regulation and protection features

Recommended Testing Conditions

1) VIN = 9.5V - 40V
2) EXPECTED VOUT = 2V - 37V

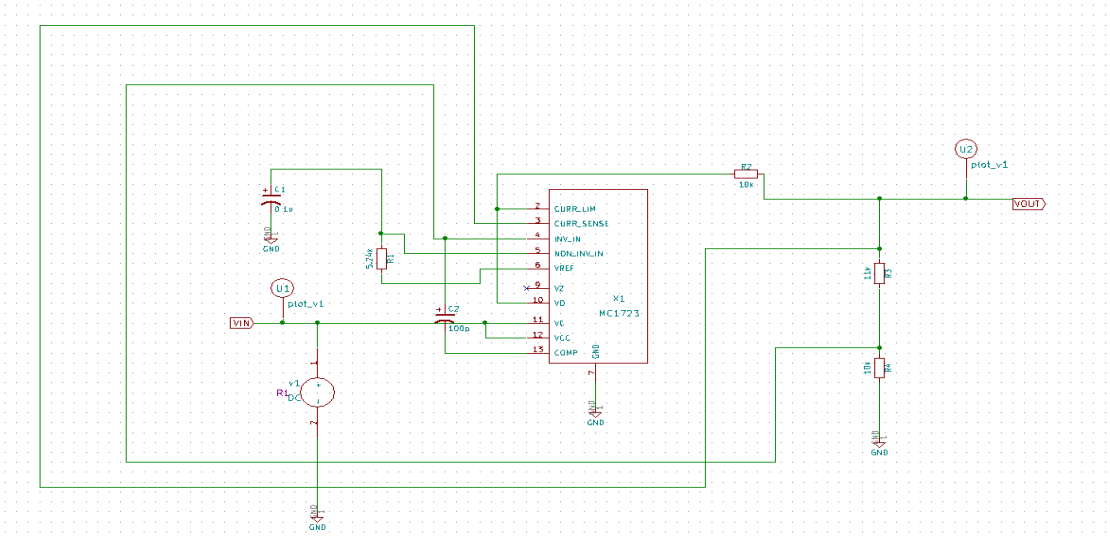

Figure 4.6.3.1: Test Circuit of MC1723

4.6.4 Input Waveform

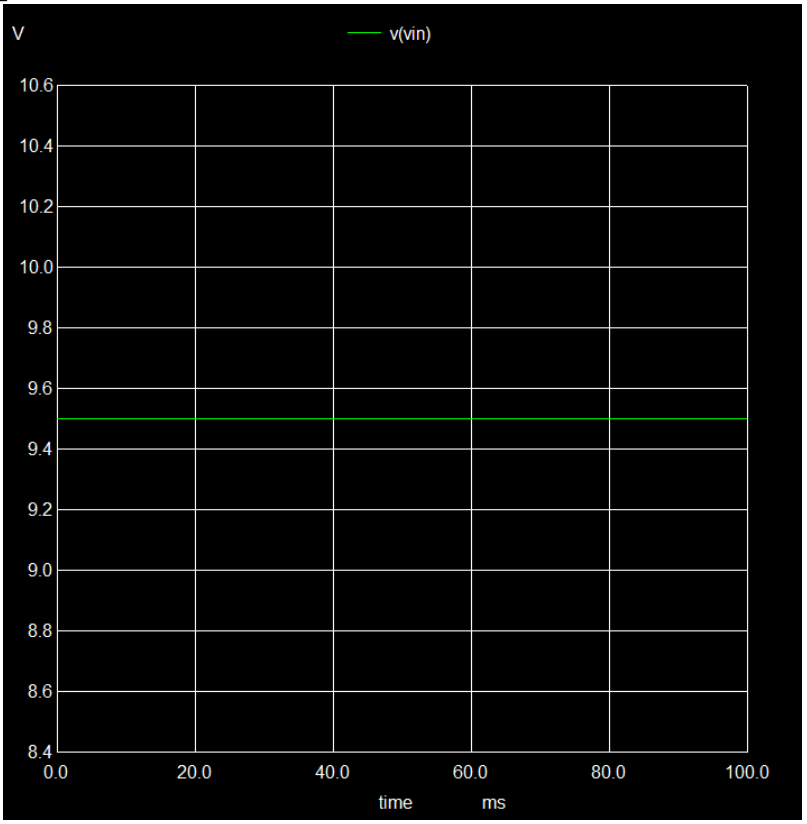

Figure 4.6.4.1 Input of MC1723 - Test 1)VIN=9.5V

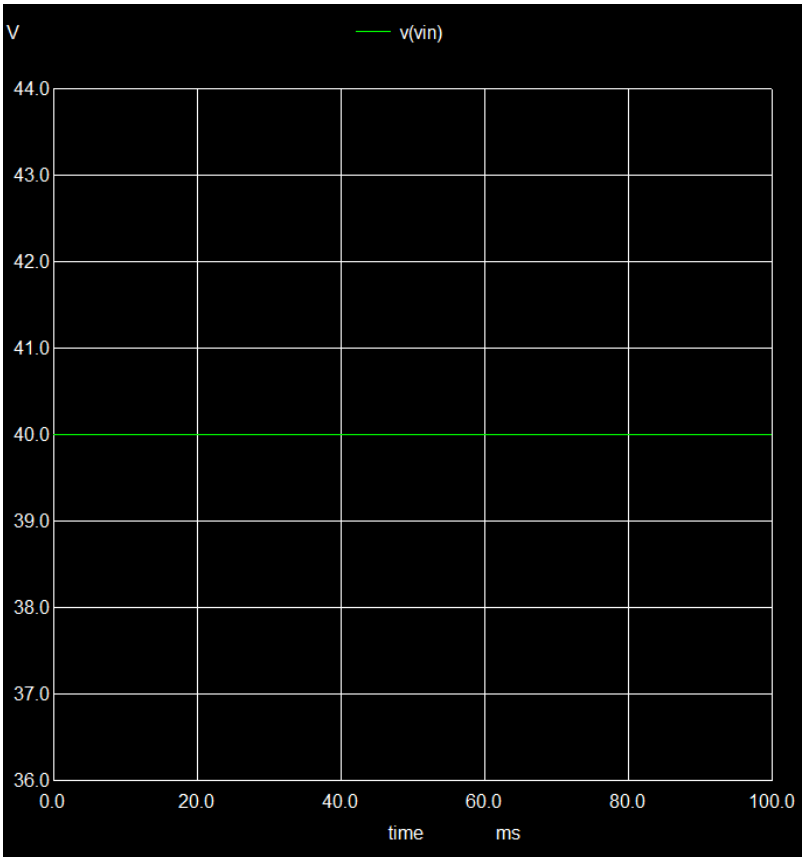

Figure 4.6.4.2 Input of MC1723 - Test 2)VIN=40V

The input waveform gives the information of applied two test cases to evaluate the MC1723 regulator circuit. In the first case,(Figure 4.5.4.1) **V1 = 9.5 V** is used as the DC input to observe the regulator's performance at a lower input voltage. In the second case (Figure 4.5.4.2) **V2 = 40 V** is applied at the collector of the external pass transistor to test the circuit's behavior under a higher input voltage and ensure proper voltage regulation.

4.6.5 Output Waveform

It is observed that output waveform form of first test (Figure 4.5.5.1) delivers the regulated output voltage 2.33V ,similarly Output waveform of second test (Figure 4.5.5.2) delivers a regulated voltage of 36.20V. Therefore it indicates that the output for voltage lies between the expected range of 2V to 37V.

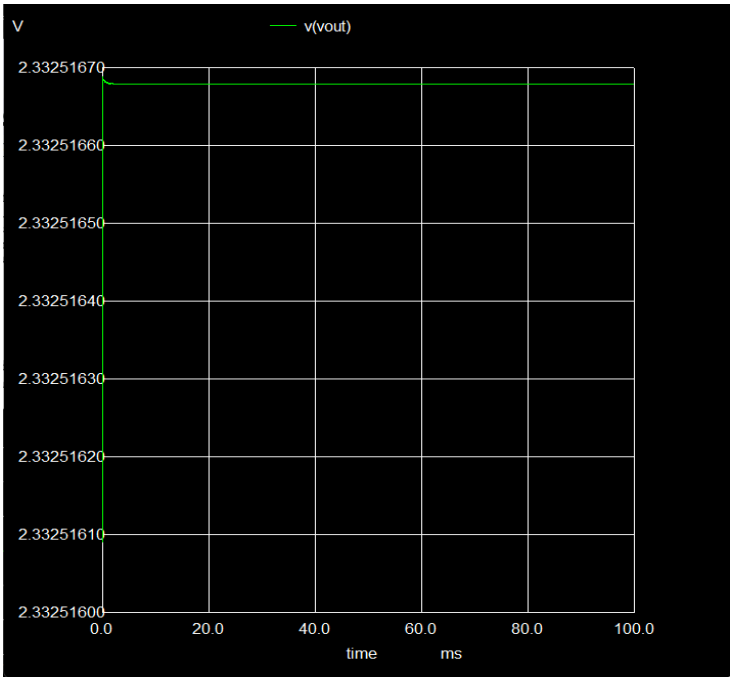

Figure 4.6.5.1: output of MC1723 - Test 1

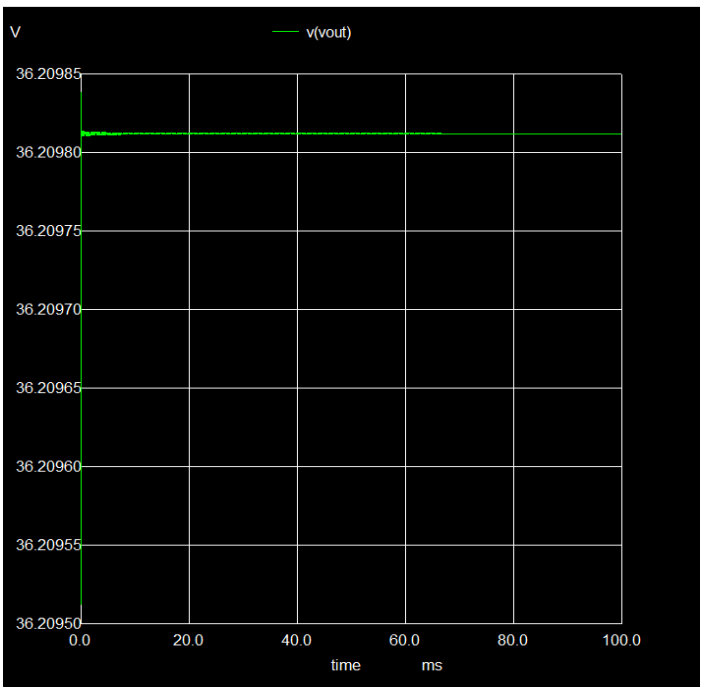

Figure 4.6.5.2: output of MC1723 - Test 2

4.7 CD4017B

The **CD4017B** is a CMOS decade counter/divider IC that plays a key role in sequential logic and timing applications. It is designed with a 5-stage Johnson counter and ten fully decoded outputs, each advancing sequentially with the input clock signal. Commonly used in circuits requiring LED sequencing, frequency division, or event counting, this IC simplifies design by offering built-in decoded outputs and a carry-out feature for cascading. It is fabricated using high-speed CMOS technology and operates over a wide voltage range of 3V to 15V, making it versatile for both TTL and CMOS logic systems. The CD4017B is available in various packages, including PDIP, SOIC, and TSSOP, ensuring compatibility with different design requirements.

4.7.1 Pin Diagram

The **CD4017B** is a 16-pin IC where pins **Q0 to Q9** are the **10 decoded outputs**, activated one at a time on each rising clock edge. **Pin 14 (Clock)** receives the input pulse to advance the counter. **Pin 13 (Clock Inhibit)** is an active-high control input that disables counting when high. **Pin 15 (Reset)** clears the count and resets the output to Q0 when held high. **Pin 12 (Carry Out)** gives a divided-by-10 signal, useful for cascading counters

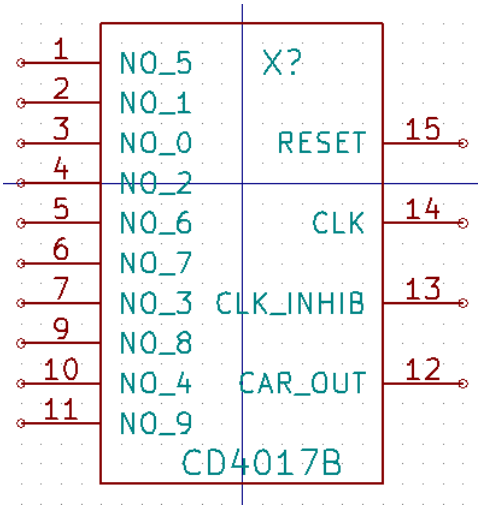

Figure 4.7.1.1: Pin Configuration of CD4017B

4.7.2 Sub Circuit Layout

The given subcircuit represents the internal architecture of the CD4017B decade counter IC, showcasing its sequential logic design. At the core, the circuit employs five D-type flip-flops connected in a Johnson counter configuration, where the output of one stage feeds into the next, enabling a 10-step counting sequence. Logic gates such as AND, OR, and inverters are used to decode the counter states and produce the 10 distinct output pulses (Q0 to Q9), with only one output active high at any time. The schematic also includes inverters for signal conditioning, a reset path to bring the count back to Q0, and logic to support clock enable and carry-out functionalities. This configuration allows the IC to function as a divide-by-10 counter and to cascade with additional counters for extended counting operations..

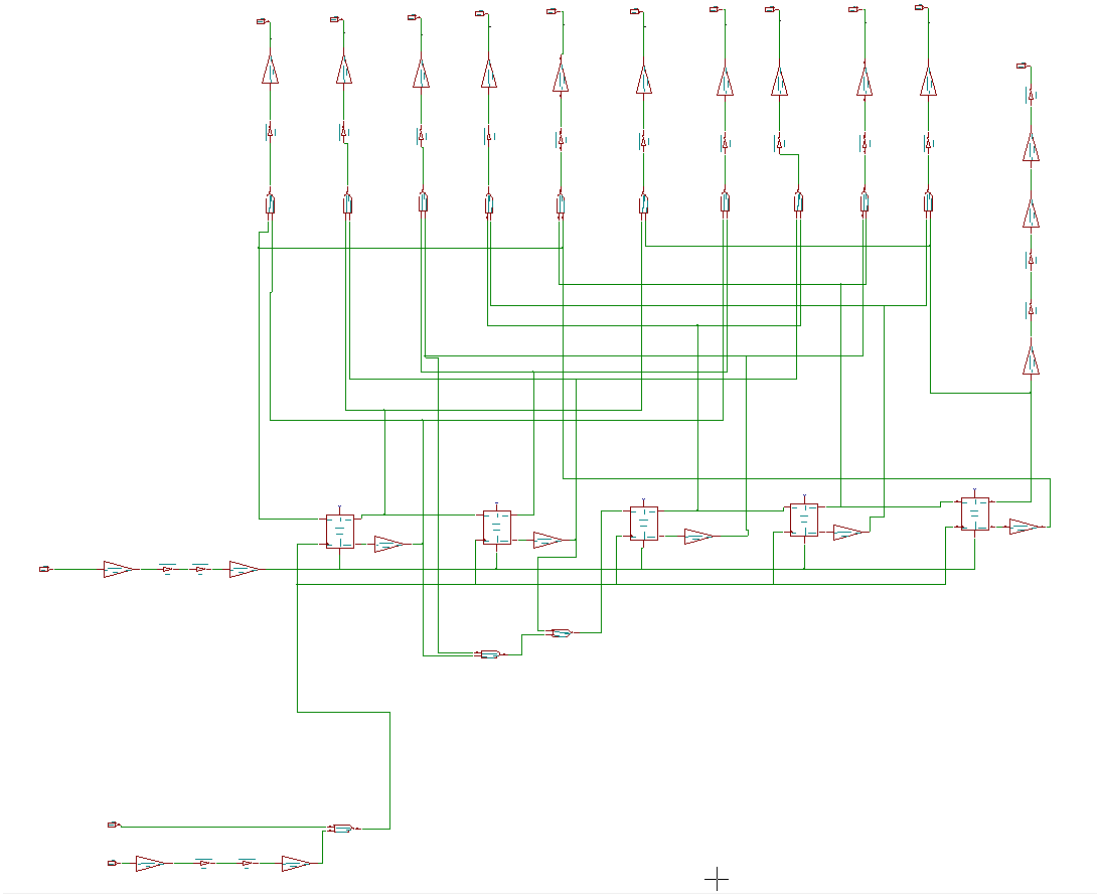

Figure 4.6.2.1: Subcircuit layout of the MC74HC238

4.7.3 Test Circuit

The test circuit for the CD4017B decade counter is designed to verify its sequential output behavior in response to clock pulses. A pulse source is applied to the CLK pin, while the RESET and CLK_INHIB inputs are controlled to test initialization and enable functions. Outputs Q0 to Q9 are monitored using voltage probes to observe the counting sequence. The carry-out (CARRY_OUT) pin is also probed to confirm divide-by-10 functionality

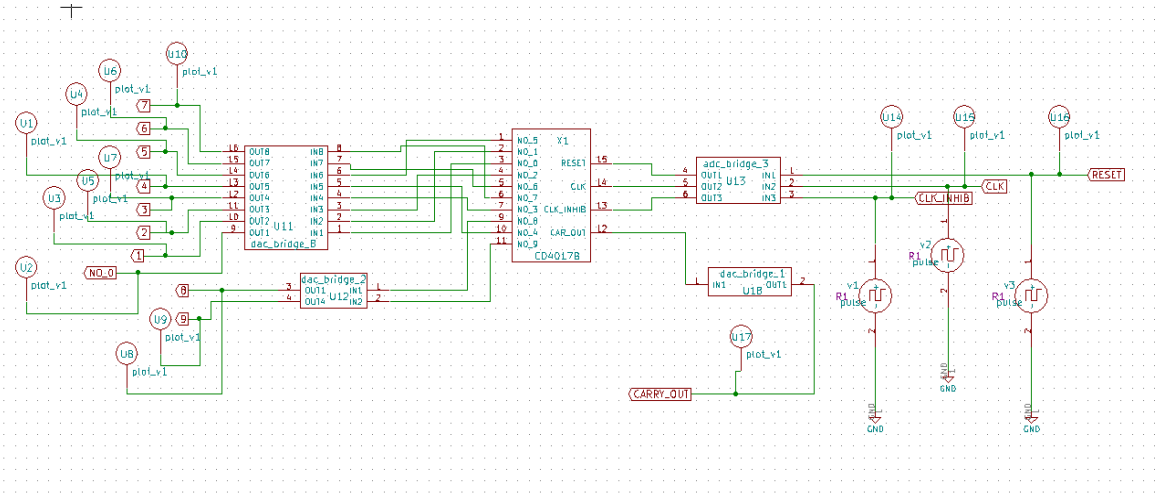

Figure 4.6.3.1: Test Circuit layout of the MC74HC238

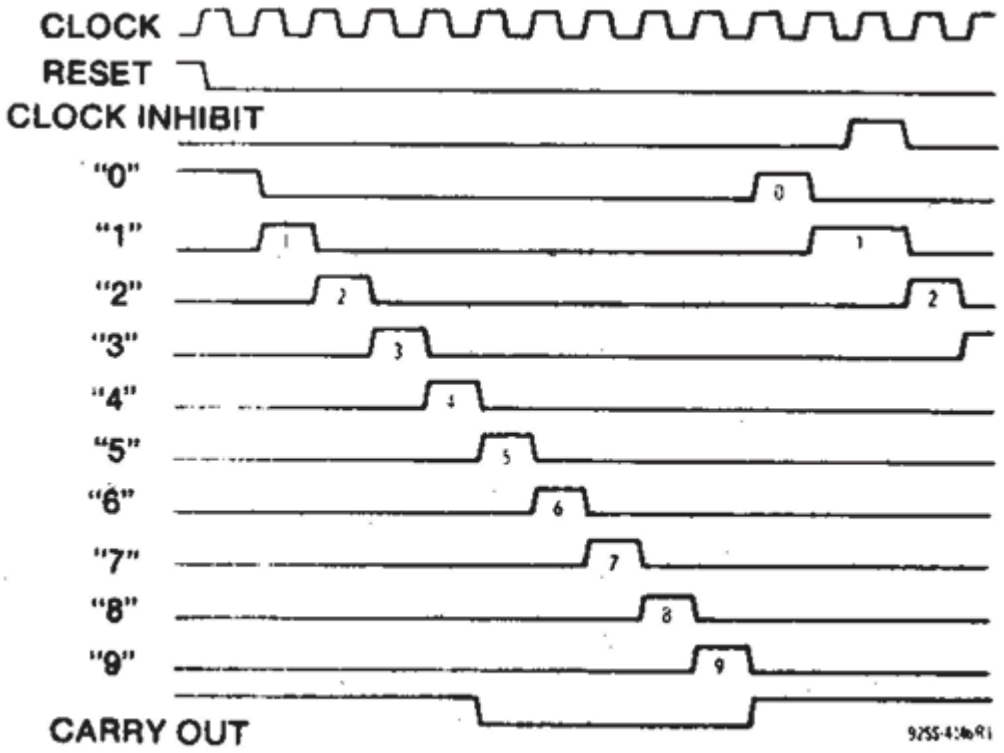

Fig. 2 – Timing diagram for CD4017B.

4.7.4 Waveform

The waveform illustrates the sequential operation of the CD4017B decade counter in response to clock pulses. Each output (Q0 to Q9) becomes high one at a time with every rising edge of the clock signal (v(clk)), confirming the expected divide-by-10 functionality. Initially, the reset signal (v(reset)) is held high, forcing all outputs low. Once reset goes low, the counter begins advancing with each clock pulse. The outputs shift sequentially, activating one output at a time in a staircase-like pattern. The carry-out signal (v(carry_out)) goes high after every tenth pulse, indicating a complete cycle. The clock inhibit signal (v(clk_inhib)) is temporarily activated around 120 ms, which halts the counting process despite the continued clock pulses. This validates the proper functioning of reset, clock, clock inhibit, and carry-out features of the CD4017B.

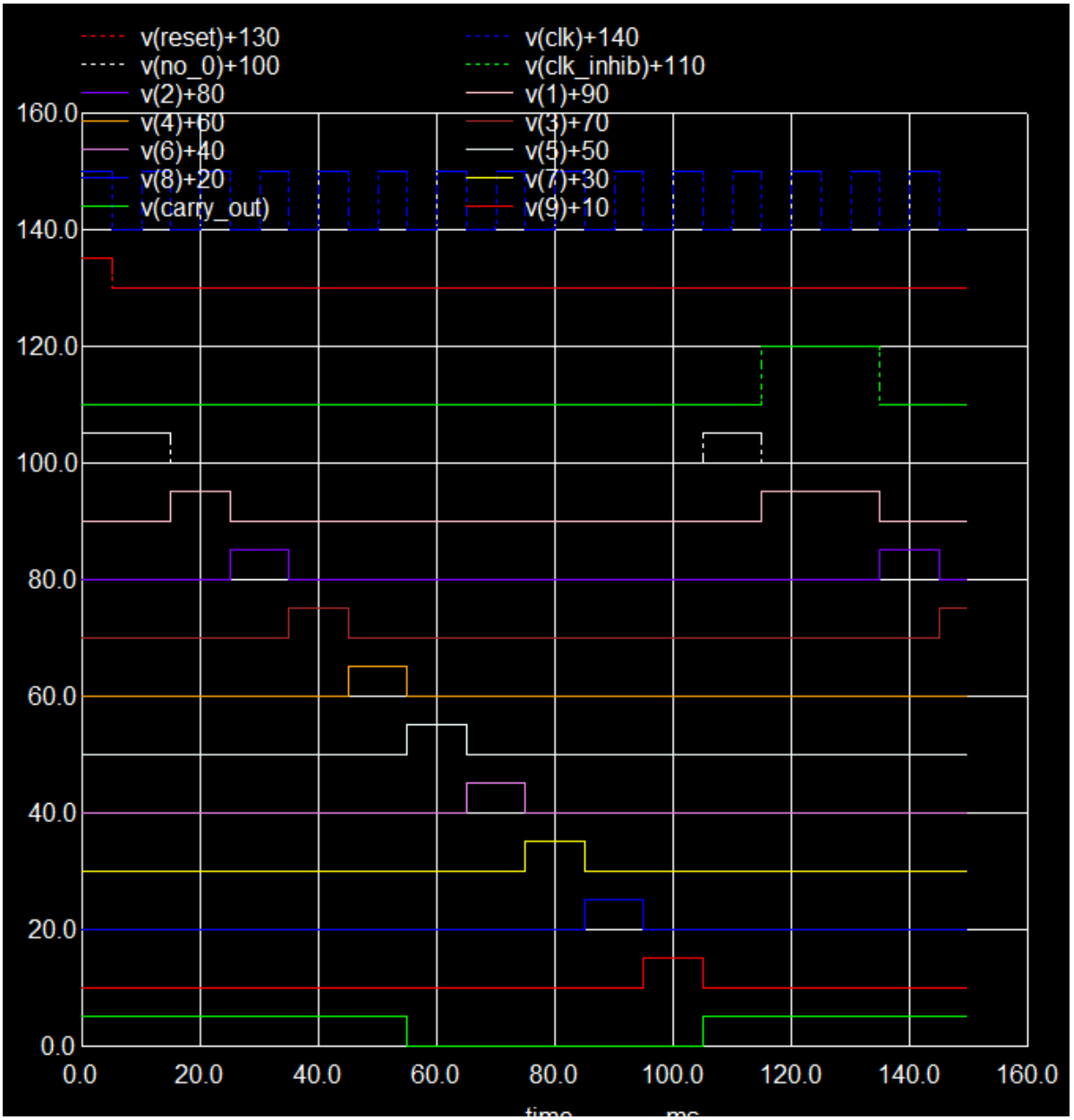

Figure 4.6.4.1 Functional Waveform of CD4017B

4.8 93L14

The **93L14** is a high-speed, multifunctional 4-bit latch IC designed for general-purpose storage applications in digital systems. It contains four independent latches, each of which can operate either in **D-type latch mode** or **set/reset latch mode**, controlled via an active-low enable input. The IC features active pull-up outputs for strong driving capability and improved noise immunity. Additionally, it includes a common active-low **master reset (MR)** input that overrides all other inputs, forcing all outputs to logic LOW. Its versatility and reliability make it suitable for use in timing, control, and data storage operations in complex digital circuits

4.8.1 Pin Diagram

The 93L14 is a 16-pin IC that includes four individual latches (Q0 to Q3), each with its own data input (D0 to D3) and set input (S0 to S3). The IC features a **common enable input (E)** and a **master reset input (MR)**, both of which are active low. The enable pin controls when the latches accept new data, while the master reset overrides all operations and clears all outputs to LOW when activated. The outputs (Q0 to Q3) provide the latched logic states based on the input combinations and control signals.

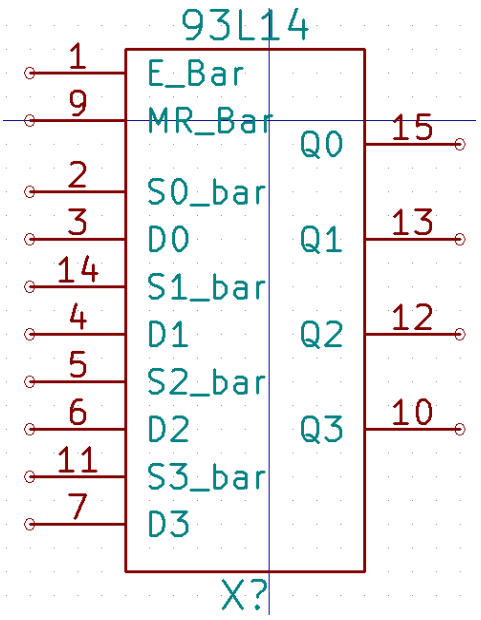

Figure 4.8.1.1: Pin Configuration of 93L14

4.8.2 Sub Circuit Layout

The subcircuit implementation of the 93L14 IC utilizes basic digital logic components such as inverters, AND, OR gates, and conditional logic to replicate the functional behavior of a quad latch with selectable D-type and Set/Reset modes. The subcircuit includes defined input terminals for Data (D), Enable (E), Set ($\overline{S}$), and Master Reset (MR), along with the output terminal Q. Logical expressions and gate arrangements are used to ensure correct mode operation based on the status of $\overline{S}$ and E, while the active-low Master Reset input overrides all other logic to force the output LOW when activated

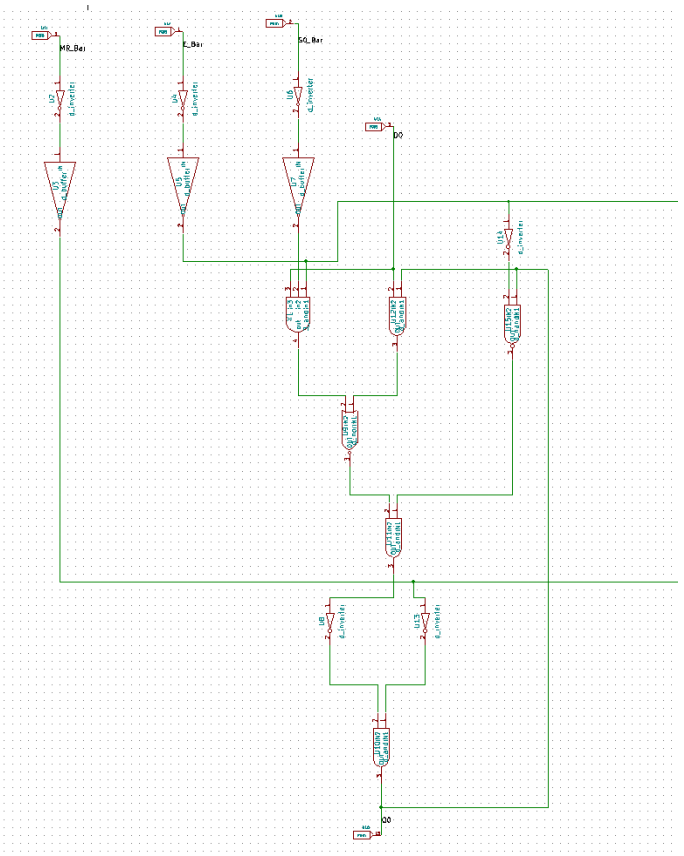

Figure 4.8.2.1: Subcircuit of Single Logic Latch of 93L14

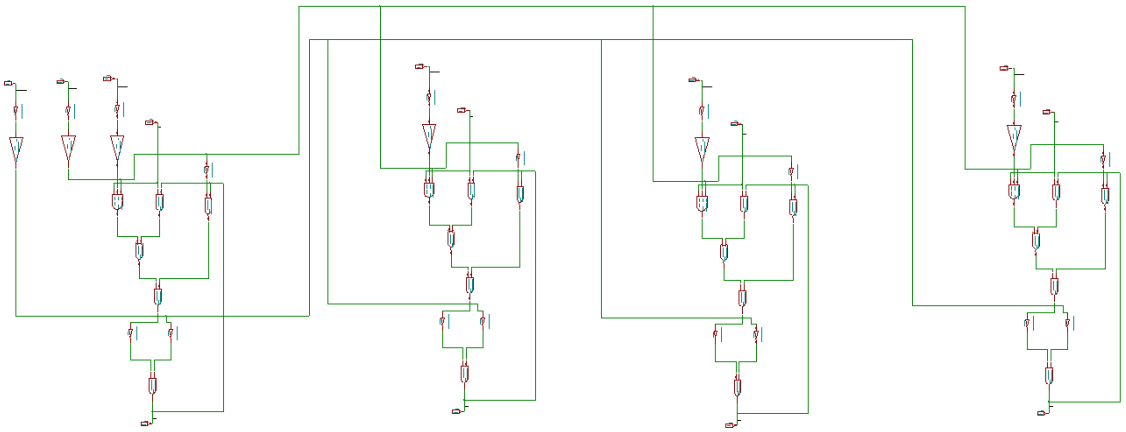

Figure 4.8.2.2 Subcircuit of 93L14

4.8.3 Test Circuit

The test circuit is designed to verify the operation of the 93L14 IC by applying controlled logic inputs to the pins $\overline{E}$, D, $\overline{S}$, and $M\overline{R}$ using independent DC voltage sources through series resistors. These inputs are labeled and connected to the respective terminals of the IC to test its behavior in D-latch and Set/Reset modes.

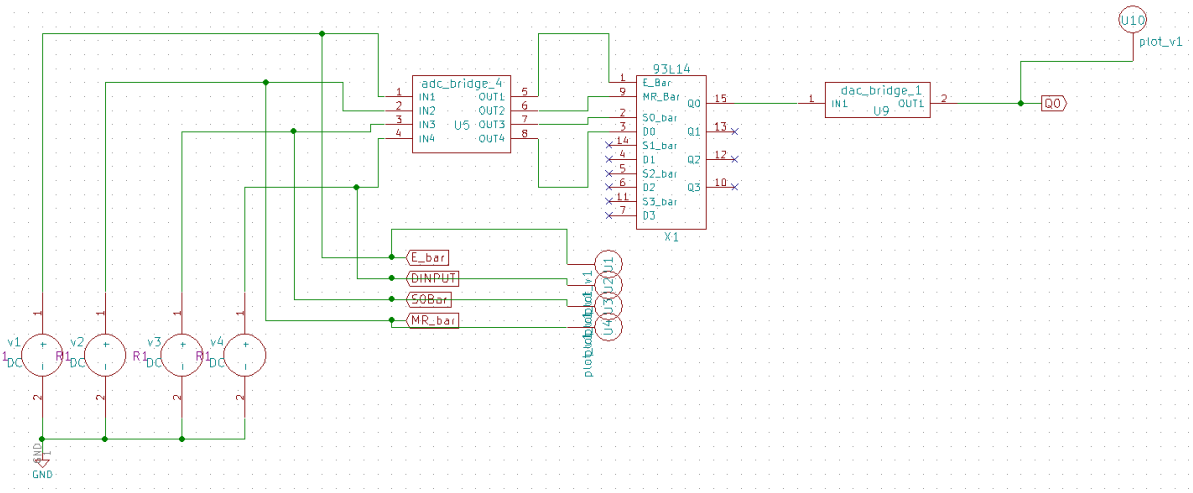

Figure 4.8.3.1: Test Circuit layout of 93L14

4.8.4 Input Condition

The waveform of 93L14 depends on this Truth Table which comprises D Latch mode and S/R latch Mode . The Mode of IC is dependent on the logic level applied to control inputs MR and E respectively which provides desired output based on inputs of D (in case of D mode) and S/R(in case of S/R Mode).

MR	E	D	$\overline{S}$	Qn	Operation Mode
H	L	L	L	L	D Mode (Q = 0)
H	L	H	L	H	D Mode (Q = 1)
H	H	X	L	Qn-1	Latch stored
H	L	L	H	L	R/S Mode (Reset)
H	L	H	H	H	R/S Mode (Set)
H	L	L	L	L	R/S Mode (D dominates)
H	H	X	H	Qn-1	Latched
L	X	X	X	L	**Reset All**

Figure 4.8.4.1: Truth Table for different conditions

4.8.5 Output Waveform

4.8.5.1 D MODE

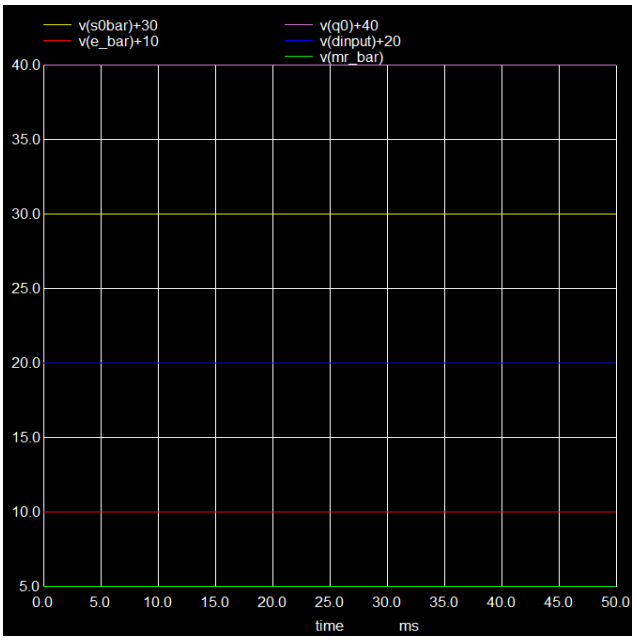

Figure 4.8.5.1.1: Output of 93L14

Input: MR - H ,E - L,D - L,S - L OUT: Q - L

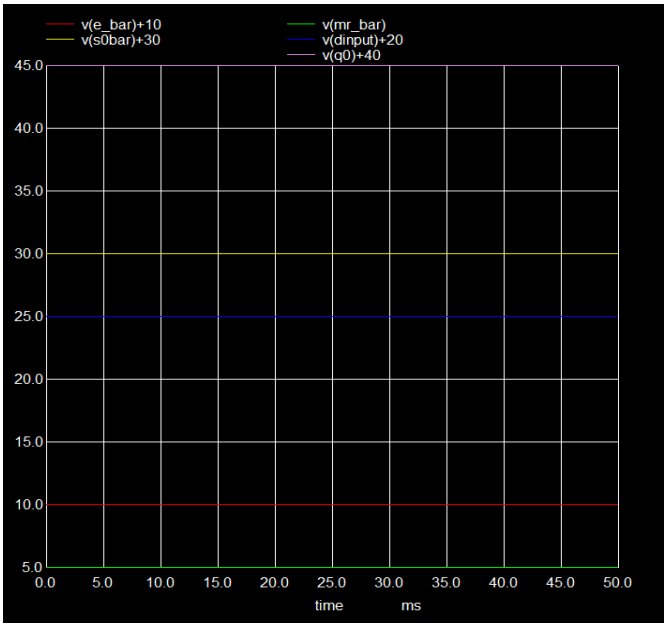

Figure 4.8.5.1.2: Output of 93L14

Input: MR - H ,E - L,D - H,S - L OUT: Q - H

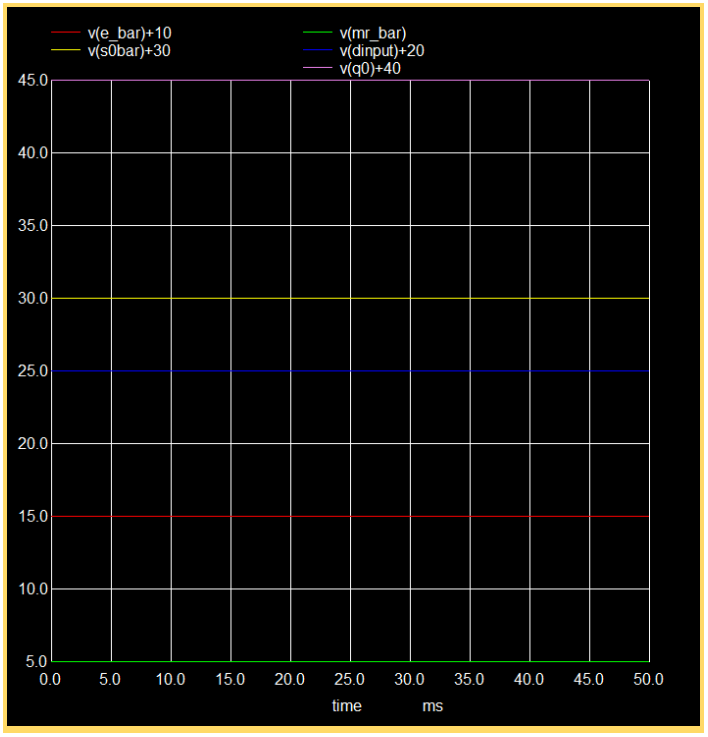

Figure 4.8.5.1.2: Output of 93L14

Input: MR - H ,E - L,D - X,S - L OUT: Q - Qn-1(Latch cond)

4.8.5.2 ALL RESET

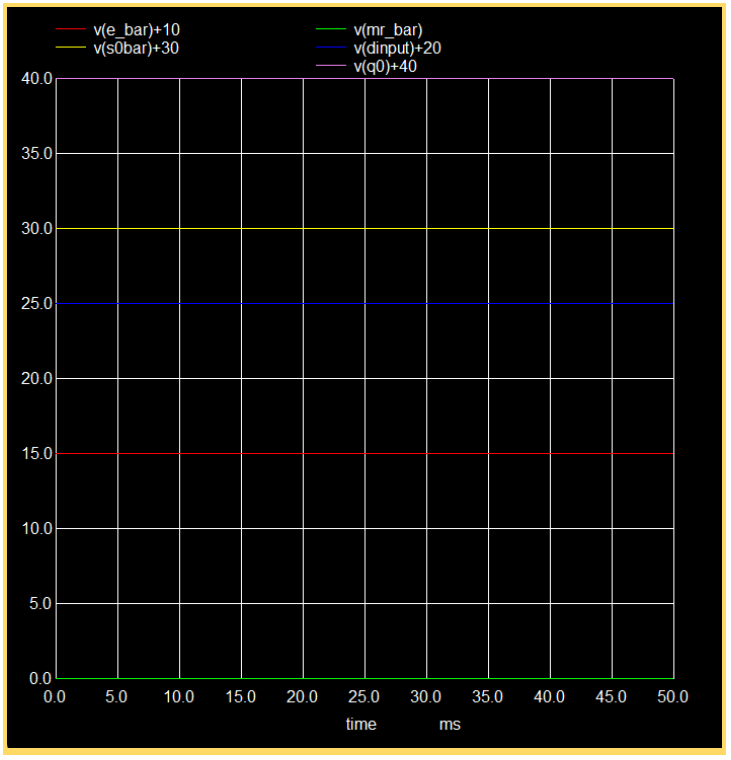

Figure 4.8.5.2.1: Output of 93L14

Input: MR - L ,E - X,D - X,S - X OUT: Q - L (ALL RESET cond)

The output waveform verifies the correct operation of the 93L14 latch, with $M\bar{R}$ held HIGH to allow normal functioning. In D-mode, with $\bar{S}$ LOW and $\bar{E}$ LOW, Q_0 followed D as expected (**Figure 4.8.5.1.1**). When $\bar{E}$ was made HIGH (and $M\bar{R}$ still HIGH), Q_0 latched the previous state of D, showing correct latch behavior (**Figure 4.8.5.1.2**). Finally, when $M\bar{R}$ was pulled LOW in any state, the output Q_0 immediately reset to logic LOW, overriding all other inputs (**Figure 4.8.5.2.1**).

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4.9 CD4030B

The **CD4030B** is a **quad 2-input Exclusive-OR (XOR) gate** IC based on CMOS technology. It consists of four independent XOR gates in a single package, each performing the logic function $\mathbf{A \oplus B}$ (output is high only when the inputs differ). This IC is commonly used in digital logic systems for operations like parity checking, bit comparison, and arithmetic circuits. The CD4030B supports a wide operating voltage range from **3V to 15V**, offers **low power consumption**, and provides **high noise immunity**, making it suitable for battery-powered and low-power applications. Its outputs are fully compatible with both TTL and CMOS logic levels.

4.9.1 Pin Diagram

The **CD4030B** is a 14-pin IC that contains four independent 2-input XOR gates. Each gate has two input pins and one output pin. The input pins for the gates are arranged in pairs: **Gate 1** uses pins 1 and 2 as inputs and pin 3 as output, **Gate 2** uses pins 5 and 6 as inputs and pin 4 as output, **Gate 3** uses pins 8 and 9 as inputs and pin 10 as output, and **Gate 4** uses pins 12 and 13 as inputs and pin 11 as output. Pin 7 is connected to ground VSS, and pin 14 is connected to the positive supply voltage VDD. This symmetrical pin arrangement allows the IC to be easily used in standard digital logic applications.

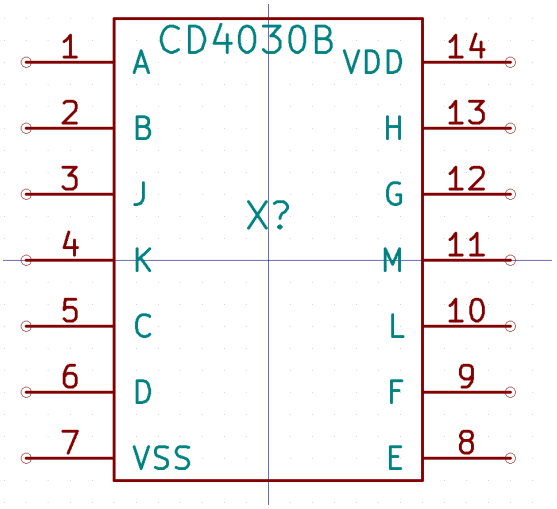

Figure 4.9.1.1: Pin Configuration of CD4017B

4.9.2 Sub Circuit Layout

The Subcircuit of the CD4030B consists of four identical 2-input Exclusive-OR (XOR) gates, each implemented using CMOS transmission gates and logic inverters. Internally, each XOR gate is formed by combining basic CMOS logic structures like NAND, NOR, and Inverter gates, configured in such a way that the output becomes logic high (`1`) only when the two inputs differ. When both inputs are the same (`0,0` or `1,1`), the output is low (`0`). The use of CMOS technology ensures low static power consumption, high input impedance, and rail-to-rail output swing.

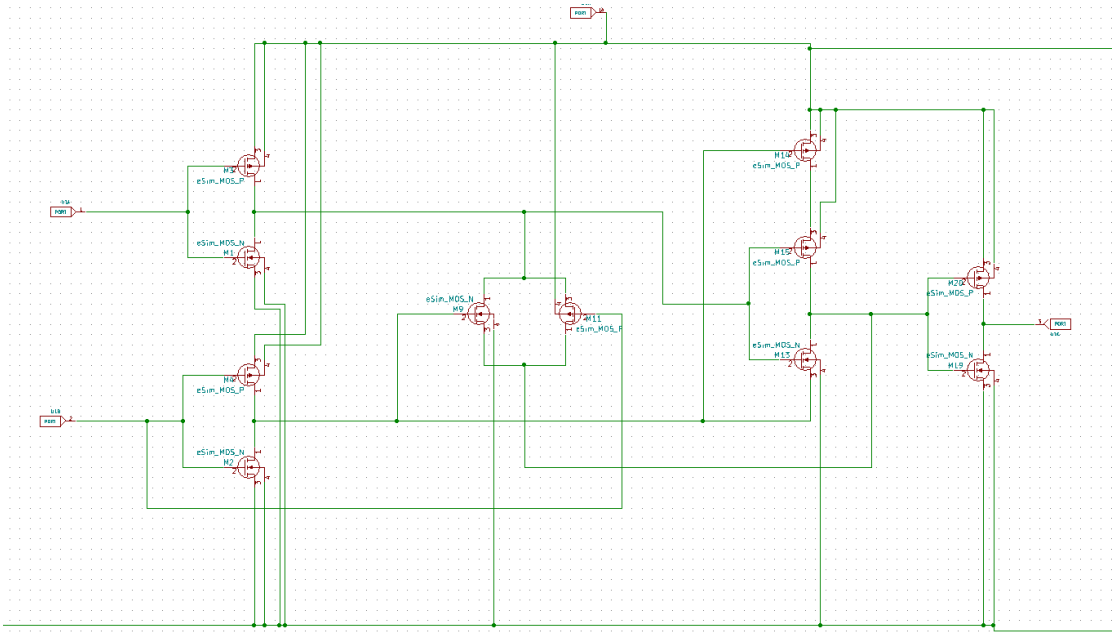

Figure 4.9.2.1: Subcircuit layout of the CD4030B(Single Logic)

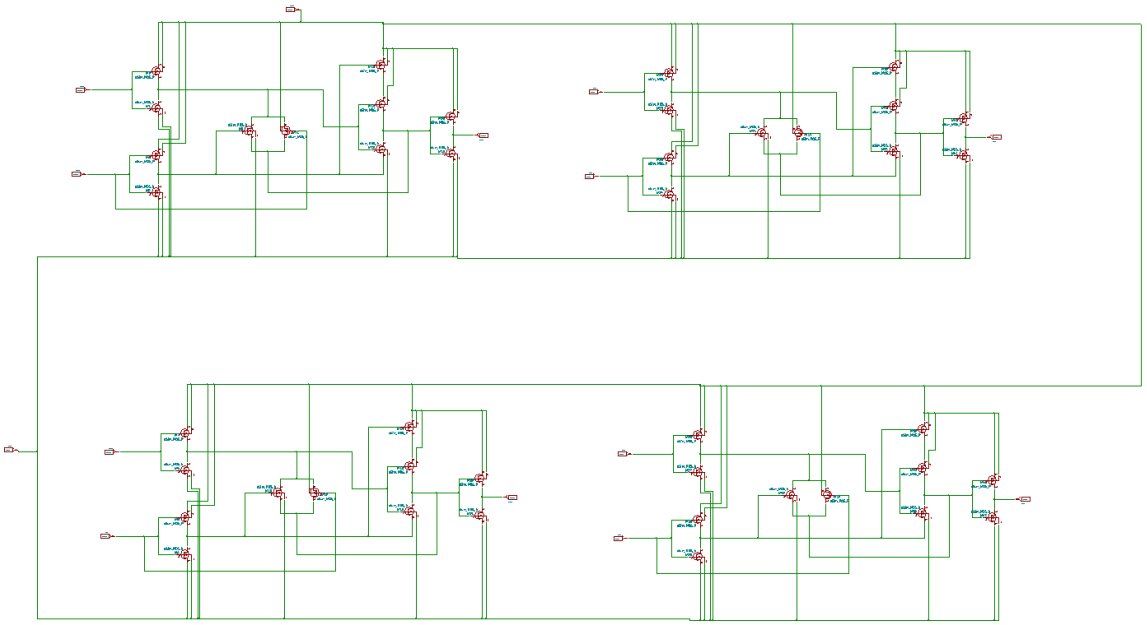

Figure 4.9.2.2: Subcircuit layout of the CD4030B

4.9.3 Test Circuit

The test circuit demonstrates the working of the **CD4030B** quad XOR gate using one of its four gates. Two digital pulse signals are applied as inputs **A** and **B** through function generators to test the XOR behavior. These inputs are connected to pins 1 and 2 of the IC, and the resulting output is taken from pin 3, which represents $\mathbf{A \oplus B}$ (high only when A and B differ). The circuit is powered using a DC voltage source connected to **VDD** (pin 14), and **VSS** (pin 7) is connected to ground.

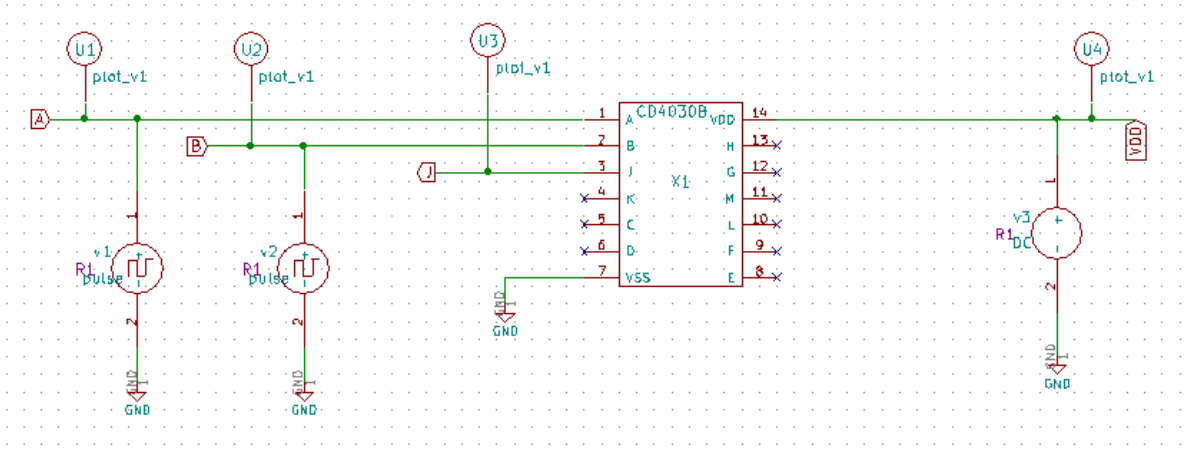

Figure 4.9..3.1: Test Circuit layout of the 4030B

4.9.4 Input Conditions

The input condition for the XOR gate in the **CD4030B** IC follows the standard Exclusive-OR logic behavior. When both inputs A and B are **low (0)** or both are **high (1)**, the output is **low (0)**. However, if one input is **high (1)** and the other is **low (0)**, the output becomes **high (1)**. In other words, the output is high only when the two inputs are **logically different**. This behavior is fundamental to XOR logic and is used in applications like parity generation, digital comparison, and controlled logic switching.

TRUTH TABLE FOR ONE OF FOUR IDENTICAL GATES

A	B	J
0	0	0
1	0	1
0	1	1
1	1	0

1 = HIGH LEVEL
0 = LOW LEVEL

Figure 4.9.4.1: Input and output conditions

4.9.5 Output Waveform

The output waveform shows about the functional and logical behaviour about EXOR gate.

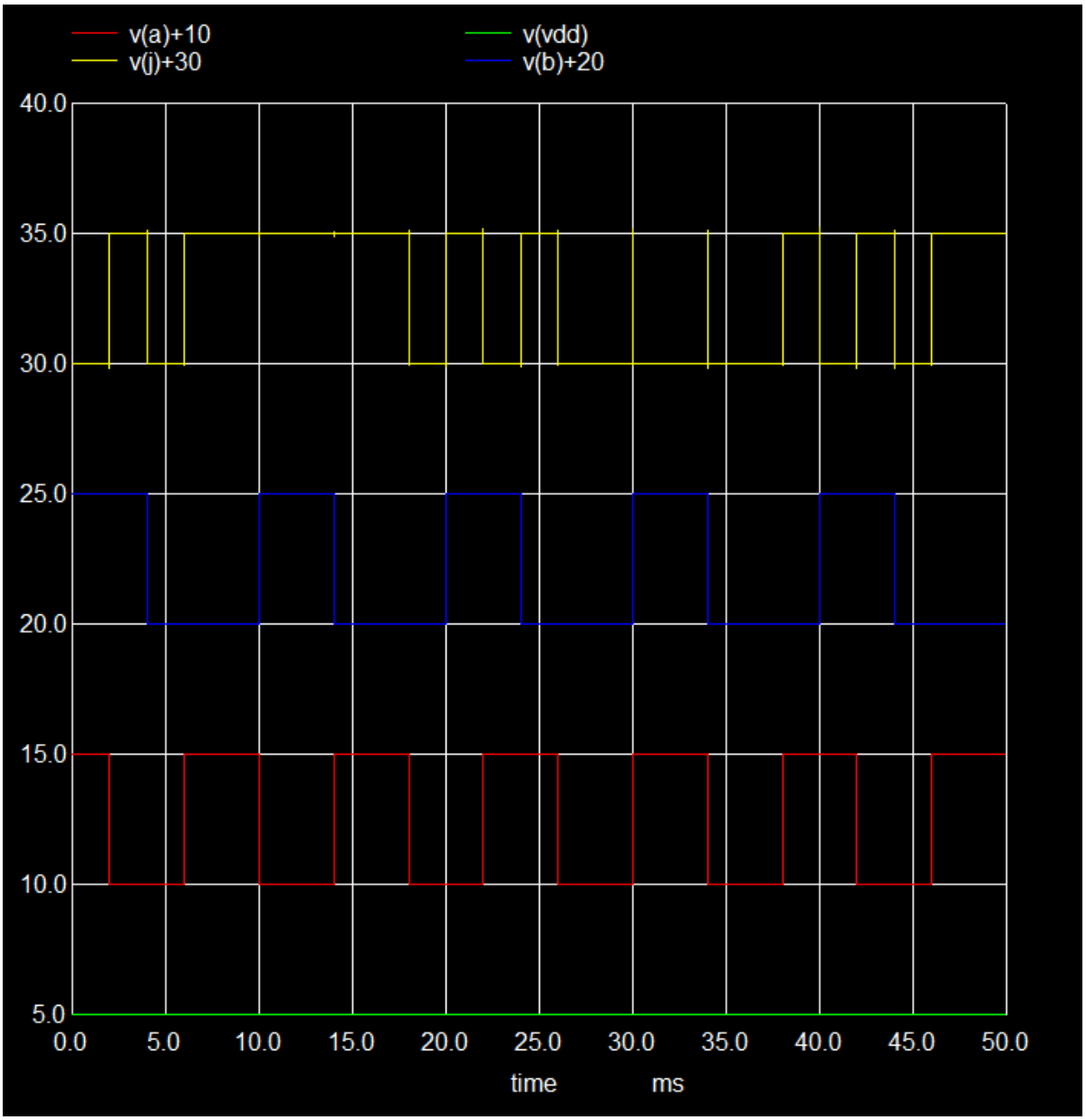

Figure 4.9.5.1: Output Waveform for CD4030B

4.10 L702

The **L702** is a monolithic quad Darlington switch IC designed for high-current, high-voltage switching applications. It features **four Darlington transistor pairs** with a common emitter and open-collector configuration, enabling it to **sink currents up to 2A** with a **sustaining voltage of 70V**. Available in **PowerDIP and Multiwatt-11 packages**, the L702 is ideal for directly driving **DC motors, solenoids, relays, stepper motors, and displays**.

This IC offers **high current gain** and can interface directly with **low-level logic circuits** like TTL and CMOS, minimizing the need for additional driver components. Its integration simplifies design, reduces space, and lowers cost, making it a practical solution for control systems and automation projects.

4.10.1 Pin Diagram

In the **Multiwatt package**, the pins are arranged such that the first half typically contains the input pins, while the second half includes the outputs, with the **center pin (pin 9 or 10)** usually designated for the **common emitter (GND)**. The pinout supports easy interfacing with multiple loads, making it effective for parallel switching of inductive devices such as motors or relays.

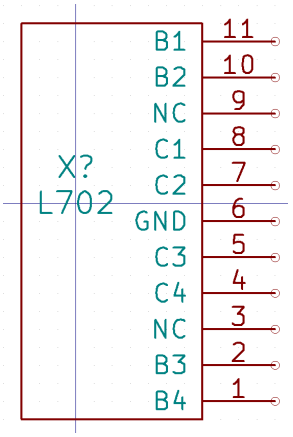

Figure 5.5.1.1: Pin Configuration of the CD4050

4.10.2 Sub Circuit Layout

The subcircuit of the **L702** consists of four Darlington transistor stages, each made up of two NPN transistors connected in a Darlington configuration to achieve high current gain. These stages have **independent inputs** and **open collector outputs**, with all emitters internally connected to a common **GND pin**. The design allows each channel to act as a current sink, enabling the IC to control high-current loads using low-level logic signals. Internal base resistors and clamp diodes are included to ensure fast switching and protection against inductive kickback, making the L702 suitable for driving relays, motors, and other inductive loads.

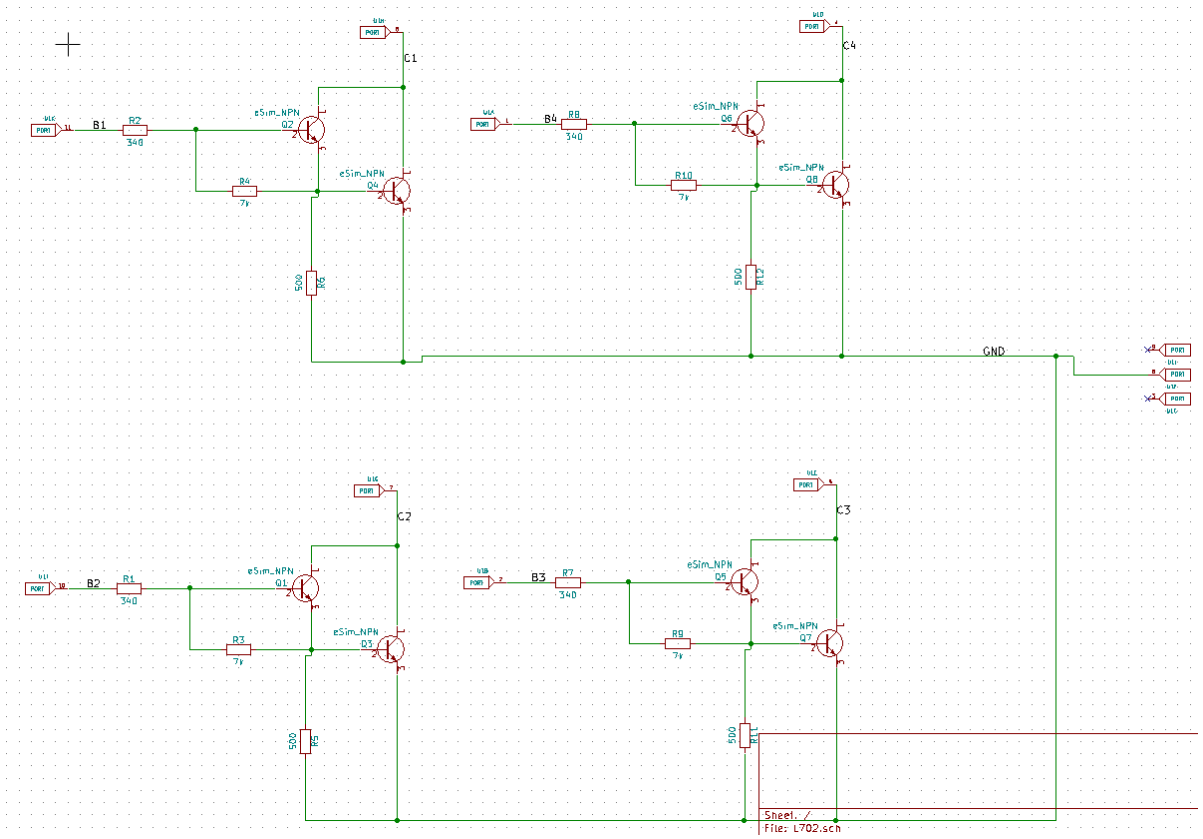

Figure 4.10.2.1: Subcircuit of L702

4.10.3 Test Circuit

The test circuit demonstrates the switching action of the L702 quad Darlington array, where a **pulse input (v2)** is applied to one of the input pins of the IC to simulate a digital control signal. The corresponding output pin is connected to a **1kΩ load resistor**, which is tied to a **DC supply (v1)**. When the input pulse goes high, the Darlington pair inside the L702 conducts, allowing current to sink through the load to ground, effectively pulling the **VOUT** node low. This setup verifies the IC's functionality in current-sinking applications, typically used for driving inductive or resistive loads with logic-level inputs..

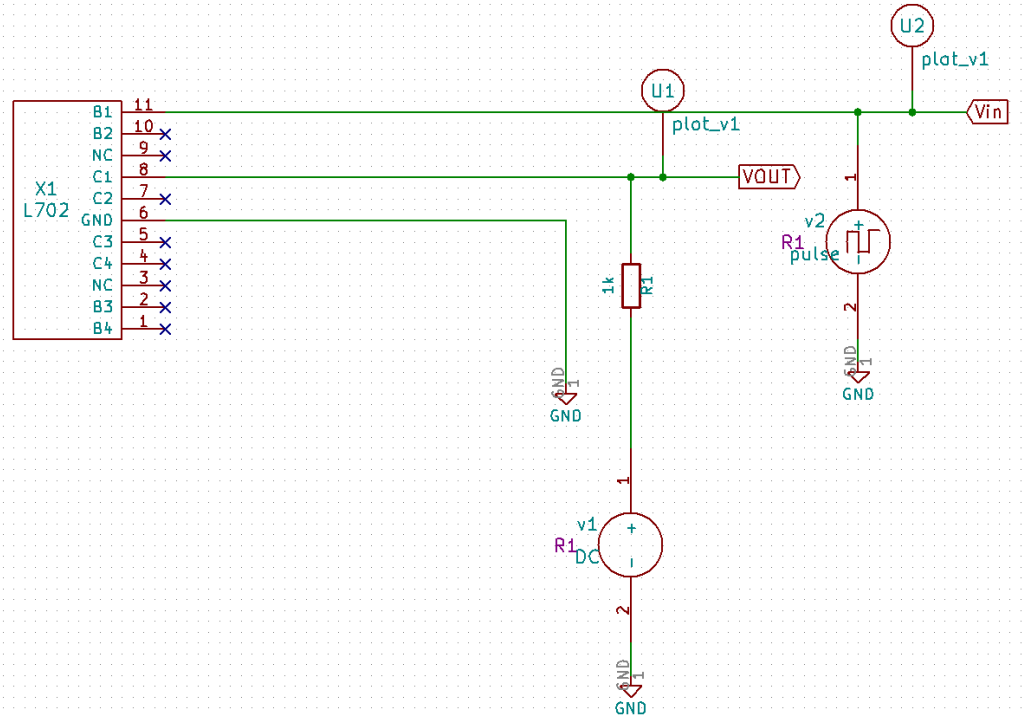

Figure 5.5.3.1: Test circuit layout of the L702

4.10.4 Input and Output waveforms

The waveform illustrates the switching behavior of the L702 when a **5V pulse input (Vin)** is applied and the output is connected to a **12V DC supply (VDD)** through a 1kΩ resistor. The green plot represents the input pulse signal, which alternates between 0V and 5V. When **Vin goes high (5V)**, the internal Darlington transistor turns on, causing the output voltage **Vout** (shown in red, shifted by +10V for clarity) to drop close to **0V**, indicating that the load is being pulled to ground. When **Vin goes low (0V)**, the Darlington pair switches off, and **Vout** rises to approximately **12V**, reflecting the pull-up from the DC supply. This confirms that the L702 IC effectively acts as a **low-side switch**, operating correctly in response to the input pulses.

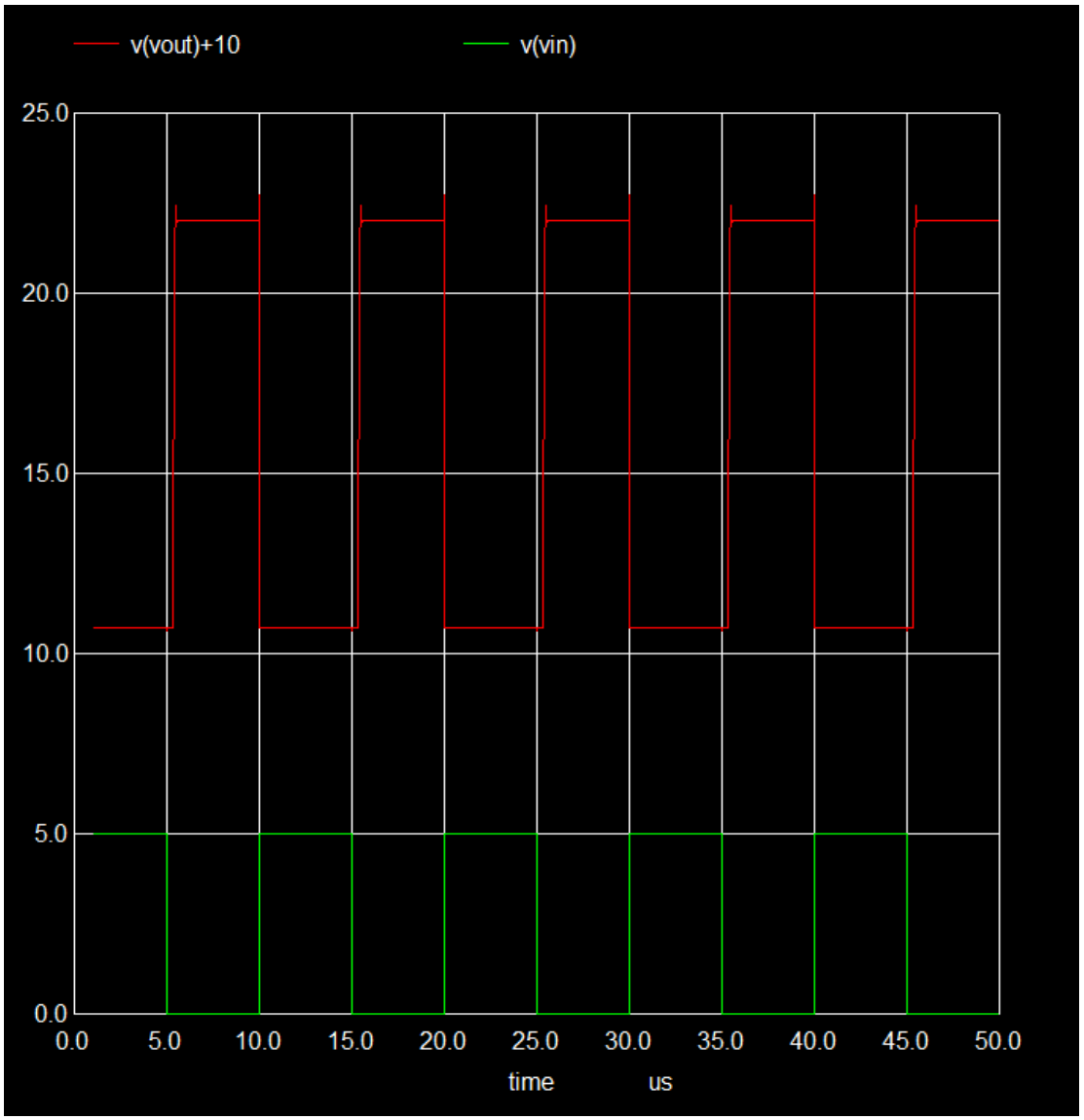

Figure 4.10.4: Waveform of L702

4.11 SN74S163

The **SN74S163** is a high-speed, synchronous 4-bit binary counter developed by Texas Instruments. It performs counting operations in perfect synchrony with the system clock, ensuring accurate and simultaneous output transitions without the ripple effect seen in asynchronous counters. The device supports functions such as synchronous clearing and presetting, making it highly suitable for use in systems requiring precise control over counting sequences.

A key feature of the SN74S163 is its **terminal count capability**, which provides an indication when the counter reaches its maximum binary value. This function is particularly useful for cascading multiple counters to create wider counting ranges or triggering subsequent operations in a digital system. Owing to its fast operation, predictable timing behavior, and flexible control features, the SN74S163 is widely used in applications such as event counting, frequency division, timing control, and digital sequencing.

4.11.1 Pin Diagram

The **SN74S163** is a 16-pin synchronous 4-bit binary counter. The **CLK** (Clock) input controls all state transitions on the rising edge, enabling precise timing. The **CLR** (Clear) input is used to synchronously reset the counter to zero, while the **LOAD** input allows loading a preset 4-bit value through inputs **A, B, C, and D**. Counting progresses only when both **ENP** and **ENT** are active. The outputs **Q0 to Q3** represent the current binary count. The **RCO** output goes high when the counter reaches its maximum value, making it suitable for cascading multiple counters.

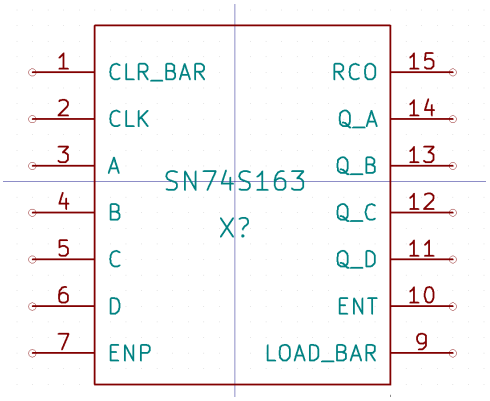

Figure 4.11.1.1 : Pin Diagram of SN74S163

4.11.2 Subcircuit Layout

The internal circuit of the SN74S163 consists of four edge-triggered D flip-flops arranged to form a 4-bit binary counter, with all flip-flops clocked synchronously by a common clock input (CLK). Logic gates manage control signals such as CLR for synchronous reset, LOAD for presetting data inputs (DATA A–D), and ENP/ENT for enabling the count operation. The outputs (QA–QD) represent the current binary count, and the terminal count output (RCO) is generated when the counter reaches its maximum value, allowing for cascading multiple counters.

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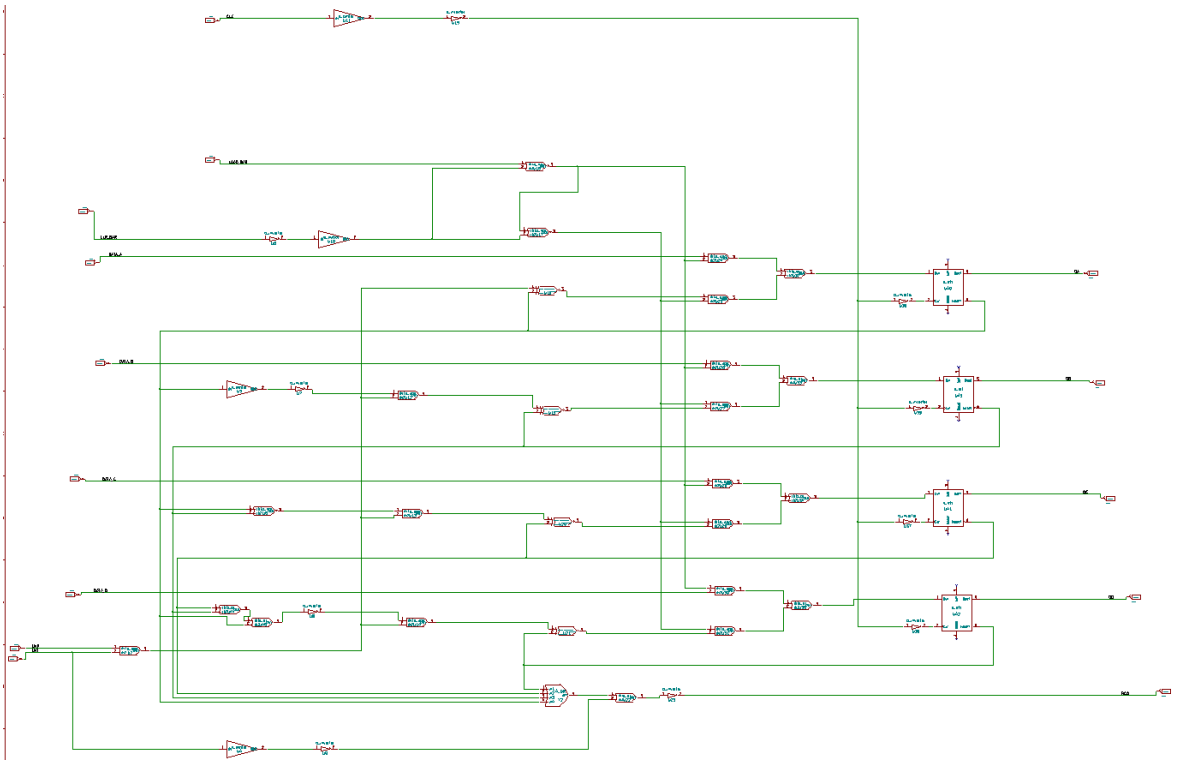

Figure 4.11.2.1 : Subcircuit Layout of Sn74S163

4.11.3 Test Circuit

The test circuit illustrates the functional verification of the **SN74S163** 4-bit synchronous binary counter using pulse generators to simulate digital inputs. Control signals such as CLK, CLR_BAR, LOAD_BAR, ENP, and ENT are driven through resistors, while data inputs A, B, C, and D are preset using separate pulse sources. The counter outputs QA to QD and the terminal count output RCO are connected to plotting terminals for waveform observation.

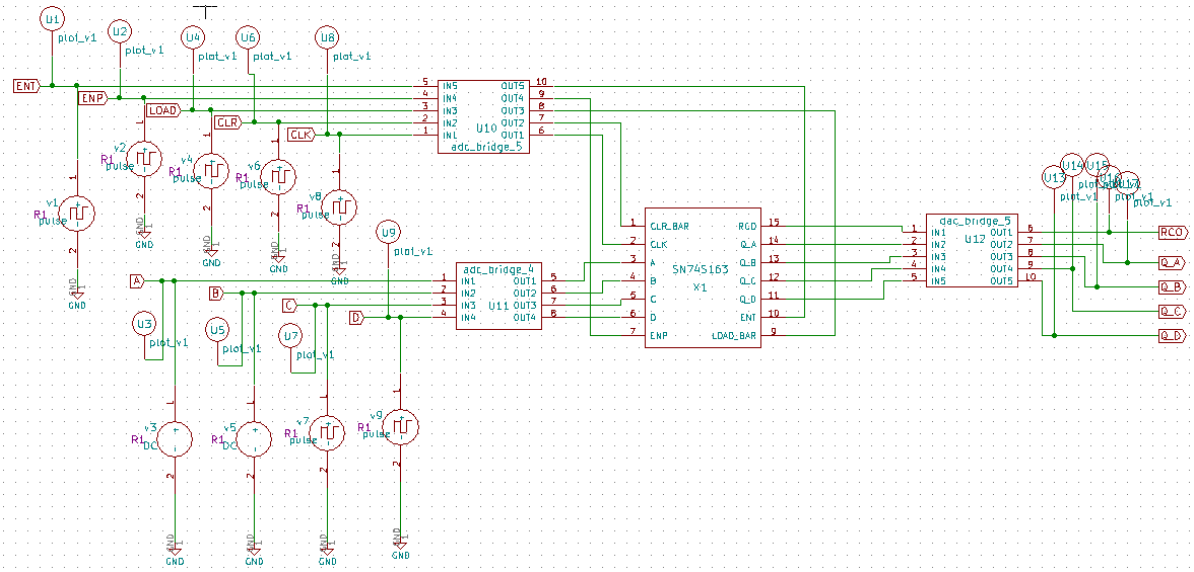

Figure 4.11.3.1 : Test Circuit of SN74S163

4.11.4 Input conditions

The Input conditions provide the expected correctness of output therefore, when the **Clear** input is low (0), the counter is synchronously reset, forcing all outputs to zero, regardless of other inputs. If **Clear** is high (1) and **Load** is low (0), the data present on inputs **A–D** is loaded into the counter. For normal counting operation, both **ENT** and **ENP** must be high (1); in this condition, the counter increments its value on each clock pulse. If either **ENT** or **ENP** is low, the counter holds its current state and no counting occurs. This logic ensures controlled and predictable counter behavior in response to external signals.

Clear	Load	ENT	ENP	Action on the rising clock edge
0	X	X	X	All 4 flip-flop outputs cleared
1	0	X	X	Load preset inputs data(A, B, C, & D) to Qn
1	1	1	1	Increment Count
1	1	0	X	No change (Hold)
1	1	X	0	No change (Hold)

Figure 4.11.4.1 : Input condition of SN74S163

The given waveform represents the **expected output response** of the SN74S163 counter. It shows synchronous clear, parallel load from data inputs (A–D), and normal counting when both enable (ENP and ENT) are active. Outputs (QA–QD) increment on each rising clock edge, and the **RCO** output goes high at terminal count. When counting is disabled, the outputs hold their last state.

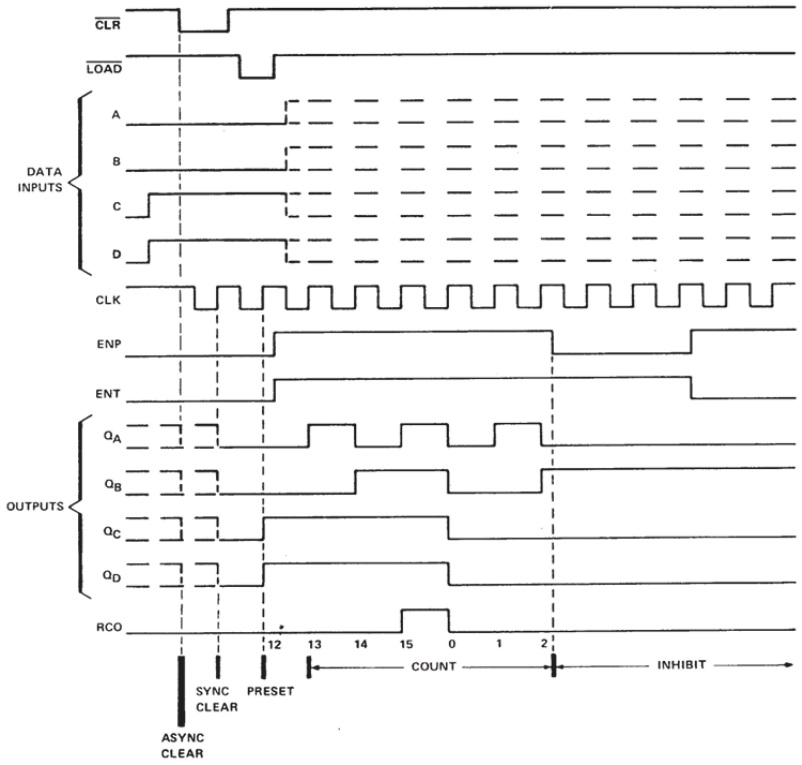

Figure 4.11.4.2 : Expected output response of SN74S163

4.11.5 Output Waveform

The waveform shown represents the **simulated output** of the SN74S163 4-bit synchronous binary counter. Control inputs CLR, LOAD, ENT, and ENP are appropriately pulsed to demonstrate various functional modes. After clearing, the counter loads the preset values from inputs A to D, followed by normal counting as observed in the sequential rise of outputs Q_A, Q_B, Q_C, and Q_D. The RCO signal goes high upon reaching the terminal count. This output validates the expected behavior of the counter under synchronous operation, confirming correct functionality of load, clear, and counting operations.

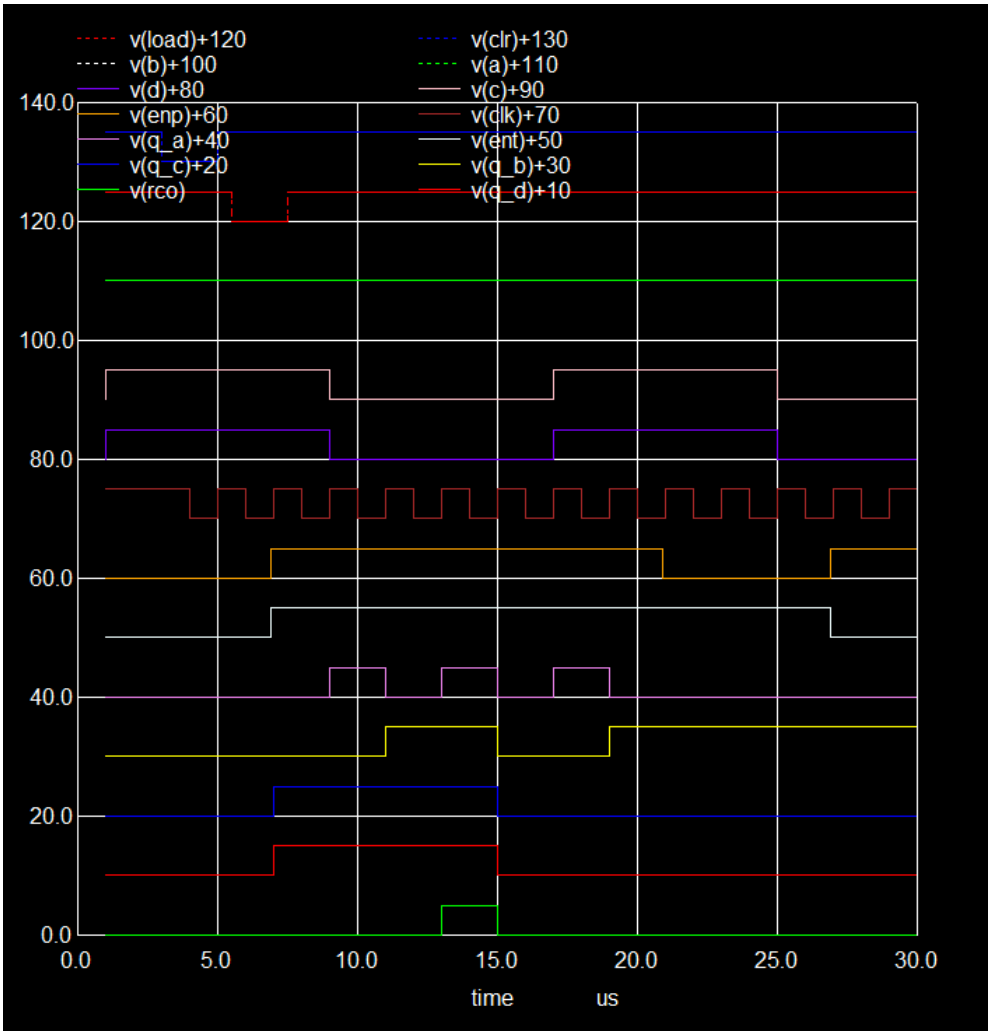

Figure 4.11.5.1 : Output of SN74S163

Chapter 5

Conclusion and Future Scope

A diverse set of subcircuits has been successfully developed for a range of fundamental Analog and Digital ICs, carefully designed in alignment with the specifications provided in their respective datasheets. This collection includes essential components such as **voltage regulators, latches, binary counters, logic gates, and amplifiers**, all of which play a crucial role in both basic and advanced circuit designs. Each subcircuit was rigorously tested using dedicated simulation testbenches to ensure accurate functionality and dependable behavior under varied conditions. These validated models are now ready for integration into the **eSim subcircuit library**, offering a reliable and modular resource for students, educators, and circuit designers. Looking ahead, the library will continue to expand with the inclusion of more specialized ICs and complex system blocks, further strengthening eSim's role as an educational and development platform for electronics design and simulation.

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