



# Summer Fellowship Report

On

## Integrated Circuit Design using Subcircuit Feature of eSim

Submitted by

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Under the guidance of

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# Acknowledgment

I would like to express my sincere gratitude to the FOSSEE team at IIT Bombay for giving me the opportunity to contribute and work on the design and integration of multiple sub-circuits using eSim. This experience has been immensely enriching, offering me hands-on exposure to open-source EDA tools and a deeper understanding of their practical significance in circuit simulation and design.

My heartfelt gratitude goes to Prof. Kannan M. Moudgalya for his invaluable guidance, motivation, and unwavering support throughout the fellowship.

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All in all, interning at FOSSEE has not only enhanced my technical capabilities but also deepened my appreciation for the open-source ecosystem. As a passionate learner and beginner stepping into the semiconductor domain, this opportunity has been a defining milestone in my academic and professional growth, one that I will always value.

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# Chapter 1

# Introduction

## 1.1 FOSSEE

FOSSEE, an abbreviation for Free/Libre and Open Source Software for Education, is an initiative based at the Indian Institute of Technology (IIT) Bombay. It operates under the National Mission on Education through Information and Communication Technology (NMEICT), a program by the Ministry of Education (MoE), Government of India.

It promotes the adoption and integration of FLOSS (Free/Libre and Open Source Software) tools to enhance the quality of education in India. FOSSEE aims to reduce the reliance on proprietary software in educational institutions by advocating for the use of open-source alternatives. Through various outreach and development activities, the project supports the replacement of commercial software with equally capable FLOSS tools. Additionally, FOSSEE actively contributes to the creation of new tools and the enhancement of existing ones to better align with the evolving needs of academia and research.

## 1.2 eSim

eSim (previously known as Oscad/FreeEDA) is a free/libre and open-source Electronic Design Automation (EDA) tool developed as part of the FOSSEE project, based at IIT Bombay. It supports circuit design, simulation, analysis, and PCB design, making it a comprehensive platform for electronics design.

Built using a suite of open-source tools such as KiCad, Ngspice, GHDL, OpenModelica, Verilator, Makerchip, and the SkyWater SKY130 PDK, eSim is released under the GNU General Public License (GPL). eSim can effectively replace commercially licensed software such as OrCAD, PSpice, LTspice, Xpedition, and HSPICE, thus, serving as a cost-effective and accessible alternative for educational institutions, students, researchers, and small and medium enterprises (SMEs) ,along with supporting the broader mission of reducing reliance on commercial software in academia and industry.

The key features of eSim include:

- Schematic design and simulation using KiCad and Ngspice
- PCB layout and Gerber file generation
- Mixed-signal simulation support
- Model and subcircuit editing via Model Builder and Subcircuit Builder
- OpenModelica interface for system-level modeling
- Compatible with Ubuntu and Windows

## 1.3 Ngspice

NgSpice is an open-source, text-based SPICE simulator used for analyzing analog, digital, and mixed-signal electronic circuits. It supports a wide range of simulations including DC, AC, transient, and noise analysis, and can handle various components such as MOSFETs, BJTs, JFETs, diodes, resistors, capacitors, and inductors. Users define circuits using netlists, and the simulator generates outputs like voltage and current waveforms or data files. NgSpice is customizable, integrates well with tools like KiCad and eSim, and is widely used in both academic and professional environments for circuit design and research.

## 1.4 Makerchip

Makerchip is an easy-to-use platform for digital circuit design that works both in a web browser and on a desktop. It allows users to write, simulate, and debug Verilog, SystemVerilog, and Transaction-Level Verilog code. Makerchip uses a mix of open-source and other tools to offer a wide range of features. It connects with eSim through a Python tool called Makerchip-App, which helps open the Makerchip interface. The platform is designed to be simple and helpful for users at any level, with clear workflows and useful features. While most open-source tools focus only on one task like simulation or PCB design, eSim fills this gap by combining design, simulation, and layout in one place.

# Chapter 2

# Feautures Of eSim

The objective behind the development of eSim is to provide an open source EDA solution for electronics and electrical engineers. The software should be capable of performing schematic creation, PCB design and circuit simulation (analog, digital and mixed-signal). It should provide facilities to create new models and components. Thus, eSim offers the following features -

1. **Schematic Creation:** eSim provides an easy-to-use graphical interface for drawing circuit schematics, making it accessible for users of all levels. Users can drag and drop components from the library onto the schematic, simplifying the design process. Comprehensive editing tools allow for easy modification of schematics, including moving, rotating, and labeling components.

2. **Circuit Simulation:** eSim supports SPICE (Simulation Program with Integrated Circuit Emphasis), a standard for simulating analog and digital circuits. Users can perform various types of analysis such as transient, AC, and DC, providing insights into circuit behavior over time and frequency.An integrated waveform viewer helps visualize simulation results, aiding in the analysis and debugging of circuit designs.

3. **PCB Design:** The PCB layout editor allows users to place components and route traces with precision. eSim includes DRC capabilities to ensure that the PCB design adheres to manufacturing constraints and electrical rules. Users can generate Gerber files, which are standard for PCB fabrication, directly from their designs.

4. **Subcircuit Feature:** This feature enables users to create complex circuits by integrating smaller, simpler subcircuits, promoting modular and hierarchical design approaches. Subcircuits can be reused in different projects, saving time and effort in redesigning common circuit elements.

5. **Open Source Integration:** eSim integrates several open-source tools like KiCad, Ngspice, and GHDL, providing a comprehensive suite for electronic design automation. Being open-source, eSim is free to use, making advanced circuit design tools accessible without the need for expensive licenses.

# Chapter 3

# Problem Statement

*To design and develop various Analog and Digital Integrated Circuit Models in the form of sub-circuits using device model files already present in the eSim library. These IC models should be useful in the future for circuit designing purposes by developers and users, once they get successfully integrated into the eSim subcircuit Library.*

## 3.1 Approach

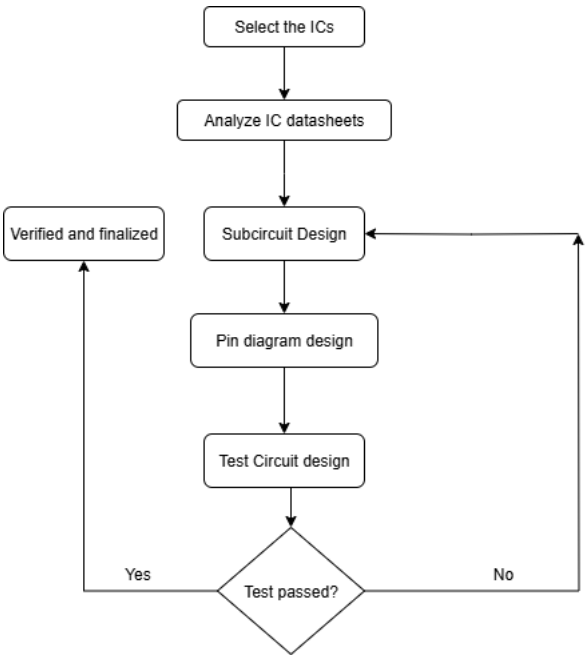



Figure 3.1: Flowchart of approach for designing IC models

Our approach to implementing the problem statement followed a structured methodology, leveraging datasheets from leading IC manufacturers such as Texas Instruments, Analog Devices, and NXP Semiconductors. We focused on selecting ICs with diverse functionalitiessuch as precision amplifiers, comparators, encoders,

and audio amplifiersand implemented them as subcircuits in eSim. The process was carried out in the following stages:

1. **Datasheet Analysis:** We began with a thorough review of datasheets for various analog and digital ICs to identify components not already available in the eSim library. This included analyzing internal schematics, truth tables, and component values to ensure the selected ICs provided unique or enhanced functionalities.

2. **Subcircuit Development:** Based on the datasheet specifications, we modeled the selected ICs as subcircuits in eSim using the available device model files. Special care was taken to replicate the pin configurations and symbols accurately, in alignment with official packaging and pin descriptions.

3. **Test Circuit Design:**We created test circuits for each subcircuit model to validate their functionality. These circuits were designed directly based on datasheet application examples, ensuring realistic and relevant testing.

4. **Simulation and Verification:**The test circuits were simulated using eSim and KiCad, generating NgSpice netlists and waveform outputs. We verified each subcircuit's behavior against expected results. In cases where discrepancies were found, we iteratively debugged and refined the designs until all test cases passed satisfactorily.

This rigorous process ensured the IC models were both accurate and reliable, contributing to the expansion of the eSim subcircuit library for future use in circuit design and simulation.

# Chapter 4

# SN74LS280

## 4.1 General Description

**9-Bit Odd/Even Parity Generators/Checkers**
The SN74LS280 is a monolithic, 9-bit parity generator/checker designed using Schottky-clamped TTL (Transistor-Transistor Logic) technology to deliver high-speed and reliable performance. Belonging to the 54LS/74LS series, the SN74LS280 strikes a balance between power efficiency and performance. It is widely used as a drop-in replacement to upgrade systems previously using the '180 parity checker/generator. Although it lacks dedicated expander inputs, its design compensates through specific pin configurationsparticularly the use of pin 4 and the unconnected pin 3which ensure functional compatibility with the older '180 devices. All inputs on the SN74LS280 are buffered to reduce loading requirements, ensuring compatibility with standard TTL logic levels and other TTL-based components.

## 4.2 Key Features

The key features of SN74LS280 includes:

- **9-Bit Parity Generation/Checking:**It has the ability to generate both odd and even parity outputs for nine data lines.
- **Cascadable:**The device supports easy expansion to larger word lengths by cascading multiple units.
- **Fast Delay:**It also offers a typical data-to-output delay of 33 ns.
- **Low Power Dissipation:**It has a typical power dissipation of 80 mW for the LS version.
- **Performance Upgrade:**It can be used to upgrade existing systems using MSI parity circuits.
- **Buffered Inputs:**The inputs are buffered, reducing the drive requirements to one LS unit load.

## 4.3 Application

The various applications of SN74LS280 are:

- **Data integrity:** It is primarily used in applications requiring parity generation or checking to ensure data integrity.
- **Memory Systems:** For error detection and correction in computer memory.
- **Data Communication:** In serial data transmission to detect errors in data streams.
- **Digital Systems:** As a component in digital circuits where parity checking is needed for various operations.
- **Upgrading Existing Systems:** Replacing older parity generator ICs with the SN74LS280 for improved performance and efficiency.

## 4.4 Pin Diagram

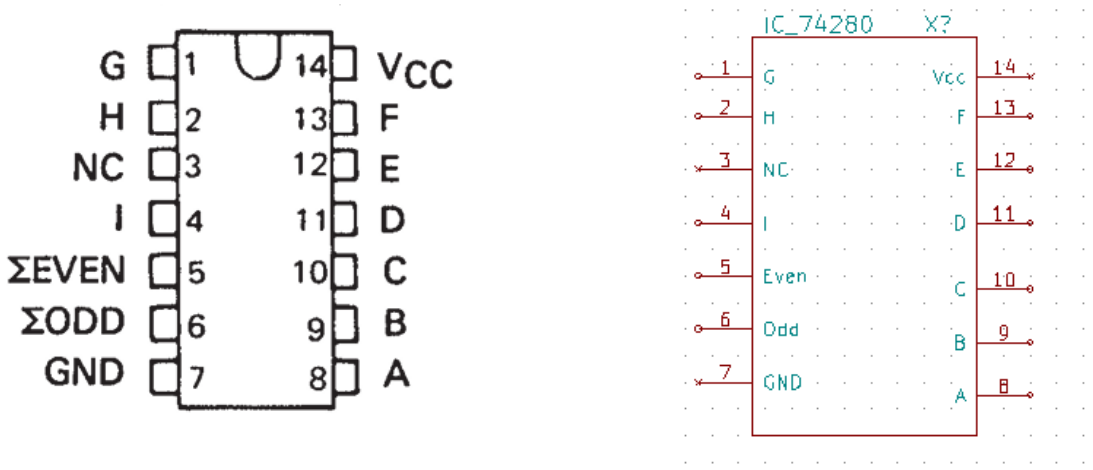



Figure 4.1: Pin diagram

## 4.5 Subcircuit Schematic Diagram

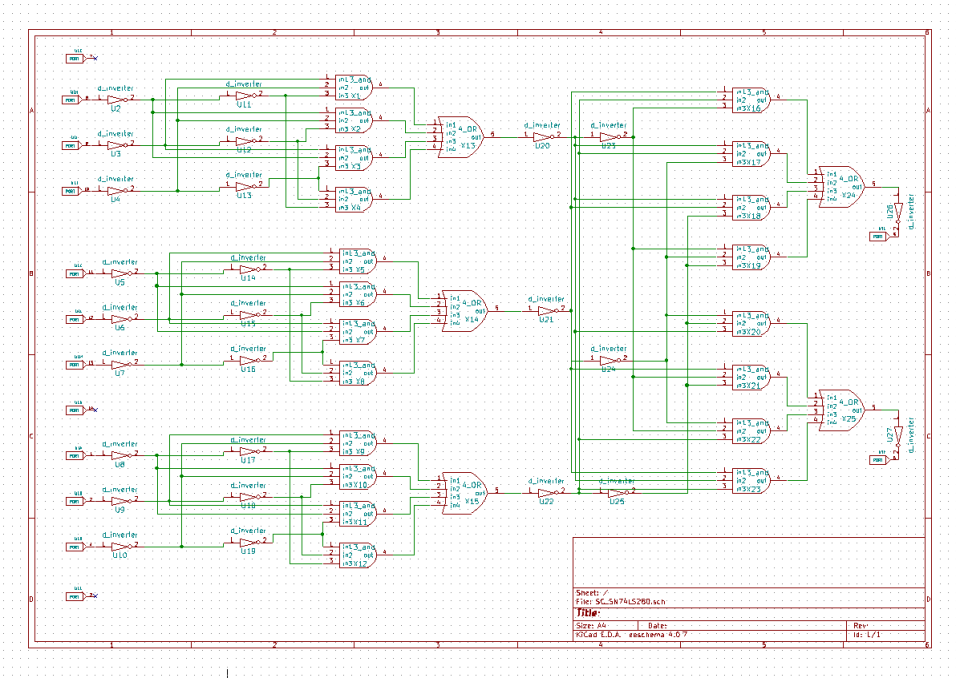


Figure 4.2: Subcircuit Schematic Diagram of SN74LS280

## 4.6 Test Circuit Schematic Diagram

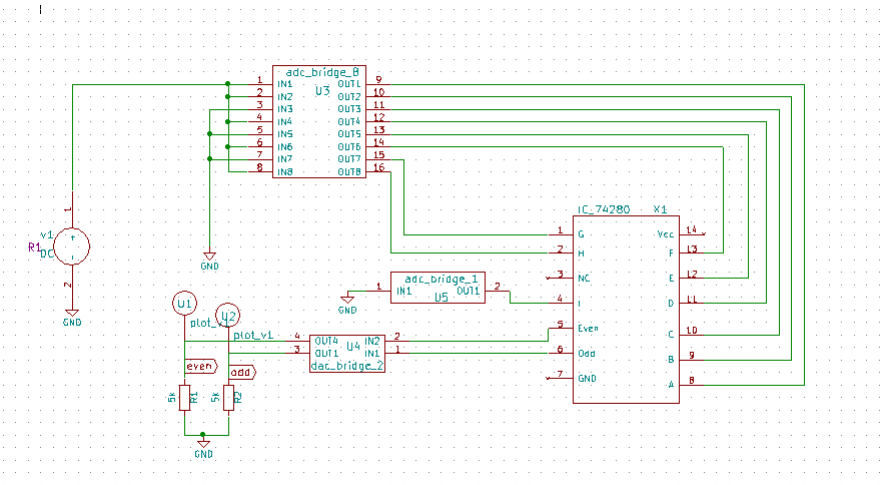



Figure 4.3: Test Circuit Schematic Diagram of SN74LS280

## 4.7 Analysis details

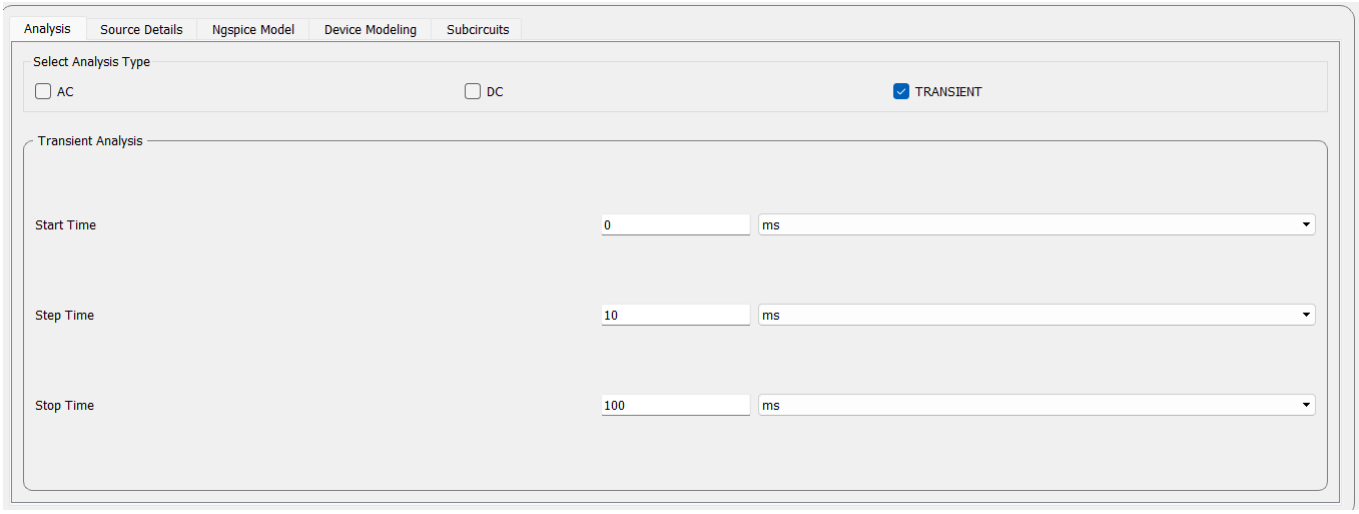



Figure 4.4: Analysis details of SN74LS280

## 4.8 Source Details


Figure 4.5: Source Details of SN74LS280

## 4.9 Inputs

**Input Bits : 110101010**

## 4.10 Outputs

**Output Bits : Even= 0; Odd = 1**

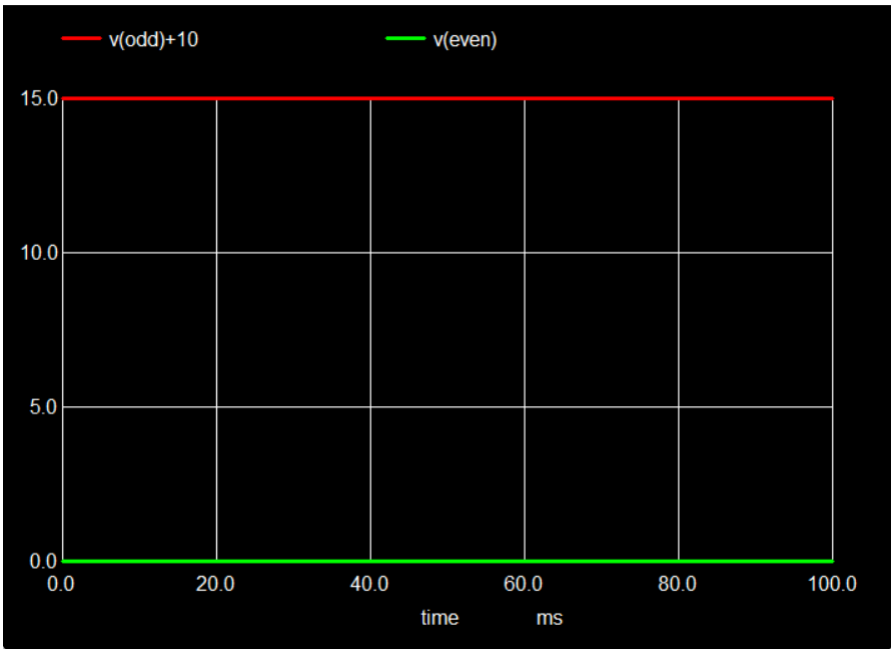



Figure 4.6: Output Plot of SN74LS280

# Chapter 5

# SN7480

## 5.1 General Description

**Gated Full Adders**
These single-bit, high-speed binary full adders feature gated complementary inputs and provide both complementary sum and inverted carry outputs. Designed for medium and high-speed, multi-bit, parallel-add or serial-carry applications, they utilize diode-transistor logic (DTL) for gated inputs and high-speed, high-fan-out transistor-transistor logic (TTL) for sum and carry outputs. Fully compatible with TTL logic families, the design includes a high-speed, Darlington-connected serial-carry circuit that reduces the need for extensive "look-ahead" and carry-cascading logic.

## 5.2 Key Features

The key features of SN7480 includes:

- **Gated Inputs:**The SN7480 has gated complementary inputs, allowing for more control over the addition process.
- **Complementary Sum Outputs:**It provides two sum outputs which are complementary, offering flexibility in circuit design.
- **Inverted Carry Output:**The carry output is inverted, which is a common convention in some adder architectures.
- **High-Speed Operation:**It is designed for medium-to-high-speed applications, enabling faster calculations in digital systems.

## 5.3 Application

The applications of SN7480 includes:

- **Parallel Adders:**The SN7480 is primarily used as a building block for creating larger, parallel adders in digital circuits.

- **Arithmetic Logic Units (ALUs):**It can be used within ALUs, which are fundamental components of microprocessors and other digital systems performing arithmetic and logical operations.
- **Digital Signal Processing (DSP):**In DSP applications, where fast calculations are crucial, the SN7480 can be employed for operations involving addition.
- **Control Systems:**It can be integrated into control systems where precise and fast arithmetic operations are necessary.

## 5.4 Pin Diagram

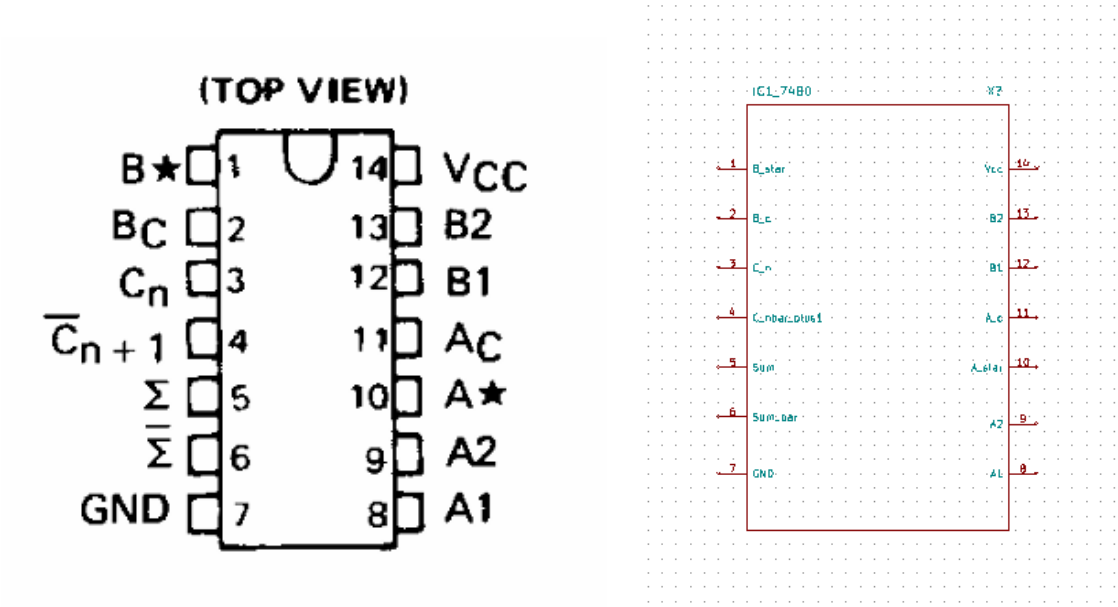



Figure 5.1: Pin diagram of SN7480

## 5.5 Subcircuit Schematic Diagram

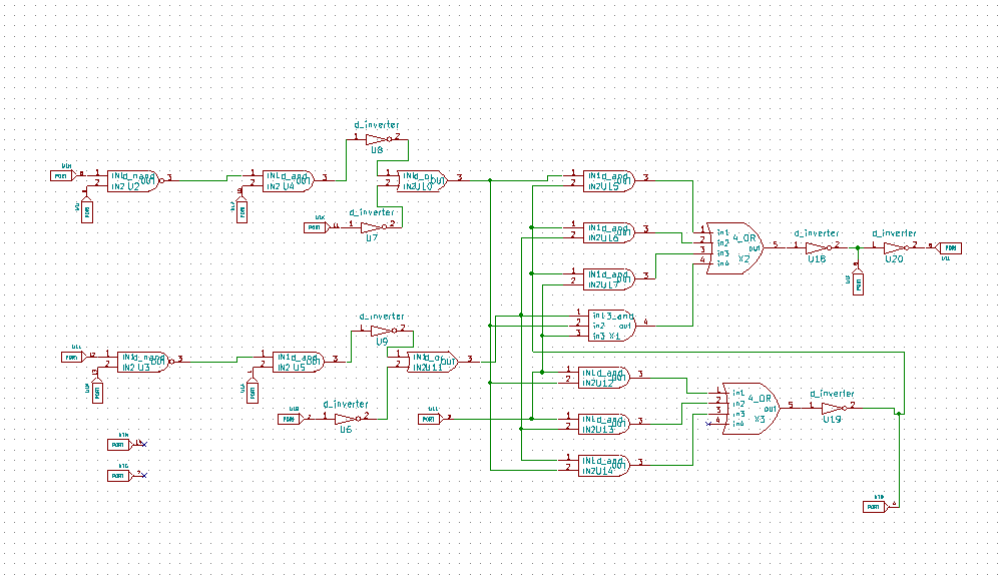


Figure 5.2: Subcircuit Schematic Diagram of SN7480

## 5.6 Test Circuit Schematic Diagram

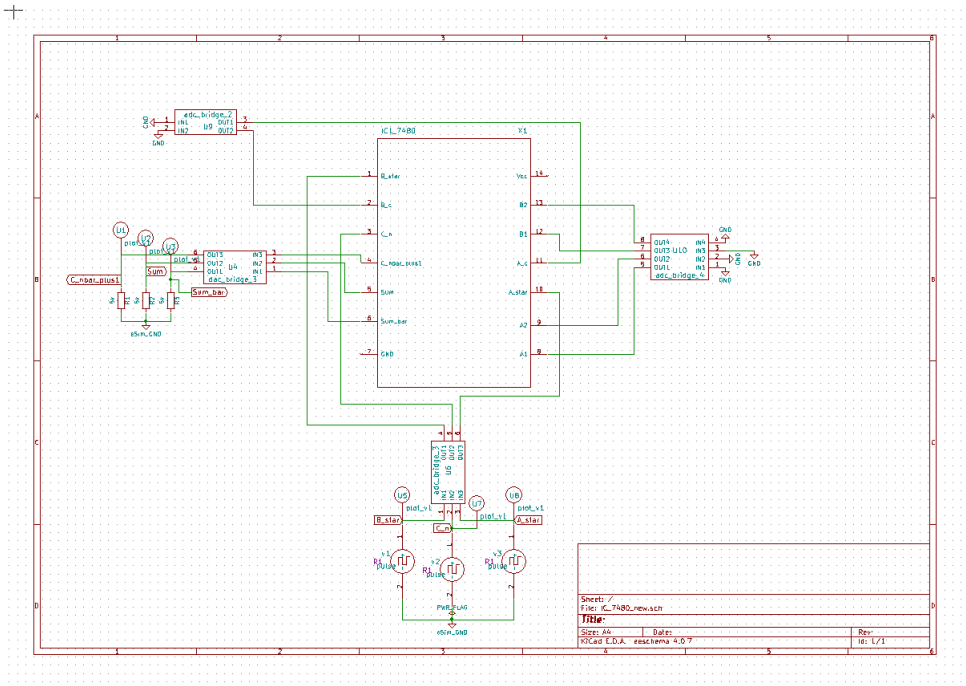


Figure 5.3: Test Circuit Schematic Diagram of SN7480

## 5.7 Analysis details

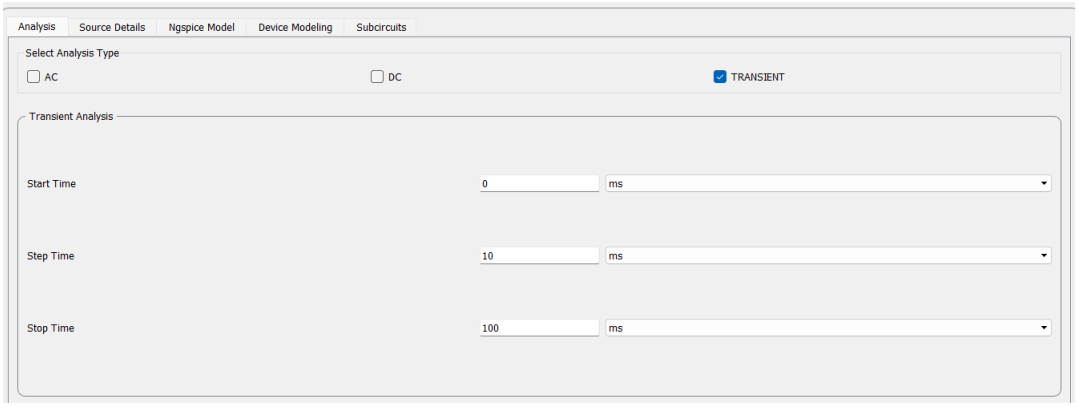



Figure 5.4: Analysis details of SN74280

## 5.8 Source Details

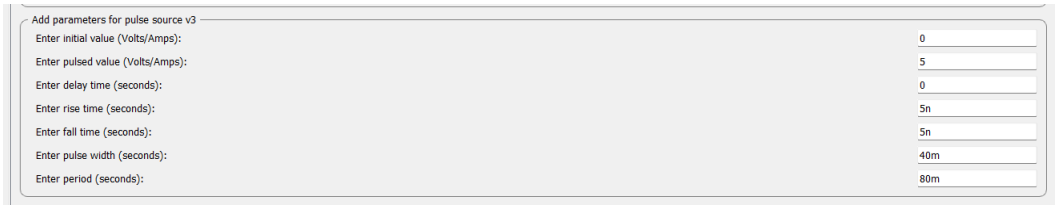




Figure 5.5: Source Details of SN7480

## 5.9 Input Plots

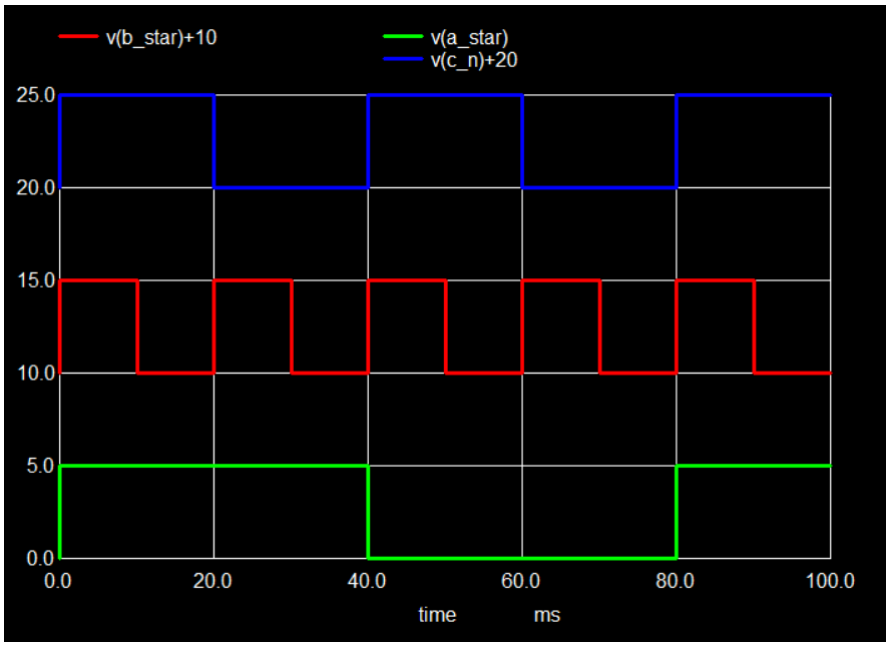



Figure 5.6: Input Plot of SN7480

## 5.10 Output Plots

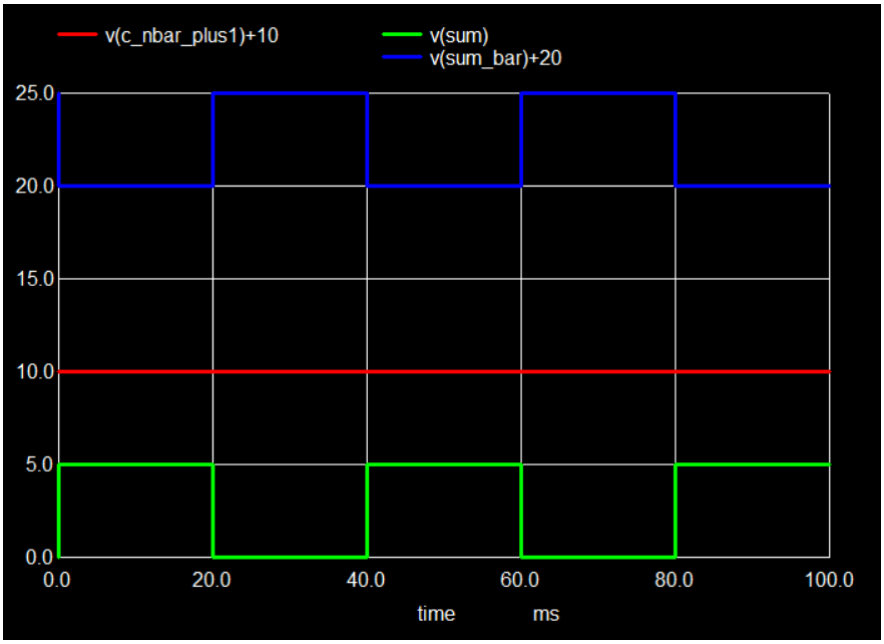



Figure 5.7: Output Plot of SN7480

# Chapter 6

# MC74HC595A

## 6.1 General Description

**8-Bit Serial-Input/Serial or Parallel-Output Shift Register with Latched 3-State Output**
The MC74HC595A is an 8-bit shift register with an integrated 8-bit D-type latch and three-state parallel outputs. It accepts serial data input and provides both serial and parallel outputs, with independent clock controls for the shift register and latch. The device includes an asynchronous reset for the shift register and is designed to interface directly with SPI-compatible CMOS microprocessors and microcontrollers.The MC74HC595A device inputs are compatible Standard CMOS outputs; with pullup resistors, they are compatible with TTL outputs.

## 6.2 Key Features

The key features of MC74HC595A includes:

- **High Output Drive Capability:**The device can drive up to 15 LSTTL loads, making it suitable for controlling multiple logic inputs simultaneously.
- **Wide Output Compatibility:**Its outputs are directly compatible with CMOS, NMOS, and TTL logic families, eliminating the need for additional interfacing components.
- **Operating Voltage Range:**The MC74HC595A operates between 2.0 V and 6.0 V.
- **Low Input Current:**The device features a low input current of just 1.0 A, which contributes to overall energy efficiency.
- **High Noise Immunity:**Designed with CMOS characteristics, the device offers excellent noise immunity for stable performance in noisy environments.
- **Reduced Power Consumption:**The quiescent power consumption is reduced by 50 percent, making the device more energy efficient.

## 6.3 Application

The applications of MC74HC595A includes:

- **Expanding Microcontroller I/O:** It allows us to control many more output pins than our microcontroller might have directly available.
- **Controlling LED Displays:**It is ideal for driving multiple LEDs, including segmented displays, matrix displays, and even creating LED animations.
- **Interfacing with SPI Devices:**It can directly interface with the SPI serial data port on many microcontrollers.
- **Digital Clocks and Timers:** It can be used to display time or time intervals.

## 6.4 Pin Diagram

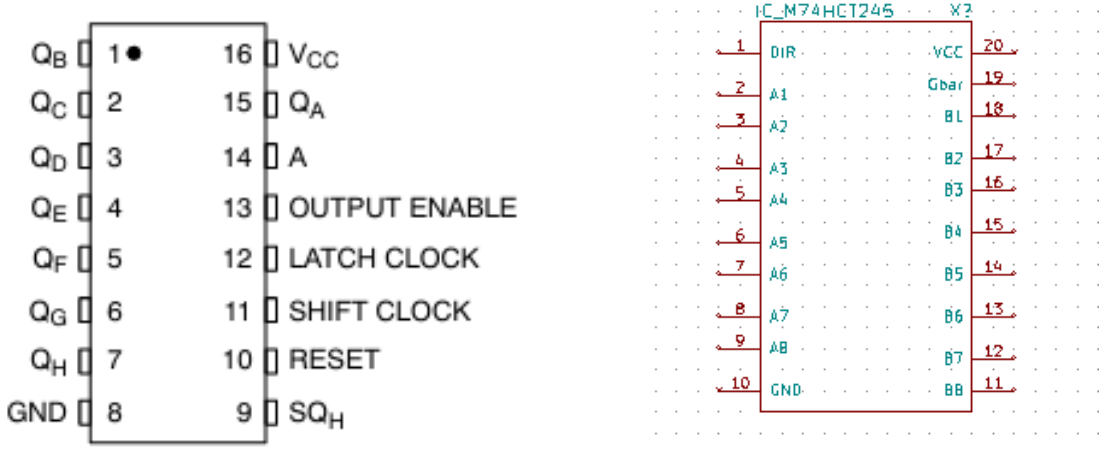



Figure 6.1: Pin diagram of MC74HC595A

## 6.5 Subcircuit Schematic Diagram

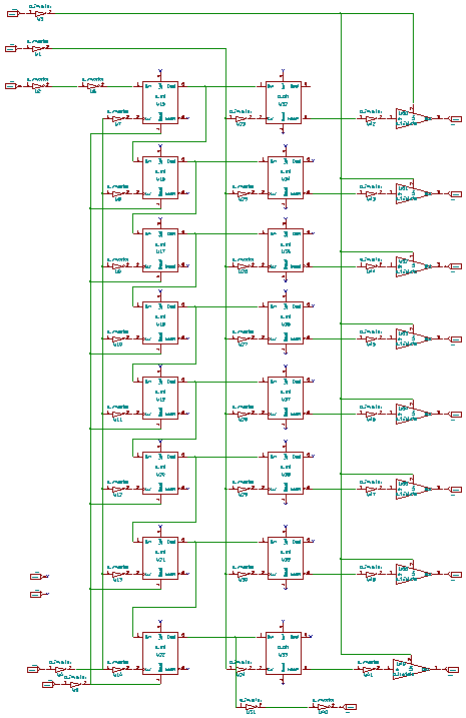


Figure 6.2: Subcircuit Schematic Diagram of MC74HC595A

## 6.6 Test Circuit Schematic Diagram

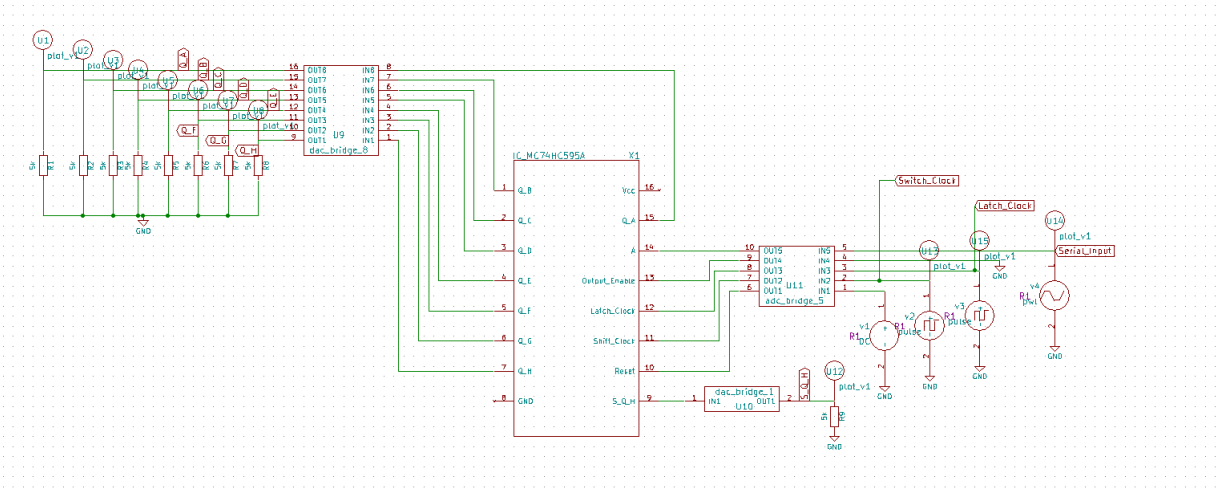



Figure 6.3: Test Circuit Schematic Diagram of MC74HC595A

## 6.7 Analysis details

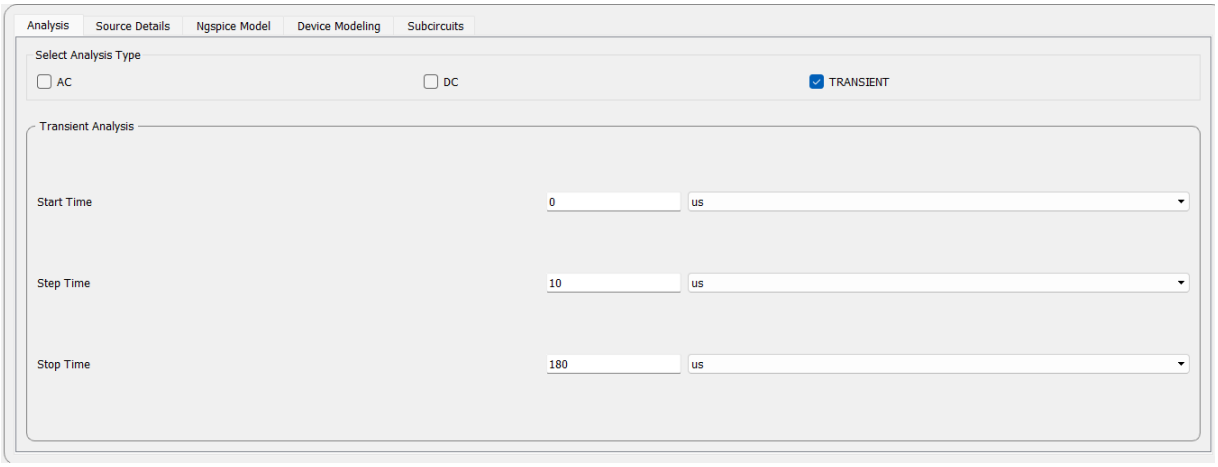
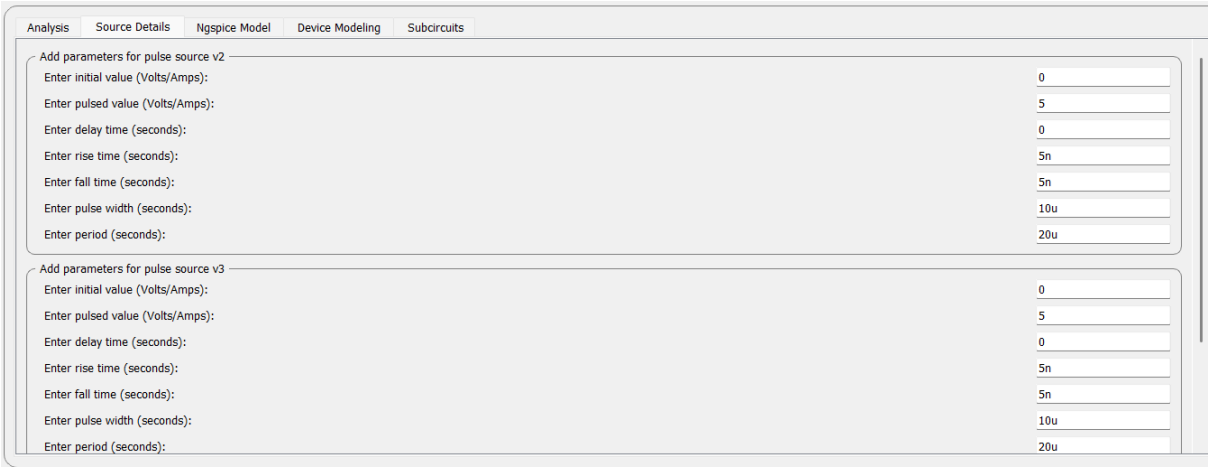



Figure 6.4: Analysis details of MC74HC595A

## 6.8 Source Details



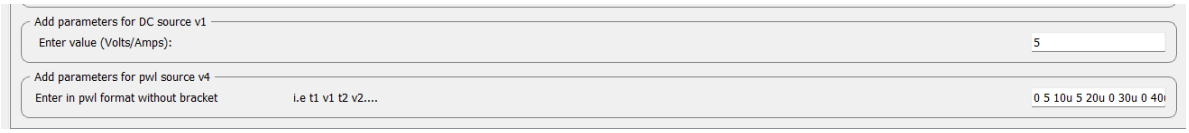




Figure 6.5: Source Details of MC74HC595A

## 6.9 Input Plots

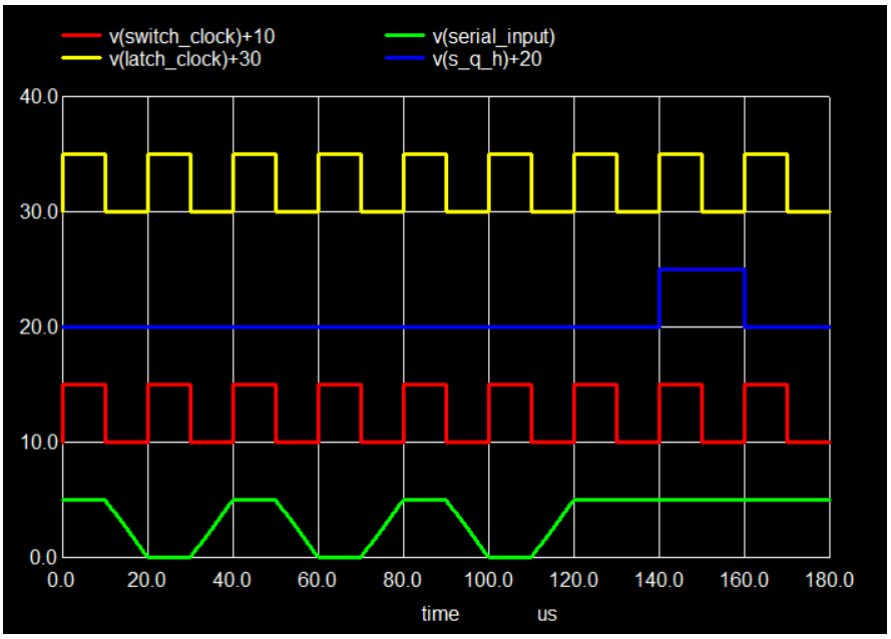



Figure 6.6: Input Plot of MC74HC595A

## 6.10 Output Plots

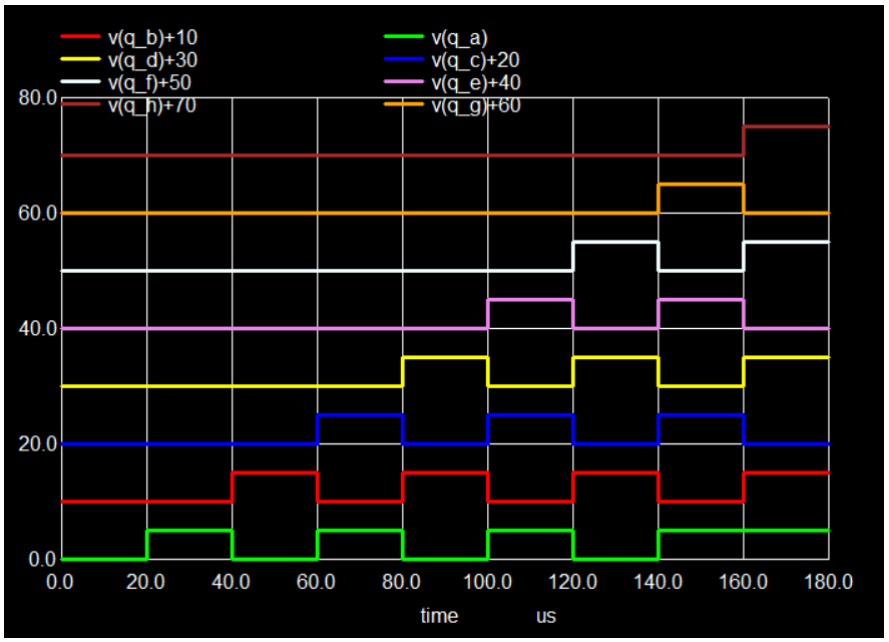



Figure 6.7: Output Plot of MC74HC595A

# Chapter 7

# 74HC4017

## 7.1 General Description

**Johnson decade counter with 10 decoded outputs**
The 74HC4017 is a 5-stage Johnson decade counter featuring 10 fully decoded outputs (Q0 to Q9) and an output from the most significant flip-flop (Qbar5-9). It includes two clock inputs (CP0 and CP1) and an asynchronous master reset (MR) that overrides the clock and resets the counter to its initial state. The device advances the count on a LOW-to-HIGH transition at CP0 while CP1 is LOW or on a HIGH-to-LOW transition at CP1 while CP0 is HIGH, allowing flexible clock control. An internal correction mechanism ensures the counter returns to a valid sequence within 11 clock pulses after an illegal state. Input clamp diodes allow interfacing with higher voltage signals using series current-limiting resistors.

## 7.2 Key Features

The key features of 74HC4017 includes:

- **Wide Supply Voltage Range:** The device operates over a broad voltage range from 2.0 V to 6.0 V, making it suitable for various low and high voltage applications.
- **Low Power Dissipation:** Built using CMOS technology, the device ensures minimal power consumption during operation.
- **High Noise Immunity:** It exhibits strong resistance to electrical noise, ensuring reliable performance in noisy environments.
- **Input Logic Level Compatibility:** The 74HC4017 supports CMOS logic levels.
- **Extended Temperature Range:** It is specified for operation across two industrial temperature ranges: 40C to +85C and 40C to +125C, making it suitable for harsh environments.

## 7.3 Application

The applications of 74HC4017 includes:

- **LED Control:** Sequentially lighting up LEDs in a pattern, like a running light or a visual counter.
- **Sequential Switching:** Activating different circuits or components in a specific order.
- **Frequency Division:** Dividing a clock signal by a factor of 10.
- **Digital Displays:** Driving the segments of a 7-segment display (with additional decoding).

## 7.4 Pin Diagram

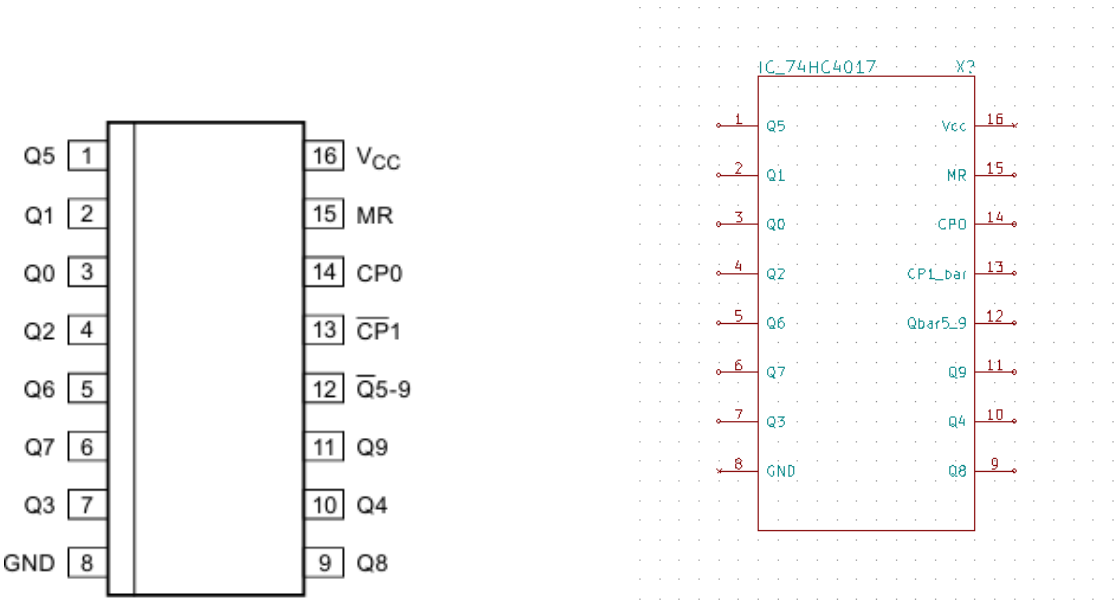



Figure 7.1: Pin diagram of 74HC4017

## 7.5 Subcircuit Schematic Diagram

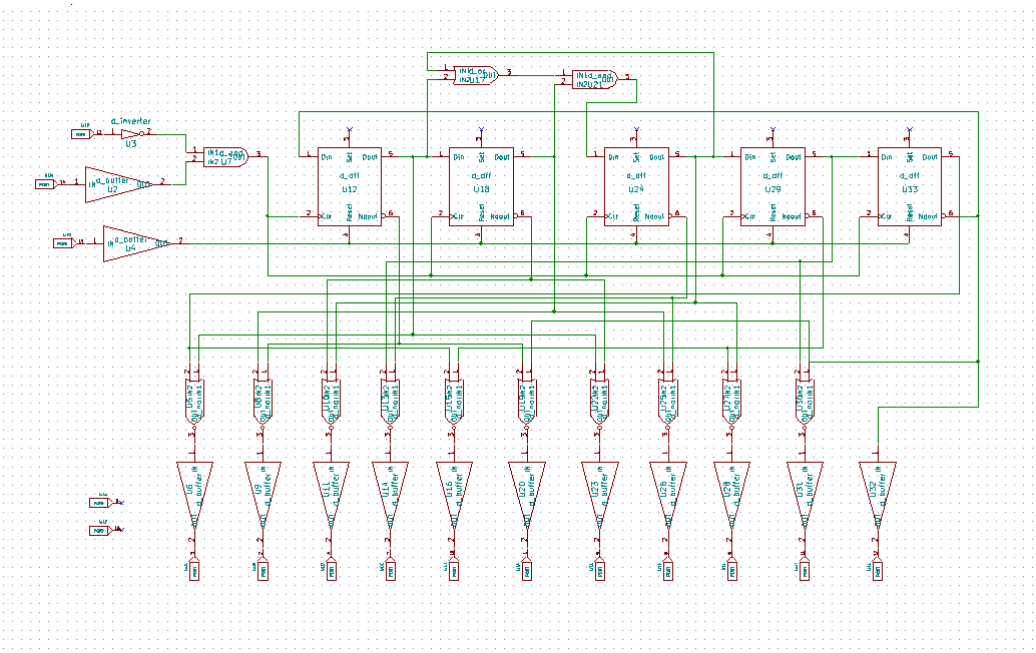


Figure 7.2: Subcircuit Schematic Diagram of 74HC4017

## 7.6 Test Circuit Schematic Diagram

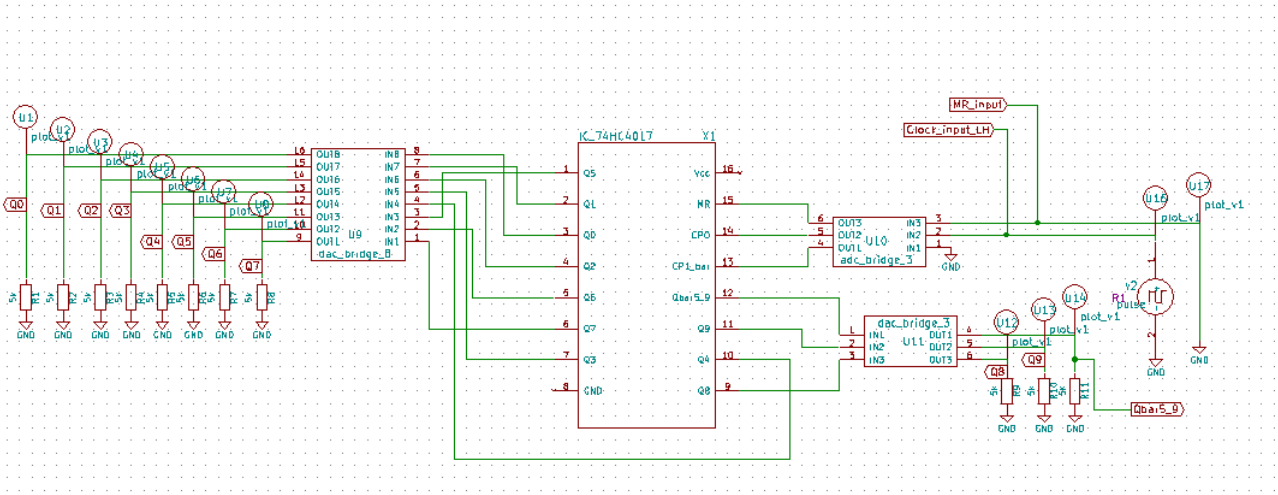


Figure 7.3: Test Circuit Schematic Diagram of 74HC4017

## 7.7 Analysis details

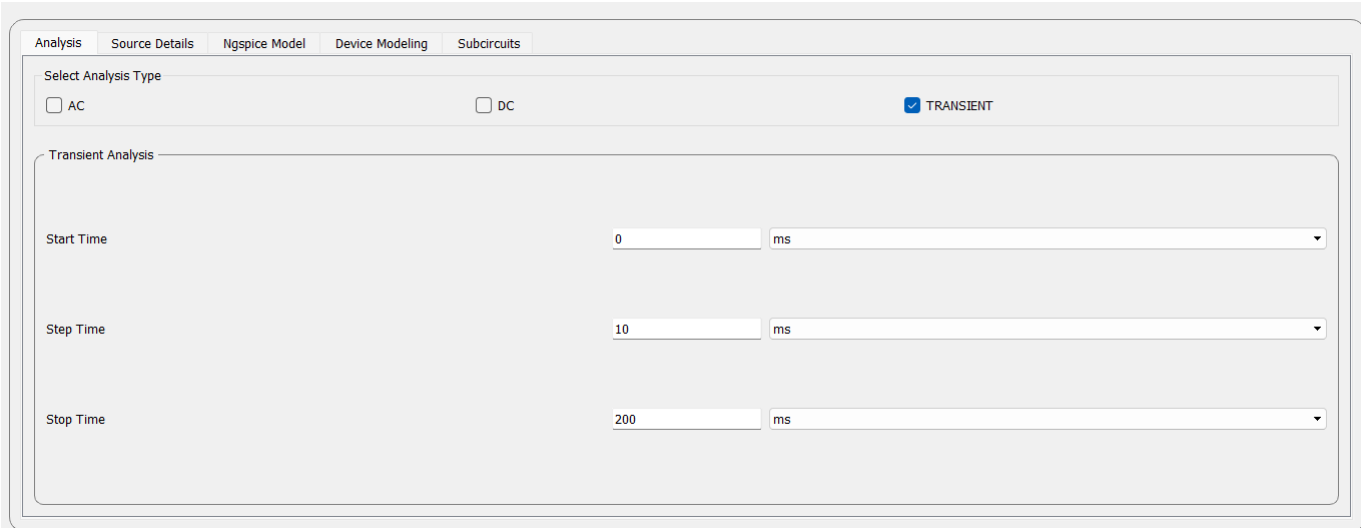



Figure 7.4: Analysis details of 74HC4017

## 7.8 Source Details


Figure 7.5: Source Details of 74HC4017

## 7.9 Input Plots

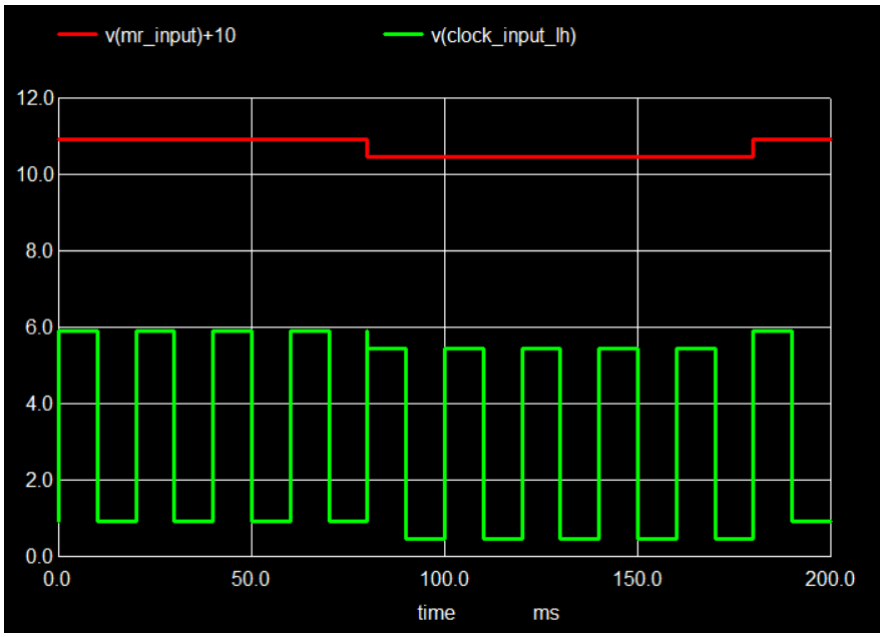



Figure 7.6: Input Plot of 74HC4017

## 7.10 Output Plots

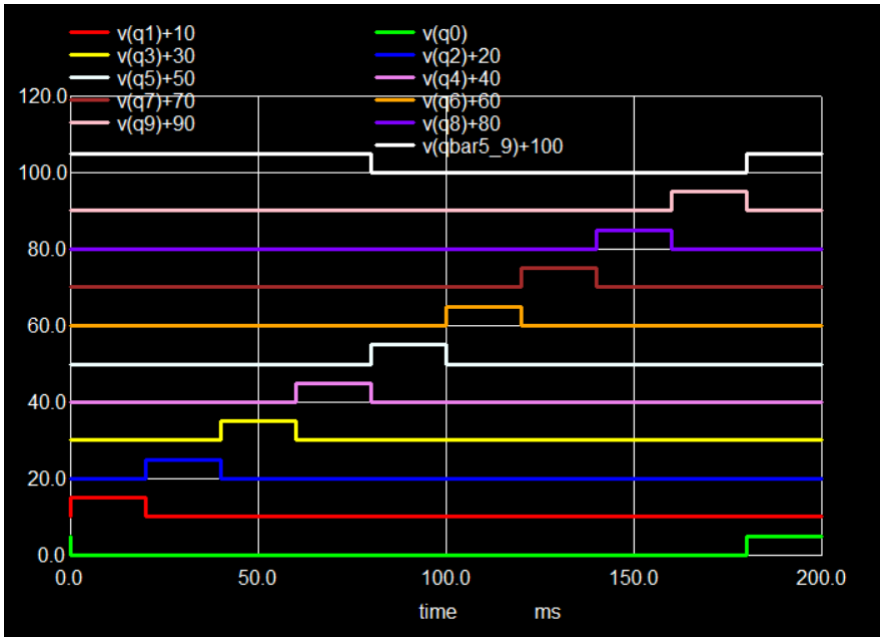



Figure 7.7: Output Plot of 74HC4017

# Chapter 8

# CD4022B

## 8.1 General Description

**Octal Counter with 8 Decoded Outputs**
The CD4022B is a CMOS-based octal counter/divider that provides 8 decoded outputs using a 4-stage Johnson counter configuration. It advances one count on each positive clock edge when the CLOCK INHIBIT input is low. If the CLOCK INHIBIT is high, counting is disabled, and the counter holds its state. A high RESET signal clears the counter to zero, restarting the sequence. Each decoded output goes high one at a time in a fixed sequence, staying high for one full clock cycle before moving to the next, thus enabling divide-by-8 functionality. Additionally, a CARRY-OUT output is provided for cascading with other counters. The Johnson counter configuration allows high-speed operation, 2-input decode-gating and spike-free decoded outputs. The anti-lock gating provided assures proper counting sequence.

## 8.2 Key Features

The key features of CD4022B includes:

- **Fully Static Operation:** The device operates without the need for continuous clocking, making it power-efficient and suitable for low-frequency applications.
- **Medium-Speed Operation:** Typical operating speed is 10 MHz at Vdd = 10 V, allowing use in moderately fast digital systems.
- **Standardized, Symmetrical Output Characteristics:** It ensures consistent and reliable output levels across all stages, simplifying interfacing with other logic devices.
- **Tested for Quiescent Current at 20 V:** Each unit is 100 percent tested to ensure minimal power consumption in the idle state even at high voltage levels.

- **Wide Voltage Range Compatibility:** It supports 5 V, 10 V, and 15 V operation, making it versatile for various logic-level environments.

## 8.3 Application

The applications of CD4022B includes:

- **LED Displays and Sequencing:** The decoded outputs can be used to control a sequence of LEDs or other indicators.
- **Counter Control and Timer Circuits:** The CD4022B is useful in applications requiring precise counting and timing.
- **Frequency Division:** It can be used to divide a clock signal frequency by a factor of eight.

## 8.4 Pin Diagram

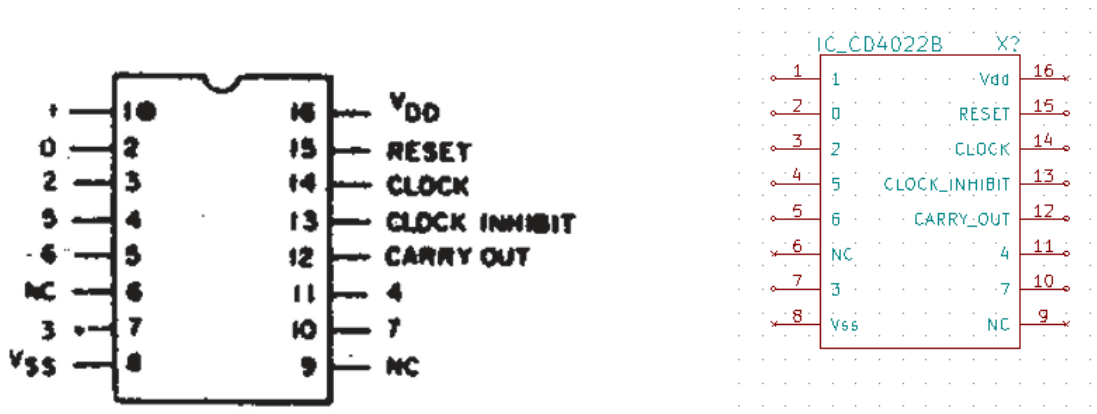



Figure 8.1: Pin diagram of CD4022B

## 8.5 Subcircuit Schematic Diagram

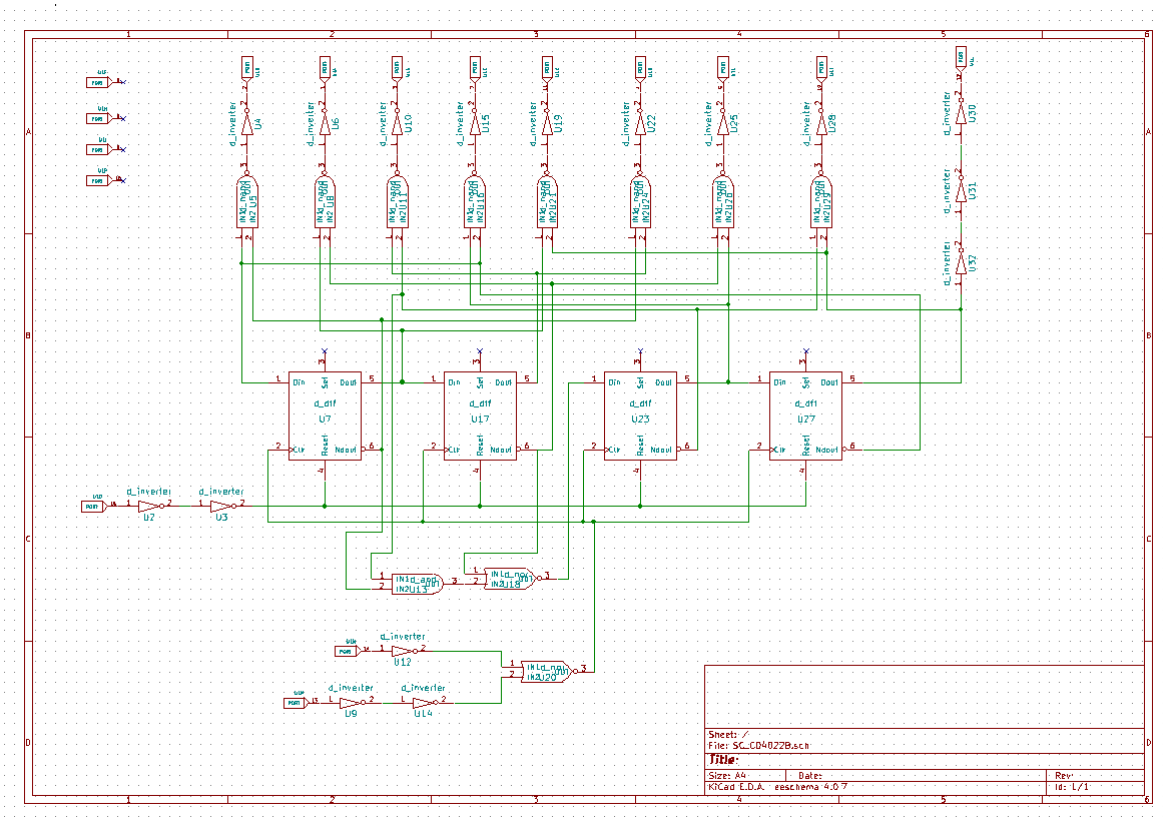



Figure 8.2: Subcircuit Schematic Diagram of CD4022B

## 8.6 Test Circuit Schematic Diagram

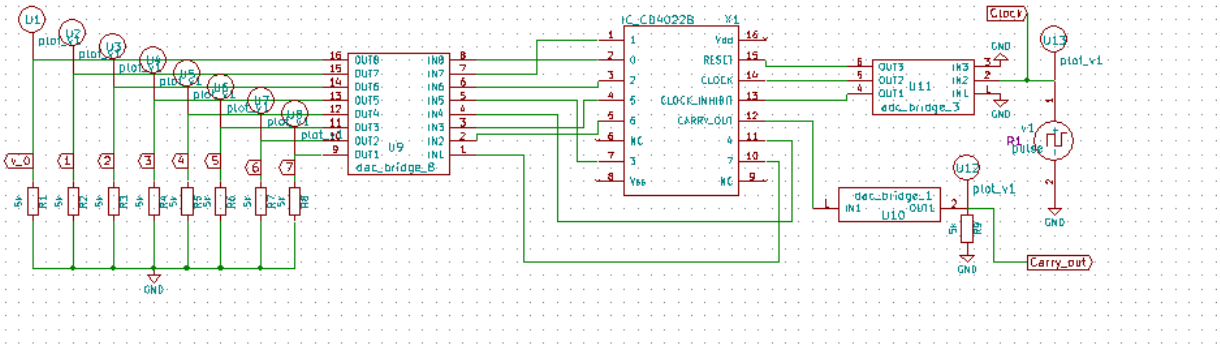



Figure 8.3: Test Circuit Schematic Diagram of CD4022B

## 8.7 Analysis details

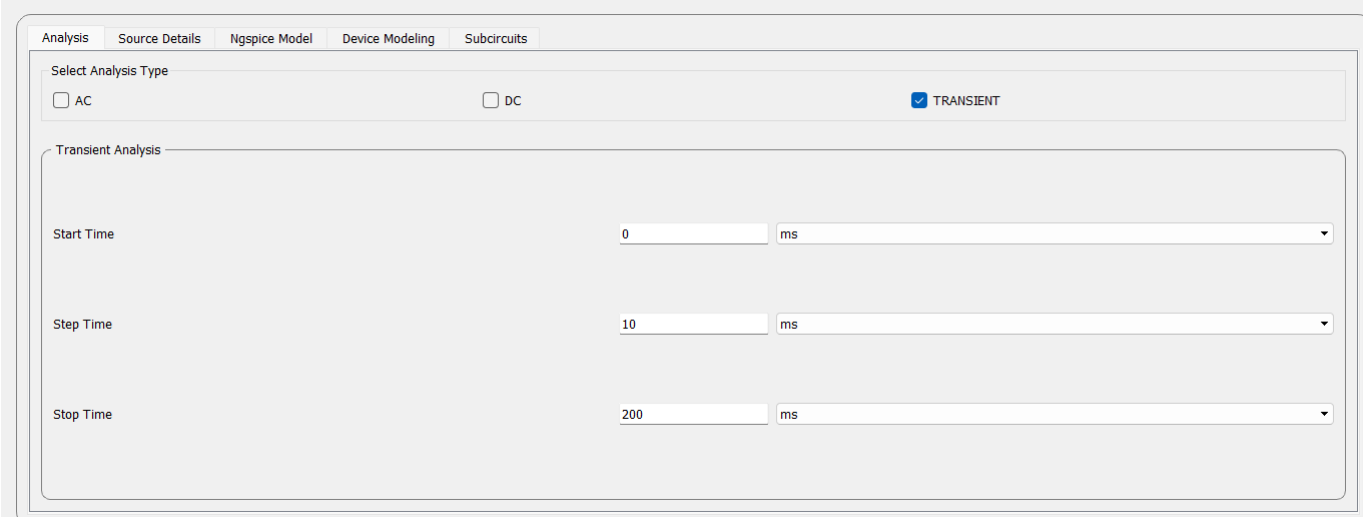



Figure 8.4: Analysis details of CD4022B

## 8.8 Source Details


Figure 8.5: Source Details of CD4022B

## 8.9 Input Plots

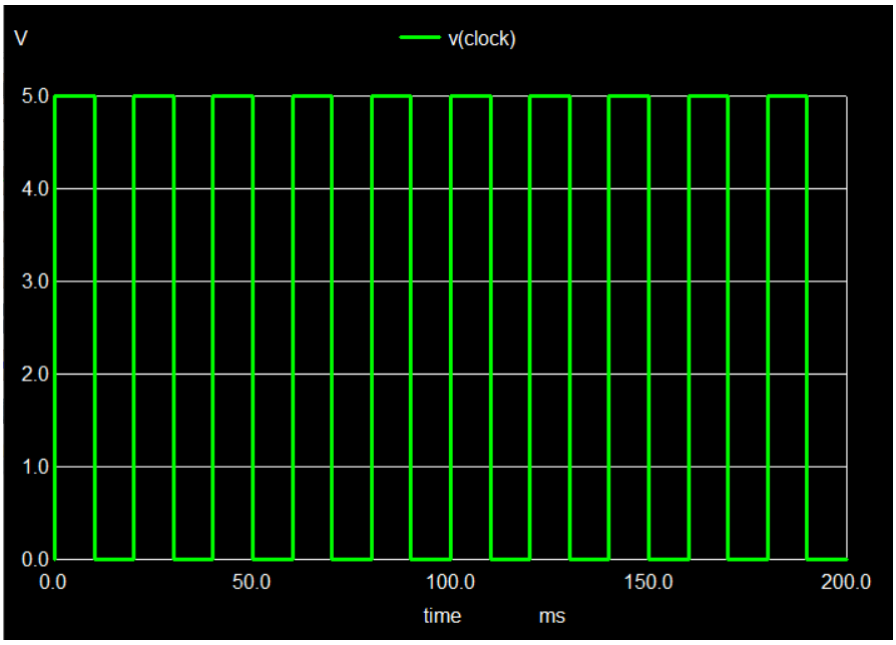



Figure 8.6: Input Plot of CD4022B

## 8.10 Output Plots

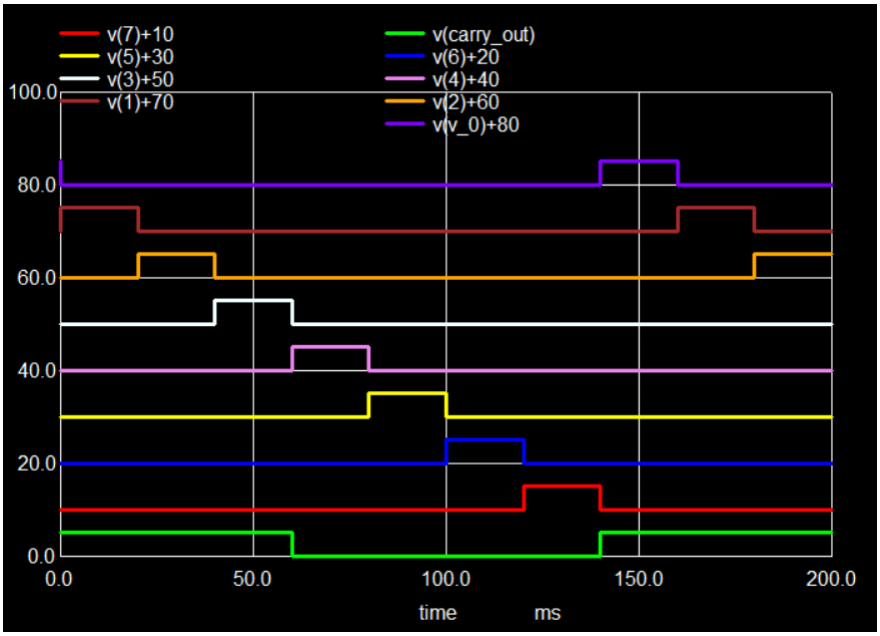



Figure 8.7: Output Plot of CD4022B

# Chapter 9

# SN74LS670

## 9.1 General Description

**4-By-4 Register Files With 3-State Outputs**
The SN74LS670 is a 16-bit TTL register file designed using MSI (Medium Scale Integration) technology, incorporating the equivalent of 98 gates. It is organized as four 4-bit words with separate on-chip decoding for efficient addressing of each word location, enabling simultaneous reading from one location and writing to another. Data is written via four data inputs, with the target word selected using write address inputs $W_A$ and $W_B$, and controlled by the write-enable signal $\overline{G_W}$; data is stored only if both internal write address gates are high. If $\overline{G_W}$ is high, the inputs are inhibited, preventing changes. Reading is performed using separate address inputs $R_A$ and $R_B$, and enabled by the read-enable signal $\overline{G_R}$; when $\overline{G_R}$ is high, outputs go into a high-impedance state. The register supports nondestructive readout, ensuring data integrity during access. Its designseparating data-entry and read addressing with individual sense lineseliminates recovery time and permits simultaneous read/write operations with typical write and read times of 27 ns and 24 ns, respectively. High-speed three-state outputs and AND-OR-INVERT decoding logic allow these registers to be bus-connected and expanded up to 512 words using up to 128 devices.

## 9.2 Key Features

The key features of SN74LS670 includes:

- **Separate Read/Write Addressing:** This allows for concurrent read and write operations, improving performance in various applications.
- **Fast Access Times:** Typically around 20ns, it enables quick data retrieval.
- **Expandable:** The SN74LS670 can be combined with other units to create larger memory arrays (up to 512 words of n-bits).
- **4x4 Organization:** The device contains four registers, each with a 4-bit capacity.

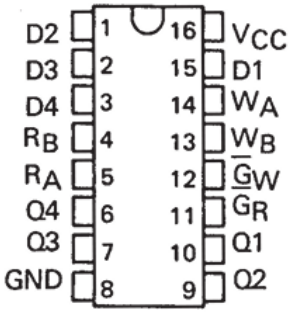
- **3-State Outputs:** These outputs allow multiple devices to share the same data bus, making it suitable for bus-oriented systems.
- **Temperature range:** The SN74LS670 operates within a temperature range of 0C to 70C.

## 9.3 Application

The applications of SN74LS670 includes:

- **Scratch-Pad Memory:** It provides temporary storage for data during calculations or processing.
- **Buffer Storage:** It can act as a buffer between different processing units or data sources.
- **Bit Storage in Fast Multiplication:** It can be used to store intermediate results in fast multiplication circuits.

## 9.4 Pin Diagram



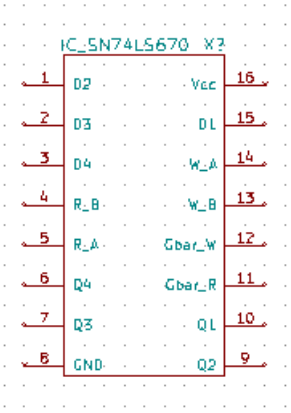




Figure 9.1: Pin diagram of SN74LS670

## 9.5 Subcircuit Schematic Diagram

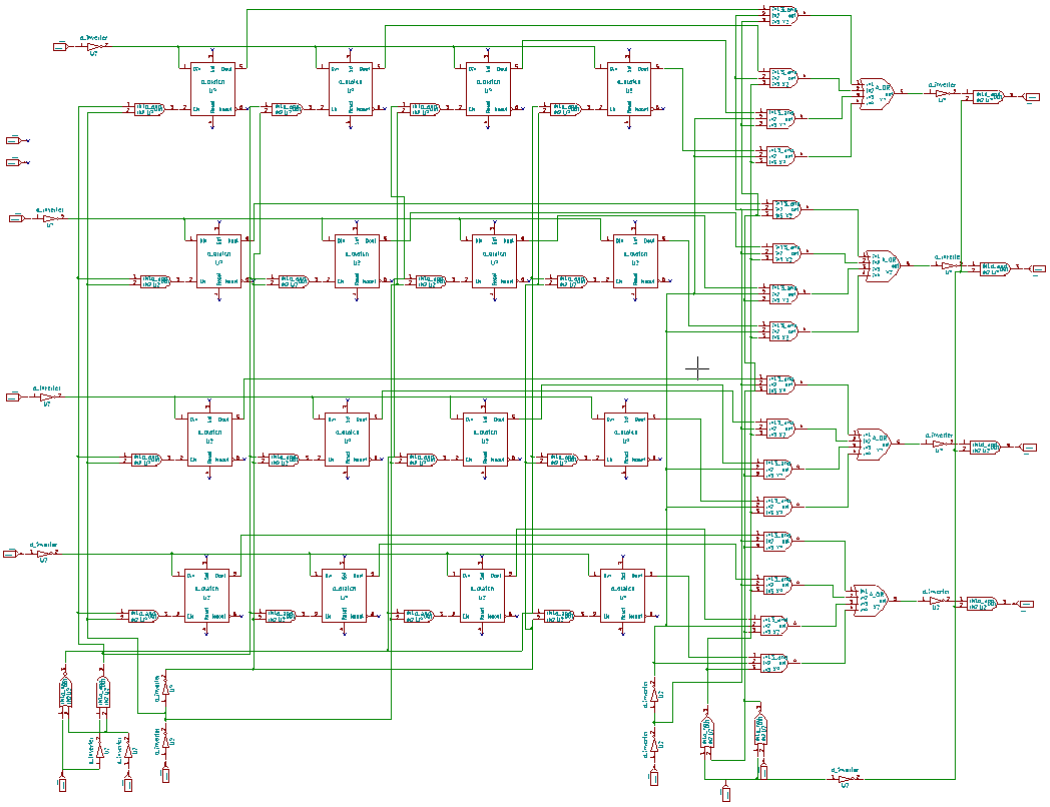


Figure 9.2: Subcircuit Schematic Diagram of SN74LS670

## 9.6 Test Circuit Schematic Diagram

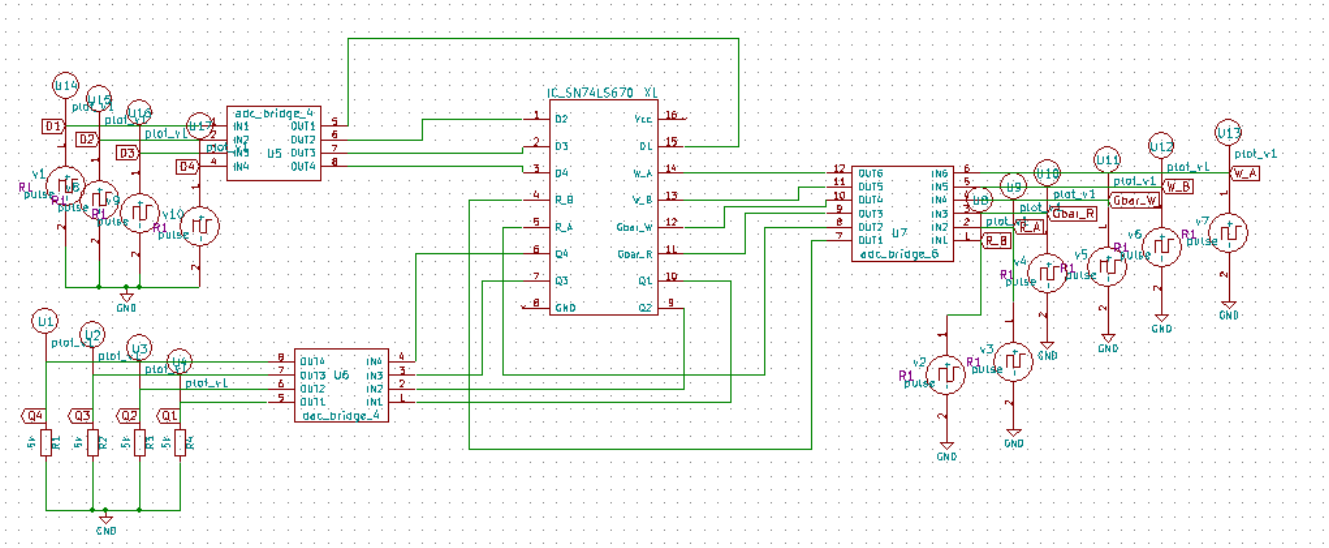



Figure 9.3: Test Circuit Schematic Diagram of SN74LS670

## 9.7 Analysis details

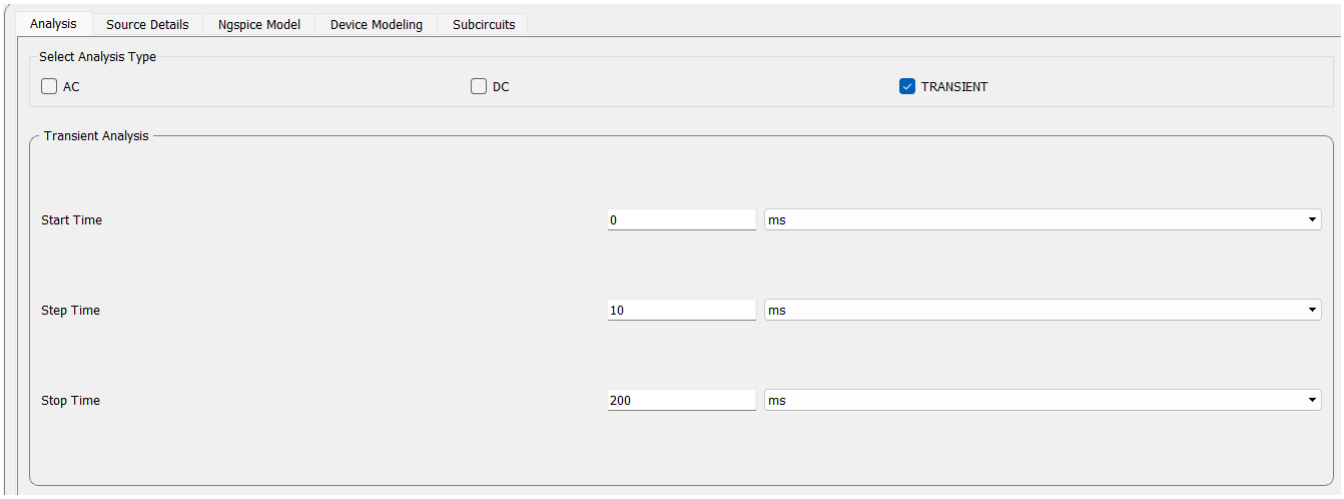
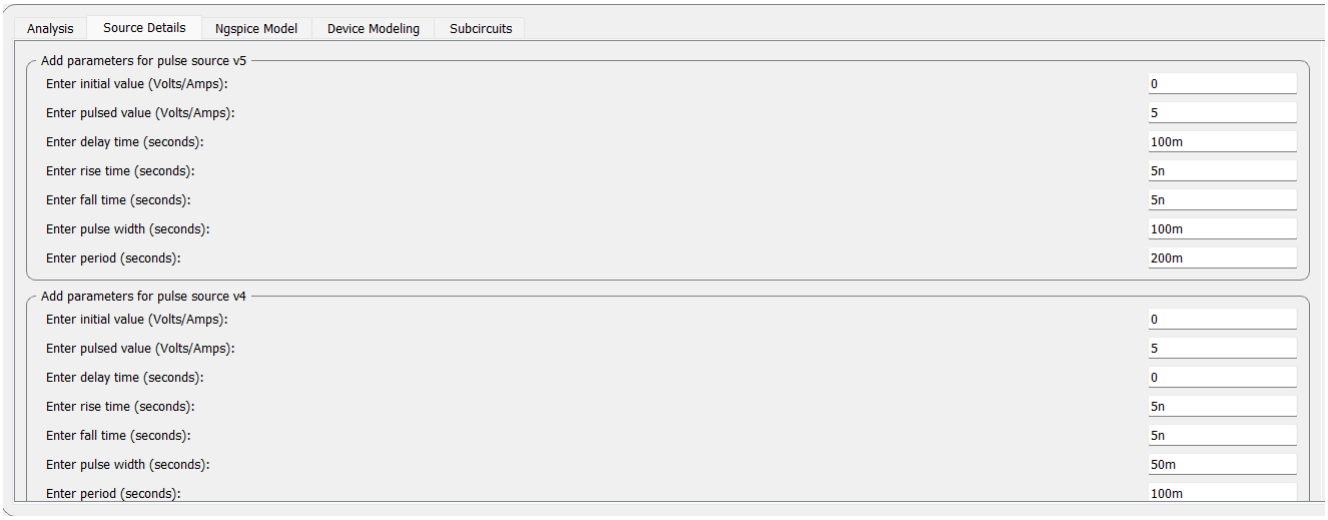



Figure 9.4: Analysis details of SN74LS670

## 9.8 Source Details




Analysis
Source Details
Ngspice Model
Device Modeling
Subcircuits
Add parameters for pulse source v7
Enter initial value (Volts/Amps): 0
Enter pulsed value (Volts/Amps): 5
Enter delay time (seconds): 0
Enter rise time (seconds): 5n
Enter fall time (seconds): 5n
Enter pulse width (seconds): 50m
Enter period (seconds): 100m
Add parameters for pulse source v6
Enter initial value (Volts/Amps): 0
Enter pulsed value (Volts/Amps): 5
Enter delay time (seconds): 50m
Enter rise time (seconds): 5n
Enter fall time (seconds): 5n
Enter pulse width (seconds): 50m
Enter period (seconds): 100m


Analysis
Source Details
Ngspice Model
Device Modeling
Subcircuits
Add parameters for pulse source v3
Enter initial value (Volts/Amps): 0
Enter pulsed value (Volts/Amps): 5
Enter delay time (seconds): 100m
Enter rise time (seconds): 5n
Enter fall time (seconds): 5n
Enter pulse width (seconds): 100m
Enter period (seconds): 200m
Add parameters for pulse source v2
Enter initial value (Volts/Amps): 0
Enter pulsed value (Volts/Amps): 5
Enter delay time (seconds): 200m
Enter rise time (seconds): 5n
Enter fall time (seconds): 5n
Enter pulse width (seconds): 100m
Enter period (seconds): 200m


Analysis
Source Details
Ngspice Model
Device Modeling
Subcircuits
Add parameters for pulse source v1
Enter initial value (Volts/Amps): 0
Enter pulsed value (Volts/Amps): 5
Enter delay time (seconds): 0
Enter rise time (seconds): 5n
Enter fall time (seconds): 5n
Enter pulse width (seconds): 100m
Enter period (seconds): 200m
Add parameters for pulse source v8
Enter initial value (Volts/Amps): 0
Enter pulsed value (Volts/Amps): 5
Enter delay time (seconds): 100m
Enter rise time (seconds): 5n
Enter fall time (seconds): 5n
Enter pulse width (seconds): 100m
Enter period (seconds): 200m

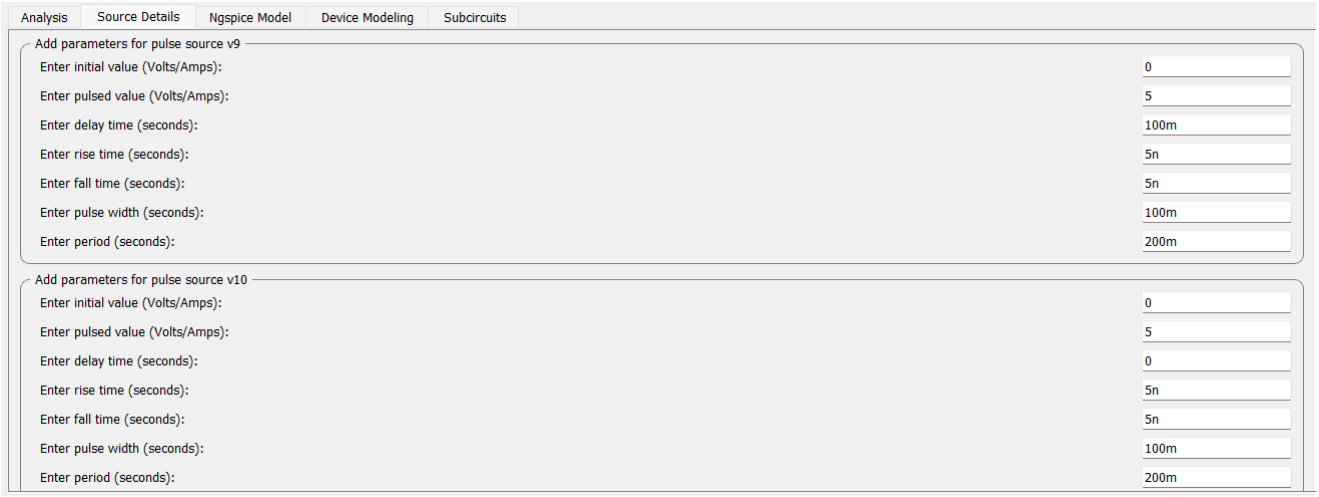



Figure 9.5: Source Details of SN74LS670

## 9.9 Input Plots

**Test condition : Read operation for 0-100ms and Write operation for 100-200ms**

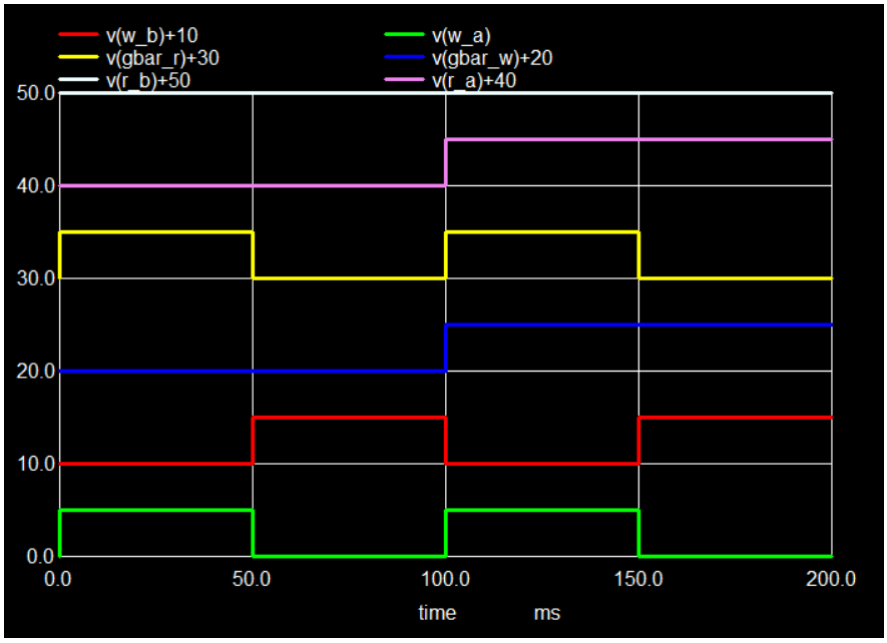



Figure 9.6: Input Plot 1 of SN74LS670 (Control Signals)

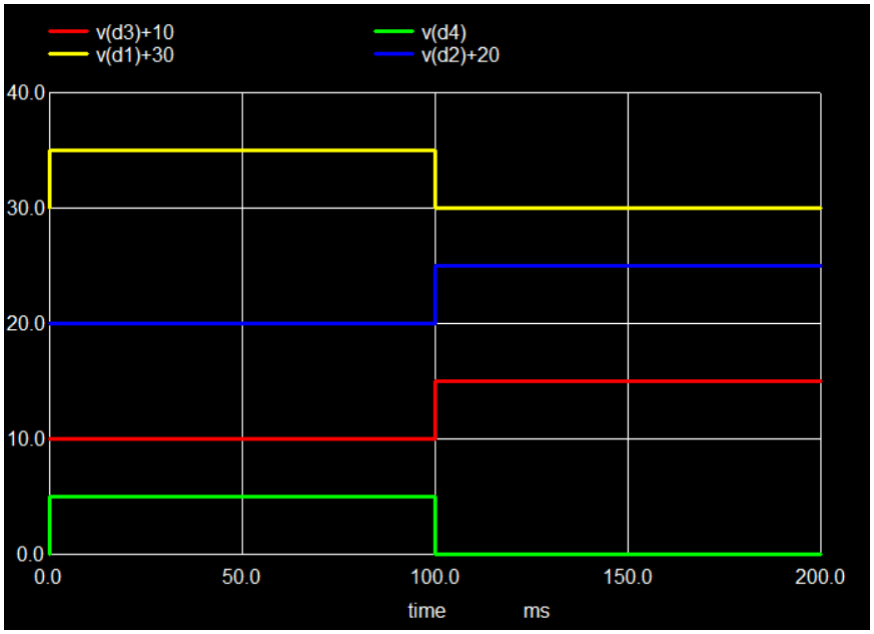



Figure 9.7: Input Plot 2 of SN74LS670 (Data Inputs)

## 9.10 Output Plots

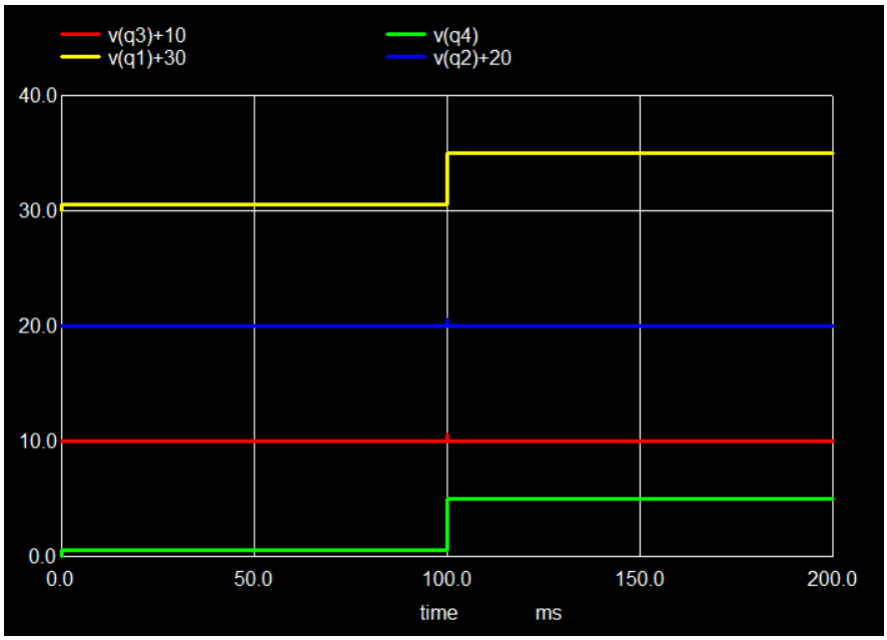



Figure 9.8: Output Plot of SN74LS670

# Chapter 10

# SL74HC154

## 10.1 General Description

**1-of-16 Decoder/Demultiplexer**
The SL74HC154 is a high-speed CMOS 1-of-16 decoder/demultiplexer with a pinout identical to that of the LS/ALS154 series, making it a drop-in replacement in compatible systems. It features two active-low chip select inputs and four address inputs to select one of 16 active-low outputs, which are all high when either chip select is high. This makes the device suitable for chip selection, demultiplexing, and cascading functions. Compatible with standard CMOS outputs and, with pull-up resistors, LS/ALS TTL logic levels, the SL74HC154 supports direct interfacing with CMOS, NMOS, and TTL circuits.The demultiplexing function is accomplished by using the Address inputs to select the desired device output.

## 10.2 Key Features

The key features of SL74HC154 includes:

- **Wide Operating Voltage Range:** It operates from 2.0 V to 6.0 V, making it suitable for both low- and high-voltage applications.
- **High Noise Immunity:** It exhibits excellent resistance to noise, a typical benefit of CMOS technology.
- **Low Input Current:** It features a low maximum input current of 1.0 A, contributing to low-power operation.
- **Direct Output Interface:** Its outputs are capable of directly interfacing with CMOS, NMOS, and TTL logic families.
- **Dual Active-Low Chip Select Inputs:** It includes two $\overline{CS}$ inputs that must both be low to enable output decoding, allowing easy control and cascading.

## 10.3 Application

The applications of SL74HC154 includes:

- **Memory Address Decoding:** It is commonly used for decoding memory address lines to enable specific memory segments.
- **Data Routing and Selection:**It routes a single input to one of several output lines based on address selection, useful in digital multiplexing systems.
- **Peripheral Chip Selection:**It enables one of many peripheral devices in microprocessor or microcontroller systems.
- **Signal Demultiplexing:** It demultiplexes a single signal line into one of 16 destinations using control logic.

## 10.4 Pin Diagram

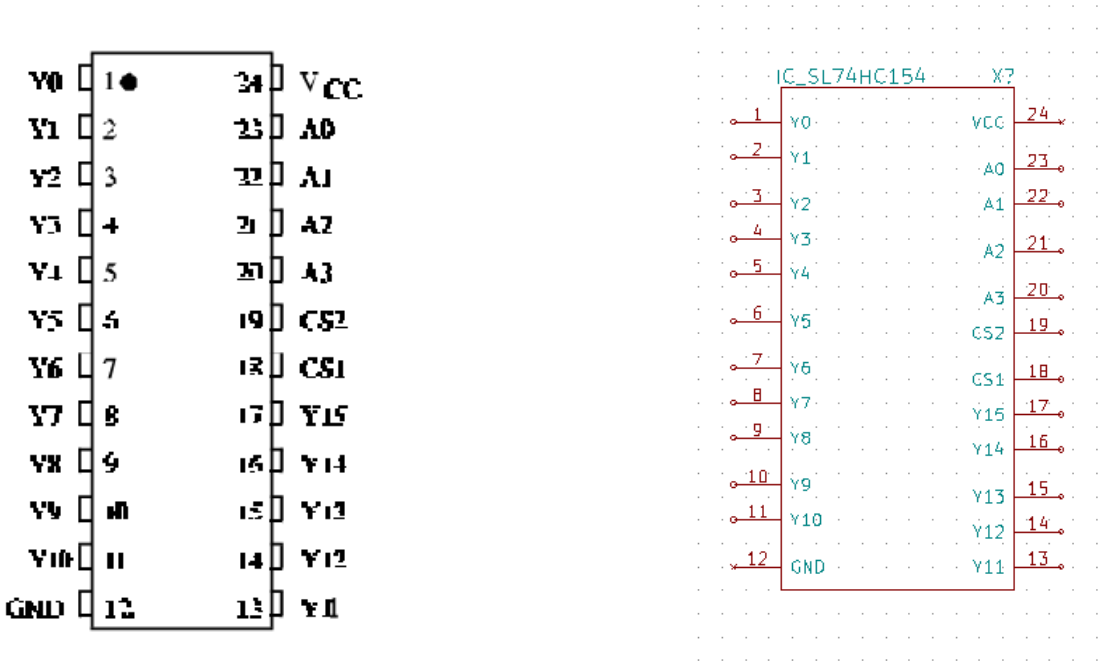



Figure 10.1: Pin diagram of SL74HC154

## 10.5 Subcircuit Schematic Diagram

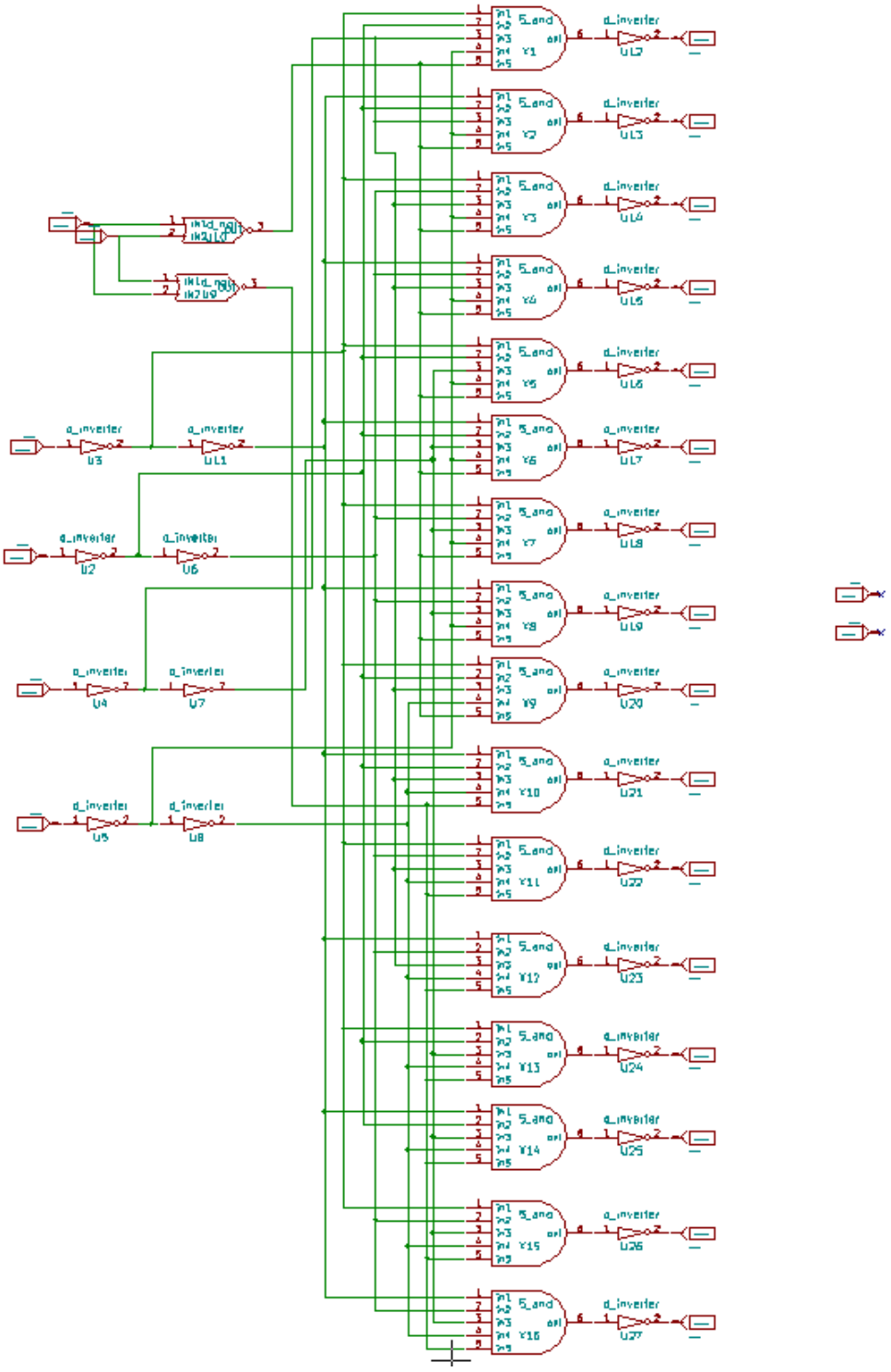


Figure 10.2: Subcircuit Schematic Diagram of SL74HC154

## 10.6 Test Circuit Schematic Diagram

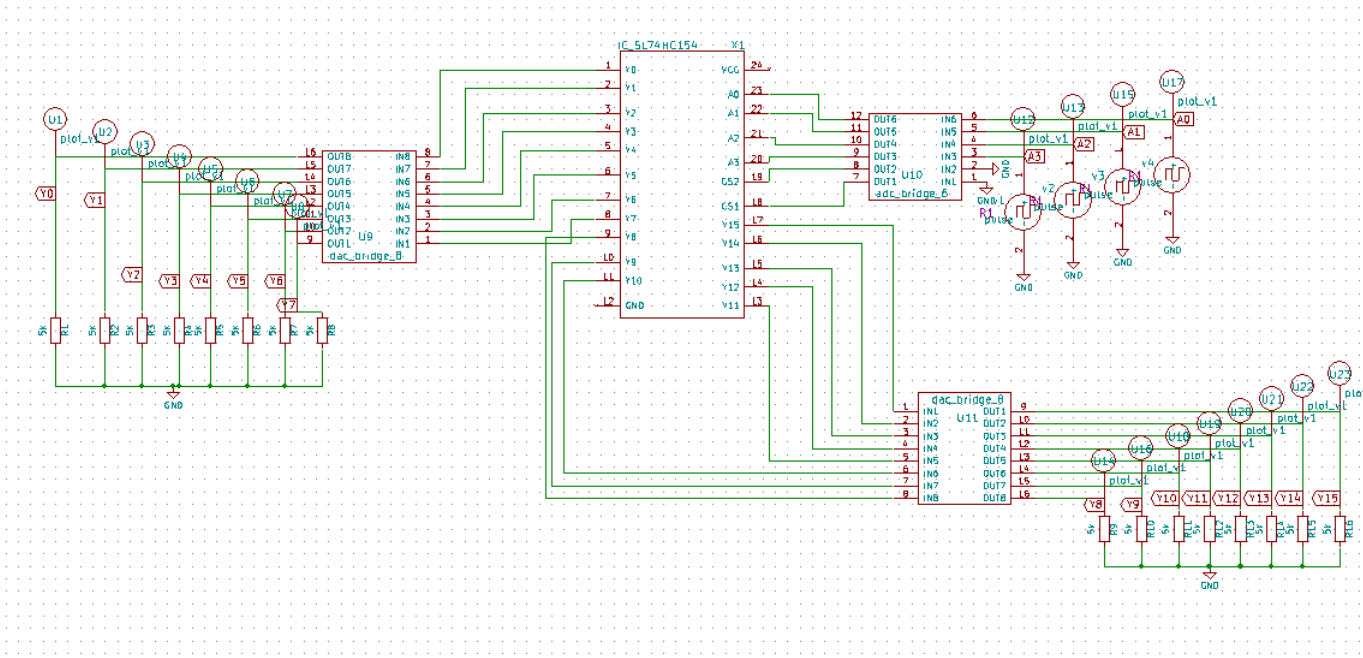


Figure 10.3: Test Circuit Schematic Diagram of SL74HC154

## 10.7 Analysis details

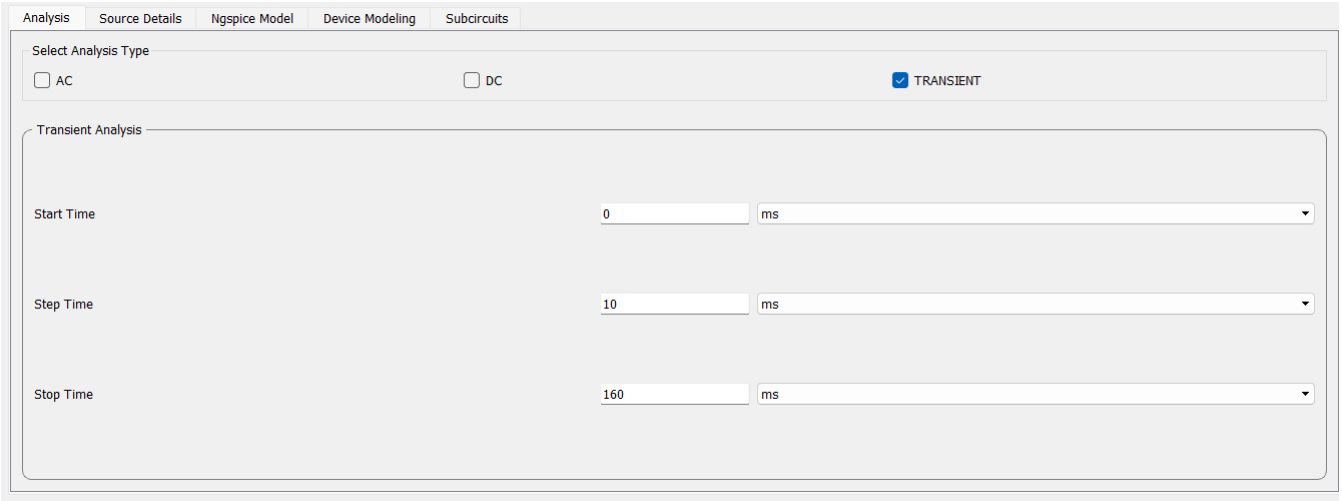



Figure 10.4: Analysis details of SL74HC154

## 10.8 Source Details

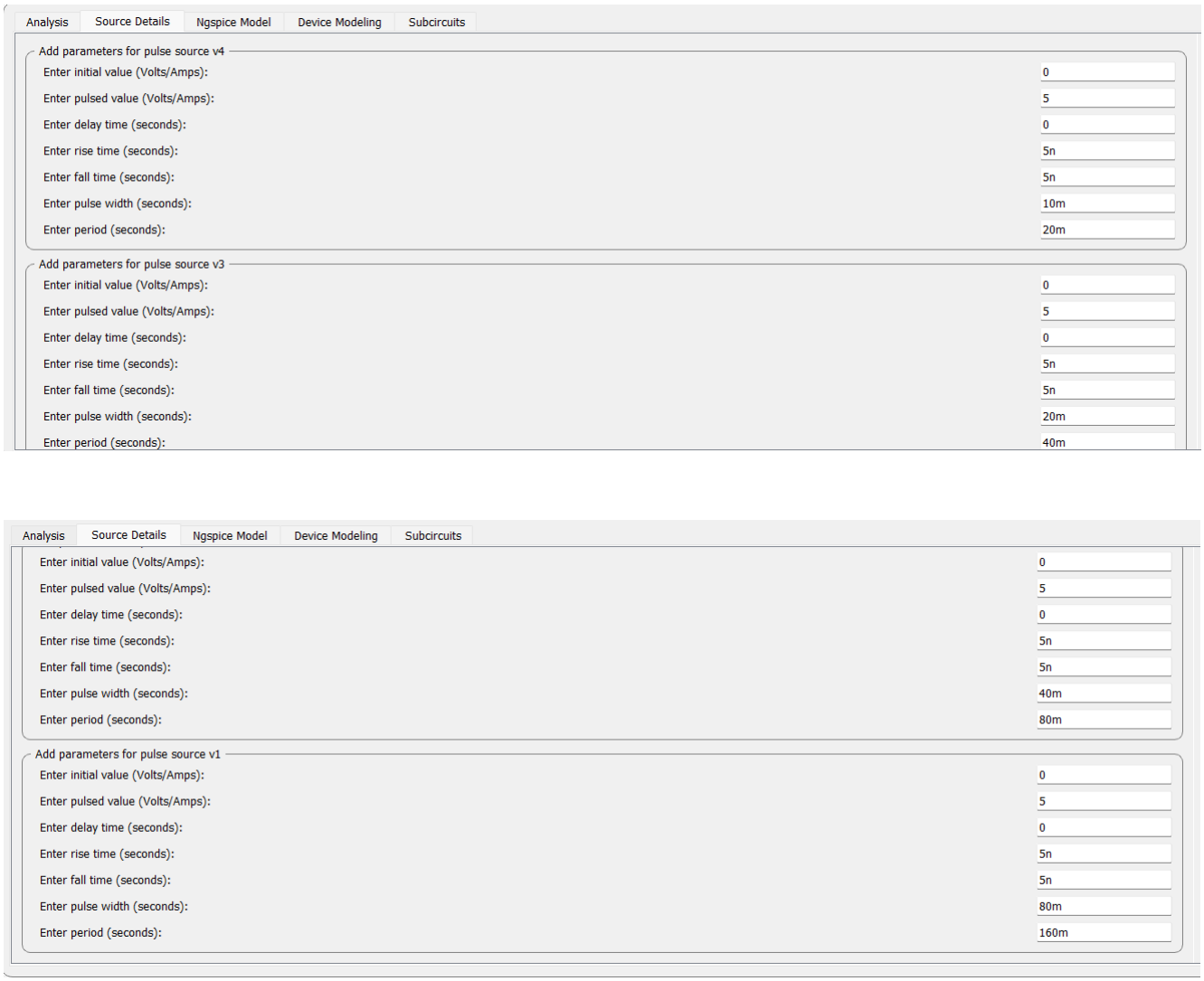



Figure 10.5: Source Details of SL74HC154

## 10.9 Input Plots

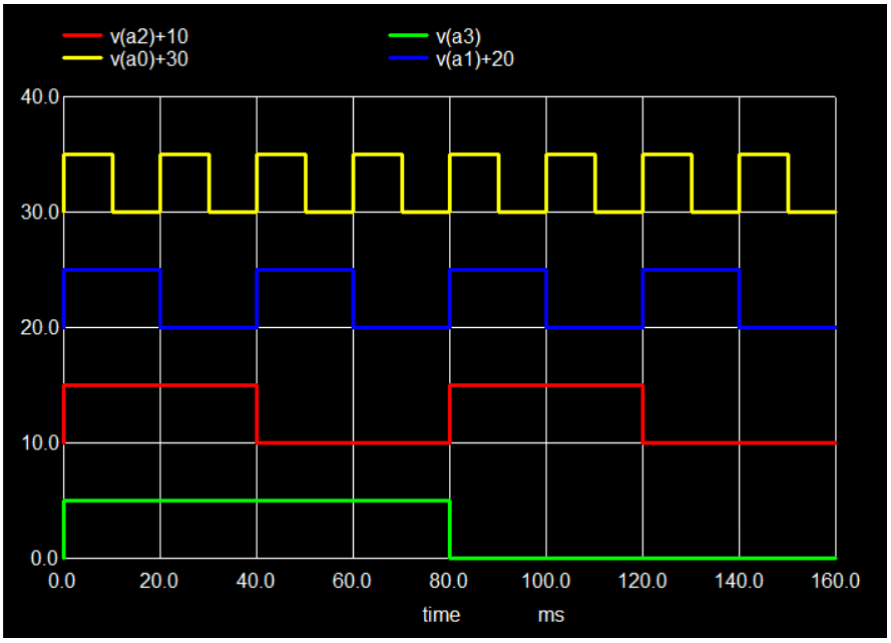



Figure 10.6: Input Plot of SL74HC154

## 10.10 Output Plots

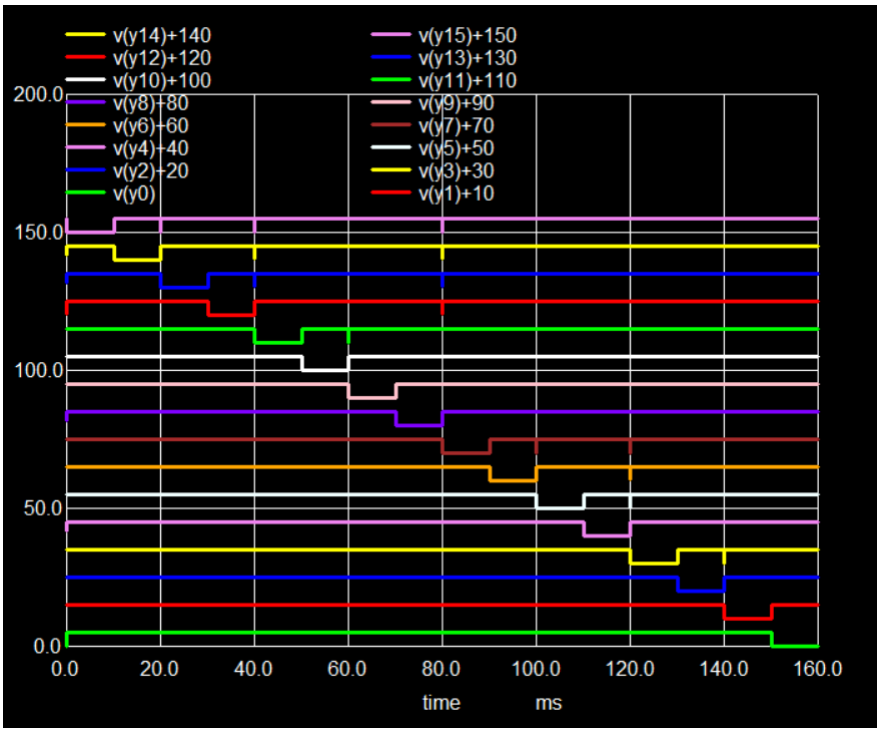



Figure 10.7: Output Plot of SL74HC154

# Chapter 11

# 74ACT11240

## 11.1 General Description

**Octal Buffer/Line Driver With 3-State Outputs (Inverted)**
The 74ACT11240 is an octal buffer or line driver designed to enhance the performance and integration density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. It features inverting outputs and symmetrical active-low output-enable $\overline{OE}$ inputs, providing both high fan-out capability and improved fan-in.

## 11.2 Key Features

The key features of 74ACT11240 includes:

- **TTL-Voltage Compatible Inputs:** Inputs are compatible with TTL logic levels, making the IC suitable for interfacing with standard TTL devices.
- **Flow-Through Architecture:** It is optimized for clean and efficient PCB layout, especially in high-density circuits.
- **Extended Temperature Range:** Guaranteed operation from 40C to +85C, suitable for industrial environments.
- **EPIC CMOS 1-m Process Technology:** It is manufactured using high-performance CMOS technology for speed and efficiency.
- **Center-Pin V¡sub¿CC¡/sub¿/GND Configuration:** It reduces high-speed switching noise for improved signal integrity.
- **High Latch-Up Immunity:** Typically 500 mA at 125C, it enhances reliability under harsh conditions.

## 11.3 Application

The applications of 74ACT11240 includes:

- **Memory Address Drivers:** It is commonly used to buffer and drive address lines in memory circuits.
- **Clock Drivers:**It buffers and distributes clock signals with minimal distortion and delay.
- **Bus-Oriented Transmitters and Receivers:** It enables one of many peripheral devices in microprocessor or microcontroller systems.
- **Signal Isolation:** It separates logic sections while inverting signals and allowing tri-state control.

## 11.4 Pin Diagram

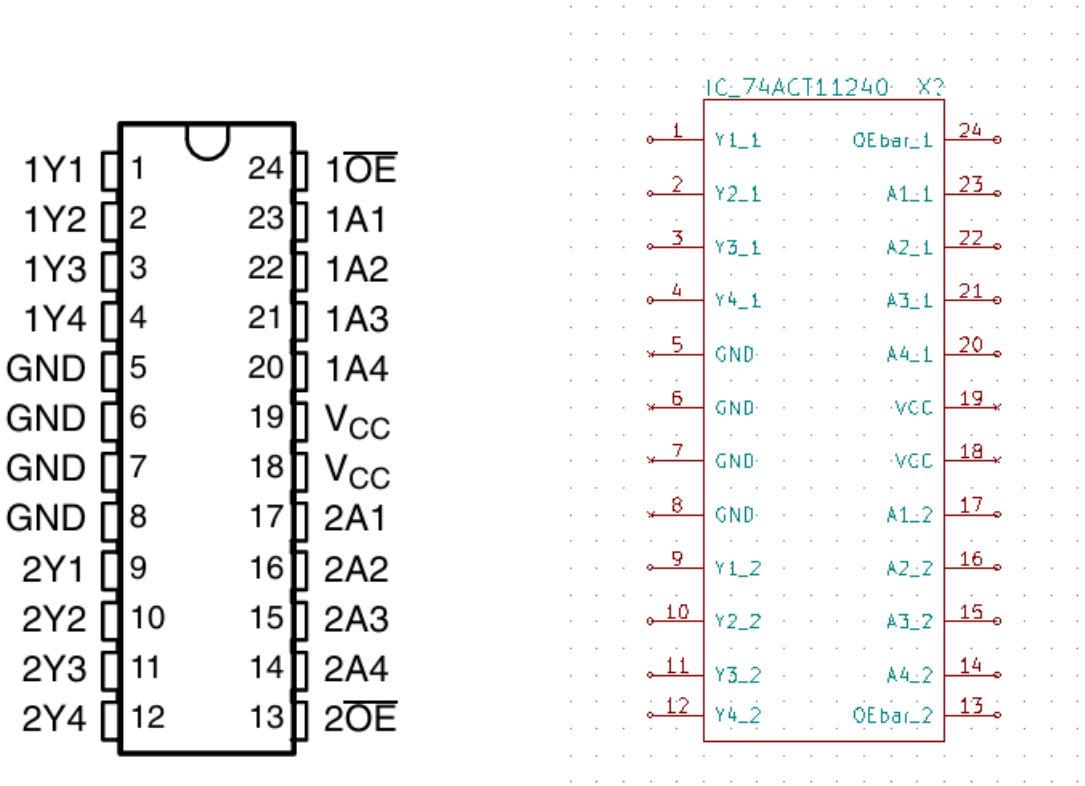



Figure 11.1: Pin diagram of 74ACT11240

## 11.5 Subcircuit Schematic Diagram

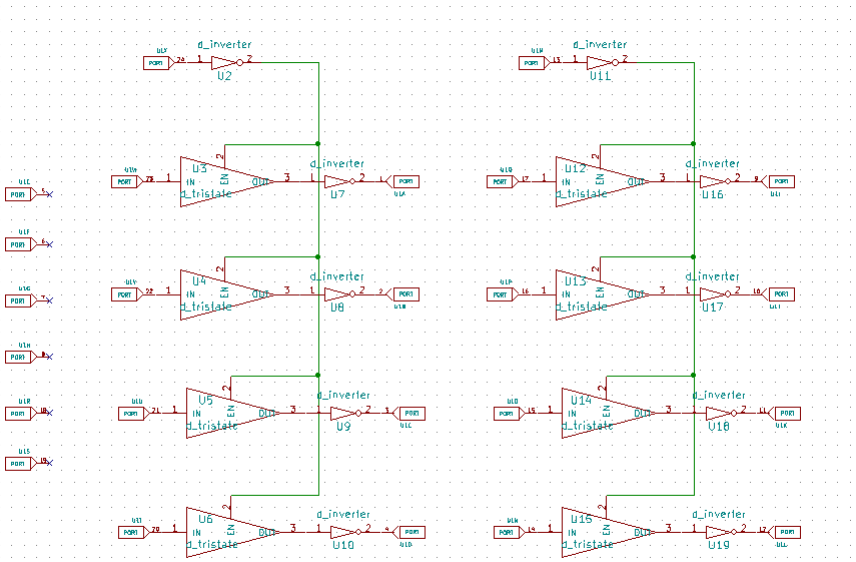



Figure 11.2: Subcircuit Schematic Diagram of 74ACT11240

## 11.6 Test Circuit Schematic Diagram

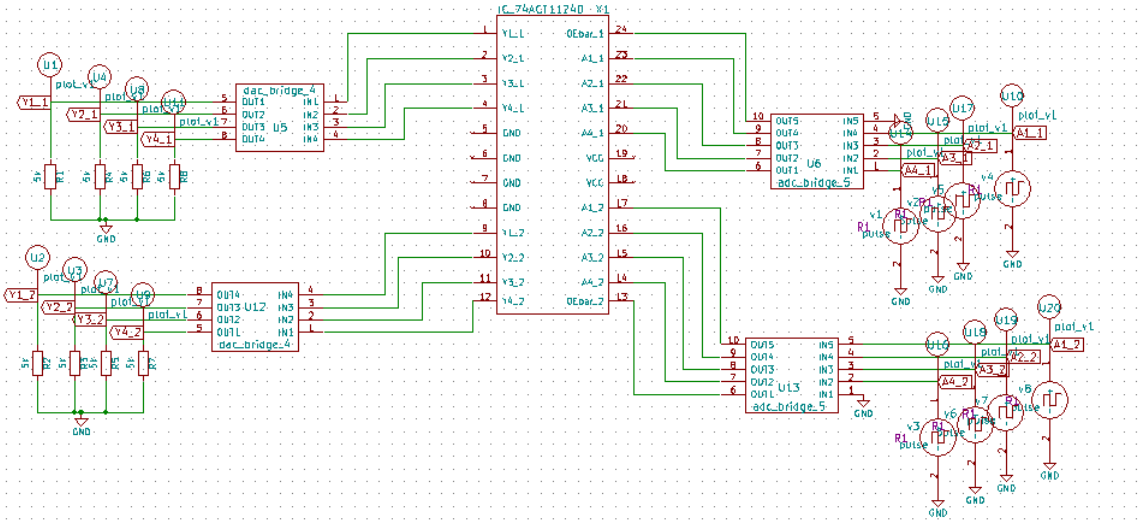



Figure 11.3: Test Circuit Schematic Diagram of 74ACT11240

## 11.7 Analysis details

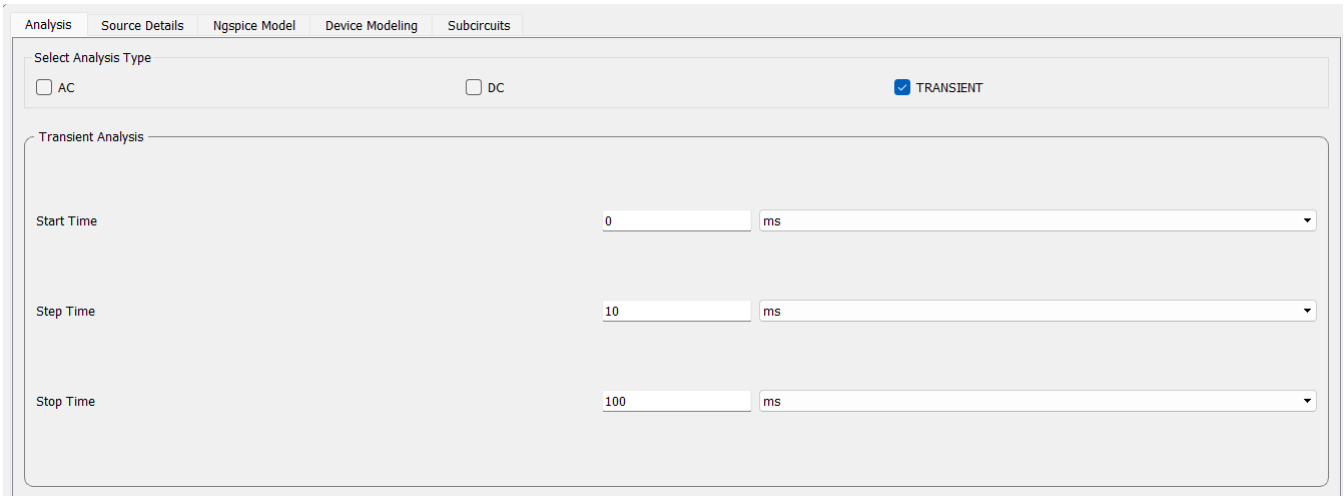



Figure 11.4: Analysis details of 74ACT11240

## 11.8 Source Details

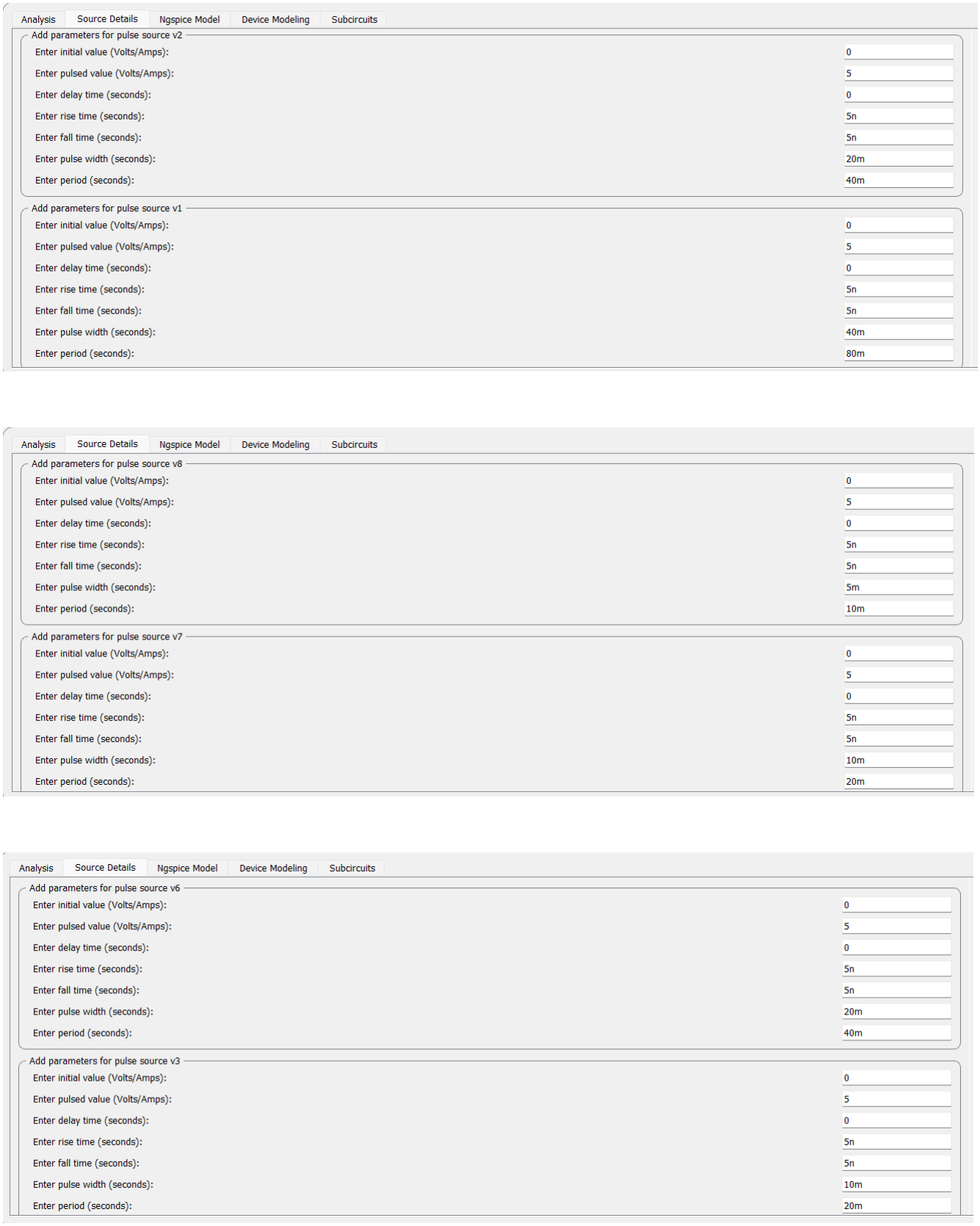



Figure 11.5: Source Details of 74ACT11240

## 11.9 Input Plots

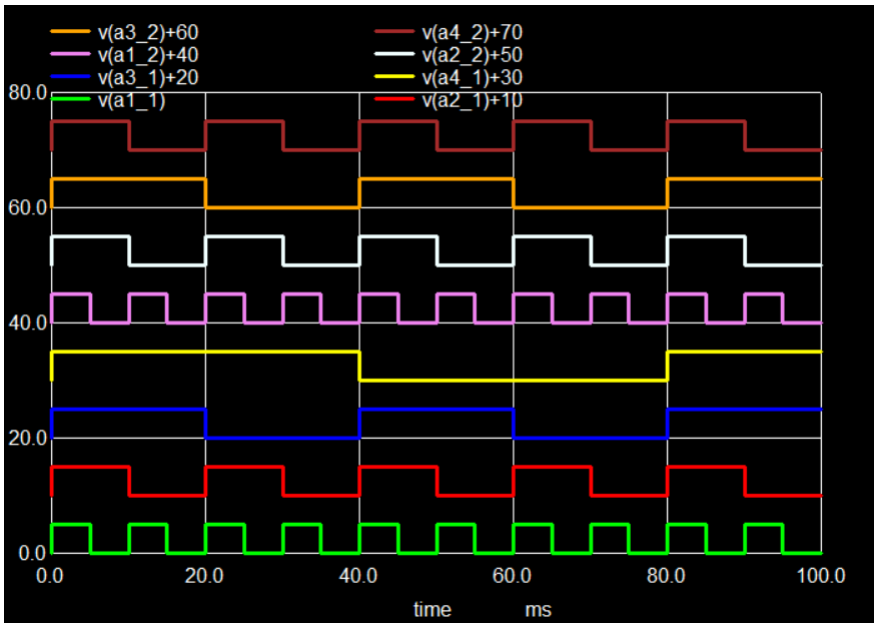



Figure 11.6: Input Plot of 74ACT11240

## 11.10 Output Plots

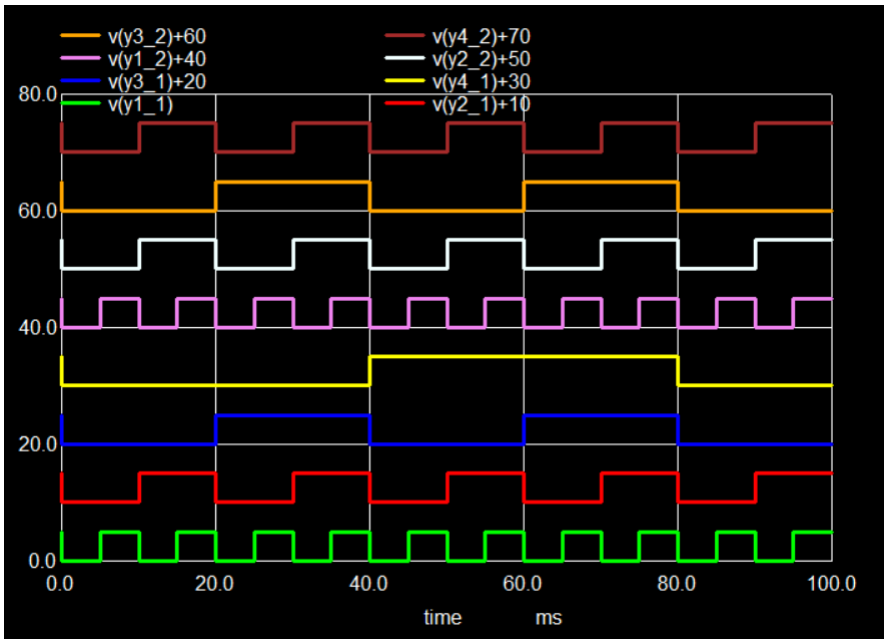



Figure 11.7: Output Plot of 74ACT11240

# Chapter 12

# M74HCT245

## 12.1 General Description

**Octal Buffer/Line Driver With 3-State Outputs (Inverted)**
The 74ACT11240 is an octal buffer or line driver designed to enhance the performance and integration density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. It features inverting outputs and symmetrical active-low output-enable $\overline{OE}$ inputs, providing both high fan-out capability and improved fan-in.

## 12.2 Key Features

The key features of M74HCT245 includes:

- **TTL-Voltage Compatible Inputs:** Inputs are compatible with TTL logic levels, making the IC suitable for interfacing with standard TTL devices.
- **Flow-Through Architecture:** It is optimized for clean and efficient PCB layout, especially in high-density circuits.
- **Extended Temperature Range:** Guaranteed operation from 40C to +85C, suitable for industrial environments.
- **EPIC CMOS 1-m Process Technology:** It is manufactured using high-performance CMOS technology for speed and efficiency.
- **Center-Pin V¡sub¿CC¡/sub¿/GND Configuration:** It reduces high-speed switching noise for improved signal integrity.
- **High Latch-Up Immunity:** Typically 500 mA at 125C, it enhances reliability under harsh conditions.

## 12.3 Application

The applications of M74HCT245 includes:

- **Memory Address Drivers:** It is commonly used to buffer and drive address lines in memory circuits.
- **Clock Drivers:**It buffers and distributes clock signals with minimal distortion and delay.
- **Bus-Oriented Transmitters and Receivers:** It enables one of many peripheral devices in microprocessor or microcontroller systems.
- **Signal Isolation:** It separates logic sections while inverting signals and allowing tri-state control.

## 12.4 Pin Diagram

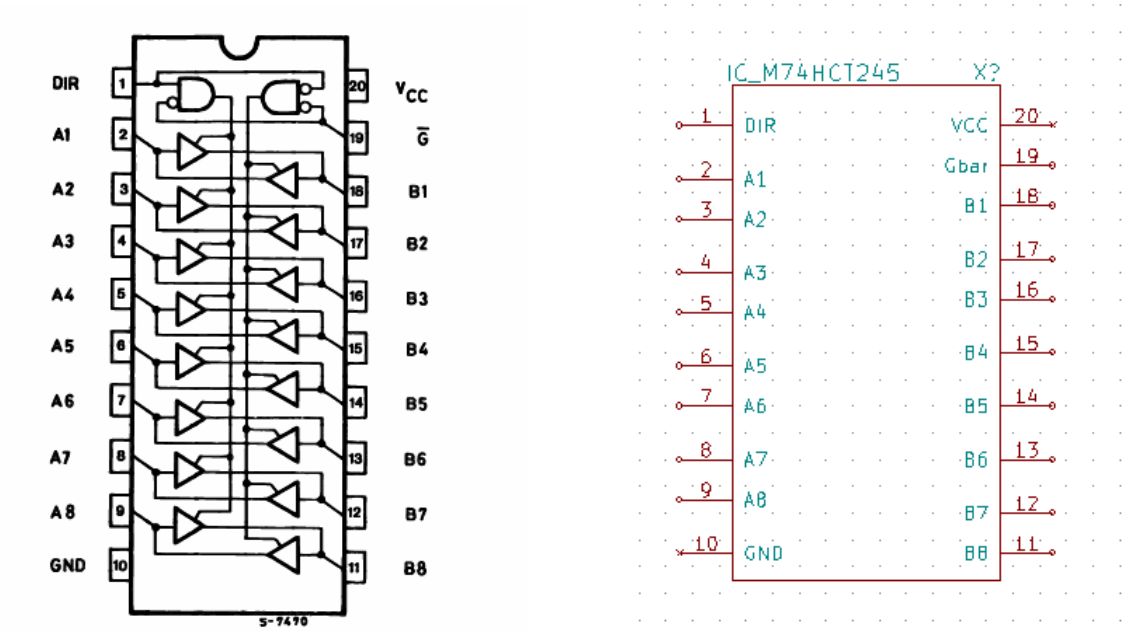



Figure 12.1: Pin diagram of M74HCT245

## 12.5 Subcircuit Schematic Diagram

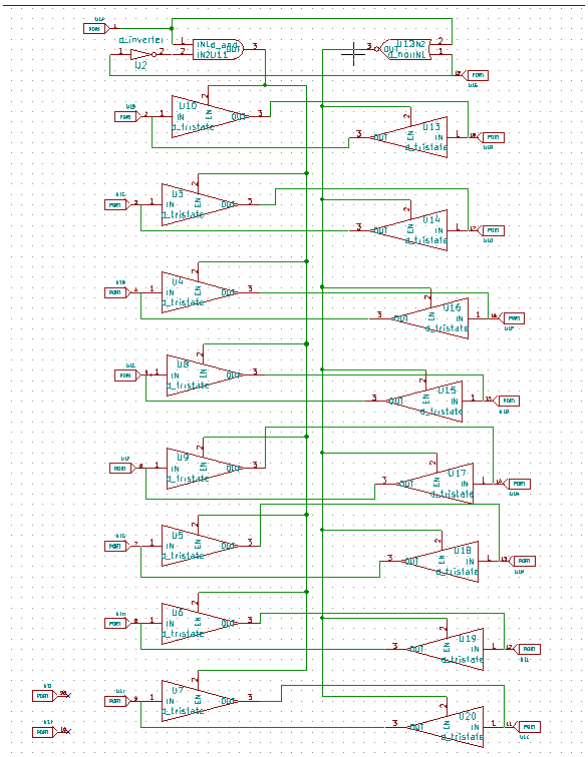


Figure 12.2: Subcircuit Schematic Diagram of M74HCT245

## 12.6 Test Circuit Schematic Diagram

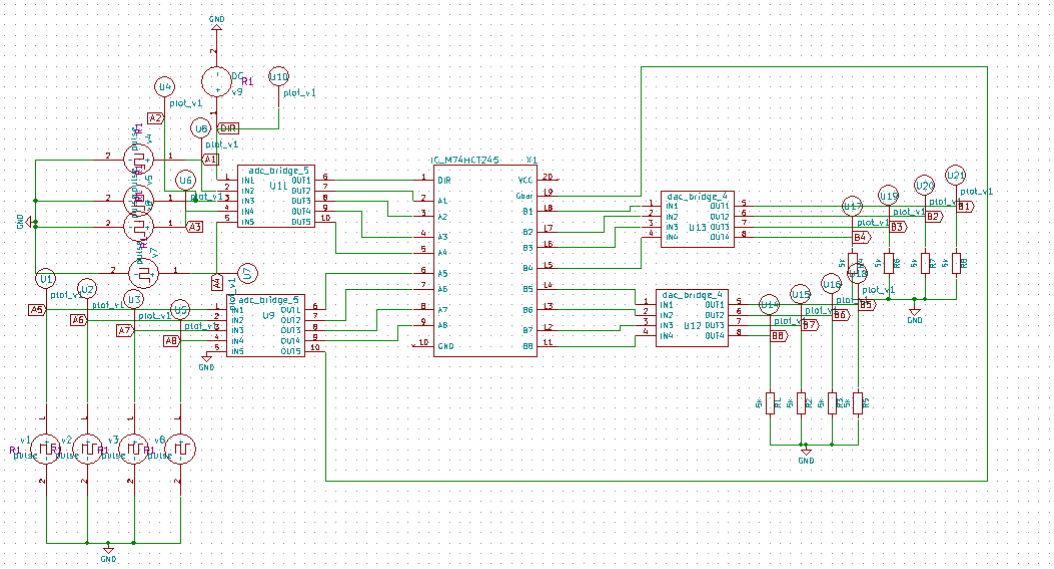


Figure 12.3: Test Circuit Schematic Diagram of M74HCT245

## 12.7 Analysis details

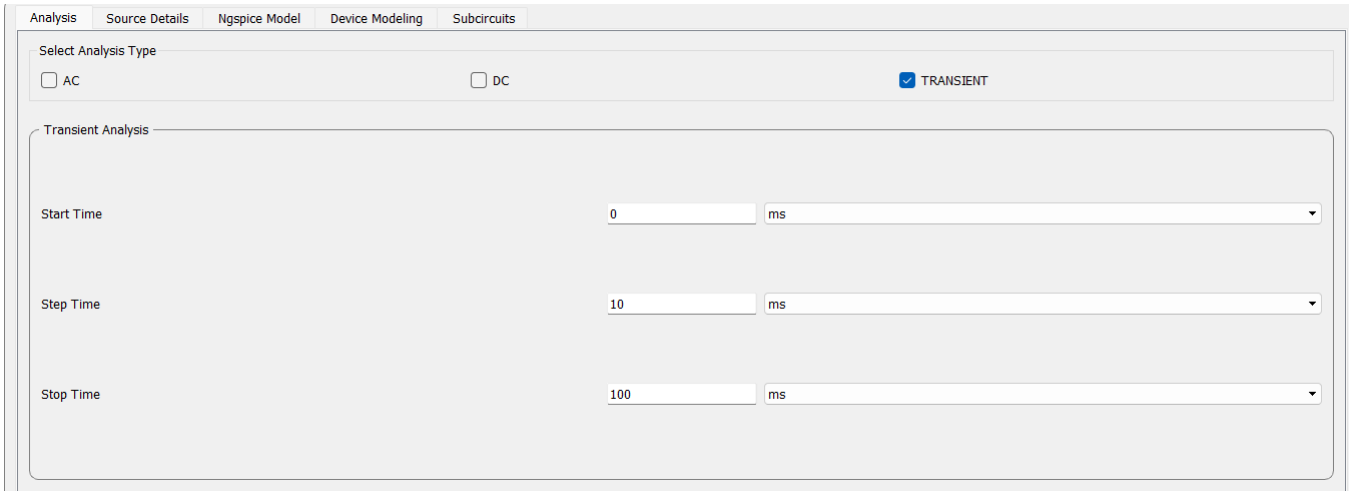
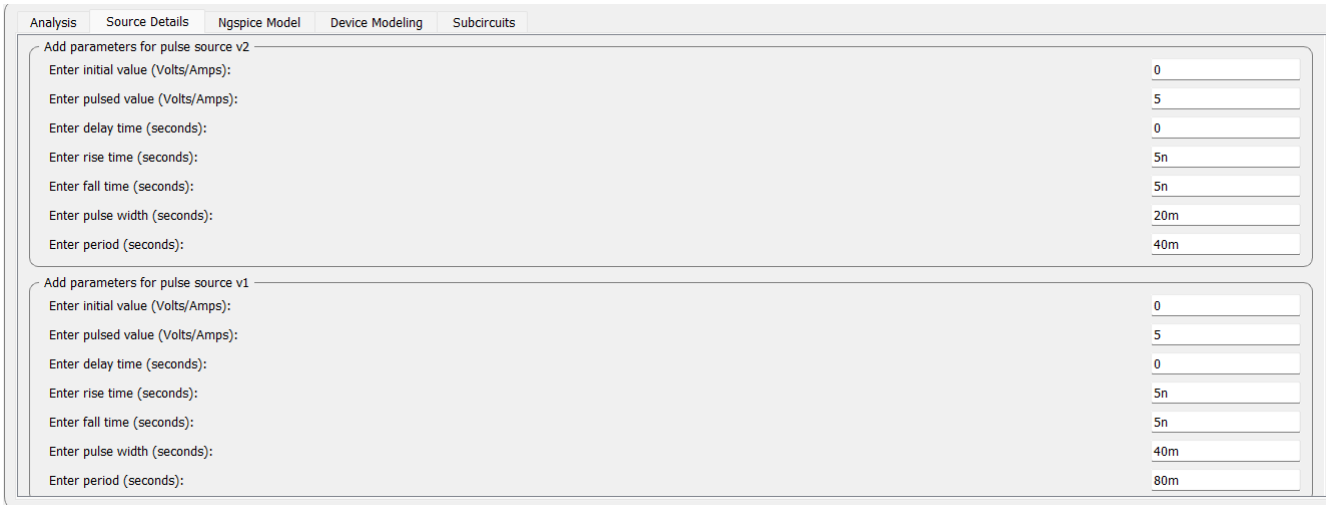



Figure 12.4: Analysis details of M74HCT245

## 12.8 Source Details


Analysis
Source Details
Ngspice Model
Device Modeling
Subcircuits
Add parameters for pulse source v2
Enter initial value (Volts/Amps):
0
Enter pulsed value (Volts/Amps):
5
Enter delay time (seconds):
0
Enter rise time (seconds):
5n
Enter fall time (seconds):
5n
Enter pulse width (seconds):
20m
Enter period (seconds):
40m
Add parameters for pulse source v1
Enter initial value (Volts/Amps):
0
Enter pulsed value (Volts/Amps):
5
Enter delay time (seconds):
0
Enter rise time (seconds):
5n
Enter fall time (seconds):
5n
Enter pulse width (seconds):
40m
Enter period (seconds):
80m


Analysis
Source Details
Ngspice Model
Device Modeling
Subcircuits
Add parameters for pulse source v7
Enter initial value (Volts/Amps):
0
Enter pulsed value (Volts/Amps):
5
Enter delay time (seconds):
0
Enter rise time (seconds):
5n
Enter fall time (seconds):
5n
Enter pulse width (seconds):
80m
Enter period (seconds):
160m
Add parameters for pulse source v6
Enter initial value (Volts/Amps):
0
Enter pulsed value (Volts/Amps):
5
Enter delay time (seconds):
0
Enter rise time (seconds):
5n
Enter fall time (seconds):
5n
Enter pulse width (seconds):
160m
Enter period (seconds):
320m


Analysis
Source Details
Ngspice Model
Device Modeling
Subcircuits
Add parameters for pulse source v5
Enter initial value (Volts/Amps):
0
Enter pulsed value (Volts/Amps):
5
Enter delay time (seconds):
0
Enter rise time (seconds):
5n
Enter fall time (seconds):
5n
Enter pulse width (seconds):
320m
Enter period (seconds):
640m
Add parameters for pulse source v4
Enter initial value (Volts/Amps):
0
Enter pulsed value (Volts/Amps):
5
Enter delay time (seconds):
0
Enter rise time (seconds):
5n
Enter fall time (seconds):
5n
Enter pulse width (seconds):
640m
Enter period (seconds):
1280m


Figure 12.5: Source Details of M74HCT245

## 12.9 Input Plots

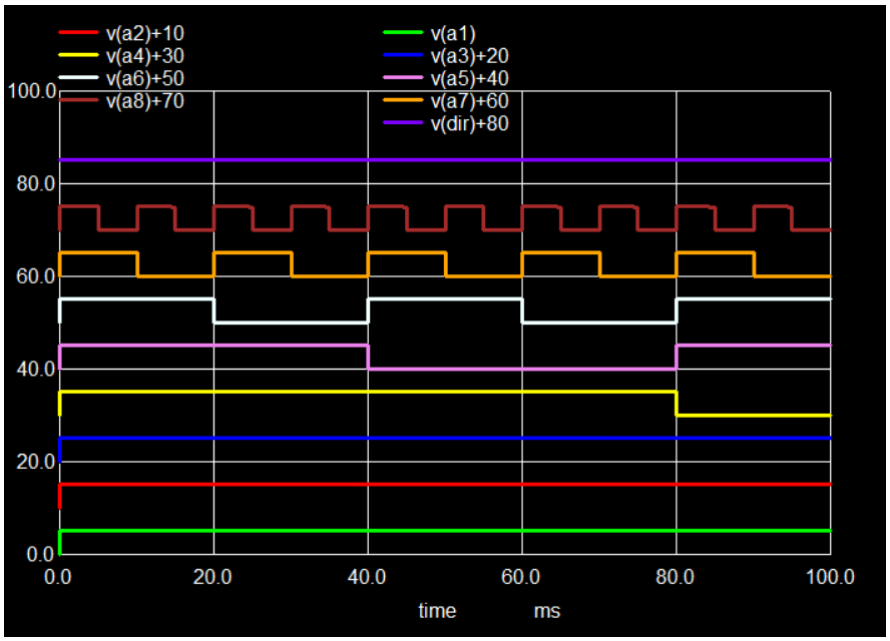



Figure 12.6: Input Plot of M74HCT245

## 12.10 Output Plots

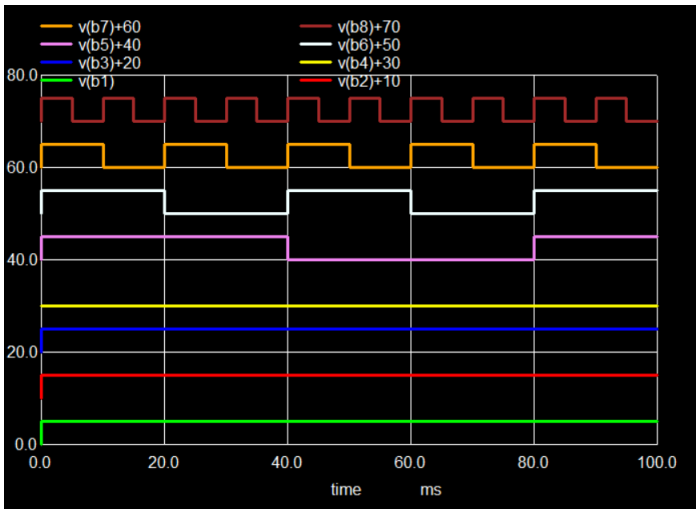



Figure 12.7: Output Plot of M74HCT245

# Chapter 13

# SN74LS51

## 13.1 General Description

**AND-OR-INVERT GATES**
The 74LS51 is a dual 2-wide input AND-OR-INVERT logic gate IC. It consists of one 2-wide 3-input AND-OR-INVERT gate and one 2-wide 2-input AND-OR-INVERT gate. The IC performs the following Boolean functions:

- $1\text{Y} = \overline{(1A.1B.1C) + (1D.1E.1F)}$
- $2\text{Y} = \overline{(2A.2B) + (2C.2D)}$

This means each gate in the IC performs the logical combination of AND operations followed by OR and then an inversion (i.e., NAND-NOR-like behavior in a compact gate structure).

## 13.2 Key Features

The key features of SN74LS51 includes:

- **Wide Operating Temperature Range:** The SN74LS51 version is characterized for operation in commercial temperature environments, specifically from 0C to 70C.
- **Operating Voltage:** The chip typically operates within a supply voltage range of 4.75V to 5.25V.
- **High Speed:** It offers relatively fast operation with typical propagation delays (tpd) between 10ns and 50ns.
- **TTL Logic Compatibility:** It belongs to the 74LS series with Low Power Schottky TTL logic levels, ensuring fast switching and low power consumption.
- **Output Type::** It features a push-pull output stage, providing both sourcing and sinking capabilities for driving loads.
- **High Reliability:** It is manufactured by Texas Instruments with assured quality and long-term reliability.

## 13.3 Application

The applications of SN74LS51 includes:

- **Control Logic:** It is commonly used for implementing control sequences, decision-making circuits, and status monitoring in digital systems.
- **Arithmetic Logic Units (ALUs):**It is useful for contributing to the construction of circuits that perform arithmetic and logical operations.
- **Computing and Memory Circuits:** It supports logic operations in CPU control units and memory access mechanisms.
- **Embedded Systems:** It is efficient for use in embedded applications where multiple AND-OR-INVERT conditions need to be evaluated.

## 13.4 Pin Diagram

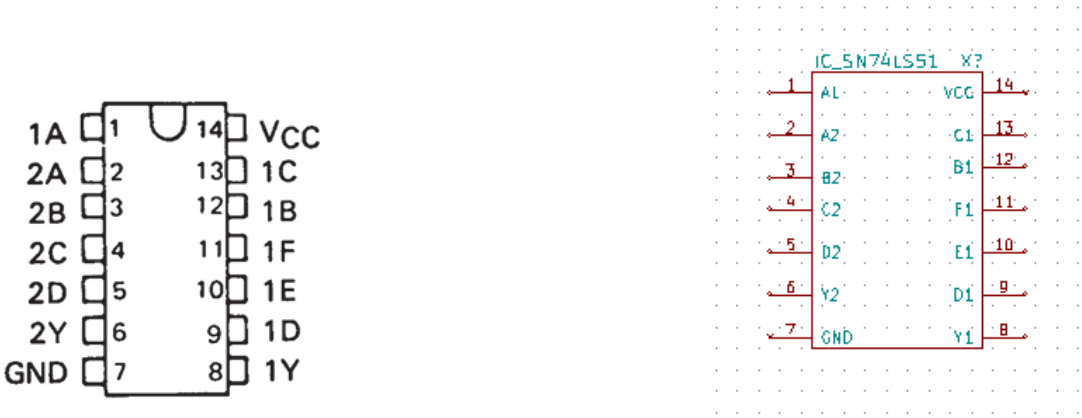



Figure 13.1: Pin diagram of SN74LS51

## 13.5 Subcircuit Schematic Diagram

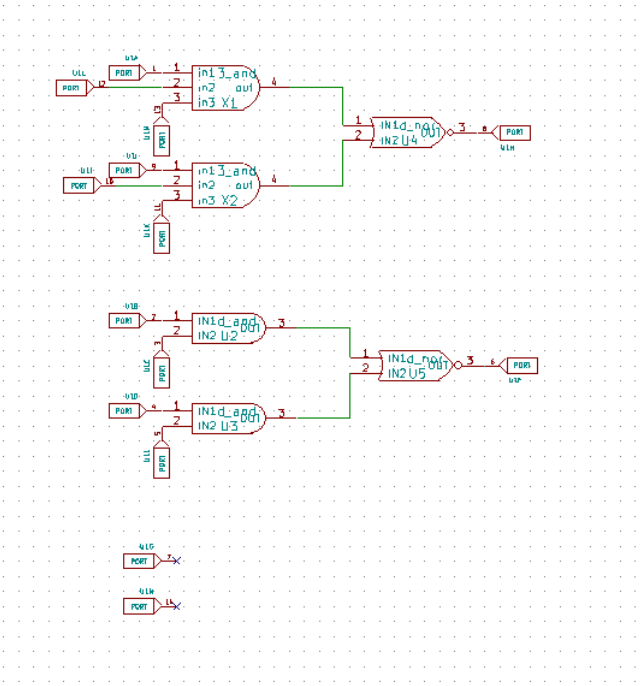


Figure 13.2: Subcircuit Schematic Diagram of SN74LS51

## 13.6 Test Circuit Schematic Diagram

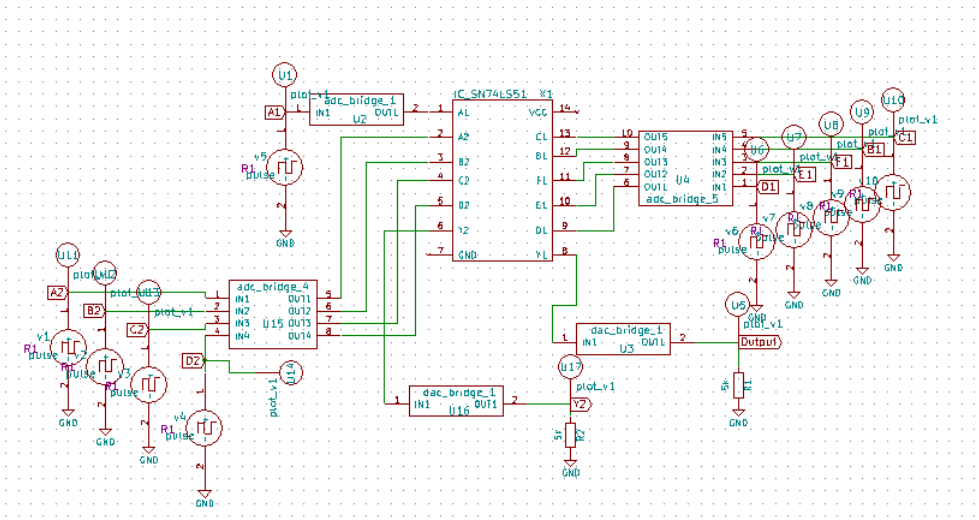


Figure 13.3: Test Circuit Schematic Diagram of SN74LS51

## 13.7 Analysis details

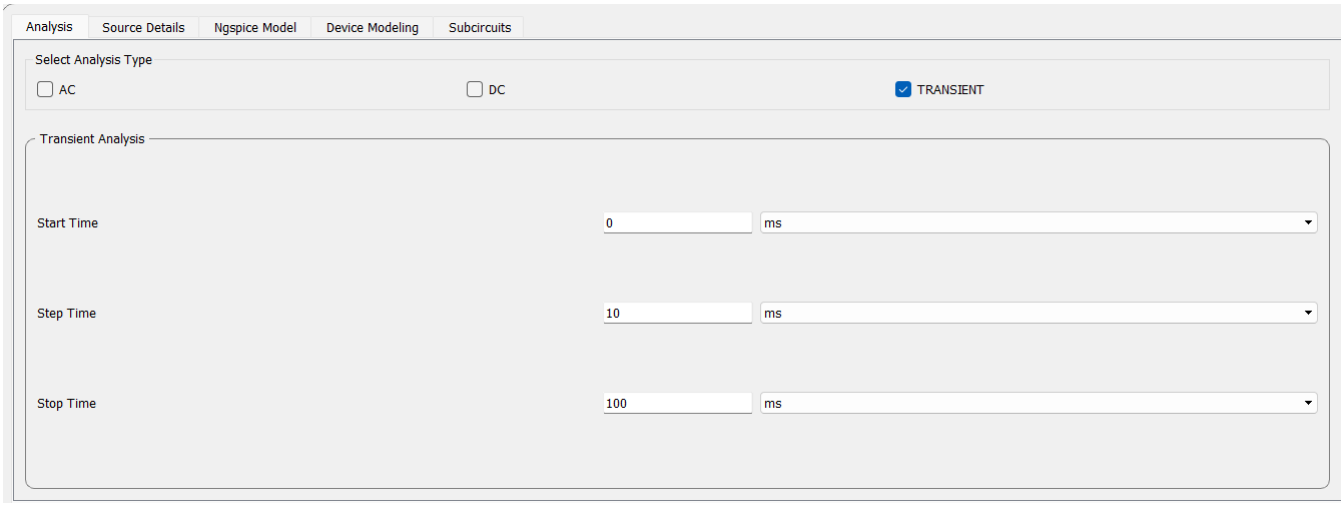
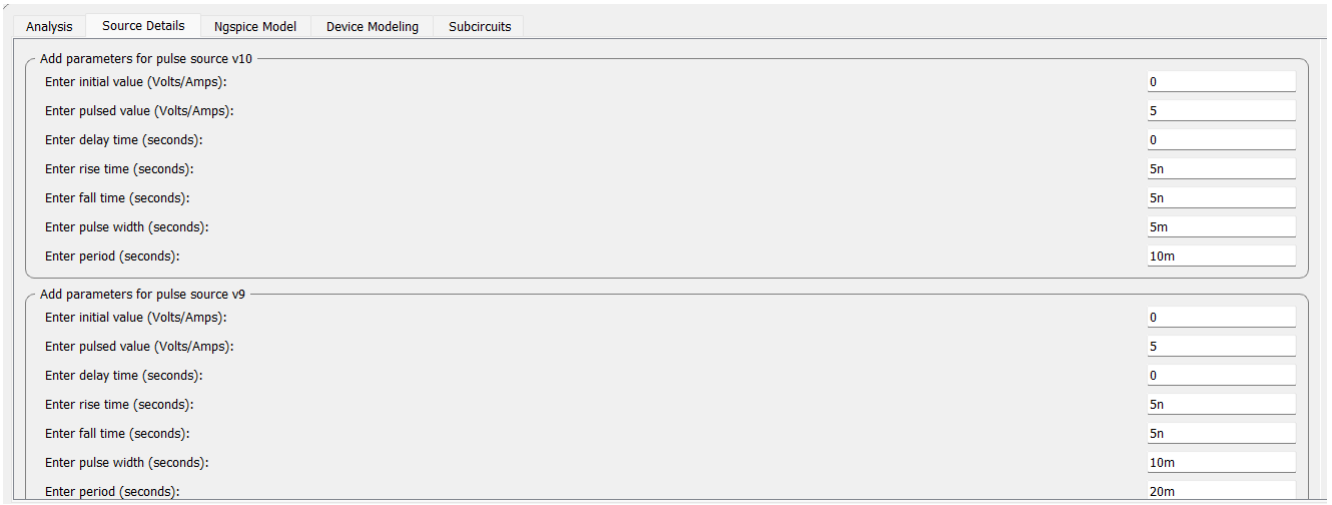
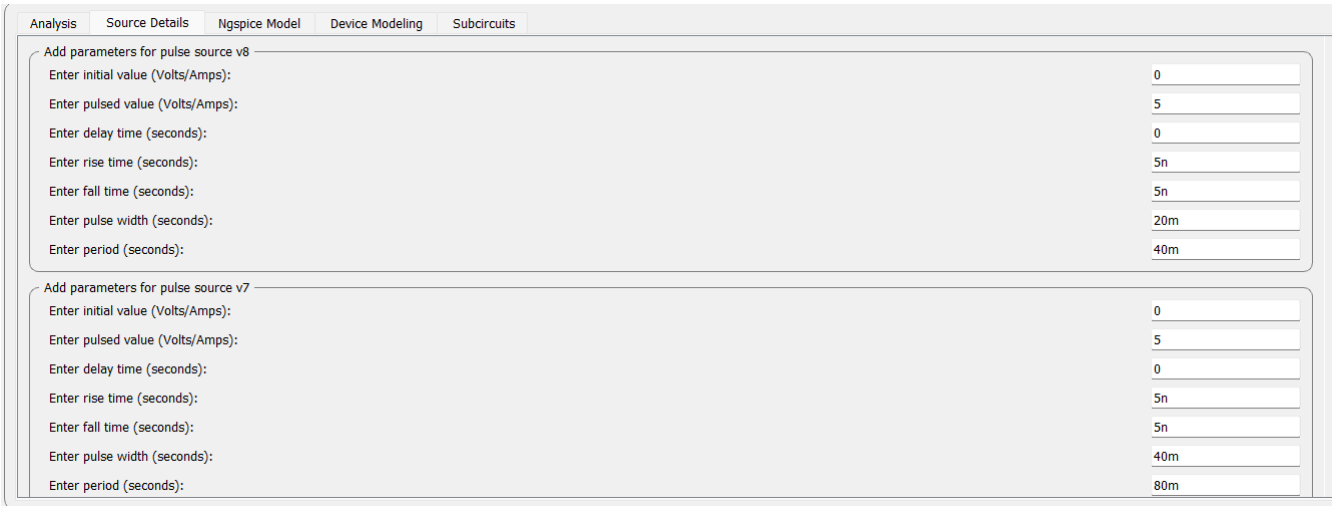



Figure 13.4: Analysis details of SN74LS51

## 13.8 Source Details




Analysis
Source Details
Ngspice Model
Device Modeling
Subcircuits
Add parameters for pulse source v8
Enter initial value (Volts/Amps): 0
Enter pulsed value (Volts/Amps): 5
Enter delay time (seconds): 0
Enter rise time (seconds): 5n
Enter fall time (seconds): 5n
Enter pulse width (seconds): 20m
Enter period (seconds): 40m
Add parameters for pulse source v7
Enter initial value (Volts/Amps): 0
Enter pulsed value (Volts/Amps): 5
Enter delay time (seconds): 0
Enter rise time (seconds): 5n
Enter fall time (seconds): 5n
Enter pulse width (seconds): 40m
Enter period (seconds): 80m


Analysis
Source Details
Ngspice Model
Device Modeling
Subcircuits
Add parameters for pulse source v6
Enter initial value (Volts/Amps): 0
Enter pulsed value (Volts/Amps): 5
Enter delay time (seconds): 0
Enter rise time (seconds): 5n
Enter fall time (seconds): 5n
Enter pulse width (seconds): 5m
Enter period (seconds): 10m
Add parameters for pulse source v5
Enter initial value (Volts/Amps): 0
Enter pulsed value (Volts/Amps): 5
Enter delay time (seconds): 0
Enter rise time (seconds): 5n
Enter fall time (seconds): 5n
Enter pulse width (seconds): 10m
Enter period (seconds): 20m


Analysis
Source Details
Ngspice Model
Device Modeling
Subcircuits
Add parameters for pulse source v1
Enter initial value (Volts/Amps): 0
Enter pulsed value (Volts/Amps): 5
Enter delay time (seconds): 0
Enter rise time (seconds): 5n
Enter fall time (seconds): 5n
Enter pulse width (seconds): 20m
Enter period (seconds): 40m
Add parameters for pulse source v2
Enter initial value (Volts/Amps): 0
Enter pulsed value (Volts/Amps): 5
Enter delay time (seconds): 0
Enter rise time (seconds): 5n
Enter fall time (seconds): 5n
Enter pulse width (seconds): 40m
Enter period (seconds): 80m

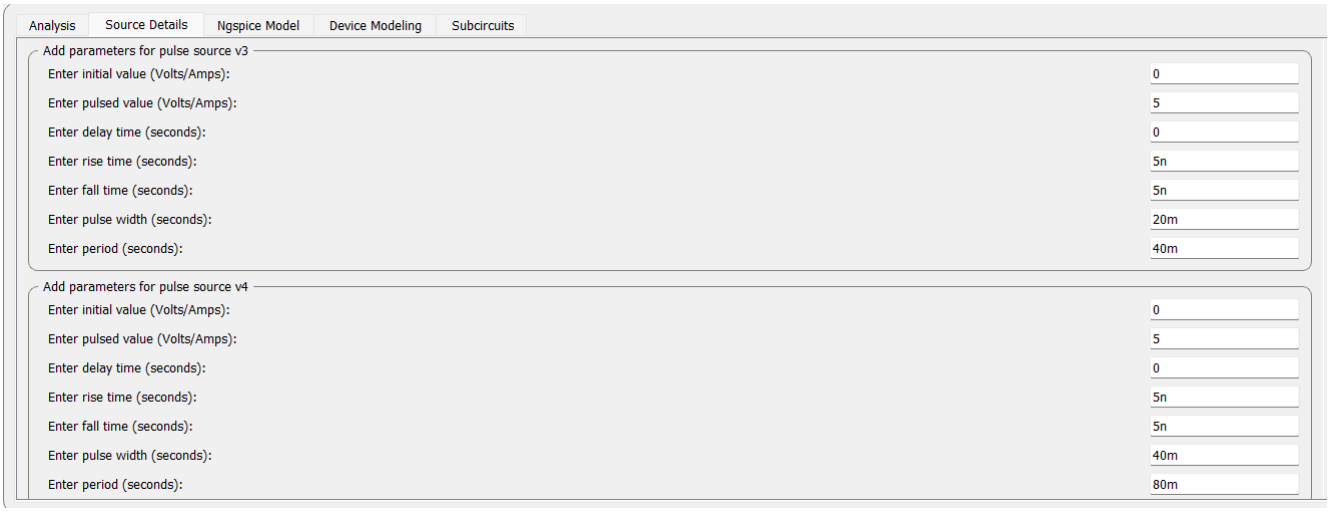



Figure 13.5: Source Details of SN74LS51

## 13.9 Input Plots

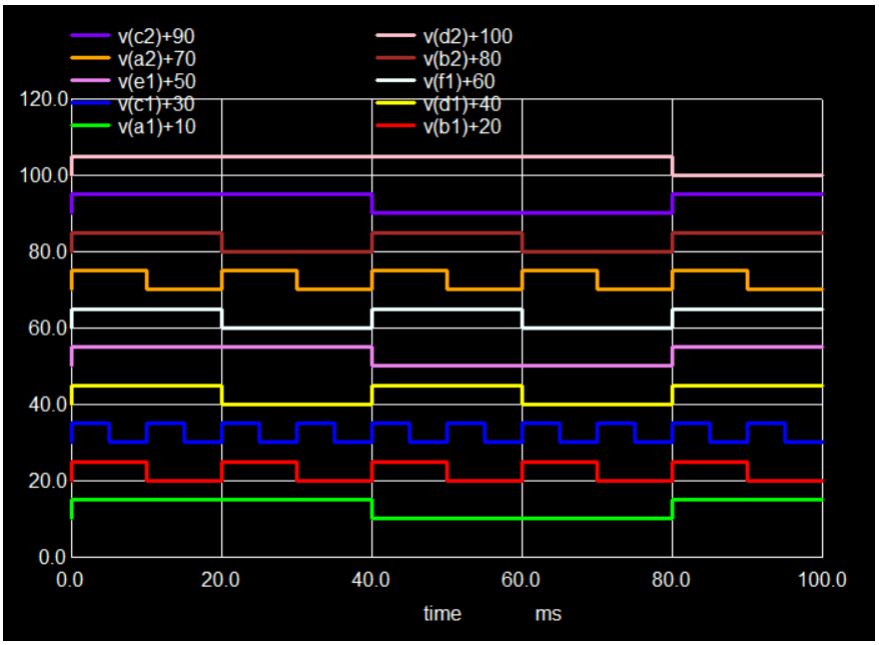



Figure 13.6: Input Plot of SN74LS51

## 13.10 Output Plots

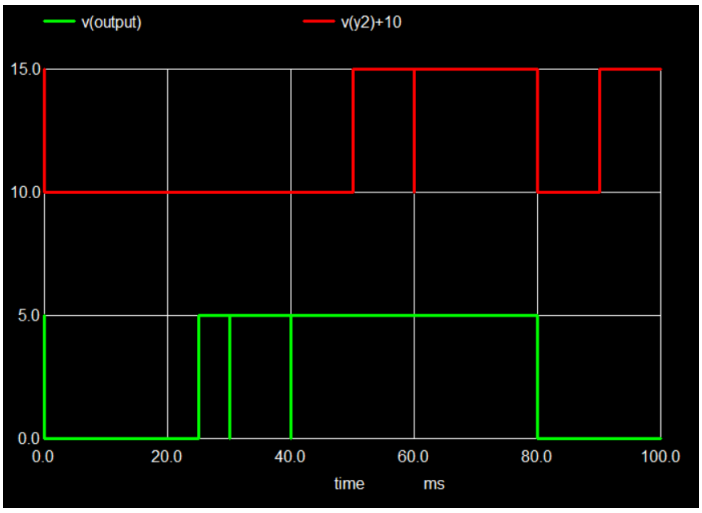



Figure 13.7: Output Plot of SN74LS51

# Chapter 14

# SN74LS684

## 14.1 General Description

**8-bit Magnitude Comparator** The SN74LS684 is an 8-bit magnitude comparator that performs bitwise comparison between two 8-bit binary or BCD inputs. It provides outputs indicating whether the two inputs are equal by performing the inverted equal operation $\overline{(P = Q)}$, and unlike the LS688, it also provides outputs for inverted greater than operation $\overline{(P > Q)}$. The SN74LS684 features totem-pole outputs, which allow for faster switching and direct drive capability without the need for external pull-up resistors. It is suitable for high-speed arithmetic and logical comparison operations in digital systems.

## 14.2 Key Features

The key features of SN74LS684 includes:

- **Totem-Pole Outputs:** It allows faster switching and direct interfacing without external pull-ups.haracterized for operation in commercial temperature environments, specifically from 0C to 70C.
- **Expandable:** It can be cascaded for comparing multi-byte data.
- **High Speed:** It is designed for fast digital comparisons in real-time processing.
- **TTL Logic Compatibility:** It operates reliably within standard TTL logic levels.

## 14.3 Application

The applications of SN74LS684 includes:

- **Data Validation:** It verifies equality or magnitude between input values in control systems.

- **Sorting and Priority Encoding:**It helps in building digital sorters or priority logic.
- **Address Matching in Memory Systems:** It compares addresses for cache or memory lookups.
- **Arithmetic Logic Units (ALUs):** It implements comparison logic in CPUs and digital processors.

## 14.4 Pin Diagram

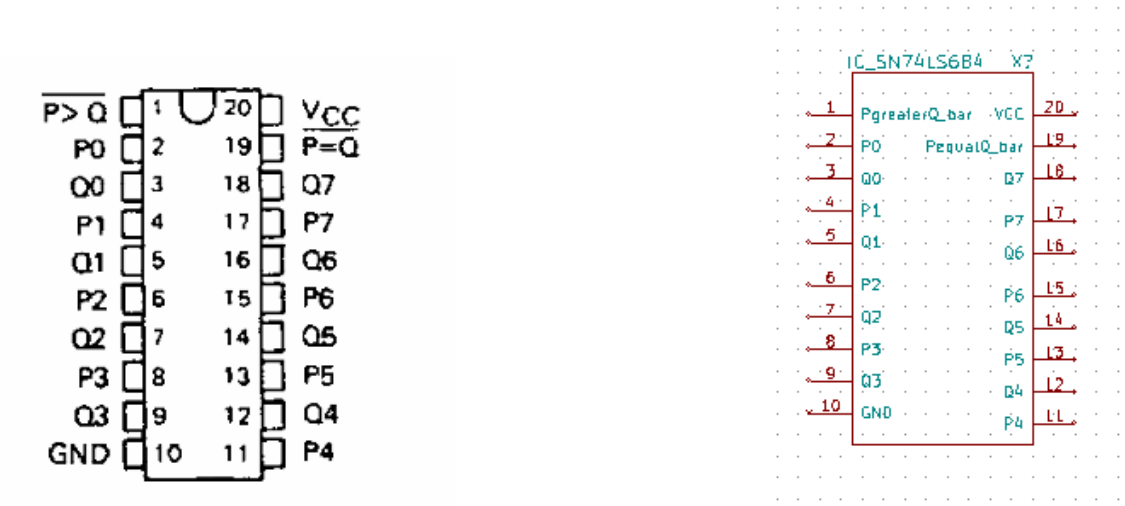



Figure 14.1: Pin diagram of SN74LS684

## 14.5 Subcircuit Schematic Diagram

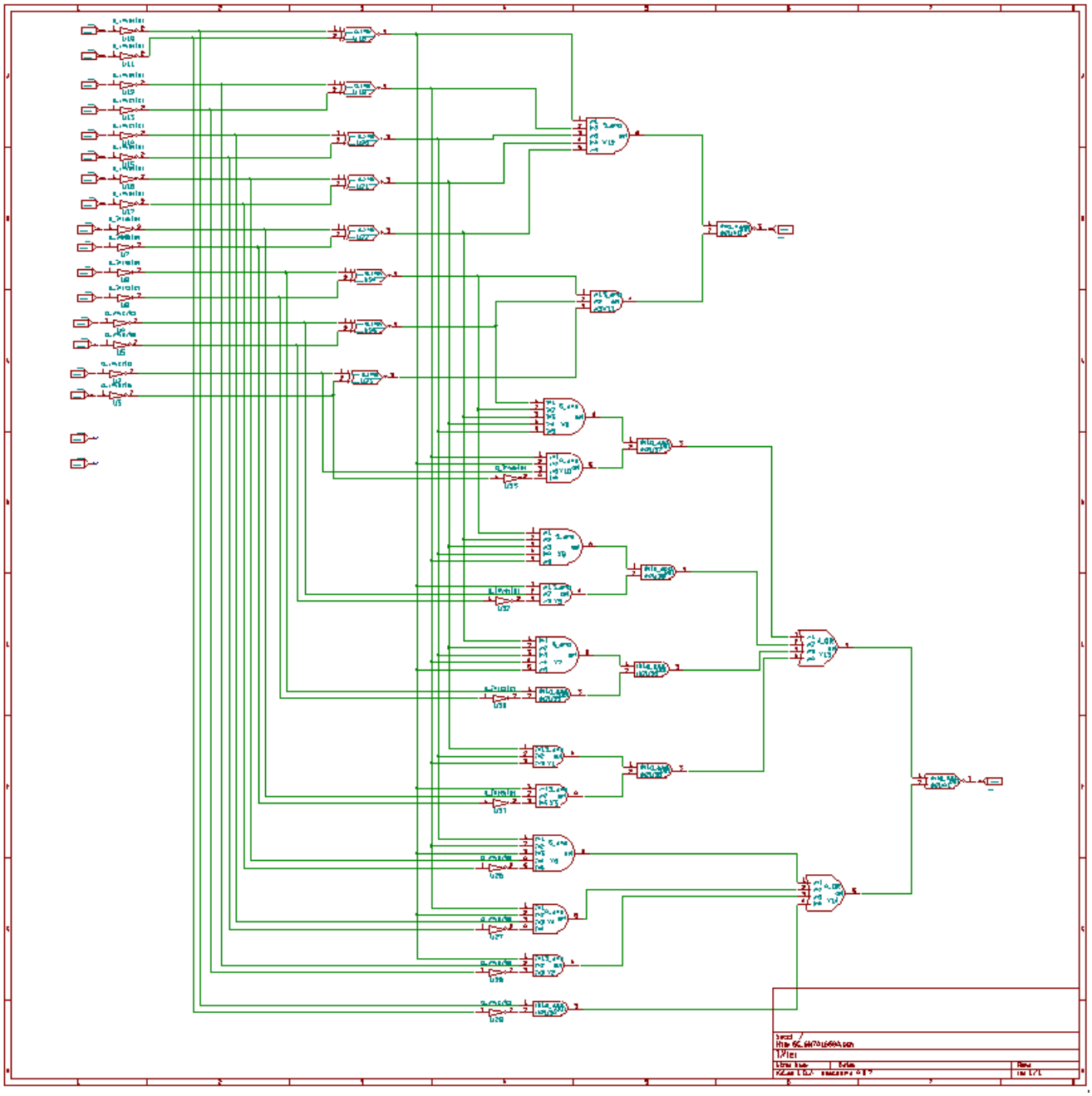


Figure 14.2: Subcircuit Schematic Diagram of SN74LS684

## 14.6 Test Circuit Schematic Diagram

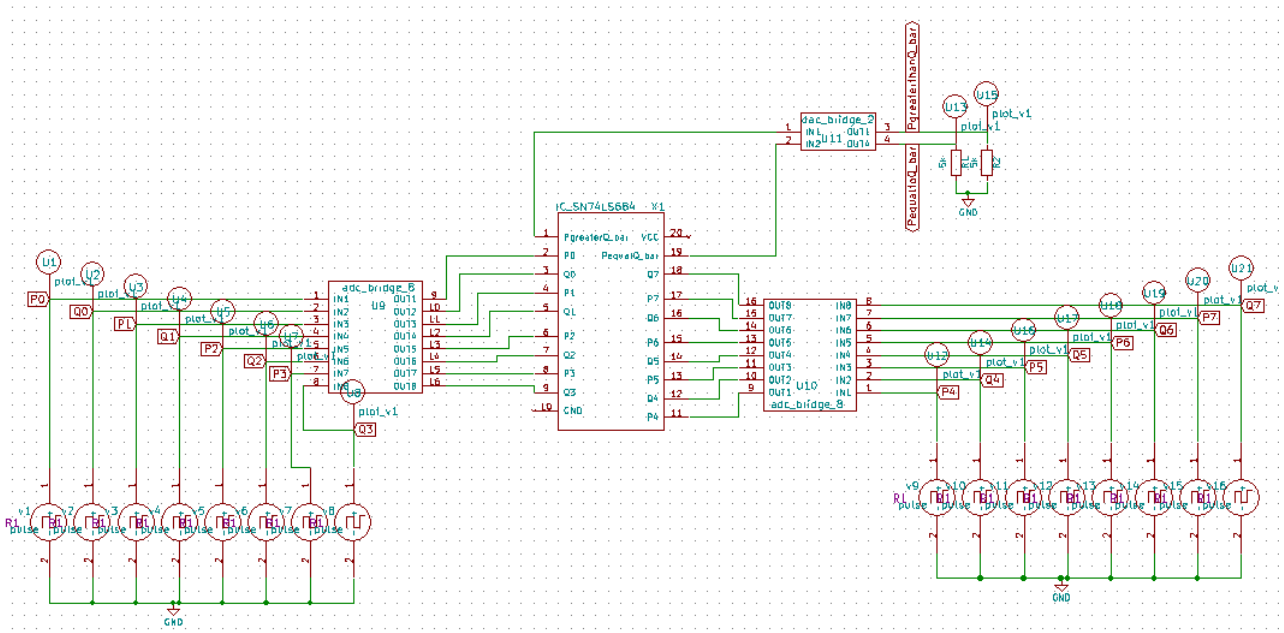



Figure 14.3: Test Circuit Schematic Diagram of SN74LS684

## 14.7 Analysis details

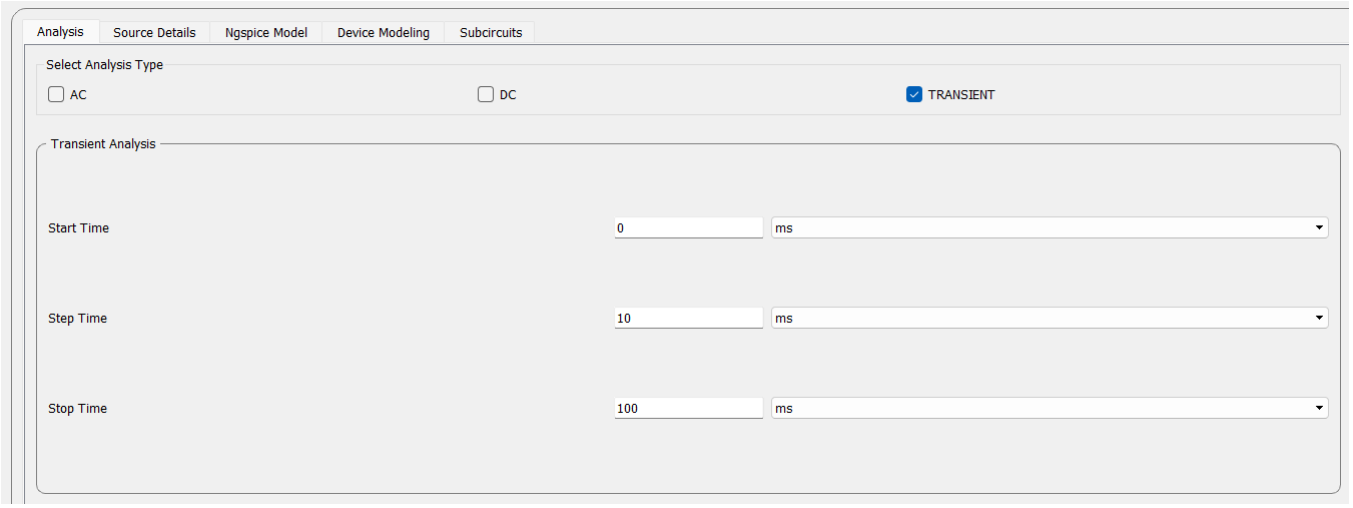
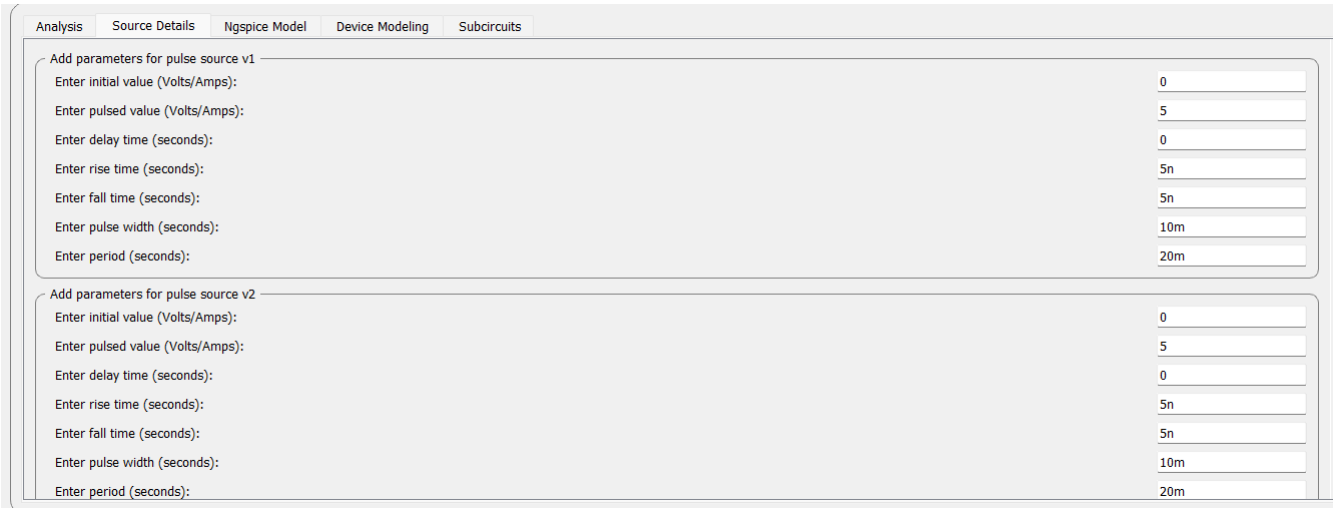
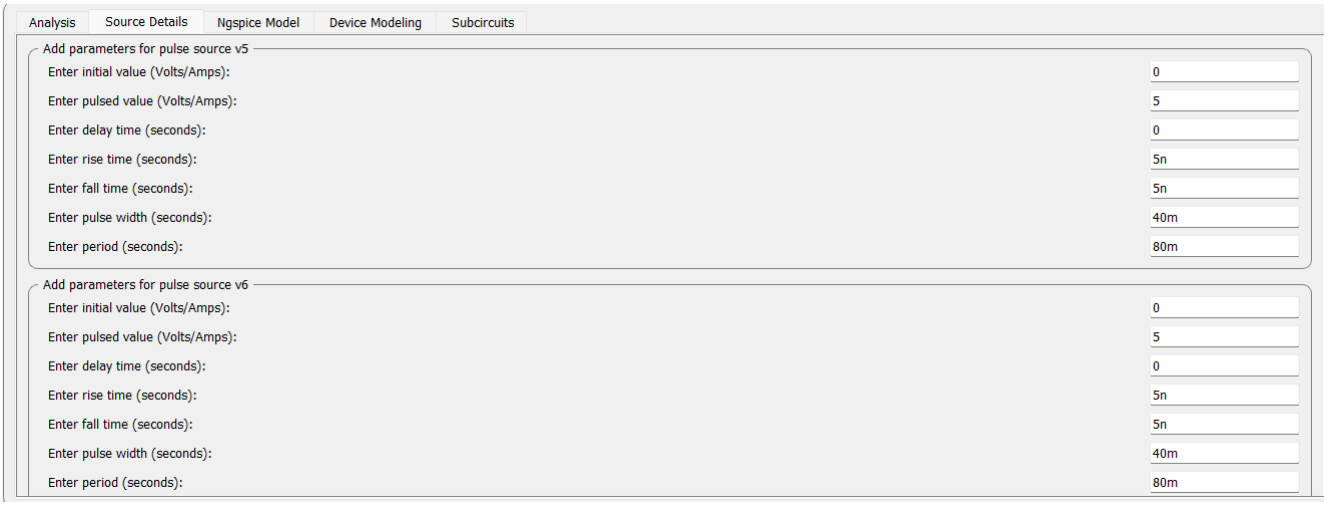



Figure 14.4: Analysis details of SN74LS684

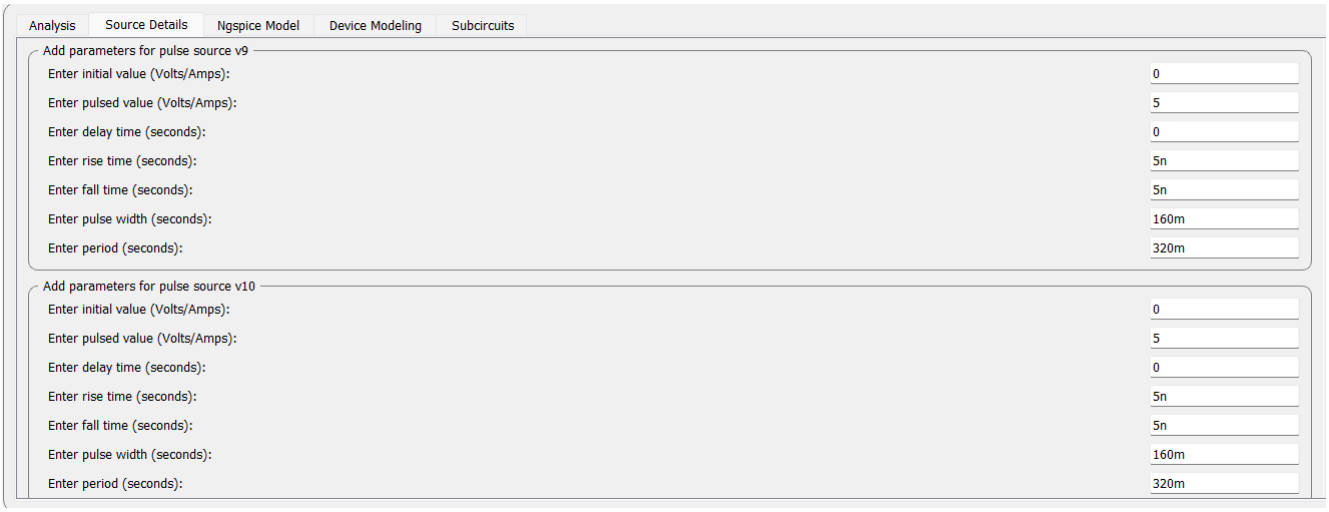
## 14.8 Source Details








Analysis
Source Details
Ngspice Model
Device Modeling
Subcircuits
Add parameters for pulse source v7
Enter initial value (Volts/Amps):
0
Enter pulsed value (Volts/Amps):
5
Enter delay time (seconds):
0
Enter rise time (seconds):
5n
Enter fall time (seconds):
5n
Enter pulse width (seconds):
80m
Enter period (seconds):
160m
Add parameters for pulse source v8
Enter initial value (Volts/Amps):
0
Enter pulsed value (Volts/Amps):
5
Enter delay time (seconds):
0
Enter rise time (seconds):
5n
Enter fall time (seconds):
5n
Enter pulse width (seconds):
80m
Enter period (seconds):
160m


Analysis
Source Details
Ngspice Model
Device Modeling
Subcircuits
Add parameters for pulse source v9
Enter initial value (Volts/Amps):
0
Enter pulsed value (Volts/Amps):
5
Enter delay time (seconds):
0
Enter rise time (seconds):
5n
Enter fall time (seconds):
5n
Enter pulse width (seconds):
160m
Enter period (seconds):
320m
Add parameters for pulse source v10
Enter initial value (Volts/Amps):
0
Enter pulsed value (Volts/Amps):
5
Enter delay time (seconds):
0
Enter rise time (seconds):
5n
Enter fall time (seconds):
5n
Enter pulse width (seconds):
160m
Enter period (seconds):
320m


Analysis
Source Details
Ngspice Model
Device Modeling
Subcircuits
Add parameters for pulse source v11
Enter initial value (Volts/Amps):
0
Enter pulsed value (Volts/Amps):
5
Enter delay time (seconds):
0
Enter rise time (seconds):
5n
Enter fall time (seconds):
5n
Enter pulse width (seconds):
320m
Enter period (seconds):
640m
Add parameters for pulse source v12
Enter initial value (Volts/Amps):
0
Enter pulsed value (Volts/Amps):
5
Enter delay time (seconds):
0
Enter rise time (seconds):
5n
Enter fall time (seconds):
5n
Enter pulse width (seconds):
320m
Enter period (seconds):
640m

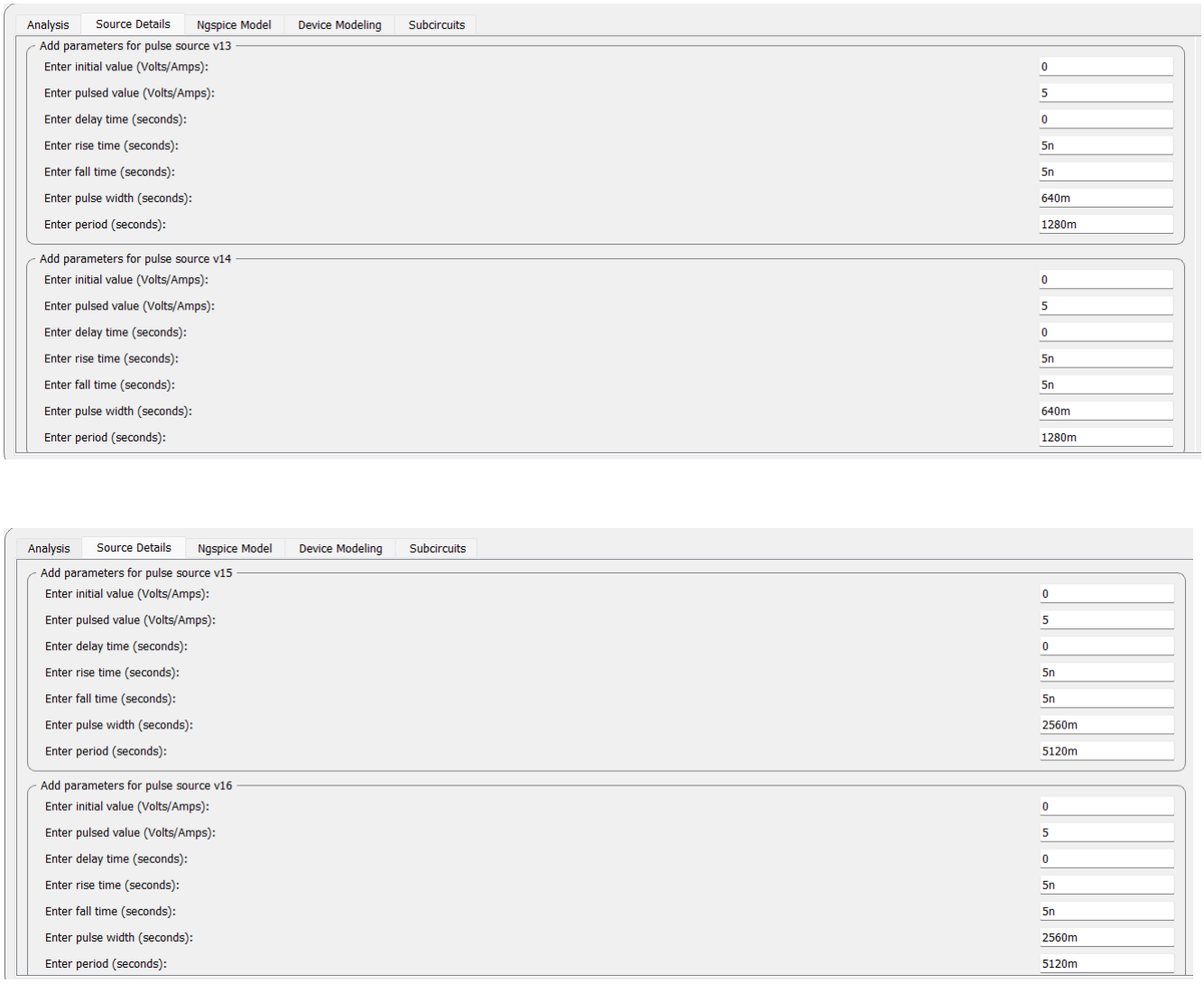



Figure 14.5: Source Details of SN74LS684

## 14.9 Input Plots

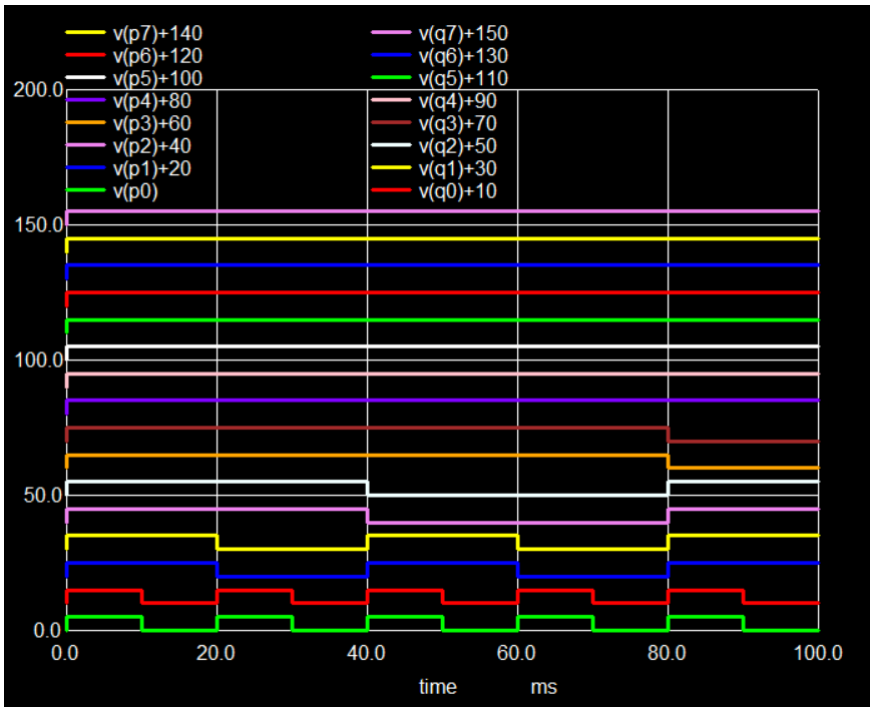



Figure 14.6: Input Plot of SN74LS684

## 14.10 Output Plots

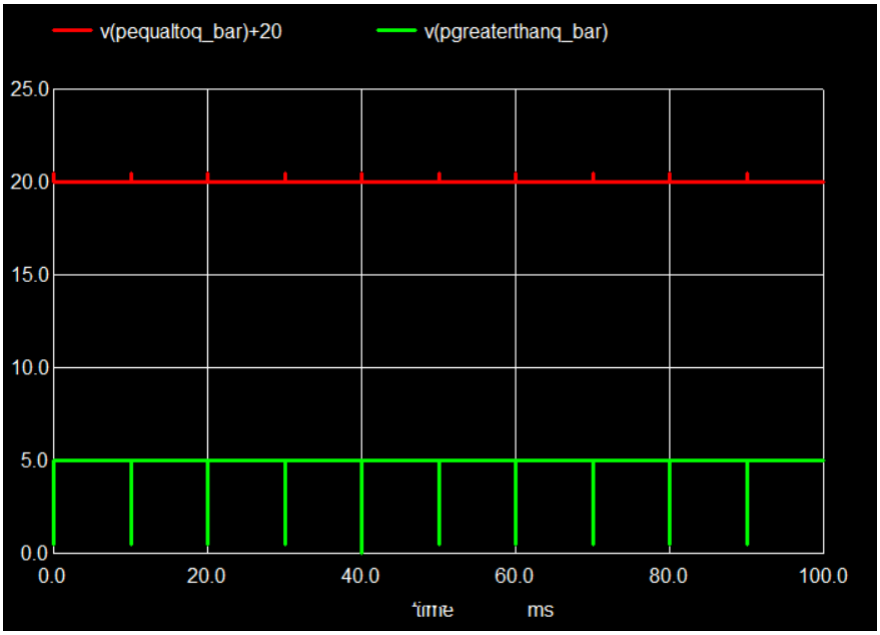



Figure 14.7: Output Plot of SN74LS684

# Chapter 15

# SN7495A

## 15.1 General Description

**4-Bit Parallel-Access Shift Registers** The SN7495A is a versatile 4-bit shift register that supports both serial and parallel data handling, allowing for efficient data movement and manipulation in digital circuits. It offers three modes of operation:

1. Parallel (broadside) load
2. Shift right (data moves from QA to QD)
3. Shift left (data moves from QD to QA)

Parallel loading occurs when the mode control input is high and data is latched on the high-to-low transition of clock 2, during which serial data input is disabled. In shift right mode (mode control low), data is shifted on the high-to-low transition of clock 1, while in shift left mode (mode control high), shifting happens on the high-to-low transition of clock 2, with each flip-flop receiving data from its neighbor. The register allows serial data to be entered at one end while shifting occurs, enabling dynamic data flow. For synchronized operation, clock 1 and clock 2 can be tied together, and care must be taken to change the mode control only when both clocks are low, though internal protection ensures data integrity during switching.

## 15.2 Key Features

The key features of SN7495A includes:

- **4-bit Universal Shift Register:** It handles both parallel and serial data inputs and outputs.
- **Dual Clock Inputs:** It has separate control for parallel loading (clock 2) and shifting (clock 1 for right, clock 2 for left).
- **Mode Control Input:** It determines operation type (load or shift).
- **Internal Data Protection:** Register contents remain protected during mode transitions.

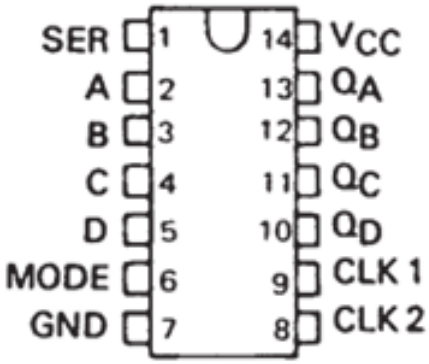
- **Edge-Triggered Operation:** Shifting and loading occur on the high-to-low transition of the clock signals.
- **TTL Logic Compatibility:** It operates reliably within standard TTL logic levels.

## 15.3 Application

The applications of SN7495A includes:

- **Shift Register Memory:** It can implement basic memory or delay lines
- **Data Manipulation in ALUs:**It assists in bitwise data shifting operations..
- **Data Storage and Transfer:** It is used in temporary data holding and movement across systems.
- **Control Units :** It can be used in finite state machines and control logic for stepping through states.

## 15.4 Pin Diagram



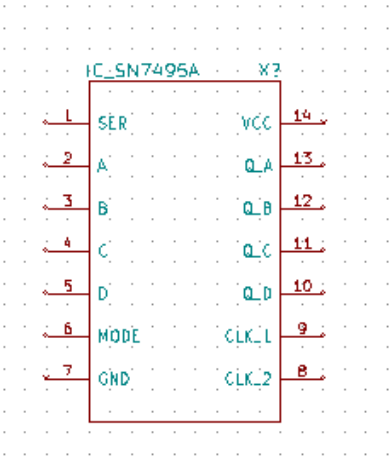




Figure 15.1: Pin diagram of SN7495A

## 15.5 Subcircuit Schematic Diagram

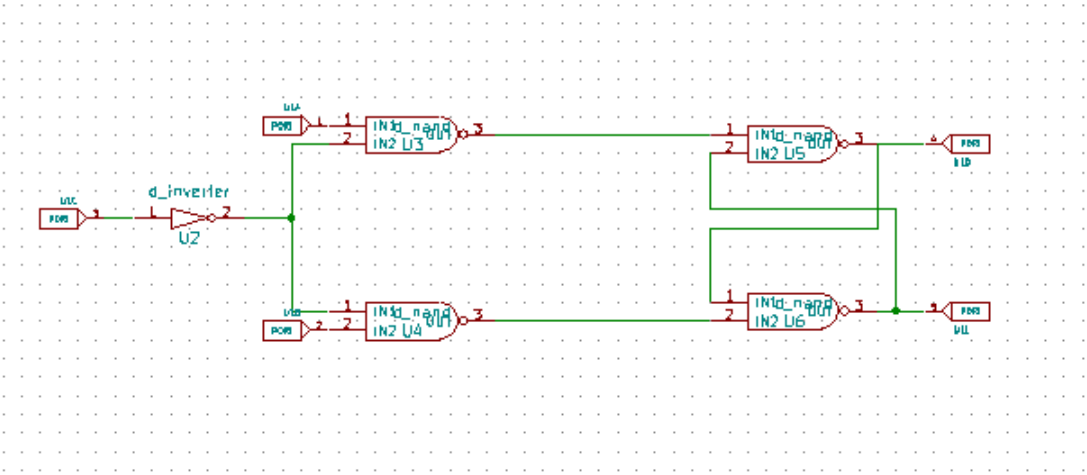



Figure 15.2: Subcircuit Schematic Diagram of Custom-made SR Flip Flop

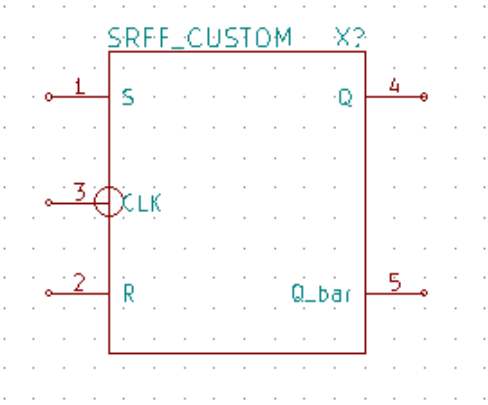



Figure 15.3: Symbol used for SR Flip Flop

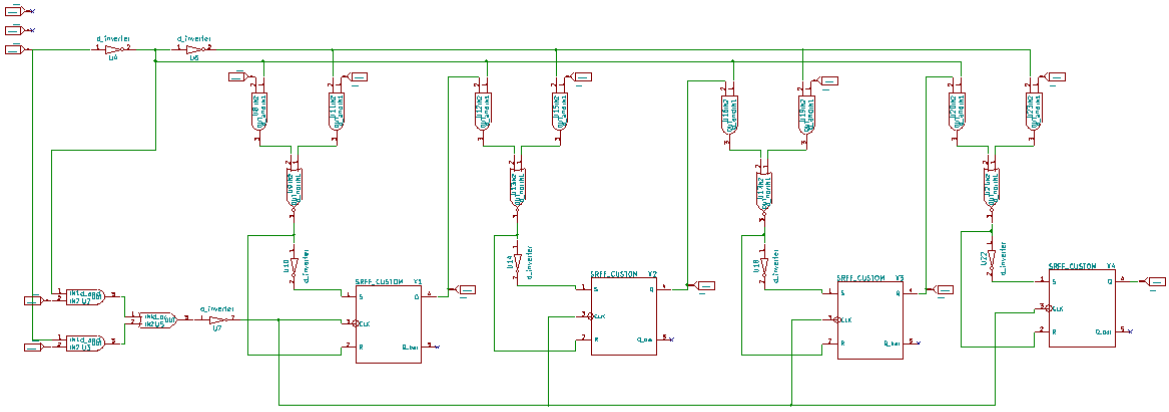


Figure 15.4: Subcircuit Schematic Diagram of SN7495A

## 15.6 Test Circuit Schematic Diagram

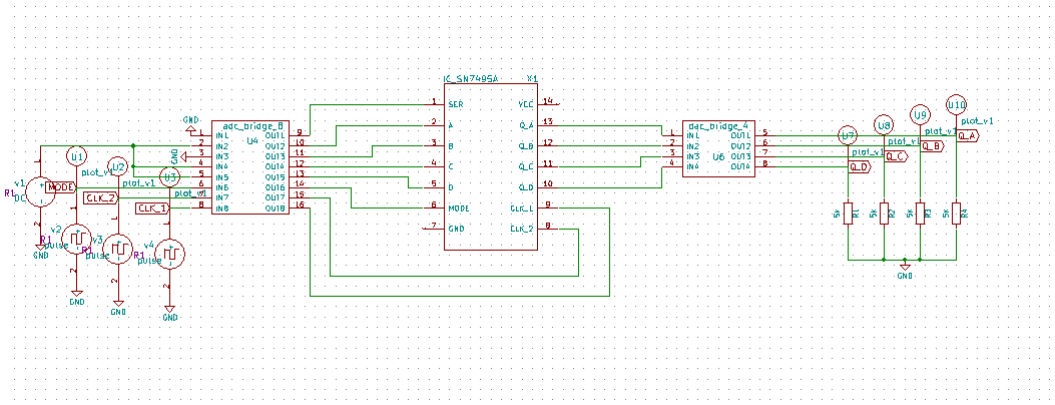


Figure 15.5: Test Circuit Schematic Diagram of SN7495A

## 15.7 Analysis details

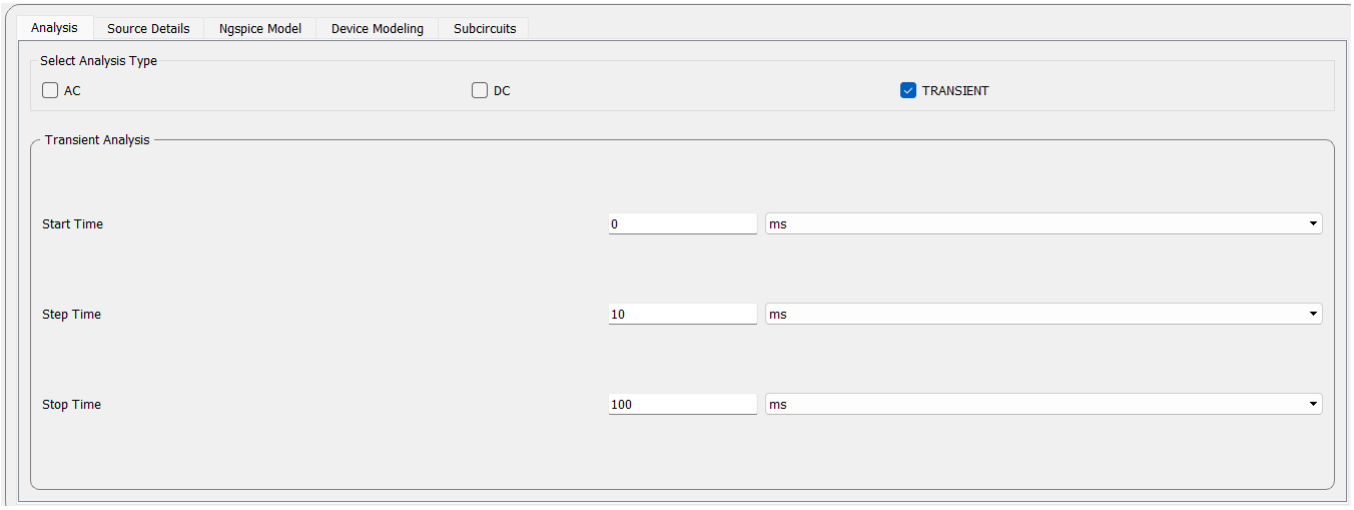
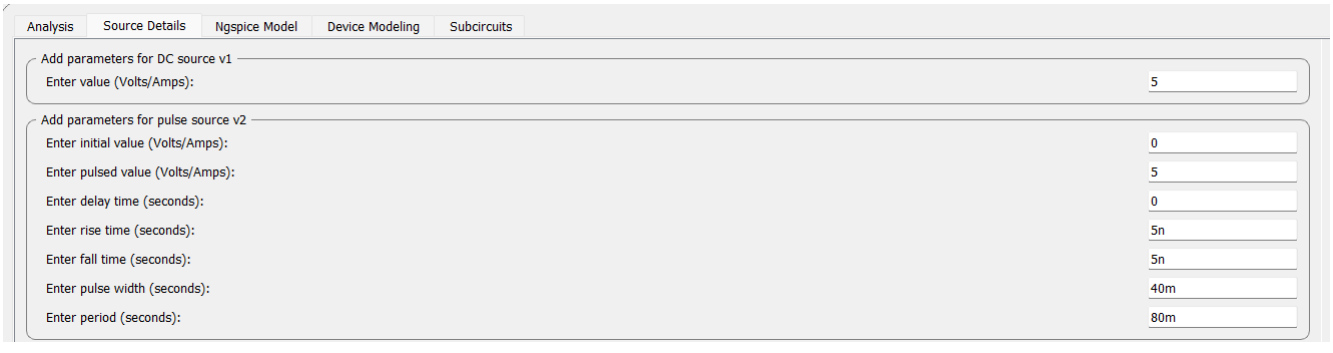



Figure 15.6: Analysis details of SN7495A

## 15.8 Source Details



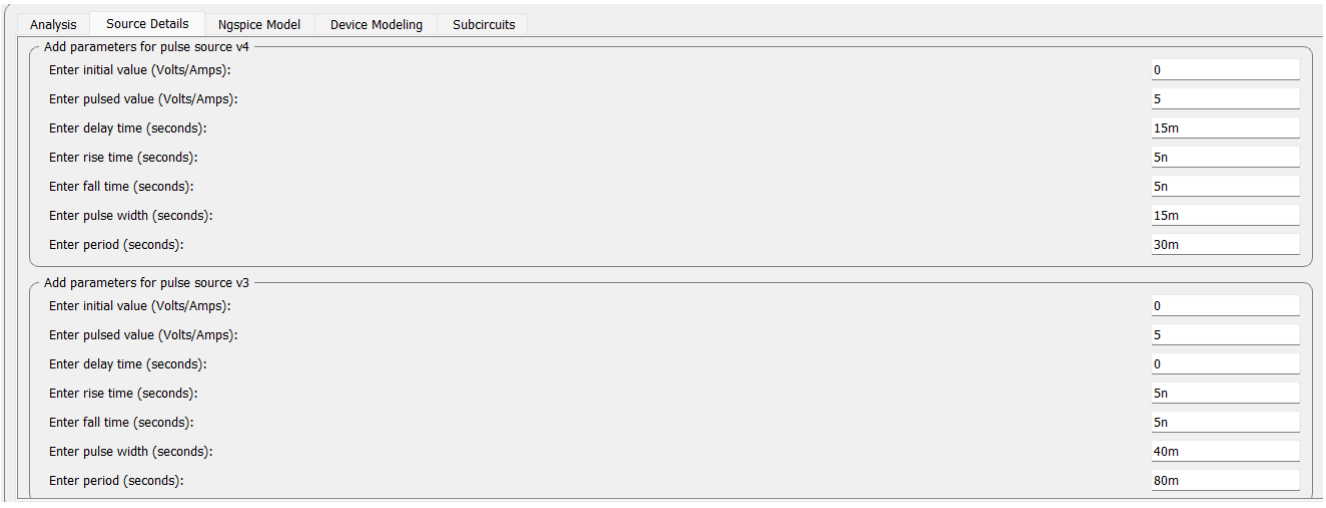




Figure 15.7: Source Details of SN7495A

## 15.9 Input Plots

**Test Condition : Parallel Loading when Mode Control is High**

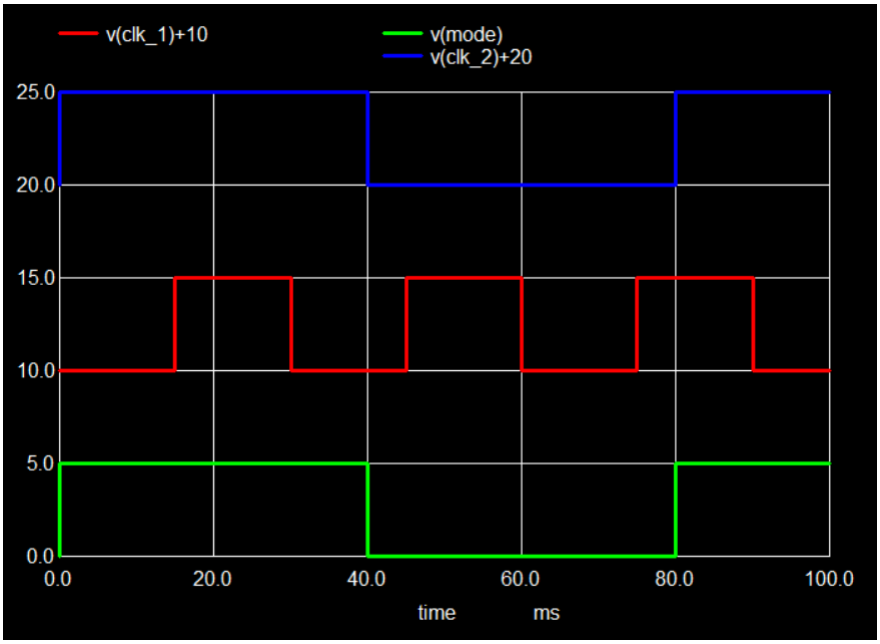



Figure 15.8: Input Plot of SN7495A

## 15.10 Output Plots

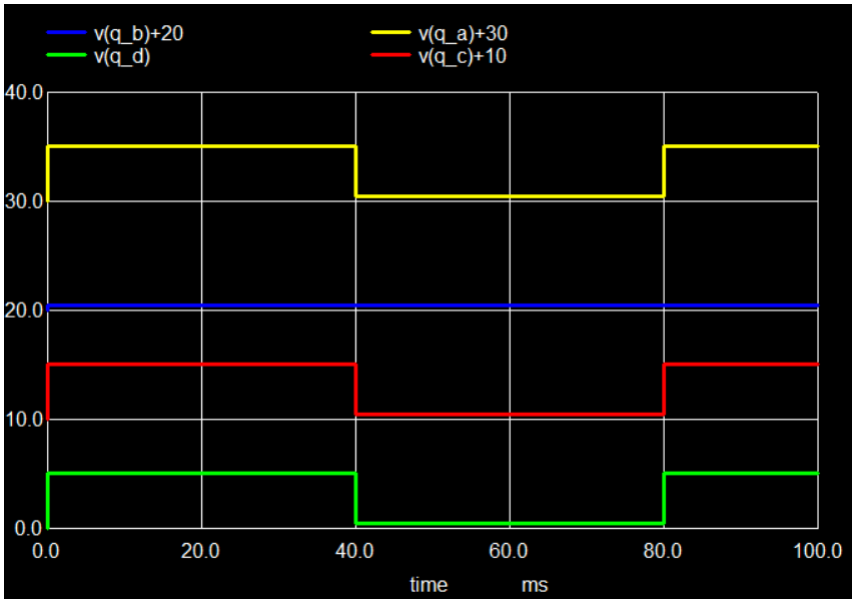



Figure 15.9: Output Plot of SN7495A

# Chapter 16

# 74F382

## 16.1 General Description

**4-Bit Arithmetic Logic Unit**
The SN74F382 is a high-speed 4-bit arithmetic logic unit (ALU) capable of performing six functionsthree arithmetic and three logic operationson two 4-bit inputs, A and B. It includes additional select inputs that can force the outputs to all LOW (clear) or all HIGH (preset), enabling flexible control. The device features a carry output for ripple expansion when chaining multiple ALUs and an Overflow output for two's complement arithmetic operations, aiding in accurate signed computations. Designed for low input loading, the SN74F382 reduces drive requirements, making it suitable for high-performance digital systems. For enhanced speed in multi-bit operations, it can be paired with a carry lookahead generator like the SN74F381.

## 16.2 Key Features

The key features of 74F382 includes:

- **Function Select Inputs:** It allows forced LOW (clear) or HIGH (preset) output states.
- **Overflow Output:** It is useful for twos complement arithmetic and signed number operations.
- **Carry Output:** It enables ripple expansion for building multi-bit ALUs.
- **Low Input Loading:** It reduces drive requirements for connected components..
- **High-Speed Operation:** It is suitable for fast arithmetic and logic computations.

## 16.3 Application

The applications of 74F382 includes:

- **Data Manipulation in Microprocessor:** It performs operations like addition, subtraction, AND, OR, etc.
- Logic Implementation:It helps execute logical decision-making in control units.
- **Multi-bit ALU Design:** It forms part of extended-bit arithmetic systems using carry chaining or lookahead.
- **High-Speed Computing Circuits:** It is suitable for time-critical data processing.

## 16.4 Pin Diagram

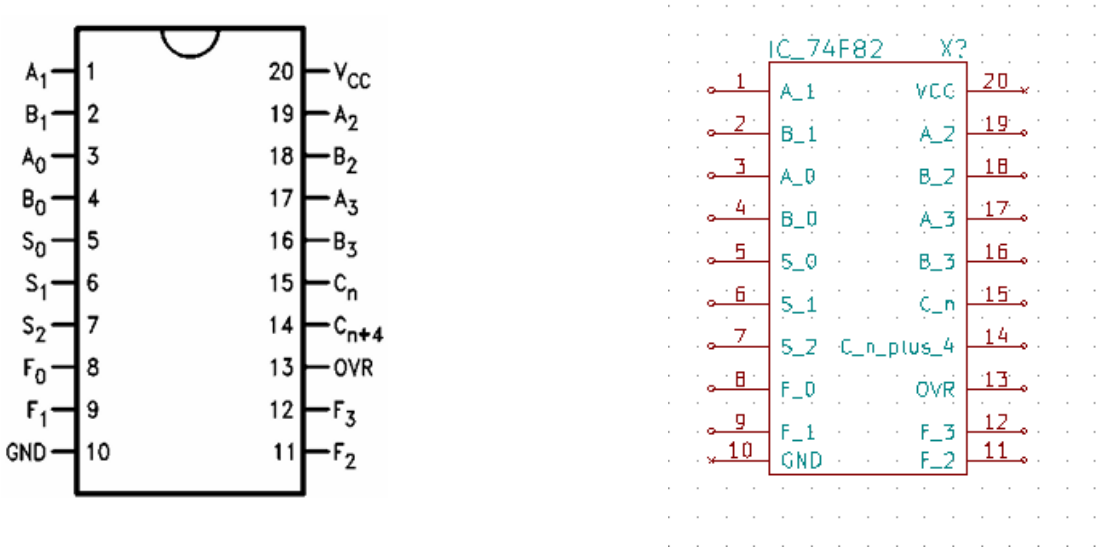



Figure 16.1: Pin diagram of 74F382

## 16.5 Subcircuit Schematic Diagram

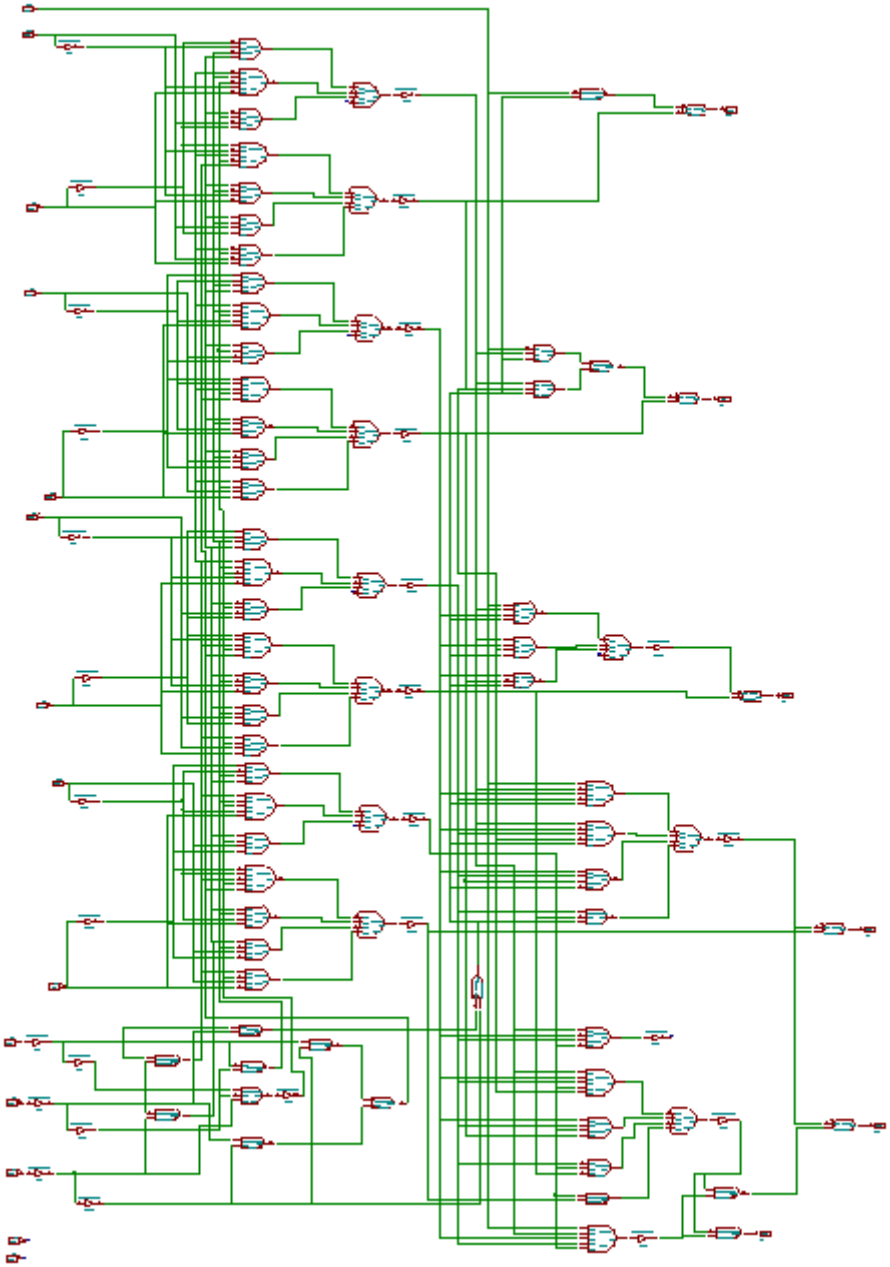


Figure 16.2: Subcircuit Schematic Diagram of 74F382

## 16.6 Test Circuit Schematic Diagram

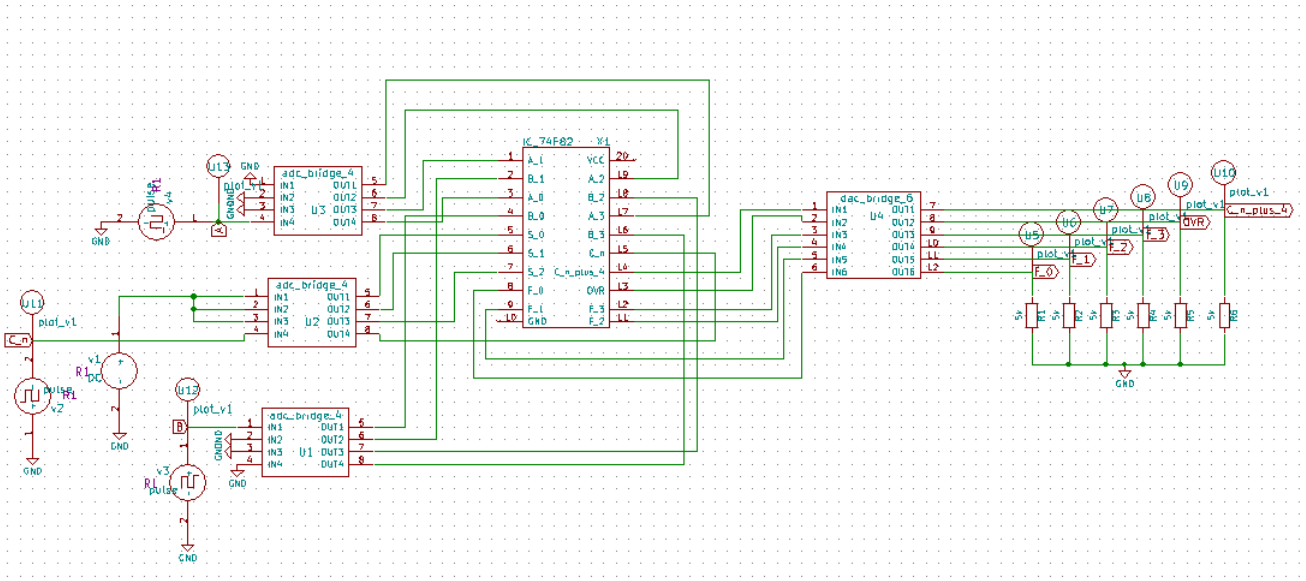



Figure 16.3: Test Circuit Schematic Diagram of 74F382

## 16.7 Analysis details

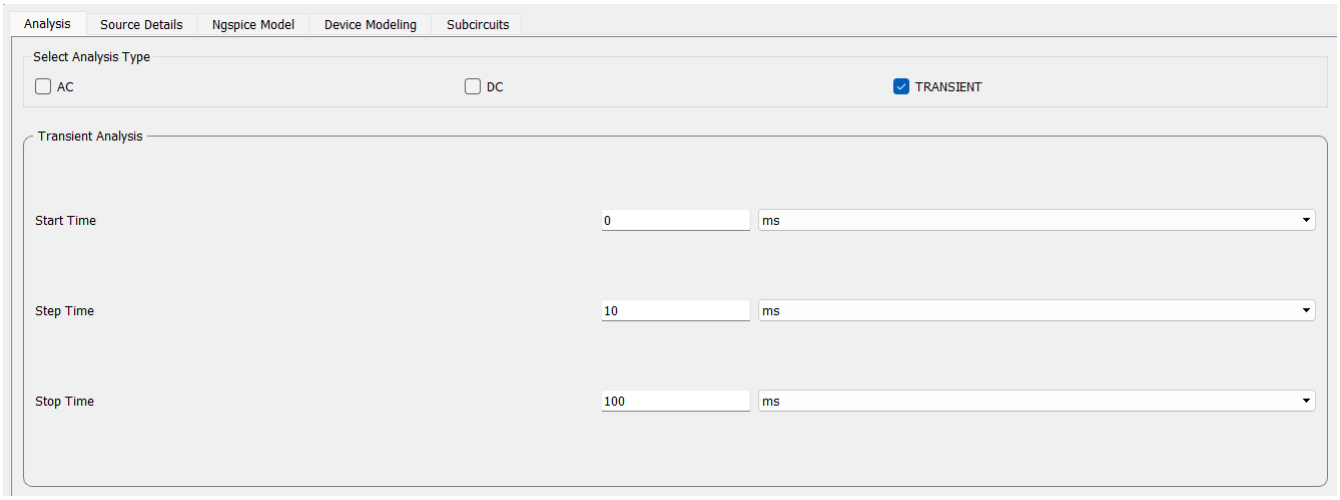



Figure 16.4: Analysis details of 74F382

## 16.8 Source Details

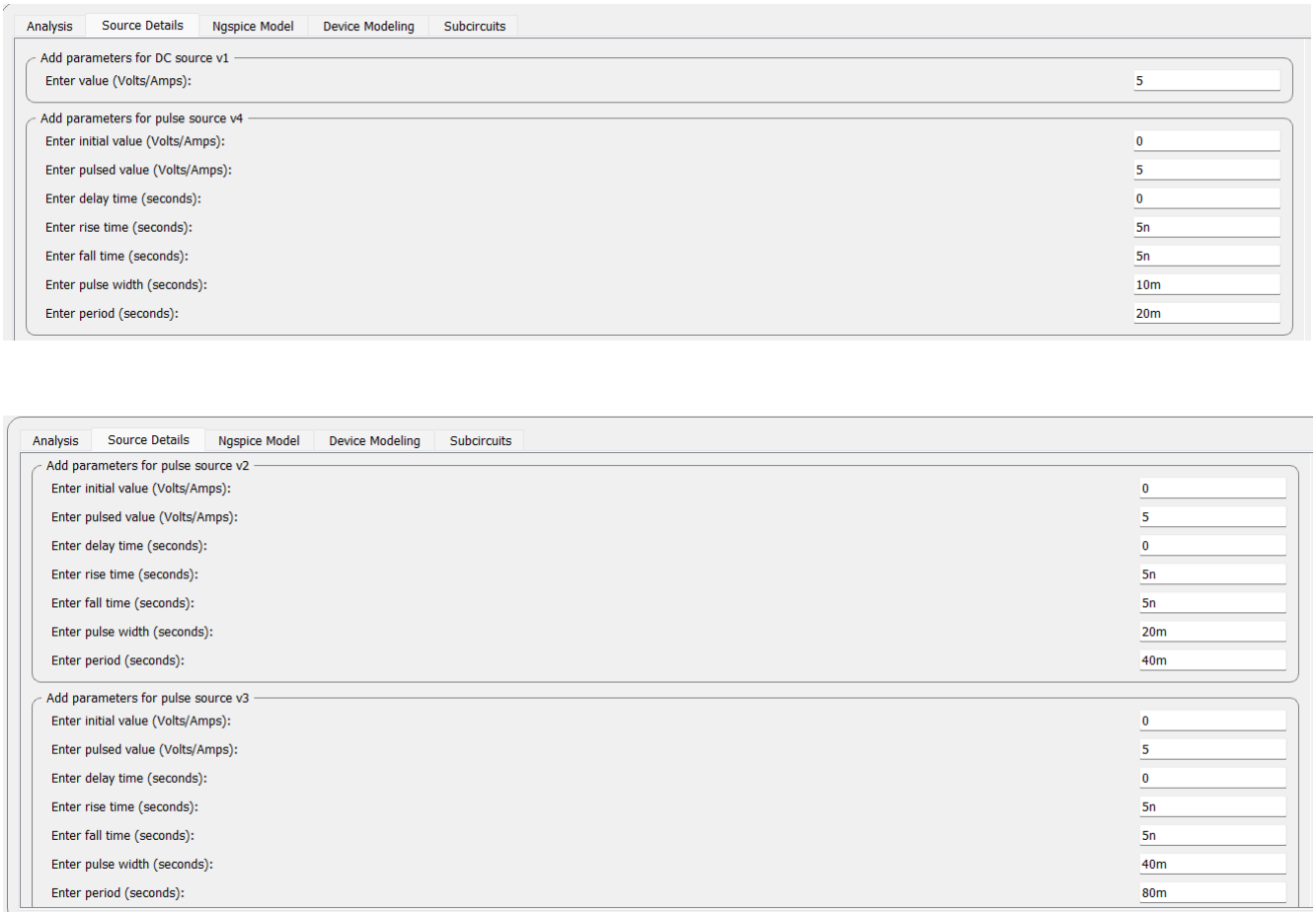



Figure 16.5: Source Details of 74F382

## 16.9 Input Plots

**Test Condition : Preset**

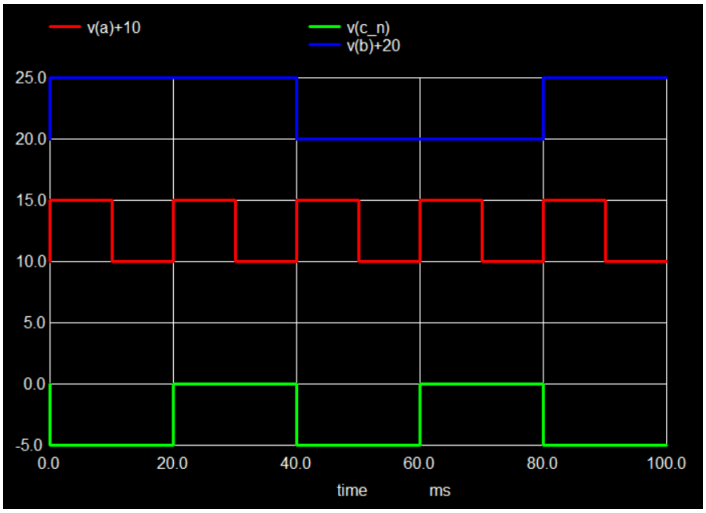



Figure 16.6: Input Plot of 74F382

## 16.10 Output Plots

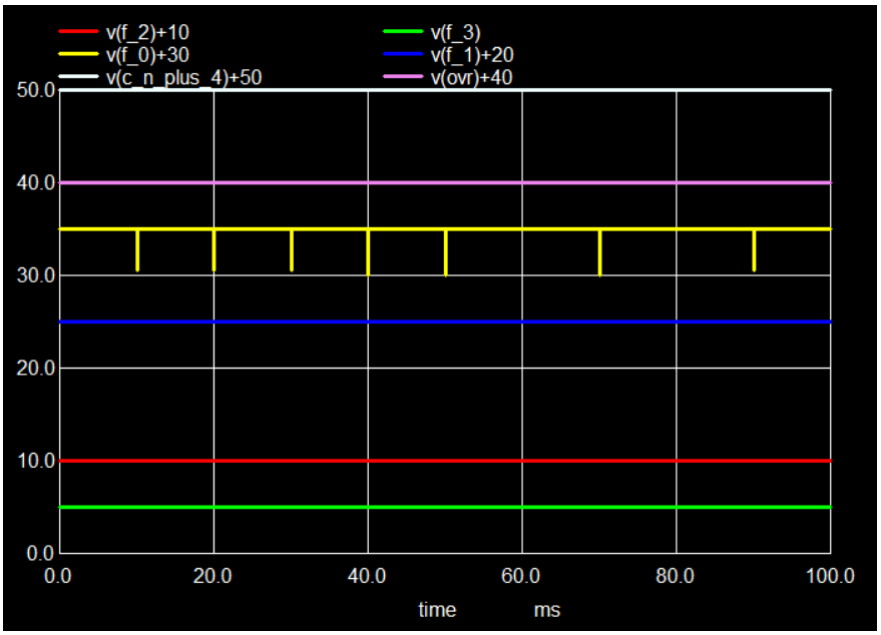



Figure 16.7: Output Plot of 74F382

# Chapter 17

# 74LCX112

## 17.1 General Description

**Low Voltage Dual J-K Negative Edge-Triggered Flip-Flop with 5V Tolerant Inputs**
The 74LCX112 is a dual J-K flip-flop featuring independent J, K, CLOCK, PRESET, and CLEAR inputs for each flip-flop, with both Q and $\overline{Q}$ outputs. It is edge-triggered and changes state on the falling edge (negative transition) of the clock signal. The asynchronous CLEAR and PRESET inputs operate independently of the clock and are activated by a LOW logic level. Designed for low-voltage systems (2.3V3.6V), it is also fully 5V-tolerant, making it suitable for mixed-voltage environments. Built using advanced CMOS technology, the device offers high-speed performance, low power consumption, and features such as high output drive, noise/EMI reduction, and robust ESD and latch-up protection.

## 17.2 Key Features

The key features of 74LCX112 includes:

- **Negative edge-triggered:** It changes state on the falling edge of the clock pulse.
- **Excellent Latch-Up Immunity:** It withstands currents exceeding 500 mA.
- **5V Tolerant Inputs:** It can interface with 5V logic levels in mixed-voltage systems.
- **Low Voltage Operation:** It supports $V_{CC}$ from 2.3V to 3.6V.
- **High-Speed Operation:** Propagation delay ($t_{PD}$) is as low as 7.5 ns at 3.3V.
- **Low Power Consumption:** It can tolerate maximum $I_{CC}$ of 10 A.
- **High Output Drive:** It gives 24 mA output current at 3.0V.

## 17.3 Application

The applications of 74LCX112 includes:

- **Frequency dividers:** It can be used to divide the frequency of a clock signal.
- **Sequential Logic Circuits:**It can be used as core component in counters, registers, and FSMs.
- **Clocked Storage Elements:** It is used in latching or temporary data storage.
- **Mixed-Voltage Digital Systems :** It is suitable for 3.3V systems that interact with 5V logic.

## 17.4 Pin Diagram

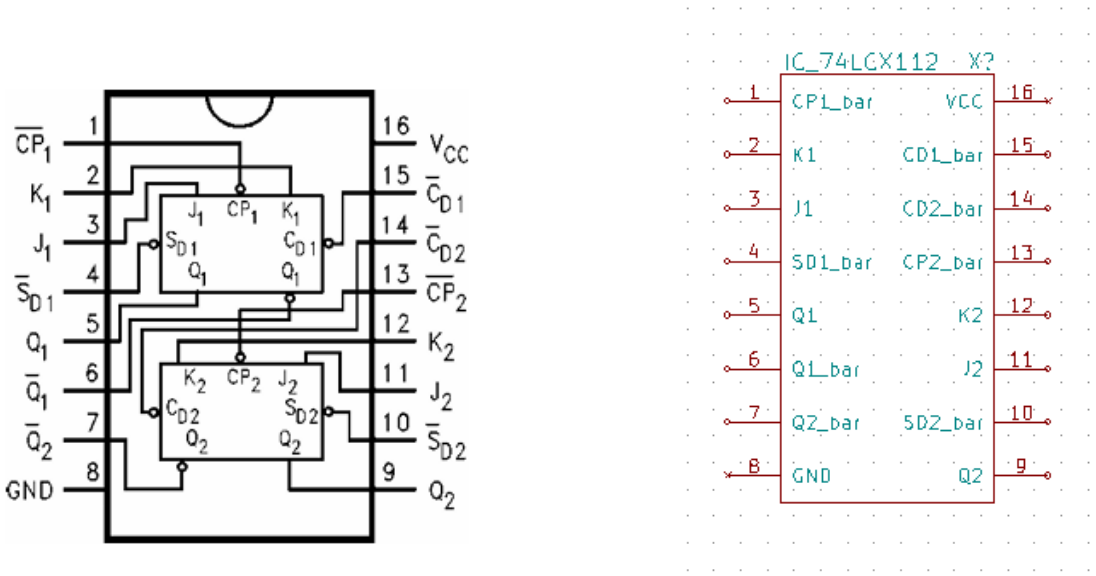



Figure 17.1: Pin diagram of 74LCX112

## 17.5 Subcircuit Schematic Diagram

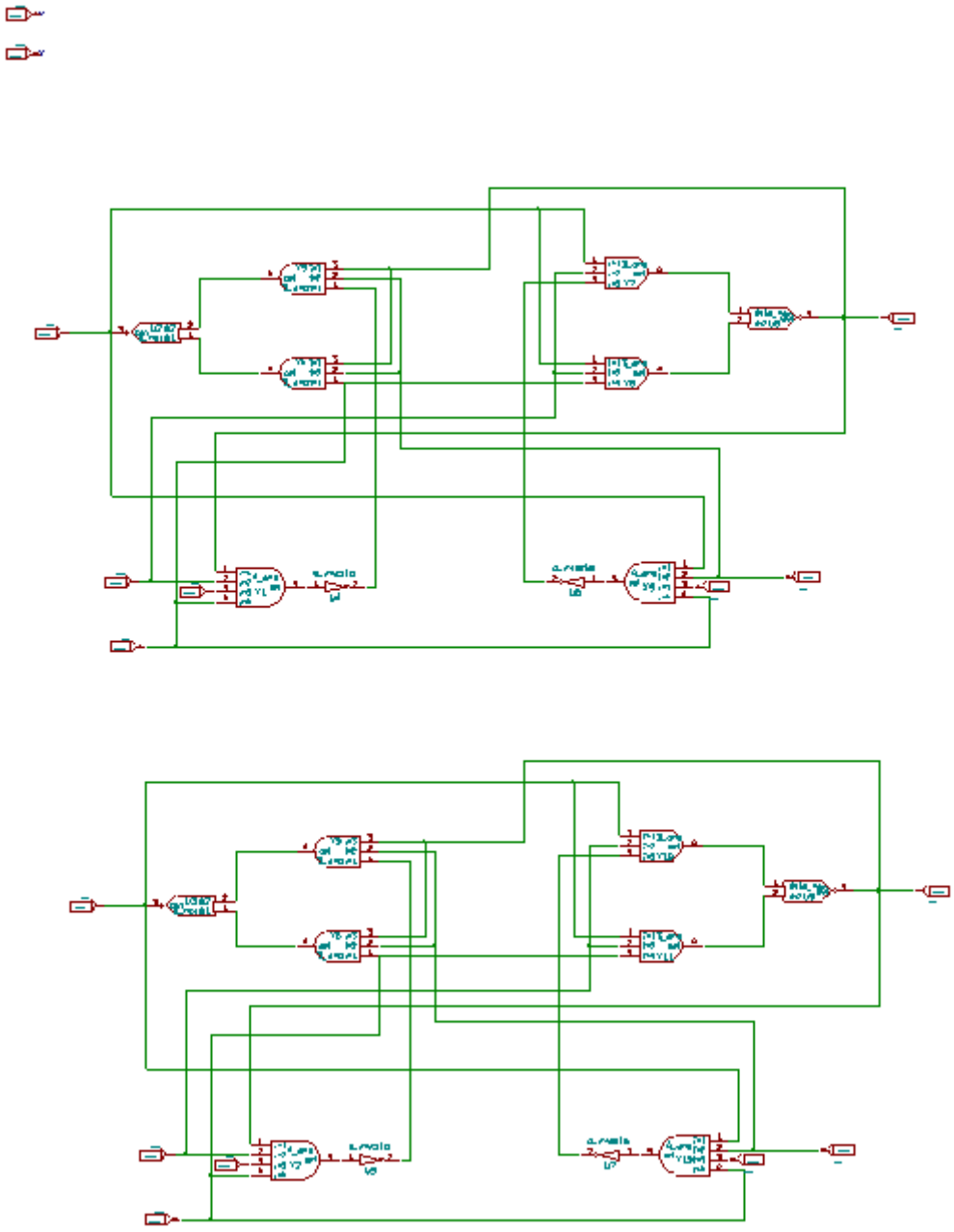


Figure 17.2: Subcircuit Schematic Diagram of 74LCX112

## 17.6 Test Circuit Schematic Diagram

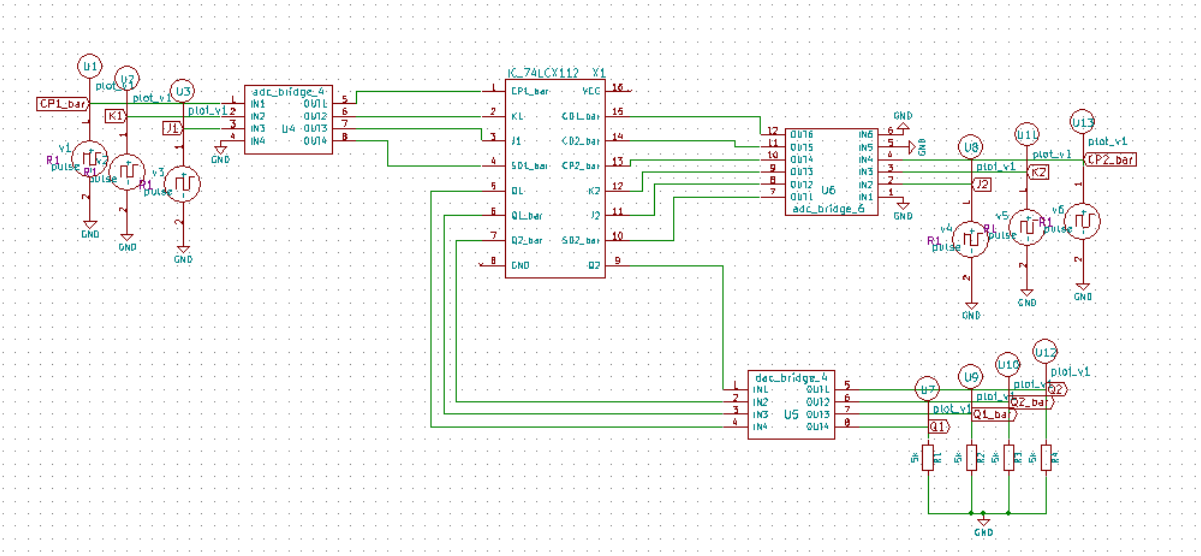


Figure 17.3: Test Circuit Schematic Diagram of 74LCX112

## 17.7 Analysis details

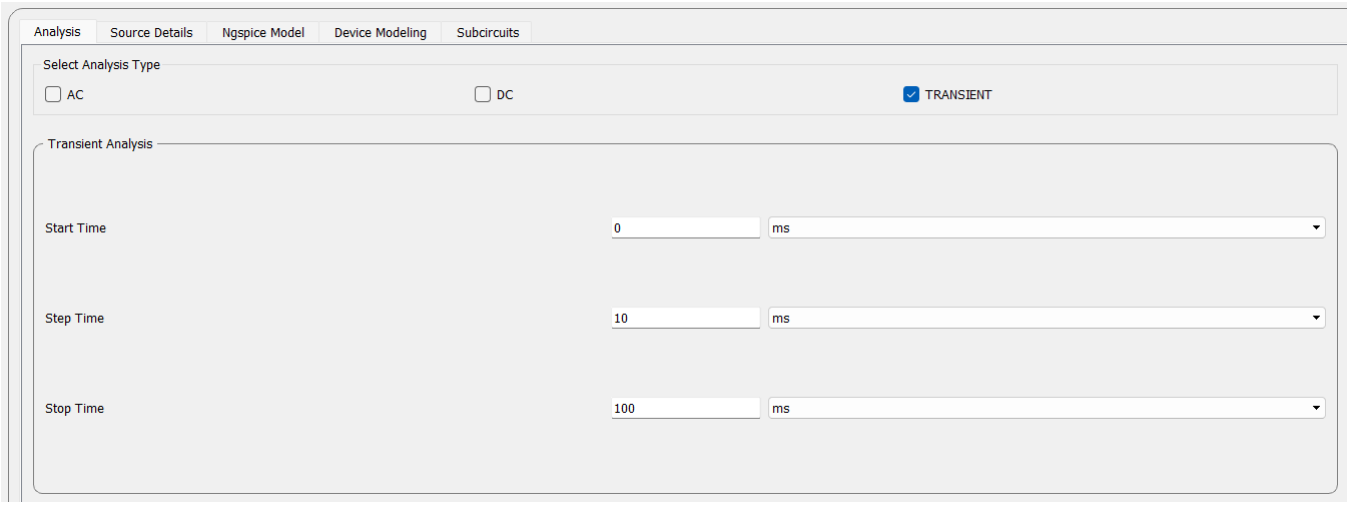



Figure 17.4: Analysis details of 74LCX112

## 17.8 Source Details

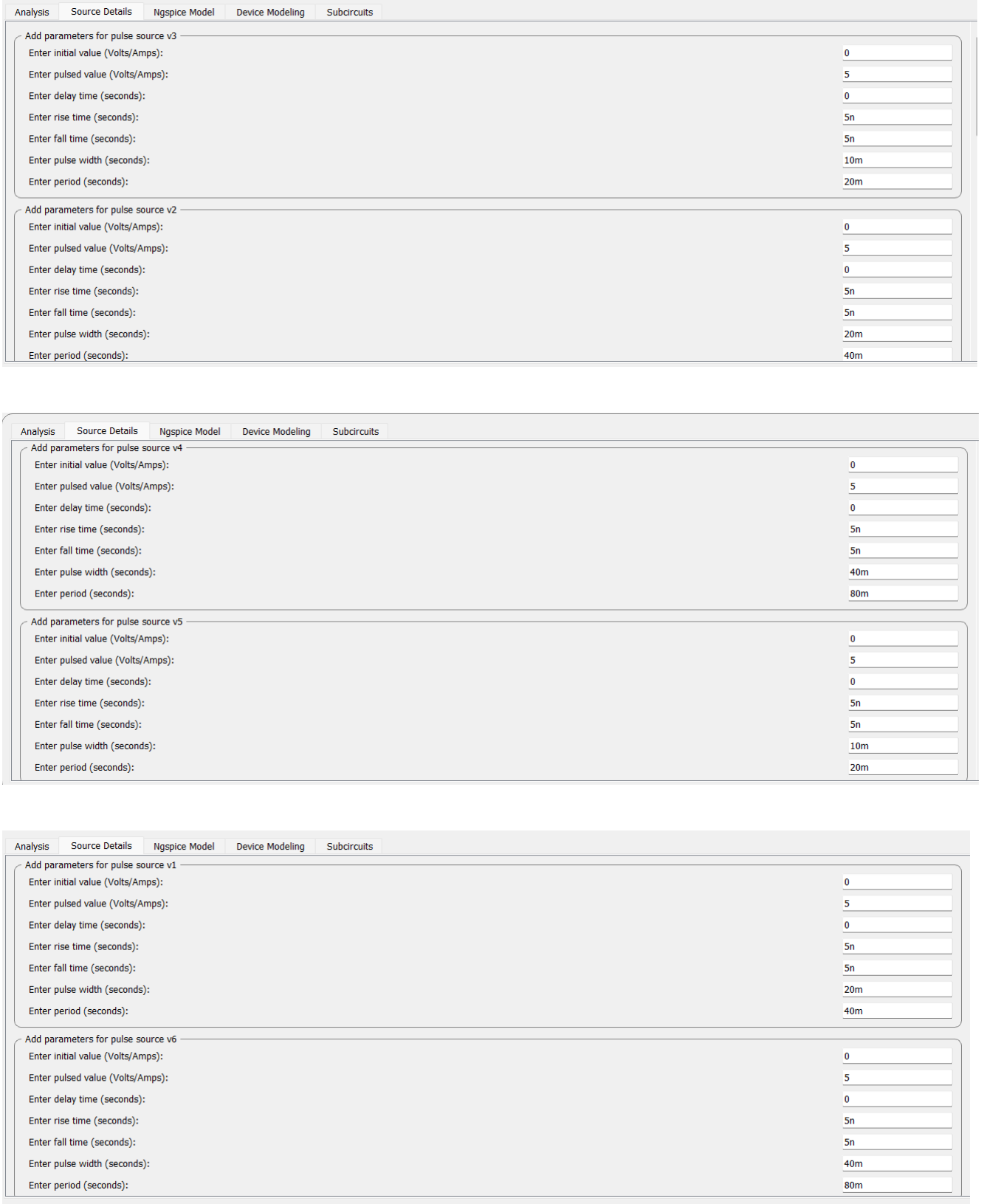



Figure 17.5: Source Details of 74LCX112

## 17.9 Input Plots

**Test condition : Forced Reset**

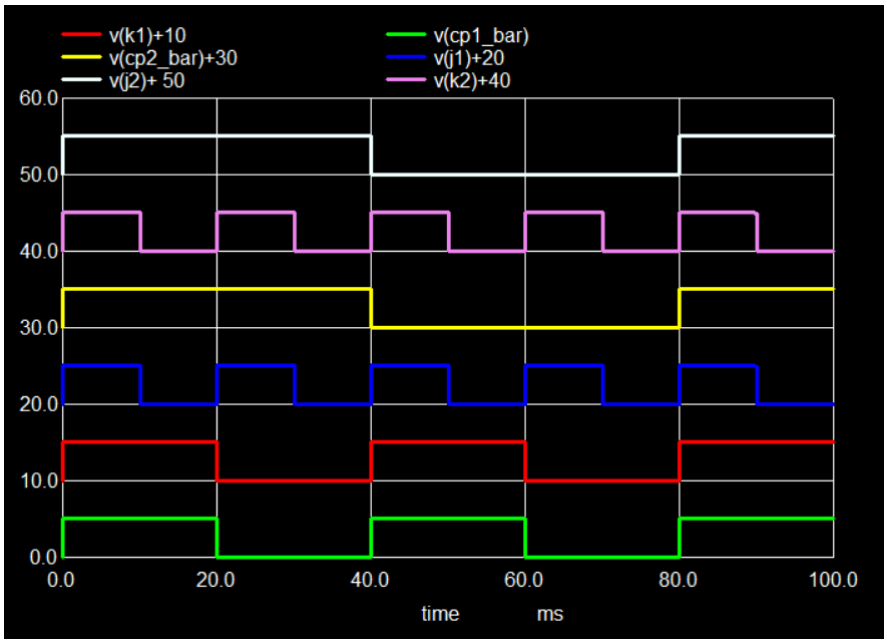



Figure 17.6: Input Plot of 74LCX112

## 17.10 Output Plots

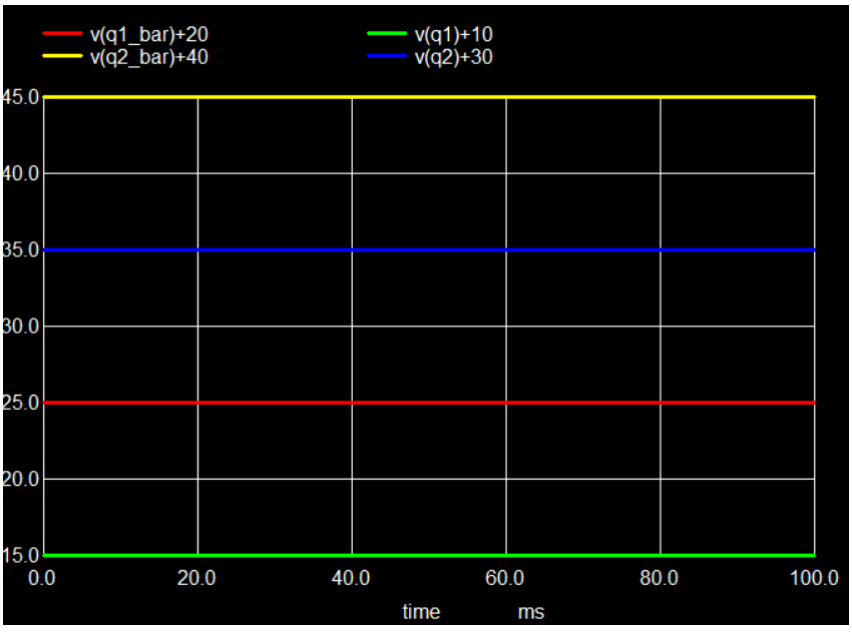



Figure 17.7: Output Plot of 74LCX112

# Chapter 18

# SN7451

## 18.1 General Description

**And-Or Invert Gates**
The SN7451 is a dual 2-wide 2-input AND-OR-INVERT (AOI) gate, which performs the Boolean function $Y = \overline{AB + CD}$. It includes two independent logic circuits that combine two 2-input AND gates, whose outputs are fed into a NOR gate, achieving complex logic functions in a single package. This gate is ideal for reducing the number of discrete logic components required in a digital circuit. The SN7451 is designed for operation in commercial temperature ranges and is available in various package types, including plastic and ceramic forms. Its high reliability and integration of multiple logic functions make it a useful component in compact and efficient digital designs.

## 18.2 Key Features

The key features of SN7451 includes:

- **Integrated Logic:** It combines AND and NOR logic in a single package to simplify circuit design.
- **Standard TTL Compatibility:** It is designed to interface with standard TTL logic levels.
- **Commercial Temperature Range:** It operates reliably from 0C to 70C.

## 18.3 Application

The applications of SN7451 includes:

- **Control Systems:** It helps in decision-making logic where multiple conditions must be evaluated.
- **Compact Logic Design:**It reduces gate count in dense digital circuits.
- **Arithmetic and Processing Units:** It is used in control paths or logic conditions in ALUs or CPUs.

## 18.4 Pin Diagram

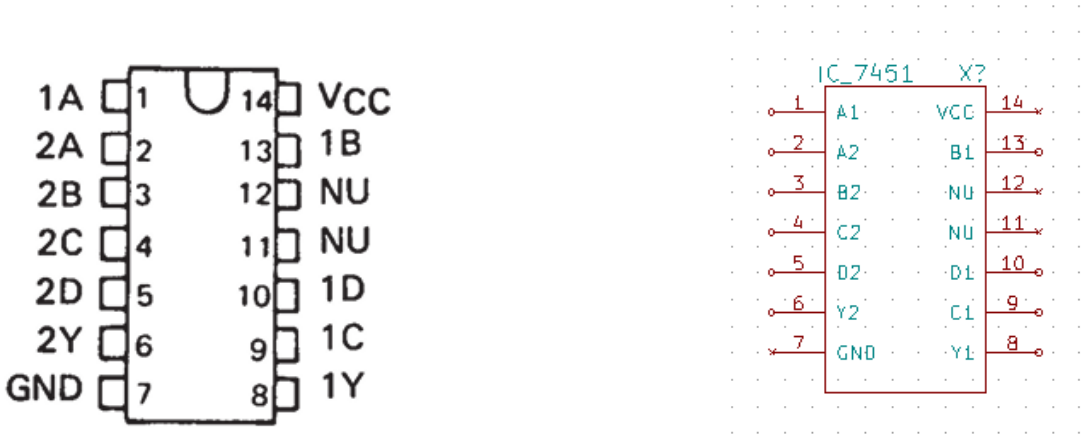



Figure 18.1: Pin diagram of SN7451

## 18.5 Subcircuit Schematic Diagram

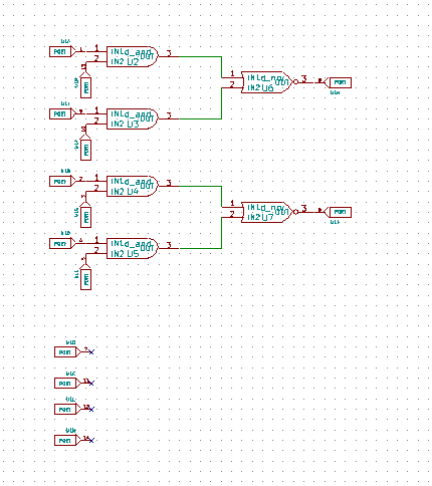


Figure 18.2: Subcircuit Schematic Diagram of SN7451

## 18.6 Test Circuit Schematic Diagram

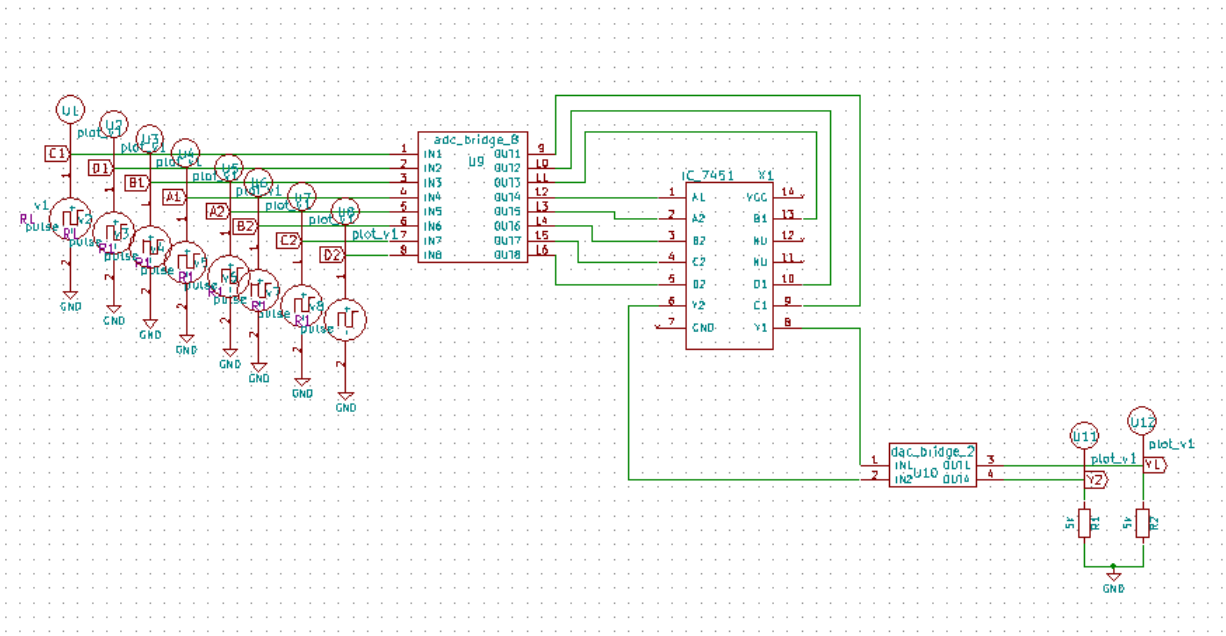



Figure 18.3: Test Circuit Schematic Diagram of SN7451

## 18.7 Analysis details

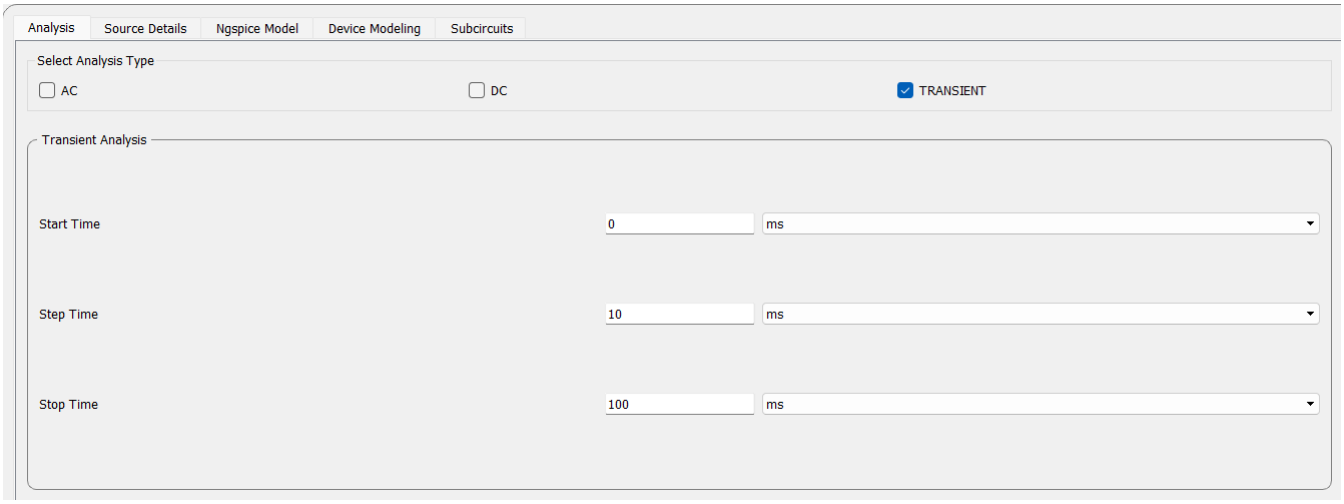



Figure 18.4: Analysis details of SN7451

## 18.8 Source Details

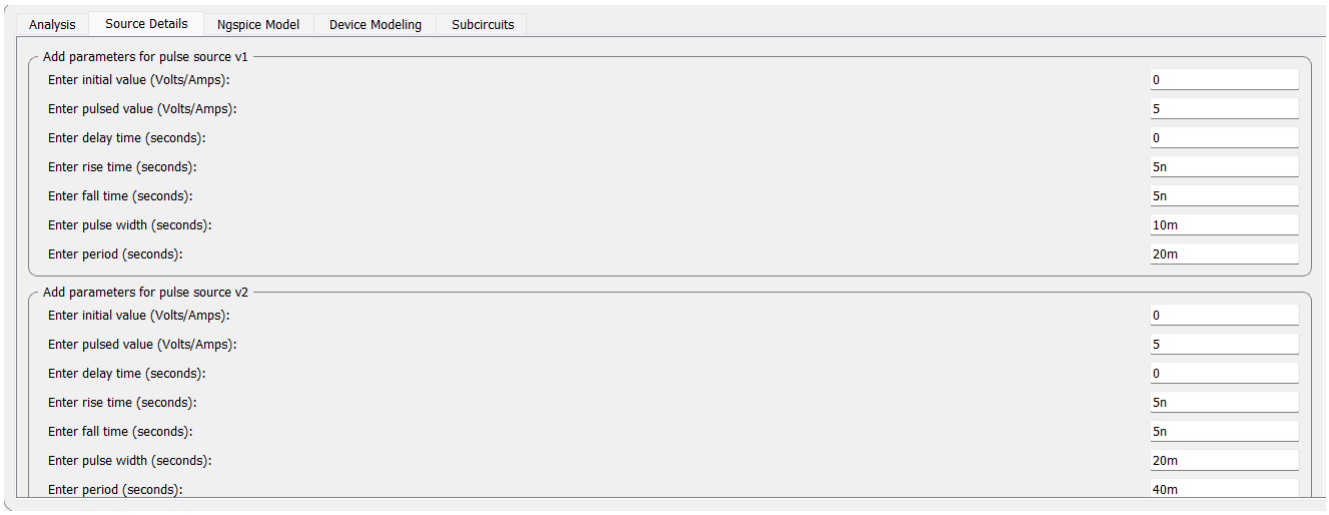





Figure 18.5: Source Details of SN7451

## 18.9 Input Plots

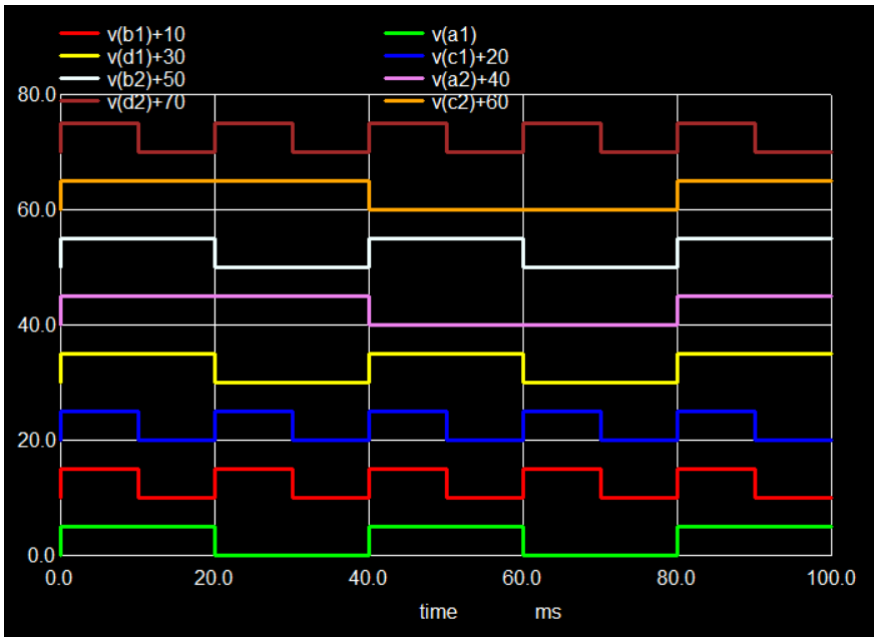



Figure 18.6: Input Plot of SN7451

## 18.10 Output Plots

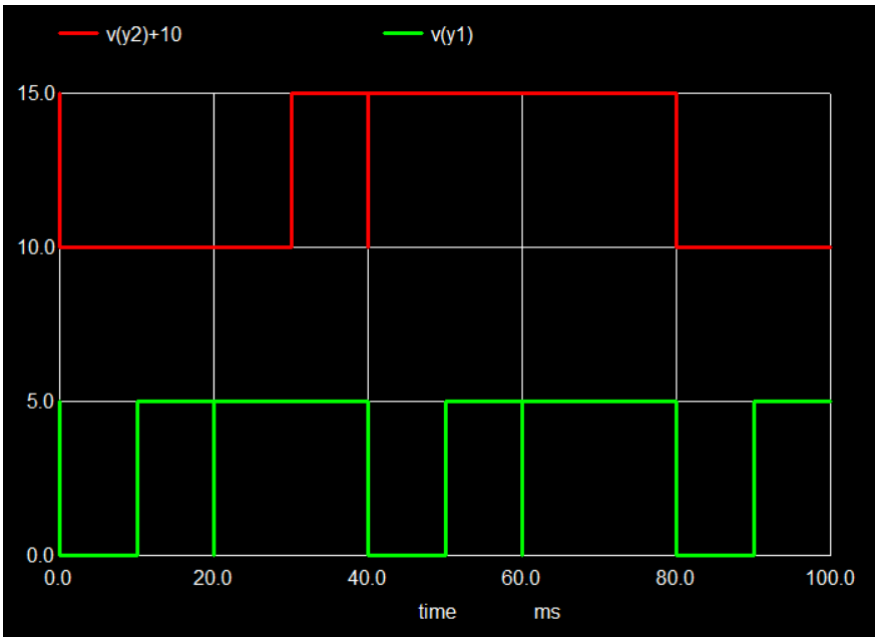



Figure 18.7: Output Plot of SN7451

# Chapter 19

# SN74F175

## 19.1 General Description

**Quadruple D-Type Flip-Flop With Clear**
The SN74F175 is a high-speed, quad D-type flip-flop that features positive-edge triggering and double-rail outputs, meaning both Q and $\overline{Q}$ outputs are available for each flip-flop. It incorporates TTL logic and includes a buffered clock input and a direct clear $\overline{CLR}$ input for asynchronous resetting. On the positive edge of the clock signal, the data present at the D inputs is transferred to the outputs, provided setup time conditions are met. When the clock is held high or low, the outputs remain unaffected by changes at the D input. This predictable clocked behavior and fast operation make the SN74F175 ideal for a range of synchronous logic applications such as registers, shift registers, and pattern generators.

## 19.2 Key Features

The key features of SN74F175 includes:

- **Buffered Clock Input:** The clock input is internally buffered, improving signal integrity and reducing susceptibility to noise during clock transitions.
- **Direct Clear Input:** A direct asynchronous clear input allows each flip-flop to be reset independently of the clock, offering fast initialization.
- **Positive-Edge Triggering:** State changes occur only on the rising edge of the clock signal, ensuring synchronous and predictable operation.
- **Stable Data Capture:** The outputs change only on valid clock edges; when the clock is held steady, D-input changes do not affect the outputs.

## 19.3 Application

The applications of SN74F175 includes:

- **Buffer and Storage Registers::** It can be used for capturing and holding data synchronously in digital systems.
- **Shift Registers::**It is suitable for designing shift registers that move data serially through a system under clock control.
- **Pattern Generators:** These are ideal for generating predefined bit patterns synchronized with the system clock.

## 19.4 Pin Diagram

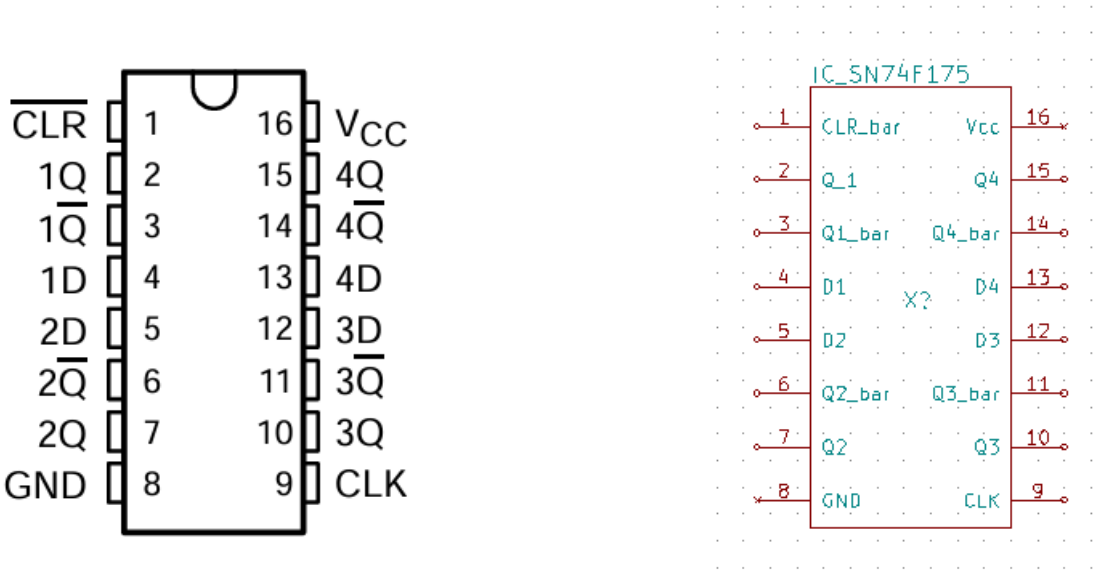



Figure 19.1: Pin diagram of SN74F175

## 19.5 Subcircuit Schematic Diagram

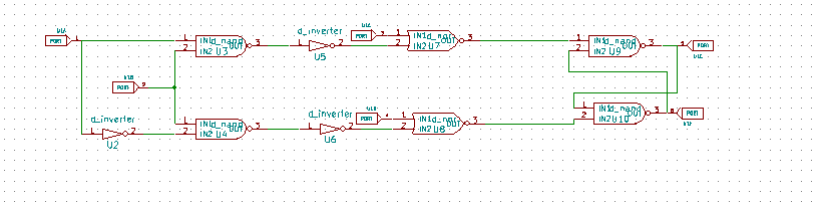


Figure 19.2: Subcircuit Schematic Diagram of Custom-made D Flip Flop

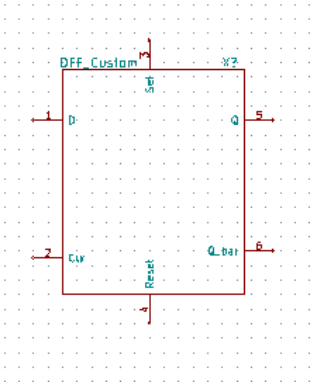



Figure 19.3: Symbol of Custom-made D Flip Flop

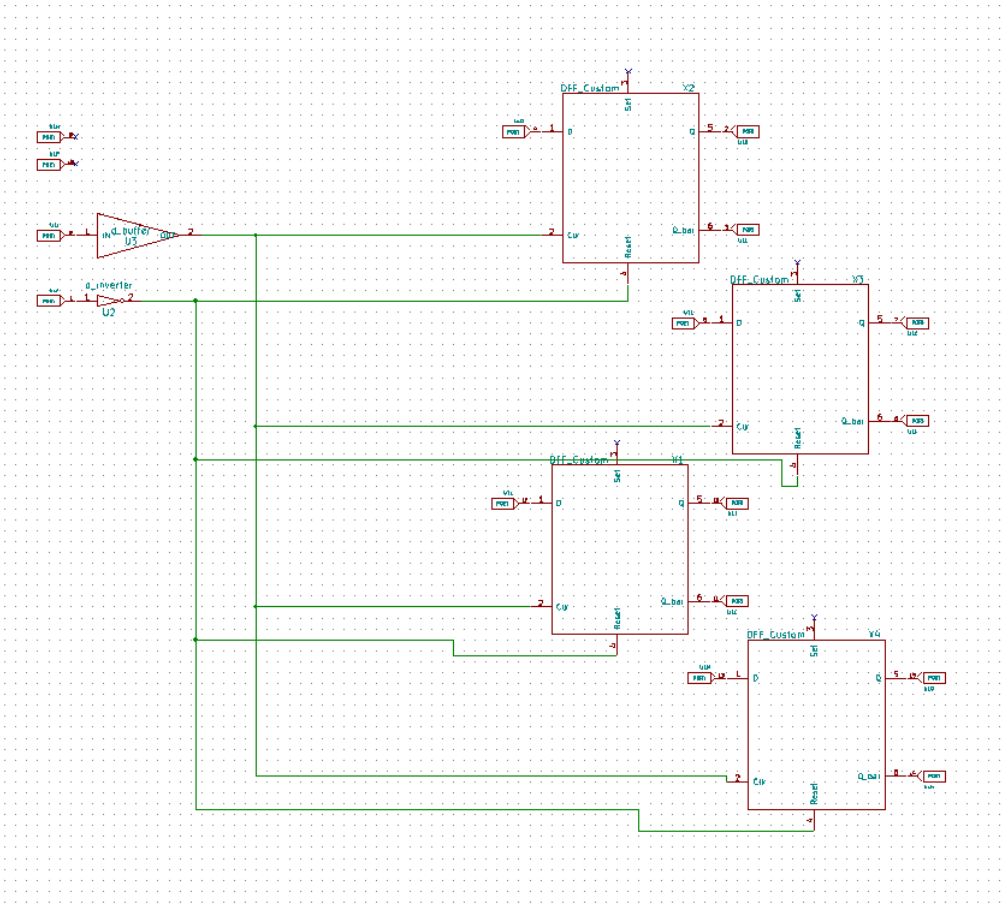



Figure 19.4: Subcircuit Schematic Diagram of SN74F175

## 19.6 Test Circuit Schematic Diagram

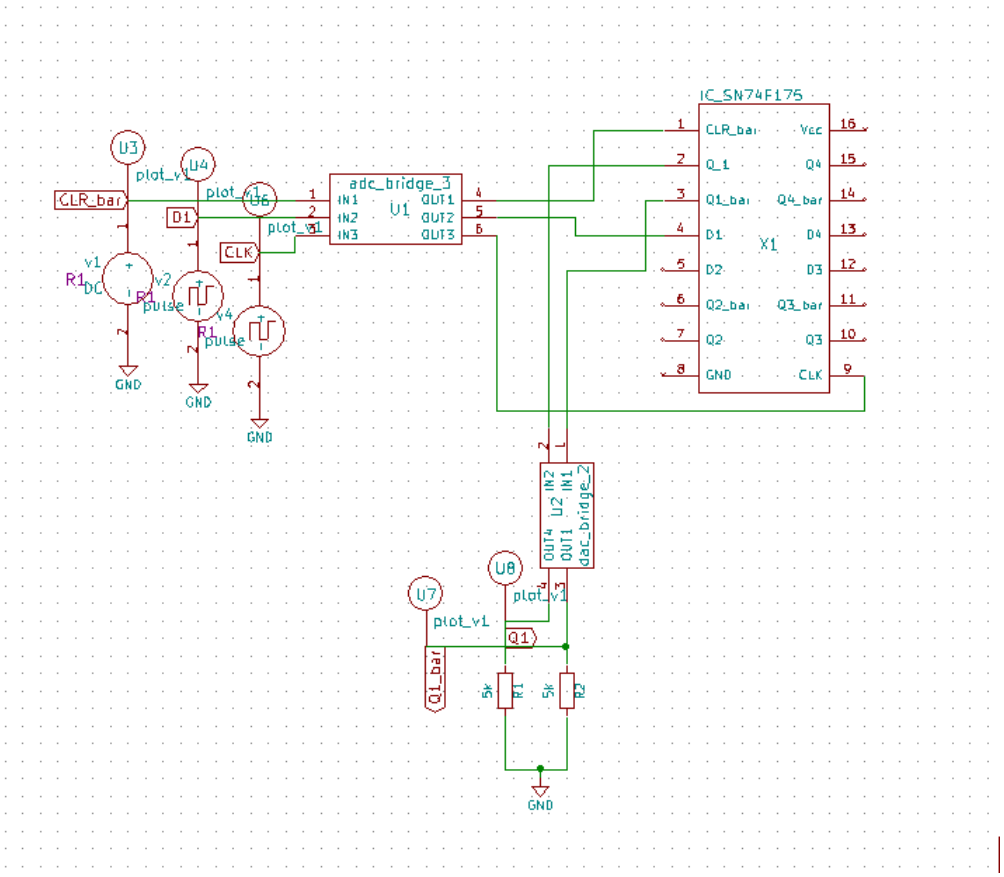



Figure 19.5: Test Circuit Schematic Diagram of SN74F175

## 19.7 Analysis details

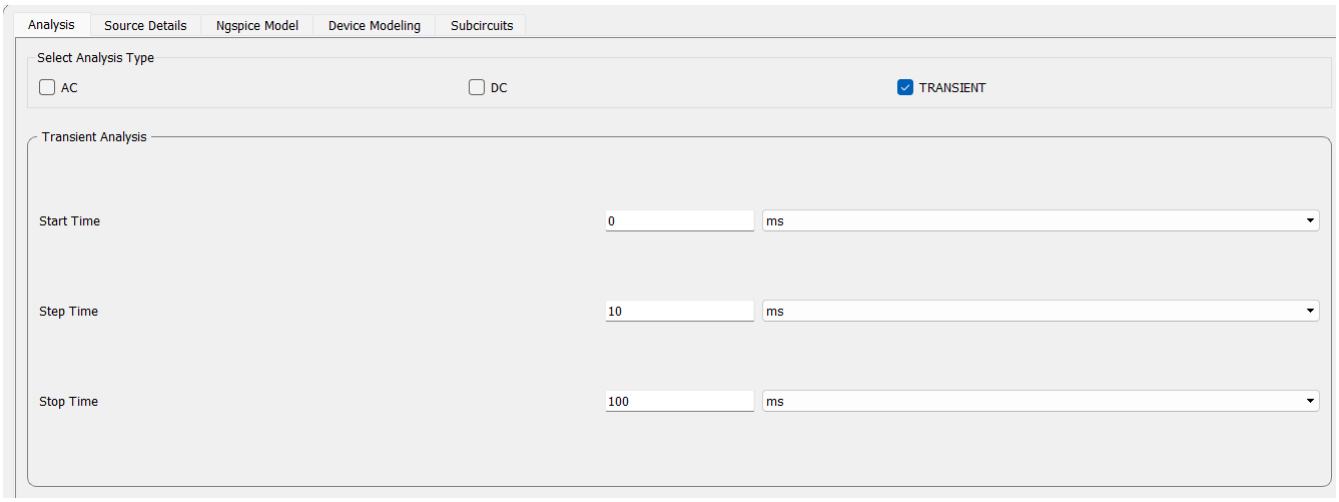



Figure 19.6: Analysis details of SN74F175

## 19.8 Source Details

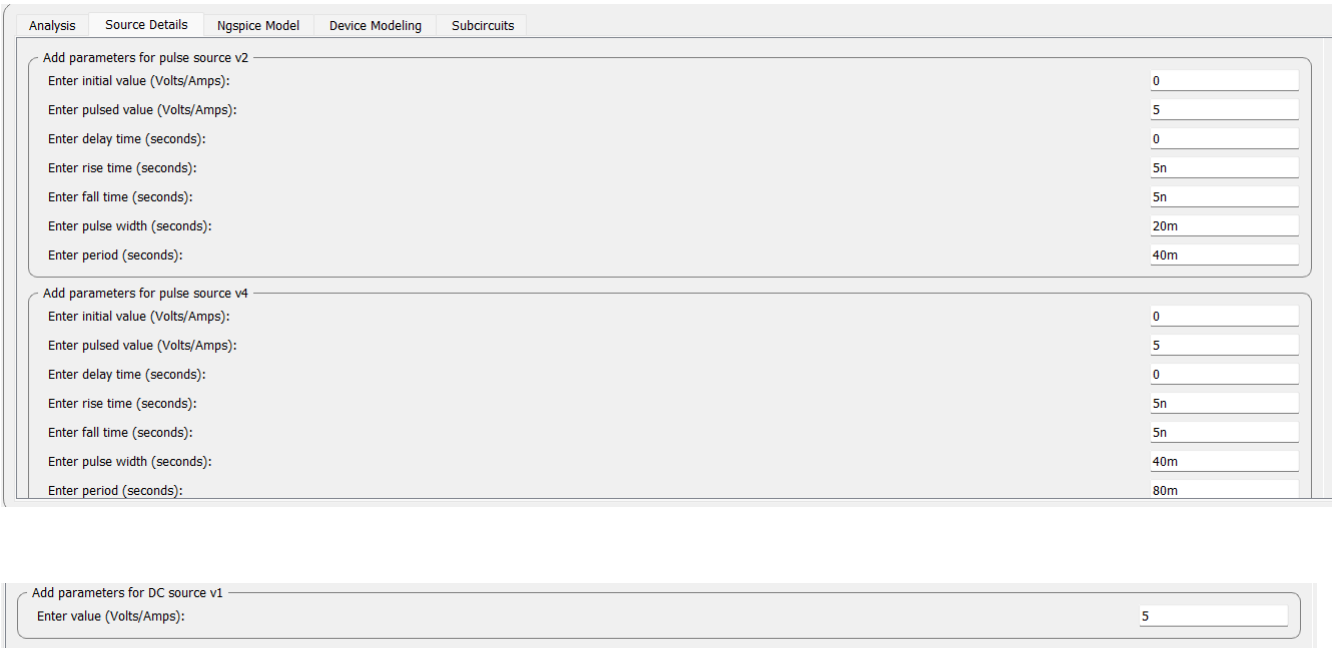



Figure 19.7: Source Details of SN74F175

## 19.9 Input Plots

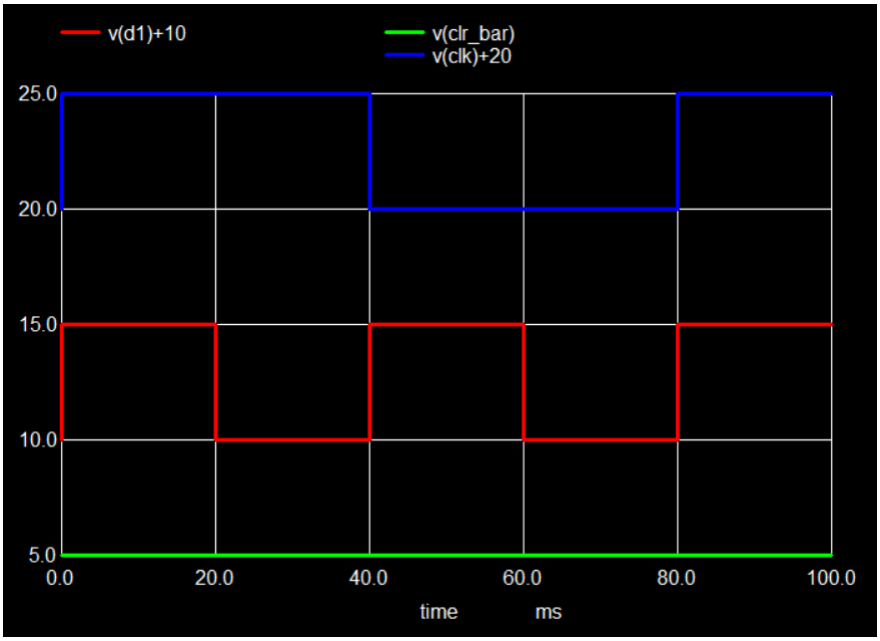



Figure 19.8: Input Plot of SN74F175

## 19.10 Output Plots

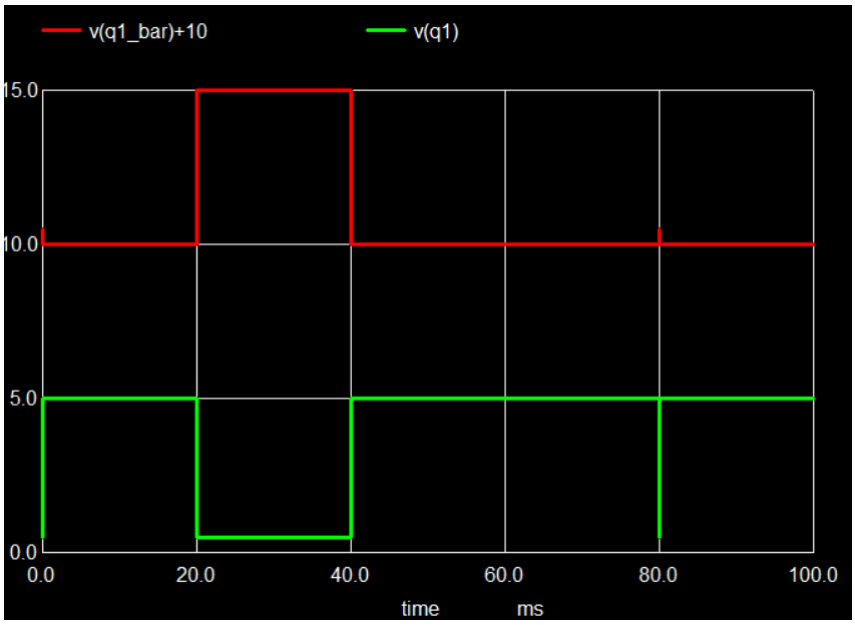



Figure 19.9: Output Plot of SN74F175

# Chapter 20

# Failed ICs

## 20.1 Failed IC 1: AD623

### 20.1.1 General Overview

**Instrumentation Amplifier**
The AD623 is a low-power, rail-to-rail instrumentation amplifier suitable for single- or dual-supply operation with a wide supply range of 2.7 V to 12 V. It features a low quiescent current of 550 A, an input voltage range extending 150 mV below ground, and a programmable gain from 1 to 1000 using a single external resistor (unity gain with no resistor). With high accuracy (0.10% gain error for $G = 1$), low noise (35 nV/$\sqrt{Hz}$ at 1 kHz), and high CMRR (up to 200 Hz), it enables precise amplification of small differential signals. Its fast dynamic response (800 kHz bandwidth at $G = 1$) makes it ideal for applications such as medical instrumentation, transducer interfaces, thermocouple amplifiers, and data acquisition systems.

### 20.1.2 Test Circuit Schematic

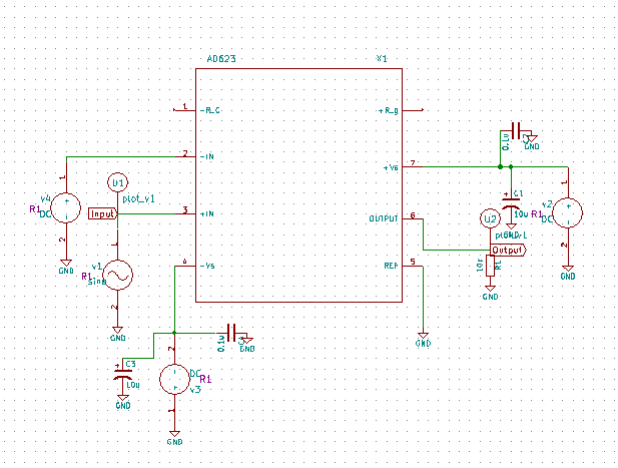



Figure 20.1: Test Circuit Schematic Diagram of AD623

### 20.1.3 Subcircuit Schematic

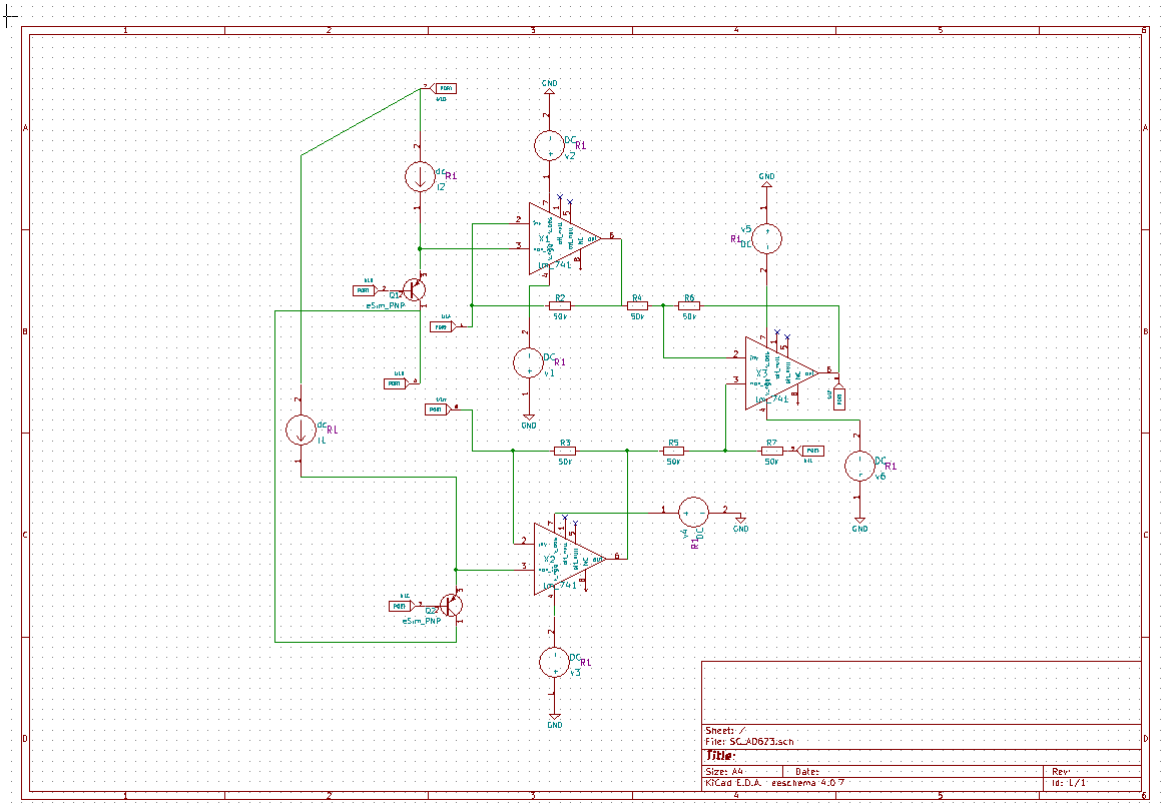



Figure 20.2: Subcircuit Schematic Diagram of AD623

### 20.1.4 Issues Faced

In the simulation of the AD623 instrumentation amplifier, an unexpected output behavior was observed despite a valid low-amplitude sinusoidal input signal. The output remained saturated at a constant negative voltage level (approximately -10.66 V) and failed to follow the input waveform. This suggests that the amplifier may have entered saturation and can be partially attributed to the use of the LM741 op-amp in the test circuit. The LM741 has limited input common-mode range and does not support rail-to-rail operation, making it unsuitable for accurately amplifying small differential signals or interfacing with low-voltage inputs as required by the AD623. This mismatch can lead to improper biasing and output saturation, as well as increased noise, as seen in the simulation results.

## 20.2 Failed IC 2: MC33171

### 20.2.1 General Overview

**Low Power Operational Amplifiers**

The MC33171 is a low-power, high-performance monolithic operational amplifier designed for both single and split supply operation, with an operating range from 3.0 V to 44 V. It features a low supply current of just 180 A per amplifier and offers a wide bandwidth of 1.8 MHz with a high slew rate of 2.1 V/s. The design includes a Darlington input stage, providing high input resistance, low offset voltage (2 mV), and excellent gain. Its all-NPN output stage ensures large output voltage swing, low distortion, and high drive capability for capacitive loads. With a common-mode input range that includes ground, built-in short-circuit protection, and ESD diodes for protection, the MC33171 is ideal for industrial, automotive, and low-power analog applications.

### 20.2.2 Subcircuit Schematic

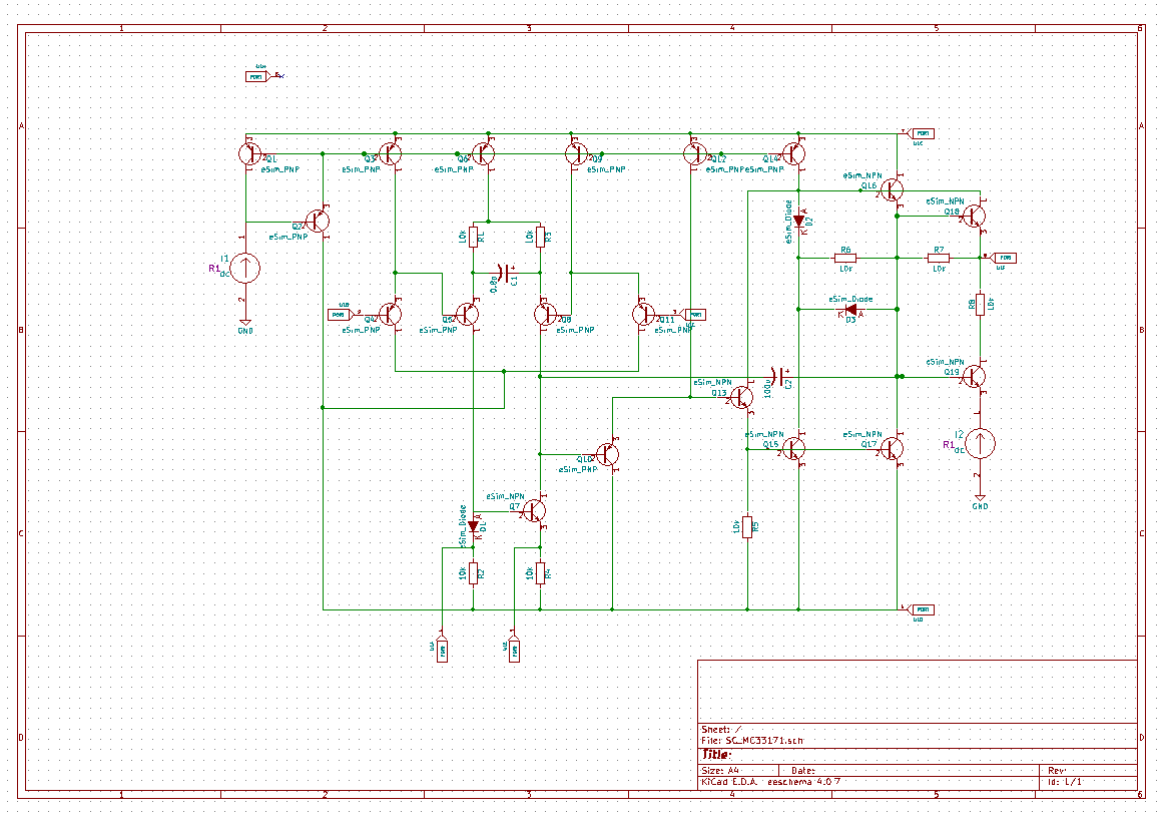



Figure 20.3: Subcircuit Schematic of MC33171

### 20.2.3 Test Circuit Schematic

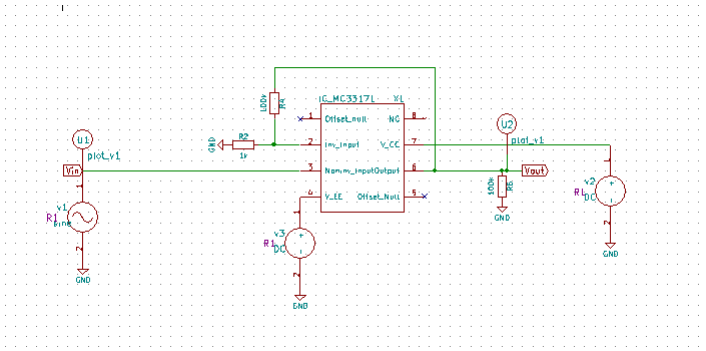



Figure 20.4: Test Circuit Schematic of MC33171

### 20.2.4 Issues Faced

In the simulation of the MC33171 operational amplifier, the output waveform failed to show the expected level of amplification in response to the sinusoidal input signal. The input swings between 10 mV, while the output remains centered around -4.12 V with only minimal variation, indicating a very low gain.

## 20.3 Failed IC 3: TLV1701

### 20.3.1 General Overview

**MicroPower Comparator**

The TLV1701 is a single-channel, general-purpose comparator from the TLV170x family, designed for low-power, high-precision applications. It features a wide supply voltage range, rail-to-rail input capability, low quiescent current, and fast propagation delay, making it suitable for a variety of analog comparison tasks. The open-collector output allows flexible interfacing by enabling the output to be pulled up to any voltage up to +36 V above the negative supply, independent of the devices own supply voltage. With low input offset voltage, minimal input bias current, and support for operation across a wide temperature range (40C to +125C), the TLV1701 is ideal for voltage monitoring, threshold detection, and relay-driving applications.

### 20.3.2 Subcircuit Schematic

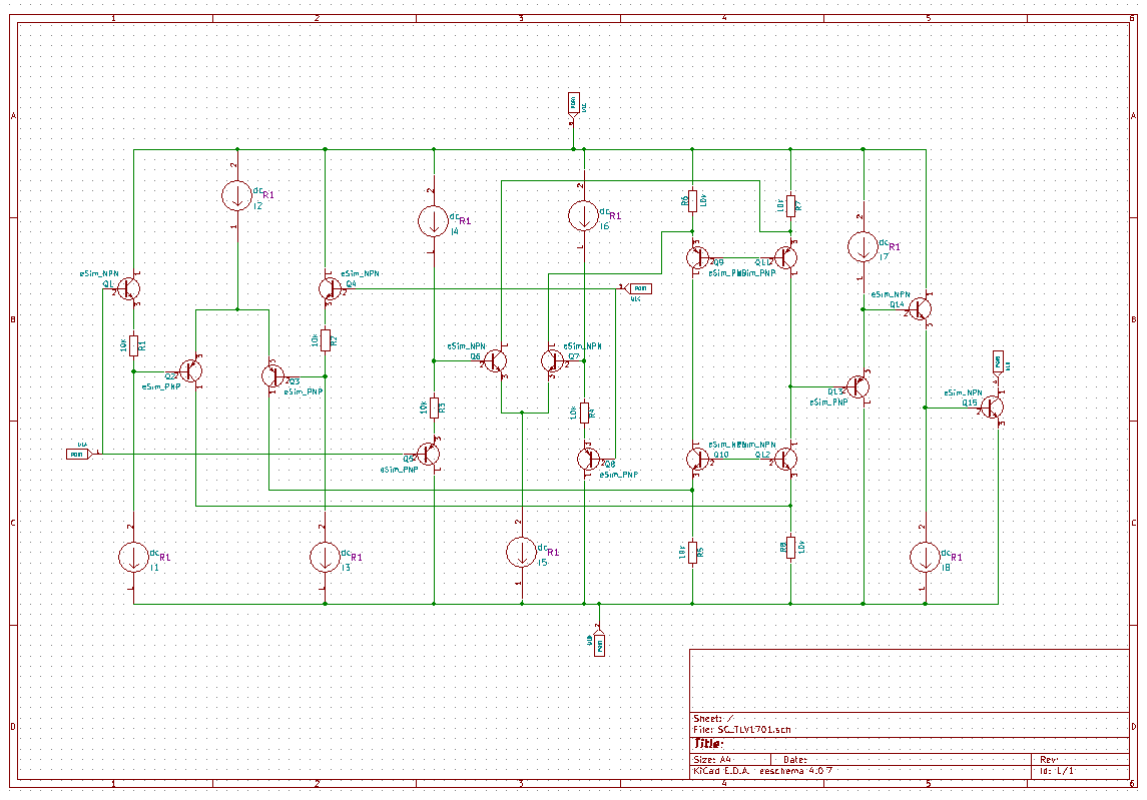


Figure 20.5: Subcircuit Schematic of TLV1701

### 20.3.3 Test Circuit Schematic

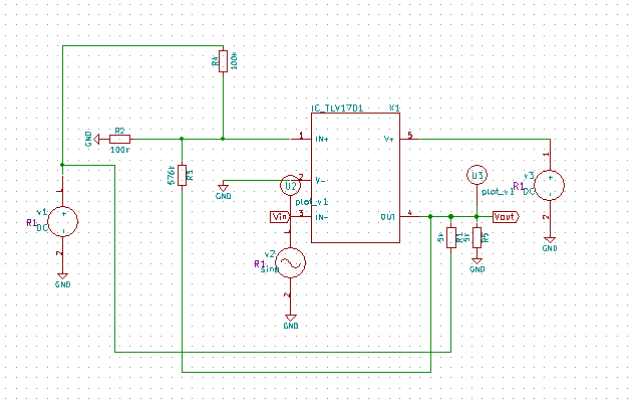


Figure 20.6: Test Circuit Schematic of TLV1701

### 20.3.4 Issues Faced

In the TLV1701 simulation, the output failed to exhibit proper comparator behavior in response to the sinusoidal input. Instead of switching states according to the input crossing the reference threshold, the output remained relatively constant at around 43 mV with only minor fluctuations.

## 20.4 Failed IC 4: SN7470

### 20.4.1 General Overview

**And-Gated J-K Positive-Edge-Triggered Flip-Flops With Preset And Clear**
The SN7470 is a monolithic, edge-triggered J-K flip-flop featuring gated inputs, direct clear and preset controls, and complementary Q and $\bar{Q}$ outputs. Data is transferred to the outputs on the positive edge of the clock pulse. It employs direct-coupled clock triggering, ensuring gated inputs are disabled once the clock input threshold is crossed. Optimized for medium- to high-speed applications, the SN7470 offers reduced power dissipation and lower package count in systems requiring input gating. It is characterized for reliable operation over a temperature range of 0C to 70C.

### 20.4.2 Subcircuit Schematic

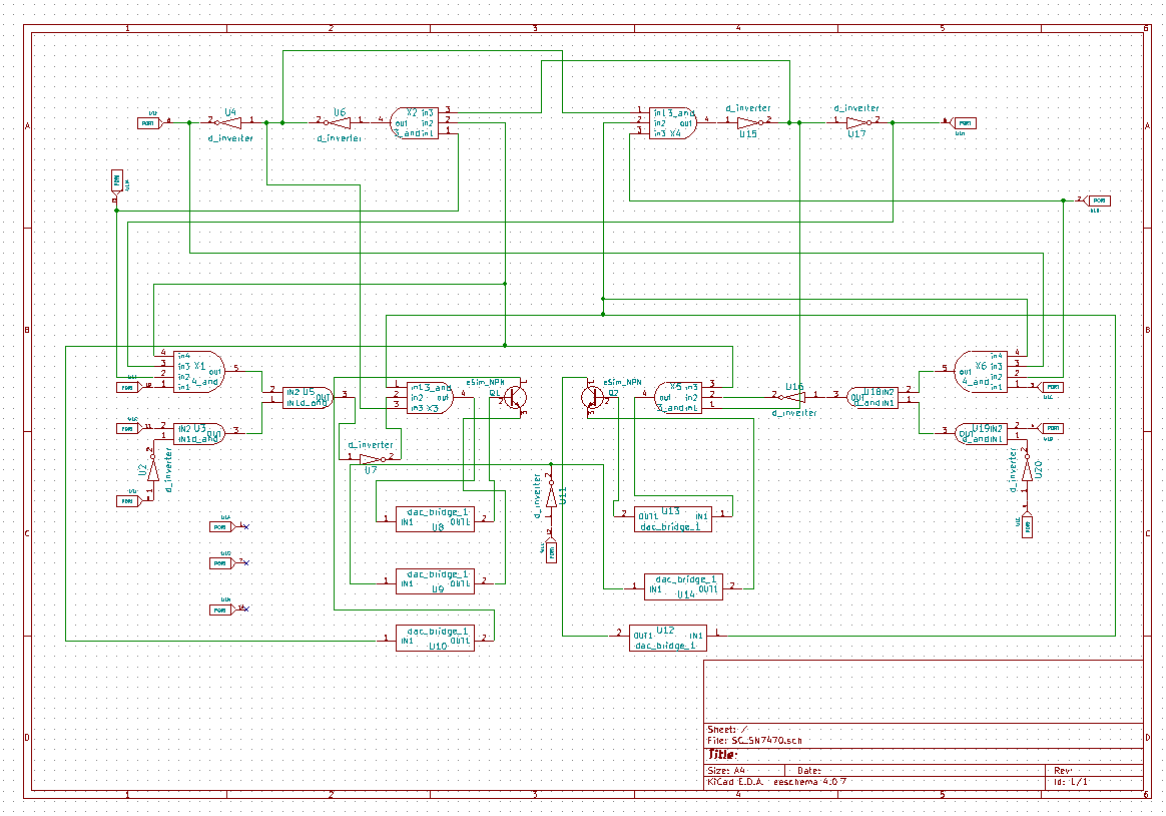



Figure 20.7: Subcircuit Schematic of SN7470

### 20.4.3 Test Circuit Schematic

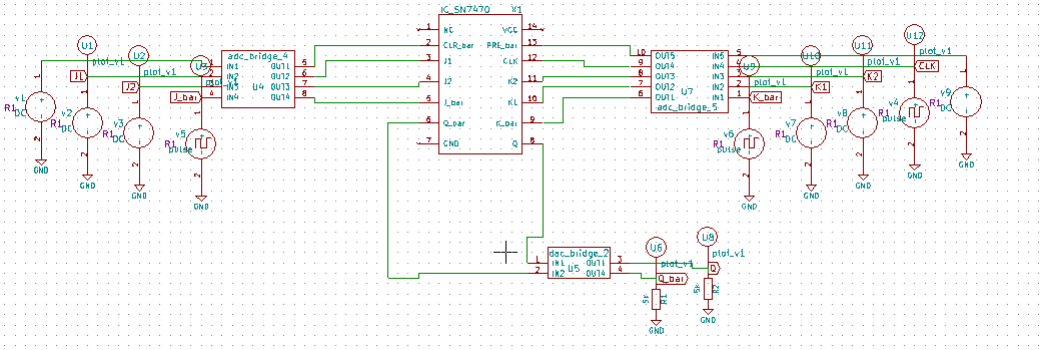



Figure 20.8: Test Circuit Schematic of SN7470

### 20.4.4 Issues Faced

The simulation for the SN7470 JK flip-flop failed to produce any output transitions at $Q$ or $\overline{Q}$, despite proper clocking and input signals. This issue likely stems from the improper mixing of NPN transistor-level analog models with digital gate components within the same subcircuit, leading to signal incompatibility or convergence errors during simulation.

# Chapter 21

# Conclusion and Future Scope

This project was undertaken as part of the FOSSEE Summer Fellowship 2025 under the eSim domain, with the primary objective of implementing and simulating a diverse range of analog and digital integrated circuits using the open-source EDA tool eSim. The workflow involved modeling each IC based on its official datasheet specifications, creating schematic representations, designing custom symbols, and developing corresponding test circuits for functional verification. Simulations were conducted using KiCad and Ngspice, ensuring that each IC model closely adhered to the expected logical and behavioral characteristics.

Through this endeavor, a comprehensive understanding of the internal operation of ICs, circuit-level design principles, and debugging techniques in open-source EDA environments was gained. The project culminated in the successful development of numerous subcircuits, including Operational Amplifiers, Comparators, Voltage Regulators, Logic Gates, Multiplexers, De-Multiplexers, Schmitt Triggers, Differential Amplifiers, and Instrumentation Amplifiers. These models have now been validated for accuracy and are ready for integration into the eSim subcircuit library, offering a valuable resource for students, educators, researchers, and developers alike.

Beyond its technical outcomes, the project significantly enhanced practical skills in schematic design, simulation-based validation, and structured documentation, all of which are critical in the domain of VLSI and circuit design. Moreover, it lays a strong foundation for the future expansion of eSims component library. As open-source EDA tools continue to gain traction, this work contributes meaningfully to the ecosystem, empowering the eSim community and supporting the broader goal of accessible, high-quality electronic design education and research.

# Chapter 22

# IC Contribution

This chapter documents the Integrated Circuits (ICs) contributed as part of the fellowship initiative. Each IC was systematically modeled, validated through simulation, and integrated into the eSim library. The contributions encompass a diverse set of analog and digital components, supporting a wide array of functionalities for academic and practical applications in electronic system design.

## 22.1 List of ICs by Annesha Dey

1. **SN74LS280**: 9-Bit Odd/Even Parity Generators/Checkers
2. **SN7480**: Gated Full Adder
3. **MC74HC595A**: 8-Bit Serial-Input/Serial or Parallel-Output Shift Register with Latched 3-State Outputs
4. **74HC4017**: Johnson Decade Counter with 10 Decoded Outputs
5. **CD4022B**: Octal Counter with 8 Decoded Outputs
6. **SN74F175**: Quadruple D-Type Flip-Flop With Clear
7. **SN74LS670**: 4-by-4 Register File With 3-State Outputs
8. **SL74HC154**: 1-of-16 Decoder/Demultiplexer
9. **74ACT11240**: Octal Buffer/Line Driver With 3-State Outputs
10. **M74HCT245**: Octal Bus Transceiver With 3-State Outputs (Non-Inverted)
11. **SN74LS51**: AND-OR-INVERT Gates
12. **SN74LS684**: 8-bit Magnitude/Identity Comparator
13. **74F382**: 4-Bit Arithmetic Logic Unit
14. **74LCX112**: Low Voltage Dual J-K Negative Edge-Triggered Flip-Flop with 5V Tolerant Inputs

15. **SN7451**: AND-OR-INVERT Gates
16. **SN7495A**: 4-Bit Parallel-Access Shift Register
17. **AD623**: Instrumentation Amplifier *(Failed Circuit)*
18. **MC33171**:Low Power Operational Amplifier *(Failed Circuit)*
19. **TLV1701**: microPower Comparator *(Failed Circuit)*
20. **SN7470**: And-Gated J-K Positive-Edge-Triggered Flip-Flops With Preset And Clear *(Failed Circuit)*

With these ICs, eSim moves a step closer to becoming a comprehensive platform for circuit design and education.

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