Summer Fellowship Report

On

Integrated Circuit Design using Subcircuit feature of eSim

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Acknowledgment

I take this opportunity to express my deepest gratitude to the entire FOSSEE team at IIT Bombay for providing me with this wonderful opportunity to work on the design and integration of sub-circuits using eSim and Device Modelling. The internship has given me valuable exposure to open-source tools, their real-world applications, and a deeper understanding of electronic design and simulation.

I am especially grateful to Prof. Kannan M. Moudgalya for his constant inspiration and vision behind the FOSSEE initiative. His commitment towards promoting open-source software for education and research has created numerous opportunities for students like me to gain hands-on experience and contribute to the open-source community. His farsighted leadership and encouragement have been truly motivating throughout this journey.

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I also sincerely appreciate the entire FOSSEE initiative for its efforts in empowering students and researchers by making tools freely accessible, thus removing the barriers imposed by costly commercial software. This mission not only fosters innovation but also strengthens the open-source ecosystem, allowing young learners to actively contribute and grow.

This internship has been a memorable and rewarding phase of my academic journey. The knowledge, skills, and experiences I have gained will undoubtedly serve as a strong foundation as I move forward in my career in the semiconductor and VLSI domain.

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Chapter 1

Introduction

The advancement of Electronic Design Automation (EDA) tools has revolutionized the way electronic circuits are designed, simulated, and verified. Among these, open-source tools play a crucial role in making advanced EDA capabilities accessible to students, educators, and researchers without the burden of expensive licenses. The FOSSEE project at IIT Bombay has taken significant steps to promote such open-source tools globally.

One of the key open-source tools developed and promoted under FOSSEE is **eSim**, which integrates multiple open-source EDA tools to provide a unified platform for circuit design, simulation, and PCB layout. Various tools like NgSpice, Makerchip, and KiCad work together under eSim to offer a complete design environment.

1.1 eSim

eSim is an open-source Electronic Design Automation (EDA) tool developed by FOSSEE, IIT Bombay. The primary objective of eSim is to provide a completely free and open-source alternative to commercial circuit design and simulation software, thereby reducing dependency on expensive proprietary tools in academia and research.

eSim integrates multiple open-source tools to provide a comprehensive design and simulation environment. **KiCad** is used for schematic capture and PCB design, while **NgSpice** performs analog circuit simulation. For digital simulation, **GHDL** is integrated, supporting VHDL based designs, and **Makerchip** enables online Transaction Level Verilog (TL-Verilog) based digital design and verification. Python support is also available in eSim, allowing users to perform customized simulations, generate netlists.

One of the key features of eSim is its **Subcircuit feature**, which allows complex designs to be modularized into reusable blocks, simplifying the design of large systems. Additionally, eSim supports device modeling, enabling users to define and simulate custom semiconductor devices using real-world parameters. As part of its continuous development, eSim also supports **SkyWater SKY130 PDK**, allowing users to perform simulations using an open-source 130nm Process Design Kit, which is widely used for analog, mixed-signal, and digital IC design research.

By supporting a fully open-source toolchain, eSim empowers students, educators, and researchers to gain hands-on experience with industry-relevant EDA tools and contribute actively to the open-source hardware ecosystem.

1.1.1 NgSpice

NgSpice is an open-source circuit simulator integrated into eSim for performing analog and mixed-signal simulations. Based on the SPICE simulation engine, NgSpice supports DC, AC, transient, and parametric analyses, making it suitable for analyzing a wide range of circuits.

It allows users to simulate circuit behavior using industry-standard SPICE models, including support for subcircuits and behavioral modeling. In eSim, NgSpice works as the backend simulator for schematics created using KiCad, providing waveform outputs for voltage, current, and frequency responses. Its flexibility and accuracy make it a powerful tool for verifying designs before hardware implementation.

1.1.2 Makerchip

Makerchip is an integrated platform designed to simplify digital circuit design by offering both browser-based and desktop-based environments for coding, simulating, and debugging digital hardware designs. It supports multiple hardware description languages including Verilog, SystemVerilog, and Transaction-Level Verilog (TL-Verilog), allowing flexibility for users at various levels of expertise.

In eSim, Makerchip is interfaced through a Python-based application called Makerchip-App, which seamlessly launches the Makerchip IDE for digital design and verification. The platform integrates several open-source and proprietary tools to provide a rich set of features such as real-time simulation, waveform viewing, and code linting, thereby improving design accuracy and productivity.

1.1.3 KiCad

KiCad is an open-source PCB design and schematic capture tool integrated within eSim for creating circuit schematics and generating PCB layouts. It allows users to design multi-layer boards, define custom footprints, and perform design rule checks to ensure design correctness before fabrication.

In eSim, KiCad acts as the primary schematic editor, allowing users to graphically build circuits by placing and interconnecting components from extensive open-source libraries. The designed schematics can directly be used for both simulation and PCB layout generation. KiCad also supports features such as 3D visualization of PCBs, Gerber file export for manufacturing, and electrical rule checking to identify design issues early. Its seamless integration within eSim enables a smooth transition from schematic design to simulation and physical realization, offering a complete design-to-fabrication workflow entirely within an open-source environment.

1.1.4 GHDL

GHDL is an open-source simulator for VHDL, a hardware description language widely used in digital circuit design. It supports the complete IEEE VHDL standard, allowing designers to simulate, verify, and debug VHDL-based digital systems effectively.

In eSim, GHDL is integrated to enable digital simulation alongside analog simulation provided by NgSpice. Users can model digital circuits using VHDL, which are then simulated using GHDL to verify logical functionality and timing behavior. This integration allows eSim to handle mixed-signal designs, where the analog components are simulated by NgSpice and the digital components by GHDL, providing a comprehensive platform for complex system design. The combination of these tools allows designers to validate both analog and digital subsystems within a unified simulation environment.

Chapter 2

Features of eSim

eSim offers a comprehensive set of features that make it a powerful open-source alternative for electronic design automation. Some of the key features include:

- **Open-source and Free**: eSim is fully open-source, allowing unrestricted access without licensing costs, making it ideal for academic and research purposes.
- **Integrated Toolchain**: Combines multiple open-source tools such as KiCad for schematic capture and PCB design, NgSpice for analog simulation, GHDL for digital simulation, and Makerchip for advanced digital design.
- **Mixed-Signal Simulation**: Supports both analog and digital simulation, allowing users to design and simulate mixed-signal circuits efficiently.
- **Subcircuit Feature**: Enables hierarchical and modular design by allowing complex circuits to be broken into reusable subcircuits.
- **Device Modeling**: Supports custom device modeling, allowing users to simulate real-world semiconductor devices using user-defined parameters.
- **SkyWater SKY130 PDK Support**: Provides access to open-source 130nm process design kit for IC design and simulation.
- **Python Integration**: Allows automation, scripting, and advanced analysis using Python interfaces.
- **User-Friendly Interface**: Offers an intuitive GUI that simplifies circuit creation, simulation setup, and result analysis, making it suitable for both beginners and advanced users.
- **Cross-Platform Support**: Compatible with major operating systems like Linux and Windows.
- **Active Community and Documentation**: Extensive documentation, tutorials, and community support provided through FOSSEE ensure smooth learning and troubleshooting.

Chapter 3

Problem Statement

To design,develop and test various Analog and Digital Integrated Circuit Models using the sub-circuit feature in eSim and create Device Models using the Model Editor tool.These subcircuits are to be built using the device models already present in the eSim library. After successful testing of these IC models and their integration into the eSim subcircuit library, these models would be useful in the future for circuit designing purposes.

3.1 Subcircuit Design and Integration

Digital ICs are modeled as subcircuits based on datasheet specifications and integrated into eSim's subcircuit library.

3.1.1 Approach

- **Datasheet Analysis**: The primary step is to browse through various analog and digital IC datasheets, and hence find suitable circuits to implement in eSim, that are not previously included into the eSim library. Check for the detailed schematic of the IC's and once the component values and the truth table is ascertained, then finalise the IC to be created.
- **Subcircuit Creation**: After deciding the IC, we start modeling it as a subcircuit in eSim, using the model files present in the eSim device model library only. The design is strictly according to the information given in the official data-sheets of the ICs.This step also includes building the Symbol/Pin diagram of the IC according to the packaging and pin description given in the data-sheets only
- **Symbol Creation**: Custom IC symbols are created according to package type and pin configuration for correct circuit integration.
- **Test Circuit Design**: Once the component of the IC is ready, now we can build the test circuits, according to the data-sheets. In this step we build the test cases and test circuits using the component IC
- **Simulation and Validation**: Once the test circuits are ready, now it's time to simulate the test circuits so that the output can be obtained in the form

of wave-forms and plots. Here we take help of KiCad to NgSpice conversion and Simulation feature in eSim If the output of the test circuit is not as per expectation, this implies that the test case has failed, and there is some error in the schematic. In such cases we go back to the design phase of the IC or the test circuits, to look for possible errors and then repeat the testing process again after making required changes. Once the expected output of the test cases are correct and satisfy the expected results, then in such a case the IC is declared successfully working. The test case has been verified and the designing process is complete.

Chapter 4

Digital IC's

The Subcircuit feature of eSim allows hierarchical modeling of complex Integrated Circuits by combining multiple basic components into a single reusable block. By utilizing datasheets and internal schematics of various ICs, accurate subcircuit models are created using eSim's schematic editor.

4.1 CD4511B - CMOS BCD -to-7-Segment Latch Decoder Drivers

Description: CD45118 types are BCD-to-7-segment atch decoder drivers constructed with CMOS logic and n-p-n bipolar transistor out-Dut devices on a single monolithic structure. These devices combine the low quiescent power dissipation and high noise immunity eatures of RCA CMOS with n-p-n bipolar Output transistors capable of sourcing up to 25 mA. This capability allows the CD4511B types to drive LED's and other displays directly.

Lamp Test (LT), Blanking (BL), and Latch Enable or Strobe inputs are provided to test the display, shut off or intensity-modulate it, and store or strobe a BCD code, respectively. Several different signals may be multiplexed and displayed when external multiplexing circuitry is used. The CD4511B types are supplied in 16-lead hermetic dual-in-line ceramic packages (F3A suffix), 16-lead dual-in-line plastic packages (E suffix), 16-lead small-outline packages (NSR suffix), and 16-lead thin shrink small-outline packages (PW and PWR suffixes).

4.1.1 IC Layout

This figure represents the Pin Package Diagram of CD4511B ic

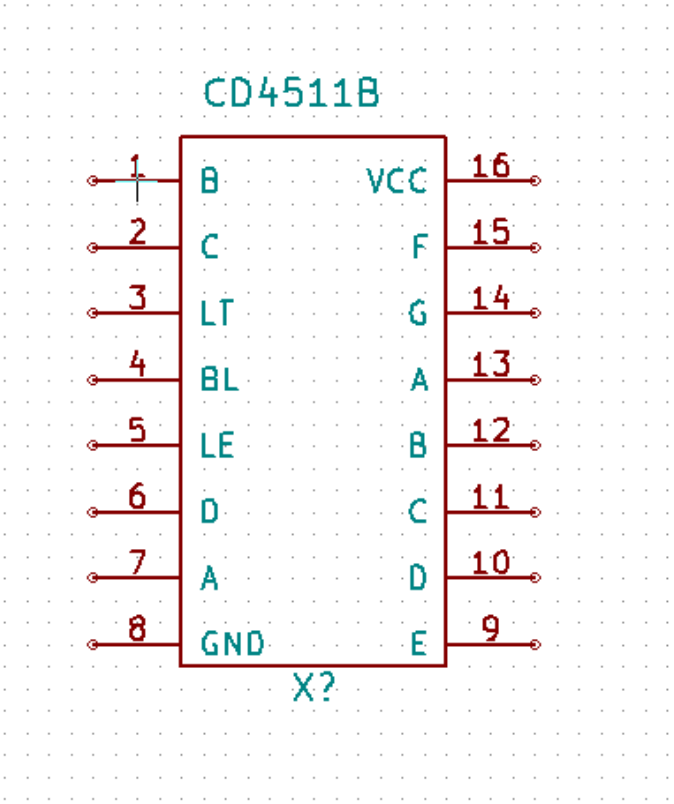

Figure 4.1: Pin diagram of CD4511B

4.1.2 Subcircuit Schematic Diagram CD4511B

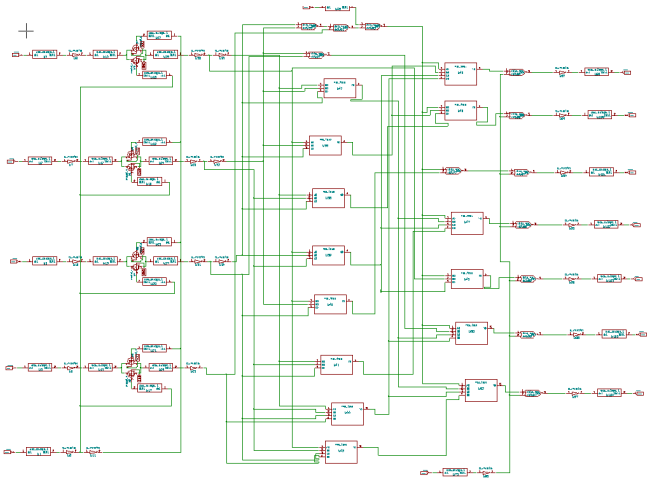

Figure 4.2: Subcircuit Schematic Diagram of CD4511B

4.1.3 Test Circuit

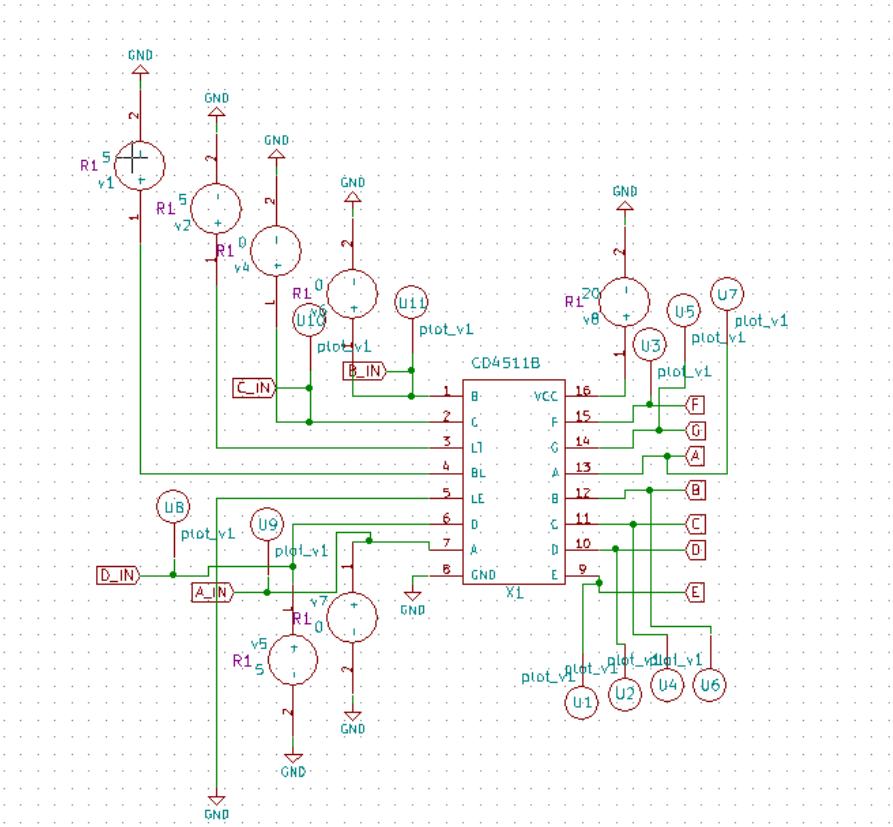

Figure 4.3: Test Circuit of CD4511B

4.1.4 Input Plots

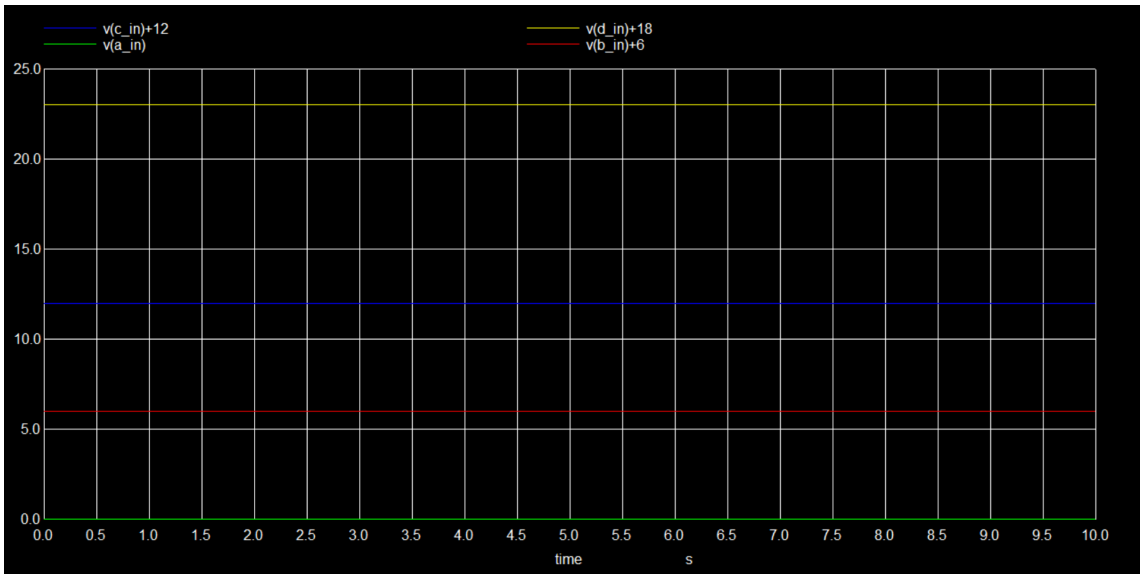

Figure 4.4: Input Plots Waveform of CD4511B

4.1.5 Output Plots

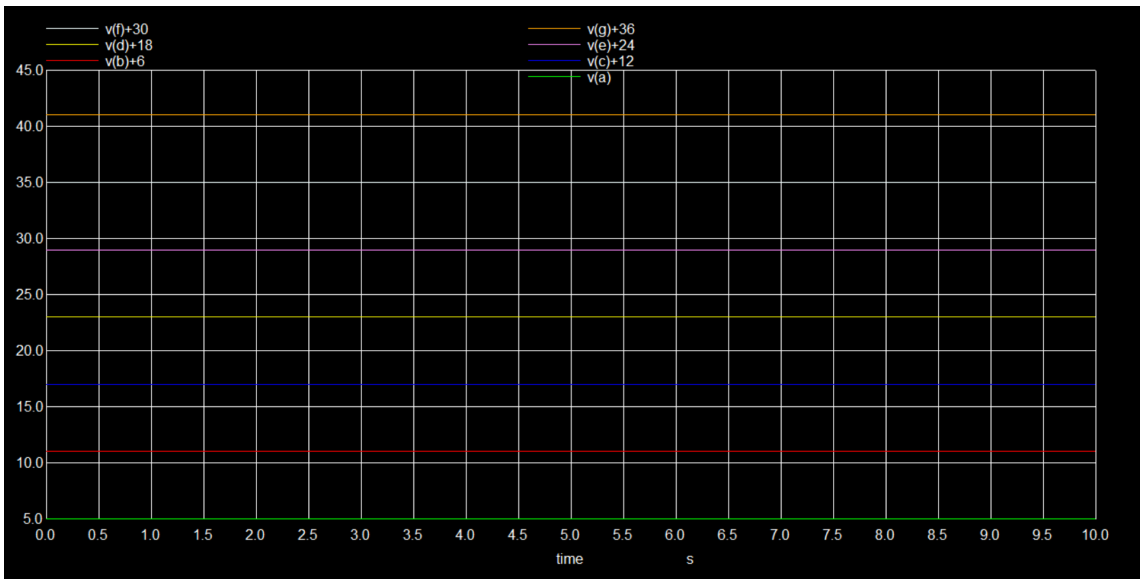

Figure 4.5: Output Voltage Waveform of CD4511B

4.2 CD4515B - CMOS 4-Bit Latch/4-to-16 Line Decoders

Description: CD4514B and CD4515B consist of a 4-bit strobed latch and a 4-to-16-line decoder. The latches hold the last input data presented prior to the strobe transition from 1 to 0. Inhibit control allows all outputs to be placed at 0(CD4514B) or 1 (CD45158) regardless of the state of the data or strobe inputs. The decode truth table indicates all combinations of data inputs and appropriate selected outputs.

4.2.1 IC Layout

This figure represents the Pin Package Diagram of CD4515B ic

Figure 4.6: Pin diagram of CD4515B

4.2.2 Subcircuit Schematic Diagram CD4515B

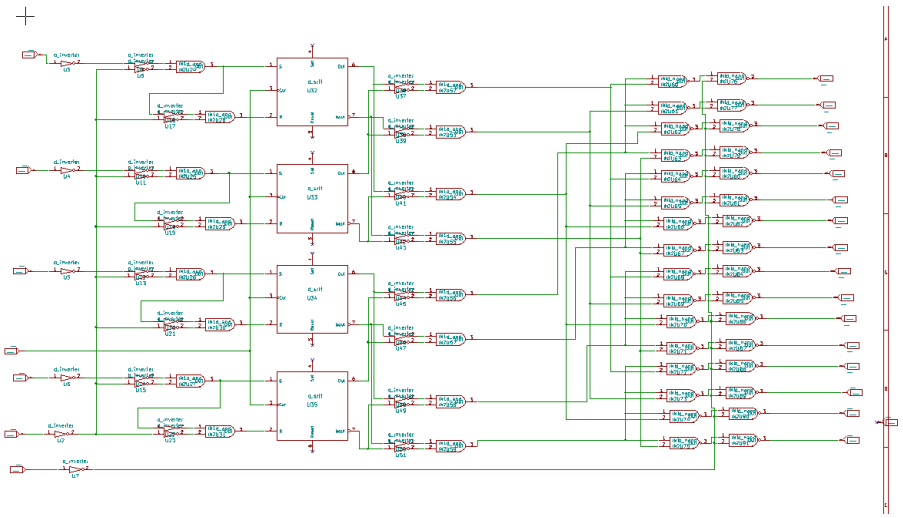

Figure 4.7: Subcircuit Schematic Diagram of CD4515B

4.2.3 Test Circuit

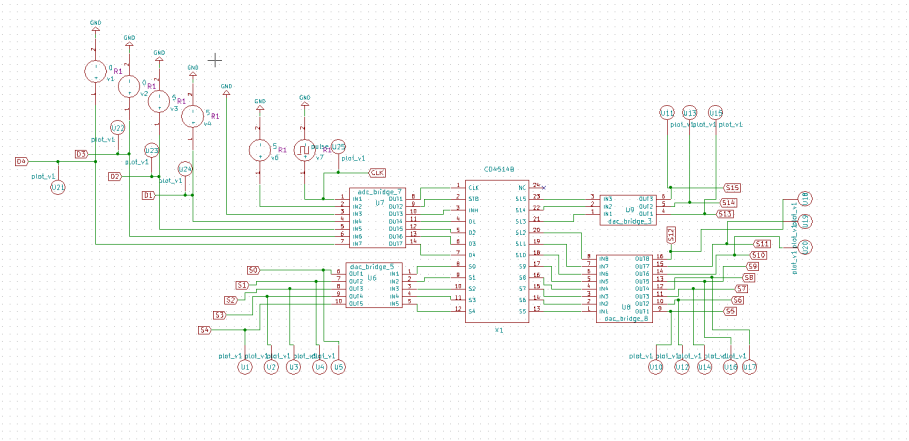

Figure 4.8: Test Circuit of CD4515B

4.2.4 Input Plots

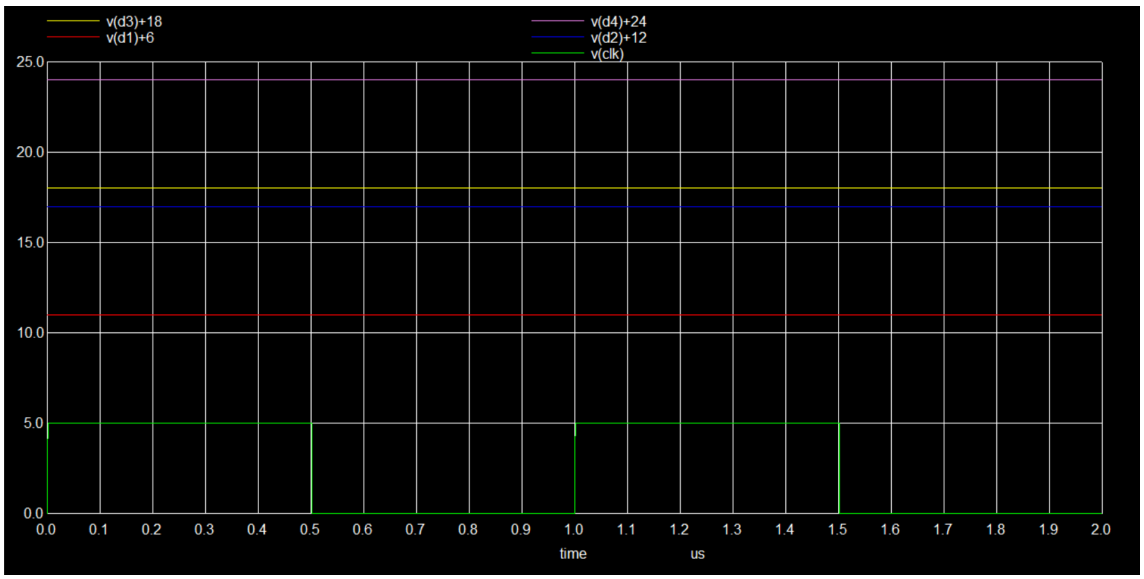

Figure 4.9: Input Plots Waveform of CD4515B

4.2.5 Output Plots

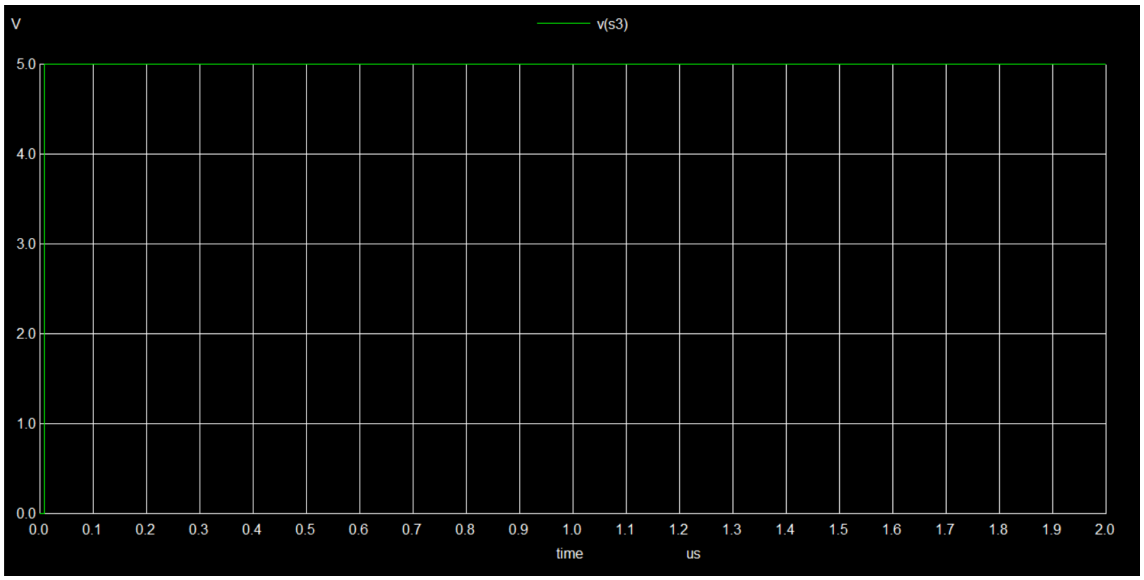

Figure 4.10: Output Voltage Waveform of CD4515B

4.3 CD4095 - CMOS Gated J-K Master-Slave Flip-Flops

Description: CD4095BMS and CD4096BMS are J-K Master-Slave Flip Flops featuring separate AND gating of multiple J and K inputs. The gated J-K inputs control transfer of information into the master section during clocked operation. Information on the J-K inputs is transferred to the Q andQ outputs on the positive edge of the clock pulse. SET and RESET inputs (active high) are provided for asynchronous operation.

4.3.1 IC Layout

This figure represents the Pin Package Diagram of CD4095B ic

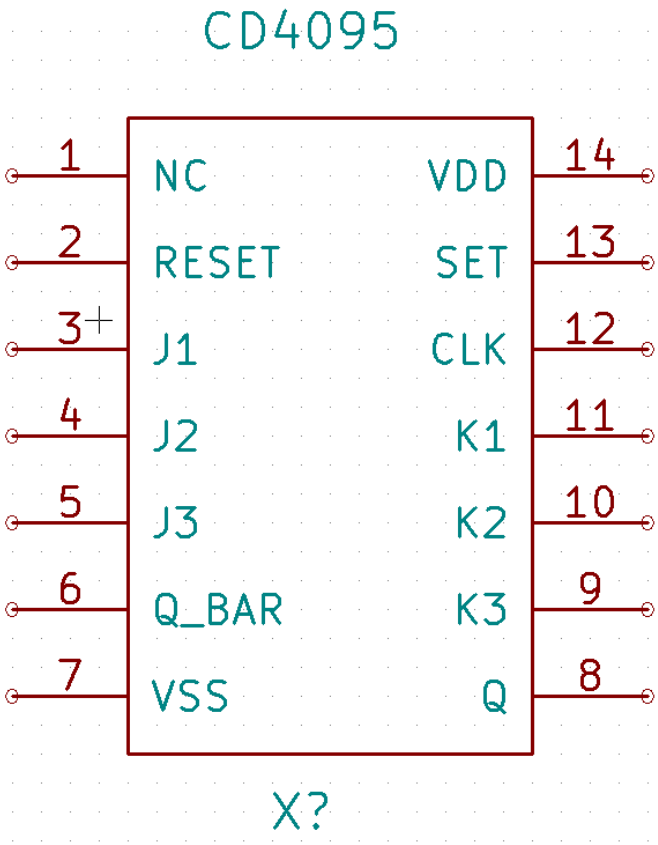

Figure 4.11: Pin diagram of CD4095B

4.3.2 Pin Diagram Schematic Diagram CD4095B

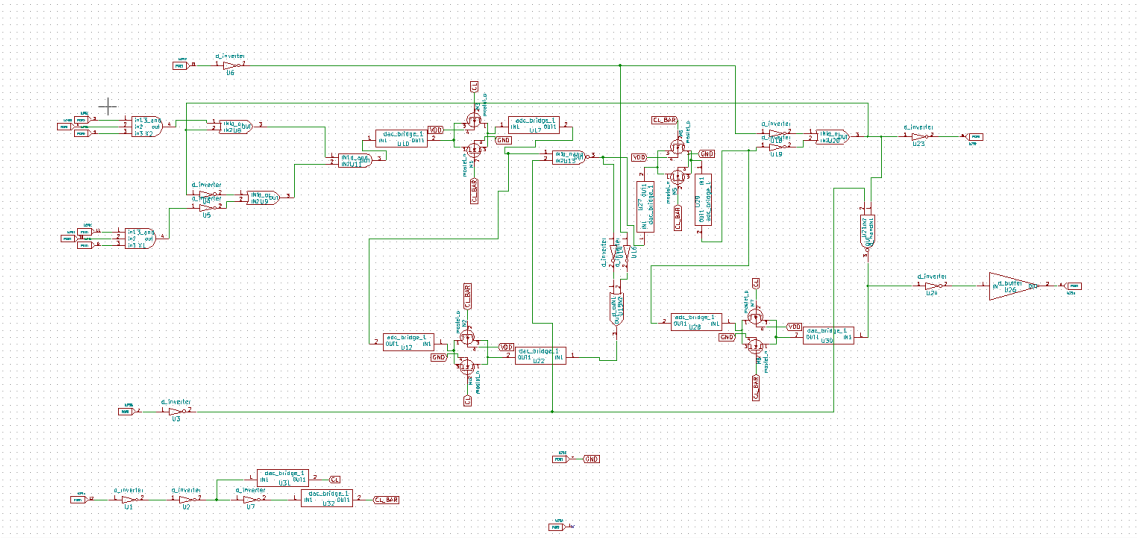

Figure 4.12: Subcircuit Schematic Diagram of CD4095B

4.3.3 Test Circuit

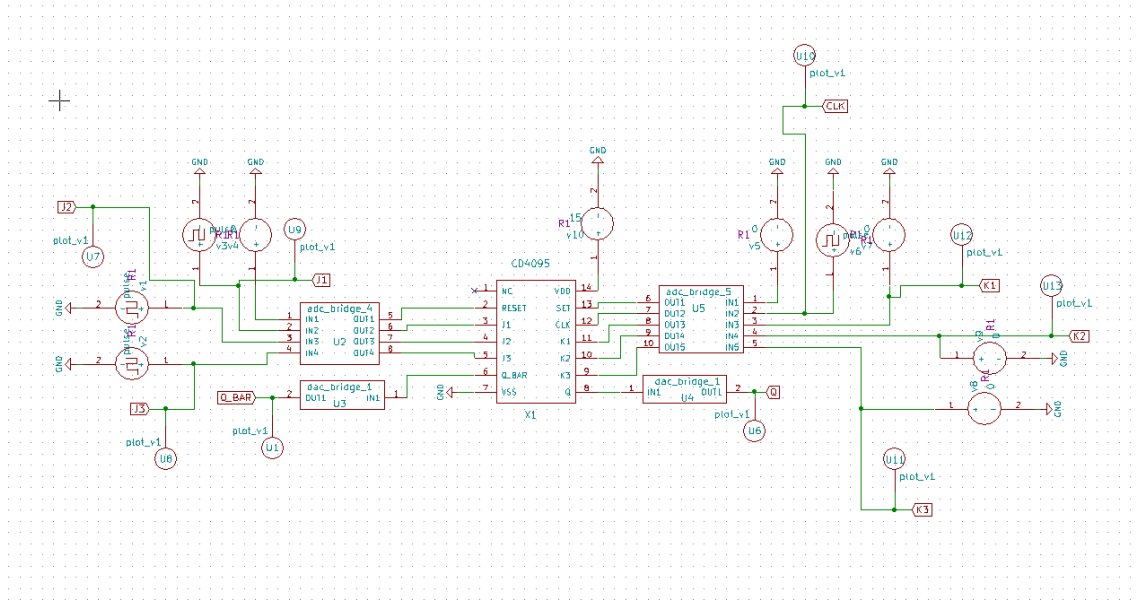

Figure 4.13: Test Circuit of CD4095B

4.3.4 Input Plots

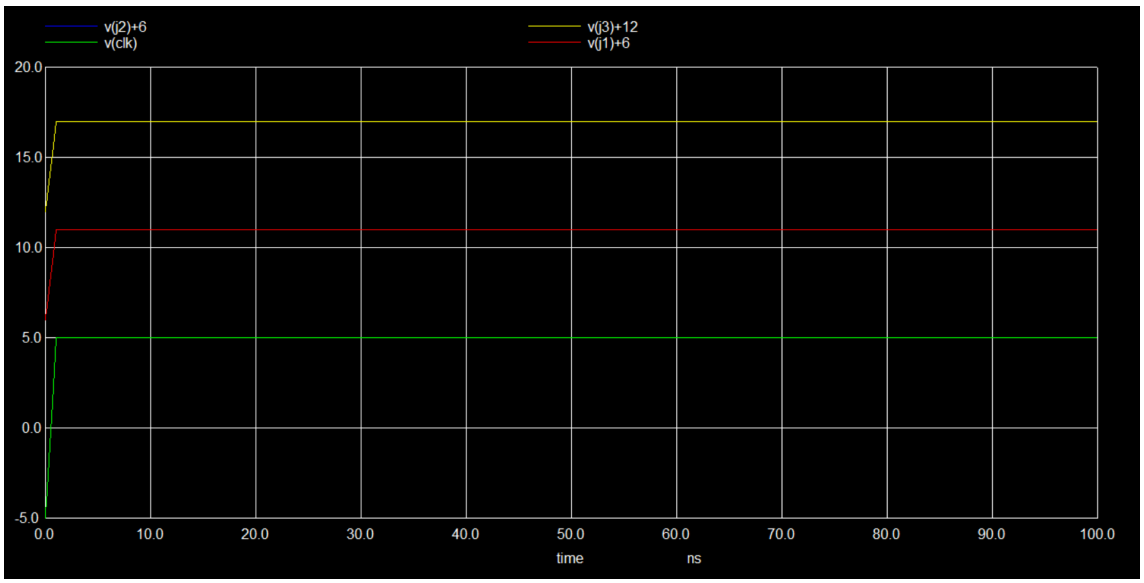

Figure 4.14: Input Plots Waveform of CD4095B

4.3.5 Output Plots

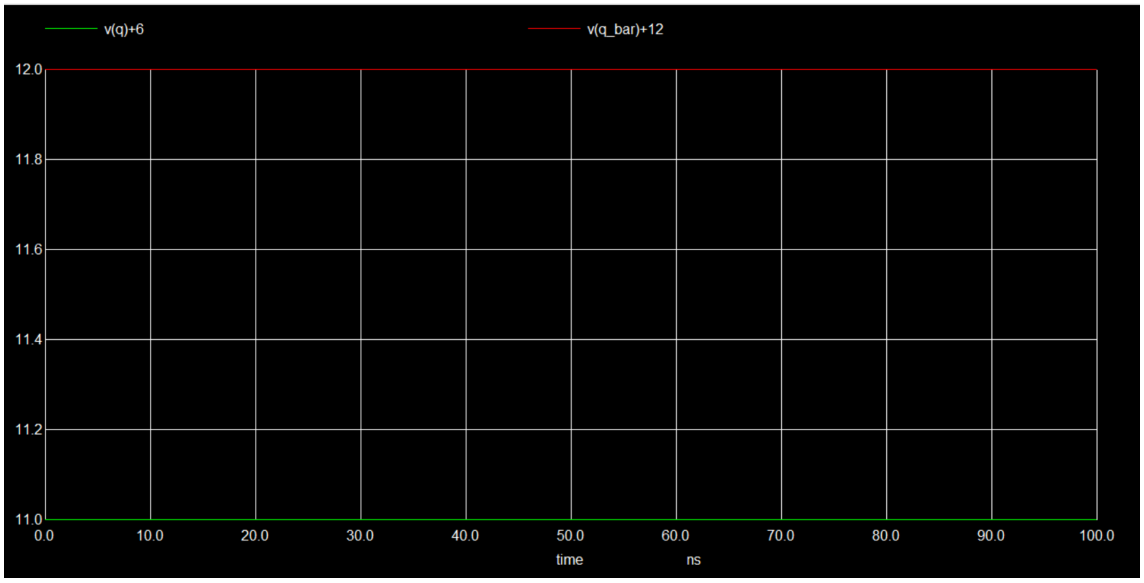

Figure 4.15: Output Voltage Waveform of CD4095B

4.4 SN74LS298 - QUAD 2-INPUT MULTIPLEXER WITH STORAGE

Description: The SN54/74LS298 is a Quad 2-Port Register. It is the logical equivalent of a quad 2-input multiplexer followed by a quad 4-bit edge-triggered register. A Common Select input selects between two 4-bit input ports (data sources.) The selected data is transferred to the output register synchronous with the HIGH to LOW transition of the Clock input.

4.4.1 IC Layout

This figure represents the Pin Package Diagram of SN74LS298 ic

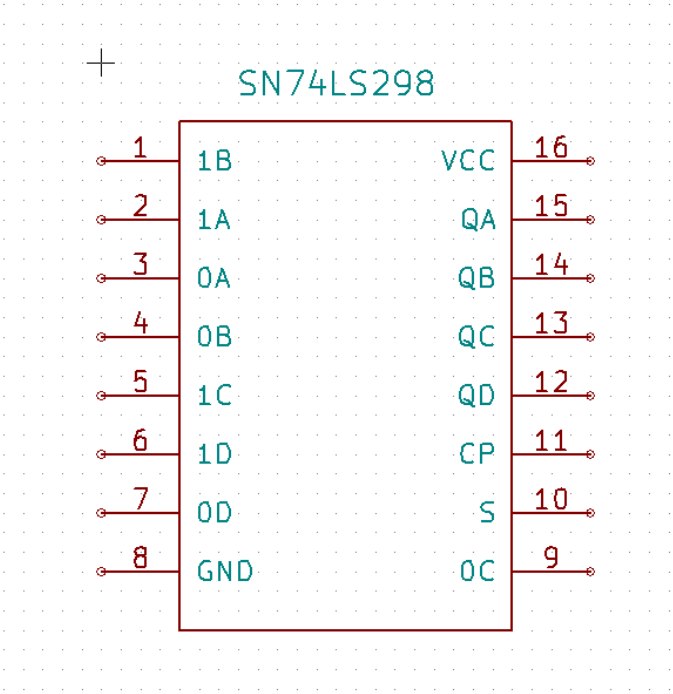

Figure 4.16: Pin diagram of SN74LS298

4.4.2 Subcircuit Schematic Diagram SN74LS298

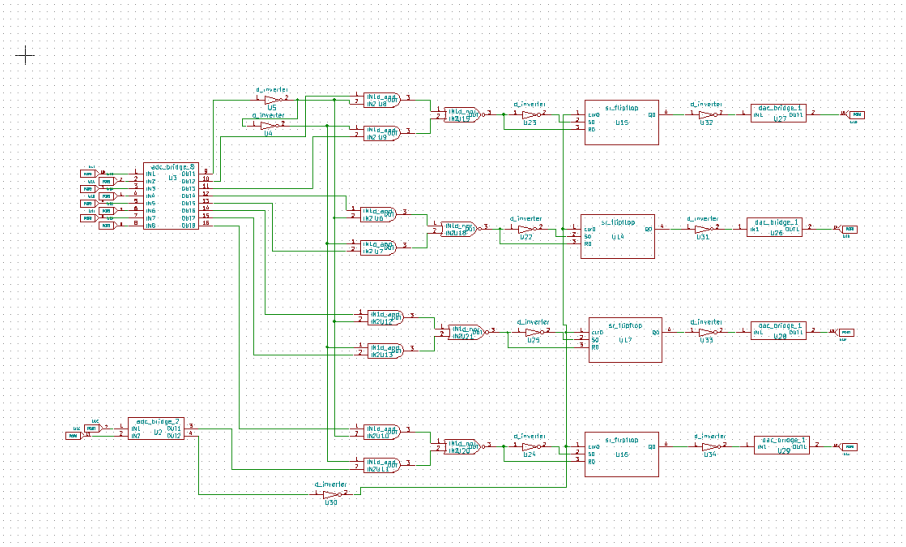

Figure 4.17: Subcircuit Schematic Diagram of SN74LS298

4.4.3 Test Circuit

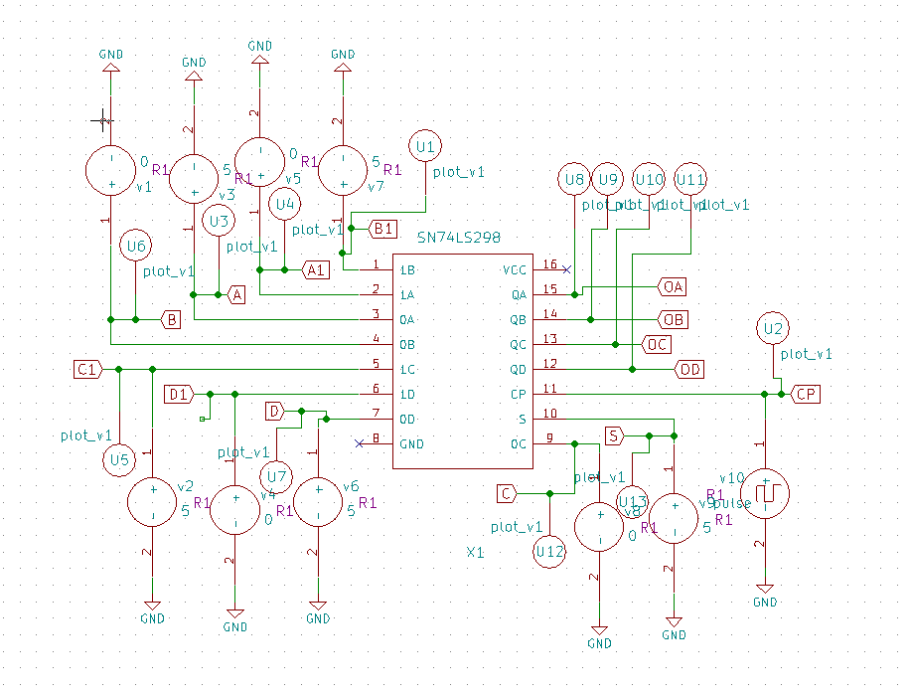

Figure 4.18: Test Circuit of SN74LS298

4.4.4 Input Plots

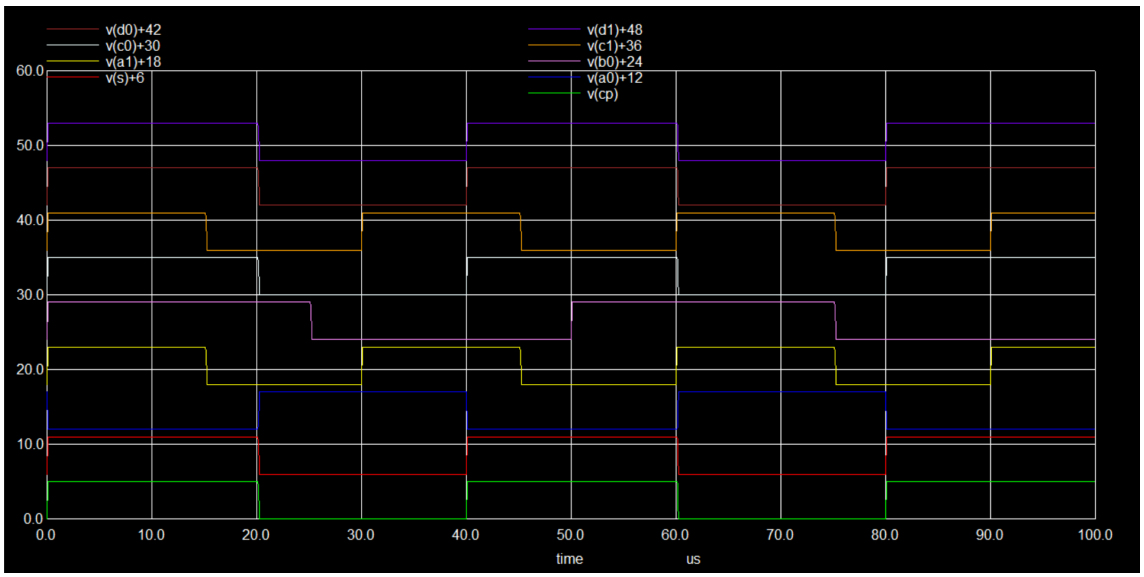

Figure 4.19: Input Plots Waveform of SN74LS298

4.4.5 Output Plots

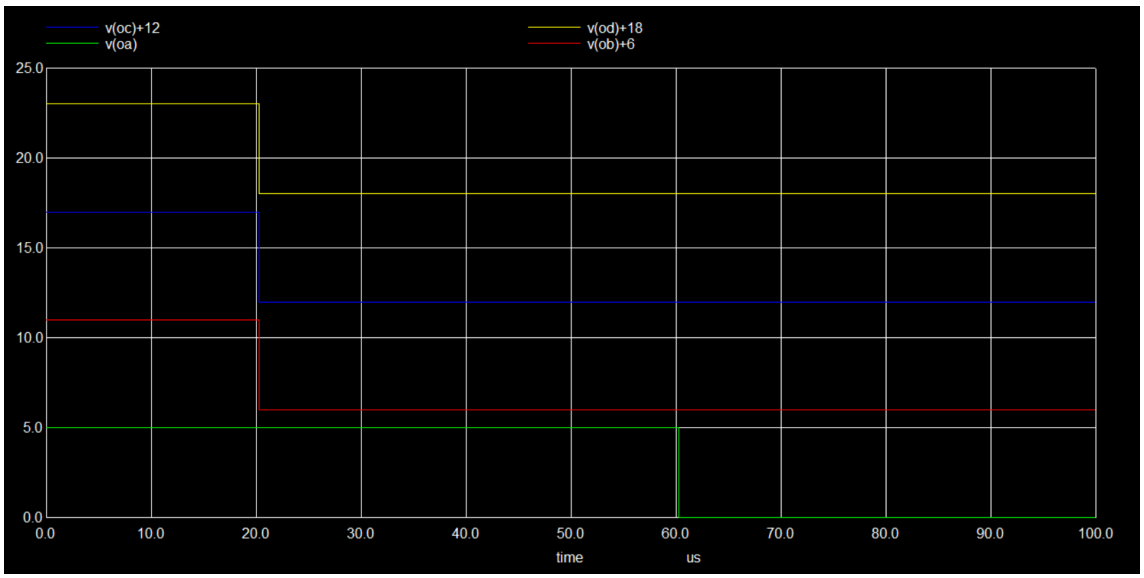

Figure 4.20: Output Voltage Waveform of SN74LS298

4.5 CD54HC374 -Octal D-Flip flop Positive-Edge Triggered

Description: The 'HC374, 'HCT374, 'HC574, and 'HCT574 are octal D-type flip-flops with 3-state outputs and the capability to drive 15 LSTTL loads. The eight edge triggered flip-flops enter data into their registers on the LOW to HIGH transition of clock (CP). The output enable (OE) controls the 3-state outputs and is independent of the register operation. When OE is HIGH, the outputs are in the high-impedance state. The 374 and 574 are identical in function and differ only in their pinout arrangements.

4.5.1 IC Layout

This figure represents the Pin Package Diagram of CD54HC374 ic

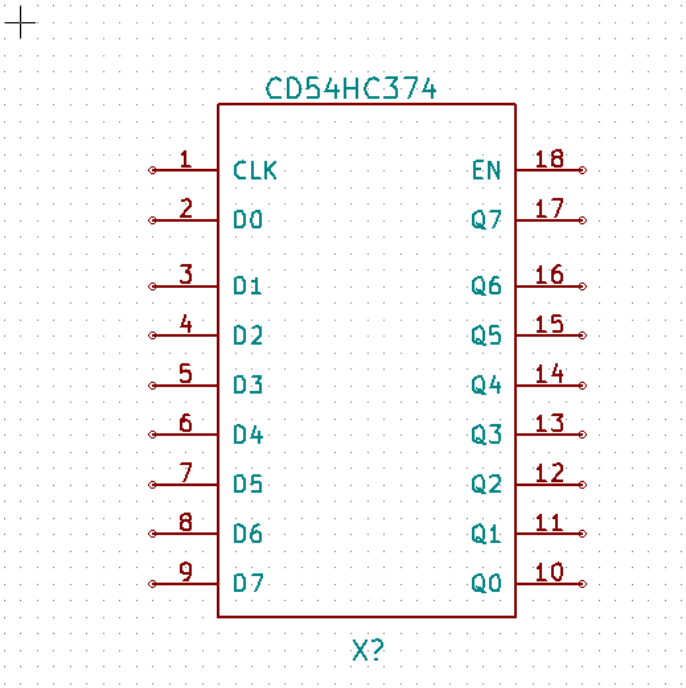

Figure 4.21: Pin diagram ofCD54HC374

4.5.2 Subcircuit Schematic Diagram CD54HC374

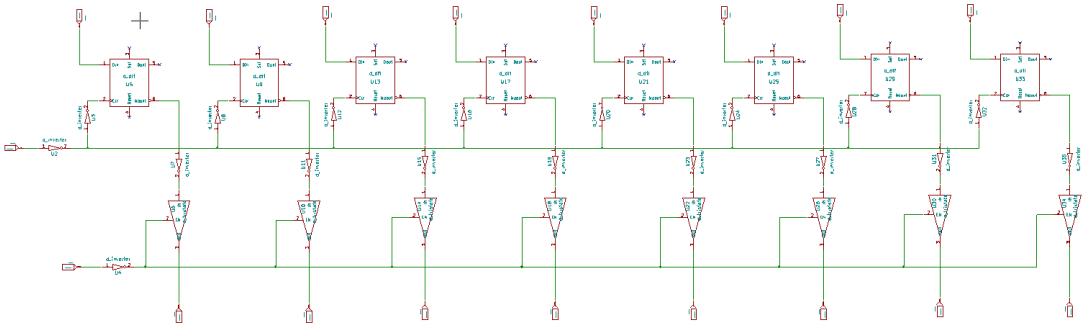

Figure 4.22: Subcircuit Schematic Diagram of CD54HC374

4.5.3 Test Circuit

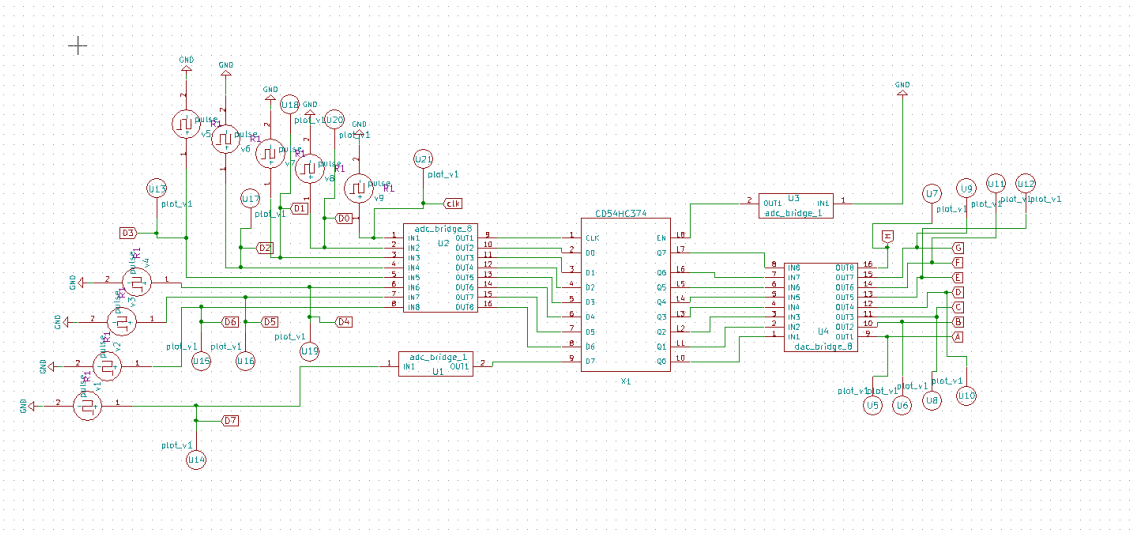

Figure 4.23: Test Circuit of CD54HC374

4.5.4 Input Plots

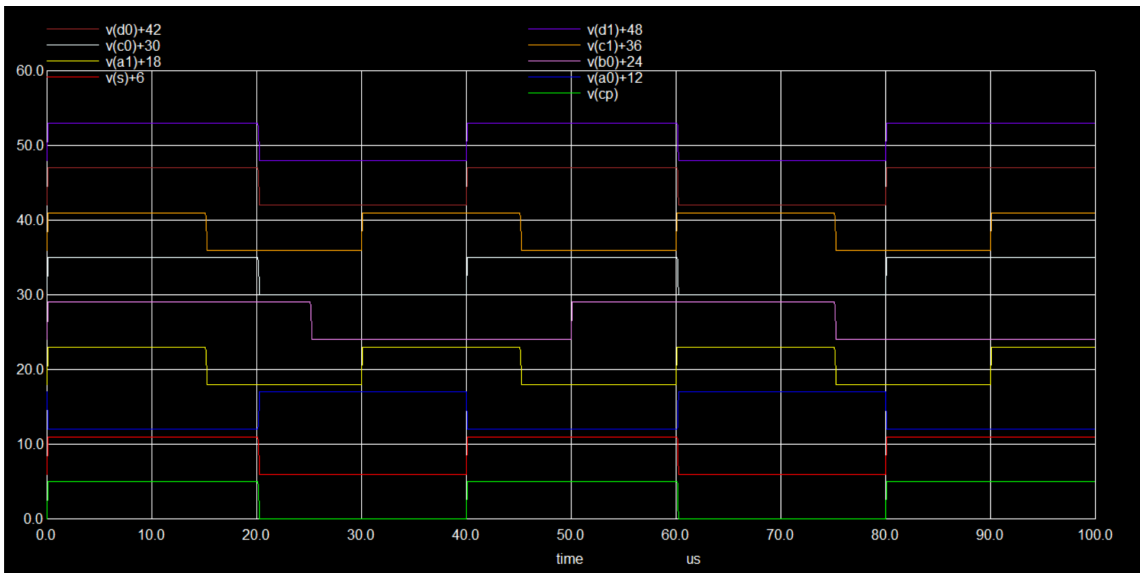

Figure 4.24: Input Plots Waveform of CD54HC374

4.5.5 Output Plots

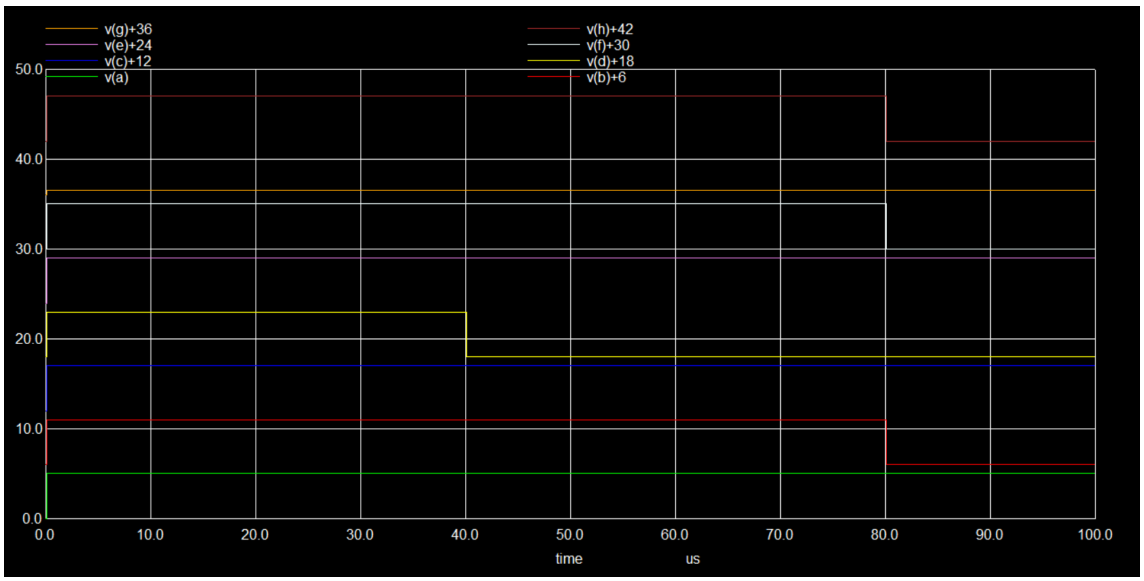

Figure 4.25: Output Voltage Waveform of CD54HC374

4.6 SN74HC377 - Octal D Type Flip Flops With Clock Enable

Description: These devices are positive-edge-triggered octal D type flip-flops with an enable input. The 'HC377 devices are similar to the 'HC273 devices, but feature a latched clock-enable (CLKEN) input instead of a common clear.

4.6.1 IC Layout

This figure represents the Pin Package Diagram of CD54HC374 ic

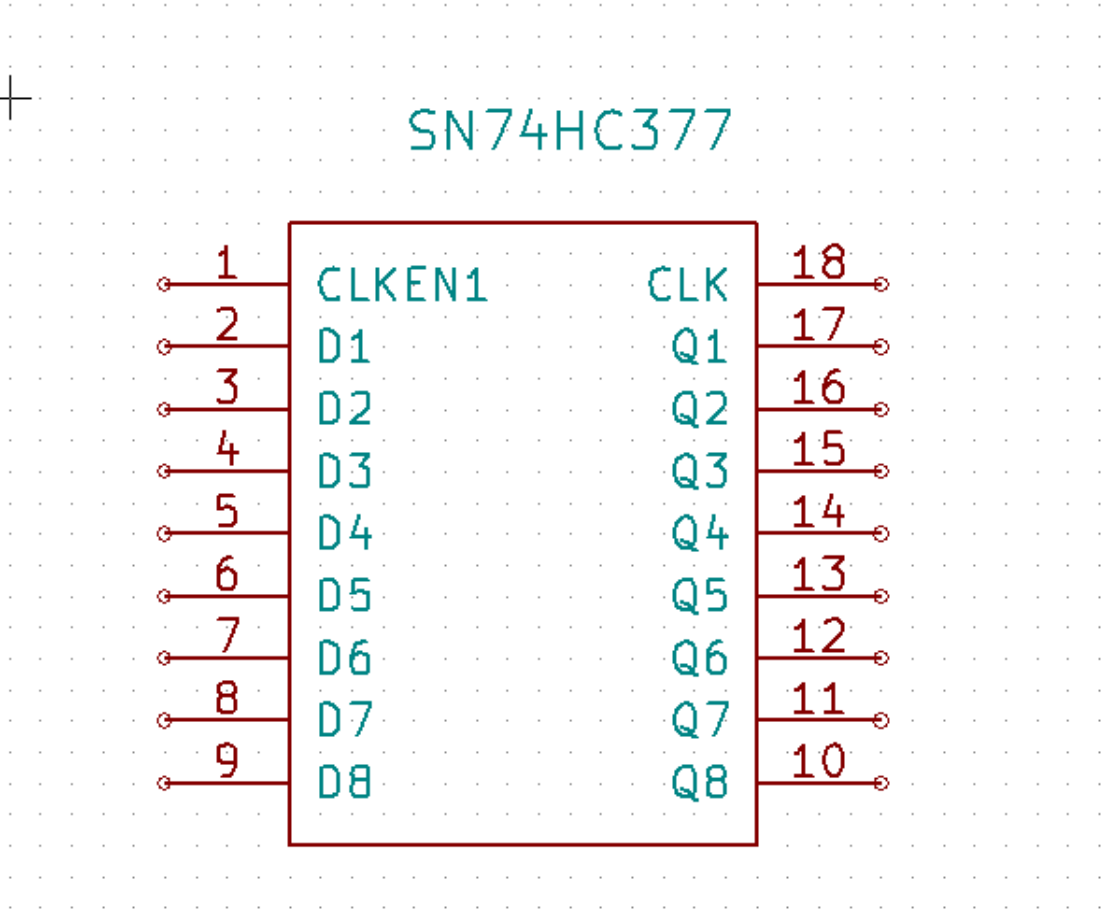

Figure 4.26: Pin diagram of SN74HC377

4.6.2 Subcircuit Schematic Diagram SN74HC377

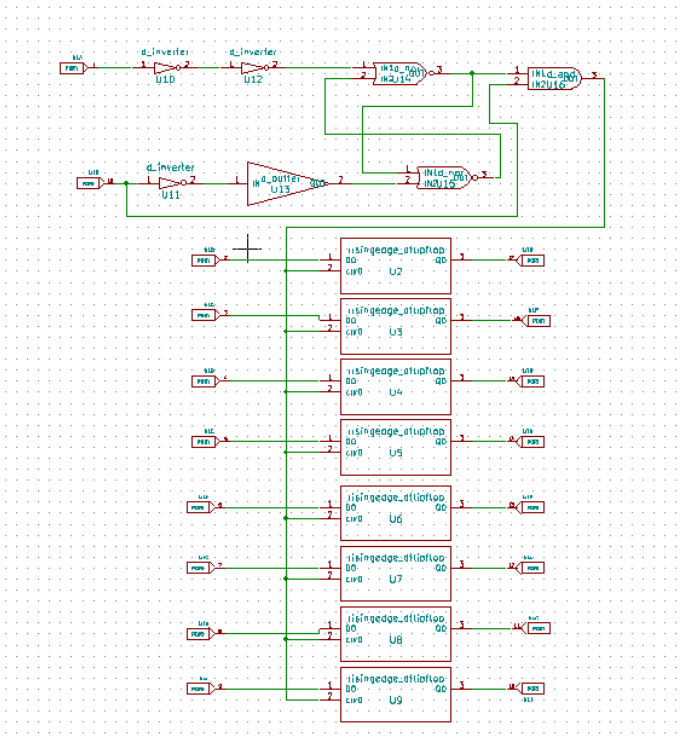

Figure 4.27: Subcircuit Schematic Diagram of SN74HC377

4.6.3 Test Circuit

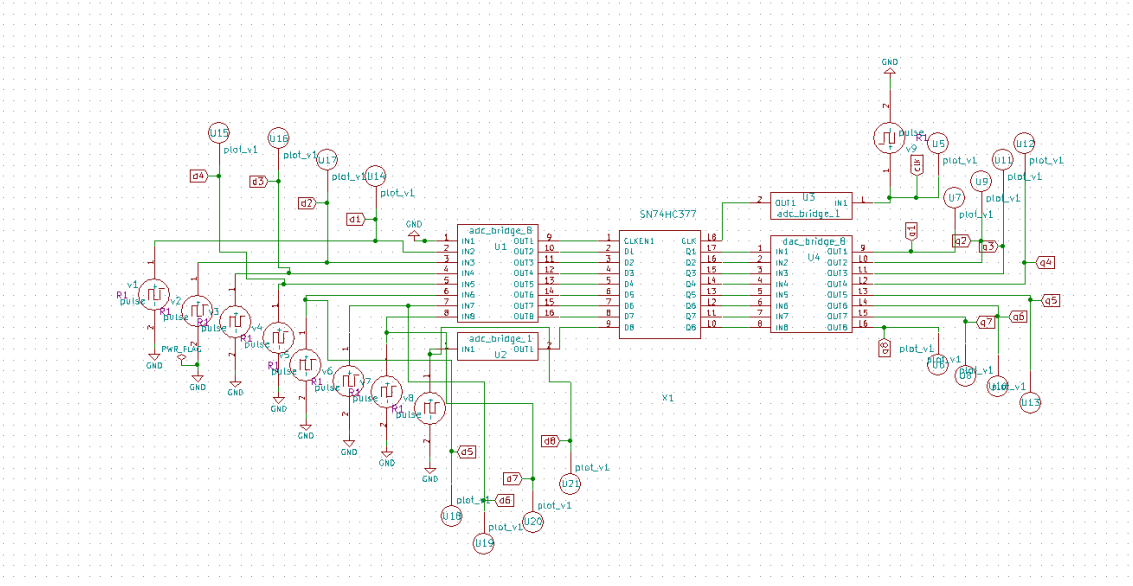

Figure 4.28: Test Circuit of SN74HC377

4.6.4 Input Plots

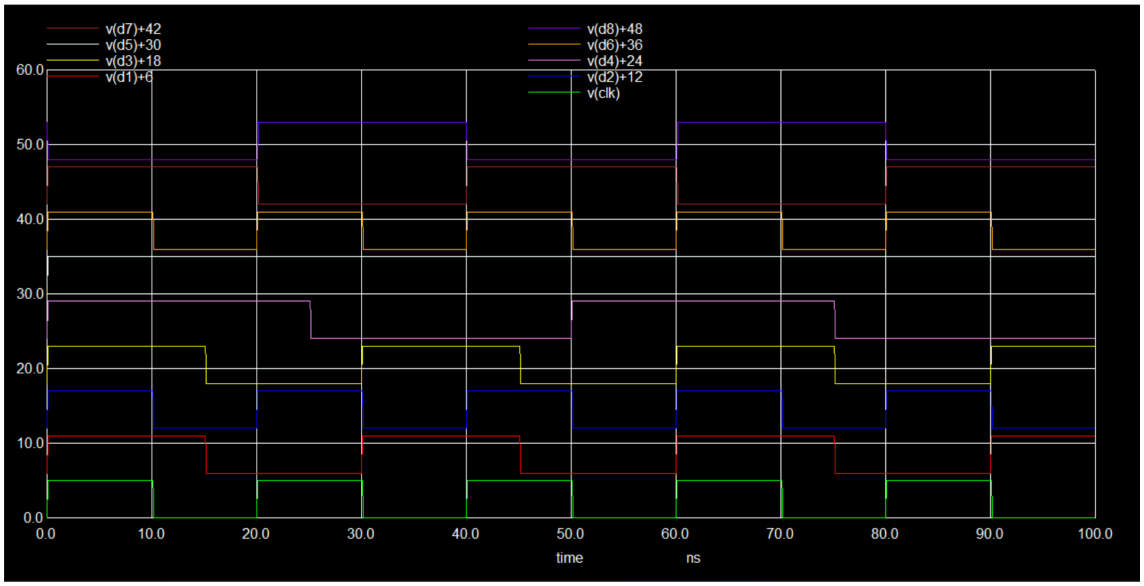

Figure 4.29: Input Plots Waveform of SN74HC377

4.6.5 Output Plots

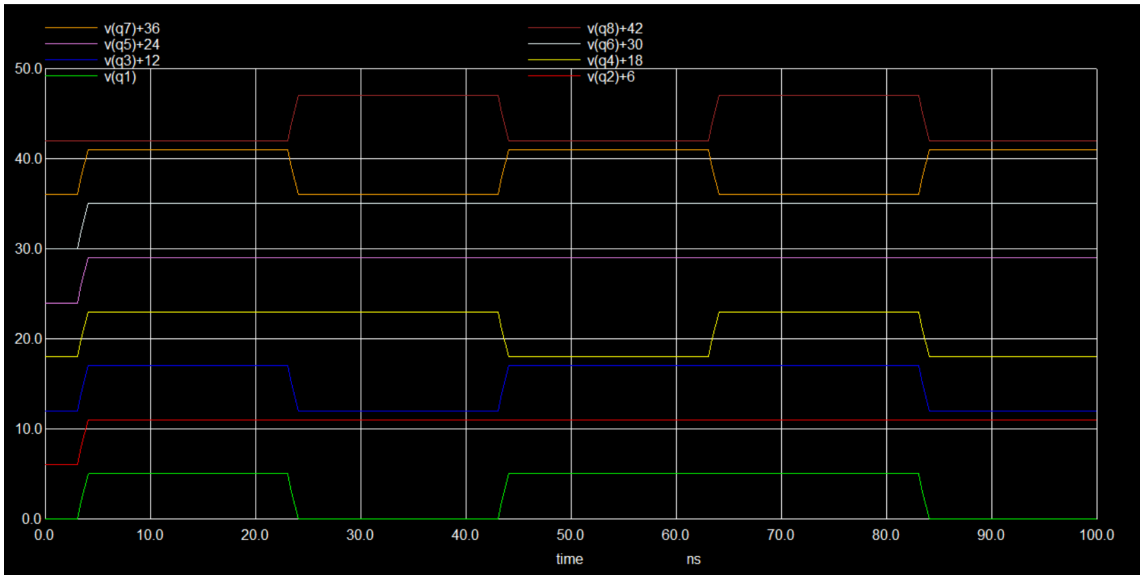

Figure 4.30: Output Voltage Waveform of SN74HC377

4.7 SN74LS606 - Octal 2 input multiplexed lactches

Description: The 'LS604, 'LS606, and 'LS607 multiplexed latches are ideal for storing data from two input buses, A and B, and providing the output bus with stored data from either the A or B register. The clock loads data on the positive-going (low-level to high-level) transition. The clock pin also controls the active and high-impedance states of the outputs. When the clock pin is low, the outputs are in the high-impedance or off state. When the clock pin is high, the outputs are enabled.

The 'LS604 is optimized for high-speed operation. The 'LS606 and 'LS607 are especially designed to eliminate decoding voltage spikes. These functions are ideal for interface from a 16-bit microprocessor to a 64K RAM board. The row and column addresses can be loaded as one word from the microprocessor and then multiplexed sequentially to the RAM during the time that RAS and CAS are active.

4.7.1 IC Layout

This figure represents the Pin Package Diagram of SN74LS606 ic

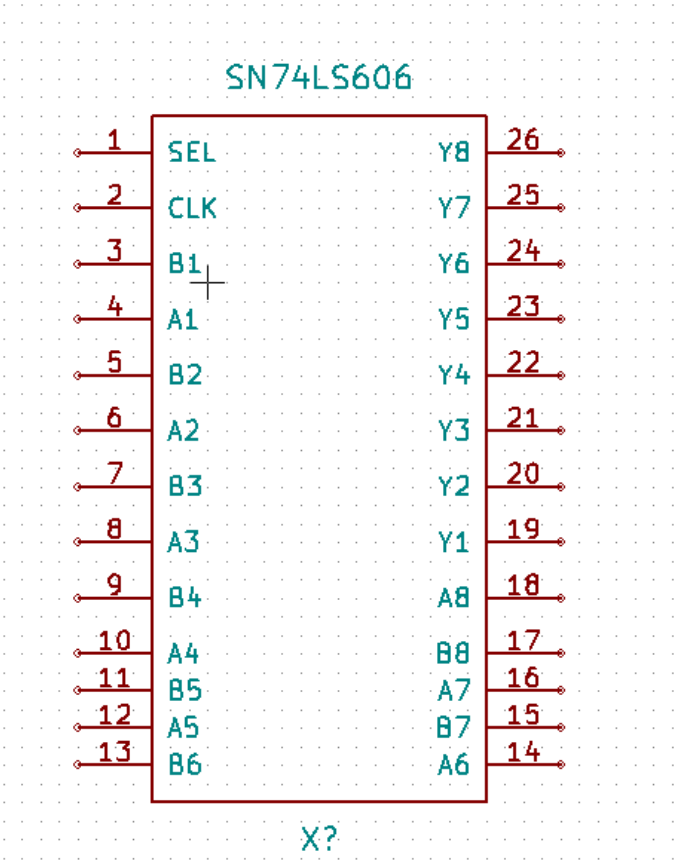

Figure 4.31: Pin diagram of SN74LS606

4.7.2 Subcircuit Schematic Diagram SN74LS606

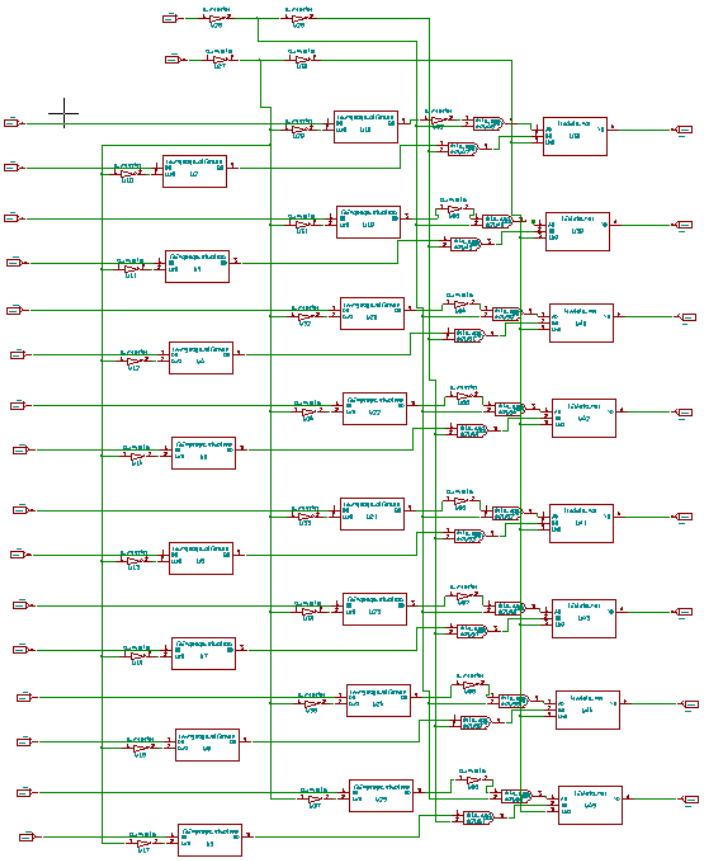

Figure 4.32: Subcircuit Schematic Diagram of SN74LS606

4.7.3 Test Circuit

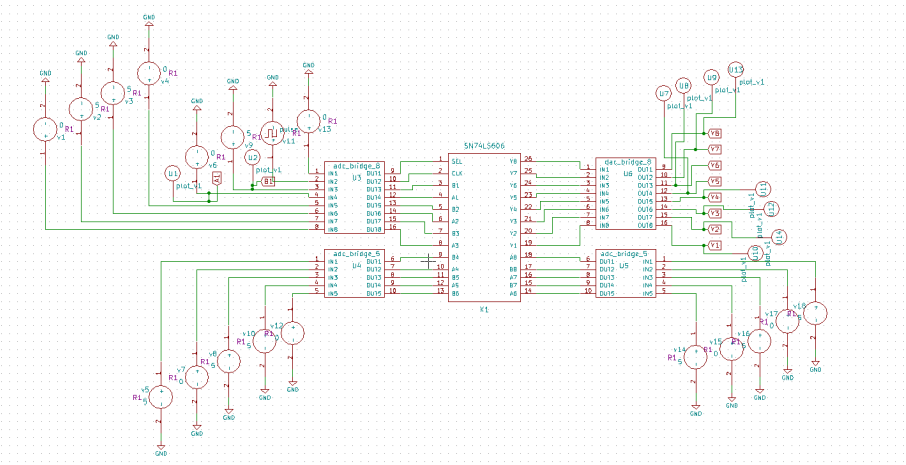

Figure 4.33: Test Circuit of SN74LS606

4.7.4 Input Plots

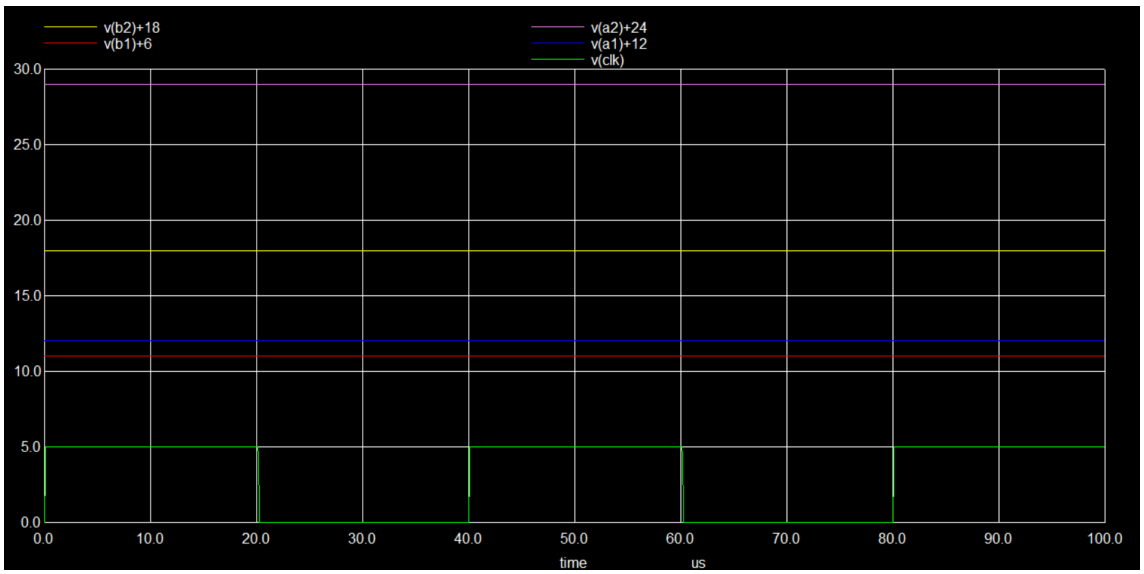

Figure 4.34: Input Plots Waveform of SN74LS606

4.7.5 Output Plots

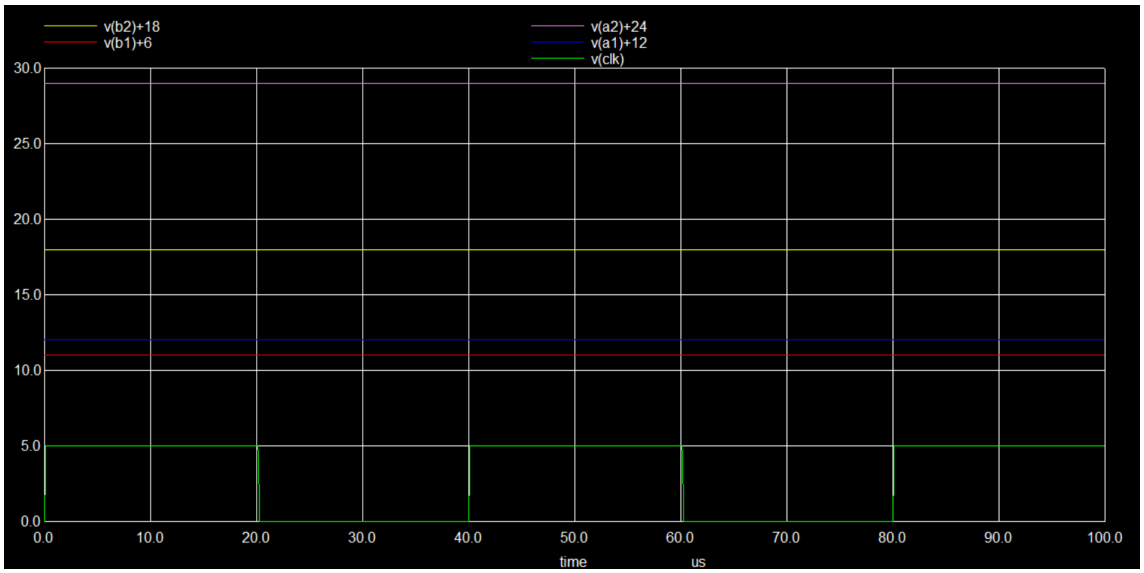

Figure 4.35: Output Voltage Waveform of SN74LS606

Chapter 5

Analog IC's

5.1 SN74CBTLV3257 - 4-Bit 1-of-2 FET Multiplexer/Demultiplexer

Description: The SN74CBTLV3257 is a 4-bit 1-of-2 high-speed FET multiplexer/demultiplexer. The low on-state resistance of the switch allows connections to be made with minimal propagation delay. The select (S) input controls the data flow. The FET multiplexers/demultiplexers are disabled when the output-enable (OE) input is high.

This device is fully specified for partial-power-down applications using Ioff. The Ioff feature ensures that damaging current will not backflow through the device when it is powered down. The device has isolation during power off. To ensure the high-impedance state during power up or power down, OE should be tied to VCC through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

5.1.1 IC Layout

This figure represents the Pin Package Diagram of SN74CBTLV3257 ic

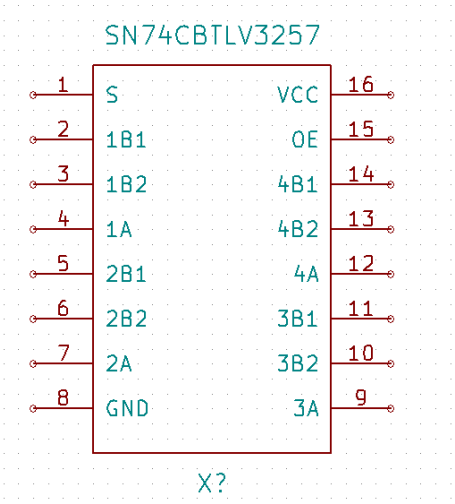

Figure 5.1: Pin diagram of SN74CBTLV3257

5.1.2 Subcircuit Schematic Diagram SN74CBTLV3257

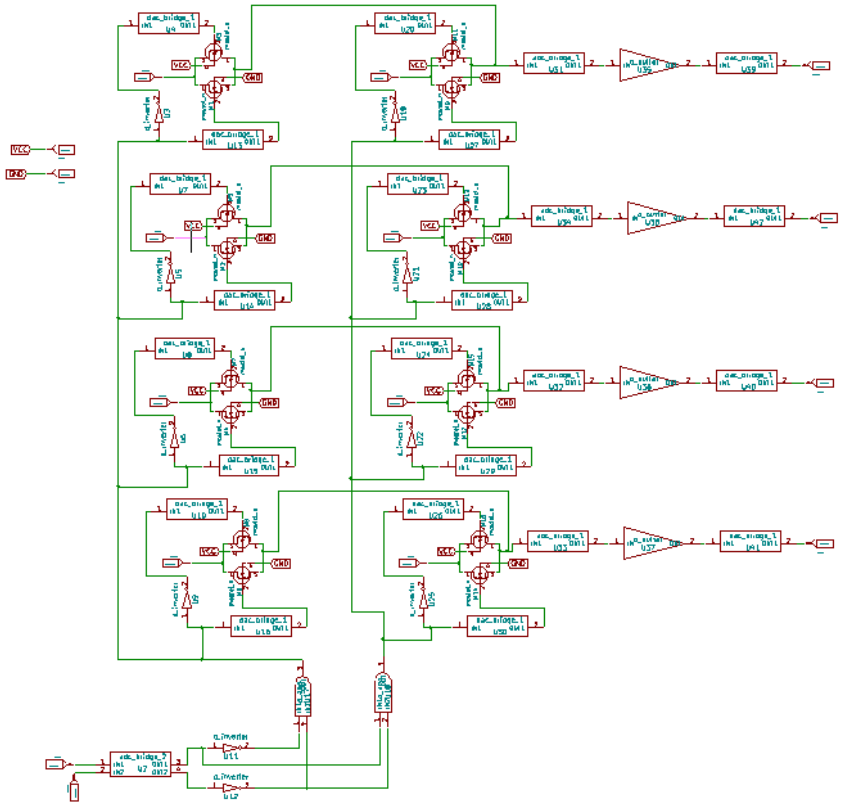

Figure 5.2: Subcircuit Schematic Diagram of SN74CBTLV3257

5.1.3 Test Circuit

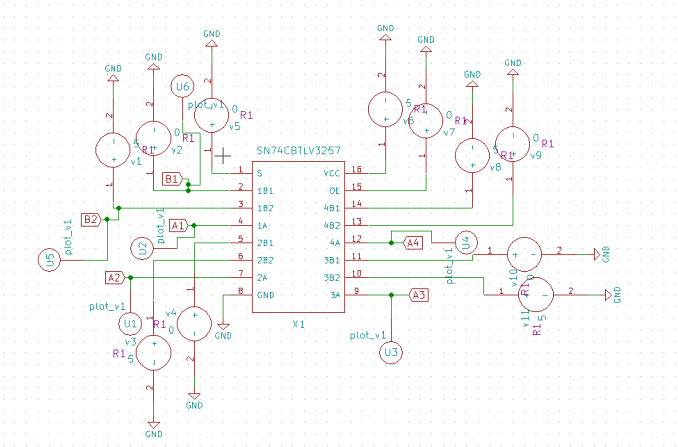

Figure 5.3: Test Circuit of SN74CBTLV3257

5.1.4 Input Plots

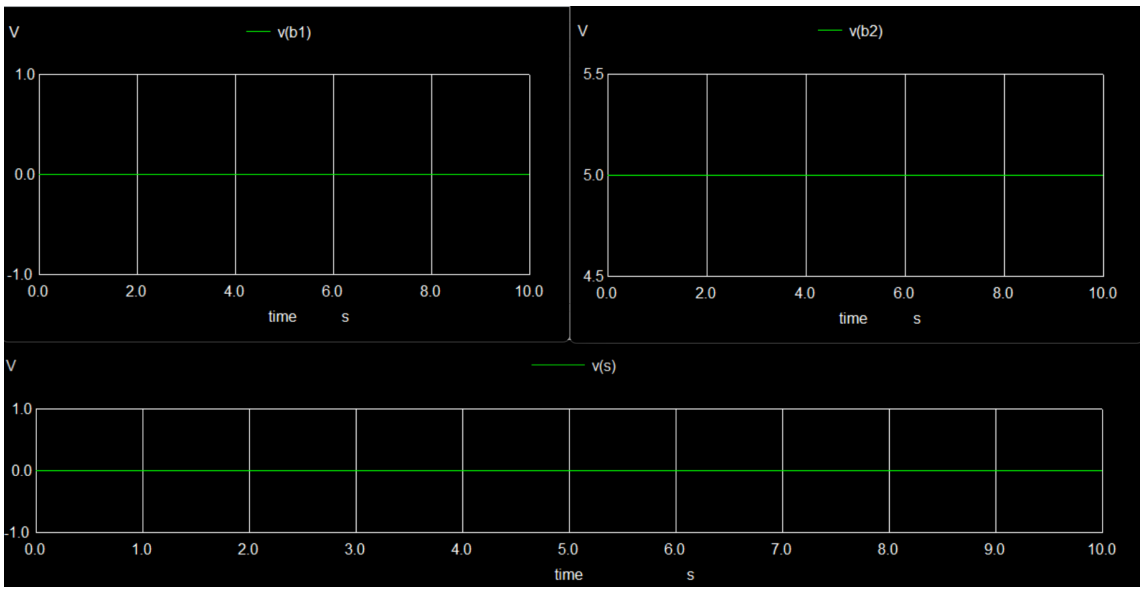

Figure 5.4: Input Plots Waveform of SN74CBTLV3257

5.1.5 Output Plots

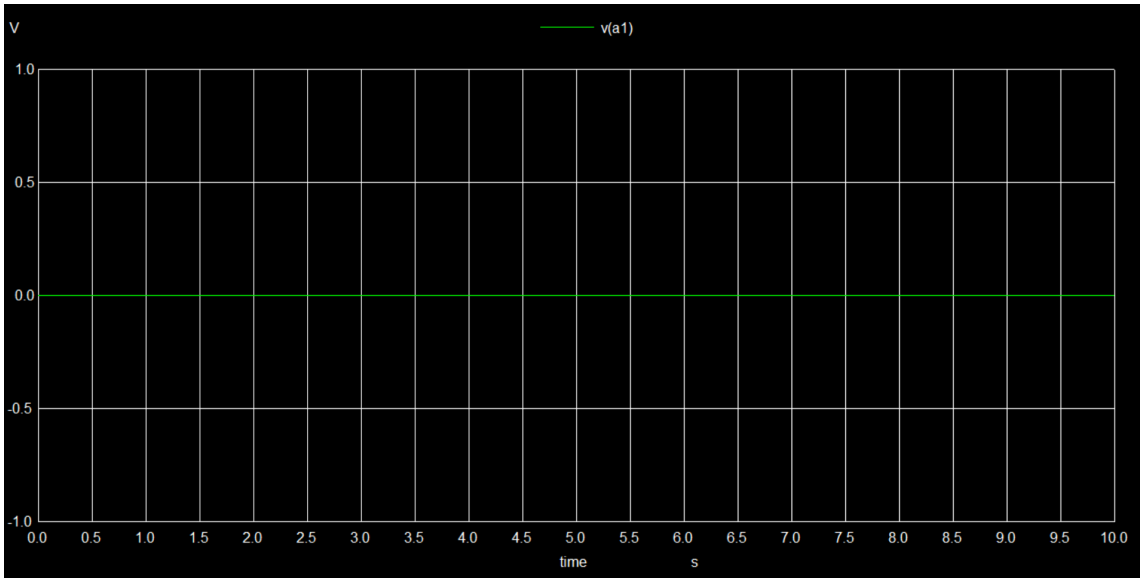

Figure 5.5: Output Voltage Waveform of SN74CBTLV3257

5.2 SN74LS38 - Quadruple 2-Input Positive Nand Buffer with Open collector

Description: These device contain four independent 2-input NAND buffer gates with open-collector outputs. The open-collector outputs require pull-up resistors to perform correctly. They may be connected to other open-collector outputs to implement active-low wired-OR or active-high wired-AND functions. Open-collector devices are often used to generate high VOH levels.

5.2.1 IC Layout

This figure represents the Pin Package Diagram of SN74LS38 ic

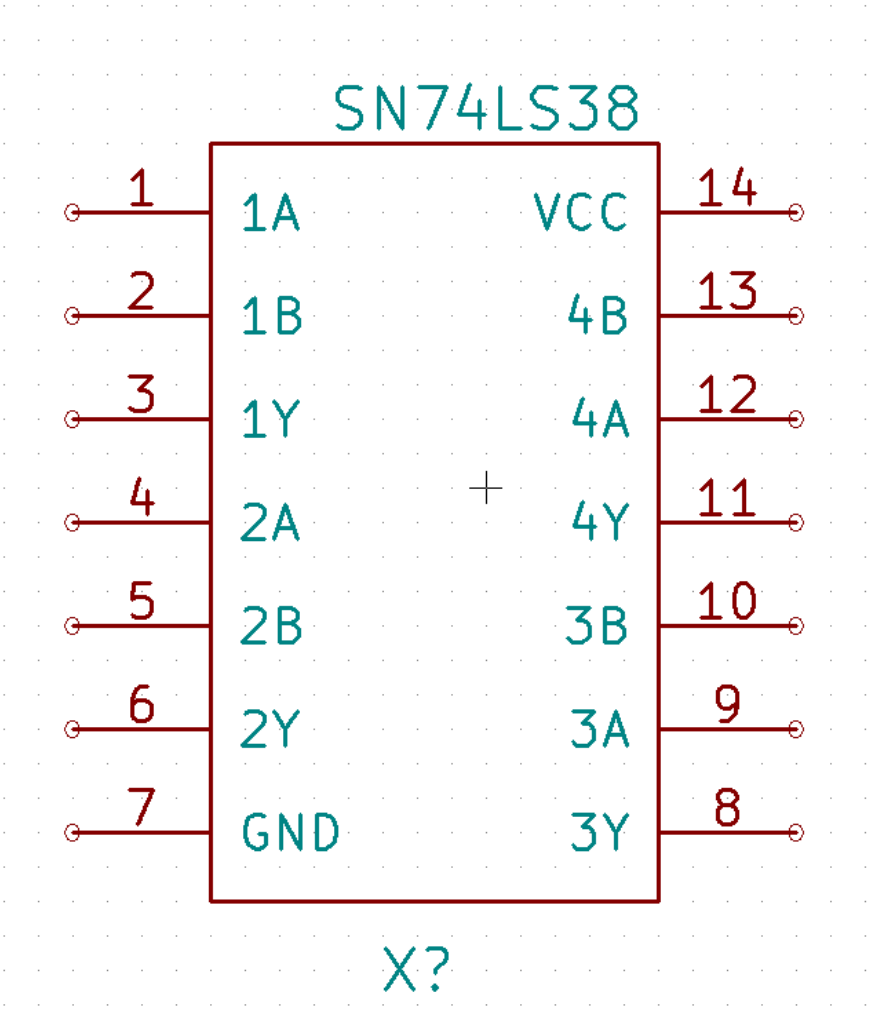

Figure 5.6: Pin diagram of SN74LS38

5.2.2 Subcircuit Schematic Diagram SN74LS38

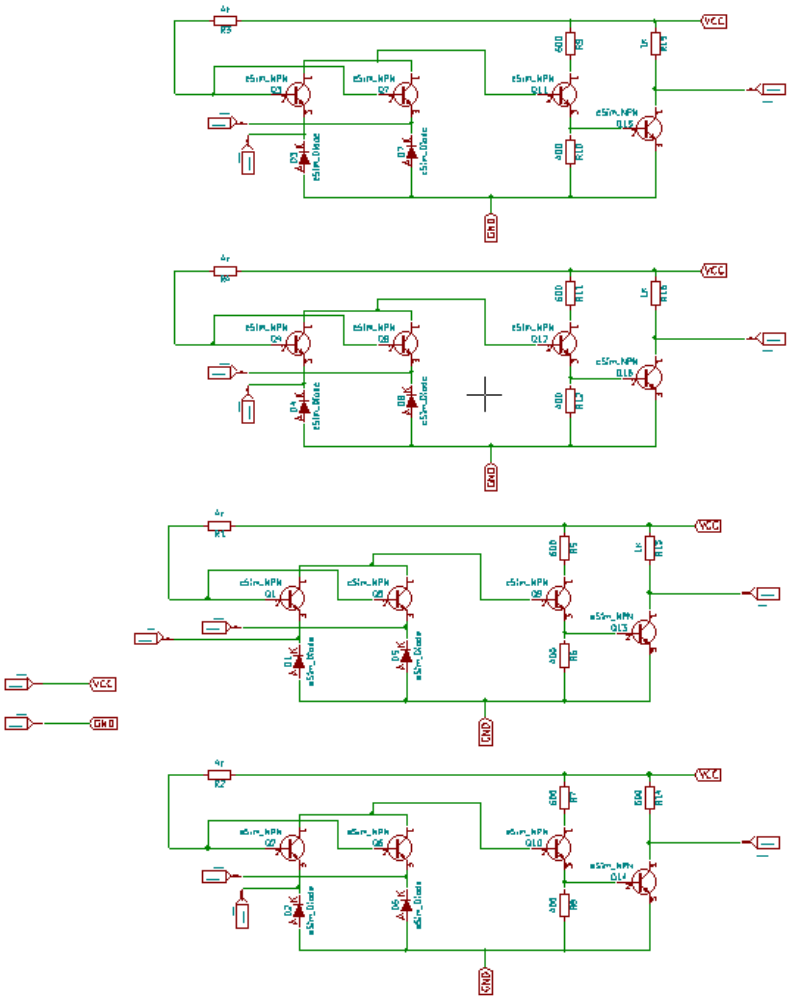

Figure 5.7: Subcircuit Schematic Diagram of SN74LS38

5.2.3 Test Circuit

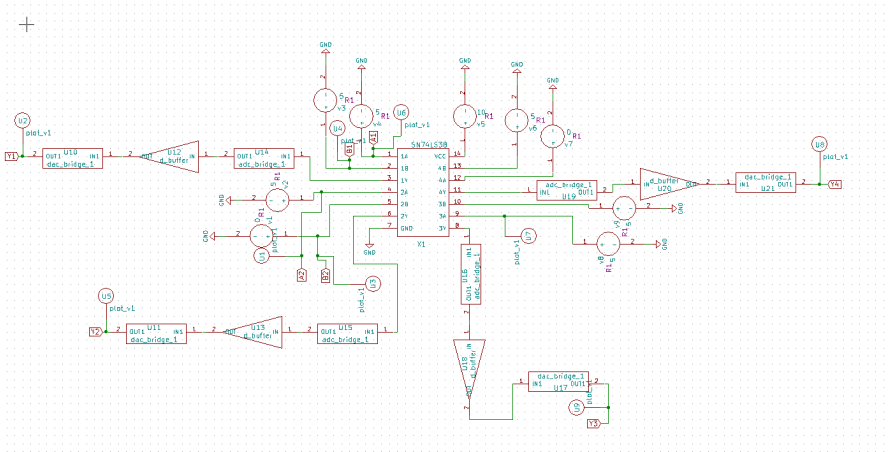

Figure 5.8: Test Circuit of SN74LS38

5.2.4 Input Plots

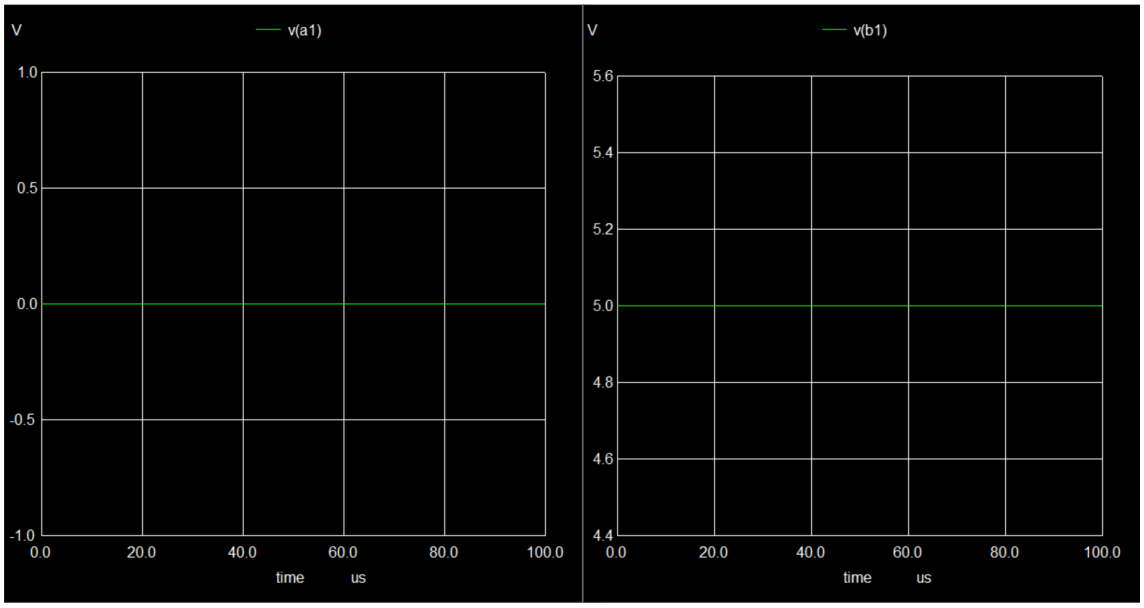

Figure 5.9: Input Plots Waveform of SN74LS38

5.2.5 Output Plots

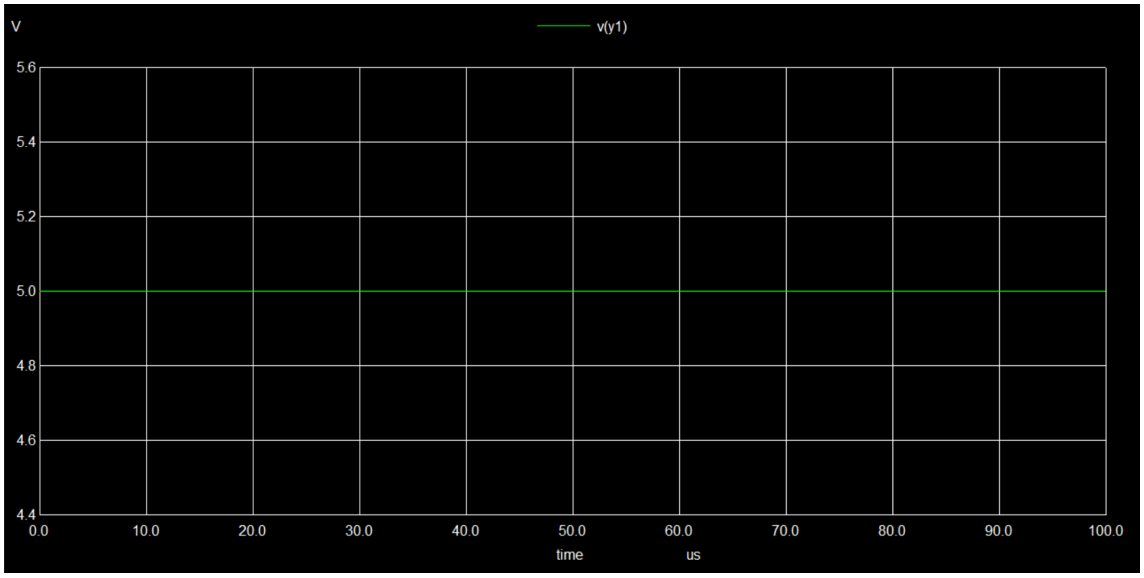

Figure 5.10: Output Voltage Waveform of SN74LS38

5.3 SN74CBT3384A - 10-Bit FET Bus Switch

Description: The SN74CBT3384A provides ten bits of high-speed TTL-compatible bus switching. The low on-state resistance of the switch allows connections to be made with minimal propagation delay. The device is organized as two 5-bit switches with separate output-enable (OE) inputs. When OE is low, the switch is on and port A is connected to port B. When OE is high, the switch is open and a high-impedance state exists between the two ports.

5.3.1 IC Layout

This figure represents the Pin Package Diagram of SN74CBT3384Aic

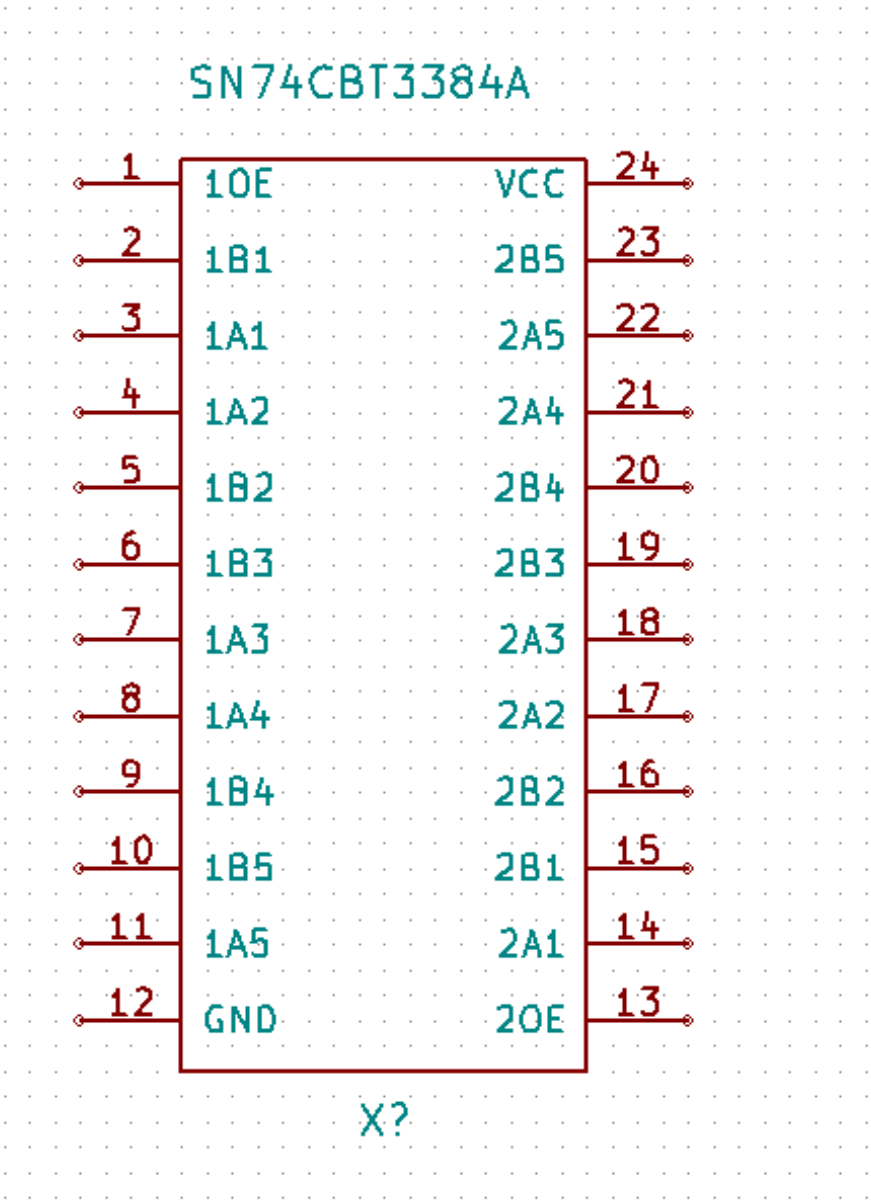

Figure 5.11: Pin diagram of SN74CBT3384A

5.3.2 Subcircuit Schematic Diagram SN74CBT3384A

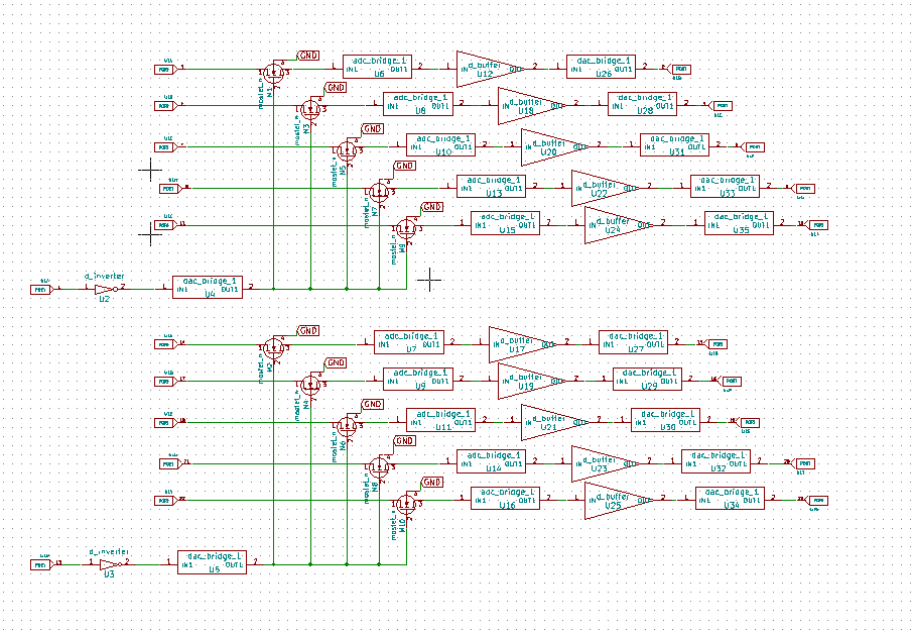

Figure 5.12: Subcircuit Schematic Diagram of SN74CBT3384A

5.3.3 Test Circuit

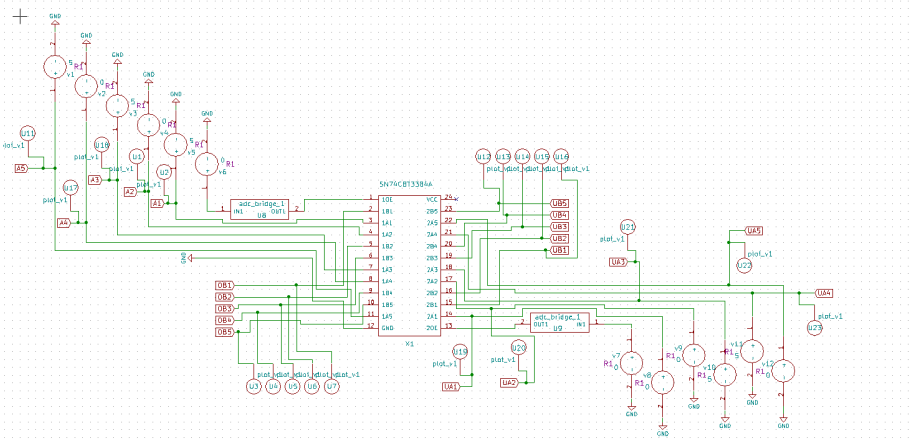

Figure 5.13: Test Circuit of SN74CBT3384A

5.3.4 Input Plots

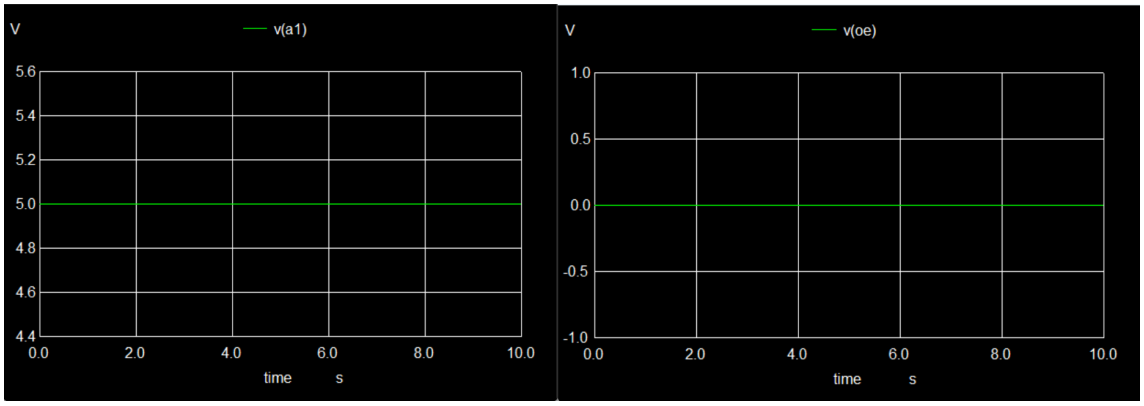

Figure 5.14: Input Plots Waveform of SN74CBT3384A

5.3.5 Output Plots

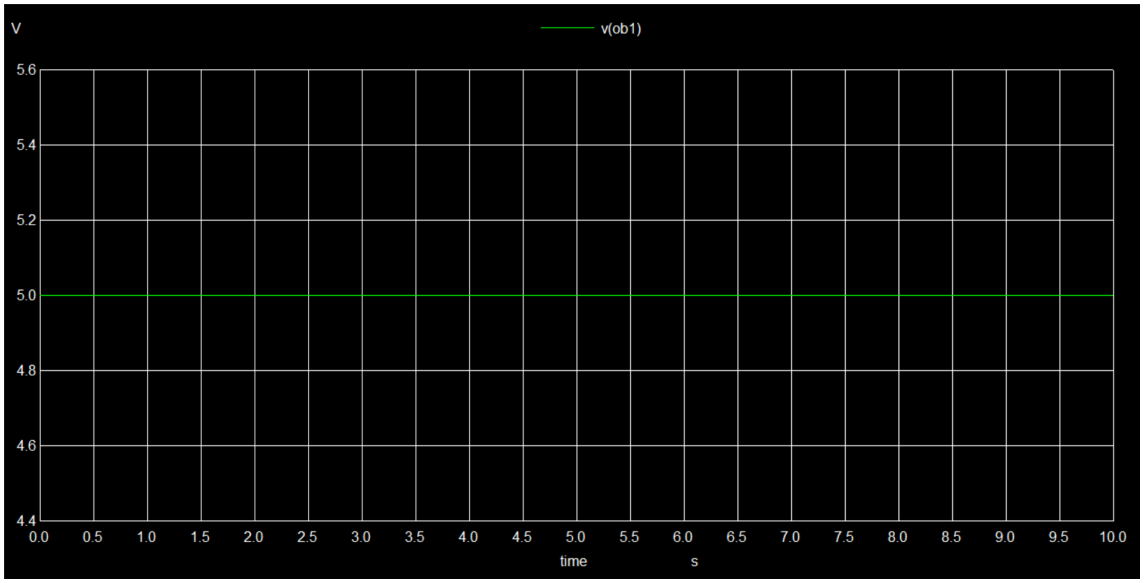

Figure 5.15: Output Voltage Waveform of SN74CBT3384A

5.4 SN74CBT3306C - Dual FET Bus Switch

Description: The SN74CBT3306C is a high-speed TTL-compatible FET bus switch with low ON-state resistance (ron), allowing for minimal propagation delay. Active Undershoot-Protection Circuitry on the A and B ports of the SN74CBT3306C provides protection for undershoot up to 2 V by sensing an undershoot event and ensuring that the switch remains in the proper OFF state.

The SN74CBT3306C is organized as two 1-bit bus switches with separate output-enable (1OE, 2OE) inputs. It can be used as two 1-bit bus switches or as one 2-bit bus switch. When OE is low, the associated 1-bit bus switch is ON, and the A port is connected to the B port, allowing bidirectional data flow between ports. When OE is high, the associated 1-bit bus switch is OFF, and the high-impedance state exists between the A and B ports.

5.4.1 IC Layout

This figure represents the Pin Package Diagram of SN74CBT3306C ic

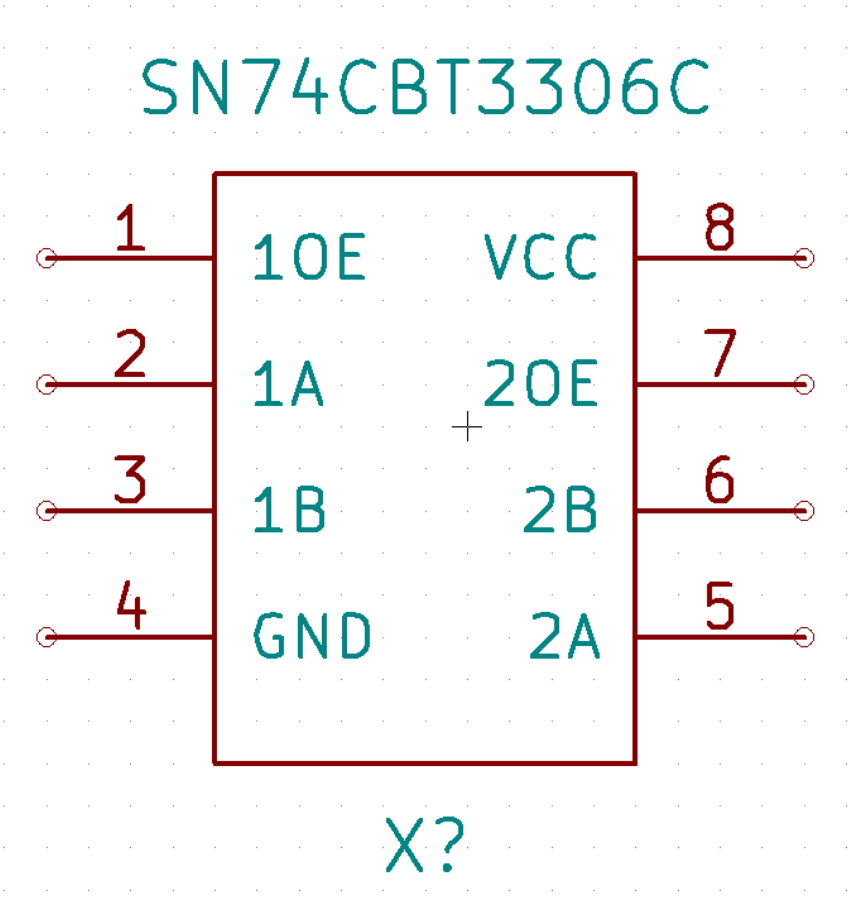

Figure 5.16: Pin diagram of SN74CBT3306C

5.4.2 Subcircuit Schematic Diagram SN74CBT3306C

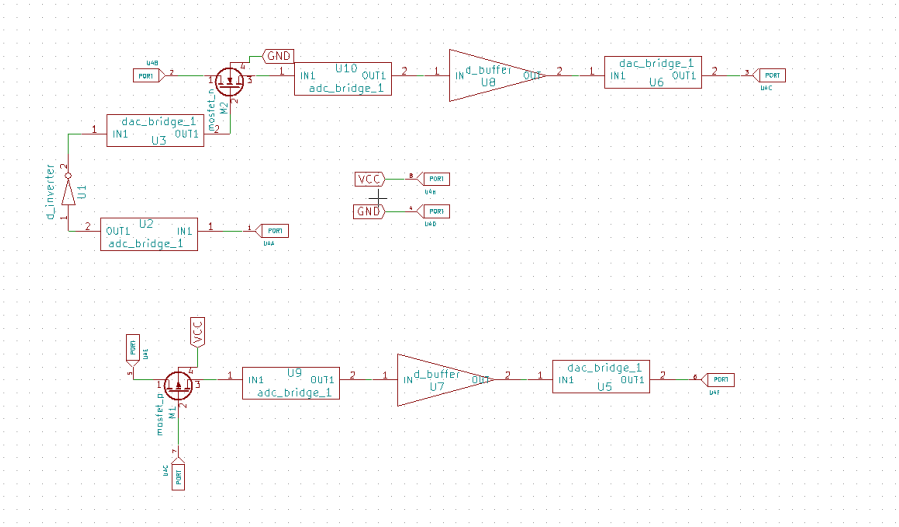

Figure 5.17: Subcircuit Schematic Diagram of SN74CBT3306C

5.4.3 Test Circuit

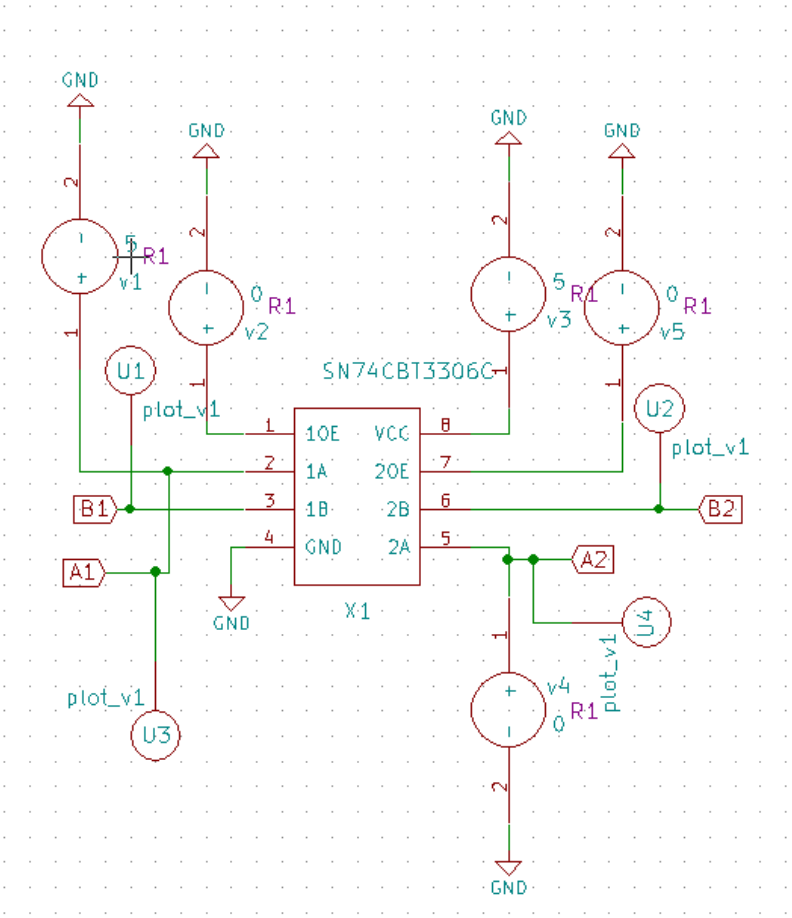

Figure 5.18: Test Circuit of SN74CBT3306C

5.4.4 Input Plots

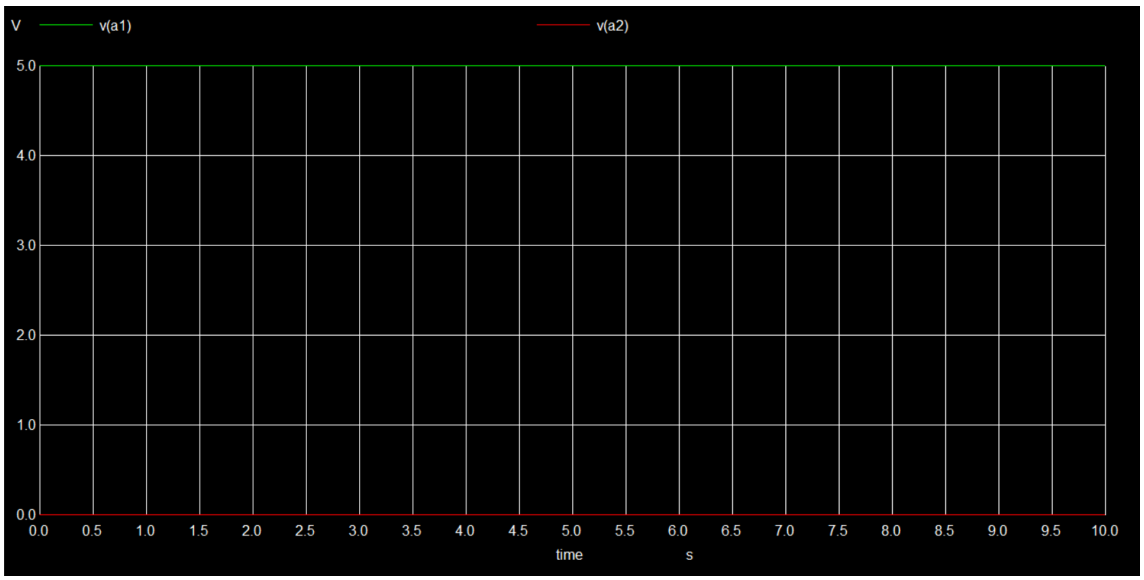

Figure 5.19: Input Plots Waveform of SN74CBT3306C

5.4.5 Output Plots

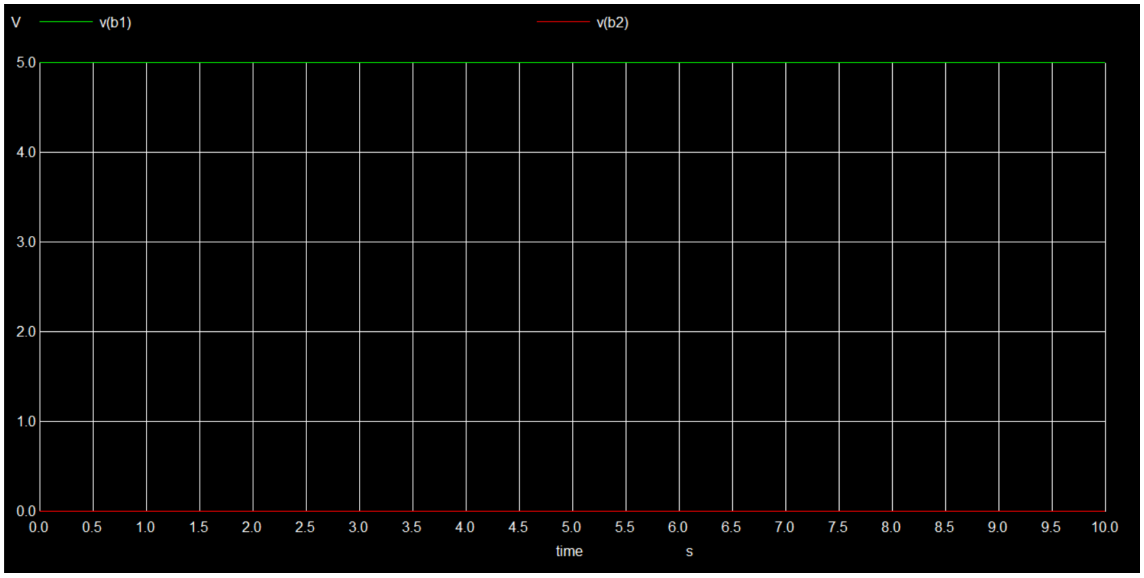

Figure 5.20: Output Voltage Waveform of SN74CBT3306C

5.5 SN74CBTLV3126 - Quadruple FET Bus Switch

Description: The SN74CBTLV3126 quadruple FET bus switch features independent line switches. Each switch is disabled when the associated output-enable (OE) input is low. To ensure the high-impedance state during power up or power down, OE should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

5.5.1 IC Layout

This figure represents the Pin Package Diagram of SN74CBTLV3126 Aic

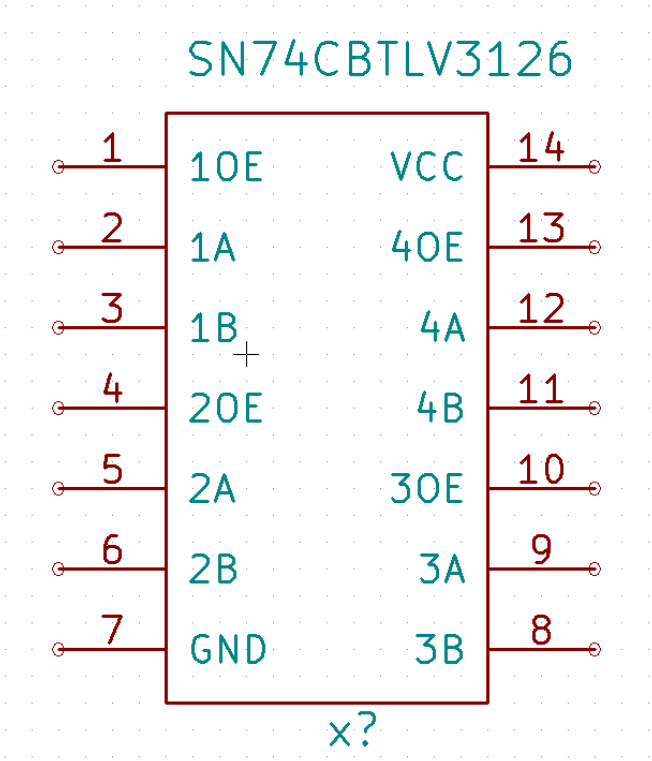

Figure 5.21: Pin diagram of SN74CBTLV3126

5.5.2 Subcircuit Schematic Diagram SN74CBTLV3126

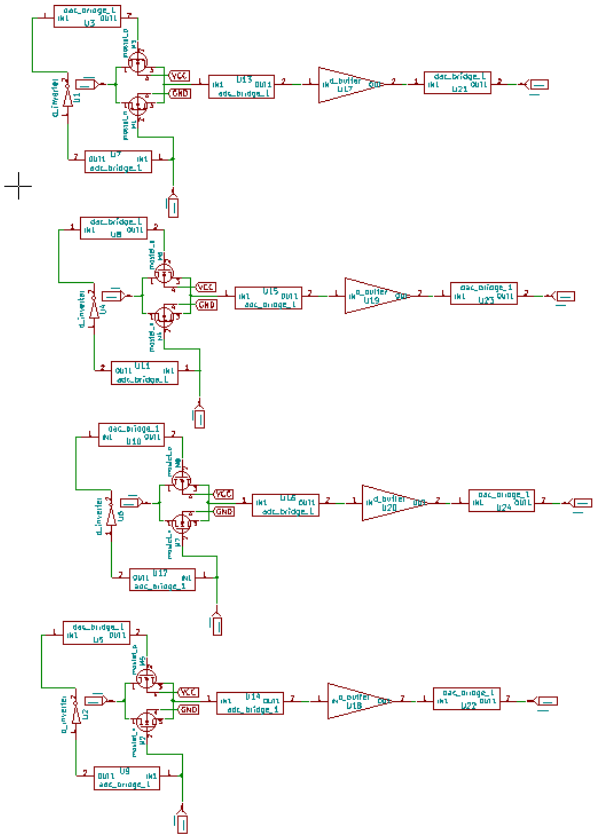

Figure 5.22: Subcircuit Schematic Diagram of SN74CBTLV3126

5.5.3 Test Circuit

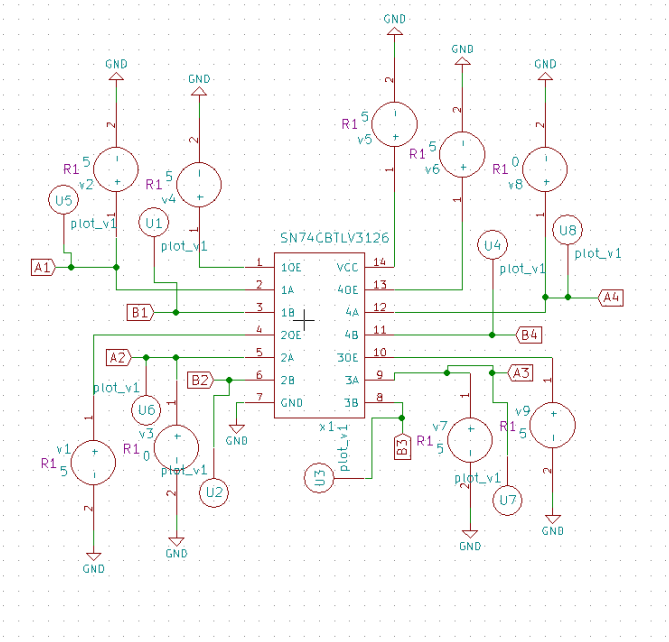

Figure 5.23: Test Circuit of SN74CBTLV3126

5.5.4 Input Plots

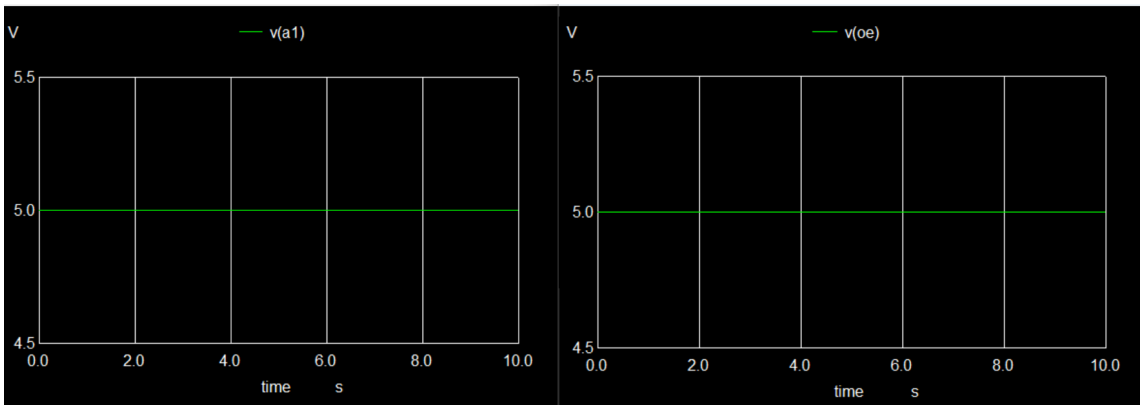

Figure 5.24: Input Plots Waveform of SN74CBTLV3126

5.5.5 Output Plots

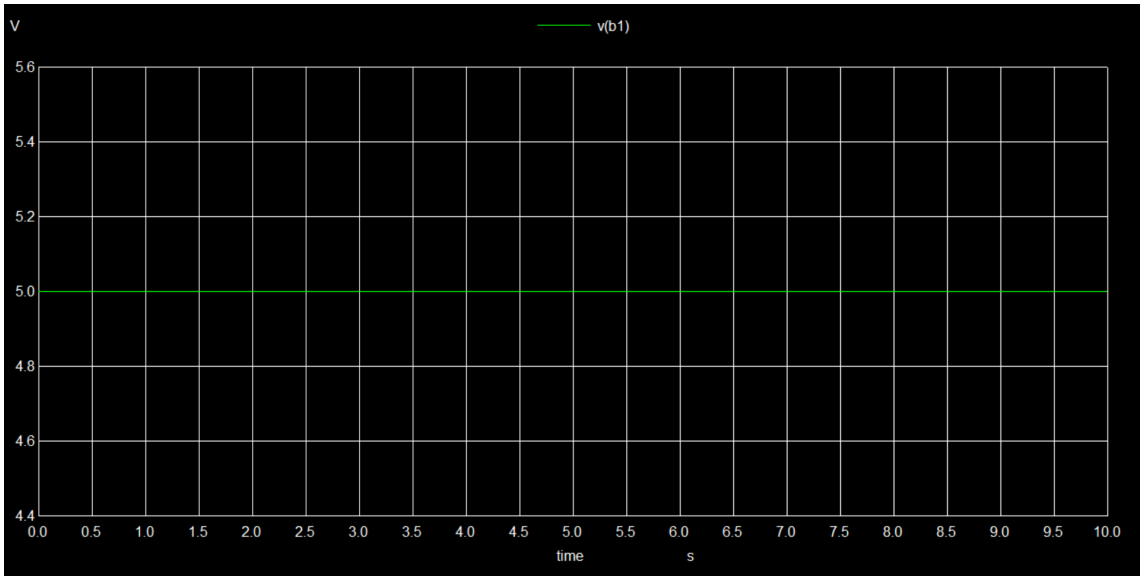

Figure 5.25: Output Voltage Waveform of SN74CBTLV3126

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