Summer Fellowship Report

On

Integrated Circuit Design using Subcircuit feature of eSim & Mixed Signal Simulation in eSim

Submitted by

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July 24, 2025

Acknowledgment

I would like to extend my sincere gratitude to the FOSSEE team at IIT Bombay for providing me with the invaluable opportunity to participate in the Summer Fellowship 2025. This prestigious program has been a profoundly rewarding experience, both in terms of technical enrichment and personal growth. Participating in this initiative enabled me to immerse myself in an intellectually stimulating environment that fosters innovation, self-learning, and excellence in the field of electronics.

Throughout the course of the project, I gained substantial exposure to opensource EDA tools and their pivotal role in modern circuit design and simulation. This handson experience not only enhanced my technical proficiency but also broadened my perspective on the significance of opensource contributions in advancing research and development. I am deeply indebted to Prof. Kannan M. Moudgalya for his visionary leadership and for spearheading initiatives that empower young minds to contribute meaningfully to the technological ecosystem.

I would like to convey my heartfelt appreciation to my mentors Mr. Sumanto Kar, Mrs. Vineeta Ghavri, and Mrs. Usha Vishwanathan and the whole team whose constant support, insightful feedback, and patient guidance were instrumental in shaping the successful outcome of my project. Their mentorship was marked by clarity, encouragement, and accessibility, creating a nurturing environment that allowed me to confidently tackle challenges and refine my problem-solving abilities.

This fellowship has significantly bolstered my foundational knowledge in electronics and deepened my interest in semiconductor design and hardware systems. The collaborative and research-driven atmosphere at FOSSEE provided me with a unique platform to explore new ideas, develop practical solutions, and understand the nuances of open-source development. The experience has also honed my skills in critical thinking, documentation, and technical communication.

Being selected for and contributing to this prestigious program represents a landmark achievement in my academic journey. The skills, insights, and experiences I have gained will undoubtedly serve as a strong foundation as I pursue further endeavors in the VLSI and hardware design domains. I remain committed to contributing to the open-source community and hope to carry forward the values of innovation, integrity, and collaboration that FOSSEE exemplifies.

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Chapter 1

Introduction

The FOSSEE (Free/Libre and Open Source Software for Education) project is a national initiative that actively promotes the adoption of open-source software tools to enhance the quality of education in India. Its primary objective is to reduce the reliance on proprietary software within academic institutions by advocating for and facilitating the use of free and open-source alternatives. Through a wide range of initiatives, FOSSEE encourages the replacement of commercial software with robust and freely available counterparts. In addition, the project undertakes the development of new FLOSS tools and upgrades existing ones to align with the evolving needs of academia and research.[12]

FOSSEE operates under the National Mission on Education through Information and Communication Technology (NMEICT), an initiative of the Ministry of Education (formerly MHRD), Government of India. The project provides a comprehensive ecosystem of support through detailed documentation, interactive tutorials, hands-on training sessions, and workshops, all aimed at empowering students, educators, and professionals to effectively integrate open-source tools into their academic and research endeavors. FOSSEE's unwavering commitment to fostering a collaborative, inclusive, and innovation-driven environment has significantly contributed to the democratization of technology, opening up new opportunities for accessible learning and creative exploration across diverse domains.

1.1 eSim

eSim, developed by the FOSSEE project at IIT Bombay, is a powerful and versatile open-source software tool designed for electronic circuit design and simulation. It integrates multiple open-source software packages into a unified platform, streamlining the process of designing, simulating, and analyzing electronic circuits. Tailored to meet the needs of students, educators, and professionals, eSim serves as a cost-effective and accessible alternative to proprietary EDA tools.

The software offers a comprehensive suite of features, including schematic creation, circuit simulation, PCB design, and access to an extensive library of elec-

tronic components. A noteworthy feature of eSim is its Subcircuit capability, which allows users to build complex circuits by integrating simpler, reusable submodules—enhancing modular design and scalability.

Through the development and promotion of eSim, FOSSEE continues to champion the use of open-source technologies in engineering education and professional practice, fostering innovation, collaboration, and self-reliance in the field of electronics design.

1.2 KiCad

KiCad is an open-source software suite for electronic design automation (EDA), used primarily for creating schematics and designing printed circuit boards (PCBs). Developed and maintained by a global community of contributors, KiCad offers a professional-grade alternative to proprietary PCB design tools, supporting multilayer board layouts and complex routing.

The tool includes an intuitive schematic editor for drawing circuit diagrams, a powerful PCB layout editor with design rule checking, and integrated 3D visualization tools for inspecting board designs. KiCad also provides extensive libraries of symbols and footprints, with the flexibility to create custom components as needed.

One of KiCad's major strengths is its interoperability with simulation tools like NgSpice, enabling seamless integration of schematic design and circuit simulation. This makes KiCad an ideal choice for both students and professionals seeking a free, open-source solution for end-to-end PCB development—from conceptual design to fabrication-ready outputs.

1.3 NgSpice

NgSpice is a widely used open-source SPICE simulator for electrical and electronic circuit analysis. It supports a broad range of circuit elements, including passive components (resistors, capacitors, and inductors), active devices such as diodes, JFETs, BJTs, and MOSFETs, as well as transmission lines and various other components—all defined through a netlist.

NgSpice is capable of simulating both analog and digital circuits, including event-driven digital simulations and mixed-signal systems. It efficiently handles everything from simple logic gates to highly complex circuits. The simulator comes with an extensive library of device models for analog, digital, active, and passive elements. These models are sourced from NgSpice's internal collections, semiconductor manufacturers, or foundries.

Users describe circuits using netlists, and the simulator provides output in the form of graphical waveforms or tabulated data, including voltage, current, and other electrical parameters. This makes NgSpice a powerful tool for both academic learning and advanced circuit analysis.

1.4 Makerchip

Makerchip is a user-friendly platform that provides convenient access to a suite of tools for digital circuit design, catering to both beginners and experienced users. It offers both browser-based and desktop environments for coding, compiling, simulating, and debugging Verilog, SystemVerilog, and Transaction-Level Verilog (TL-Verilog) designs. By integrating open-source and proprietary tools, Makerchip ensures a robust and feature-rich design experience.

A key integration exists between eSim and Makerchip through a Python-based utility known as the Makerchip-App, which launches the Makerchip IDE directly from within eSim. This interface facilitates a seamless workflow for users wishing to simulate digital designs as part of their overall circuit development process.

Makerchip emphasizes accessibility and ease of use through its clean interface, intuitive workflows, and comprehensive simulation features, aiming to make digital design both engaging and efficient for users across varying proficiency levels.

However, a notable limitation in the current open-source ecosystem is the lack of a unified platform that supports schematic capture, circuit simulation, and PCB layout within a single tool. While tools such as KiCad focus primarily on PCB design and others like gEDA support circuit simulation, none offer complete end-to-end functionality. In contrast, eSim addresses this gap by combining schematic creation, simulation, and layout design within a single cohesive environment—making it a comprehensive open-source alternative to proprietary EDA software.

Chapter 2

Features of eSim

The development of eSim stems from the vision of providing a comprehensive, open-source EDA (Electronic Design Automation) solution tailored for electronics and electrical engineers. The goal is to deliver a unified platform capable of performing schematic creation, PCB design, and circuit simulation—covering analog, digital, and mixed-signal domains. Additionally, eSim offers the flexibility to create and incorporate custom models and components, empowering users to extend its capabilities for diverse design needs.

eSim offers the following key features:

1. **Schematic Creation: eSim** provides an easy-to-use graphical interface for drawing circuit schematics, making it accessible for users of all levels. Users can drag and drop components from the library onto the schematic, simplifying the design process. Comprehensive editing tools allow for easy modification of schematics, including moving, rotating, and labeling components.

2. **Circuit Simulation: eSim** supports **SPICE (Simulation Program with Integrated Circuit Emphasis)**, a widely accepted standard for simulating analog and digital circuits. Users can perform transient, AC, and DC analysis to understand circuit behavior over time and frequency. An integrated waveform viewer aids in visualizing simulation results for better debugging and analysis.

3. **PCB Design:** The PCB layout editor allows users to place components and route traces with precision. **eSim** includes **DRC (Design Rule Check)** capabilities to ensure the PCB design adheres to manufacturing and electrical constraints. Users can directly generate **Gerber files**, the industry standard for PCB fabrication.

4. **Subcircuit Feature:** This feature enables users to create complex circuits by integrating smaller subcircuits, promoting modular and hierarchical design. Subcircuits can be reused across projects, enhancing design efficiency and reducing redundancy.

5. **Model Builder:** The Model Builder module allows users to define custom device models for components such as Diodes, BJTs, MOSFETs, JFETs, IG-

BTs, and Magnetic Cores. This is particularly useful for simulations involving non-standard or emerging devices.

6. **KiCad to NgSpice Converter:** This module bridges the gap between schematic design and simulation by enabling the translation of circuit schematics into NgSpice-compatible formats. It supports configuration of sources, model parameters, and subcircuits directly within the design environment.

7. **NGHDL Integration: NGHDL** is a simulation module integrated with **eSim** to support mixed-signal simulation using **VHDL** code. It allows seamless co-simulation of analog and digital components in the same design.

8. **NgVeri Integration: NgVeri** supports mixed-signal simulation using **Verilog**, **SystemVerilog**, and **Transaction-Level Verilog (TL-Verilog)**. It allows users to integrate and simulate HDL-based designs within the **eSim** framework.

9. **Makerchip Interface: eSim** interfaces with the cloud-based digital design platform **Makerchip** through a Python-based tool called **Makerchip-App**. It enables users to simulate Verilog, SystemVerilog, and TL-Verilog designs directly in the browser.

10. **Verilator Integration: Verilator** is a high-performance simulator that converts Verilog/SystemVerilog code into C++ object files. These files are linked with NgSpice to enable efficient mixed-signal simulations in **eSim**.

11. **Open Source Integration: eSim** integrates several powerful open-source tools such as **KiCad**, **NgSpice**, and **GHDL**, offering a complete EDA solution. Its open-source nature ensures free access to advanced circuit design functionalities without licensing barriers.

Chapter 3

Problem Statement

3.1 Problem Statement

To design and develop various Analog and Digital Integrated Circuit (IC) models in the form of subcircuits using device model files already available in the eSim library. These IC models, once successfully integrated into the eSim Subcircuit Library, will serve as reusable components for circuit design purposes by developers and end users.

3.2 Approach

Our implementation began with a detailed study of datasheets from reputed IC manufacturers such as Texas Instruments, Analog Devices, and NXP Semiconductors. We identified a diverse set of ICs that provide functionalities such as precision amplification, voltage comparison, encoding, and audio amplification. Each subcircuit was constructed based on verified datasheet information and subsequently tested using NgSpice simulations to validate basic configurations.

The step-by-step roadmap followed is outlined below:

1. **Analyzing Datasheets:** The first step involved reviewing datasheets of various analog and digital ICs to identify models not currently present in the eSim library. Once a candidate IC was shortlisted, we analyzed its detailed schematic, electrical characteristics, and truth table. Upon verifying these design elements, the IC was finalized for implementation.

2. **Subcircuit Creation:** The selected IC was modeled as a subcircuit in eSim using only the existing device model files in the eSim library. The design process strictly adhered to official datasheet specifications. This phase also included creating the symbol and pin diagram of the IC based on its package type and pin configuration.

3. **Test Circuit Design:** After the subcircuit was modeled, we designed test circuits as recommended in the respective datasheets. These test cases were specifically constructed to validate the functional behavior of the IC under various input conditions.

4. **Schematic Testing:** The designed test circuits were then simulated using eSim's KiCad-to-NgSpice conversion and simulation interface. Output waveforms and plots were analyzed to verify expected performance. If the outputs did not align with datasheet specifications, the process reverted to the design phase to identify and rectify potential errors. The subcircuit and its associated test circuit were then revalidated.

Chapter 4

Integrated Circuit Design

4.1 CD4025B

The CD4025B is a CMOS logic IC from Texas Instruments that contains three independent 3-input NOR gates. It is part of the high-voltage CD4000 series and operates across a wide voltage range of 3 V to 15 V, with an absolute maximum rating of 20 V, making it suitable for a variety of digital applications. The IC features buffered inputs and outputs for improved signal integrity and noise immunity, along with standardized symmetrical output characteristics. It has a typical propagation delay of 60 ns at $V_{DD} = 10$ V and a capacitive load of 50 pF. The CD4025B is designed for low power consumption, offering a maximum input leakage current of 1 μA at 18 V and 100 nA at room temperature. It also provides robust noise margins (1 V at 5 V, 2 V at 10 V, and 2.5 V at 15 V supplies). Packaged in various 14-lead formats including DIP, SOIC, and TSSOP, it complies with JEDEC standards and is ideal for systems requiring reliable NOR logic functions under higher voltage conditions.

Table 4.1: Truth Table for 3-input NOR Gate (CD4025B)

A	B	C	Y = NOR(A, B, C)
0	0	0	1
X	X	1	0
X	1	X	0
1	X	X	0

4.1.1 Pin Diagram

The figure shows the physical representation of the CD4025B IC, indicating the arrangement of its pins. It includes input pins, an output pin, a power supply pin, and a ground pin. The pin diagram is essential for correctly integrating the IC into a circuit, ensuring proper connections and functionality in digital applications.

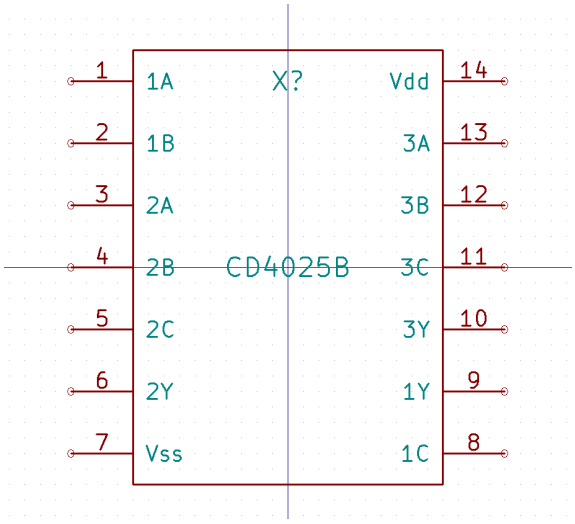

Figure 4.1: Pin layout of CD4025B

4.1.2 SubCircuit Layout

The figure represents the internal design of the CD4025B IC, showing how logic gates and components are interconnected within the chip. This layout determines how the IC processes input signals to generate the required output. Understanding the sub-circuit helps in optimizing circuit performance and ensuring efficient logic operation.

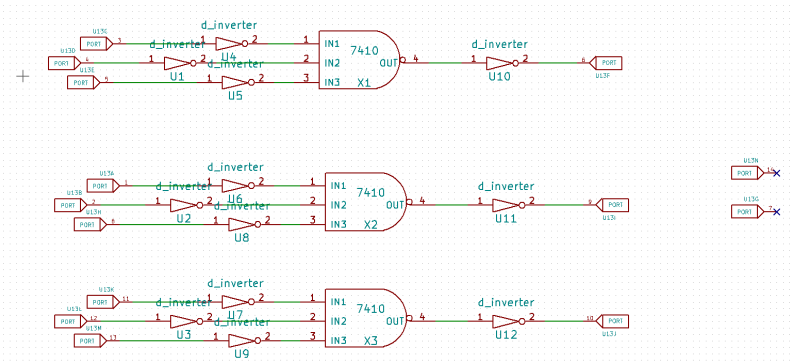

Figure 4.2: Sub Circuit of CD4025B

4.1.3 Test Circuit

The figure illustrates a test setup used to verify the performance of the CD4025B IC. A test circuit includes a power source, input signal generators, and output monitoring devices such as oscilloscopes or logic analyzers. This setup helps evaluate response time, signal integrity, and overall functionality under different conditions.

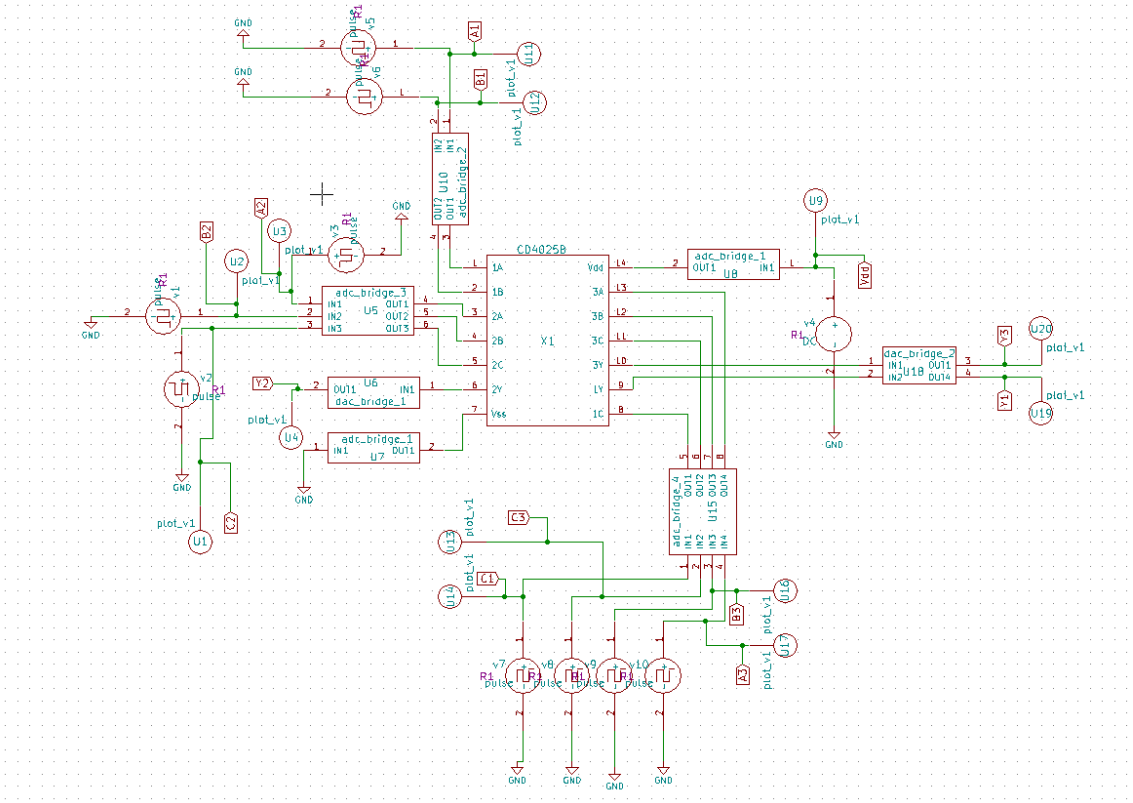

Figure 4.3: Test Circuit of CD4025B

4.1.4 Output Waveforms

The figure shows the signal produced at the output pin of the CD4025B IC after processing the input signals. This waveform represents the NOR logic operation performed by the IC.

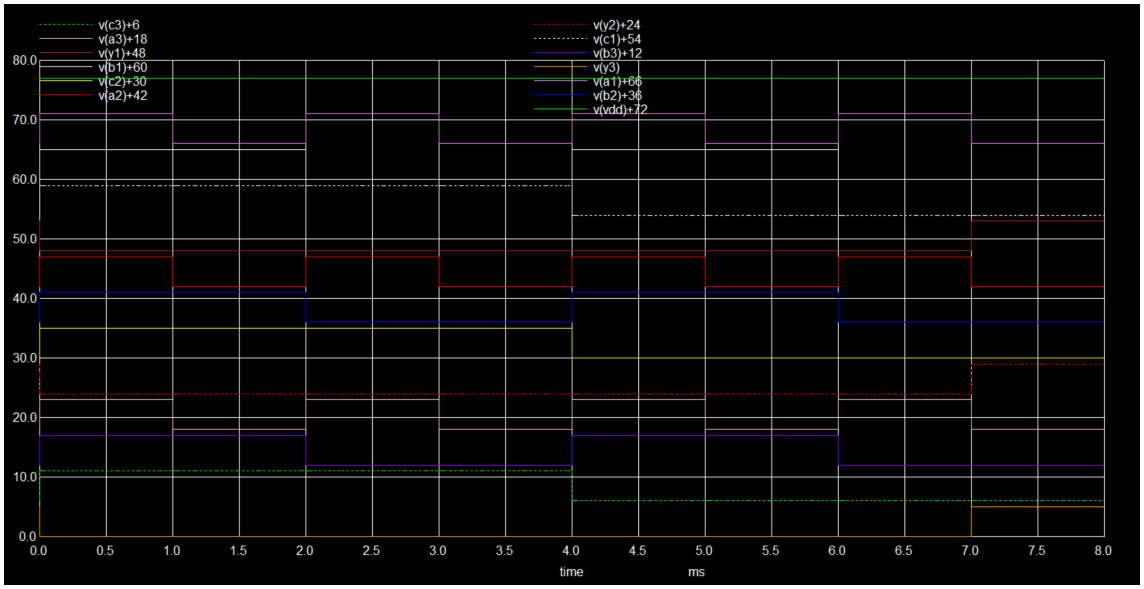

Figure 4.4: Output Waveform of CD4025B

4.2 SN74AS10

The SN74AS10 is a high-speed TTL logic IC from Texas Instruments that contains three independent 3-input positive-NAND gates. Each gate performs the Boolean function $Y = \neg(A \cdot B \cdot C)$, meaning the output is LOW only when all three inputs are HIGH, and HIGH for all other input combinations. This device is commonly used in digital systems for implementing logic control, gating, and timing functions. It operates within the commercial temperature range of 0 °C to 70 °C, while the military-grade variant, SN54AS10, supports a wider range of –55 °C to 125 °C. The IC is available in several package types, including 14-pin Dual-In-Line (DIP), Small-Outline (SOIC), and ceramic chip carriers, making it suitable for both standard and high-reliability environments. With buffered TTL outputs, it ensures signal integrity in high-speed logic operations. The SN74AS10 is ideal for applications requiring reliable NAND logic operations in embedded systems, industrial electronics, and processor interfacing.

A	B	C	Y = NAND(A, B, C)
H	H	H	L
L	X	X	H
X	L	X	H
X	X	L	H

Table 4.2: Truth Table for 3-input NAND Gate (SN74AS10)

4.2.1 Pin Diagram

The figure shows the physical representation of the SN74AS10 IC, indicating the arrangement of its pins.

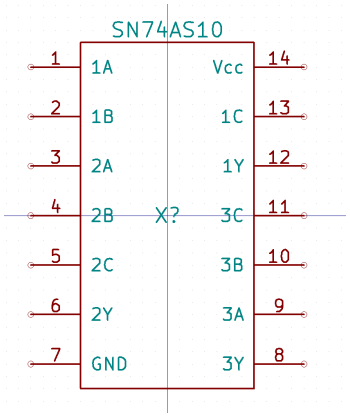

Figure 4.5: Pin layout of SN74AS10

It includes input pins, an output pin, a power supply pin, and a ground pin. The pin diagram is essential for correctly integrating the IC into a circuit, ensuring proper connections and functionality in digital applications.

4.2.2 SubCircuit Layout

The figure represents the internal design of the SN74AS10 IC, showing how logic gates and components are interconnected within the chip. This layout determines how the IC processes input signals to generate the required output. Understanding the sub-circuit helps in optimizing circuit performance and ensuring efficient logic operation.

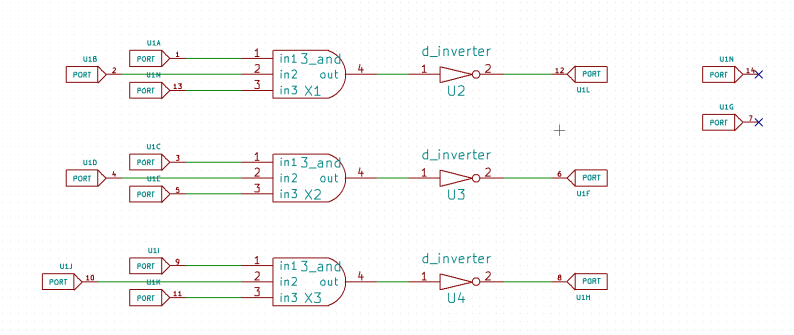

Figure 4.6: Sub Circuit of SN75AS10

4.2.3 Test Circuit

The figure illustrates a test setup used to verify the performance of the SN74AS10 IC. A test circuit includes a power source, input signal generators, and output monitoring devices such as oscilloscopes or logic analyzers. This setup helps evaluate response time, signal integrity, and overall functionality under different conditions.

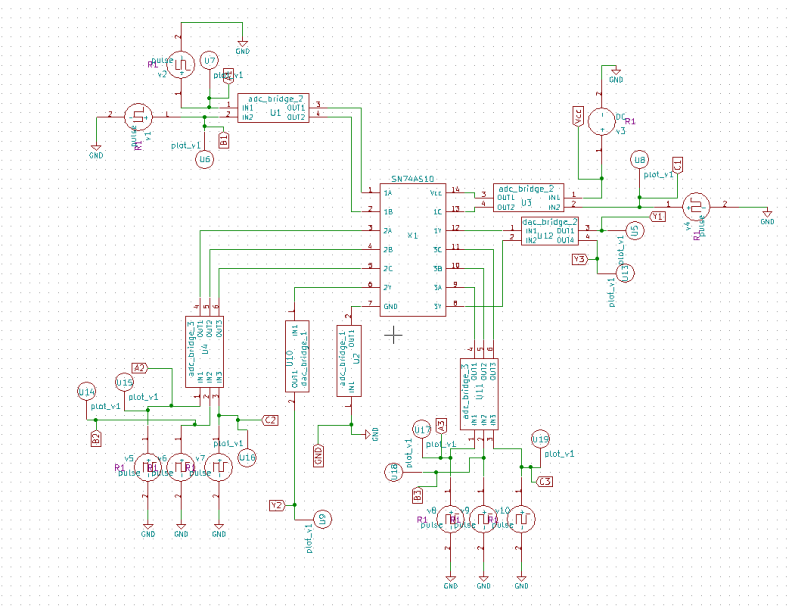

Figure 4.7: Test Circuit of SN74AS10

4.2.4 Output Waveforms

The figure shows the signal produced at the output pin of the SN74AS10 IC after processing the input signals. This waveform represents the NAND logic operation performed by the IC.

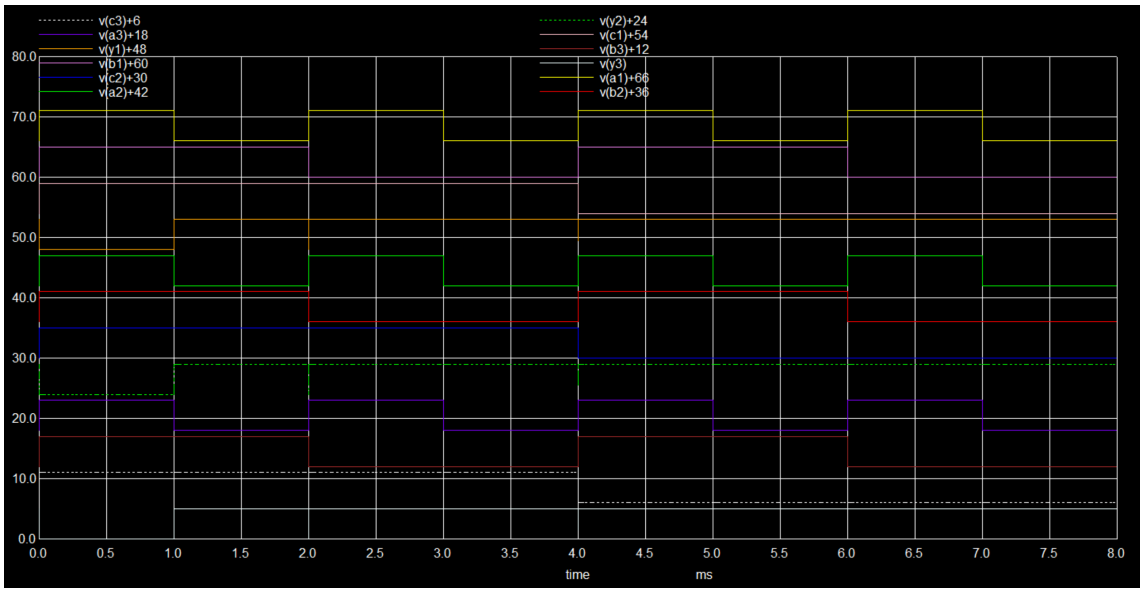

Figure 4.8: Output Waveform of SN74AS10

4.3 CD74HC4002

The CD74HC4002 is a high-speed CMOS digital logic IC that contains two independent 4-input NOR gates. It belongs to the HC (High-Speed CMOS) family and is designed to provide performance comparable to LSTTL logic with significantly lower power consumption. Each gate performs the Boolean function $Y = \sim (A+B+C+D)$, meaning the output is LOW only when any one or more of the inputs are HIGH, and HIGH only when all inputs are LOW. The IC offers a typical propagation delay of 8 ns at $V_{CC} = 5\,\text{V}$, and it supports a wide voltage range from 2 V to 6 V, with high noise immunity. It is compatible with standard LS logic in terms of functionality and pin configuration and can drive up to 10 LSTTL loads. The CD74HC4002 is available in multiple 14-pin packages, including SOIC, PDIP, TSSOP, and CDIP, making it suitable for a variety of commercial and industrial digital applications.

Table 4.3: Truth Table for 4-input NOR Gate (CD74HC4002)

A	B	C	D	Y = NOR(A, B, C, D)
0	0	0	0	1
X	X	X	1	0
X	X	1	X	0
X	1	X	X	0
1	X	X	X	0

4.3.1 Pin Diagram

The figure shows the physical representation of the CD74HC4002 IC, indicating the arrangement of its pins. It includes input pins, an output pin, a power supply pin, and a ground pin. The pin diagram is essential for correctly integrating the IC into a circuit, ensuring proper connections and functionality in digital applications.

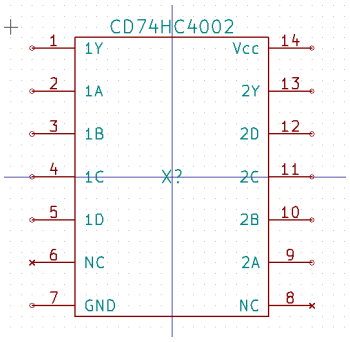

Figure 4.9: Pin layout of CD74HC4002

4.3.2 SubCircuit Layout

The figure represents the internal design of the CD74HC4002 IC, showing how logic gates and components are interconnected within the chip. This layout determines

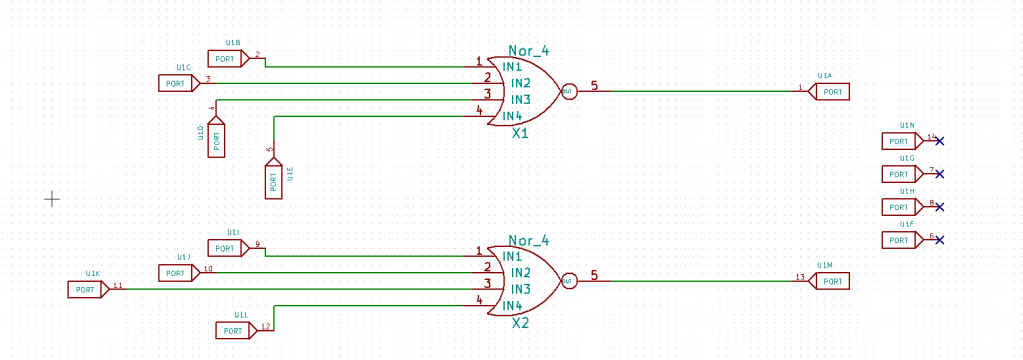

Figure 4.10: Sub Circuit of CD74HC4002

how the IC processes input signals to generate the required output. Understanding

the sub-circuit helps in optimizing circuit performance and ensuring efficient logic operation.

4.3.3 Test Circuit

The figure illustrates a test setup used to verify the performance of the CD74HC4002 IC. A test circuit includes a power source, input signal generators, and output monitoring devices such as oscilloscopes or logic analyzers. This setup helps evaluate response time, signal integrity, and overall functionality under different conditions.

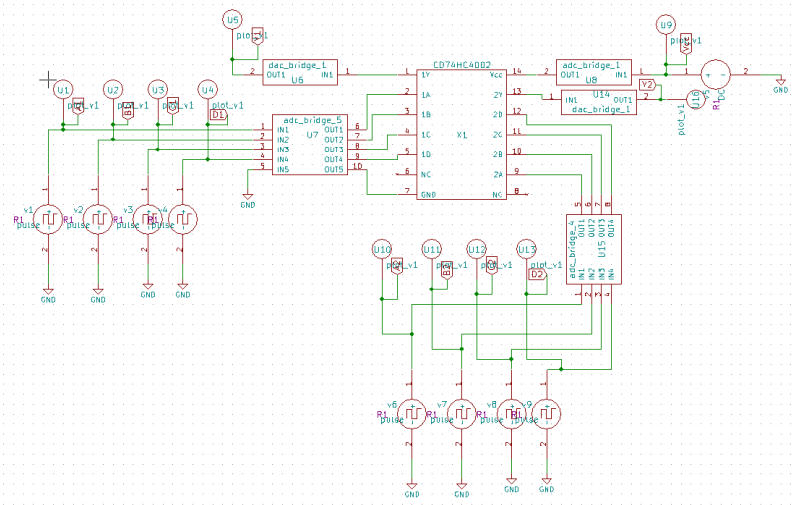

Figure 4.11: Test Circuit of CD74HC4002

4.3.4 Output Waveforms

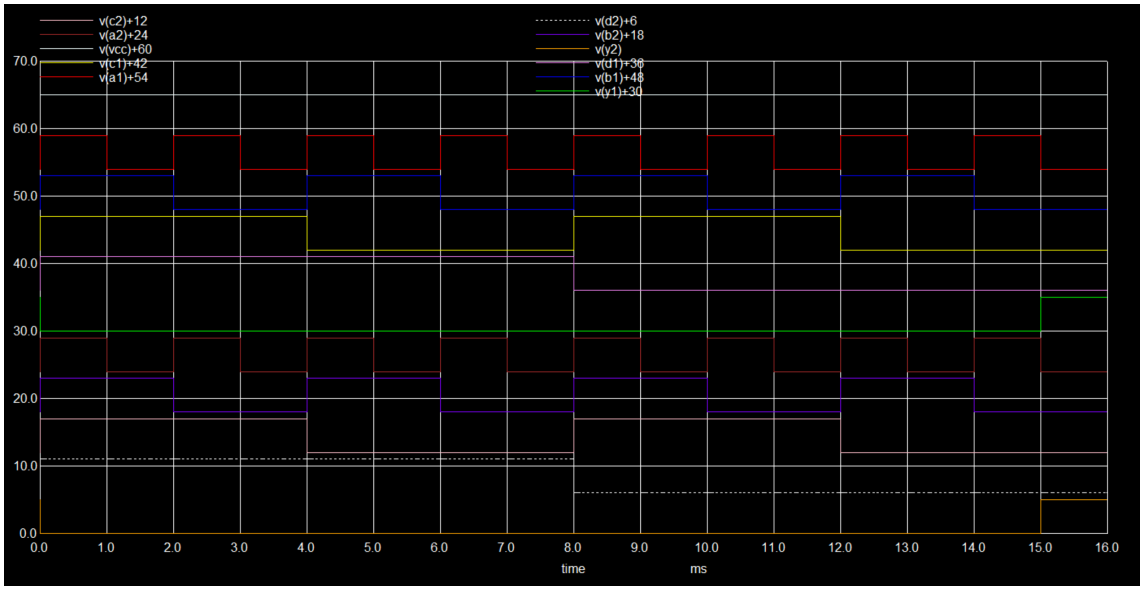

Figure 4.12: Output Waveform of CD74HC4002

The figure shows the signal produced at the output pin of the CD74HC4002 IC after processing the input signals. This waveform represents the NOR logic operation performed by the IC.

4.4 CD4012B

The CD4012B is a CMOS digital logic IC from Texas Instruments that contains two independent 4-input NAND gates. It belongs to the high-voltage CD4000 series, capable of operating across a wide voltage range of 3 V to 18 V, and features buffered inputs and outputs for enhanced signal integrity. Each NAND gate implements the Boolean logic function $Y = \neg(A \cdot B \cdot C \cdot D)$, meaning the output is HIGH for all input combinations except when all four inputs are HIGH, in which case the output becomes LOW. The device offers a typical propagation delay of 60 ns at $V_{DD} = 10\,\text{V}$ and $C_L = 50\,\text{pF}$, and supports symmetrical output characteristics and high noise immunity. It is especially suitable for low-power applications due to its CMOS technology, while still maintaining compatibility with TTL logic levels. The CD4012B is available in various 14-pin packages including DIP, SOIC, and TSSOP, making it suitable for both prototyping and production in digital control, signal gating, and logic-level interfacing applications.

Table 4.4: Truth Table for 4-input NAND Gate (CD4012B)

A	B	C	D	Y = NAND(A, B, C, D)
X	X	X	0	1
X	X	0	X	1
X	0	X	X	1
0	X	X	X	1
1	1	1	1	0

4.4.1 Pin Diagram

The figure shows the physical representation of the CD4012B IC, indicating the arrangement of its pins. It includes input pins, an output pin, a power supply pin, and a ground pin. The pin diagram is essential for correctly integrating the IC into a circuit, ensuring proper connections and functionality in digital applications.

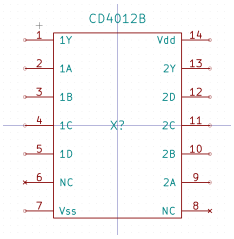

Figure 4.13: Pin layout of CD4012B

4.4.2 SubCircuit Layout

The figure represents the internal design of the CD4012B IC, showing how logic gates and components are interconnected within the chip. This layout determines

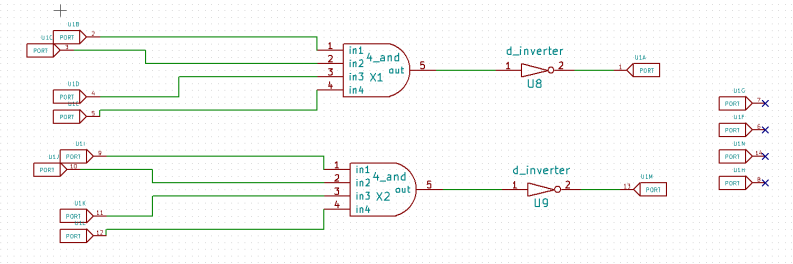

Figure 4.14: Sub Circuit of CD4012B

how the IC processes input signals to generate the required output. Understanding the sub-circuit helps in optimizing circuit performance and ensuring efficient logic operation.

4.4.3 Test Circuit

The figure illustrates a test setup used to verify the performance of the CD4012B IC. A test circuit includes a power source, input signal generators, and output monitoring devices such as oscilloscopes or logic analyzers. This setup helps evaluate response time, signal integrity, and overall functionality under different conditions.

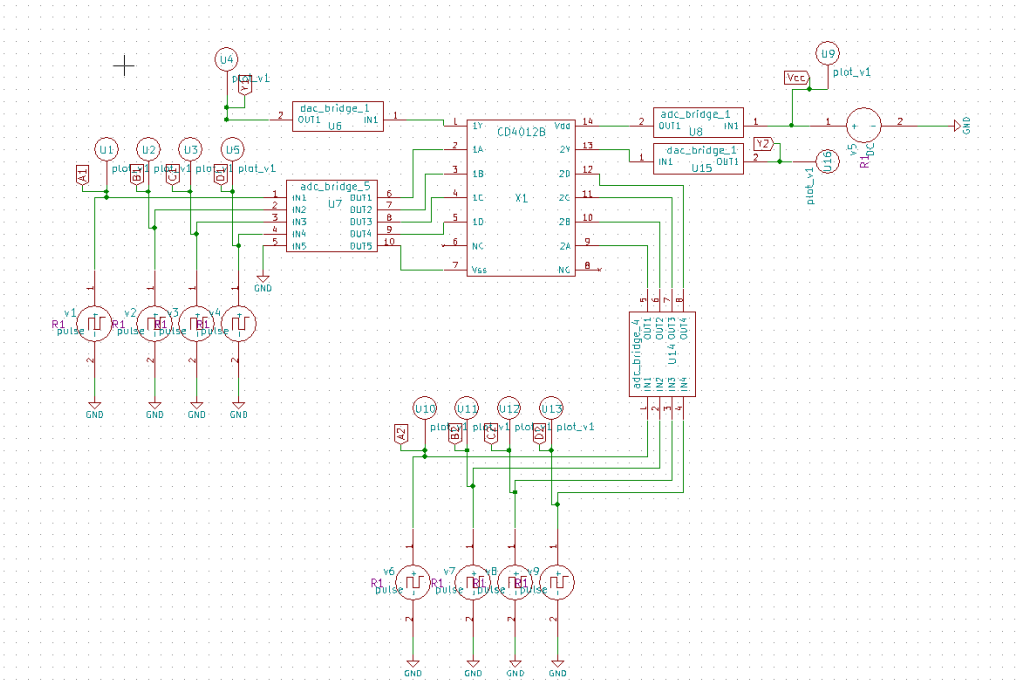

Figure 4.15: Test Circuit of CD4012B

4.4.4 Output Waveforms

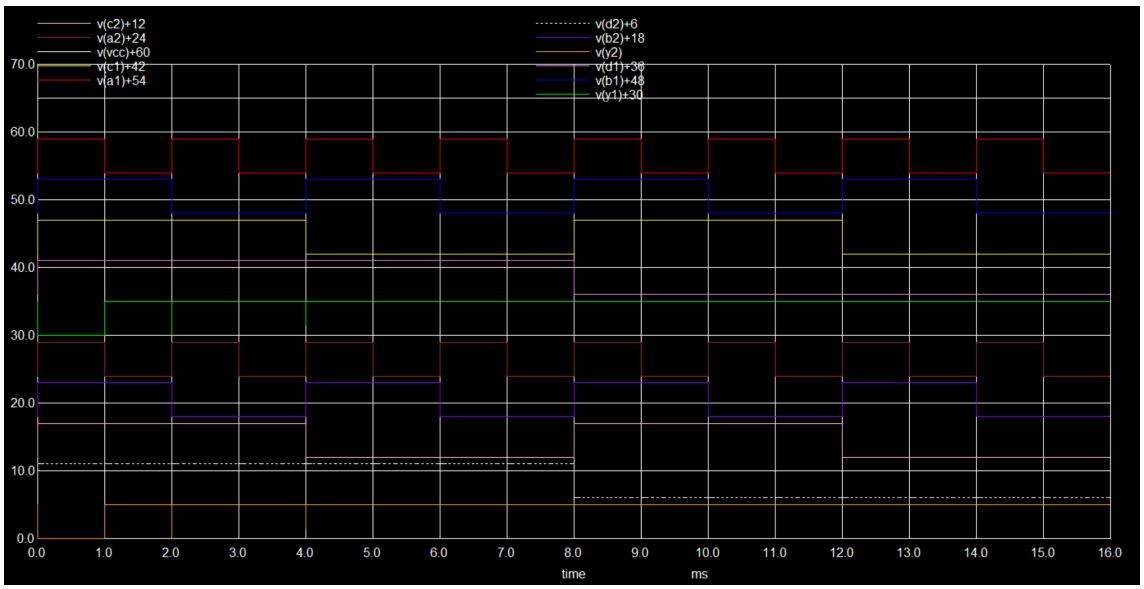

Figure 4.16: Output Waveform of CD4012B

The figure shows the signal produced at the output pin of the CD4012B IC after processing the input signals. This waveform represents the NAND logic operation performed by the IC.

4.5 CD74HC238

The CD74HC238 is a high-speed CMOS 3-to-8 line decoder/demultiplexer from Texas Instruments that features inverting outputs. It takes three binary select inputs (A0, A1, A2) and three enable inputs—one active HIGH (G2) and two active LOW (G1 and G0)—to select one of eight active LOW outputs (Y0–Y7). Only one output line is LOW at a time, depending on the binary input combination, while all others remain HIGH, making it ideal for address decoding, data routing, and memory chip selection. When any of the strobe inputs (enable lines) are not properly activated (i.e., G2 is LOW or G1/G0 are HIGH), all outputs stay HIGH, effectively disabling the decoder. The device operates over a wide supply range of 2 V to 6 V, offers low power consumption compared to LSTTL equivalents, and supports fast switching speeds. It is available in multiple 16-pin packages including PDIP, SOIC, and TSSOP, and is pin-compatible with LS logic families, making it a versatile choice for modern digital logic systems.

Table 4.5: Truth Table for 3-to-8 Decoder (CD74HC238)

G1	G0	G2	A2	A1	A0	Selected Output	Y Output
1	X	X	X	X	X	None	All HIGH
X	1	X	X	X	X	None	All HIGH
X	X	0	X	X	X	None	All HIGH
0	0	1	0	0	0	Y0	LOW
0	0	1	0	0	1	Y1	LOW
0	0	1	0	1	0	Y2	LOW
0	0	1	0	1	1	Y3	LOW
0	0	1	1	0	0	Y4	LOW
0	0	1	1	0	1	Y5	LOW
0	0	1	1	1	0	Y6	LOW
0	0	1	1	1	1	Y7	LOW

4.5.1 Pin Diagram

The figure shows the physical representation of the CD74HC238 IC, indicating the arrangement of its pins. It includes input pins, an output pin, a power supply pin, and a ground pin. The pin diagram is essential for correctly integrating the IC into a circuit, ensuring proper connections and functionality in digital applications.

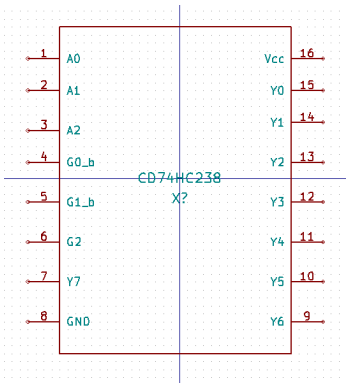

Figure 4.17: Pin layout of CD74HC238

4.5.2 SubCircuit Layout

The figure represents the internal design of the CD74HC238 IC, showing how logic gates and components are interconnected within the chip. This layout determines how the IC processes input signals to generate the required output. Understanding the sub-circuit helps in optimizing circuit performance and ensuring efficient logic operation.

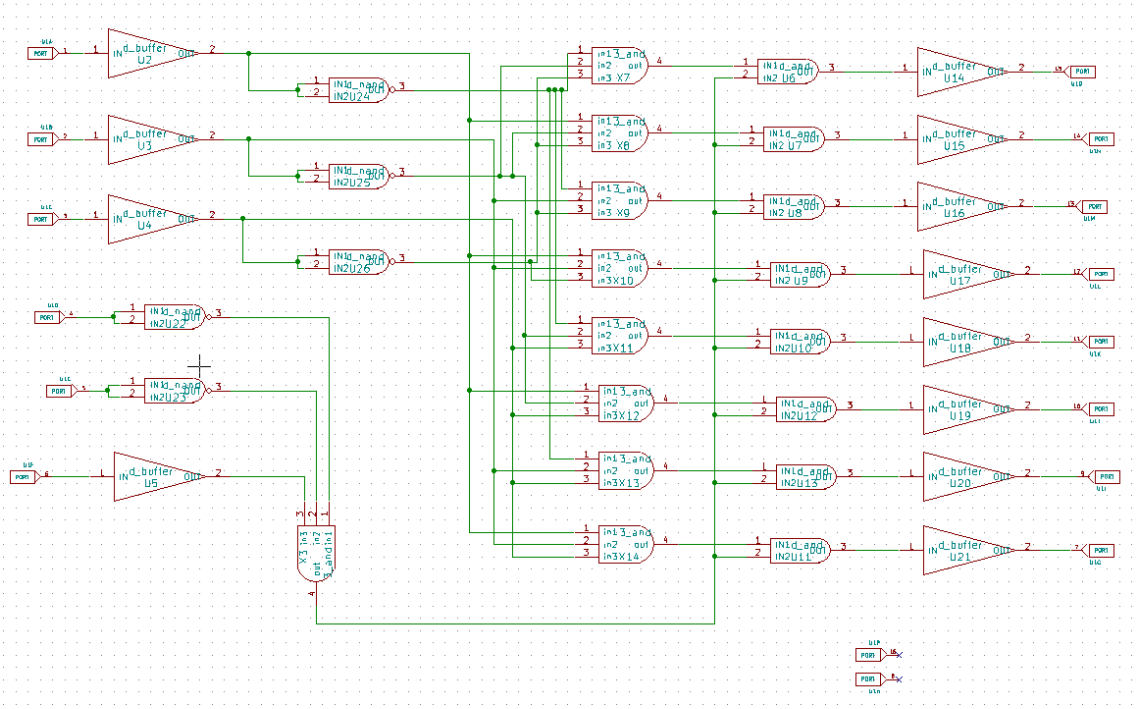

Figure 4.18: Sub Circuit of CD74HC238

4.5.3 Test Circuit

The figure illustrates a test setup used to verify the performance of the CD74HC238 IC. A test circuit includes a power source, input signal generators, and output monitoring devices such as oscilloscopes or logic analyzers. This setup helps evaluate response time, signal integrity, and overall functionality under different conditions.

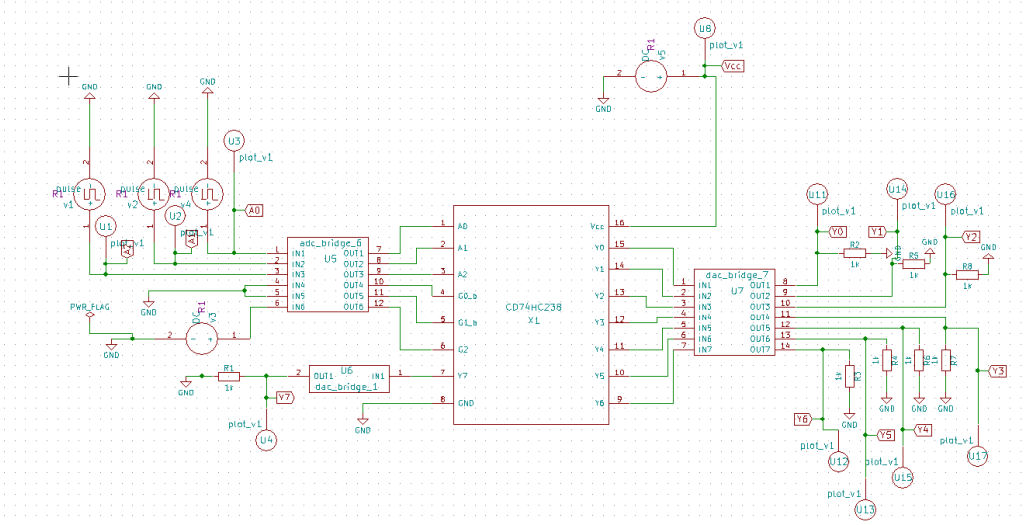

Figure 4.19: Test Circuit of CD74HC238

4.5.4 Output Waveforms

The figure shows the signal produced at the output pin of the CD74HC238 IC after processing the input signals. This waveform represents the decoding operation performed by the IC.

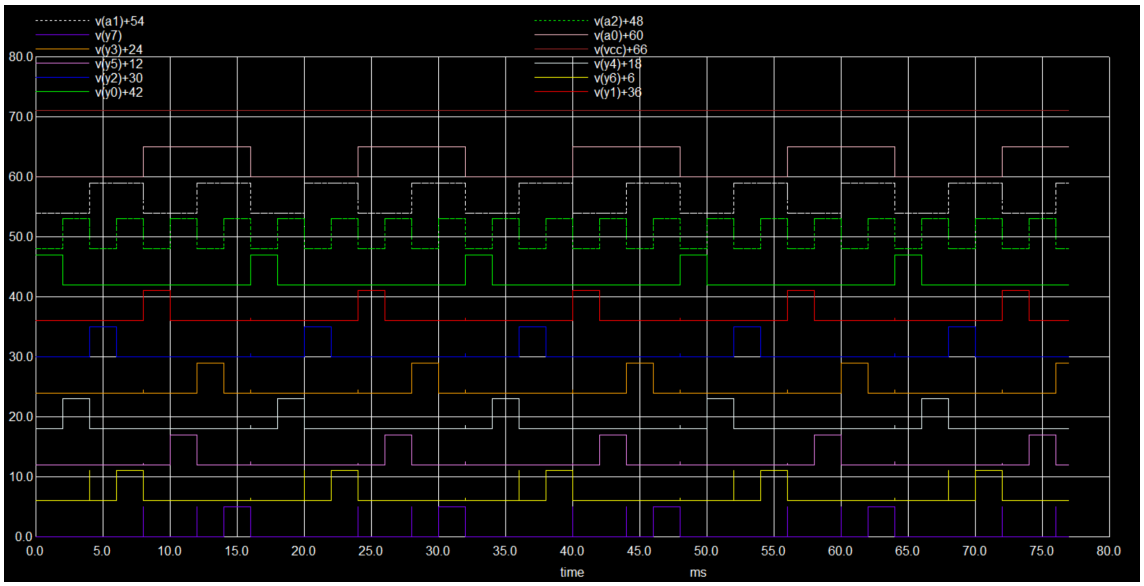

Figure 4.20: Output Waveform of CD74HC238

4.6 SN74LS76A

The SN74LS76A is a dual J-K positive-edge-triggered flip-flop IC from Texas Instruments, featuring two independent flip-flops with asynchronous preset (PRE) and clear (CLR) inputs (active-low) for immediate output control. Operating within a 4.75V to 5.25V supply range, it supports clock frequencies up to 30 MHz with propagation delays of 15-20 ns. Each flip-flop includes J and K inputs for toggling, holding, or setting outputs (Q and $\overline{Q}$) on the rising clock edge, complying with TTL logic levels ($V_{IH} \geq 2\,V$, $V_{IL} \leq 0.8\,V$). With low power consumption 4-6 mA and robust output drive (8 mA sink current), it is ideal for counters, shift registers, and state machines. Available in PDIP (N) and SOIC (D) packages (though SOIC is obsolete), the IC operates in 0-70 °C (commercial) or -55 to 125°C (military, SN54LS76A). Its compact design and reliable performance make it a staple in digital logic circuits for synchronization and sequential control.

Table 4.6: Truth Table of JK-Flipflop (SN74LS76A)

PRE	CLR	CLK	J	K	Q	$\overline{Q}$	Mode
0	1	X	X	X	1	0	Preset (Set)
1	0	X	X	X	0	1	Clear (Reset)
0	0	X	X	X	1*	1*	Invalid
1	1	↑	0	0	Q_0	$\overline{Q}_0$	Hold
1	1	↑	1	0	1	0	Set
1	1	↑	0	1	0	1	Reset
1	1	↑	1	1	$\overline{Q}_0$	Q_0	Toggle
1	1	X	X	X	Q_0	$\overline{Q}_0$	No Change

4.6.1 Pin Diagram

The figure shows the physical representation of the SN74LS76A IC, indicating the arrangement of its pins. It includes input pins, an output pin, a power supply pin, and a ground pin. The pin diagram is essential for correctly integrating the IC into a circuit, ensuring proper connections and functionality in digital applications.

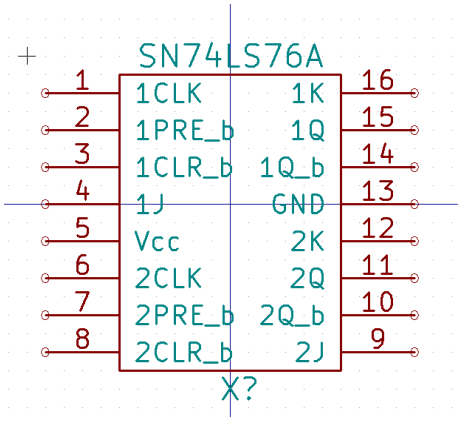

Figure 4.21: Pin layout of SN74LS76A

4.6.2 SubCircuit Layout

The figure represents the internal design of the SN74LS76A IC, showing how logic gates and components are interconnected within the chip. This layout determines how the IC processes input signals to generate the required output. Understanding the sub-circuit helps in optimizing circuit performance and ensuring efficient logic operation.

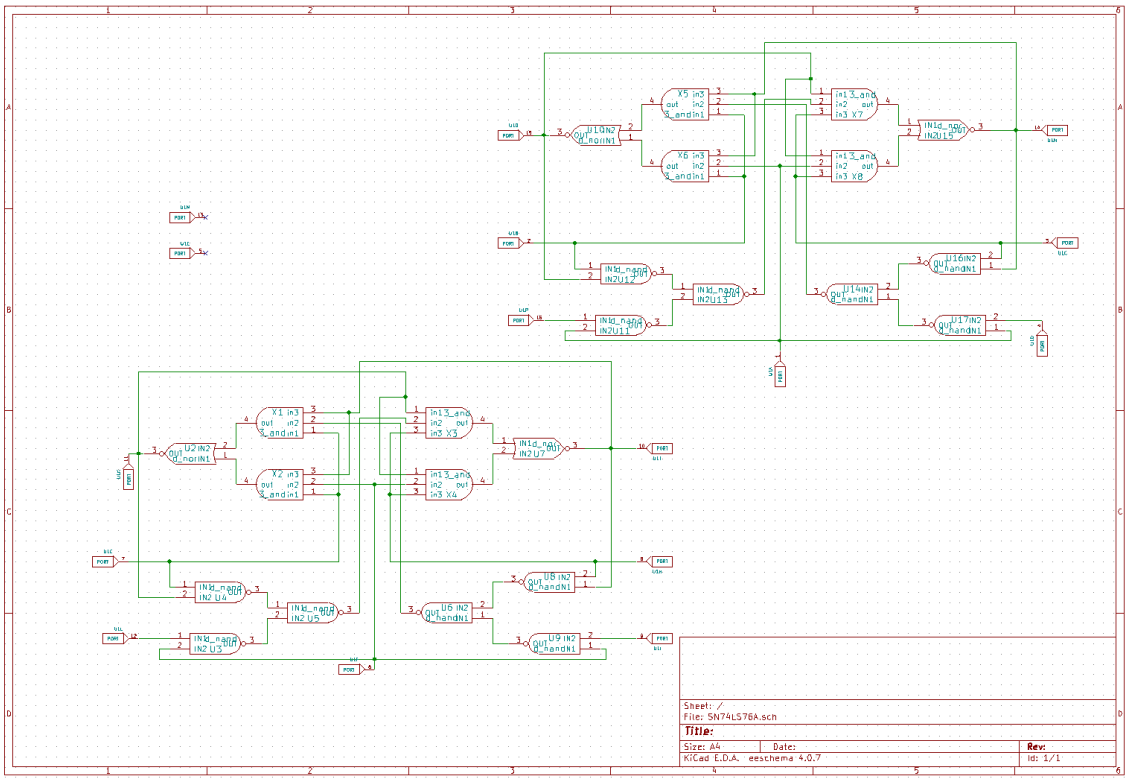

Figure 4.22: Sub Circuit of SN74LS76A

4.6.3 Test Circuit

The figure illustrates a test setup used to verify the performance of the SN74LS76A IC. A test circuit includes a power source, input signal generators, and output monitoring devices such as oscilloscopes or logic analyzers. This setup helps evaluate response time, signal integrity, and overall functionality under different conditions.

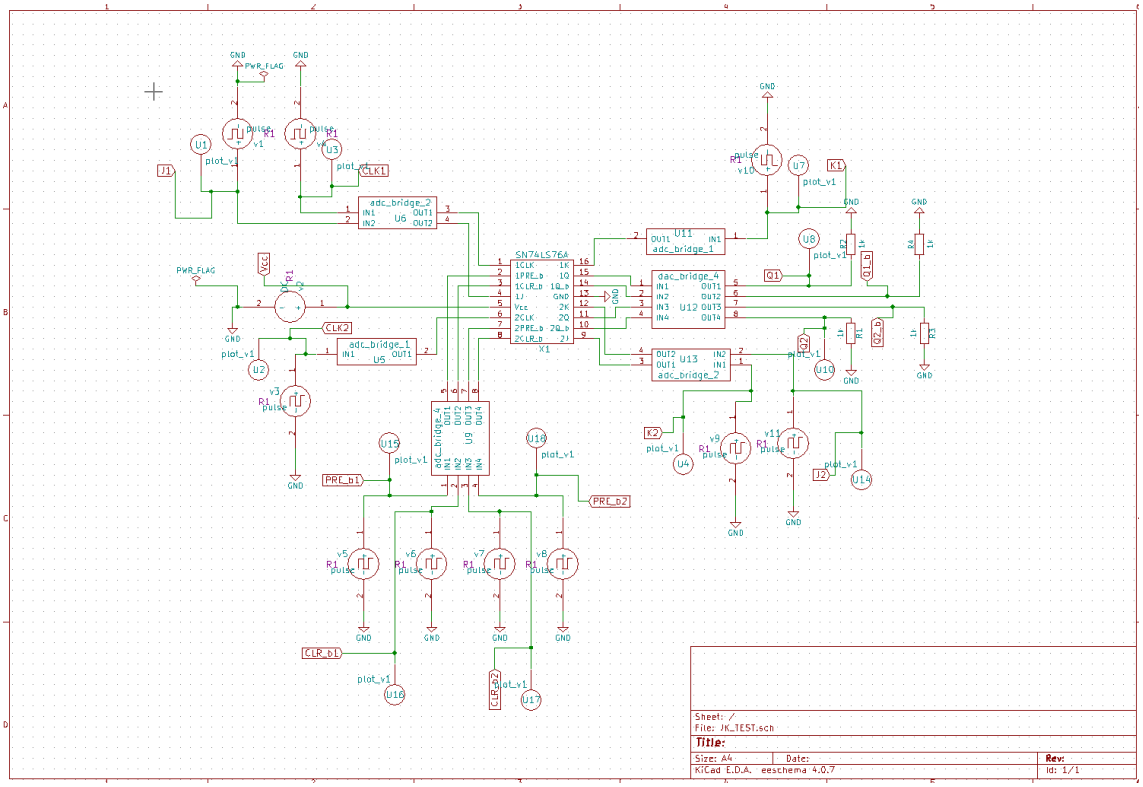

Figure 4.23: Test Circuit of SN74LS76A

4.6.4 Output Waveforms

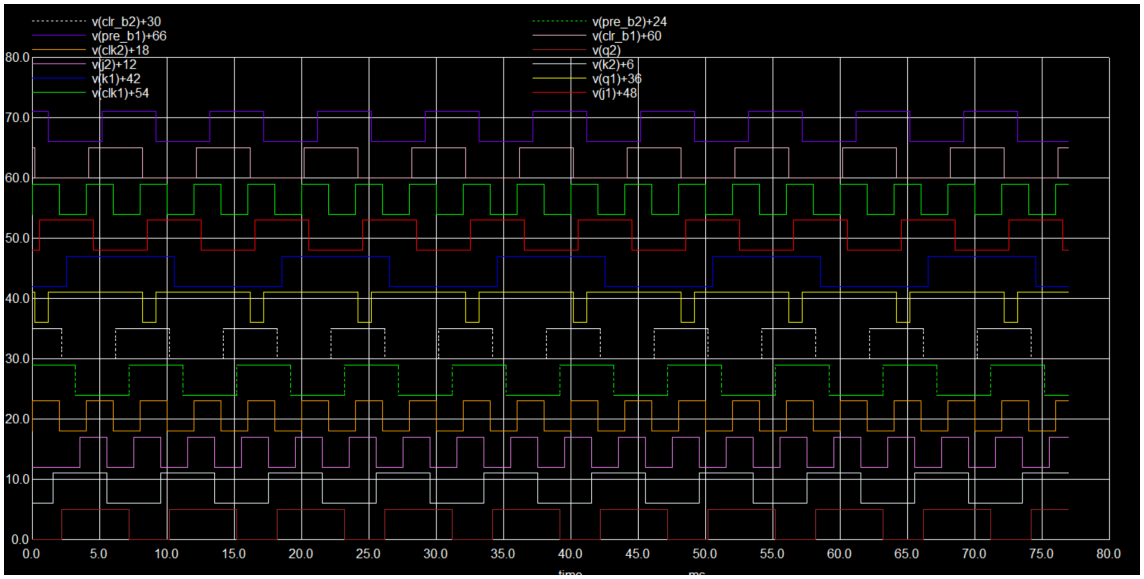

Figure 4.24: Output Waveform of SN74LS76A

The figure shows the signal produced at the output pin of the SN74LS76A IC after processing the input signals. This waveform represents the decoder operation performed by the IC.

4.7 SN74HC14

The SN74HC14 is a hex Schmitt-trigger inverter IC from Texas Instruments containing six independent inverters with hysteresis input capability, designed to transform noisy or slowly changing signals into clean digital outputs. Operating from 2–6 V, it features typical hysteresis of 0.9v (at 4.5v Vcc) with propagation delays of 15ns, making it ideal for signal conditioning, switch debouncing, and oscillator circuits. Each inverter converts input voltages below the negative threshold ($V_{T-} \approx 0.7\,\text{V}$) to high outputs, and inputs above the positive threshold ($V_{T+} \approx 1.6\,\text{V}$) to low outputs, while maintaining state between these thresholds. With low power consumption (1 µA max input current) and robust 5.2 mA output drive, it's available in PDIP-14, SOIC-14, and TSSOP-14 packages for industrial -40 to 85 °C applications.

Table 4.7: Truth Table of Schmitt Trigger (SN74HC14)

Input (A)	**Output (Y)**
$A < V_{T-}$	High (1)
$A > V_{T+}$	Low (0)
$V_{T-} < A < V_{T+}$	Previous state

4.7.1 Pin Diagram

The figure shows the physical representation of the SN74HC14 IC, indicating the arrangement of its pins. It includes input pins, an output pin, a power supply pin, and a ground pin. The pin diagram is essential for correctly integrating the IC into a circuit, ensuring proper connections and functionality in digital applications.

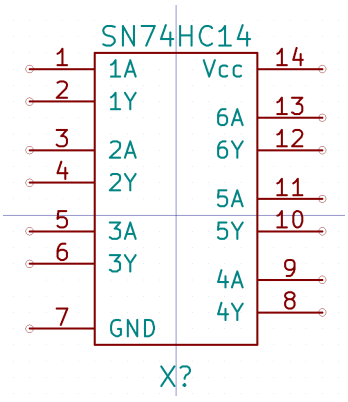

Figure 4.25: Pin layout of SN74HC14

4.7.2 SubCircuit Layout

The figure represents the internal design of the SN74HC14 IC, showing how logic gates and components are interconnected within the chip. This layout determines how the IC processes input signals to generate the required output. Understanding

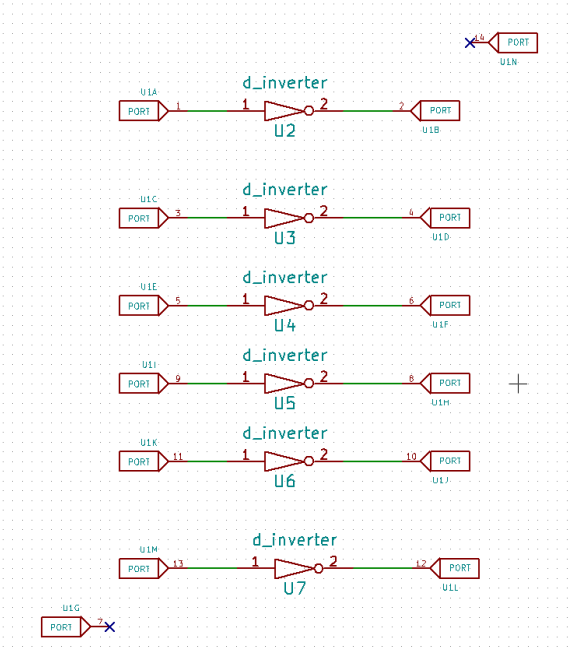

Figure 4.26: Sub Circuit of SN74HC14

the sub-circuit helps in optimizing circuit performance and ensuring efficient logic operation.

4.7.3 Test Circuit

The figure illustrates a test setup used to verify the performance of the SN74HC14 IC. A test circuit includes a power source, input signal generators, and output monitoring devices such as oscilloscopes or logic analyzers. This setup helps evaluate response time, signal integrity, and overall functionality under different conditions.

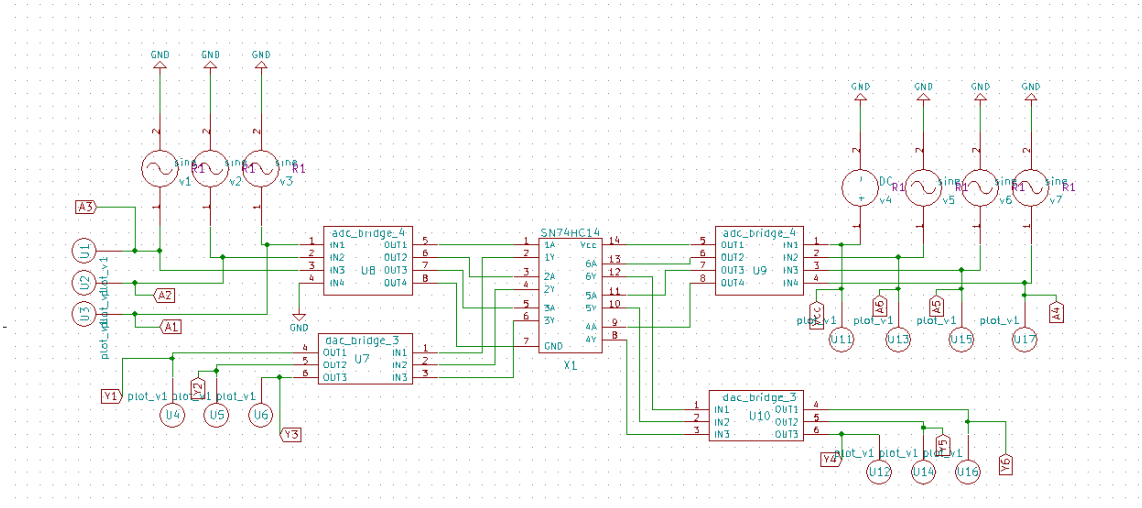

Figure 4.27: Test Circuit of SN74HC14

4.7.4 Output Waveforms

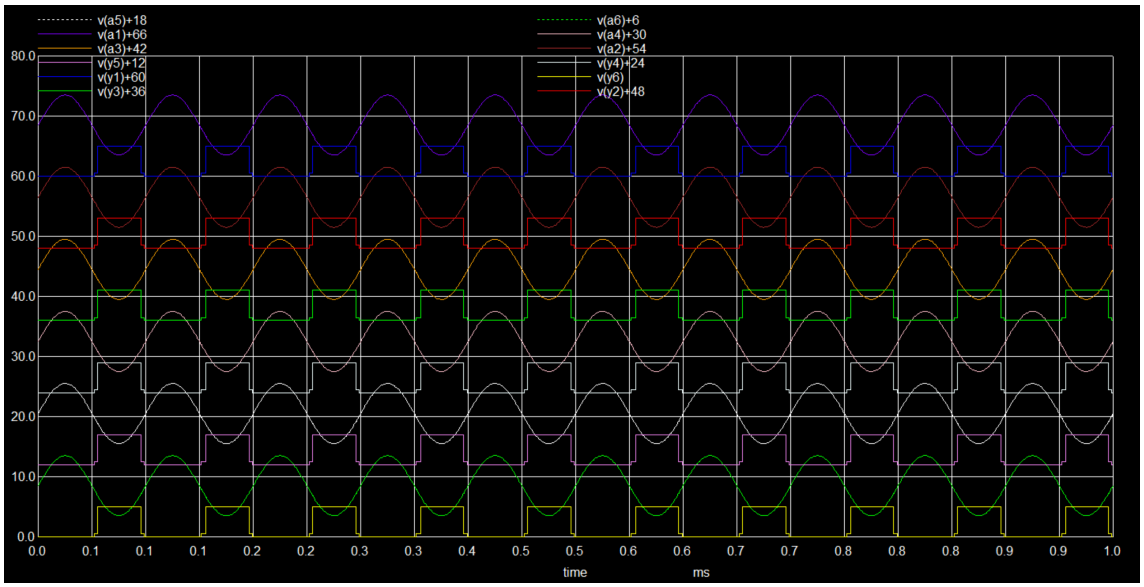

Figure 4.28: Output Waveform of SN74HC14

The figure shows the signal produced at the output pin of the SN74HC14 IC after processing the input signals. This waveform represents the Schmitt trigger operation performed by the IC.

4.8 SN54LS181

The SN54LS181/SN74LS181 is a 4-bit arithmetic logic unit (ALU) and function generator from Texas Instruments that performs 16 arithmetic operations (including addition, subtraction, and comparison) and 16 logic functions (AND, OR, XOR, etc.) on two 4-bit operands (A and B). Operating at 4.5-5.5 v, it features Schmitt-trigger inputs for noise immunity and provides outputs for carry generation (G, P, and C_{n+4}) to support multi-ALU cascading. With active-low or active-high data handling (configurable via pin designations), it executes operations based on four function-select inputs (S0–S3) and a mode-control input (M), where M=H enables logic functions and M=L enables arithmetic operations. The IC includes an open-collector A=B output for magnitude comparison and achieves propagation delays of 13-50 ns depending on operation mode. It is available in military (SN54LS181, -55 to 125 °C and commercial (SN74LS181, 0-70 °C) grades in PDIP-24, CDIP-24, and other packages.

Key:

- **Logic Symbols:** + = OR, AB = AND, $\oplus$ = XOR
- **Arithmetic:** All operations are 4-bit (e.g., A+B = arithmetic addition)
- **C$_n$**: Carry input (L=no carry, H=with carry)

Table 4.8: Truth Table of SN54LS181/SN74LS181

Select				Logic	Arithmetic Mode (M=L)	
S3	**S2**	**S1**	**S0**	**Mode (M=H)**	**C_n=L**	**C_n=H**
L	L	L	L	F = A	A - 1	A
L	L	L	H	F = AB	AB - 1	AB
L	L	H	L	F = A+B	AB - 1	AB
L	L	H	H	F = 1	-1	0
L	H	L	L	F = A+B	A+(A+B)	A+(A+B)+1
L	H	L	H	F = B	AB+(A+B)	AB+(A+B)+1
L	H	H	L	F = A⊕B	A-B-1	A-B
L	H	H	H	F = A+B	A+B	(A+B)+1
H	L	L	L	F = AB	A+(A+B)	A+(A+B)+1
H	L	L	H	F = A⊕B	A+B	A+B+1
H	L	H	L	F = B	AB+(A+B)	AB+(A+B)+1
H	L	H	H	F = A+B	(A+B)	(A+B)+1
H	H	L	L	F = 0	A+A	A+A+1
H	H	L	H	F = AB	AB+A	AB+A+1
H	H	H	L	F = AB	AB+A	AB+A+1
H	H	H	H	F = A	A	A+1

4.8.1 Pin Diagram

The figure shows the physical representation of the SN54LS181 IC, indicating the arrangement of its pins. It includes input pins, an output pin, a power supply pin, and a ground pin. The pin diagram is essential for correctly integrating the IC into a circuit, ensuring proper connections and functionality in digital applications.

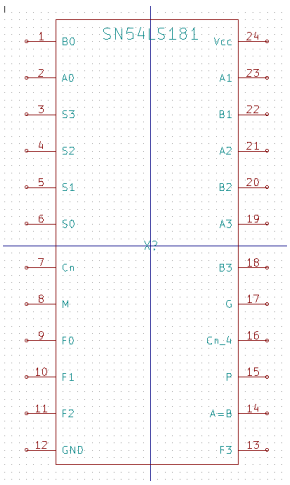

Figure 4.29: Pin layout of SN54LS181

4.8.2 SubCircuit Layout

The figure represents the internal design of the SN54LS181 IC, showing how logic gates and components are interconnected within the chip. This layout determines how the IC processes input signals to generate the required output. Understanding the sub-circuit helps in optimizing circuit performance and ensuring efficient logic operation.

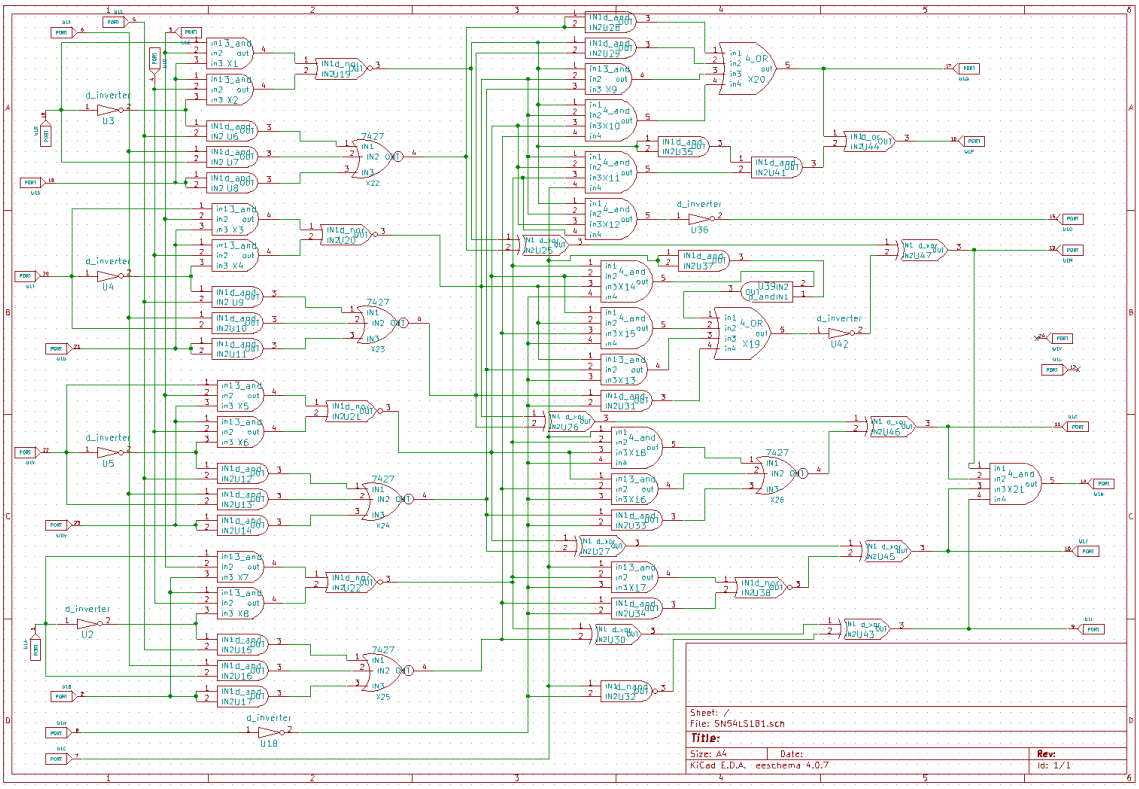

Figure 4.30: Sub Circuit of SN54LS181

4.8.3 Test Circuit

The figure illustrates a test setup used to verify the performance of the SN54LS181 IC. A test circuit includes a power source, input signal generators, and output monitoring devices such as oscilloscopes or logic analyzers. This setup helps evaluate response time, signal integrity, and overall functionality under different conditions.

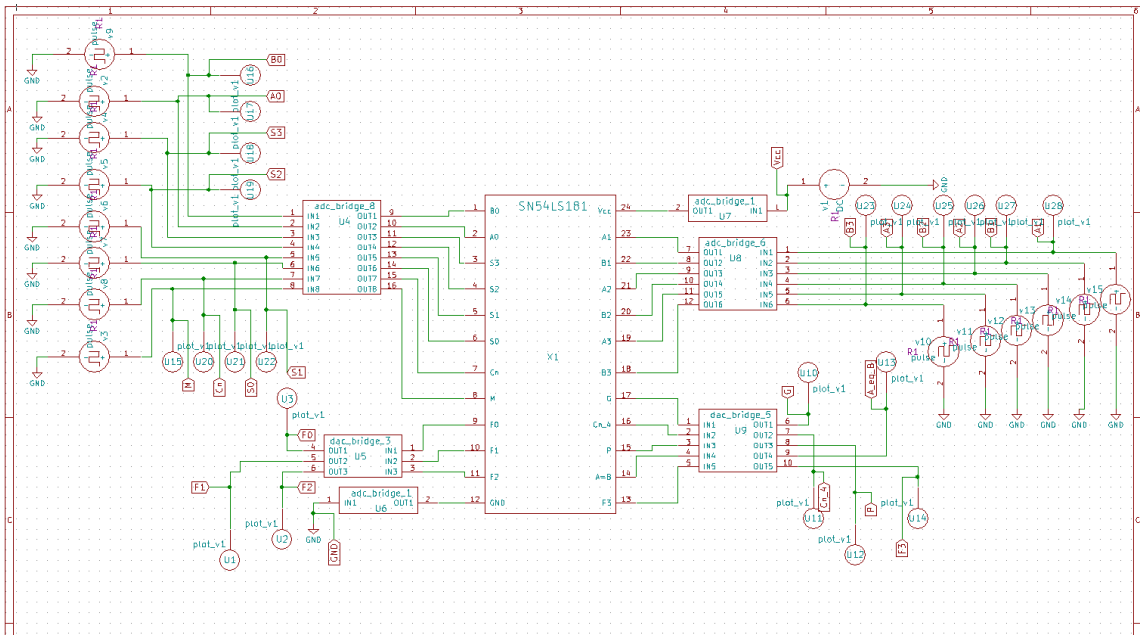

Figure 4.31: Test Circuit of SN54LS181

4.8.4 Output Waveforms

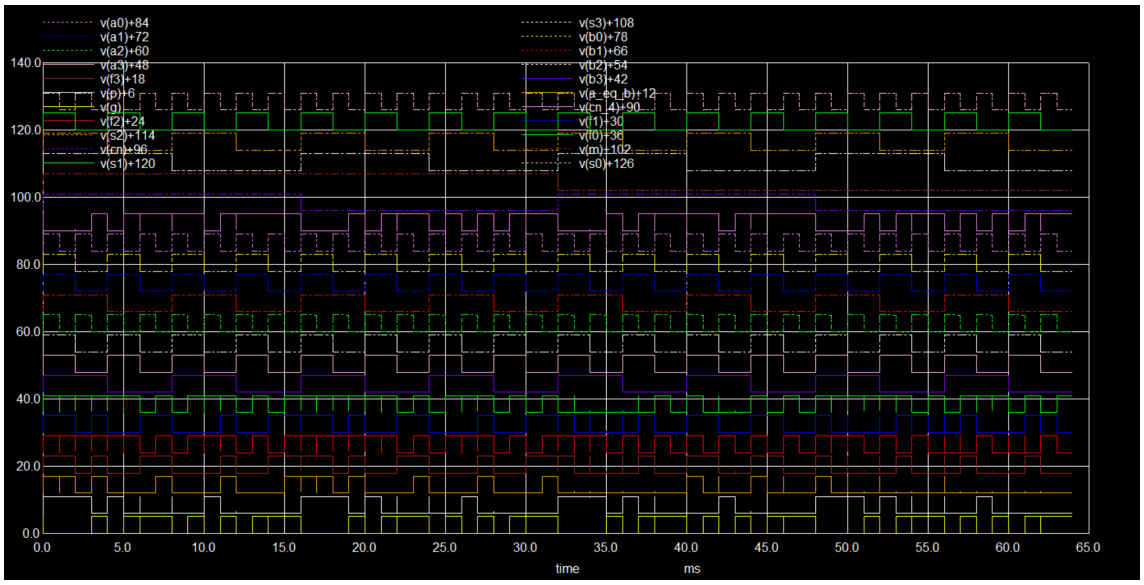

Figure 4.32: Output Waveform of SN54LS181

The figure shows the signal produced at the output pin of the SN54LS181 IC after processing the input signals. This waveform represents the ALU operation performed by the IC.

4.9 SN74ALS677A

The SN74ALS677A is a 16-bit binary counter and storage register IC from Texas Instruments. It features two separate 8-bit binary counters that can operate independently or be cascaded for extended counting operations. Each counter is edge-triggered and includes internal storage flip-flops to retain the count until latched or reset. The IC supports asynchronous master reset and synchronous enable/clock inputs, allowing for flexible control over counting and data storage processes. The SN74ALS677A is designed using Advanced Low-Power Schottky (ALS) technology, providing improved speed-power performance compared to standard TTL logic families. It operates reliably within a supply voltage range of 4.75 V to 5.25 V and is compatible with TTL-level logic inputs and outputs.

This device is especially useful in applications requiring wide counters, high-speed data acquisition, or event counting. It is well-suited for microprocessor interfacing, frequency division, and timing control systems. The SN74ALS677A is available in standard 24-pin dual in-line (DIP), small-outline (SOIC), and ceramic packages for use in both commercial and industrial systems.

4.9.1 Pin Diagram

The figure shows the physical representation of the SN74ALS677A IC, indicating the arrangement of its pins. It includes input pins, an output pin, a power supply pin, and a ground pin. The pin diagram is essential for correctly integrating the IC into a circuit, ensuring proper connections and functionality in digital applications.

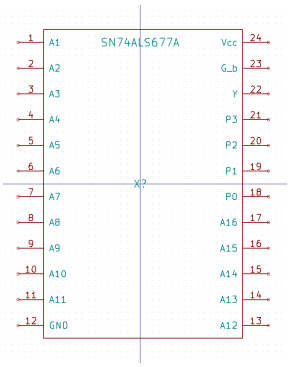

Figure 4.33: Pin layout of SN74ALS677A

4.9.2 SubCircuit Layout

The figure represents the internal design of the SN74ALS677A IC, showing how logic gates and components are interconnected within the chip. This layout determines how the IC processes input signals to generate the required output. Understanding the sub-circuit helps in optimising circuit performance and ensuring efficient logic operation.

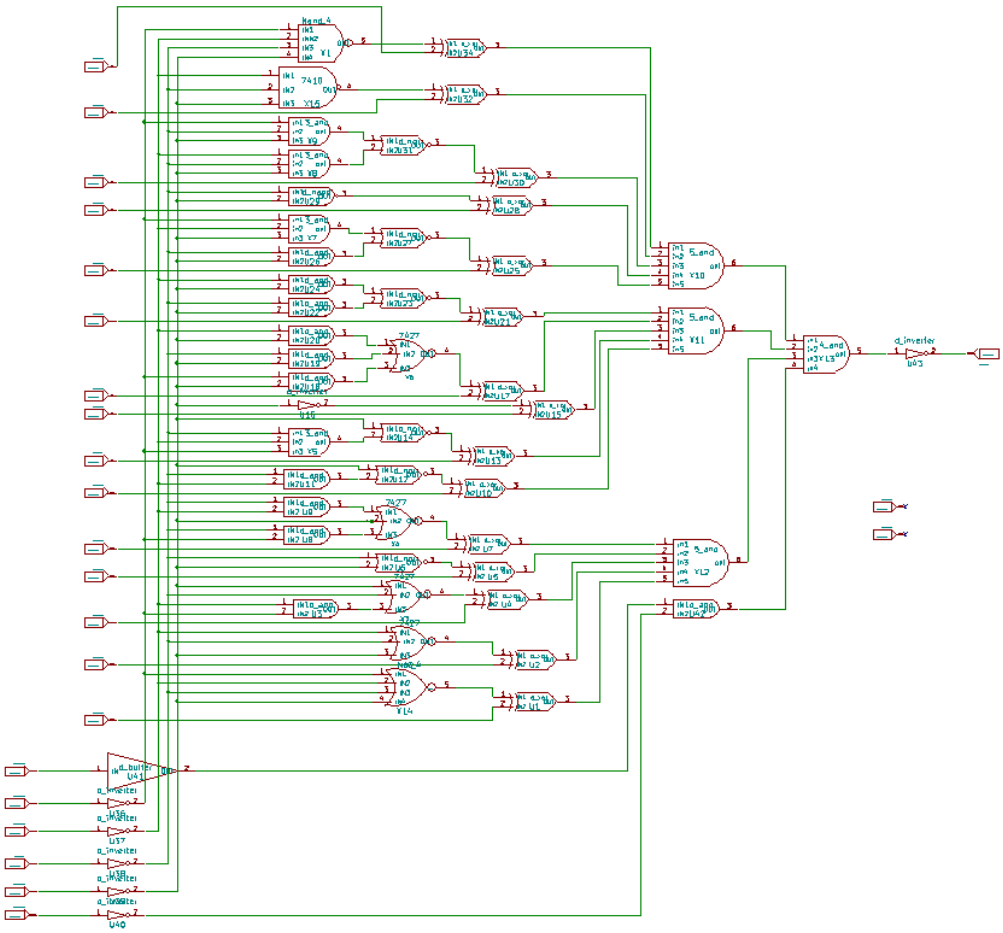

Figure 4.34: Sub Circuit of SN74ALS677A

4.9.3 Test Circuit

The figure illustrates a test setup used to verify the performance of the SN74ALS677A IC. A test circuit includes a power source, input signal generators, and output monitoring devices such as oscilloscopes or logic analyzers. This setup helps evaluate response time, signal integrity, and overall functionality under different conditions.

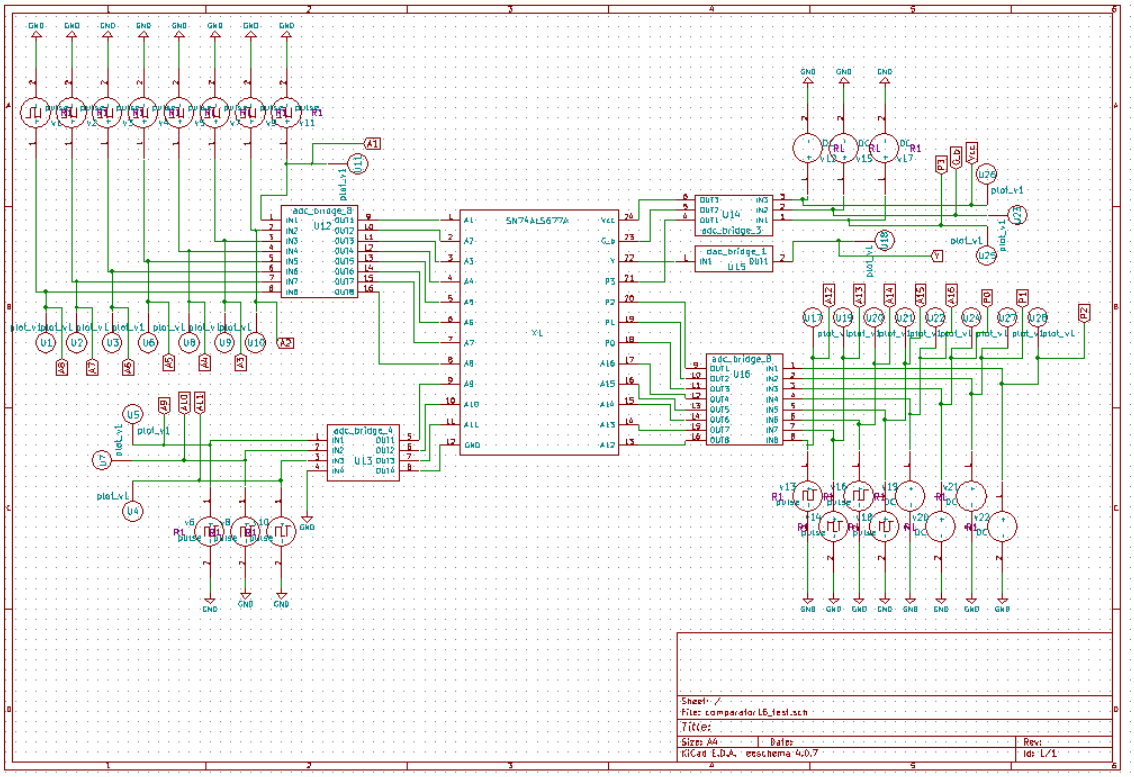

Figure 4.35: Test Circuit of SN74ALS677A

4.9.4 Output Waveforms

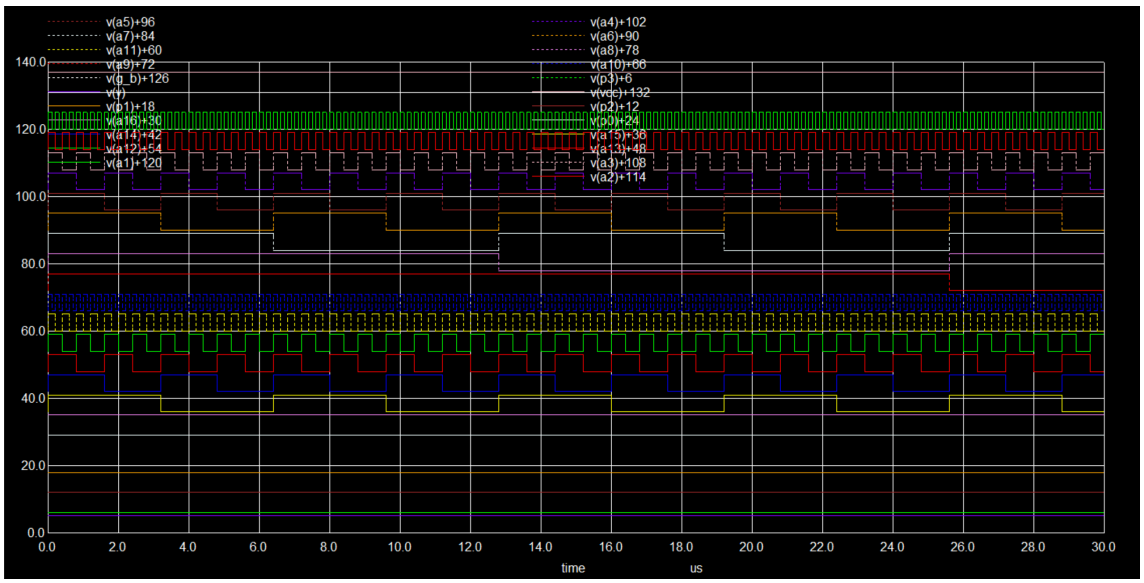

Figure 4.36: Output Waveform of SN74ALS677A

The figure shows the signal produced at the output pin of the SN74ALS677A IC after processing the input signals. This waveform represents the comparator operation performed by the IC.

4.10 SN74LS91

The SN5491A/SN74LS91 is an 8-bit serial-in/serial-out shift register IC that operates on TTL logic levels, featuring a compact design with eight R-S master-slave flip-flops, input gating, and clock control. With a typical operating frequency of 18 Mhz (guaranteed 10 Mhz) and power dissipation of just 60 mwatt for the LS version, it accepts data through its gated A and B inputs (with internal inversion) and shifts bits on positive clock edges. The IC provides complementary outputs (Q_H and $\overline{Q_H}$) after 8 clock cycles, supports cascading for extended shift operations, and operates across 4.5-5.5 v. Available in PDIP-14 and SOIC-14 packages, it offers propagation delays of 24-40 ns and functions reliably in both military (-55 to 125 °C) and commercial (0-70 °C) temperature ranges, making it ideal for data buffering, time delay circuits, and serial data processing applications.

Table 4.9: Truth Table of SN5491A/SN74LS91

A	**B**	**Clock**	**Output After 8 Clocks ($\overline{Q_H}$)**
H	H	↑	L (Loads '1')
L	X	↑	H (Loads '0')
X	L	↑	H (Loads '0')
H	L	↑	H (Loads '0')
L	H	↑	H (Loads '0')

Legend:

- ↑ = Low-to-High clock transition (positive edge)
- H = High level (logic '1')
- L = Low level (logic '0')
- X = Don't care (either H or L)

Operation:

- The output $\overline{Q_H}$ reflects the input state (A AND B) after 8 clock cycles
- When both A and B are High, a '1' is shifted in (output becomes Low)
- Any other input combination shifts in a '0' (output becomes High)

4.10.1 Pin Diagram

The figure shows the physical representation of the SN74LS91 IC, indicating the arrangement of its pins. It includes input pins, an output pin, a power supply pin, and a ground pin. The pin diagram is essential for correctly integrating the IC into a circuit, ensuring proper connections and functionality in digital applications.

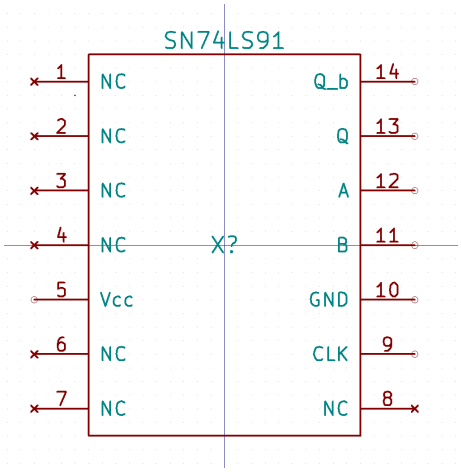

Figure 4.37: Pin layout of SN74LS91

4.10.2 SubCircuit Layout

The figure represents the internal design of the SN74LS91 IC, showing how logic gates and components are interconnected within the chip. This layout determines how the IC processes input signals to generate the required output. Understanding the sub-circuit helps in optimizing circuit performance and ensuring efficient logic operation.

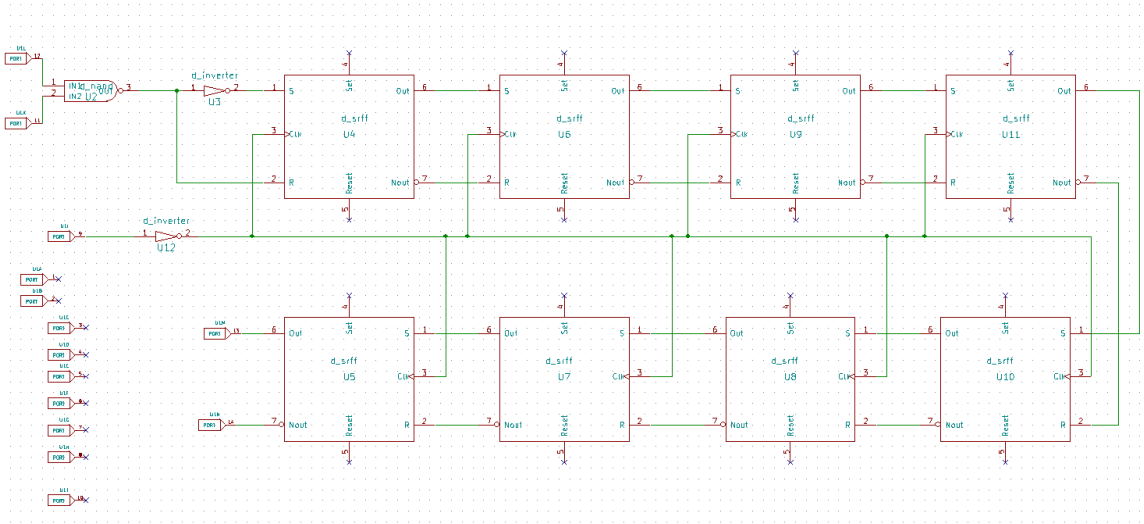

Figure 4.38: Sub Circuit of SN74LS91

4.10.3 Test Circuit

The figure illustrates a test setup used to verify the performance of the SN74LS91 IC. A test circuit includes a power source, input signal generators, and output monitoring devices such as oscilloscopes or logic analyzers. This setup helps evaluate response time, signal integrity, and overall functionality under different conditions.

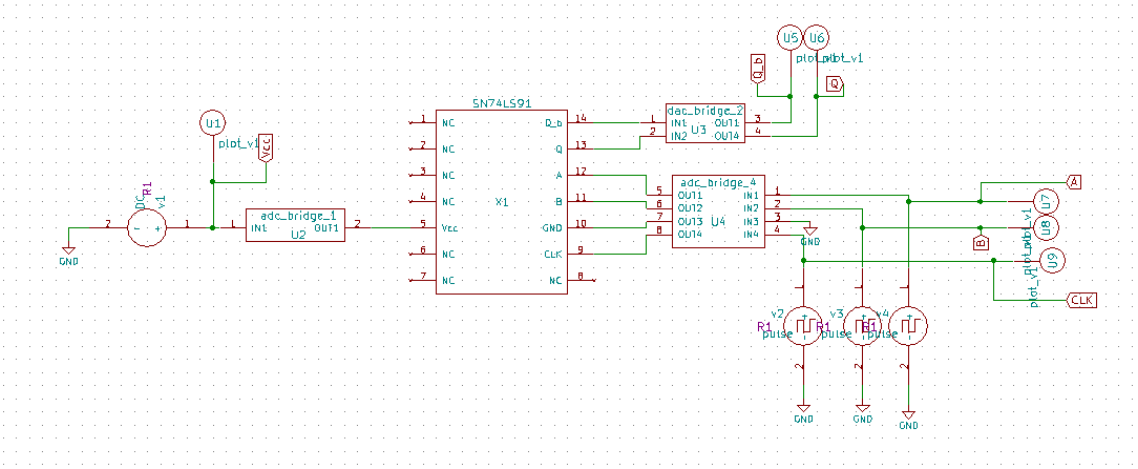

Figure 4.39: Test Circuit of SN74LS91

4.10.4 Output Waveforms

The figure shows the signal produced at the output pin of the SN74LS91 IC after processing the input signals. This waveform represents the NOR logic operation performed by the IC.

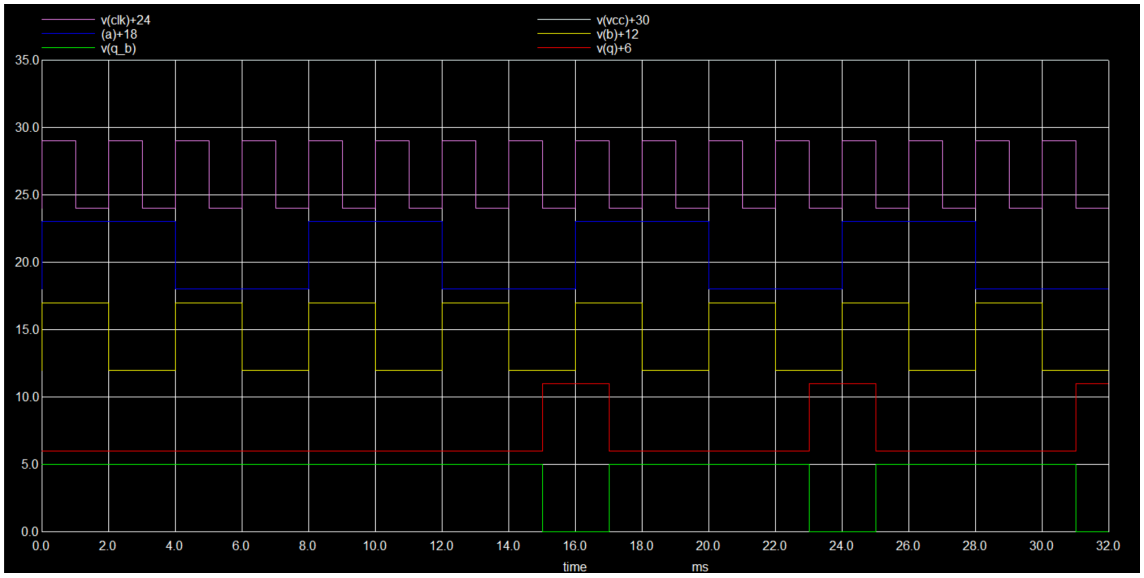

Figure 4.40: Output Waveform of SN74LS91

4.11 SN74159

The SN54159/SN74159 is a 4-line to 16-line decoder/demultiplexer IC with open-collector outputs, designed for TTL systems. It features:

- **4 binary address inputs** (A-D) selecting one of 16 active-low outputs
- **Two active-low strobe inputs** for output enable control
- **Open-collector outputs** allowing wired-AND connections
- **High-voltage capability** (upto 5.5v) with 16 mA sink current
- **Fast operation**: 36ns max propagation delay
- **Wide temperature range**: -55 to 125 °C (military) or 0-70 °C (commercial)

Operating at 4.5-5.5v, it's ideal for memory addressing, I/O expansion, and logic function generation. The open-collector outputs permit direct drive of indicators or interface with higher-voltage systems.

Table 4.10: Truth Table of SN54159/SN74159

Inputs				**Strobes**	**Output**
D	C	B	A	$\overline{G1}$ $\overline{G2}$	$\overline{Y0}$–$\overline{Y15}$
L	L	L	L	L L	$\overline{Y0}$ = L, others = H
L	L	L	H	L L	$\overline{Y1}$ = L, others = H
L	L	H	L	L L	$\overline{Y2}$ = L, others = H
L	L	H	H	L L	$\overline{Y3}$ = L, others = H
L	H	L	L	L L	$\overline{Y4}$ = L, others = H
L	H	L	H	L L	$\overline{Y5}$ = L, others = H
L	H	H	L	L L	$\overline{Y6}$ = L, others = H
L	H	H	H	L L	$\overline{Y7}$ = L, others = H
H	L	L	L	L L	$\overline{Y8}$ = L, others = H
H	L	L	H	L L	$\overline{Y9}$ = L, others = H
H	L	H	L	L L	$\overline{Y10}$ = L, others = H
H	L	H	H	L L	$\overline{Y11}$ = L, others = H
H	H	L	L	L L	$\overline{Y12}$ = L, others = H
H	H	L	H	L L	$\overline{Y13}$ = L, others = H
H	H	H	L	L L	$\overline{Y14}$ = L, others = H
H	H	H	H	L L	$\overline{Y15}$ = L, others = H
X	X	X	X	H X	All outputs = H
X	X	X	X	X H	All outputs = H

Legend:

- L = Low (0), H = High (1), X = Don't care
- $\overline{G1}$, $\overline{G2}$ = Active-low strobe inputs
- $\overline{Y0}$-$\overline{Y15}$ = Active-low outputs (only one low at a time)

4.11.1 Pin Diagram

The figure shows the physical representation of the SN74159 IC, indicating the arrangement of its pins. It includes input pins, an output pin, a power supply pin, and a ground pin. The pin diagram is essential for correctly integrating the IC into a circuit, ensuring proper connections and functionality in digital applications.

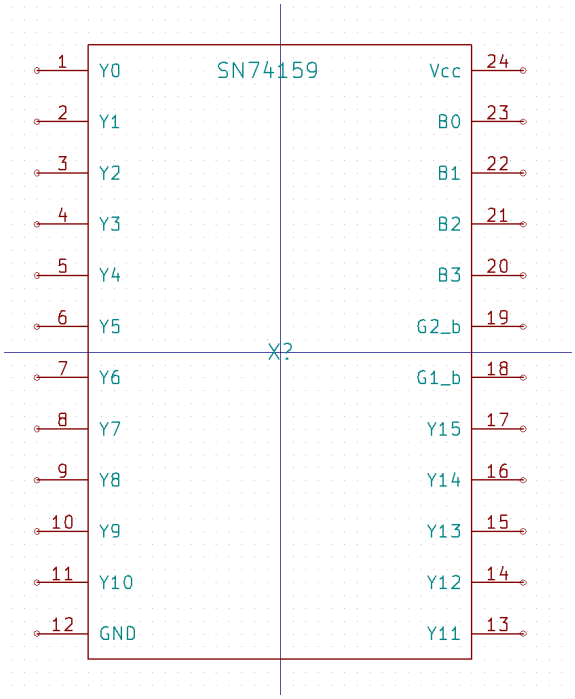

Figure 4.41: Pin layout of SN74159

4.11.2 SubCircuit Layout

The figure represents the internal design of the SN74159 IC, showing how logic gates and components are interconnected within the chip. This layout determines how the IC processes input signals to generate the required output. Understanding the sub-circuit helps in optimizing circuit performance and ensuring efficient logic operation.

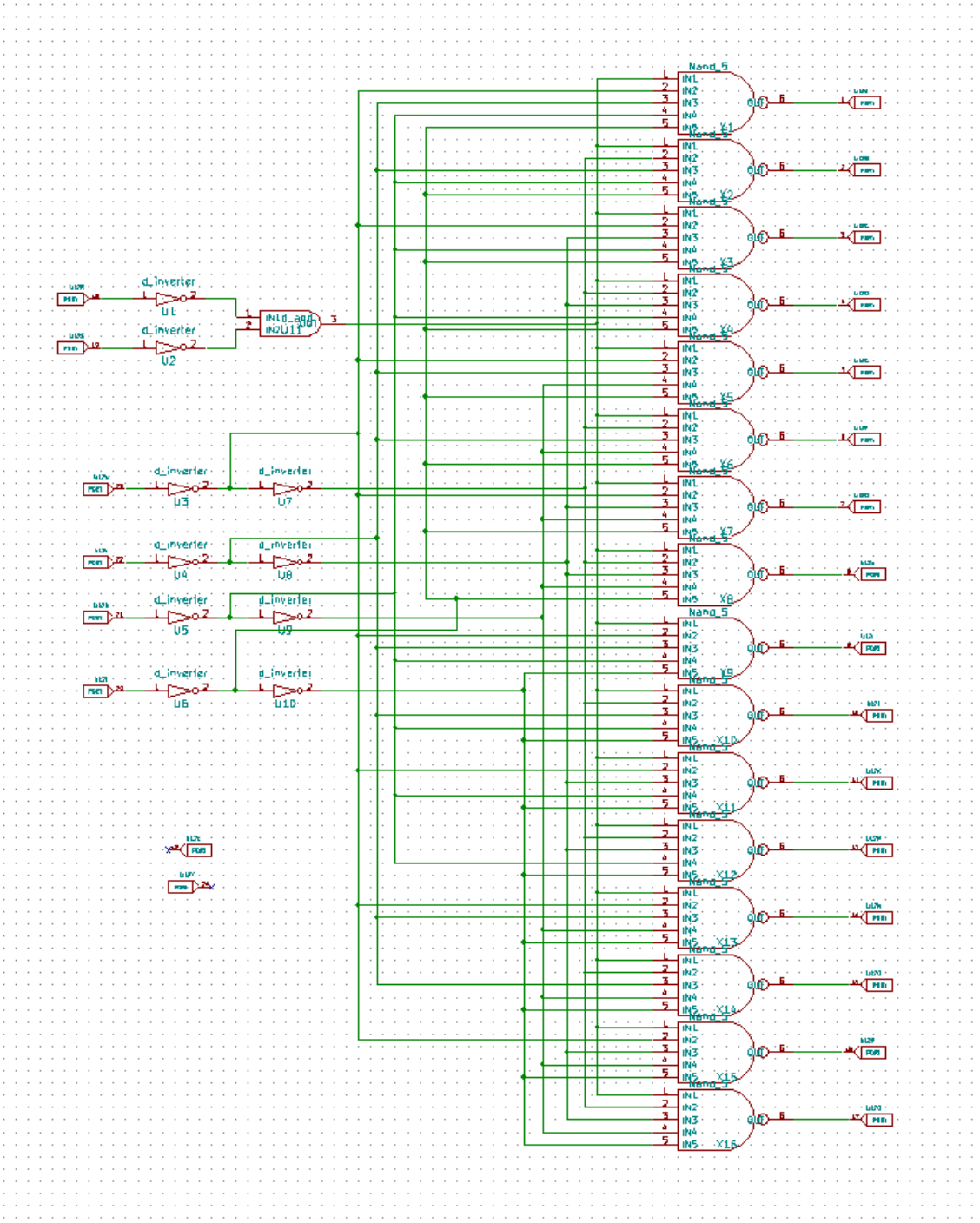

Figure 4.42: Sub Circuit of SN74159

4.11.3 Test Circuit

The figure illustrates a test setup used to verify the performance of the SN74159 IC. A test circuit includes a power source, input signal generators, and output monitoring devices such as oscilloscopes or logic analyzers. This setup helps evaluate response time, signal integrity, and overall functionality under different conditions.

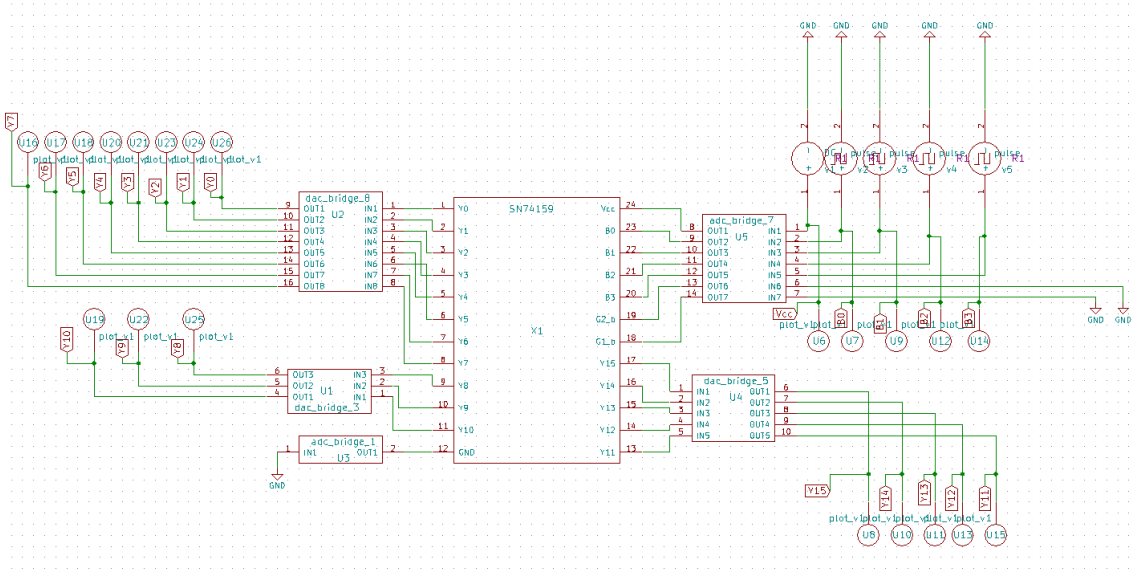

Figure 4.43: Test Circuit of SN74159

4.11.4 Output Waveforms

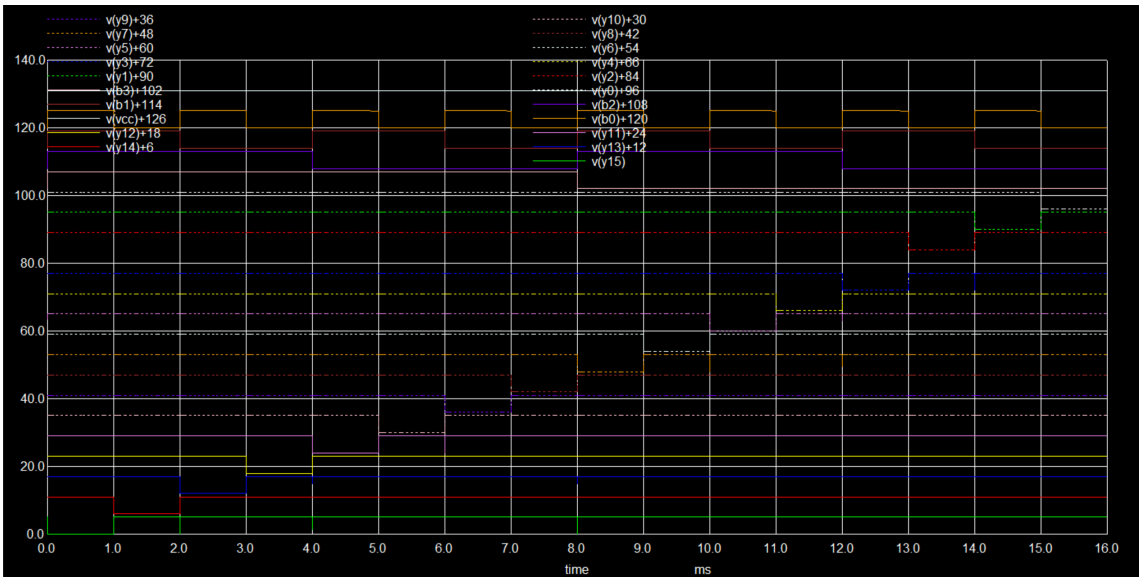

Figure 4.44: Output Waveform of SN74159

The figure shows the signal produced at the output pin of the SN74159 IC after processing the input signals. This waveform represents the 4 to 16 line decoder/demultiplexer operation performed by the IC.

4.12 SN74LS147

The SN74LS147 is a 10-line to 4-line priority encoder belonging to the 74LS TTL logic family. It accepts 10 active-low inputs (0–9) and provides a 4-bit binary code output (A, B, C, D) also in active-low format. The primary function of this IC is to encode the position of the highest-priority active-low input into a binary representation on the output. It is particularly useful in keyboard encoding, data compression, and other priority resolution applications. When more than one input is active (i.e., low), the encoder prioritizes the input with the highest numerical value, ensuring only one unique output combination at a time. The IC features built-in input buffers and exhibits typical TTL speed and power characteristics. All outputs and inputs are compatible with TTL levels. It operates over a standard voltage range of 4.75V to 5.25V. This device greatly reduces the number of lines needed to convey information and simplifies complex decision logic in digital circuits by prioritizing the most significant input.

Table 4.11: Truth Table for SN74LS147 (Active Low Inputs and Outputs)

Input	**D**	**C**	**B**	**A**	**Output Code (Decimal)**
I9 = 0	1	0	0	1	9
I8 = 0, I9 = 1	1	0	0	0	8
I7 = 0, I8–I9 = 1	0	1	1	1	7
I6 = 0, I7–I9 = 1	0	1	1	0	6
I5 = 0, I6–I9 = 1	0	1	0	1	5
I4 = 0, I5–I9 = 1	0	1	0	0	4
I3 = 0, I4–I9 = 1	0	0	1	1	3
I2 = 0, I3–I9 = 1	0	0	1	0	2
I1 = 0, I2–I9 = 1	0	0	0	1	1
I0 = 0, I1–I9 = 1	0	0	0	0	0

4.12.1 Pin Diagram

The figure shows the physical representation of the SN74LS147 IC, indicating the arrangement of its pins. It includes input pins, an output pin, a power supply pin, and a ground pin. The pin diagram is essential for correctly integrating the IC into a circuit, ensuring proper connections and functionality in digital applications.

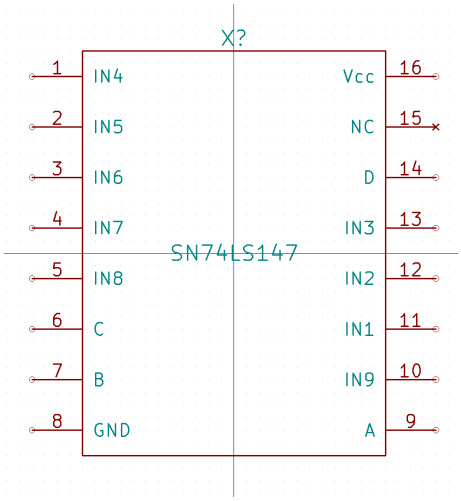

Figure 4.45: Pin layout of SN74LS147

4.12.2 SubCircuit Layout

The figure represents the internal design of the SN74LS147 IC, showing how logic gates and components are interconnected within the chip. This layout determines how the IC processes input signals to generate the required output. Understanding the sub-circuit helps in optimizing circuit performance and ensuring efficient logic operation.

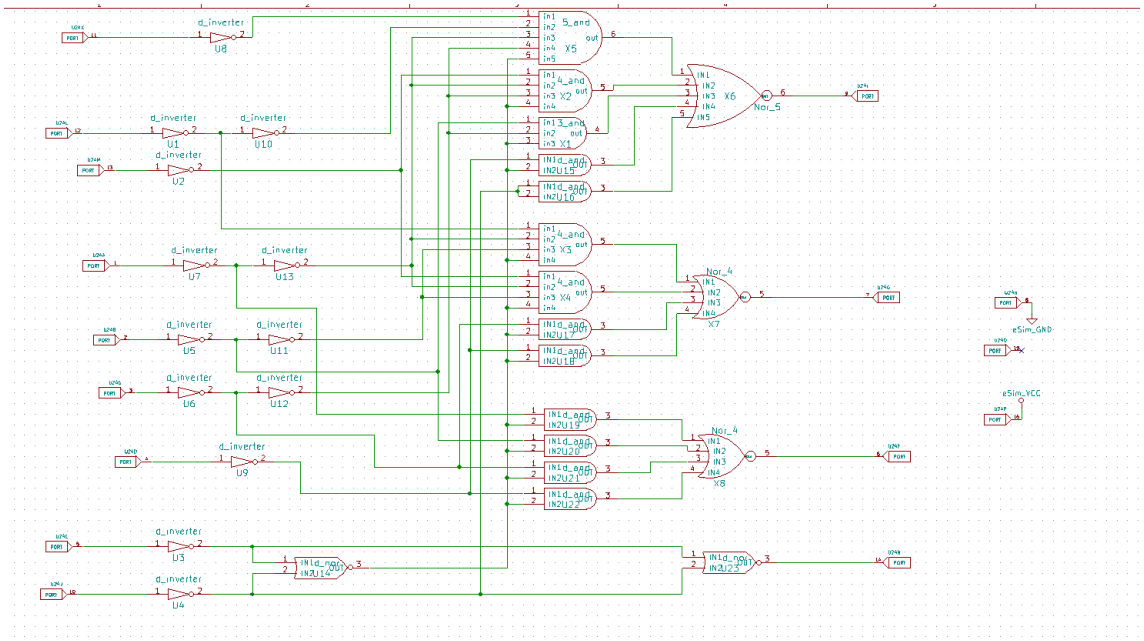

Figure 4.46: Sub Circuit of SN74LS147

4.12.3 Test Circuit

The figure illustrates a test setup used to verify the performance of the SN74LS147 IC. A test circuit includes a power source, input signal generators, and output monitoring devices such as oscilloscopes or logic analyzers. This setup helps evaluate response time, signal integrity, and overall functionality under different conditions.

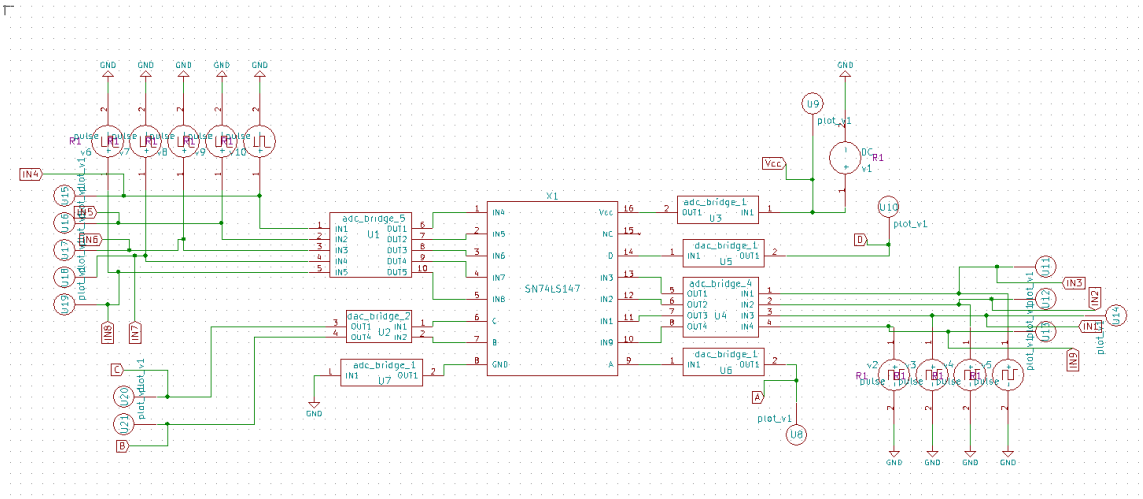

Figure 4.47: Test Circuit of SN74LS147

4.12.4 Output Waveforms

The figure shows the signal produced at the output pin of the SN74LS147 IC after processing the input signals. This waveform represents the 10 to 4 line priority encoding operation performed by the IC.

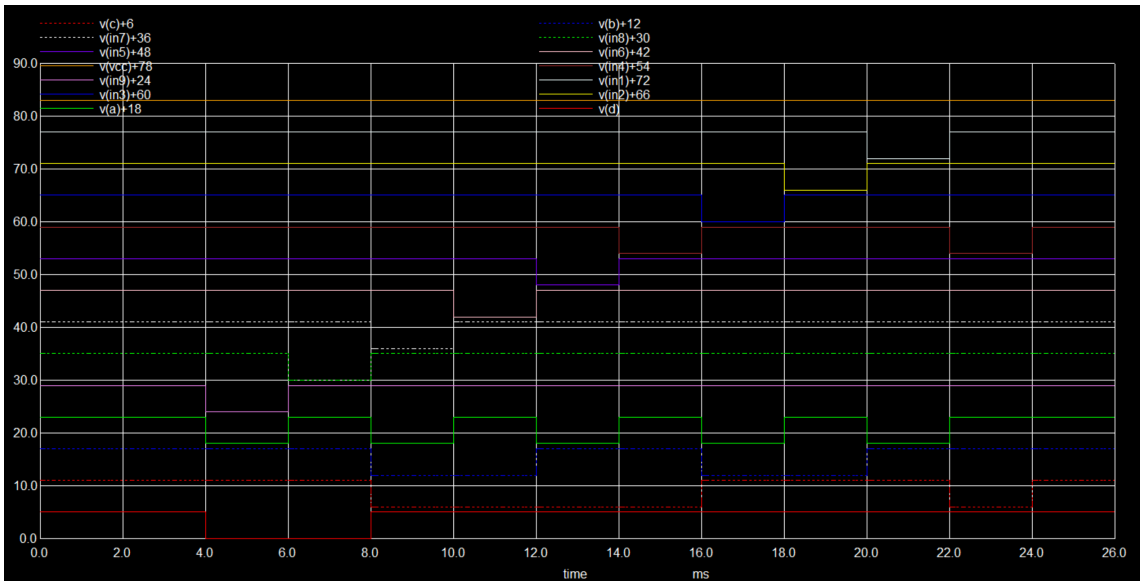

Figure 4.48: Output Waveform of SN74LS147

4.13 SN74HC4020

The SN74HC4020 is a high-speed CMOS 14-bit asynchronous binary counter. It is configured as a ripple-carry counter, where each flip-flop in the series toggles on the negative edge of the input clock signal. This device is primarily used for frequency division and time delay applications due to its predictable counting behavior and extended range of outputs. The IC features a Clock input (CLK) and an asynchronous Master Reset (CLR). When CLR is held high, all outputs are reset to logic low, regardless of the clock signal. When CLR is low, the counter advances its binary count with each negative clock transition. The outputs are available at specific divide-by stages: *Q4, Q5, Q6, Q7, Q8, Q9, Q11, Q12, Q13, Q14*, offering a range of frequency divisions from $\frac{f_{CLK}}{16}$ to $\frac{f_{CLK}}{16384}$. Operating over a wide voltage range of **2 V to 6 V**, this IC provides TTL and CMOS compatibility, with low power consumption (typically 80 µA) and fast switching speeds (12 ns typical propagation delay at 5 V). Its versatility and efficiency make it ideal for digital timing, frequency counting, and control logic applications. Truth Table:

Table 4.12: Truth Table for SN74HC4020

CLK	CLR	Function
↑	L	No Change
↓	L	Advance to Next State
X	H	Reset (All Outputs LOW)

4.13.1 Pin Diagram

The figure shows the physical representation of the SN74HC4020 IC, indicating the arrangement of its pins. It includes input pins, an output pin, a power supply pin, and a ground pin. The pin diagram is essential for correctly integrating the IC into a circuit, ensuring proper connections and functionality in digital applications.

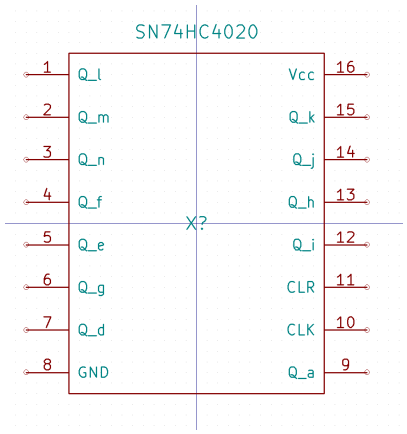

Figure 4.49: Pin layout of SN74HC4020

4.13.2 SubCircuit Layout

The figure represents the internal design of the SN74HC4020 IC, showing how logic gates and components are interconnected within the chip. This layout determines how the IC processes input signals to generate the required output. Understanding the sub-circuit helps in optimizing circuit performance and ensuring efficient logic operation.

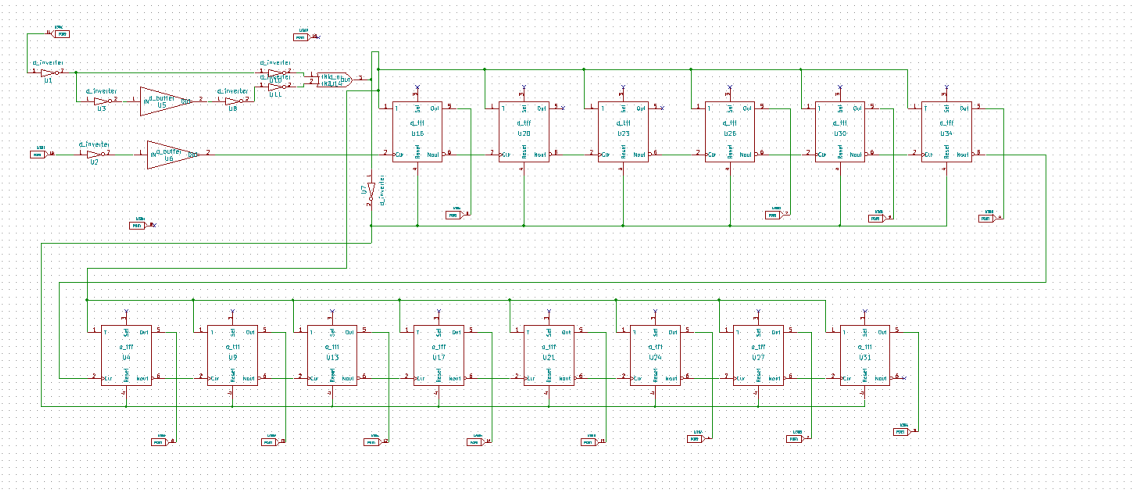

Figure 4.50: Sub Circuit of SN74HC4020

4.13.3 Test Circuit

The figure illustrates a test setup used to verify the performance of the SN74HC4020 IC. A test circuit includes a power source, input signal generators, and output monitoring devices such as oscilloscopes or logic analyzers. This setup helps evaluate response time, signal integrity, and overall functionality under different conditions.

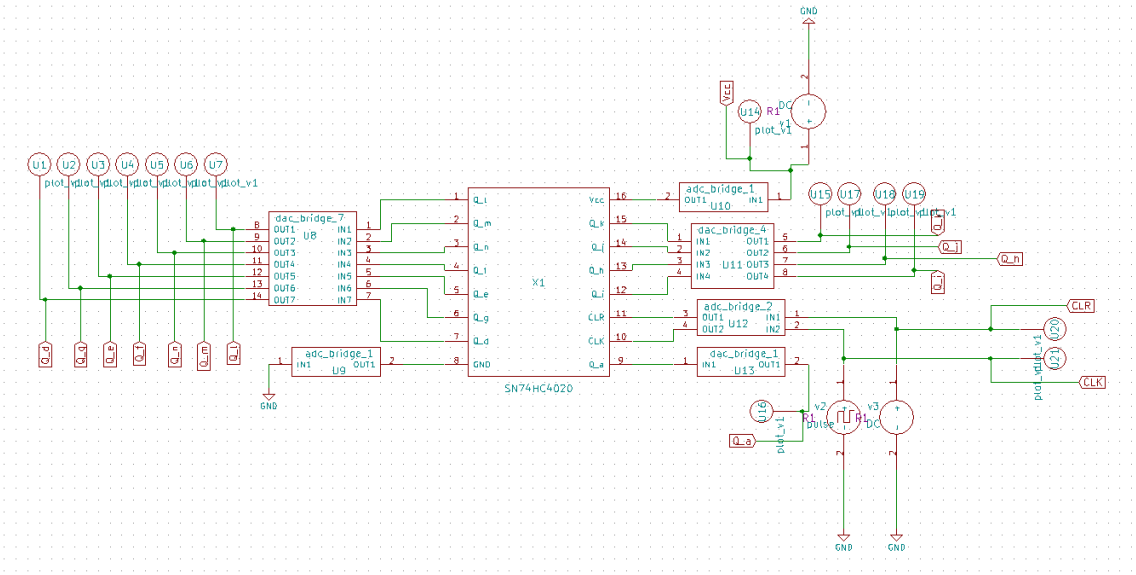

Figure 4.51: Test Circuit of SN74HC4020

4.13.4 Output Waveforms

The figure shows the signal produced at the output pin of the SN74HC4020 IC after processing the input signals. This waveform represents the binary counting operation performed by the IC.

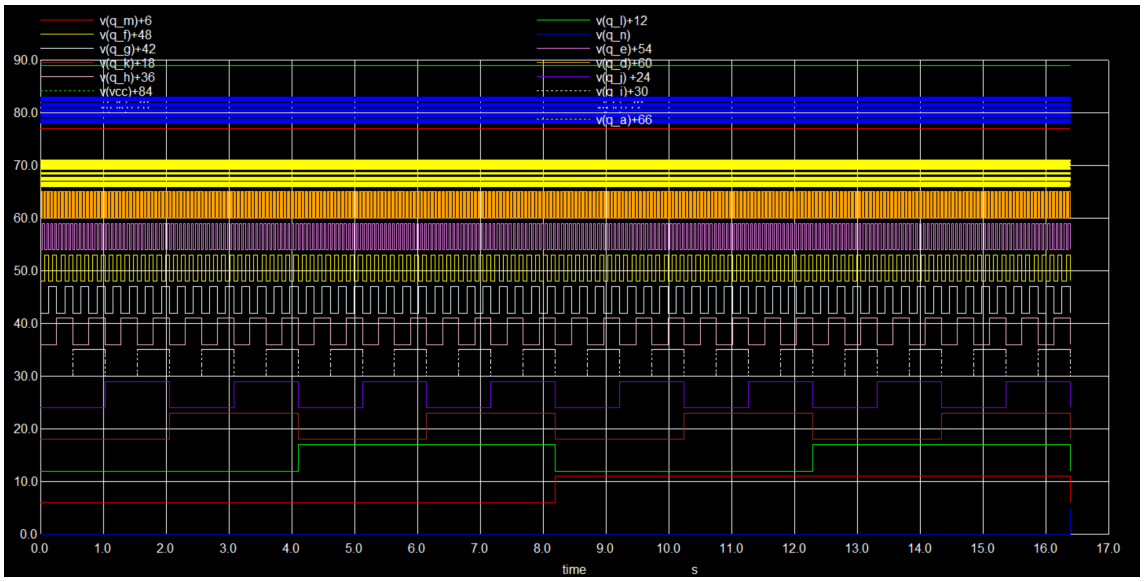

Figure 4.52: Output Waveform of SN74HC4020

4.14 SN74LS75

The SN5475, SN7475, and SN74LS75 are quad (4-bit) bistable latches designed for temporary data storage applications. Each latch in the IC has a *D-type* configuration

with a data input (D), an output (Q), and an enable input (G, sometimes labeled EN or LE).

These latches are *level-triggered*, meaning data on the D input is latched into the Q output when the enable input is held high (logic 1). When the enable goes low (logic 0), the last value present at the D input is retained at the output, effectively "locking" the output until the next latch-enable cycle.

The IC is ideal for use in temporary data storage, buffering, and I/O interfacing where simple memory elements are needed. It supports TTL-compatible voltage levels and is available in standard DIP and SOIC packages.

Internally, each latch behaves independently, allowing users to control or latch four separate bits of data simultaneously or selectively. These features make the SN5475 family a fundamental building block in synchronous and asynchronous digital systems.

Table 4.13: Function Table of D-Type Transparent Latch (SN74LS75)

G (Enable)	D (Data Input)	Q (Output)
H	L	L
H	H	H
L	X	$Q_{previous}$

4.14.1 Pin Diagram

The figure shows the physical representation of the SN74LS75 IC, indicating the arrangement of its pins. It includes input pins, an output pin, a power supply pin, and a ground pin. The pin diagram is essential for correctly integrating the IC into a circuit, ensuring proper connections and functionality in digital applications.

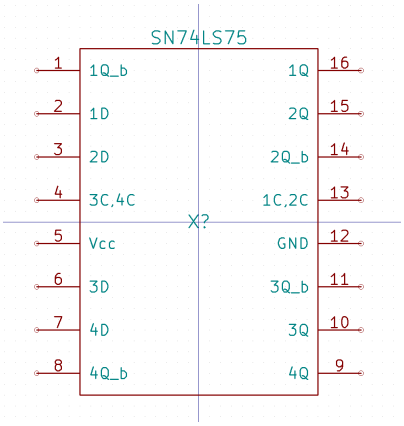

Figure 4.53: Pin layout of SN74LS75

4.14.2 SubCircuit Layout

The figure represents the internal design of the SN74HC4020 IC, showing how logic gates and components are interconnected within the chip. This layout determines

how the IC processes input signals to generate the required output. Understanding the sub-circuit helps in optimizing circuit performance and ensuring efficient logic operation.

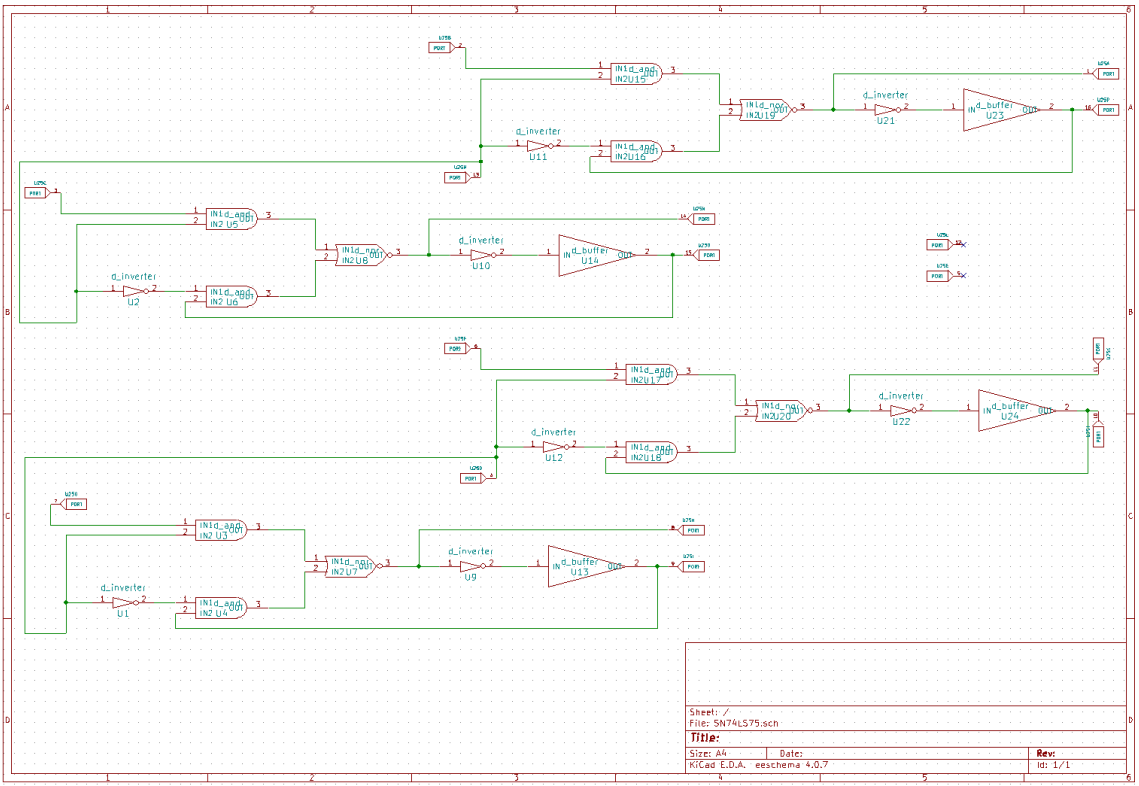

Figure 4.54: Sub Circuit of SN74LS75

4.14.3 Test Circuit

The figure illustrates a test setup used to verify the performance of the SN74LS75 IC. A test circuit includes a power source, input signal generators, and output monitoring devices such as oscilloscopes or logic analysers. This setup helps evaluate response time, signal integrity, and overall functionality under different conditions.

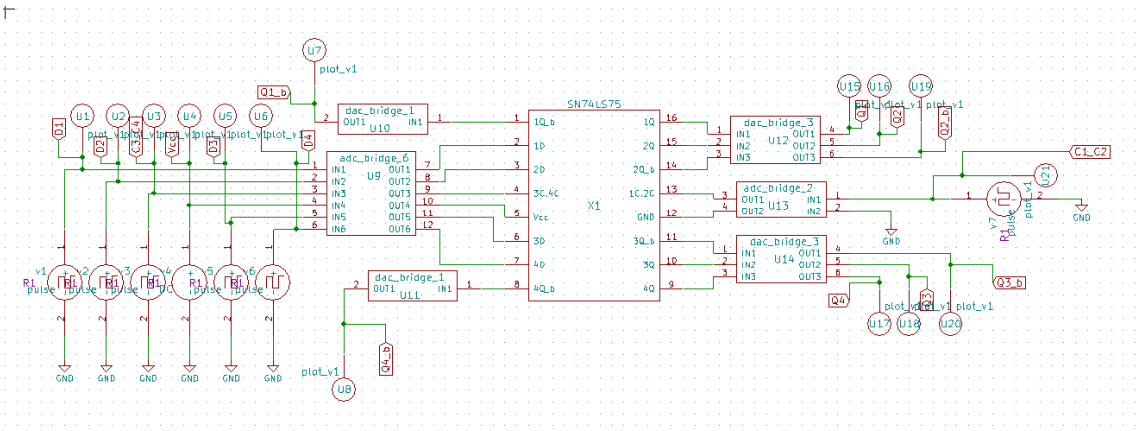

Figure 4.55: Test Circuit of SN74LS75

4.14.4 Output Waveforms

The figure shows the signal produced at the output pin of the SN74LS75 IC after processing the input signals. This waveform represents the latching operation performed by the IC.

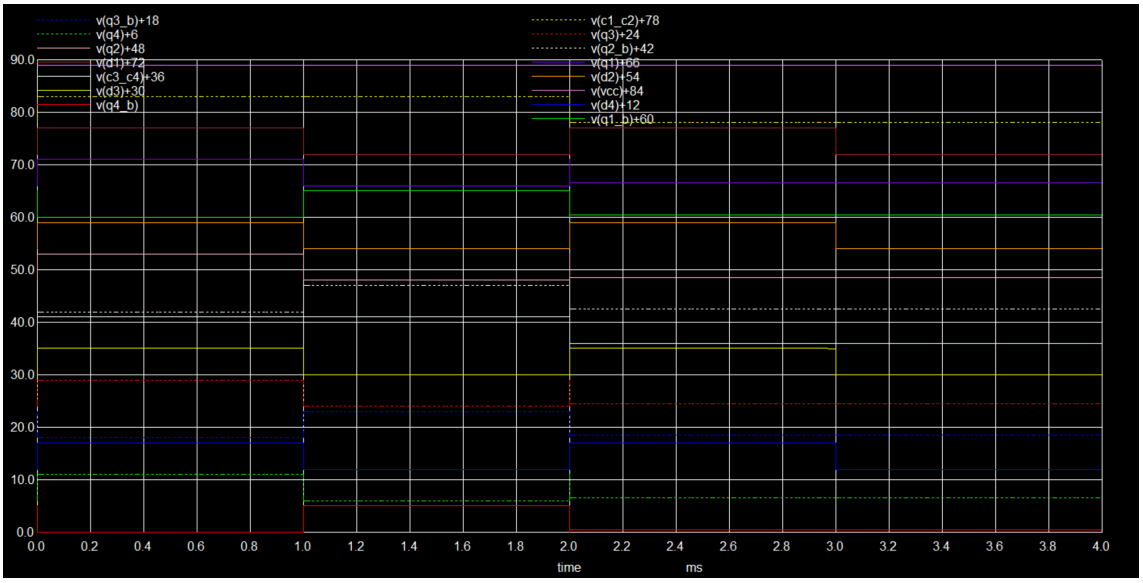

Figure 4.56: Output Waveform of SN74LS75

4.15 SN74LVC1G57

The SN74LVC1G57 is a configurable multiple-function gate from Texas Instruments, designed using advanced CMOS technology to achieve high-speed and low-power operation. It operates from a wide supply voltage range of 1.65 V to 5.5 V, making it compatible with both TTL and CMOS logic levels. The device supports various logic functions, including AND, OR, NAND, NOR, XOR, XNOR, inverter, buffer, and constant logic levels, based on the configuration of its three inputs.

The IC has three inputs (A, B, C) and one output (Y), and its logic function is defined by hardwiring any unused input to HIGH or LOW. This flexibility allows the designer to replace multiple logic gates with a single, space-saving component. The SN74LVC1G57 is particularly useful in portable and battery-powered applications due to its low power consumption and small footprint (available in packages like SOT-23 and SC-70).

The device includes Schmitt-trigger action at the inputs for better noise immunity and has protection features such as partial power-down support and high drive capability (up to ±24 mA at 3.3 V).

Table 4.14: Logic Function Configurations for SN74LVC1G57

A	**B**	**C**	**Y (Output Function)**
X	X	0	0 (Constant LOW)
X	X	1	1 (Constant HIGH)
A	0	0	A (Buffer)
A	0	1	$\overline{A}$ (Inverter)
A	B	0	A AND B
A	B	1	A OR B
A	$\overline{B}$	1	A XOR B
$\overline{A}$	$\overline{B}$	0	A XNOR B

4.15.1 Pin Diagram

The figure shows the physical representation of the SN74LVC1G57 IC, indicating the arrangement of its pins. It includes input pins, an output pin, a power supply pin, and a ground pin. The pin diagram is essential for correctly integrating the IC into a circuit, ensuring proper connections and functionality in digital applications.

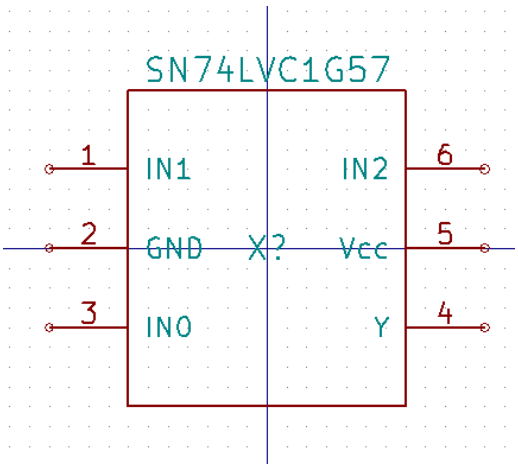

Figure 4.57: Pin layout of SN74LVC1G57

4.15.2 SubCircuit Layout

The figure represents the internal design of the SN74LVC1G57 IC, showing how logic gates and components are interconnected within the chip. This layout determines how the IC processes input signals to generate the required output. Understanding the sub-circuit helps in optimizing circuit performance and ensuring efficient logic operation.

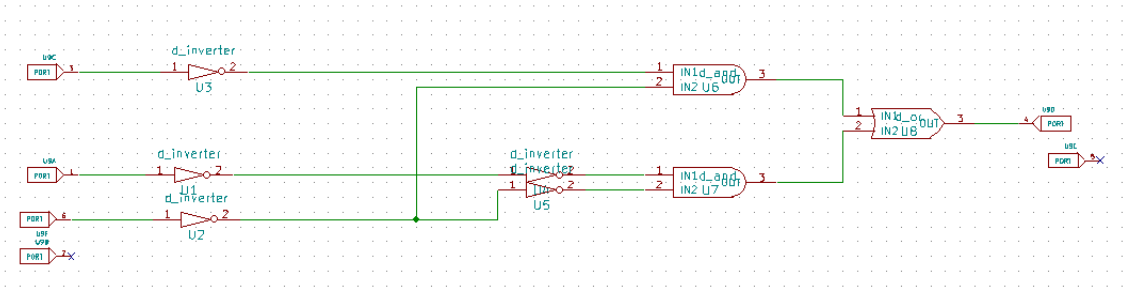

Figure 4.58: Sub Circuit of SN74LVC1G57

4.15.3 Test Circuit

The figure illustrates a test setup used to verify the performance of the SN74LVC1G57 IC. A test circuit includes a power source, input signal generators, and output monitoring devices such as oscilloscopes or logic analyzers. This setup helps evaluate response time, signal integrity, and overall functionality under different conditions.

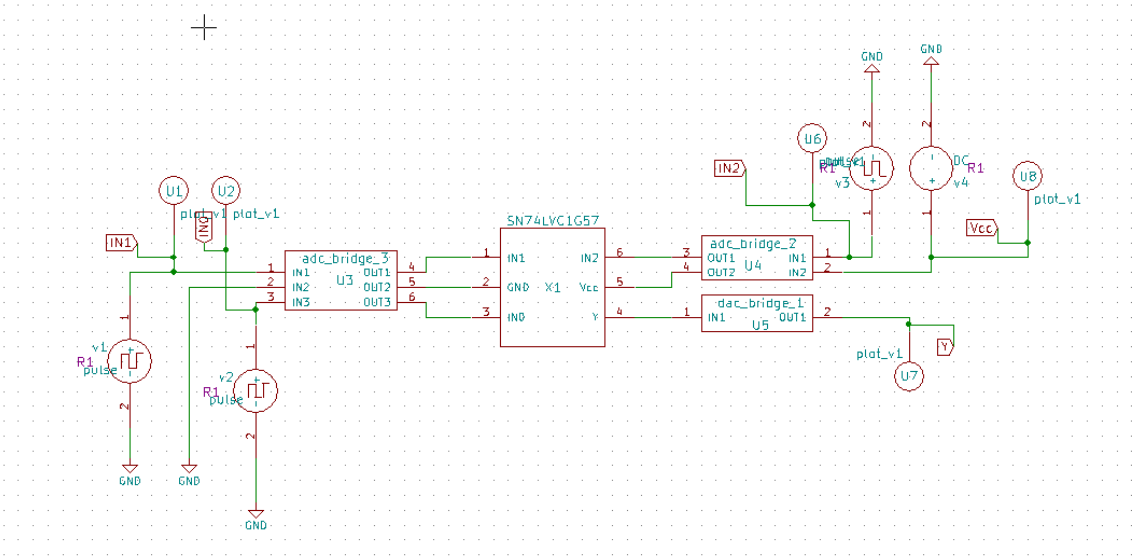

Figure 4.59: Test Circuit of SN74LVC1G57

4.15.4 Output Waveforms

The figure shows the signal produced at the output pin of the SN74LVC1G57 IC after processing the input signals. This waveform represents the multiple-function

logic operation performed by the IC.

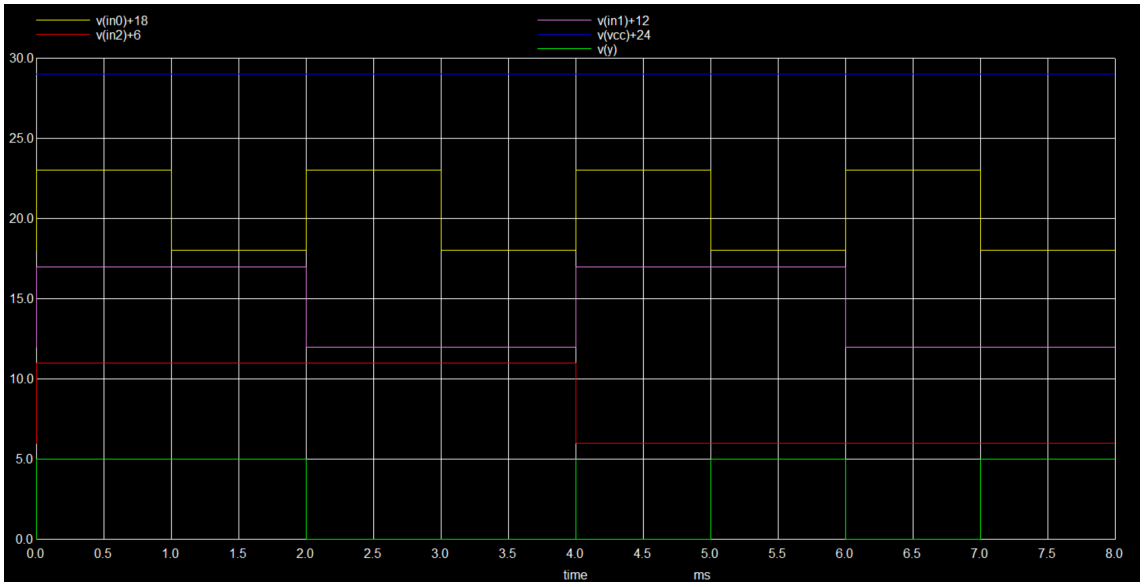

Figure 4.60: Output Waveform of SN74LVC1G57

4.16 SN54S182

The SN54S182 and SN74S182 are look-ahead carry generators designed for high-speed arithmetic operations in binary adder circuits. These devices are intended to improve the speed of binary addition by eliminating the delay caused by the ripple-carry method. They generate carry signals in advance of the actual binary addition, allowing for faster multi-bit addition.

Each IC accepts four pairs of generate (G) and propagate (P) signals from binary adders, along with a carry input (C_0), and produces three carry outputs: C_1, C_2, and C_3, as well as a carry-out (C_4). It also provides group propagate (P_G) and group generate (G_G) signals which can be used to cascade multiple carry look-ahead blocks for wider adders.

These ICs significantly reduce propagation delay in multi-bit addition systems and are particularly useful in constructing fast arithmetic logic units (ALUs) and high-performance processors. The devices support TTL logic levels and are available in military and commercial temperature ranges.

Table 4.15: Truth Table of Look-Ahead Carry Generator (SN54S182 / SN74S182)

Inputs	**Carry Look-Ahead Outputs**	**Group Signals**
C_0	C_1	G_G, P_G
G_0, P_0	C_2	
G_1, P_1	C_3	
G_2, P_2	C_4	
G_3, P_3		

4.16.1 Pin Diagram

The figure shows the physical representation of the SN54S182 IC, indicating the arrangement of its pins. It includes input pins, an output pin, a power supply pin, and a ground pin. The pin diagram is essential for correctly integrating the IC into a circuit, ensuring proper connections and functionality in digital applications.

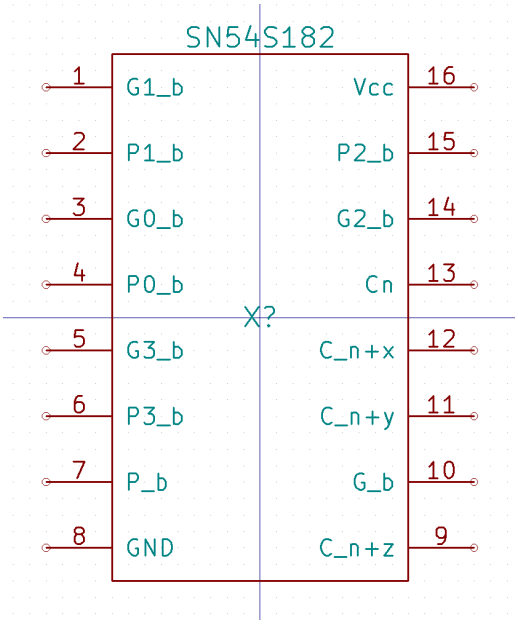

Figure 4.61: Pin layout of SN54S182

4.16.2 SubCircuit Layout

The figure represents the internal design of the SN54S182 IC, showing how logic gates and components are interconnected within the chip. This layout determines how the IC processes input signals to generate the required output. Understanding the sub-circuit helps in optimizing circuit performance and ensuring efficient logic operation.

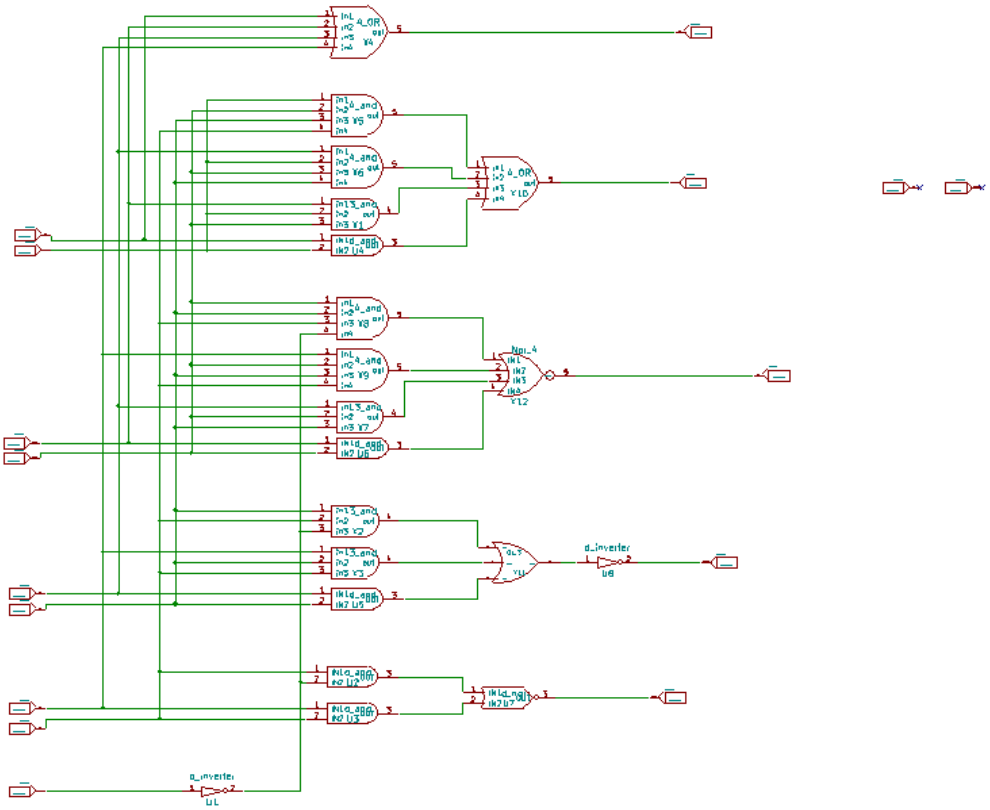

Figure 4.62: Sub Circuit of SN54S182

4.16.3 Test Circuit

The figure illustrates a test setup used to verify the performance of the SN54S182 IC. A test circuit includes a power source, input signal generators, and output monitoring devices such as oscilloscopes or logic analyzers. This setup helps evaluate response time, signal integrity, and overall functionality under different conditions.

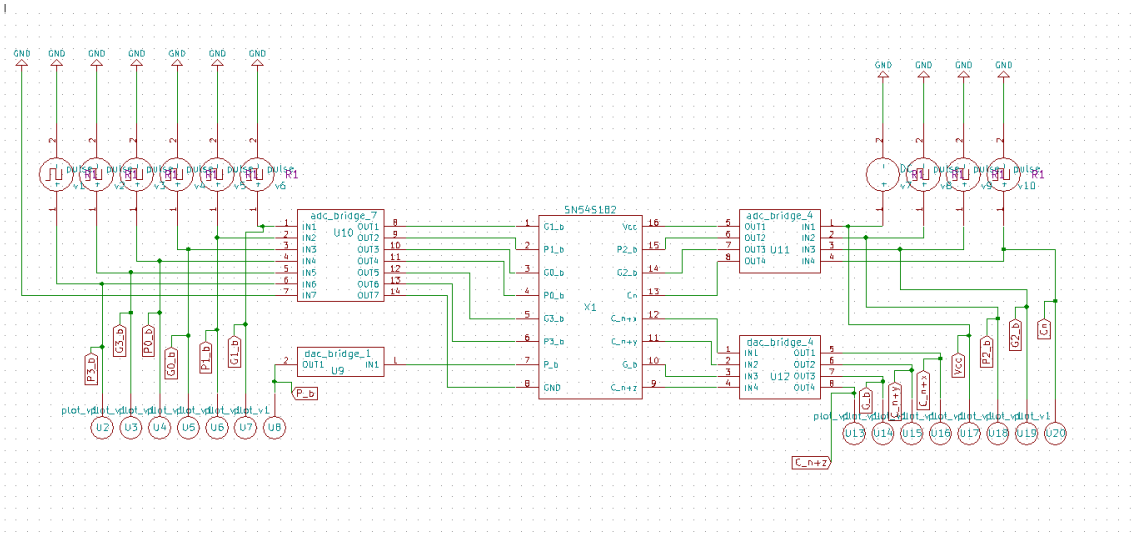

Figure 4.63: Test Circuit of SN54S182

4.16.4 Output Waveforms

The figure shows the signal produced at the output pin of the SN54S182 IC after processing the input signals. This waveform represents the look-ahead carry generation operation performed by the IC.

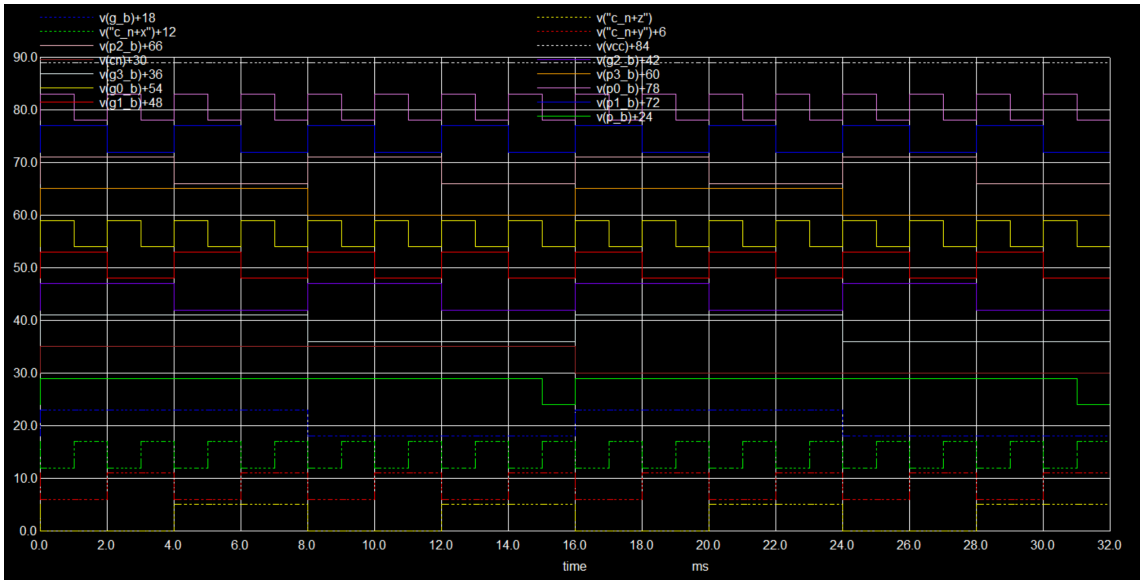

Figure 4.64: Output Waveform of SN54S182

4.17 SN74AUP1G99

The SN74AUP1G99 is a single configurable multiple-function gate from Texas Instruments, designed for ultra-low-power operation and high performance in space-constrained systems. It supports a broad voltage range from 0.8 V to 3.6 V and

operates efficiently even at very low supply levels. The device has three inputs (A, B, and SEL) and one output (Y), with the output function determined by the state of the select input (SEL).

When SEL is held low, the gate functions as a 2-input AND gate. When SEL is high, the function switches to a 2-input OR gate. This dynamic configurability allows flexible logic design without requiring multiple discrete components. The device includes features such as Schmitt-trigger action on all inputs for noise immunity and supports partial power-down through IOFF circuitry, preventing backflow of current when the device is powered down.

Due to its compact size, low power consumption, and multi-functionality, the SN74AUP1G99 is ideal for portable, battery-powered, and logic replacement applications.

Table 4.16: Truth Table of SN74AUP1G99

A	B	SEL	Y (Output)
0	0	0	0
0	1	0	0
1	0	0	0
1	1	0	1
0	0	1	0
0	1	1	1
1	0	1	1
1	1	1	1

4.17.1 Pin Diagram

The figure shows the physical representation of the SN74AUP1G99 IC, indicating the arrangement of its pins. It includes input pins, an output pin, a power supply pin, and a ground pin. The pin diagram is essential for correctly integrating the IC into a circuit, ensuring proper connections and functionality in digital applications.

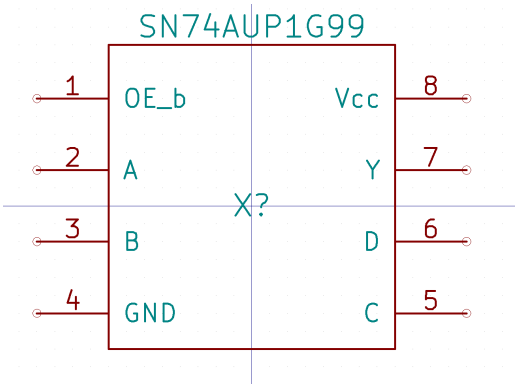

Figure 4.65: Pin layout of SN74AUP1G99

4.17.2 SubCircuit Layout

The figure represents the internal design of the SN74AUP1G99 IC, showing how logic gates and components are interconnected within the chip. This layout determines how the IC processes input signals to generate the required output. Understanding the sub-circuit helps in optimizing circuit performance and ensuring efficient logic operation.

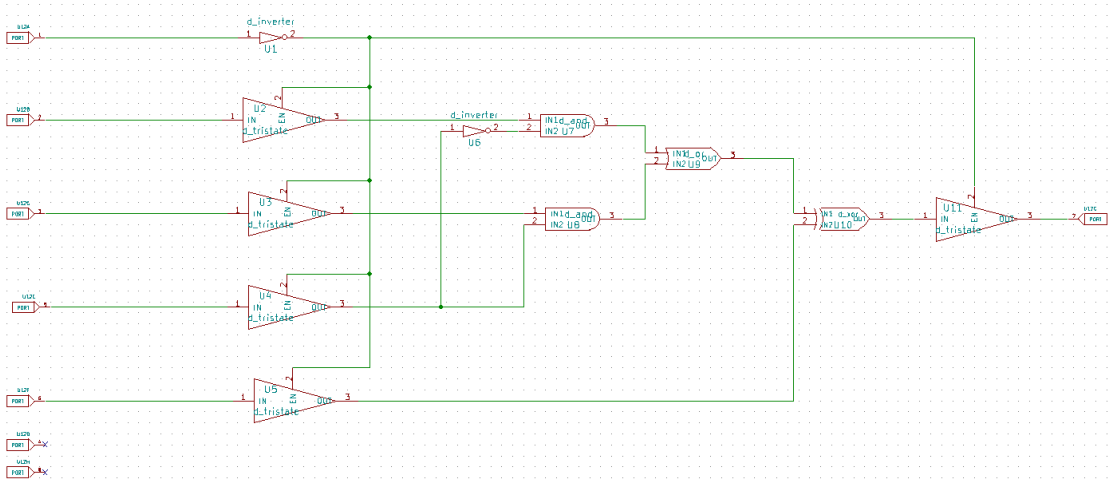

Figure 4.66: Sub Circuit of SN74AUP1G99

4.17.3 Test Circuit

The figure illustrates a test setup used to verify the performance of the SN74AUP1G99 IC. A test circuit includes a power source, input signal generators, and output monitoring devices such as oscilloscopes or logic analyzers. This setup helps evaluate response time, signal integrity, and overall functionality under different conditions.

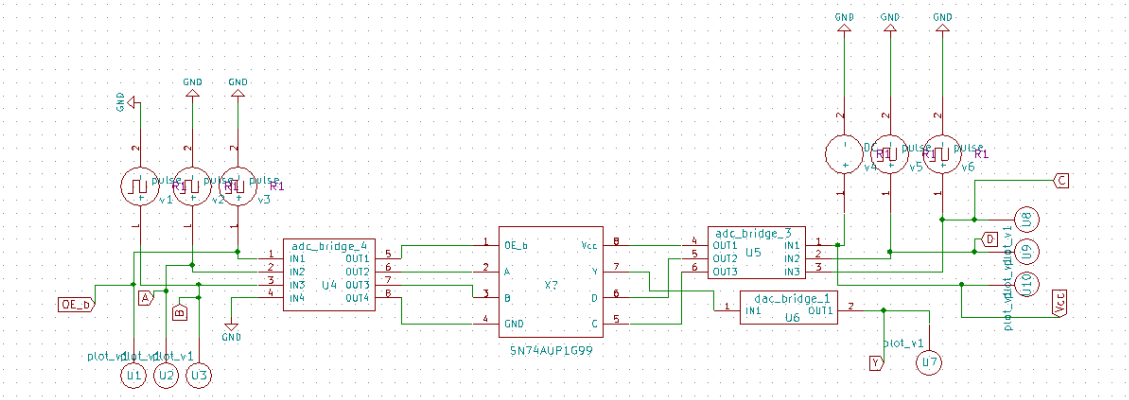

Figure 4.67: Test Circuit of SN74AUP1G99

4.17.4 Output Waveforms

The figure shows the signal produced at the output pin of the SN74AUP1G99 IC after processing the input signals. This waveform represents the multiple-function gate operation performed by the IC.

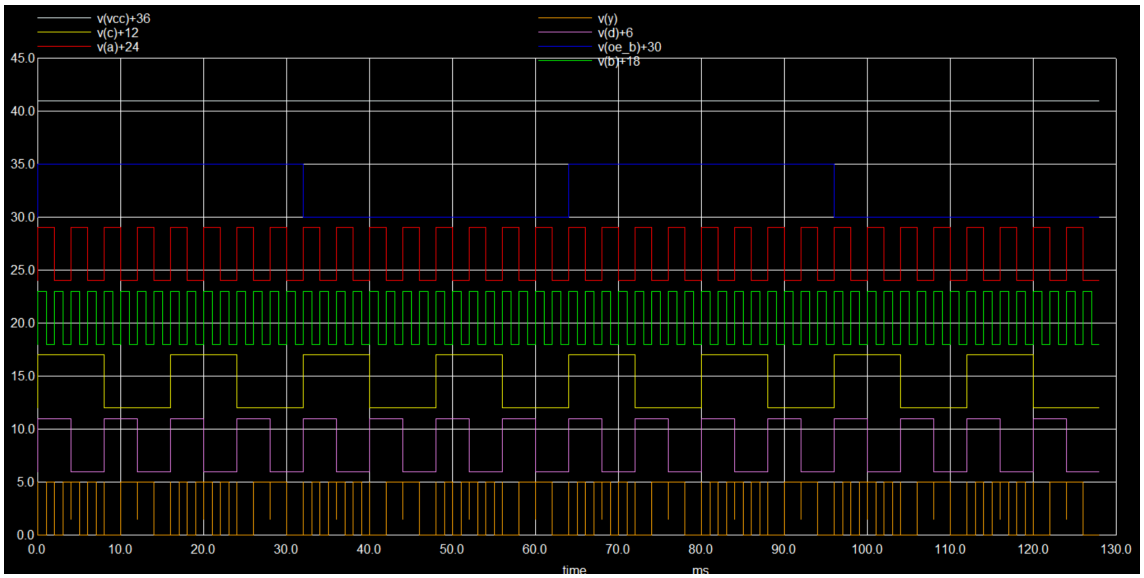

Figure 4.68: Output Waveform of SN74AUP1G99

4.18 SN74LS697

The SN74LS697 is a high-speed 8-bit synchronous binary up-counter with programmable load capability. It is built using TTL technology and integrates two 4-bit binary counters internally, which operate together to form an 8-bit counter. The device has a clear (reset), enable, and load function for flexible operation.

The counter advances on the positive edge of the clock signal if both enable inputs (ENP and ENT) are high. The programmable load feature allows loading of a preset value into the counter on demand using the load control (LOAD) input. The clear (CLR) input resets all outputs to zero asynchronously.

The terminal count (TC) output is active high when the counter reaches its maximum value (255), and both enable inputs are active. This output can be used for cascading multiple counters for wider bit counting.

The SN74LS697 is commonly used in digital timers, frequency dividers, event counters, and address sequencing applications where both high-speed and preset-table counting features are required.

Table 4.17: Truth Table for SN74LS697

CLR	LOAD	ENP	ENT	Clock ↑	Function
L	X	X	X	X	Reset to 0 (asynchronous)
H	L	X	X	X	Load preset data (synchronous)
H	H	H	H	Yes	Count up by 1
H	H	H	L	Yes	No change
H	H	L	X	Yes	No change
H	H	X	X	No	No change

4.18.1 Pin Diagram

The figure shows the physical representation of the SN74LS697 IC, indicating the arrangement of its pins. It includes input pins, an output pin, a power supply pin, and a ground pin. The pin diagram is essential for correctly integrating the IC into a circuit, ensuring proper connections and functionality in digital applications.

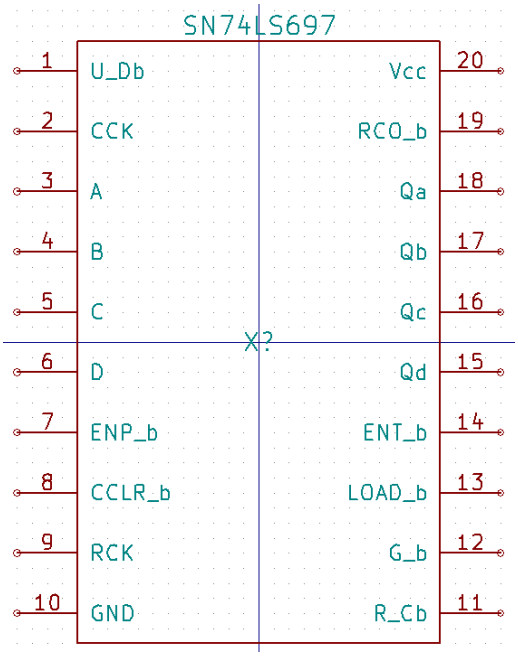

Figure 4.69: Pin layout of SN74LS697

4.18.2 SubCircuit Layout

The figure represents the internal design of the SN74LS697 IC, showing how logic gates and components are interconnected within the chip. This layout determines how the IC processes input signals to generate the required output. Understanding the sub-circuit helps in optimizing circuit performance and ensuring efficient logic operation.

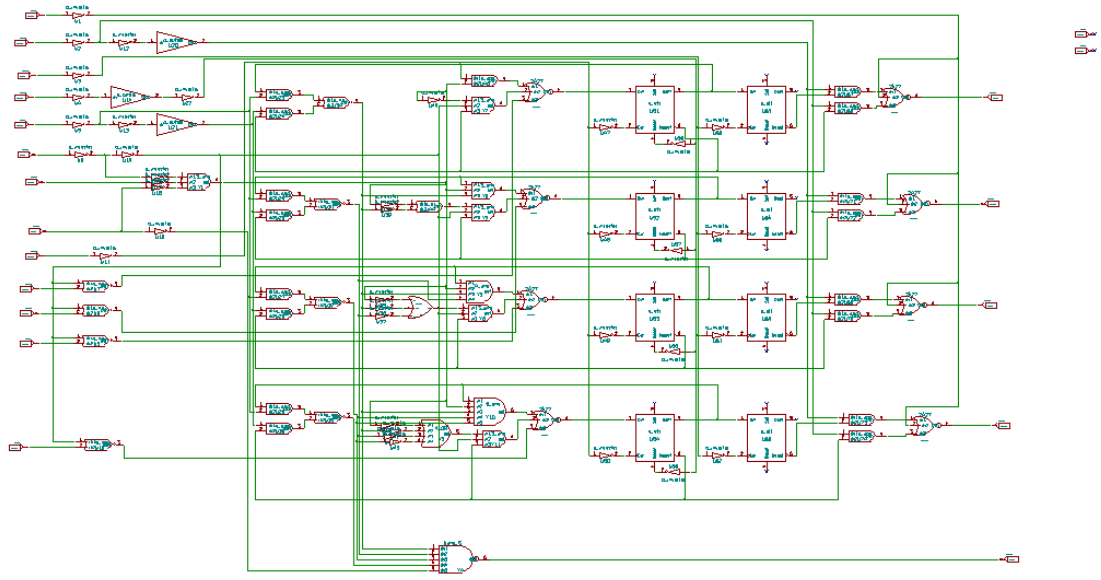

Figure 4.70: Sub Circuit of SN74LS697

4.18.3 Test Circuit

The figure illustrates a test setup used to verify the performance of the SN74LS697 IC. A test circuit includes a power source, input signal generators, and output monitoring devices such as oscilloscopes or logic analyzers. This setup helps evaluate response time, signal integrity, and overall functionality under different conditions.

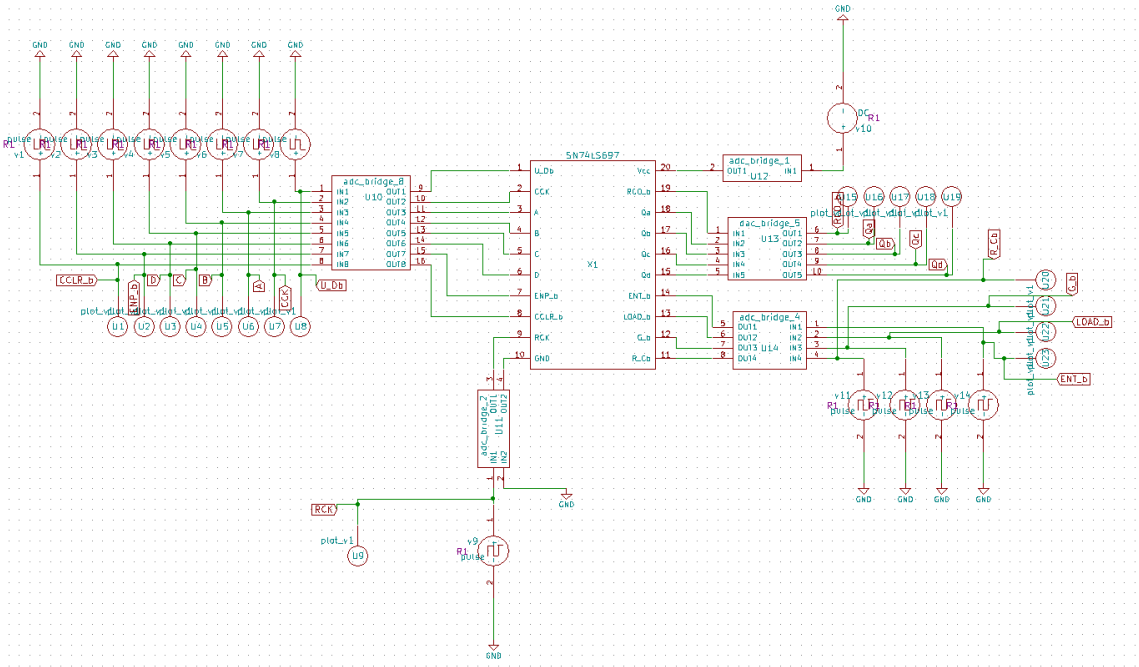

Figure 4.71: Test Circuit of SN74LS697

4.18.4 Output Waveforms

The figure shows the signal produced at the output pin of the SN74LS697 IC after processing the input signals. This waveform represents the asynchronous binary up-counter operation performed by the IC.

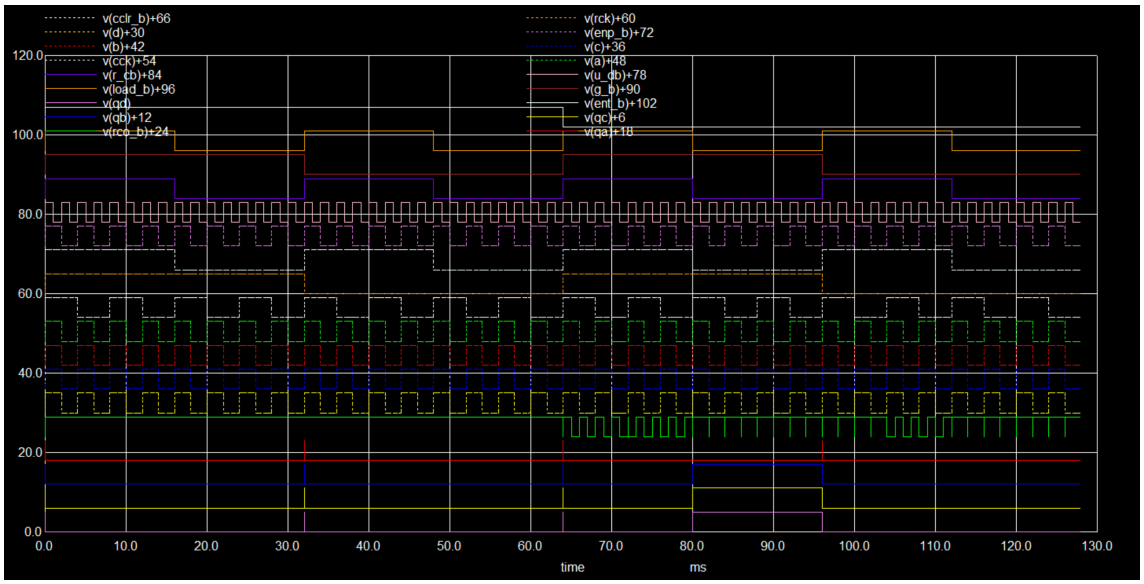

Figure 4.72: Output Waveform of SN74LS697

4.19 SN54ALS560A

The SN54ALS560A and SN74ALS560A are octal (8-bit) buffers and line drivers designed specifically for driving high-capacitance bus lines or buffers. These ICs feature 3-state outputs, allowing multiple devices to share a common output line without conflict, making them ideal for bus-oriented applications.

Each device contains eight non-inverting buffers with a common output enable (OE) control. When the output enable is low, all eight outputs are enabled and reflect the input states. When the output enable is high, all outputs are placed in the high-impedance state, effectively disconnecting them from the bus.

These ICs are manufactured using advanced low-power Schottky TTL technology, which offers improved speed and power characteristics. The devices are pin-compatible with standard 74ALS series logic and operate over a recommended supply voltage of 4.5 V to 5.5 V.

The SN54ALS560A is specified for military temperature ranges, while the SN74ALS560A is specified for commercial applications. They are widely used in memory systems, microprocessor buses, and digital backplanes.

Table 4.18: Truth Table of SN54ALS560A / SN74ALS560A

OE	A (Input)	Y (Output)
L	L	L
L	H	H
H	X	Z (High Impedance)

4.19.1 Pin Diagram

The figure shows the physical representation of the SN54ALS560A IC, indicating the arrangement of its pins. It includes input pins, an output pin, a power supply pin, and a ground pin. The pin diagram is essential for correctly integrating the IC into a circuit, ensuring proper connections and functionality in digital applications.

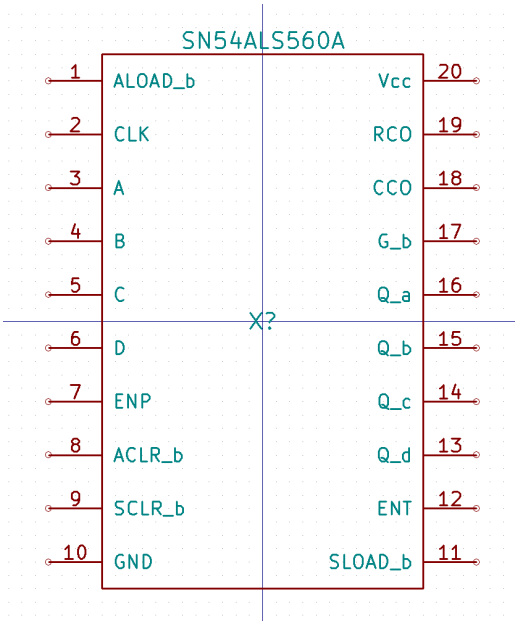

Figure 4.73: Pin layout of SN54ALS560A

4.19.2 SubCircuit Layout

The figure represents the internal design of the SN54ALS560A IC, showing how logic gates and components are interconnected within the chip. This layout determines how the IC processes input signals to generate the required output. Understanding the sub-circuit helps in optimizing circuit performance and ensuring efficient logic operation.

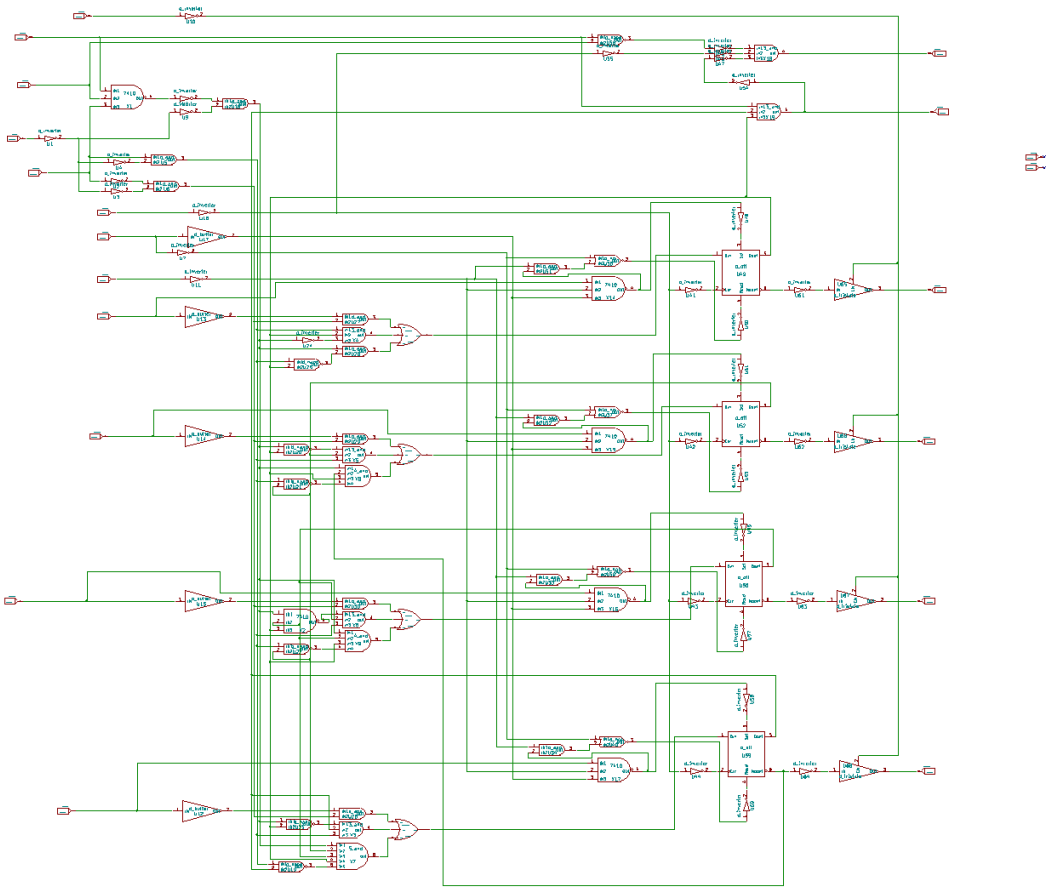

Figure 4.74: Sub Circuit of SN54ALS560A

4.19.3 Test Circuit

The figure illustrates a test setup used to verify the performance of the SN54ALS560A IC. A test circuit includes a power source, input signal generators, and output monitoring devices such as oscilloscopes or logic analyzers. This setup helps evaluate response time, signal integrity, and overall functionality under different conditions.

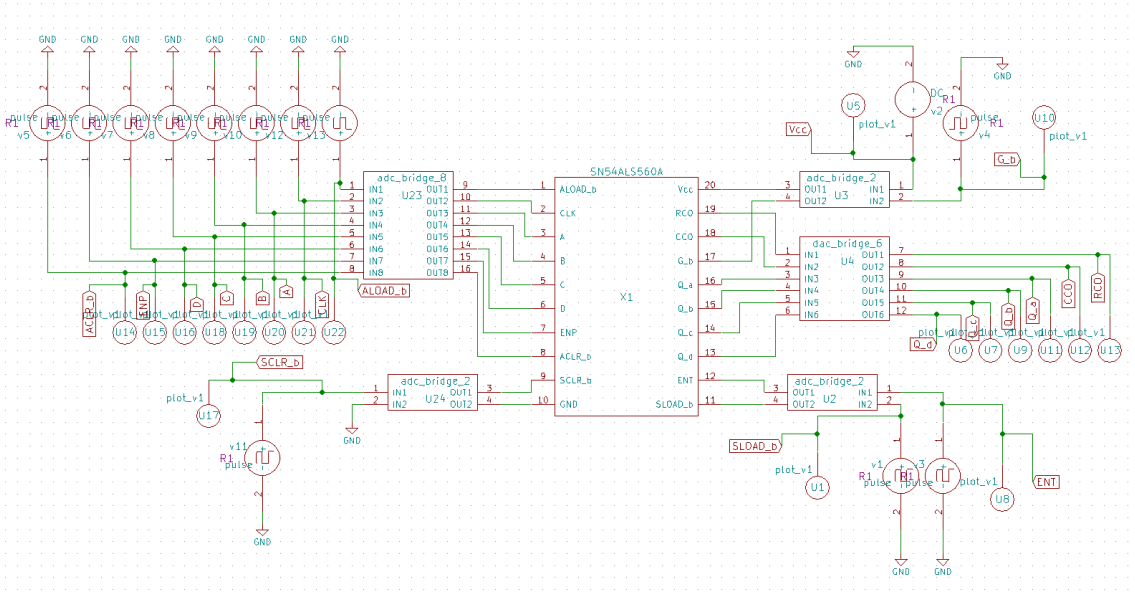

Figure 4.75: Test Circuit of SN54ALS560A

4.19.4 Output Waveforms

The figure shows the signal produced at the output pin of the SN54ALS560A IC after processing the input signals. This waveform represents the buffer operation performed by the IC.

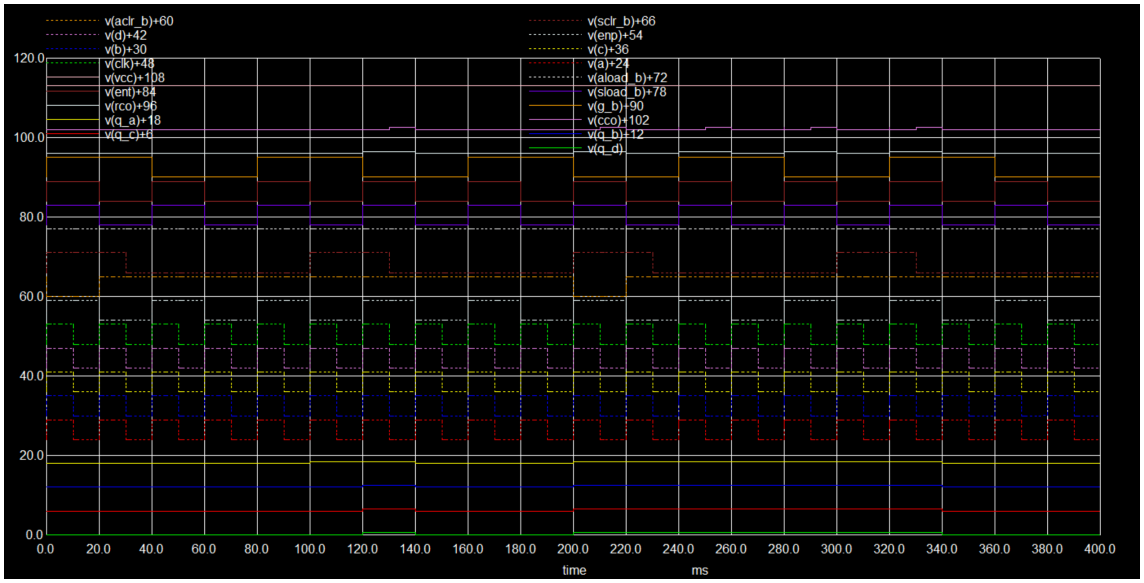

Figure 4.76: Output Waveform of SN54ALS560A

4.20 SN74ALS8161

The SN74ALS8161 is a 9-bit identity comparator designed for high-speed comparison of two binary words. It compares two sets of 9-bit binary inputs (A0–A8 and B0–B8)

and provides three active-low outputs: A > B (A ¿ B), A = B ($A = B$), and A < B (A ¡ B). These outputs allow cascading of multiple devices for wider word comparisons.

The device performs bit-by-bit comparison starting from the most significant bit (A8 vs B8) to the least significant (A0 vs B0), terminating early if a difference is found. All outputs are active-low and provide definitive comparison signals for equality and inequality. This IC supports high-speed logic families (ALS), and it is optimized for use in arithmetic logic units (ALUs), memory address decoding, and data sorting operations.

The SN74ALS8161 operates with TTL-compatible input levels and delivers fast propagation delays while maintaining low power dissipation. It is commonly used in systems requiring digital word comparison for control logic and bus arbitration.

Table 4.19: Truth Table for Identity Comparator (SN74ALS8161)

Comparison Result	**A = B**	**A ¿ B**	**A ¡ B**
A = B	L	H	H
A ¿ B	H	L	H
A ¡ B	H	H	L

4.20.1 Pin Diagram

The figure shows the physical representation of the SN74ALS8161 IC, indicating the arrangement of its pins. It includes input pins, an output pin, a power supply pin, and a ground pin. The pin diagram is essential for correctly integrating the IC into a circuit, ensuring proper connections and functionality in digital applications.

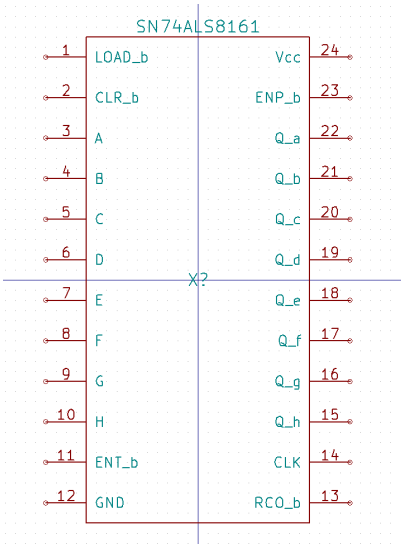

Figure 4.77: Pin layout of SN74ALS8161

4.20.2 SubCircuit Layout

The figure represents the internal design of the SN74ALS8161 IC, showing how logic gates and components are interconnected within the chip. This layout determines how the IC processes input signals to generate the required output. Understanding the sub-circuit helps in optimizing circuit performance and ensuring efficient logic operation.

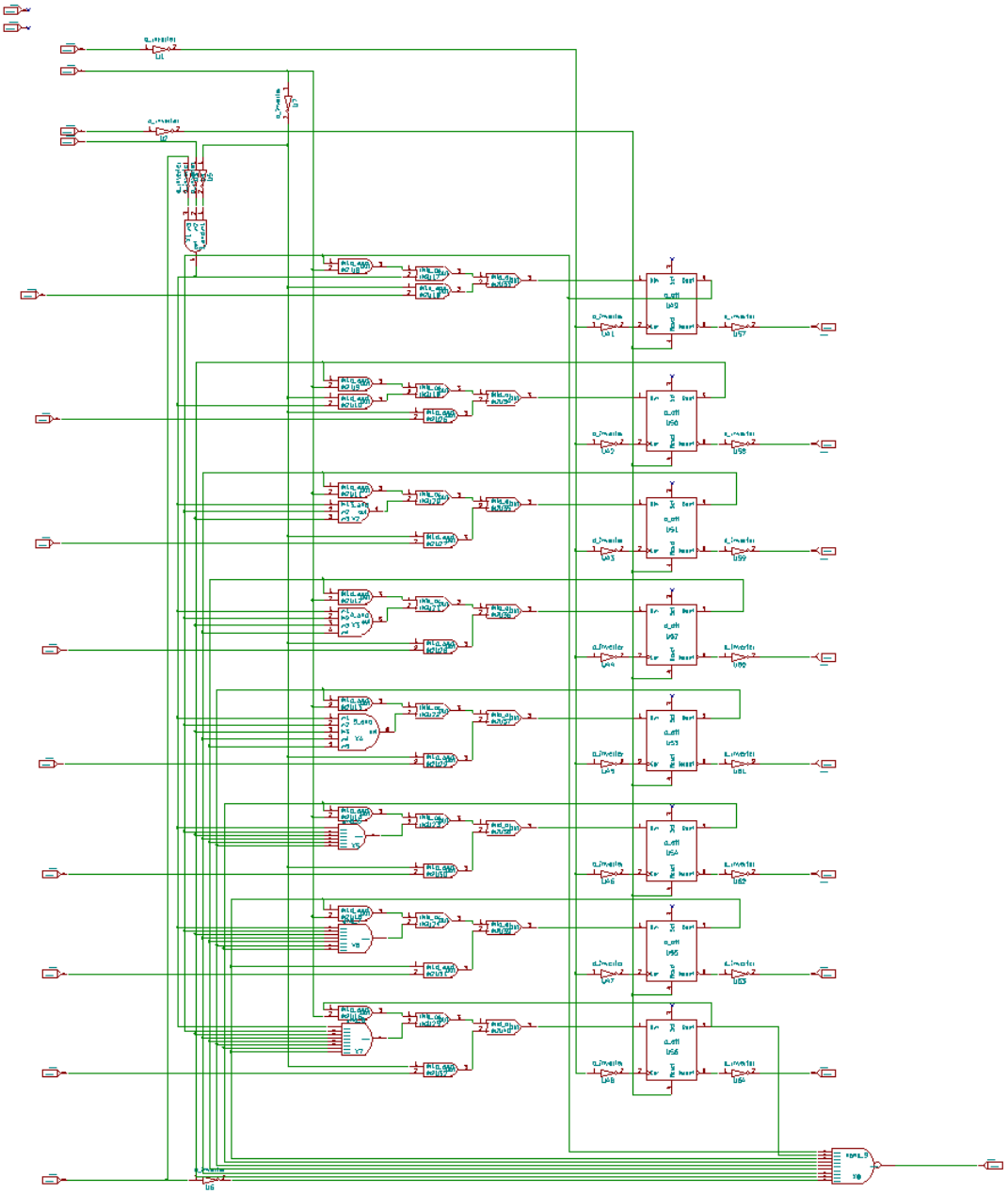

Figure 4.78: Sub Circuit of SN74ALS8161

4.20.3 Test Circuit

The figure illustrates a test setup used to verify the performance of the SN74ALS8161 IC. A test circuit includes a power source, input signal generators, and output monitoring devices such as oscilloscopes or logic analyzers. This setup helps evaluate response time, signal integrity, and overall functionality under different conditions.

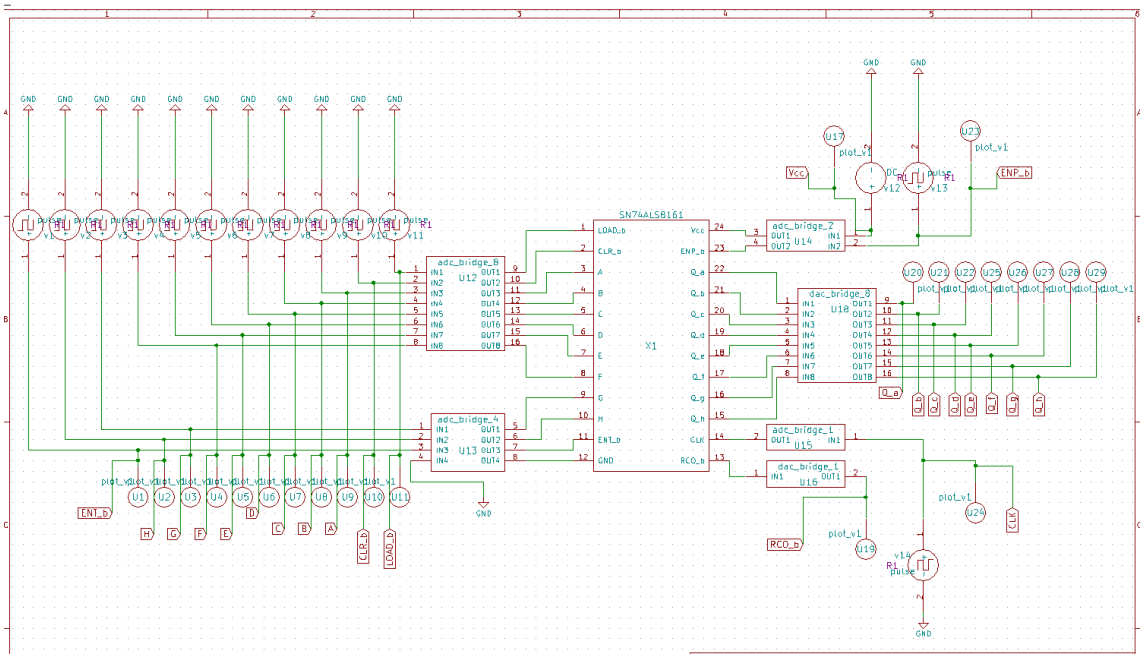

Figure 4.79: Test Circuit of SN74ALS8161

4.20.4 Output Waveforms

The figure shows the signal produced at the output pin of the SN74ALS8161 IC after processing the input signals. This waveform represents the binary comparison operation performed by the IC.

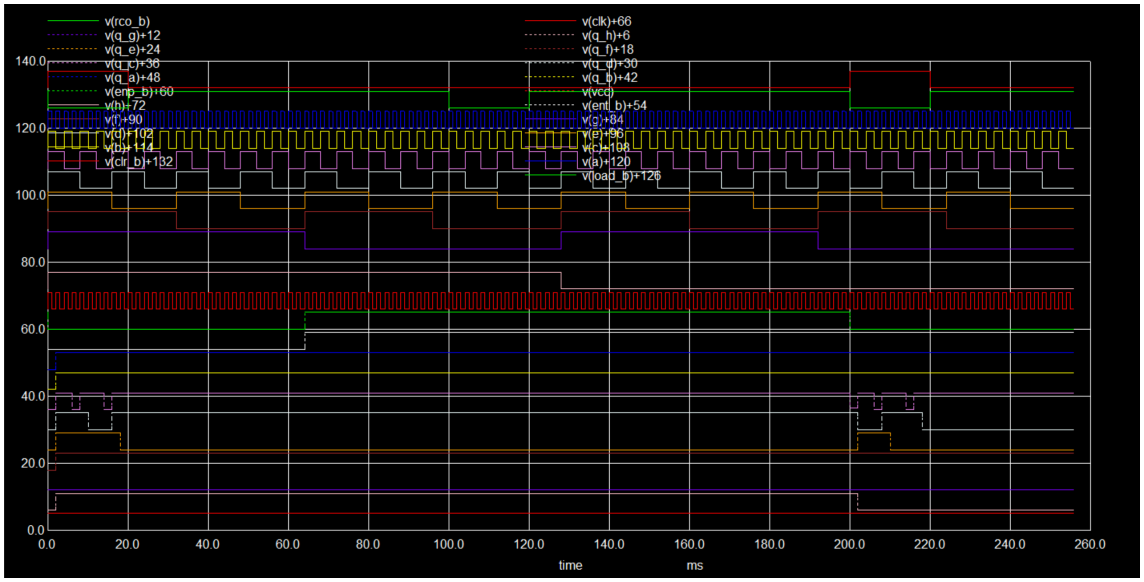

Figure 4.80: Output Waveform of SN74ALS8161

4.21 SN74LVC8T245

The SN74LVC8T245 is an 8-bit non-inverting bus transceiver with configurable voltage-level translation capabilities, designed by Texas Instruments. It features two separate supply voltage pins: V_{CCA} and V_{CCB}, which allow it to perform bidirectional logic level shifting between different voltage domains ranging from 1.2 V to 5.5 V. The device is ideal for interfacing components that operate at different logic levels, such as 1.8 V to 3.3 V or 3.3 V to 5 V. Direction control is managed by the DIR pin, and data transmission is enabled or disabled using the OE (Output Enable) pin. Both control inputs are referenced to V_{CCA}, ensuring compatibility with the low-voltage side.

The SN74LVC8T245 uses a dual-supply architecture and includes internal one-shot circuitry to prevent contention during power-up and power-down. It offers excellent signal integrity and high-speed operation, making it suitable for applications in mobile phones, portable electronics, and embedded systems. The device is available in multiple package options, including TSSOP, SOIC, and QFN, and supports hot-insertion and partial power-down protection features.

Table 4.20: Truth Table for SN74LVC8T245

OE	**DIR**	**A ↔ B**	**Operation**
L	L	B → A	Data from B to A
L	H	A → B	Data from A to B
H	X	High-Z	Outputs disabled (high-impedance)

4.21.1 Pin Diagram

The figure shows the physical representation of the SN74LVC8T245 IC, indicating the arrangement of its pins. It includes input pins, an output pin, a power supply

pin, and a ground pin. The pin diagram is essential for correctly integrating the IC into a circuit, ensuring proper connections and functionality in digital applications.

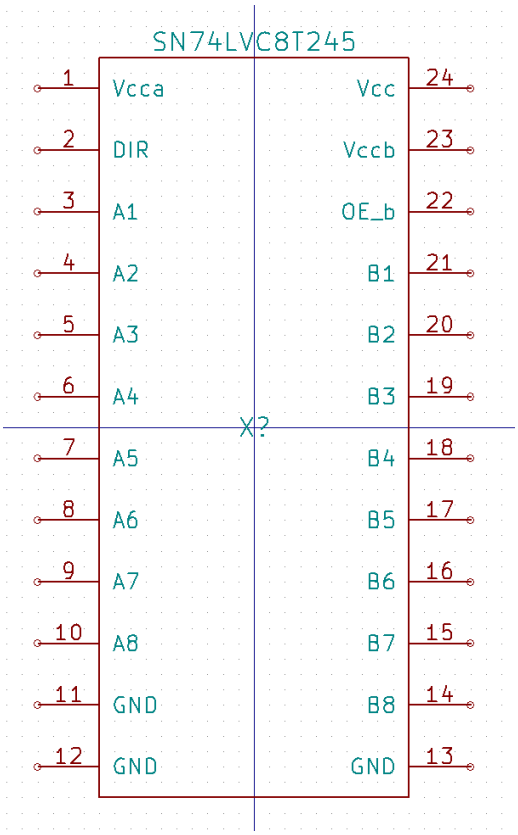

Figure 4.81: Pin layout of SN74LVC8T245

4.21.2 SubCircuit Layout

The figure represents the internal design of the SN74LVC8T245 IC, showing how logic gates and components are interconnected within the chip. This layout determines how the IC processes input signals to generate the required output. Understanding the sub-circuit helps in optimizing circuit performance and ensuring efficient logic operation.

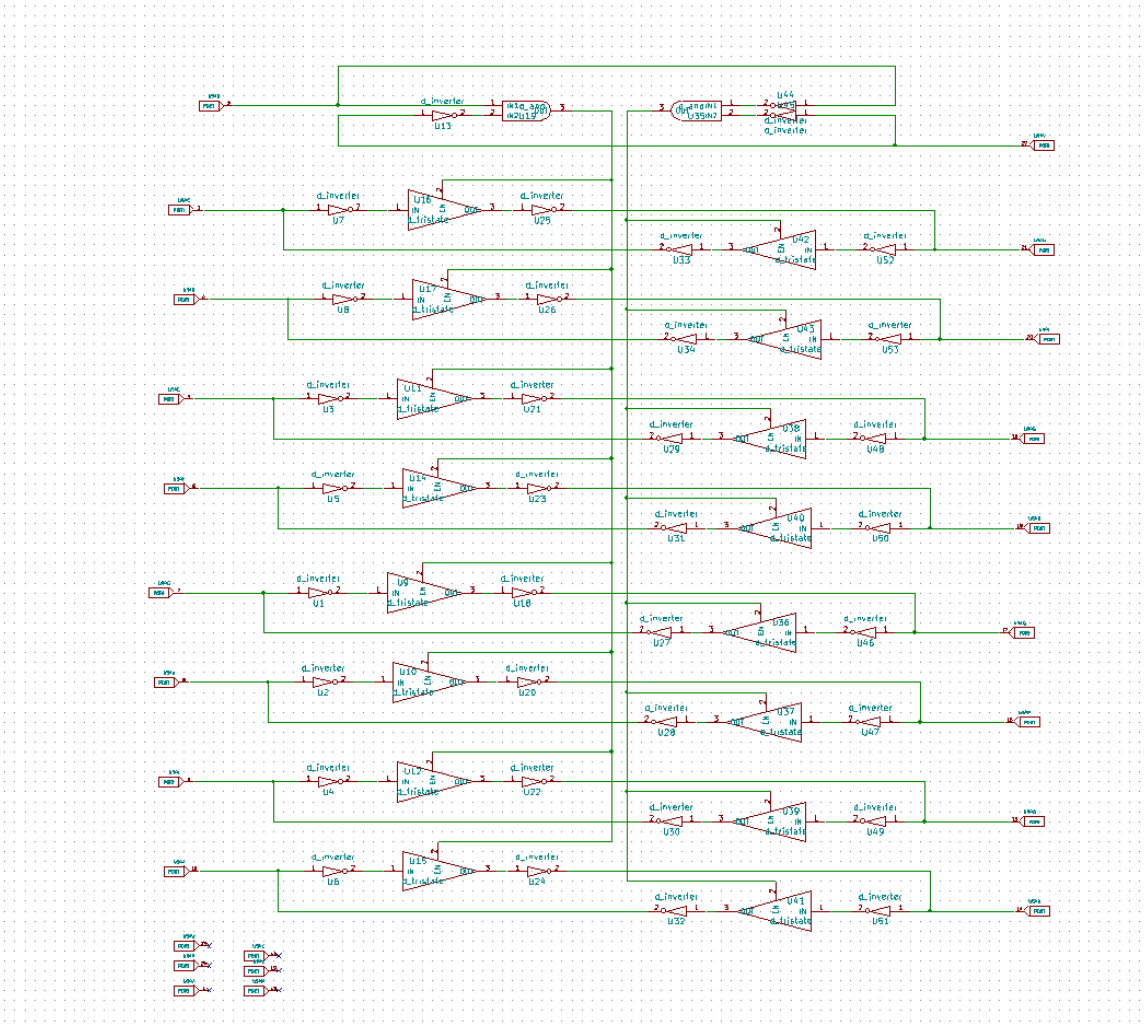

Figure 4.82: Sub Circuit of SN74LVC8T245

4.21.3 Test Circuit

The figure illustrates a test setup used to verify the performance of the SN74LVC8T245 IC. A test circuit includes a power source, input signal generators, and output monitoring devices such as oscilloscopes or logic analyzers. This setup helps evaluate response time, signal integrity, and overall functionality under different conditions.

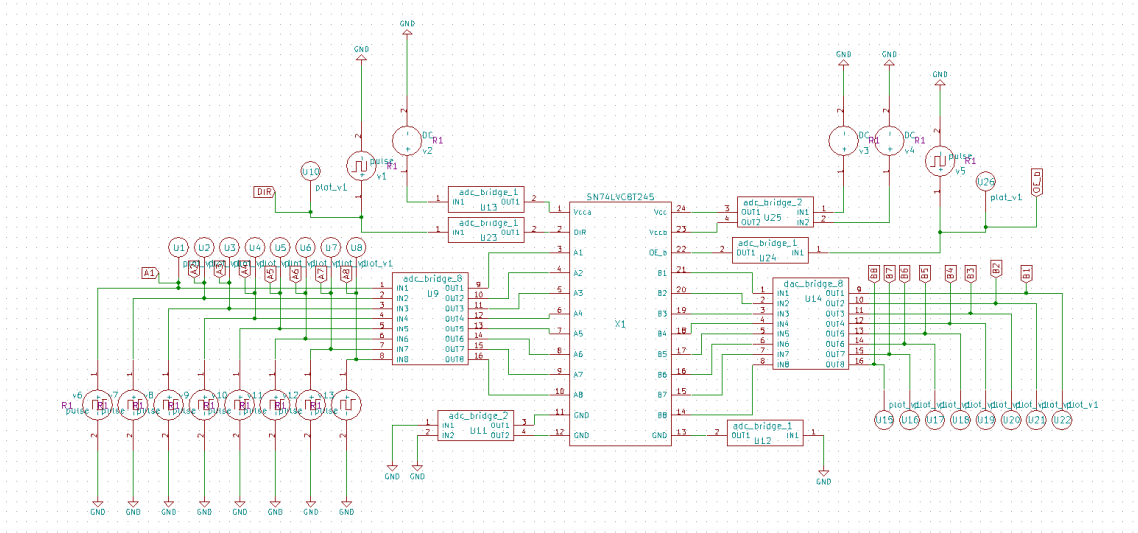

Figure 4.83: Test Circuit of SN74LVC8T245

4.21.4 Output Waveforms

The figure shows the signal produced at the output pin of the SN74LVC8T245 IC after processing the input signals. This waveform represents the NOR logic operation performed by the IC. .

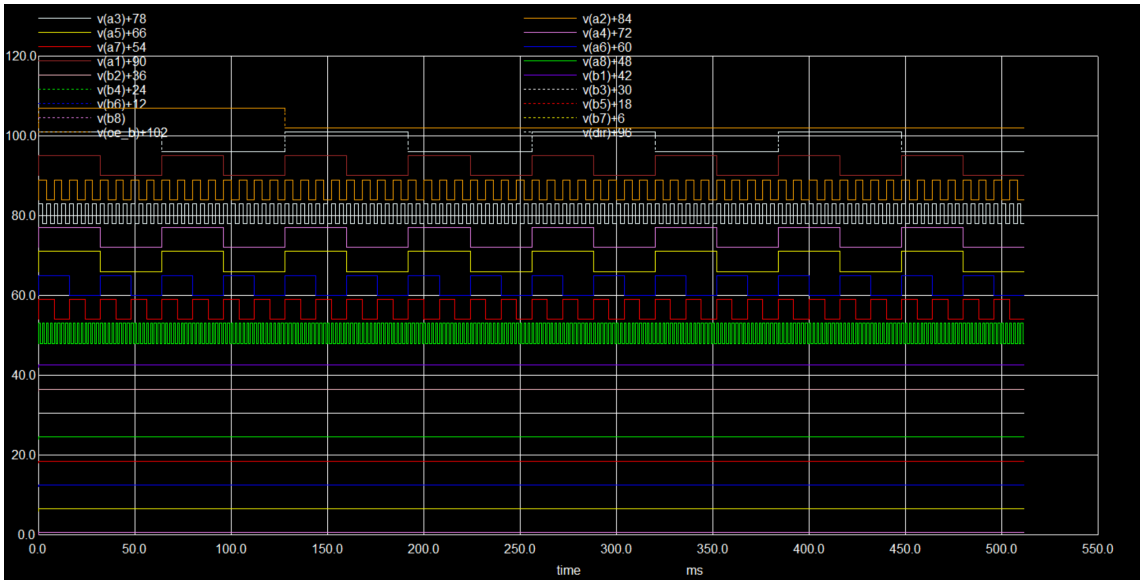

Figure 4.84: Output Waveform of SN74LVC8T245

Chapter 5

Mixed Signal Simulation

5.1 AD5340

5.1.1 Description

The AD5340 is a single-channel, 14-bit, voltage-output Digital-to-Analog Converter (DAC) from Analog Devices. It features a parallel interface and operates from a single supply ranging from 2.5 V to 5.5 V. The DAC provides high-resolution digital-to-analog conversion suitable for precision applications like waveform generation, instrumentation, and control systems.
The device is equipped with a rail-to-rail output amplifier, ensuring the output voltage spans the entire supply range. Data is transferred into the AD5340 via a parallel data bus using standard control pins such as WR (Write), CS (Chip Select), and LDAC (Load DAC). An internal power-on reset circuit ensures that the DAC output powers up to 0 V, and remains there until valid data is written.
The AD5340 offers high accuracy with low INL and DNL errors, and has low power consumption, making it ideal for battery-operated systems. It is available in compact packages such as MSOP and LFCSP, offering a small footprint for space-constrained designs.
This IC is commonly used in industrial process control, data acquisition systems, and automatic test equipment requiring precise analog output control.

Truth Table:

CS	WR	LDAC	Function
L	L	X	Data written to DAC register
X	X	L	DAC output updated from register
H	X	X	DAC disabled (no action)
X	H	X	No write operation

Table 5.1: Control Logic Table for AD5340

5.1.2 Verilog Code

AD5340.v × tbb.v × Untitled 1 ×

D:/Vivado_files/AD5340/AD5340.srcs/sources_1/new/AD5340.v

```
1   `timescale 1ns / 1ps
2
3   module AD5340 (
4       input wire clk,
5       input wire cs_n,
6       input wire wr_n,
7       input wire ldac_n,
8       input wire clr,
9       input wire pd,
10      input wire gain,
11      input wire [11:0] db,
12      output reg [11:0] dac_out
13  );
14
15      reg [11:0] input_reg;
16      reg [11:0] dac_reg;
17      reg wr_n_prev;
18      initial begin
19          input_reg = 12'b0;
20          dac_reg = 12'b0;
21          dac_out = 12'b0;
22          wr_n_prev = 1'b1;
23      end
24      always @(posedge clk) begin
25          wr_n_prev <= wr_n;
26      end
27
28      always @(posedge clk or posedge clr) begin
29          if (clr) begin
30              input_reg <= 12'b0;
```

Figure 5.1: Verilog code for AD5340 (Part 1)

```
AD5340.v × tbb.v × Untitled 1 ×
D:/Vivado_files/AD5340/AD5340.srcs/sources_1/new/AD5340.v
31          dac_reg <= 12'b0;
32          dac_out <= 12'b0;
33      end
34      else begin
35          if (pd) begin
36              dac_out <= 12'b0;
37          end
38          else begin
39              if (cs_n == 1'b0 && wr_n_prev == 1'b0 && wr_n == 1'b1) begin
40                  input_reg <= db;
41              end
42              if (ldac_n == 1'b0) begin
43                  dac_reg <= input_reg;
44              end
45              if (gain == 1'b0) begin
46                  dac_out <= dac_reg;
47              end
48              else begin
49                  if (dac_reg > 2047) begin
50                      dac_out <= 12'd4095;
51                  end
52                  else begin
53                      dac_out <= dac_reg << 1;
54                  end
55              end
56          end
57      end
58  end
59
60  endmodule
```

Figure 5.2: Verilog code for AD5340 (Part 2)

5.1.3 Simulation Waveform

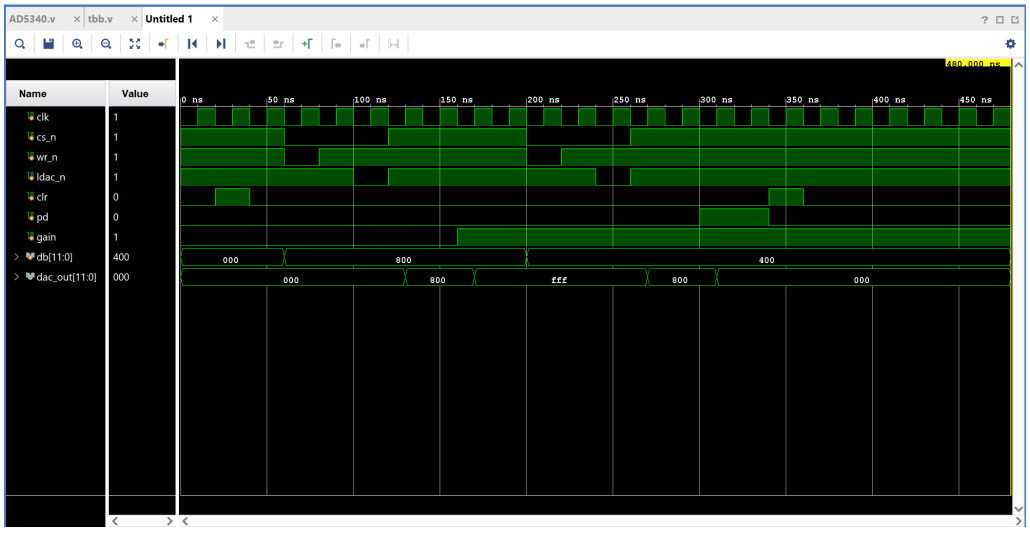

Figure 5.3: Simulation waveform of the AD5340 DAC Verilog implementation showing digital-to-analog output transitions

5.1.4 NgVeri Model

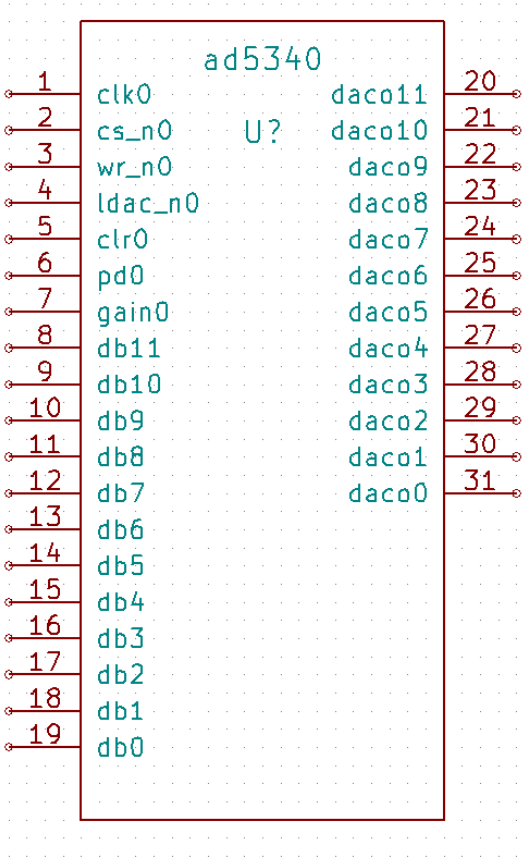

Figure 5.4: Model of the AD5340 DAC after Verilog to NGSpice conversion

5.1.5 Test Circuit

The figure illustrates a test setup used to verify the performance of the AD5340 IC. A test circuit includes a power source, input signal generators, and output monitoring devices such as oscilloscopes or logic analyzers. This setup helps evaluate response time, signal integrity, and overall functionality under different conditions.

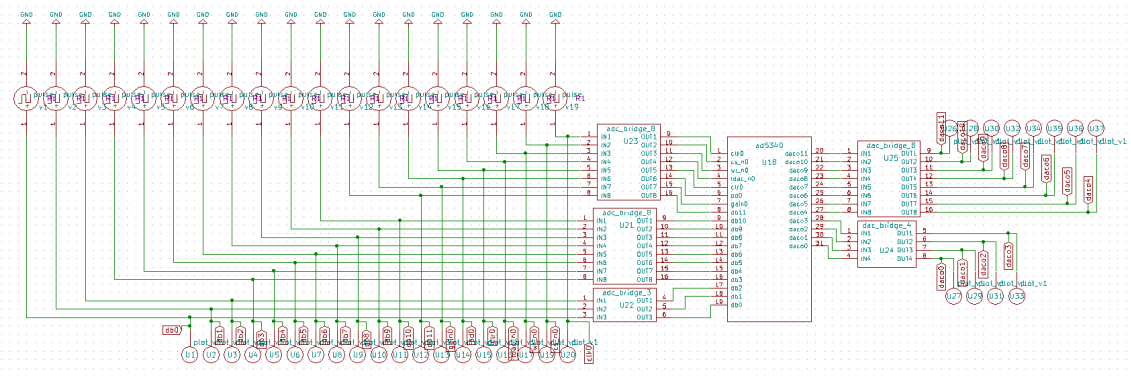

Figure 5.5: Test Circuit of AD5340

5.1.6 NgSpice Simulation Results

The figure shows the signal produced at the output pin of the AD5340 IC after processing the input signals. This waveform represents the NOR logic operation performed by the IC.

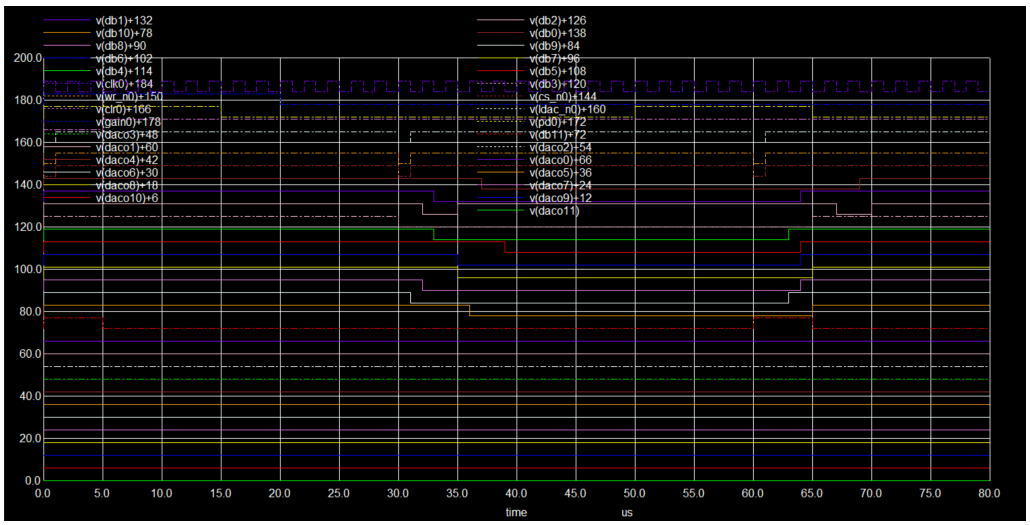

Figure 5.6: Output waveform of the AD5340 DAC showing analog voltage response corresponding to digital input

5.2 8*8 Array Multiplier

5.2.1 Description

An 8×8 array multiplier is a combinational circuit used to multiply two 8-bit binary numbers, producing a 16-bit output. It works by generating all the partial products using AND gates and then summing them in a structured array using adders such as half adders and full adders. Each row of the array corresponds to one bit of the multiplier, and the alignment of partial products follows the binary positional significance. The regular structure of the array makes the design scalable, easy to layout, and suitable for hardware realisation. Due to its parallel nature, the array multiplier provides faster multiplication compared to sequential techniques and is widely used in arithmetic logic units (ALUs), digital signal processors (DSPs), and embedded systems.

- Multiplies two 8-bit binary numbers to produce a 16-bit product.
- Built using basic logic gates (AND) and adders (half and full adders).
- Partial products are generated in parallel and summed in a regular array.
- Suitable for hardware implementation due to modular and regular structure.
- Offers low latency but consumes more area compared to serial multipliers.

- Commonly used in DSP, image processing, and arithmetic-intensive applications.
- Can be pipelined to improve speed in high-performance computing systems.

5.2.2 Verilog Code

Verilog Code: 8×8 Array Multiplier

```
1  `timescale 1ns/1ps
2
3  module array_multiplier_8x8(input [7:0] A, B, output [15:0] z);
4    wire [7:0] p[7:0];
5    genvar i;
6
7    generate
8      for (i = 0; i < 8; i = i + 1) begin: partial
9        assign p[i][0] = A[i] & B[0];
10       assign p[i][1] = A[i] & B[1];
11       assign p[i][2] = A[i] & B[2];
12       assign p[i][3] = A[i] & B[3];
13       assign p[i][4] = A[i] & B[4];
14       assign p[i][5] = A[i] & B[5];
15       assign p[i][6] = A[i] & B[6];
16       assign p[i][7] = A[i] & B[7];
17     end
18   endgenerate
19   wire [149:0] s, c;
20
21   // Bit 0
22   assign z[0] = p[0][0];
23
24   // Bit 1
25   half_adder ha1(p[0][1], p[1][0], z[1], c[0]);
26
27   // Bit 2
28   full_adder fa2a(p[0][2], p[1][1], p[2][0], s[0], c[1]);
29   half_adder ha2(s[0], c[0], z[2], c[2]);
30
```

Figure 5.7: Verilog code for 8×8 Array Multiplier (Part 1)

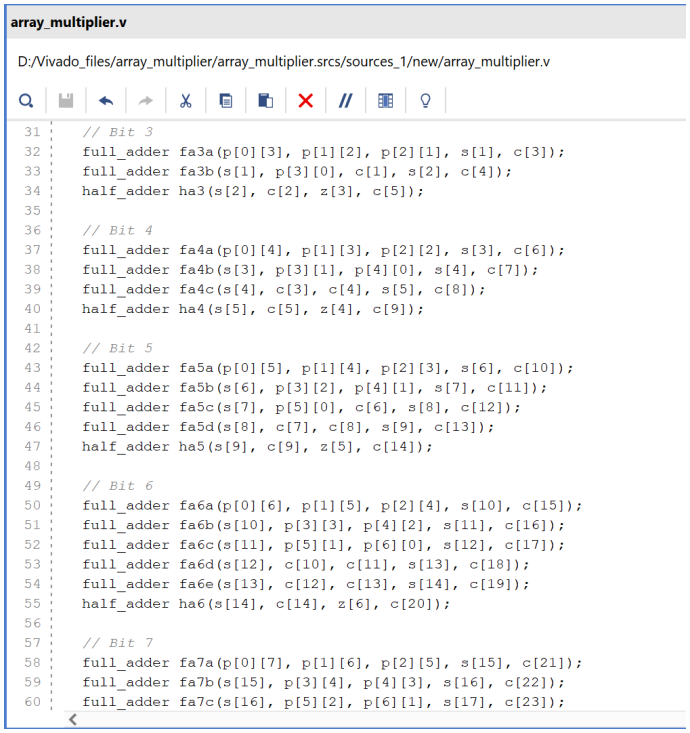

Figure 5.8: Verilog code for 8×8 Array Multiplier (Part 2)

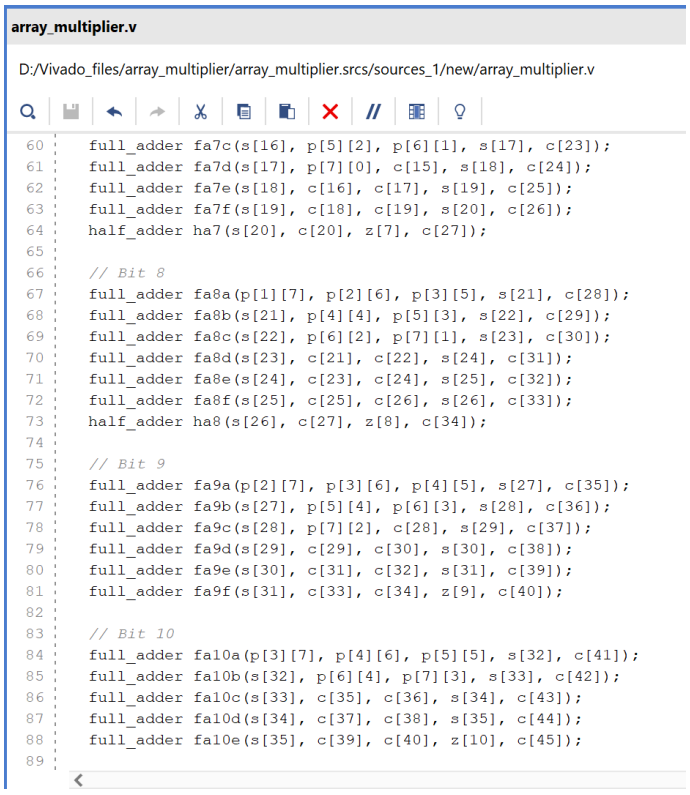

Figure 5.9: Verilog code for 8×8 Array Multiplier (Part 3)

array_multiplier.v

D:/Vivado_files/array_multiplier/array_multiplier.srcs/sources_1/new/array_multiplier.v

```
84    full_adder fa10a(p[3][7], p[4][6], p[5][5], s[32], c[41]);
85    full_adder fa10b(s[32], p[6][4], p[7][3], s[33], c[42]);
86    full_adder fa10c(s[33], c[35], c[36], s[34], c[43]);
87    full_adder fa10d(s[34], c[37], c[38], s[35], c[44]);
88    full_adder fa10e(s[35], c[39], c[40], z[10], c[45]);
89
90    // Bit 11
91    full_adder fa11a(p[4][7], p[5][6], p[6][5], s[36], c[46]);
92    full_adder fa11b(s[36], p[7][4], c[41], s[37], c[47]);
93    full_adder fa11c(s[37], c[42], c[43], s[38], c[48]);
94    full_adder fa11d(s[38], c[44], c[45], z[11], c[49]);
95
96    // Bit 12
97    full_adder fa12a(p[5][7], p[6][6], p[7][5], s[39], c[50]);
98    full_adder fa12b(s[39], c[46], c[47], s[40], c[51]);
99    full_adder fa12c(s[40], c[48], c[49], z[12], c[52]);
100
101   // Bit 13
102   full_adder fa13a(p[6][7], p[7][6], c[50], s[41], c[53]);
103   full_adder fa13b(s[41], c[51], c[52], z[13], c[54]);
104
105   // Bit 14
106   full_adder fa14a(p[7][7], c[53], c[54], z[14], c[55]);
107
108   // Bit 15
109   assign z[15] = c[55];
110
111 endmodule
112
113
```

Figure 5.10: Verilog code for 8×8 Array Multiplier (Part 4)

5.2.3 Simulation Waveform

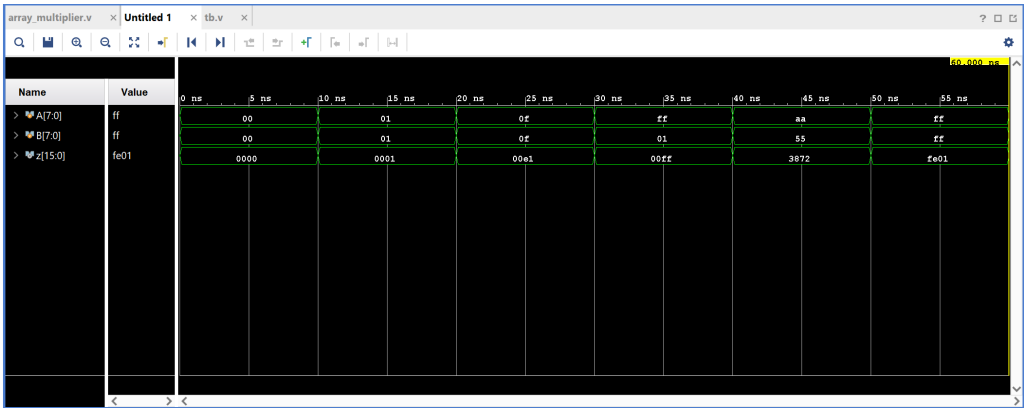

Figure 5.11: Simulation waveform of the 8*8 array multiplier

5.2.4 NgVeri Model

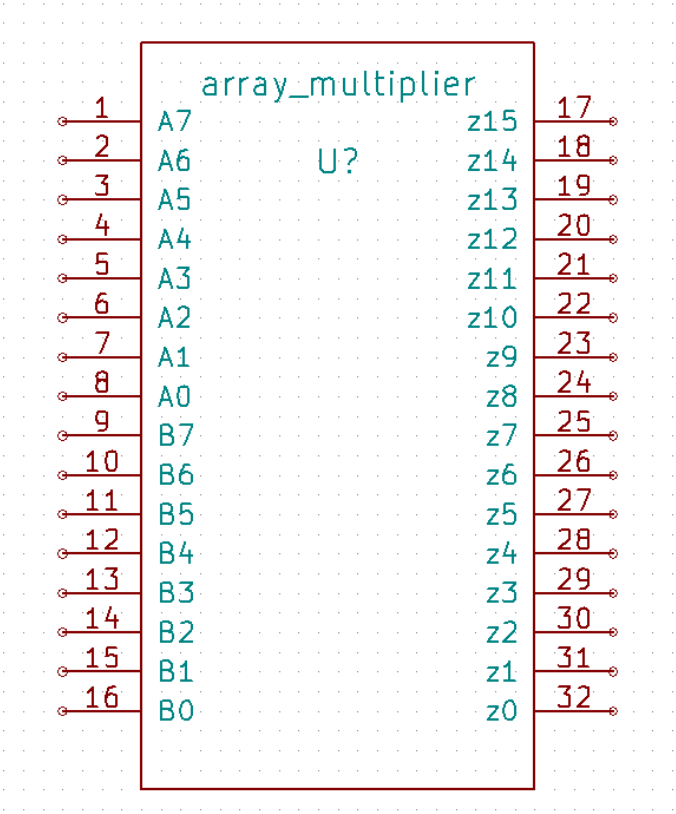

Figure 5.12: Model of the 8*8 Array Multiplier after Verilog to NGSpice conversion

5.2.5 Test Circuit

The figure illustrates a test setup used to verify the performance of the Array Multiplier. A test circuit includes a power source, input signal generators, and output monitoring devices such as oscilloscopes or logic analyzers. This setup helps evaluate response time, signal integrity, and overall functionality under different conditions.

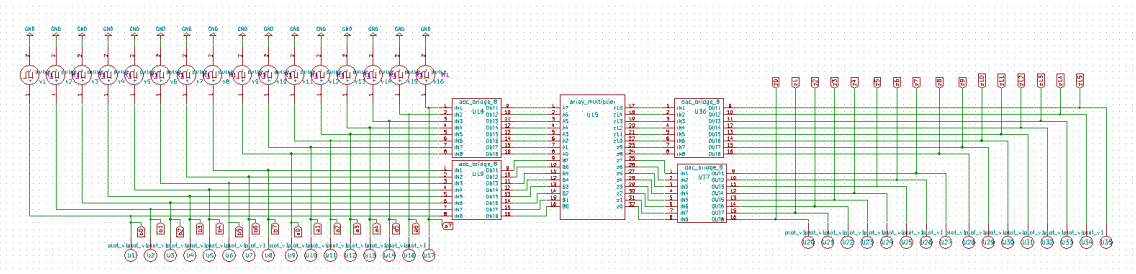

Figure 5.13: Test Circuit of Array Multiplier

5.2.6 NgSpice Simulation Results

The figure shows the signal produced at the output pin of the 8*8 Array Multiplier IC after processing the input signals. This waveform represents the multiplier logic operation performed by the IC.

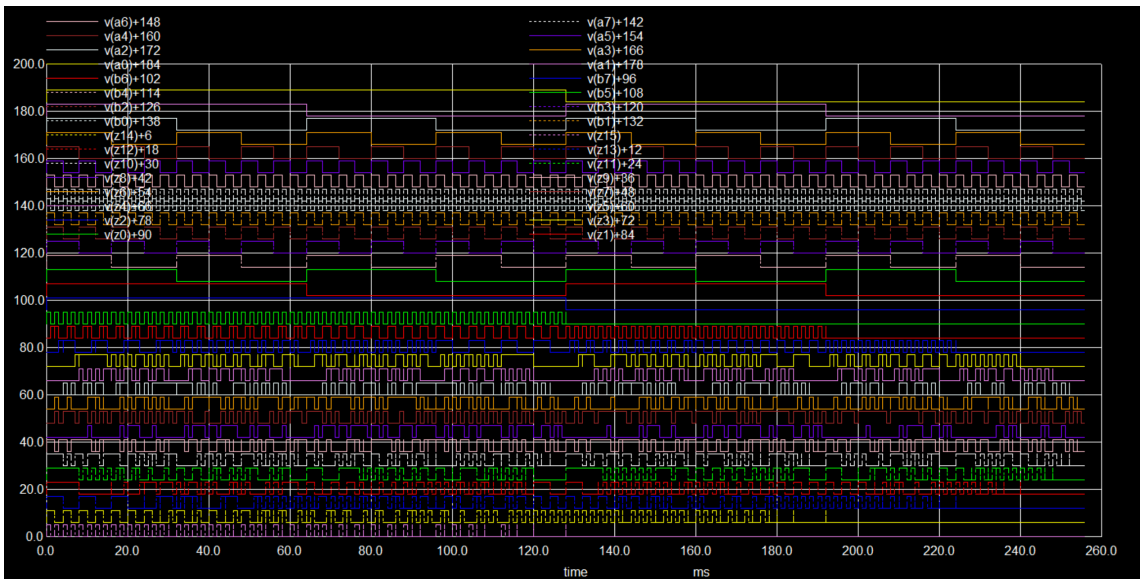

Figure 5.14: Output waveform of the 8*8 Array Multiplier showing multiplication response corresponding to inputs

5.3 4*4 Walace Tree Multiplier

5.3.1 Description

A 4×4 Wallace Tree Multiplier is a fast and efficient combinational circuit used to multiply two 4-bit binary numbers. It is based on the Wallace tree reduction method, which minimizes the number of sequential addition steps required to sum partial products. In this technique, all partial products are generated using AND gates, and then grouped and reduced in parallel using half adders and full adders. The Wallace tree structure significantly reduces the critical path delay by performing additions in a logarithmic fashion, rather than sequentially as in traditional array multipliers.

After reduction, the final two rows of partial sums are added using a conventional carry-propagate adder, producing an 8-bit product. The Wallace tree multiplier provides high-speed multiplication, making it suitable for performance-critical applications such as digital signal processing and graphics processing units (GPUs).

- Multiplies two 4-bit binary numbers to produce an 8-bit output.
- Uses Wallace tree technique to reduce partial products in parallel.
- Requires fewer addition stages compared to array multipliers.

- Reduces critical path delay, improving multiplication speed.
- Uses a combination of AND gates, half adders, and full adders.
- Suitable for high-speed arithmetic units in digital processors.
- Area-efficient for small operand sizes like 4×4.

5.3.2 Verilog Code

Verilog Code: 4×4 Wallace Tree Multiplier

wallace_tree_multiplier.v

D:/Vivado_files/wallace_tree_multiplier/wallace_tree_multiplier.srcs/sources_1/new/wallace_tree_multiplier.v

```
1  `timescale 1ns / 1ps
2
3  module half_adder(input a, b, output s0, c0);
4    assign s0 = a ^ b;
5    assign c0 = a & b;
6  endmodule
7
8  module full_adder(input a, b, cin, output s0, c0);
9    assign s0 = a ^ b ^ cin;
10   assign c0 = (a & b) | (b & cin) | (a & cin);
11 endmodule
12
13 // Wallace Tree Multiplier with signed A and unsigned B
14 module wallace_tree_multiplier(input [3:0] A, B, output [7:0] z);
15   wire [7:0] M;
16   assign M = { {4{A[3]}}, A }; // Sign-extend A to 8 bits
17
18   wire p[0:7][0:3];
19
20   genvar i, j;
21
22   // Generate partial products for M[0] to M[3]
23   generate
24     for (i = 0; i < 4; i = i + 1) begin : gen_row1
25       for (j = 0; j < 4; j = j + 1) begin : gen_col1
26         assign p[i][j] = M[i] & B[j];
27       end
28     end
29   endgenerate
30
```

Figure 5.15: Verilog code for 4×4 Wallace Tree Multiplier (Part 1)

wallace_tree_multiplier.v *

D:/Vivado_files/wallace_tree_multiplier/wallace_tree_multiplier.srcs/sources_1/new/wallace_tree_multiplier.v

```
31    generate
32      for (j = 0; j < 4; j = j + 1) begin : gen_row2
33        assign p[4][j] = M[4] & B[j];
34      end
35      for (j = 0; j < 3; j = j + 1) begin : gen_row3
36        assign p[5][j] = M[5] & B[j];
37      end
38      for (j = 0; j < 2; j = j + 1) begin : gen_row4
39        assign p[6][j] = M[6] & B[j];
40      end
41    endgenerate
42    assign p[7][0] = M[7] & B[0];
43
44    wire [17:0] c;
45    wire [10:0] s;
46
47    assign z[0] = p[0][0];
48
49    // Stage 1
50    half_adder h0(p[0][2], p[1][1], s[0], c[0]);
51
52    full_adder fg0_0(p[0][3], p[1][2], p[2][1], s[1], c[1]);
53    full_adder fg0_1(p[1][3], p[2][2], p[3][1], s[2], c[2]);
54    full_adder fg0_2(p[2][3], p[3][2], p[4][1], s[3], c[3]);
55    full_adder fg0_3(p[3][3], p[4][2], p[5][1], s[4], c[4]);
56    full_adder fg0_4(p[4][3], p[5][2], p[6][1], s[5], c[5]);
57
58    // Stage 2
59    half_adder h1(s[1], p[3][0], s[6], c[6]);
60
```

Figure 5.16: Verilog code for 4×4 Wallace Tree Multiplier (Part 2)

wallace_tree_multiplier.v *

D:/Vivado_files/wallace_tree_multiplier/wallace_tree_multiplier.srcs/sources_1/new/wallace_tree_multiplier.v

```
47    assign z[0] = p[0][0];
48
49    // Stage 1
50    half_adder h0(p[0][2], p[1][1], s[0], c[0]);
51
52    full_adder fg0_0(p[0][3], p[1][2], p[2][1], s[1], c[1]);
53    full_adder fg0_1(p[1][3], p[2][2], p[3][1], s[2], c[2]);
54    full_adder fg0_2(p[2][3], p[3][2], p[4][1], s[3], c[3]);
55    full_adder fg0_3(p[3][3], p[4][2], p[5][1], s[4], c[4]);
56    full_adder fg0_4(p[4][3], p[5][2], p[6][1], s[5], c[5]);
57
58    // Stage 2
59    half_adder h1(s[1], p[3][0], s[6], c[6]);
60
61    full_adder fg1_0(s[2], p[4][0], c[1], s[7], c[7]);
62    full_adder fg1_1(s[3], p[5][0], c[2], s[8], c[8]);
63    full_adder fg1_2(s[4], p[6][0], c[3], s[9], c[9]);
64    full_adder fg1_3(s[5], p[7][0], c[4], s[10], c[10]); // c[10] not used further
65
66    // Final stage additions for z[1] to z[7]
67    half_adder h2(p[0][1], p[1][0], z[1], c[11]);
68    full_adder f9(s[0], p[2][0], c[11], z[2], c[12]);
69    full_adder f10(s[6], c[0], c[12], z[3], c[13]);
70    full_adder f11(s[7], c[6], c[13], z[4], c[14]);
71    full_adder f12(s[8], c[7], c[14], z[5], c[15]);
72    full_adder f13(s[9], c[8], c[15], z[6], c[16]);
73    full_adder f14(s[10], c[9], c[16], z[7], c[17]);
74  endmodule
75
76
```

Figure 5.17: Verilog code for 4×4 Wallace Tree Multiplier (Part 3)

5.3.3 Simulation Waveform

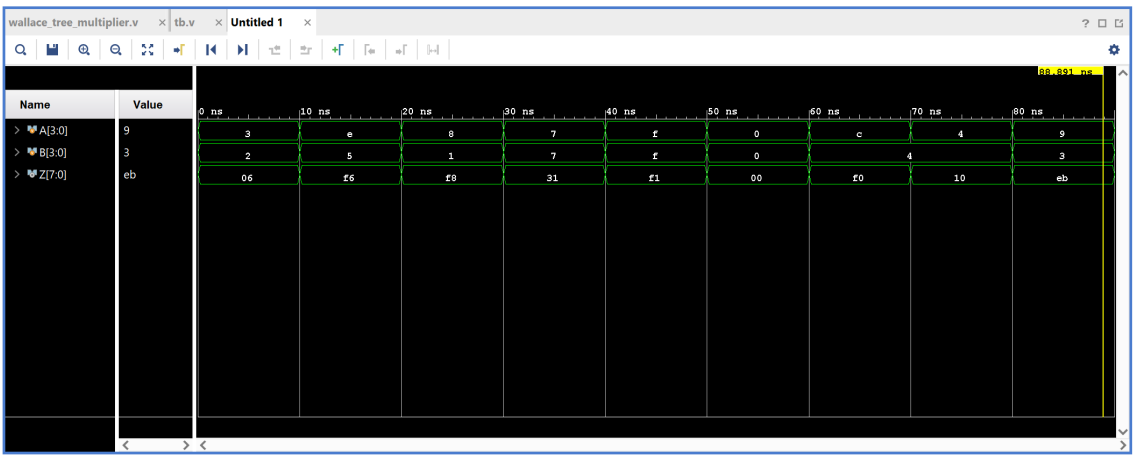

Figure 5.18: Simulation waveform of the 4*4 wallace tree multiplier

5.3.4 NgVeri Model

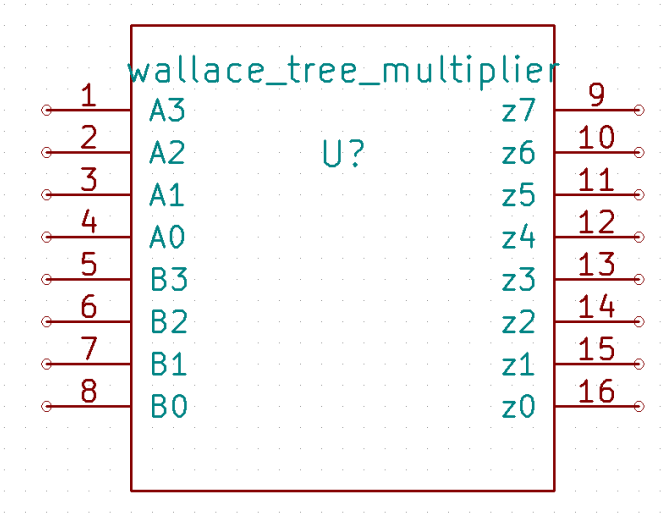

Figure 5.19: Model of the 4*4 Wallace Tree Multiplier after Verilog to NGSpice conversion

5.3.5 Test Circuit

The figure illustrates a test setup used to verify the performance of the 4*4 Wallace tree multiplier. A test circuit includes a power source, input signal generators, and output monitoring devices such as oscilloscopes or logic analyzers. This setup helps evaluate response time, signal integrity, and overall functionality under different conditions.

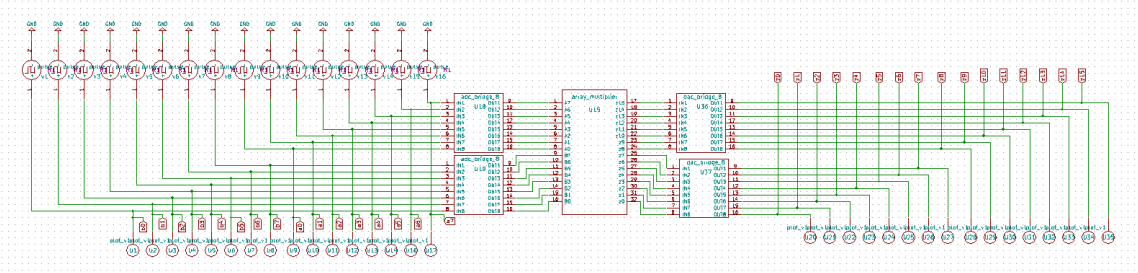

Figure 5.20: Test Circuit of 4*4 wallace tree multiplier

5.3.6 NgSpice Simulation Results

The figure shows the signal produced at the output pin of the 4*4 Wallace tree multiplier IC after processing the input signals. This waveform represents the multiplier logic operation performed by the IC.

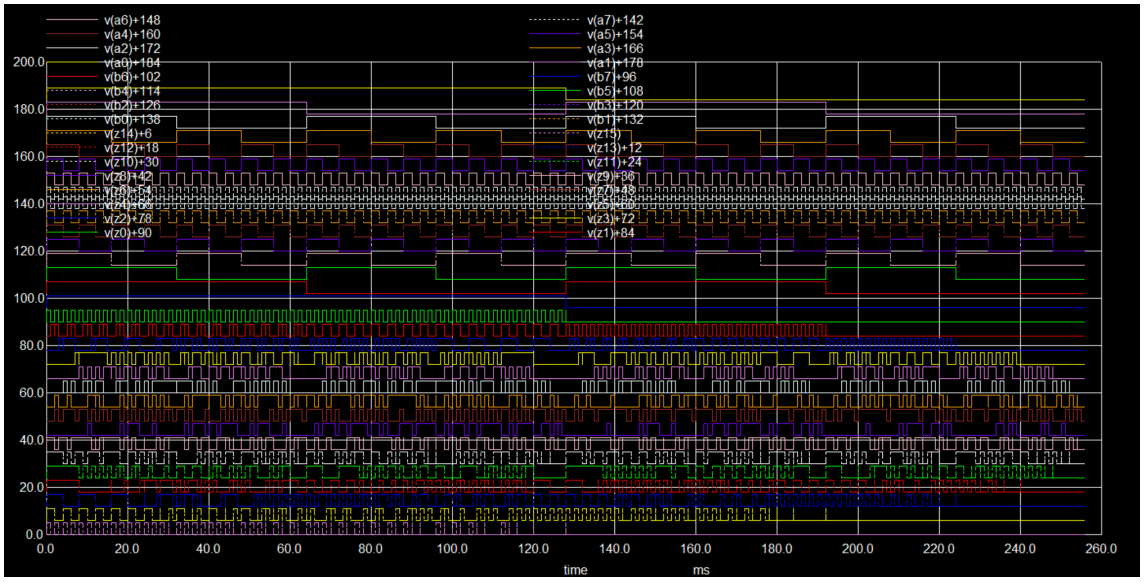

Figure 5.21: Output waveform of the 4*4 Wallace tree multiplier showing multiplication response corresponding to inputs

Chapter 6

Conclusion and Future Scope

Conclusion and Future Scope

During the FOSSEE Summer Fellowship at IIT Bombay, I was involved in two key tasks—Integrated Circuit Design using the subcircuit feature of eSim and Mixed-Signal Simulation in eSim. These tasks provided a hands-on understanding of digital and analog circuit integration within open-source simulation environments. Through this, I gained proficiency in implementing various logic ICs using Verilog, simulating their behavior, and verifying output waveforms through NGSpice and GTKWave. The subcircuit feature enabled hierarchical design and modular analysis of complex circuits, while mixed-signal simulation bridged the gap between analog device behavior and digital control logic.

Additionally, I was introduced to the fundamentals of device modeling, which enriched my understanding of how physical semiconductor parameters influence circuit performance. This experience deepened my appreciation of the relationship between hardware description languages, SPICE-level simulation, and real-world circuit characteristics.

As a future scope, this work can be extended toward large-scale digital system design, custom IC layout, and performance analysis using open-source EDA tools. Advancing to parameterized device modeling, power-delay optimization, and FPGA-based prototyping would provide further insight into the real-time behavior of integrated systems. This foundation also opens pathways to research in VLSI design, analog-digital co-design, and system-level verification.

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