# Summer Fellowship Report

On

**Integrated Circuit Design using Subcircuit feature of eSim**
**& Mixed Signal Simulation in eSim**
**& Device Modelling in eSim**

Submitted by

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# Acknowledgment

I take this opportunity to express my deepest gratitude to the entire FOSSEE team at IIT Bombay for providing me with this wonderful opportunity to work on the design and integration of sub-circuits using eSim and Device Modelling. The internship has given me valuable exposure to open-source tools, their real-world applications, and a deeper understanding of electronic design and simulation.

I am especially grateful to Prof. Kannan M. Moudgalya for his constant inspiration and vision behind the FOSSEE initiative. His commitment towards promoting open-source software for education and research has created numerous opportunities for students like me to gain hands-on experience and contribute to the open-source community. His farsighted leadership and encouragement have been truly motivating throughout this journey.

I would like to convey my heartfelt thanks to Mr. Sumanto Kar for his constant support, guidance, and encouragement throughout the internship. His valuable insights, timely feedback, and patient mentoring have been instrumental in helping me overcome challenges and successfully complete my project objectives. His dedication towards guiding interns like me has made this journey both enlightening and enjoyable

I also sincerely appreciate the entire FOSSEE initiative for its efforts in empowering students and researchers by making tools freely accessible, thus removing the barriers imposed by costly commercial software. This mission not only fosters innovation but also strengthens the open-source ecosystem, allowing young learners to actively contribute and grow.

This internship has been a memorable and rewarding phase of my academic journey. The knowledge, skills, and experiences I have gained will undoubtedly serve as a strong foundation as I move forward in my career in the semiconductor and VLSI domain.

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# Chapter 1

# Introduction

The advancement of Electronic Design Automation (EDA) tools has revolutionized the way electronic circuits are designed, simulated, and verified. Among these, open-source tools play a crucial role in making advanced EDA capabilities accessible to students, educators, and researchers without the burden of expensive licenses. The FOSSEE project [1] at IIT Bombay has taken significant steps to promote such open-source tools globally.

One of the key open-source tools developed and promoted under FOSSEE is **eSim**, which integrates multiple open-source EDA tools to provide a unified platform for circuit design, simulation, and PCB layout. Various tools like NgSpice, Makerchip, and KiCad work together under eSim to offer a complete design environment.

## 1.1 eSim

eSim is an open-source Electronic Design Automation (EDA) tool developed by FOSSEE, IIT Bombay. The primary objective of eSim is to provide a completely free and open-source alternative to commercial circuit design and simulation software, thereby reducing dependency on expensive proprietary tools in academia and research.[2]

eSim integrates multiple open-source tools to provide a comprehensive design and simulation environment. **KiCad** is used for schematic capture and PCB design, while **NgSpice** performs analog circuit simulation. For digital simulation, **GHDL** is integrated, supporting VHDL based designs, and **Makerchip** enables online Transaction Level Verilog (TL-Verilog) based digital design and verification. Python support is also available in eSim, allowing users to perform customized simulations, generate netlists.

One of the key features of eSim is its **Subcircuit feature**, which allows complex designs to be modularized into reusable blocks, simplifying the design of large systems. Additionally, eSim supports device modeling, enabling users to define and simulate custom semiconductor devices using real-world parameters. As part of its continuous development, eSim also supports **SkyWater SKY130 PDK**, allowing users to perform simulations using an open-source 130nm Process Design Kit, which is widely used for analog, mixed-signal, and digital IC design research.

By supporting a fully open-source toolchain, eSim empowers students, educators, and researchers to gain hands-on experience with industry-relevant EDA tools and contribute actively to the open-source hardware ecosystem.

## 1.2 NgSpice

NgSpice is an open-source circuit simulator integrated into eSim for performing analog and mixed-signal simulations. Based on the SPICE simulation engine, NgSpice supports DC, AC, transient, and parametric analyses, making it suitable for analyzing a wide range of circuits.[3]

It allows users to simulate circuit behavior using industry-standard SPICE models, including support for subcircuits and behavioral modeling. In eSim, NgSpice works as the backend simulator for schematics created using KiCad, providing waveform outputs for voltage, current, and frequency responses. Its flexibility and accuracy make it a powerful tool for verifying designs before hardware implementation.

## 1.3 Makerchip

Makerchip is an integrated platform designed to simplify digital circuit design by offering both browser-based and desktop-based environments for coding, simulating, and debugging digital hardware designs. It supports multiple hardware description languages including Verilog, SystemVerilog, and Transaction-Level Verilog (TL-Verilog), allowing flexibility for users at various levels of expertise.[4]

In eSim, Makerchip is interfaced through a Python-based application called Makerchip-App, which seamlessly launches the Makerchip IDE for digital design and verification. The platform integrates several open-source and proprietary tools to provide a rich set of features such as real-time simulation, waveform viewing, and code linting, thereby improving design accuracy and productivity.

## 1.4 KiCad

KiCad is an open-source PCB design and schematic capture tool integrated within eSim for creating circuit schematics and generating PCB layouts. It allows users to design multi-layer boards, define custom footprints, and perform design rule checks to ensure design correctness before fabrication.[5]

In eSim, KiCad acts as the primary schematic editor, allowing users to graphically build circuits by placing and interconnecting components from extensive open-source libraries. The designed schematics can directly be used for both simulation and PCB layout generation. KiCad also supports features such as 3D visualization of PCBs, Gerber file export for manufacturing, and electrical rule checking to identify design issues early. Its seamless integration within eSim enables a smooth transition from schematic design to simulation and physical realization, offering a complete design-to-fabrication workflow entirely within an open-source environment.

## 1.5 GHDL

GHDL is an open-source simulator for VHDL, a hardware description language widely used in digital circuit design. It supports the complete IEEE VHDL standard, allowing designers to simulate, verify, and debug VHDL-based digital systems effectively.[6]

In eSim, GHDL is integrated to enable digital simulation alongside analog simulation provided by NgSpice. Users can model digital circuits using VHDL, which are then simulated using GHDL to verify logical functionality and timing behavior. This integration allows eSim to handle mixed-signal designs, where the analog components are simulated by NgSpice and the digital components by GHDL, providing a comprehensive platform for complex system design. The combination of these tools allows designers to validate both analog and digital subsystems within a unified simulation environment.

# Chapter 2

# Features of eSim

eSim offers a comprehensive set of features that make it a powerful open-source alternative for electronic design automation. Some of the key features include:

- **Open-source and Free**: eSim is fully open-source, allowing unrestricted access without licensing costs, making it ideal for academic and research purposes.
- **Integrated Toolchain**: Combines multiple open-source tools such as KiCad for schematic capture and PCB design, NgSpice for analog simulation, GHDL for digital simulation, and Makerchip for advanced digital design.
- **Mixed-Signal Simulation**: Supports both analog and digital simulation, allowing users to design and simulate mixed-signal circuits efficiently.
- **Subcircuit Feature**: Enables hierarchical and modular design by allowing complex circuits to be broken into reusable subcircuits.
- **Device Modeling**: Supports custom device modeling, allowing users to simulate real-world semiconductor devices using user-defined parameters.
- **SkyWater SKY130 PDK Support**: Provides access to open-source 130nm process design kit for IC design and simulation.
- **Python Integration**: Allows automation, scripting, and advanced analysis using Python interfaces.
- **User-Friendly Interface**: Offers an intuitive GUI that simplifies circuit creation, simulation setup, and result analysis, making it suitable for both beginners and advanced users.
- **Cross-Platform Support**: Compatible with major operating systems like Linux and Windows.
- **Active Community and Documentation**: Extensive documentation, tutorials, and community support provided through FOSSEE ensure smooth learning and troubleshooting.

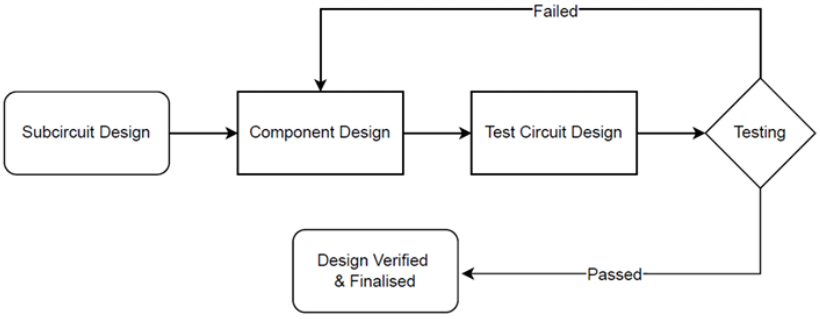
# Chapter 3

# Problem Statement

The objective of this project is to design and develop Digital Integrated Circuits using the Subcircuit feature of eSim, create Device Models using the Model Editor tool, and perform Mixed-Signal Simulation using NGVeri. The developed models enhance the eSim library and extend its functionality for future academic and industrial applications.

## 3.1 Subcircuit Design and Integration

Digital ICs are modeled as subcircuits based on datasheet specifications and integrated into eSim's subcircuit library.



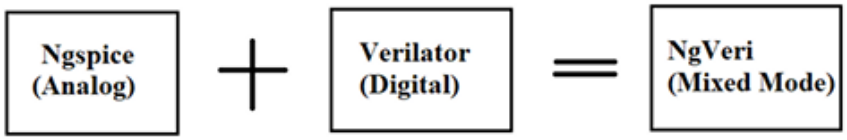

### 3.1.1 Approach

- **Datasheet Analysis**: Datasheets from various manufacturers are studied to extract internal circuit diagrams, truth tables, pin configurations, and functional blocks.
- **Subcircuit Creation**: The extracted circuits are implemented using eSim's schematic editor with available device models from eSim's internal library.
- **Symbol Creation**: Custom IC symbols are created according to package type and pin configuration for correct circuit integration.

- **Test Circuit Design**: Standard test circuits are designed as per datasheet test conditions to validate subcircuit functionality.
- **Simulation and Validation**: NgSpice is used to simulate the test circuits, and the results are compared against reference plots from datasheets.

## 3.2 Mixed-Signal Simulation using NGVeri

This part involves using eSim's NGVeri feature for mixed-signal simulation by integrating analog circuits with Verilog digital designs. NGVeri allows simultaneous simulation of analog (NgSpice) and digital (Verilator) domains.

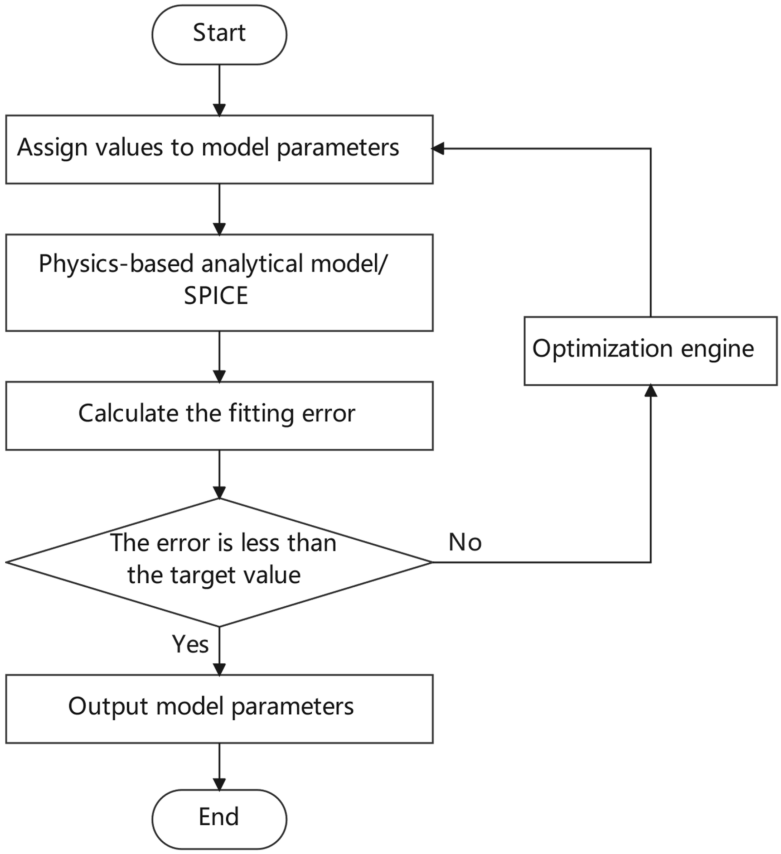



### 3.2.1 Approach

- **Verilog Code Development**: The digital design was first written using Verilog, SystemVerilog or TL-Verilog depending on the requirement.
- **Code Verification using Icarus Verilog**: The Verilog code was initially verified using Icarus Verilog to ensure functionality before integration.
- **Makerchip IDE (optional)**: Additional verification was carried out using Makerchip IDE for debugging and simulation.
- **NGVeri Model Creation**: Once verified, the Verilog files were imported into NGVeri, where TL-Verilog (if used) was converted into SystemVerilog using SandPiper SaaS, and finally compiled using Verilator to generate the NGVeri model.
- **Analog Circuit Design**: The analog portion of the circuit was designed in eSim's schematic editor using KiCad interface.
- **Mixed-Signal Simulation**: The complete mixed-signal simulation was performed using NgVeri with NgSpice and Verilator, and the outputs were verified using eSim's plotting and NgSpice.

## 3.3 Device Modeling using Model Editor

Device models are created for components where SPICE models are not available, using eSim's built-in Model Editor. This allows users to manually define device parameters extracted from datasheets or calculated using standard equations. The Model Editor generates corresponding XML model files, which are integrated into eSim for simulation and verification. This feature ensures flexibility in modeling custom devices when predefined models are not provided by manufacturers.




### 3.3.1 Approach

- **Parameter Extraction**: Device parameters like saturation current, ideality factor, capacitances, and breakdown voltage are extracted from datasheets or calculated.
- **Model File Creation**: The extracted parameters are entered into eSim's Model Editor manually to generate device XML files.
- **Test Circuit Design**: Test circuits are created to validate the newly modeled devices under typical operating conditions.
- **Simulation and Validation**: The designed test circuits are simulated using NgSpice, and the results are compared with datasheet characteristics to verify accuracy.

# Chapter 4

# Subcircuit Design and Integration

The Subcircuit feature of eSim allows hierarchical modeling of complex Integrated Circuits by combining multiple basic components into a single reusable block. By utilizing datasheets and internal schematics of various ICs, accurate subcircuit models are created using eSim's schematic editor.

## 4.1 SN74LVC4245A

**Description:** Octal Bus Transceiver and 3.3V to 5V Level Shifter with 3-state outputs.

### 4.1.1 General Description

The **SN74LVC4245A** is an 8-bit (octal) bidirectional voltage-level translator and bus transceiver designed by Texas Instruments. It facilitates asynchronous communication between data buses operating at different voltage levels, specifically between 3.3 V and 5 V systems. The device features two separate supply rails: $V_{CCA}$ (5 V) for the A port and $V_{CCB}$ (3.3 V) for the B port.[8]

### 4.1.2 Features

**Core Functionality :**

- **Bidirectional Voltage-Level Translator:**
  - Converts signals between 5V (A port) and 3.3V (B port).
  - Supports asynchronous data transfer in both directions.
- **Octal Bus Transceiver:**
  - 8-bit non-inverting data path.
  - Direction controlled by the **DIR** pin:
    - `DIR = L`: B $\rightarrow$ A data transfer.
    - `DIR = H`: A $\rightarrow$ B data transfer.

- **3-State Outputs:**
  - Output-enable ($\overline{OE}$) pin isolates buses when disabled (high).
  - High-impedance state prevents bus contention.
- **Supply Rail Separation:**
  - Independent $V_{CCA}$ (5 V) and $V_{CCB}$ (3.3 V) supplies.

**Control Logic**

| Inputs | Operation |
|---|---|
| $\overline{OE} = L$, DIR = L | B data → A bus |
| $\overline{OE} = L$, DIR = H | A data → B bus |
| $\overline{OE} = H$ (X = don't care) | Isolation (high-Z) |

### 4.1.3 Subcircuit

Below is the subcircuit implementation for the `SN74LVC4245A` octal bus transceiver, demonstrating bidirectional voltage translation between 3.3V and 5V logic levels. The design features direction-controlled data flow and 3-state output isolation.

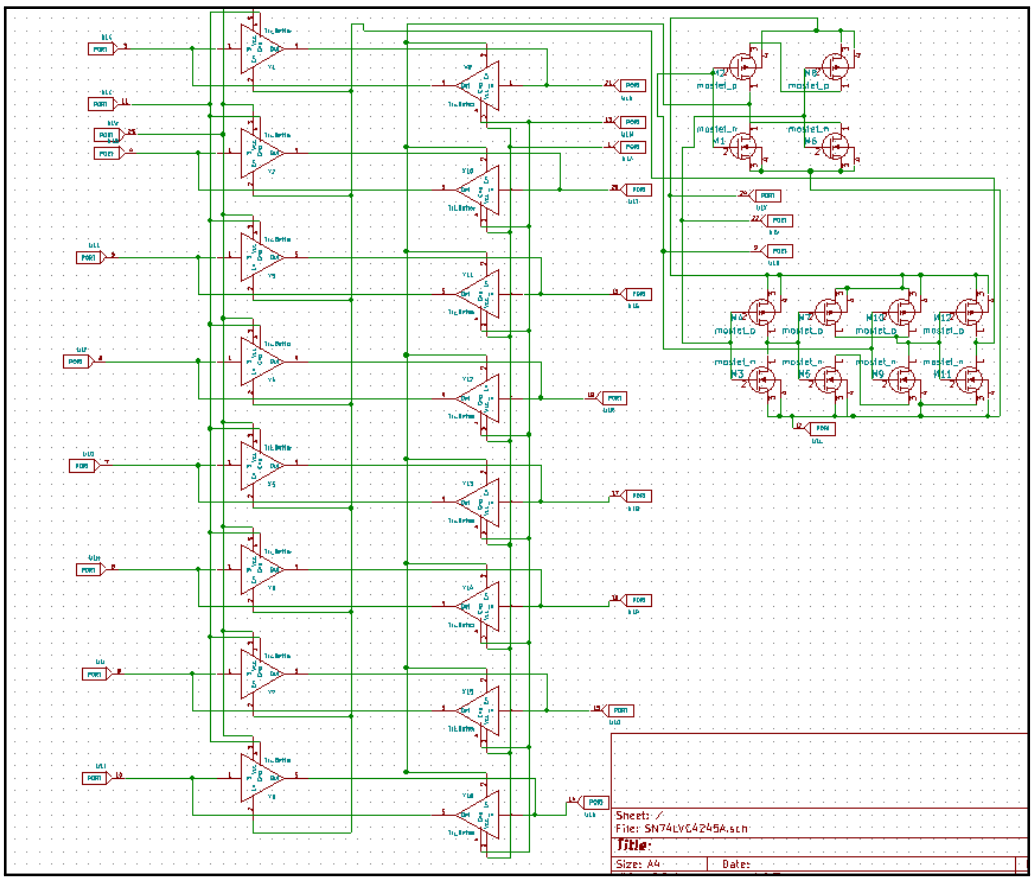



Figure 4.1: Subcircuit of SN74LVC4245A

The schematic shown above represents a hierarchical subcircuit consisting of multiple Tri-State Buffer elements arranged to form a controlled signal routing structure. Each buffer component is itself a custom subcircuit embedded within the main module.

The subcircuit schematic for the Tri State Buffer is as follows:

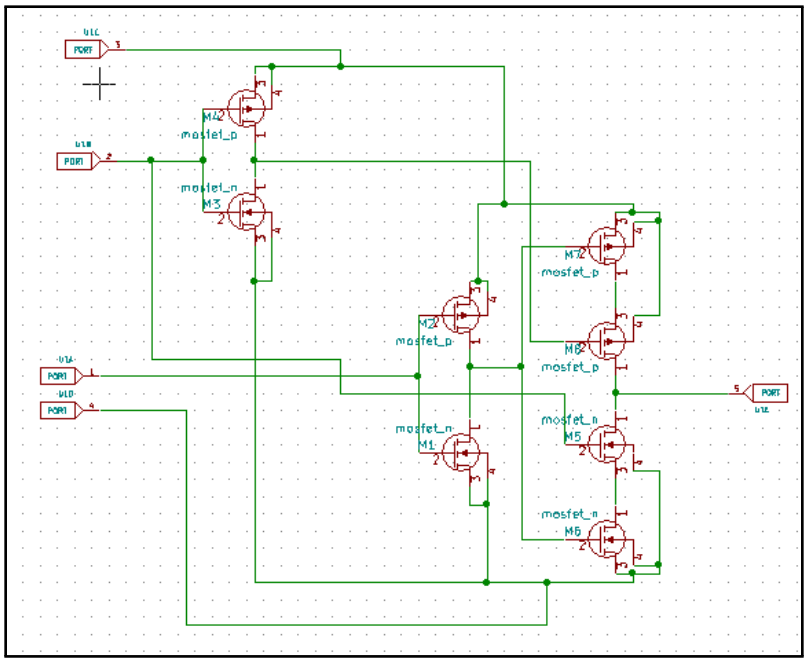



Figure 4.2: Subcircuit of SN74LVC4245A

The package symbol for the subcircuit, Tri State Buffer is as follows:

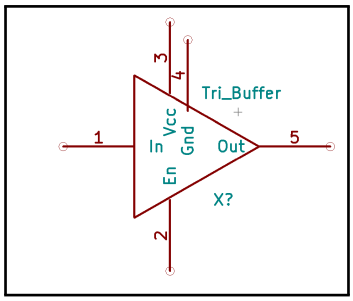



Figure 4.3: Subcircuit of SN74LVC4245A

### 4.1.4 IC Package

Below is the physical package configuration for the SN74LVC4245A, illustrating the pinout arrangement and mechanical layout.

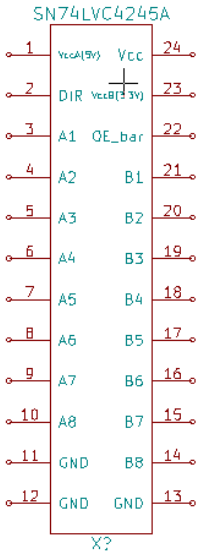



Figure 4.4: IC Layout of SN74LVC4245A

### 4.1.5 Test Circuit

Below is the test circuit configuration for the SN74LVC4245A, designed to validate bidirectional voltage translation and 3-state functionality. The setup includes all necessary signal conditioning and measurement points.

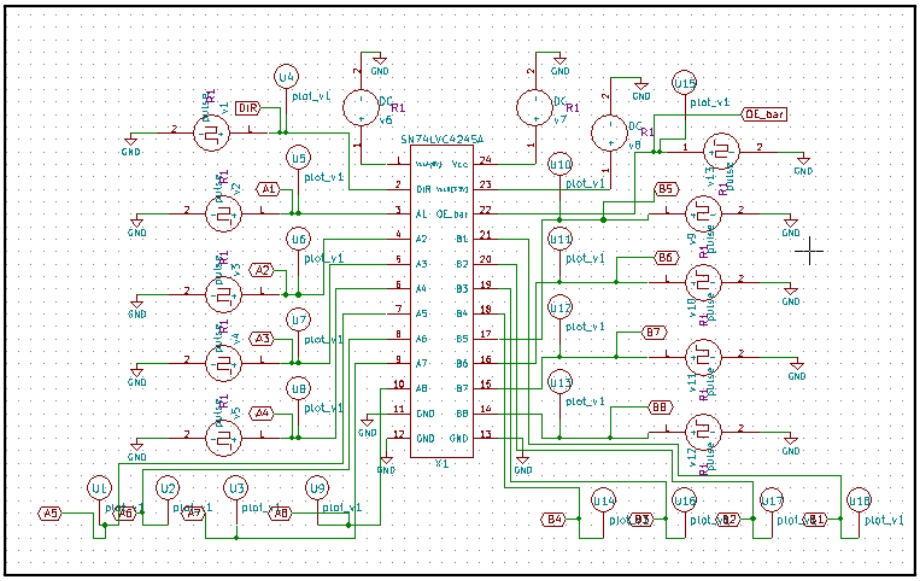



Figure 4.5: Test Circuit of SN74LVC4245A

### 4.1.6 NgSpice Simulation Results

Below are the NGspice simulation results for the `SN74LVC4245A` test circuit, validating bidirectional level-shifting performance.

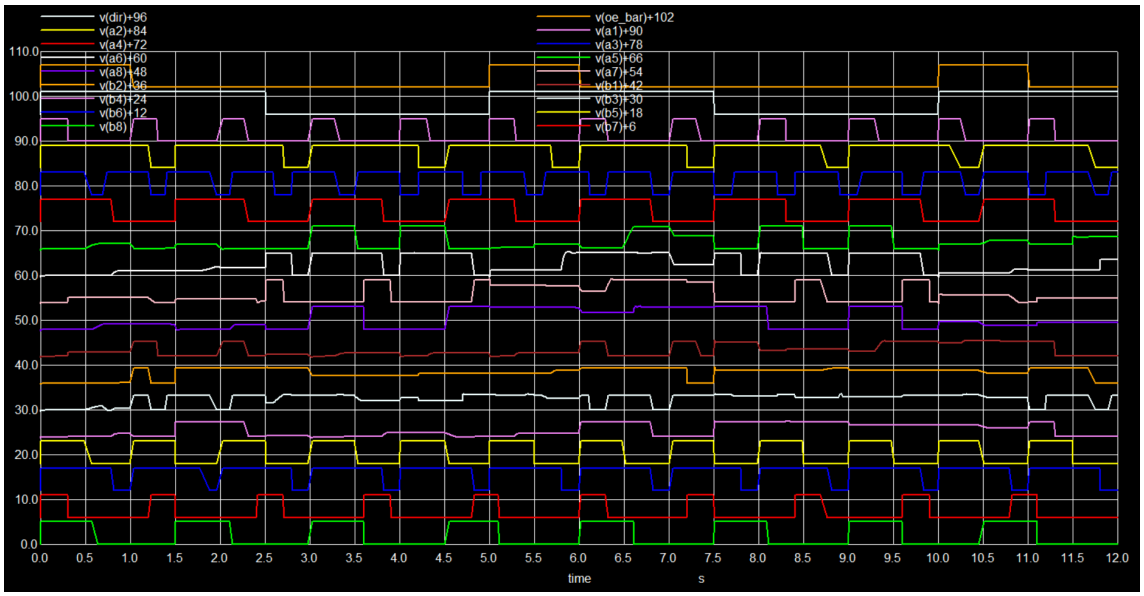



Figure 4.6: NgSpice Simulation result of SN74LVC4245A

### 4.1.7 Conclusion

The SN74LVC4245A proves to be an efficient solution for bidirectional voltage translation between 3.3V and 5V systems, combining reliable level-shifting capability with robust bus management features. Its integrated DIR and $\overline{\text{OE}}$ control logic simplifies system design while maintaining signal integrity during voltage transitions.

## 4.2 SN74S64

**Description:** 4-2-3-2 Input AOI Gates.

### 4.2.1 General Description

The **SN54S64** is an IC that implements a complex combinational logic function in a single package. Designed for military applications (-55°C to 125°C operation), this device provides a space-efficient solution for implementing multi-input Boolean expressions. Its unique 4-2-3-2 input configuration allows designers to combine multiple logic operations while maintaining high-speed performance characteristics.[9]

### 4.2.2 Features

- **Core Logic Operation**:

$$Y = \overline{ABCD + EF + GHI + JK}$$

- **Input Flexibility**:
  - Partial function usage (e.g., can implement just ABCD + EF)
  - Unused inputs can be tied high for constant '1' input

### 4.2.3 Subcircuit

Below is the subcircuit implementation for the `SN74S64` 4-2-3-2 input AND-OR-INVERT gate, demonstrating the compound logic function $Y = \overline{ABCD + EF + GHI + JK}$.

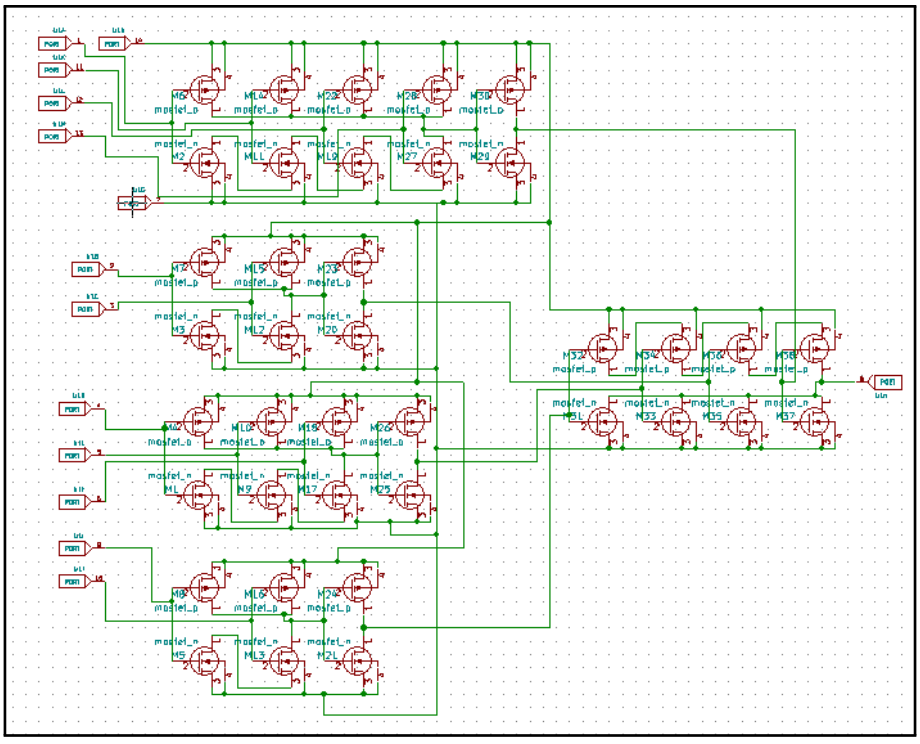


Figure 4.7: Subcircuit of SN74S64

### 4.2.4 IC Package

Below is the physical package configuration for the SN74S64, illustrating the pinout arrangement and mechanical layout.

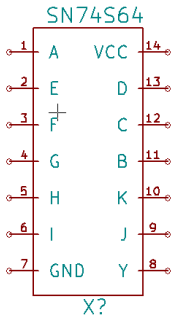



Figure 4.8: IC Layout of SN74S64

### 4.2.5 Test Circuit

Below is the test circuit configuration for the SN74S64, 4-2-3-2 input AND-OR-INVERT gate, designed to validate the Boolean function $Y = \overline{ABCD + EF + GHI + JK}$

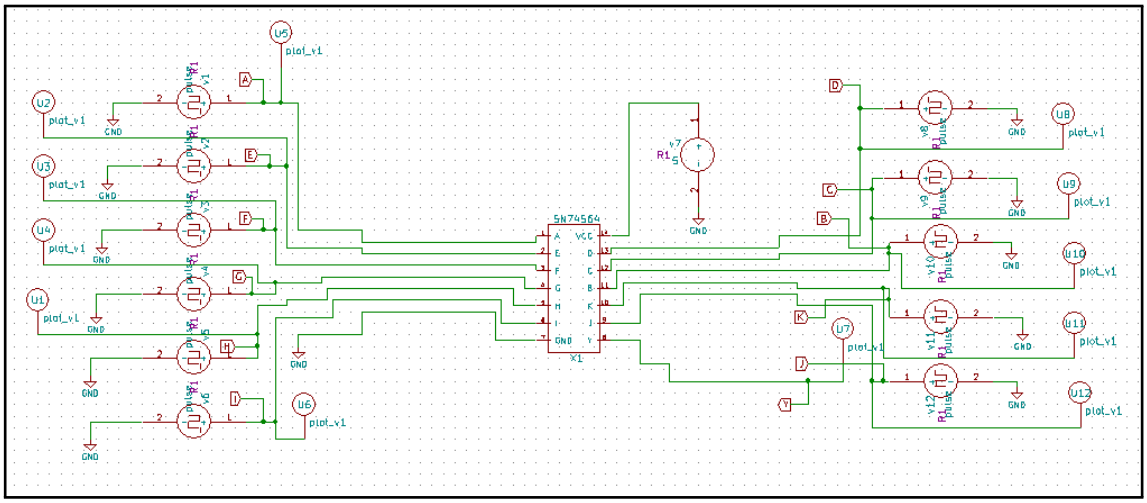



Figure 4.9: Test Circuit of SN74S64

### 4.2.6 NgSpice Simulation Results

Below are the NGspice simulation results for the `SN74S64` test circuit, validating the complex AOI logic function $Y = \overline{ABCD + EF + GHI + JK}$.

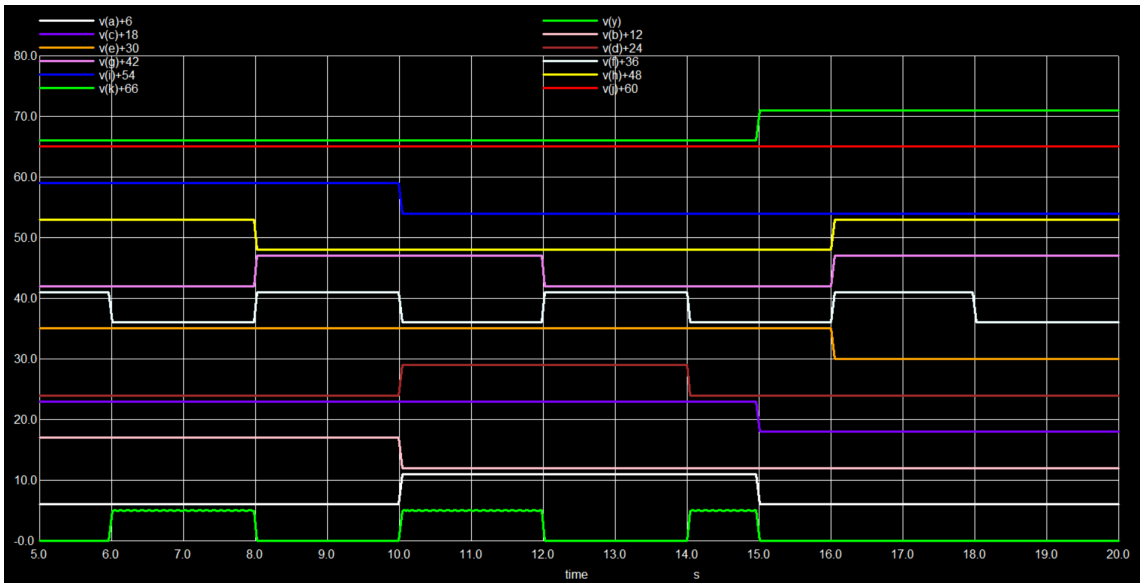



Figure 4.10: NgSpice Simulation result of SN74S64

### 4.2.7 Conclusion

The SN54S64 remains a valuable component for military and industrial systems requiring robust logic implementation. Its ability to condense multiple AND operations with an inverted sum into a single package makes it particularly useful for:

- Complex Boolean expression implementation
- Error detection circuits
- Control logic in harsh environments
- Legacy system maintenance and repairs

The device exemplifies the efficiency of combining multiple logic operations in integrated form while maintaining the ruggedness expected from Texas Instruments' 54-series components.

## 4.3 SN74100

**Description:** 8-Bit Bistable Latches.

### 4.3.1 General Description

The **SN74100** (commercial-grade) is a 8-bit transparent latche designed for temporary data storage in digital systems. These TTL-compatible devices feature a simple enable-controlled operation that allows real-time data monitoring when enabled and data retention when disabled. The latches are particularly useful for interfacing between processing units and I/O systems where temporary data buffering is required.[10]

### 4.3.2 Features

- **Transparent Latching Operation**:
  - Data inputs (D) propagate directly to outputs (Q) when enable (G) is high
  - Latches data on high-to-low transition of enable signal
- **Independent Bit Control**:
  - Eight identical but independent latch circuits
  - Common enable signal controls all bits simultaneously

### 4.3.3 Subcircuit

Below is the subcircuit implementation for the `SN74100`, showcasing the 8-bit bistable latch architecture with transparent data input and enable control. The design emphasizes reliable data retention and TTL-compatible signal levels.

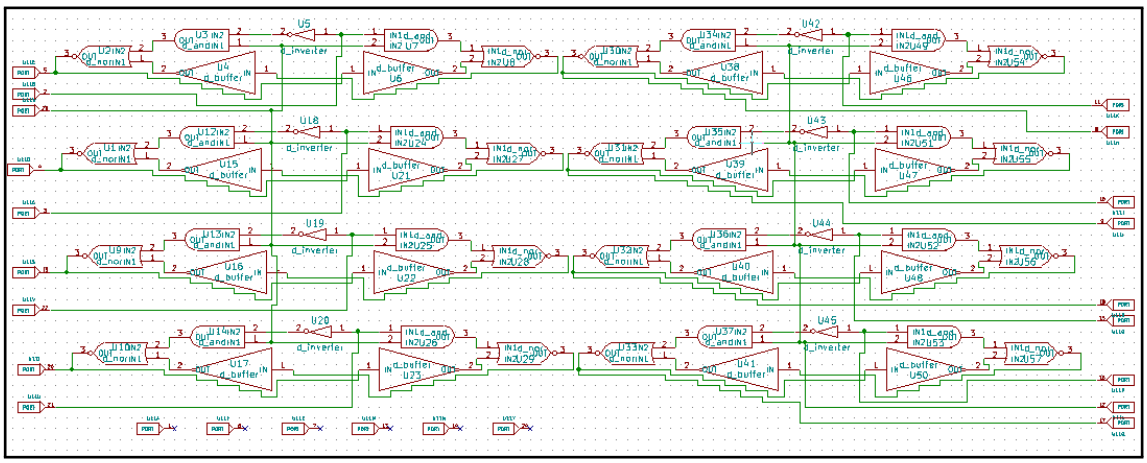


Figure 4.11: Subcircuit of SN74100

### 4.3.4 IC Package

Below is the physical package configuration for the SN74100, illustrating the pinout arrangement and mechanical layout.

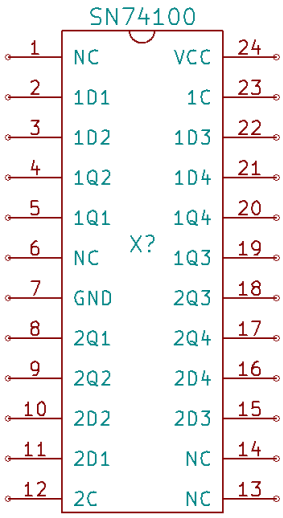



Figure 4.12: IC Layout of SN74100

### 4.3.5 Test Circuit

Below is the test circuit configuration for the SN74100 8-bit bistable latch, designed to verify transparent and latched data transfer functionality

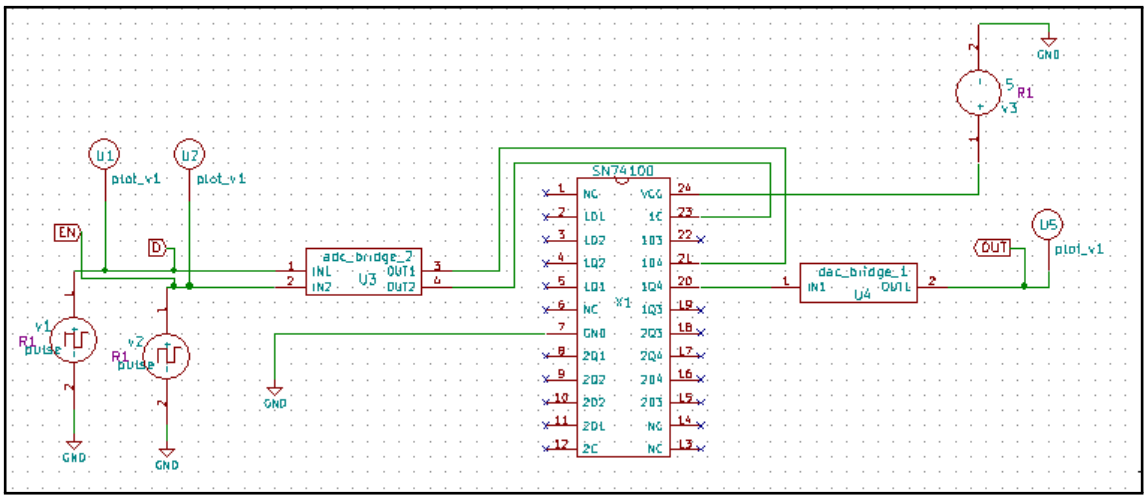



Figure 4.13: Subcircuit of SN74100

### 4.3.6 NgSpice Simulation Results

Below are the NGspice simulation results for the `SN74100` test circuit, demonstrating latch timing characteristics.

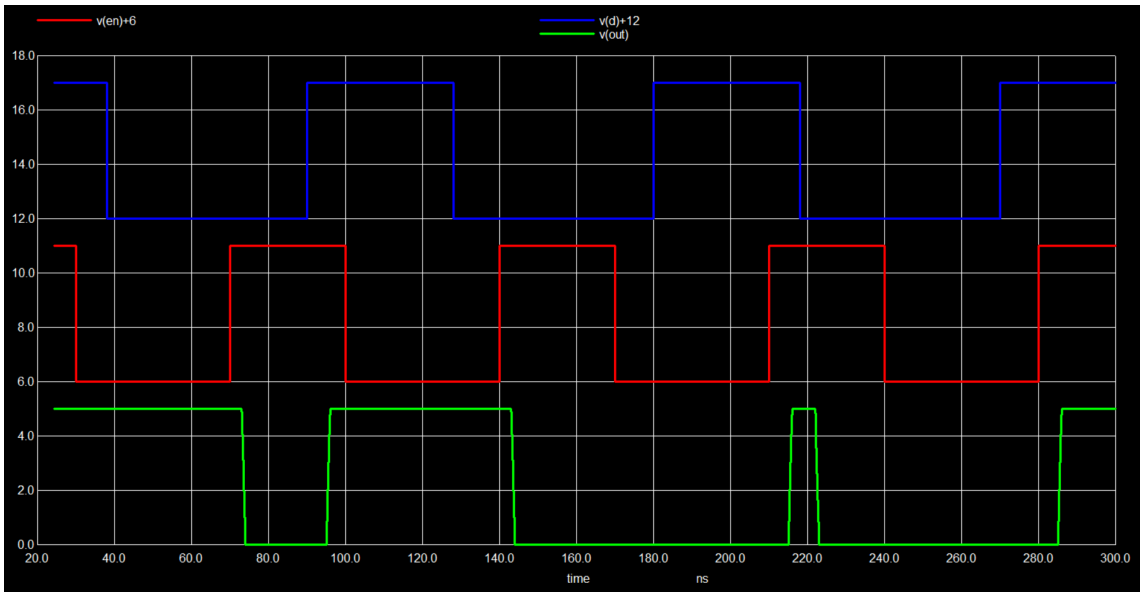



Figure 4.14: NgSpice Simulation result of SN74100

### 4.3.7 Conclusion

The SN74100 latche provide a robust solution for temporary data storage in TTL-based systems. Their simple enable control and transparent operation make them ideal for:

- Processor-to-peripheral data buffering
- Signal synchronization between asynchronous systems
- Temporary storage in data processing pipelines

While modern CMOS alternatives offer lower power consumption, these TTL latches remain valuable in applications requiring TTL compatibility and robust operation in electrically noisy environments.

## 4.4 SN74120

**Description:** Dual Pulse Synchronizers/Drivers.

### 4.4.1 General Description

**SN74120** is a dual pulse synchronizer designed for use in digital systems where signal integrity and metastability control are critical. It ensures that asynchronous input pulses are safely synchronized to a system clock domain, preventing glitches and timing hazards that can occur when signals cross clock boundaries. The device includes two independent channels, each capable of receiving an input pulse and outputting a clean, clock-synchronized pulse.[11]

This IC is particularly useful in applications such as event signaling between asynchronous systems, digital handshaking, and synchronization of external interrupts.

### 4.4.2 Features

- Dual independent pulse synchronizer channels
- Converts asynchronous input pulses to synchronized outputs
- Suitable for clock domain crossing and interrupt synchronization

### 4.4.3 Subcircuit

Below is the subcircuit implementation for the `SN74120` Dual Pulse Synchronizer/-Driver, featuring independent pulse generation channels with precise timing control and output driving capability.

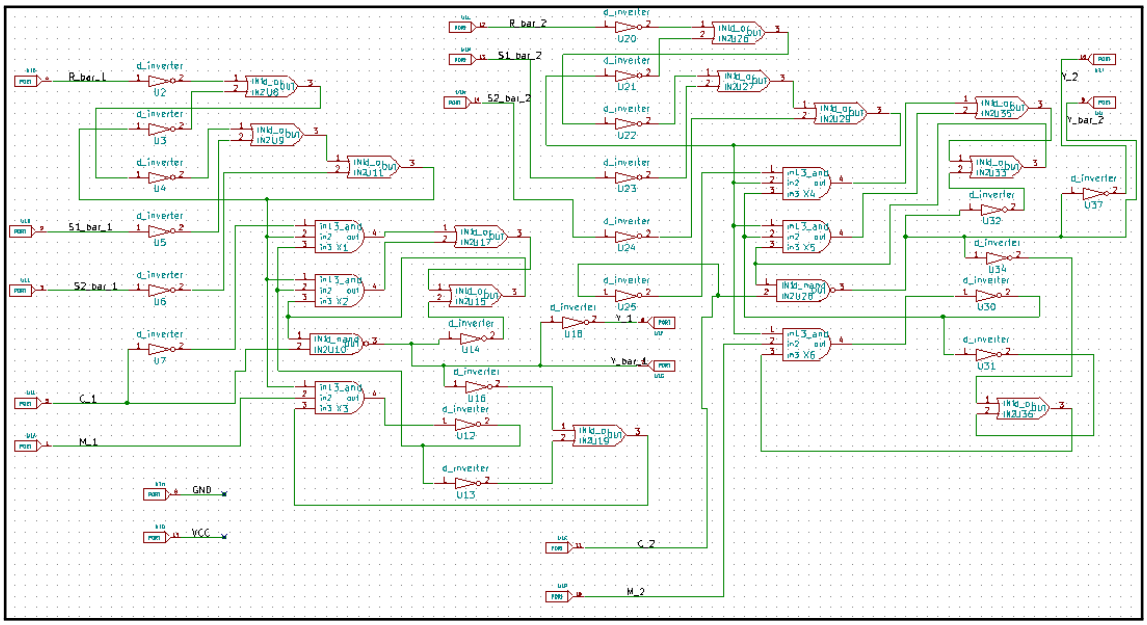



Figure 4.15: Subcircuit of SN74120

### 4.4.4 IC Package

Below is the physical package configuration for the SN74120, illustrating the pinout arrangement and mechanical layout.

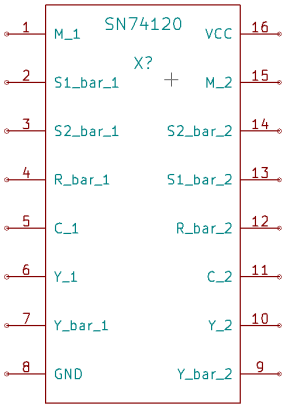



Figure 4.16: IC Layout of SN74120

### 4.4.5 Test Circuit

Below is the test circuit configuration for the SN74120 dual pulse synchronizer/-driver, designed to verify pulse generation and synchronization characteristics.

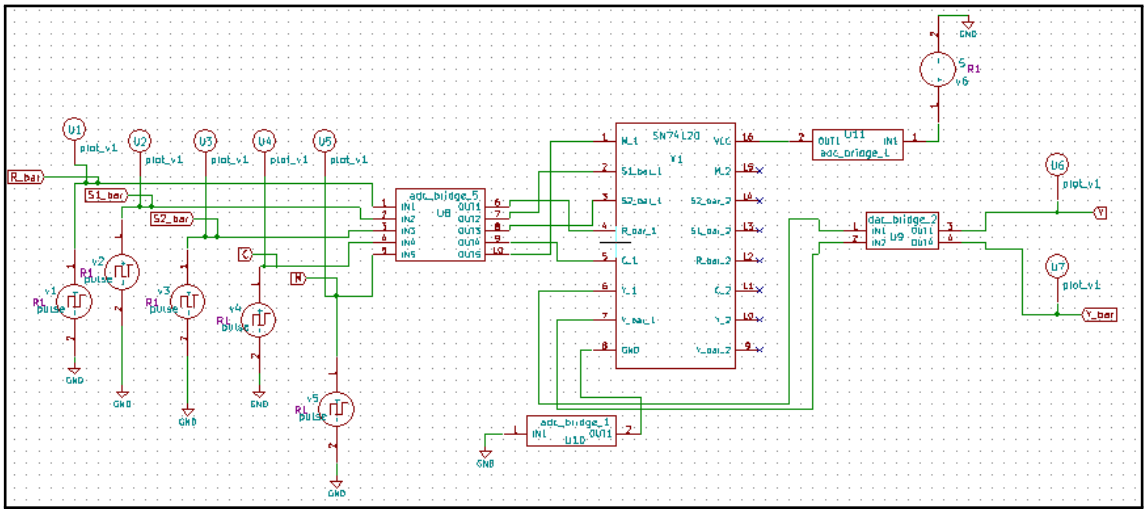



Figure 4.17: Subcircuit of SN74120

### 4.4.6 NgSpice Simulation Results

Below are the NGspice simulation results for the `SN74120` test circuit, verifying pulse synchronization.

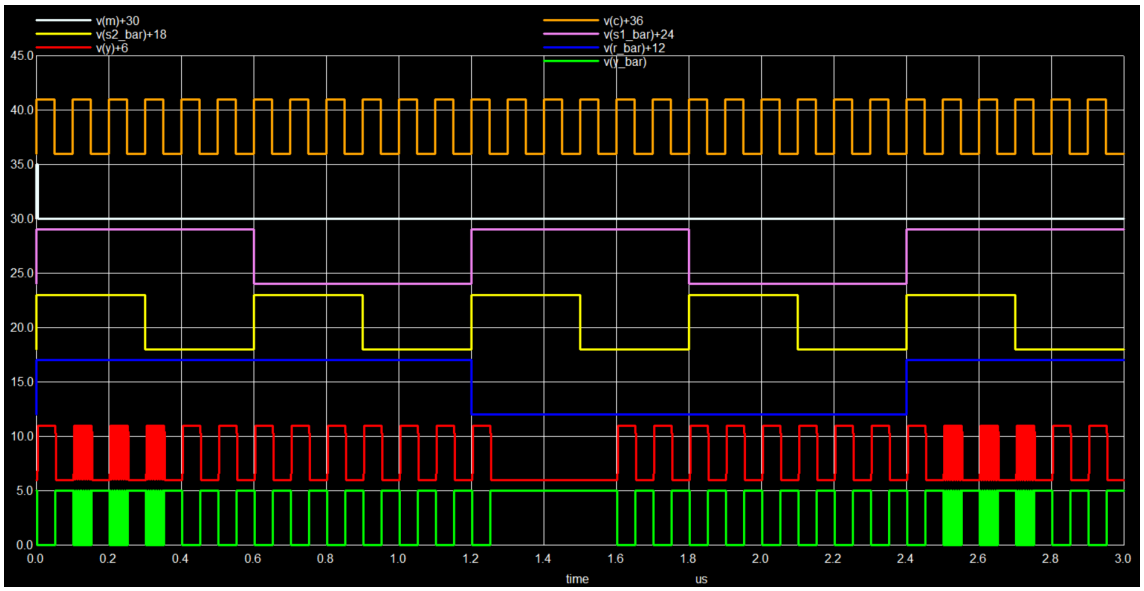



Figure 4.18: NgSpice Simulation result of SN74120

### 4.4.7 Conclusion

The SN54120 is a robust and effective solution for synchronizing asynchronous pulses in digital systems. By providing clean, glitch-free pulse outputs aligned to the system clock, it plays a crucial role in ensuring timing reliability across clock domains. Its dual-channel design and TTL compatibility make it ideal for embedded, control, and communication system designs where metastability must be minimized.

## 4.5 CD4048BMS

**Description:** CMOS Multifunction Expandable 8 Input Gate.

### 4.5.1 General Description

**CD4048BMS** is a CMOS-based multifunction expandable logic gate designed to implement up to eight logic functions using a single 16-pin IC. It includes eight standard logic inputs (A–H), four control inputs (Ka, Kb, Kc, Kd), and one expand input for cascading multiple devices. The logic function is determined by the binary values applied to Ka, Kb, and Kc, while Kd enables a three-state output control for bus interfacing applications.[12]

The IC is capable of performing multiple logic operations such as OR, NOR, AND, NAND, OR/AND, OR/NAND, AND/OR, and AND/NOR based on control input combinations. With a wide supply voltage range up to 20V and low input current, it is ideal for low-power logic designs in space- and performance-constrained applications. The expand input allows cascading multiple devices to increase the number of logic inputs.

### 4.5.2 Features

- Eight-input multifunction logic gate with 3 binary control inputs (Ka, Kb, Kc)
- Supports eight logic functions: OR, NOR, AND, NAND, OR/AND, OR/-NAND, AND/OR, AND/NOR
- Expand input for cascading multiple gates (e.g., for 16-input logic functions)
- Three-state output control via Kd for bus interfacing

### 4.5.3 Configurable Functions of CD4048BMS

The CD4048BMS provides eight different logic functions based on the binary control inputs Ka, Kb, and Kc. The table below summarizes these functions along with their corresponding Boolean expressions and the required connections for unused inputs.

Table 4.1: Function Truth Table for CD4048BMS

| Output Function | Boolean Expression | Ka | Kb | Kc |
|---|---|---|---|---|
| NOR | $J = \overline{A + B + C + D + E + F + G + H}$ | 0 | 0 | 0 |
| OR | $J = A + B + C + D + E + F + G + H$ | 0 | 0 | 1 |
| OR/AND | $J = \overline{(A + B + C + D) \cdot (E + F + G + H)}$ | 0 | 1 | 0 |
| OR/NAND | $J = \overline{(A + B + C + D) \cdot (E + F + G + H)}$ | 0 | 1 | 1 |
| AND | $J = A \cdot B \cdot C \cdot D \cdot E \cdot F \cdot G \cdot H$ | 1 | 0 | 0 |
| NAND | $J = \overline{A \cdot B \cdot C \cdot D \cdot E \cdot F \cdot G \cdot H}$ | 1 | 0 | 1 |
| AND/NOR | $J = \overline{A \cdot B \cdot C \cdot D + E \cdot F \cdot G \cdot H}$ | 1 | 1 | 0 |
| AND/OR | $J = A \cdot B \cdot C \cdot D + E \cdot F \cdot G \cdot H$ | 1 | 1 | 1 |

**Note:** The control input Kd determines the output state:
- $Kd = 1$: Normal output (logic 1 or 0).
- $Kd = 0$: High-impedance output (open circuit).

### 4.5.4 Subcircuit

Below is the subcircuit implementation for the `CD4048BMS` CMOS multifunction gate, demonstrating its configurable 8-input logic capability with expansion control.

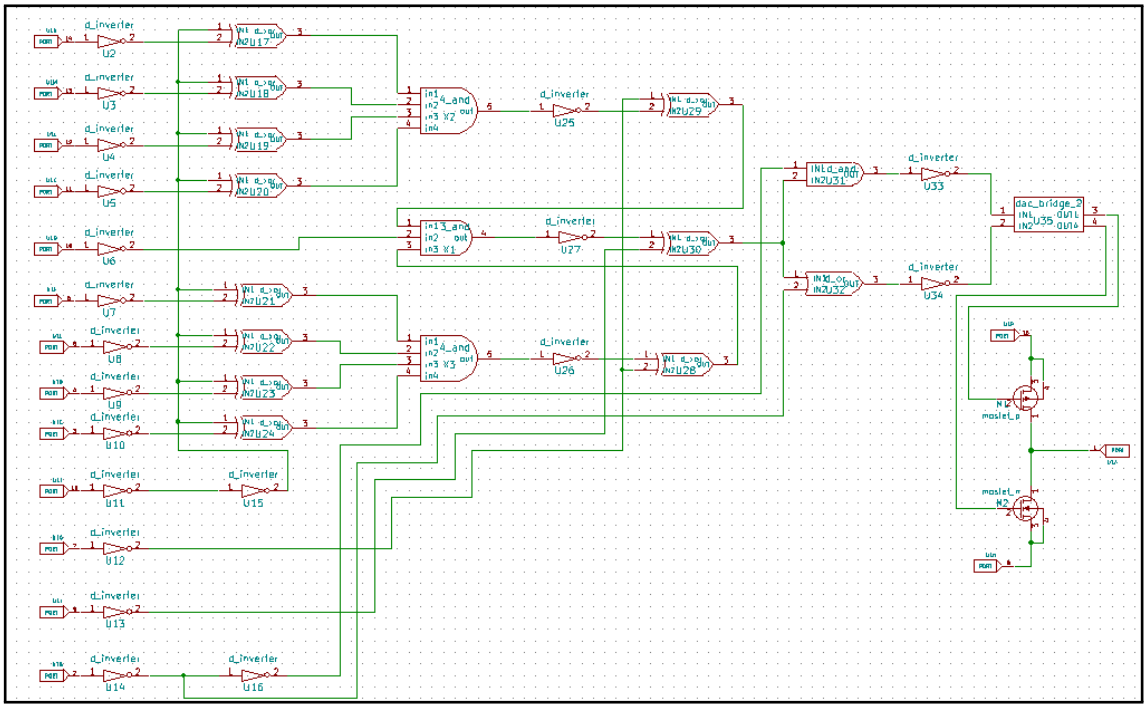


Figure 4.19: Subcircuit of CD4048BMS

### 4.5.5 IC Package

Below is the physical package configuration for the `CD4048BMS`, illustrating the pinout arrangement and mechanical layout.

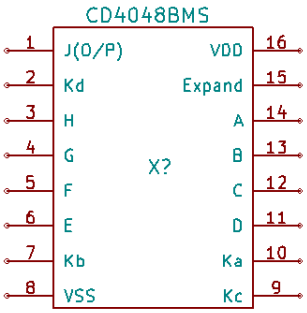



Figure 4.20: IC Layout of CD4048BMS

### 4.5.6 Test Circuit

Below is the test circuit for the CD4048BMS CMOS multifunction expandable 8-input gate, designed to verify all programmable logic operations and expansion capabilities.

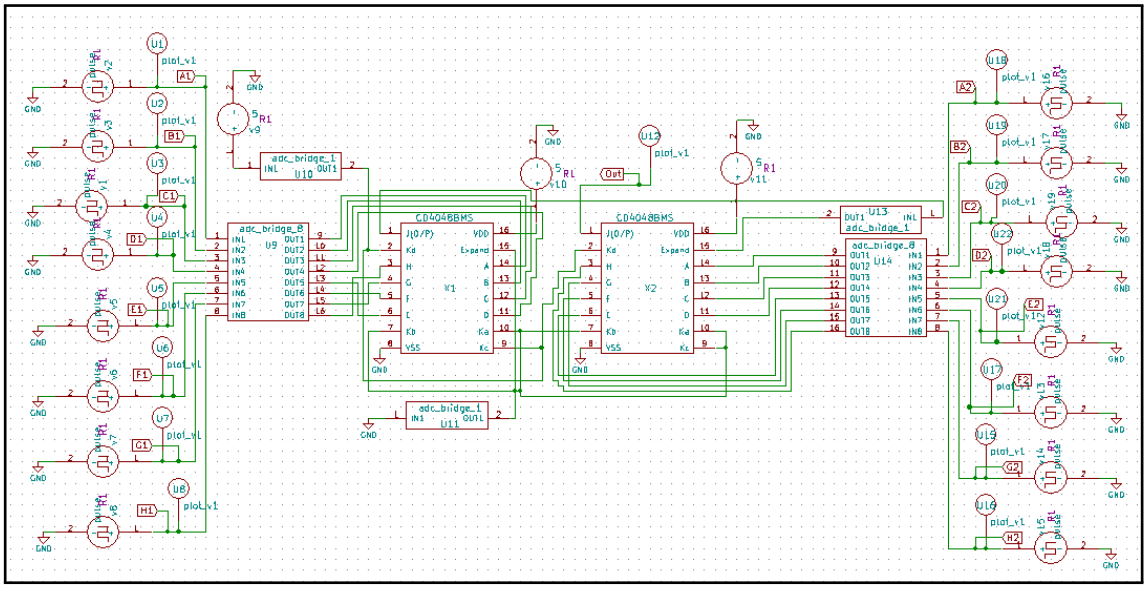


Figure 4.21: Subcircuit of CD4048BMS

### 4.5.7 NgSpice Simulation Results

Below are the NGspice simulation results for the CD4048BMS test circuit, validating configurable logic operations.

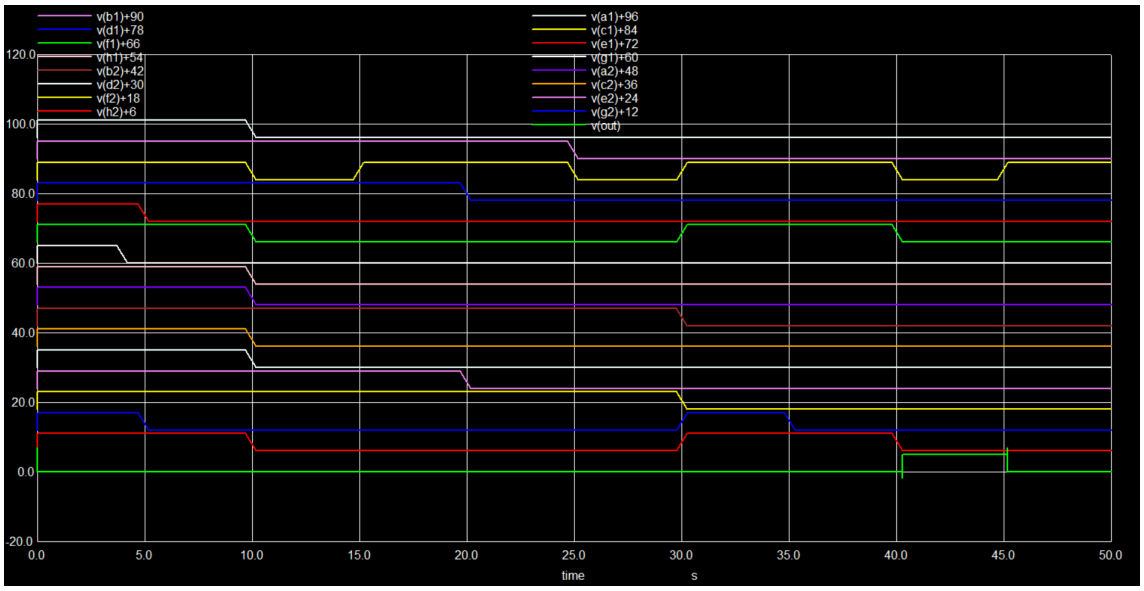



Figure 4.22: NgSpice Simulation result of CD4048BMS

### 4.5.8 Conclusion

The CD4048BMS is a versatile and reliable CMOS logic IC offering multiple logic functions in a single package. Its expandability and ability to perform complex combinational logic operations make it a strong candidate for applications in decoding, encoding, digital control, and signal conditioning. Its broad voltage compatibility and low power design further enhance its suitability for both industrial and aerospace-grade systems.

## 4.6 CBTL02043B

**Description:** 2 differential channel, 2:1 multiplexer/demultiplexer switch.

### 4.6.1 General Description

The CBTL02043B is a bidirectional 2:1 differential multiplexer/demultiplexer switch optimized for high-speed serial interfaces. It provides low-loss signal routing between multiple ports in applications like USB 3.1, PCIe Gen3, and DisplayPort systems. The device features two variants with different pinouts.[13]

### 4.6.2 Features

- **Switching Configuration**:
  - 2 differential channels with 2:1 routing (A↔B or A↔C)
  - Bidirectional operation (MUX/DEMUX modes)
- **Control Interface**:
  - Single SEL pin for path selection (LOW=A-B, HIGH=A-C)
  - XSD shutdown pin for power saving.

### 4.6.3 Subcircuit

Below is the subcircuit implementation for the `CBTL02043B` 2:1 differential multiplexer/demultiplexer switch, featuring bidirectional channel switching and low-loss signal routing.

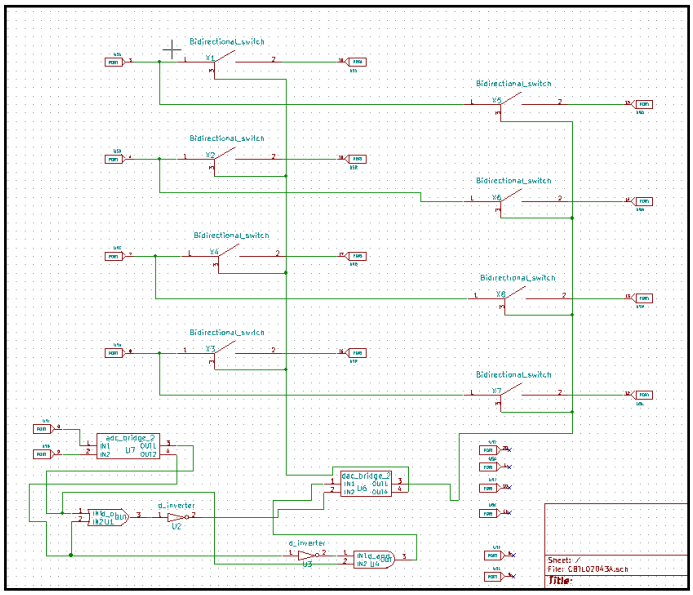



Figure 4.23: Subcircuit of CBTL02043B

This subcircuit serves as a switching network that uses Bidirectional Switches as the core switching elements.

Each switch in the design is represented by a custom-defined subcircuit, which allows current flow in both directions based on the control logic.

The Subcircuit implementation for the Bidirectional switch is as follows:

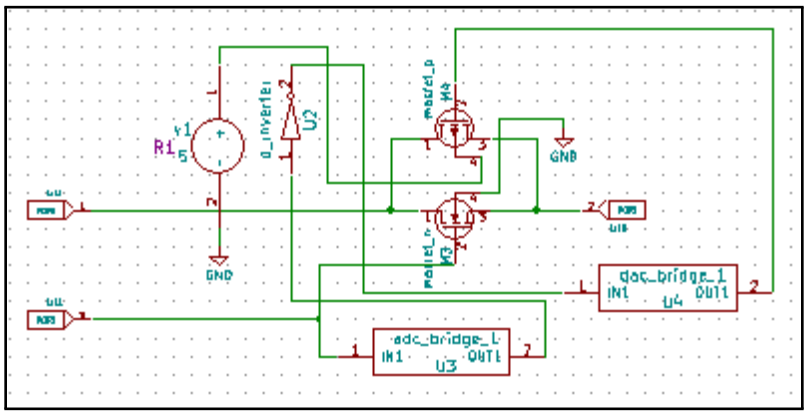



Figure 4.24: Subcircuit of CBTL02043B

The symbol for the bidirectional switch is as follows:

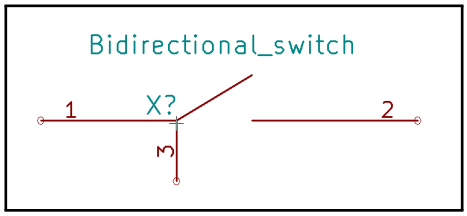



Figure 4.25: Subcircuit of CBTL02043B

### 4.6.4 IC Package

Below is the physical package configuration for the `CBTL02043B`, illustrating the pinout arrangement and mechanical layout.

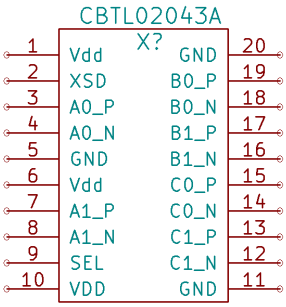



Figure 4.26: IC Layout of CBTL02043B

### 4.6.5 Test Circuit

Below is the test circuit for the CBTL02043B 2:1 differential multiplexer/demultiplexer switch, designed to validate high-speed signal switching characteristics and channel isolation.

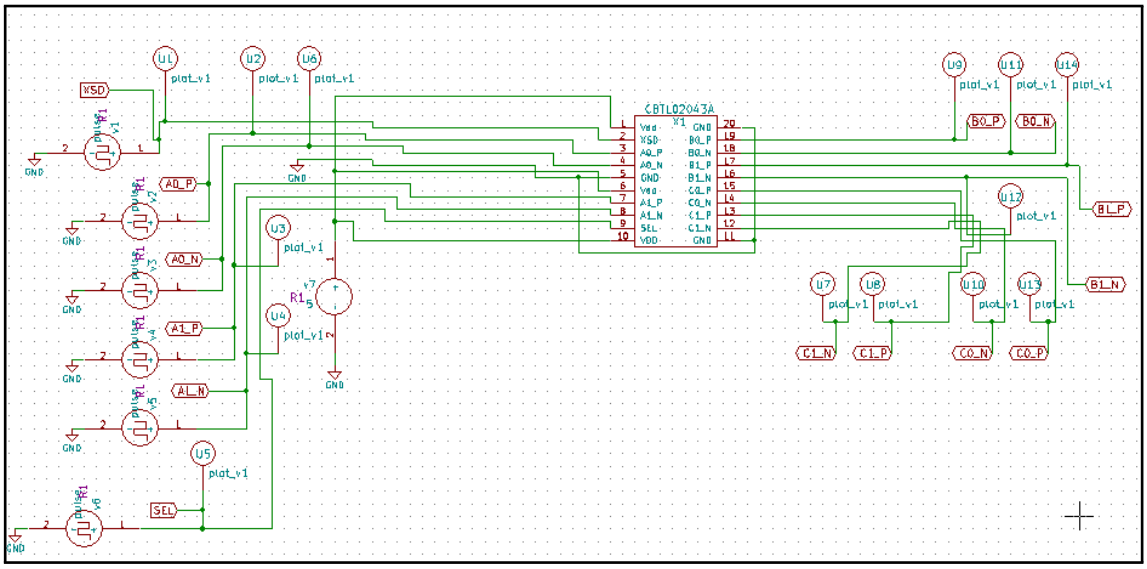



Figure 4.27: Subcircuit of CBTL02043B

### 4.6.6 NgSpice Simulation Results

Below are the NGspice simulation results for the CBTL02043B test circuit, characterizing high-speed switching.

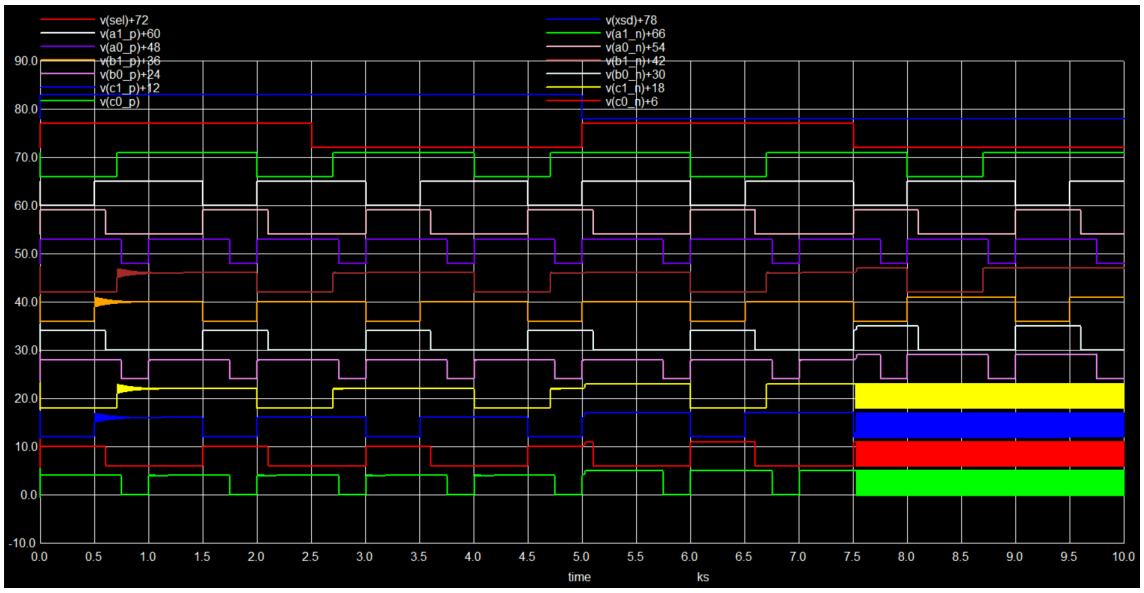



Figure 4.28: NgSpice Simulation result of CBTL02043B

### 4.6.7 Conclusion

This switch is ideal for:

- Port expansion in multi-interface systems integrity-critical routing
- Space-constrained high-speed designs

The combination of excellent signal integrity and flexible configuration options makes it particularly valuable for modern serial interface applications requiring reliable, low-loss switching.

## 4.7 AN1186

**Description:** Cyclic Redundancy Check Generator Unit for 1-wire Protocol.

### 4.7.1 General Description

**AN1186** is a dedicated Cyclic Redundancy Check (CRC) Generator Unit designed for the 1-Wire communication protocol. It utilizes an 8-bit shift register and the polynomial $x^8 + x^5 + x^4 + 1$ to compute CRC codes for 64-bit data streams. Implemented using the **SLG46533V GreenPAK™ IC**, the design supports LSB-first serial input and provides an 8-bit parallel CRC output. It is capable of detecting single, double, and clustered bit errors, enhancing communication reliability. The unit includes clock and reset inputs for synchronized operation, making it ideal for embedded systems lacking hardware CRC support.[14]

### 4.7.2 Features

- Implements 8-bit CRC for 1-Wire protocol using $x^8 + x^5 + x^4 + 1$
- Detects single, double, and burst errors within 8-bit windows
- Accepts LSB-first serial input and outputs an 8-bit parallel CRC
- Configurable via SLG46533V GreenPAK™ programmable IC

### 4.7.3 Subcircuit

Below is the subcircuit implementation for the `AN1186` CRC Generator Unit, demonstrating the 1-Wire protocol-compatible error detection architecture.

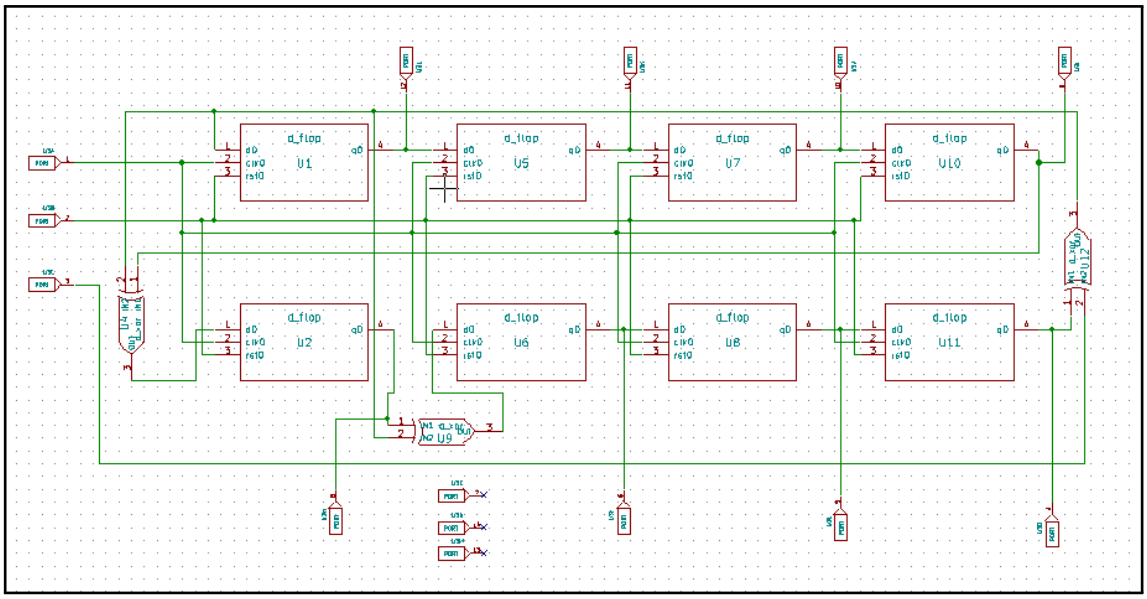


Figure 4.29: Subcircuit of AN1186

Above subcircuit comprises of the multiple D Flip Flops connected in a cascaded manner. These individual blocks are designed through Mixed signal approach.

The verilog code for the D flip flop is as follows:

```
module d_flop(d, clk, rst, q);
input d, clk, rst;
output reg q;
always @(posedge clk) begin
  if(rst) begin
    q <= 0;
  end
  else begin
    q <= d;
  end
end
endmodule
```

Listing 4.1: Verilog Code for D Flip Flop

### 4.7.4 IC Package

Below is the physical package configuration for the AN1186, illustrating the pinout arrangement and mechanical layout.

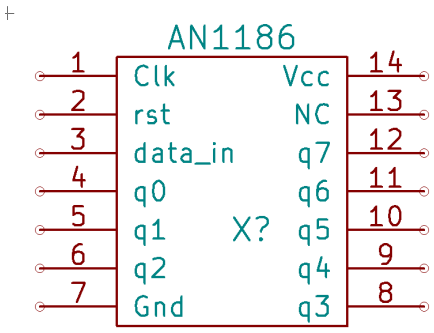



Figure 4.30: IC Layout of AN1186

### 4.7.5 Test Circuit

Below is the test circuit configuration for the AN1186 CRC-8 generator unit, designed to validate error detection capabilities for 1-Wire protocol communications.

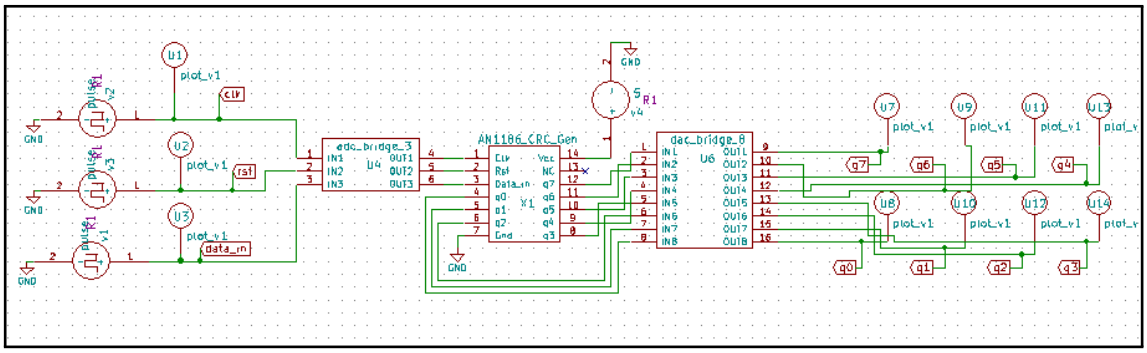



Figure 4.31: Subcircuit of AN1186

### 4.7.6 NgSpice Simulation Results

Below are the NGspice simulation results for the AN1186 test circuit, verifying CRC-8 generation.

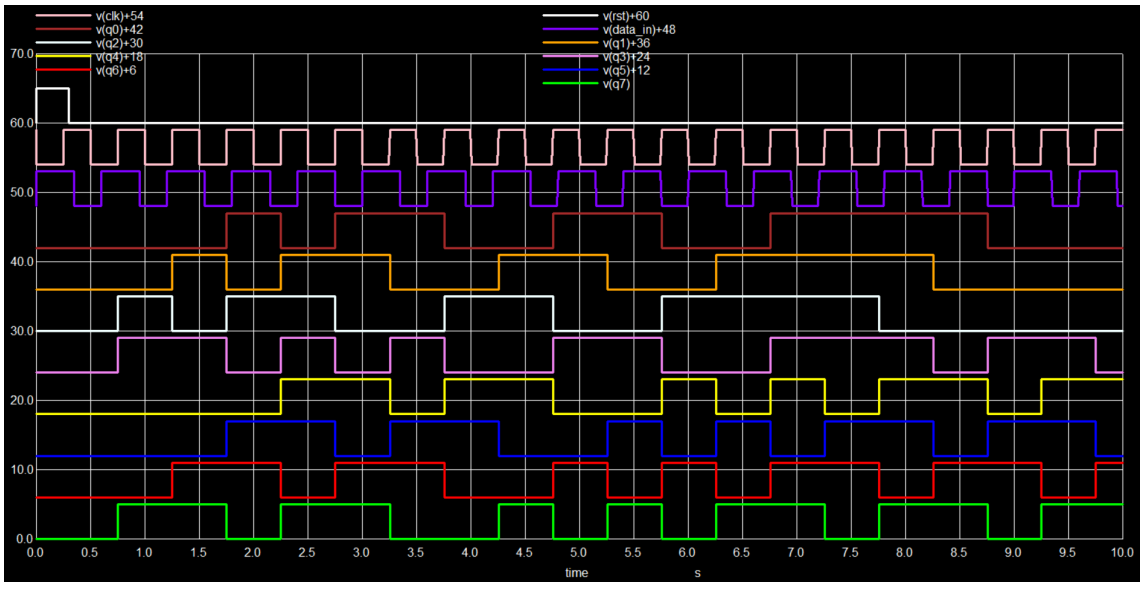



Figure 4.32: NgSpice Simulation result of AN1186

### 4.7.7 Conclusion

The AN1186 CRC Generator Unit offers a reliable and compact solution for ensuring data integrity in 1-Wire communication systems. By leveraging the configurable SLG46533V GreenPAK™ IC, it enables efficient hardware-based CRC computation with minimal external components. The design is particularly beneficial in embedded applications where dedicated CRC peripherals are unavailable.

# Chapter 5

# Mixed-Signal Simulation

The Mixed-Signal Simulation feature of eSim allows co-simulation of analog and digital domains by integrating SPICE-based analog circuits with Verilog-based digital designs. This is achieved using the NgVeri interface, which combines NgSpice for analog simulation and Verilator for digital simulation. Mixed-signal co-simulation helps in analyzing real-world circuits where both analog and digital blocks interact, providing a complete system-level verification platform.

## 5.1 IDT72V201

**Description:** 256 x 9 CMOS Sync FIFO

### 5.1.1 General Description

The **IDT72V201** is a synchronous First-In-First-Out (FIFO) memory component designed for high-speed digital systems that require reliable data buffering and flow control. It features a **256 × 9-bit** memory configuration, supporting independent read and write operations, making it ideal for interfacing devices with mismatched data rates.[15]

This FIFO operates on the principle of sequential data storage and retrieval, where data is read in the same order as it is written. The internal pointer mechanism and programmable flag logic allow real-time tracking of memory status, helping prevent overflows.

### 5.1.2 Functional Block Diagram

Below is the Functional Block Diagram of the IDT72V201, 256 x 9 CMOS Sync FIFO.

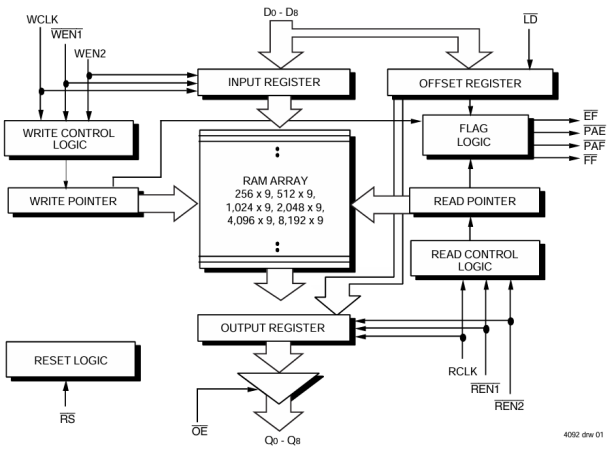



Figure 5.1: Functional Block Digram of SyncFIFO-IDT72V201

### 5.1.3 Features

- 256 × 9-bit memory organization
- Supports independent read (RCLK) and write (WCLK) clocks
- Dual-ported architecture with zero fall-through time
- Empty Flag (EF) and Full Flag (FF) indicate FIFO status
- Programmable Almost-Empty (PAE) and Almost-Full (PAF) flags
  - Default thresholds: Empty+7 and Full–7
  - Programmable to any desired depth
- Output Enable (OE) provides tri-state control for data bus
- Available in 32-pin PLCC and 32-pin TQFP packages

### 5.1.4 Verilog Code

```
module FIFO (
    input  wire [8:0] D,
    input  wire       WCLK,
    input  wire       RCLK,
    input  wire       WEN1,
    input  wire       WEN2,
    input  wire       REN1,
    input  wire       REN2,
    input  wire       OE,
    input  wire       RS,

    output reg  [8:0] Q,
    output reg        EF,
    output reg        FF,
    output reg        PAE,
    output reg        PAF
);
    parameter DEPTH = 256;
    parameter ADDR_WIDTH = 8;

    reg [8:0] mem [0:DEPTH-1];
    reg [ADDR_WIDTH:0] write_ptr, read_ptr;

    // Local domain used counters
    reg [ADDR_WIDTH:0] used_words_wr;
    reg [ADDR_WIDTH:0] used_words_rd;

    // Programmable offsets
    reg [8:0] empty_offset = 9'd10;
    reg [8:0] full_offset  = 9'd10;
    reg [1:0] offset_state = 0;

    // Reset block
    always @(posedge RS) begin
        write_ptr     <= 0;
        read_ptr      <= 0;
        used_words_wr <= 0;
        used_words_rd <= 0;
        Q             <= 9'd0;
        EF            <= 1;
        FF            <= 0;
        PAE           <= 1;
        PAF           <= 0;
        empty_offset  <= 9'd7;
        full_offset   <= 9'd7;
        offset_state  <= 0;
    end

// Write domain counter and flags
   always @(posedge WCLK) begin
```

```
51      if (RS) begin
52          write_ptr     <= 0;
53          used_words_wr <= 0;
54          FF            <= 0;
55          PAF           <= 0;
56          offset_state  <= 0;
57      end else begin
58          if (!WEN2) begin
59              case (offset_state)
60                  2'd0: empty_offset[7:0] <= D;
61                  2'd1: empty_offset[8]   <= D[0];
62                  2'd2: full_offset[7:0]  <= D;
63                  2'd3: full_offset[8]    <= D[0];
64              endcase
65              offset_state <= offset_state + 1;
66          end else if (!WEN1 && WEN2 && !FF) begin
67              mem[write_ptr[ADDR_WIDTH-1:0]] <= D;
68              write_ptr <= write_ptr + 1;
69              used_words_wr <= used_words_wr + 1;
70          end
71
72          FF  <= ((used_words_wr - used_words_rd) >= DEPTH - 1);
73          PAF <= (full_offset < DEPTH) ? ((used_words_wr -
                used_words_rd) >= (DEPTH - full_offset)) : 1'b1;
74      end
75  end
76
77
78  // Read domain counter and flags
79  always @(posedge RCLK) begin
80      if (RS) begin
81          read_ptr     <= 0;
82          Q            <= 9'd0;
83          used_words_rd <= 0;
84          EF           <= 1;
85          PAE          <= 1;
86      end else begin
87          if (!REN1 && !REN2 && !EF) begin
88              Q <= OE ? mem[read_ptr[ADDR_WIDTH-1:0]] : 9'd0;
89              read_ptr <= read_ptr + 1;
90              used_words_rd <= used_words_rd + 1;
91          end
92
93          EF  <= ((used_words_wr - used_words_rd) == 0);
94          PAE <= ((used_words_wr - used_words_rd) <=
                empty_offset);
95      end
96  end
97
98  endmodule
```

Listing 5.1: Verilog Code for IDT72V201 - Sync FIFO

### 5.1.5 Simulation Waveforms

Below are the Simulation Waveforms of the Icarus Verilog, which is showcasing the accurate functional behaviour of the IDT72V201, 256 x 9 CMOS Sync FIFO.

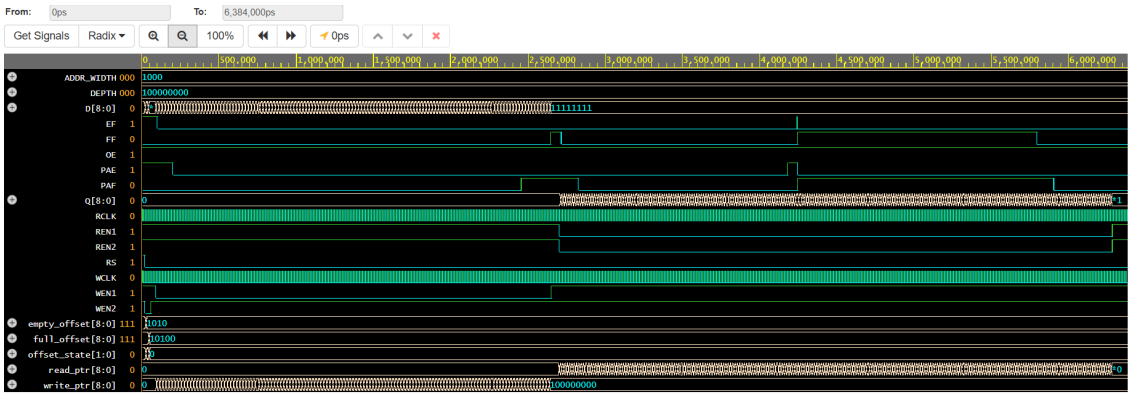



Figure 5.2: Simulation result from Icarus Verilog

### 5.1.6 NgVeri Model

Below is the NgVeri Model created for the IC - IDT72V201.

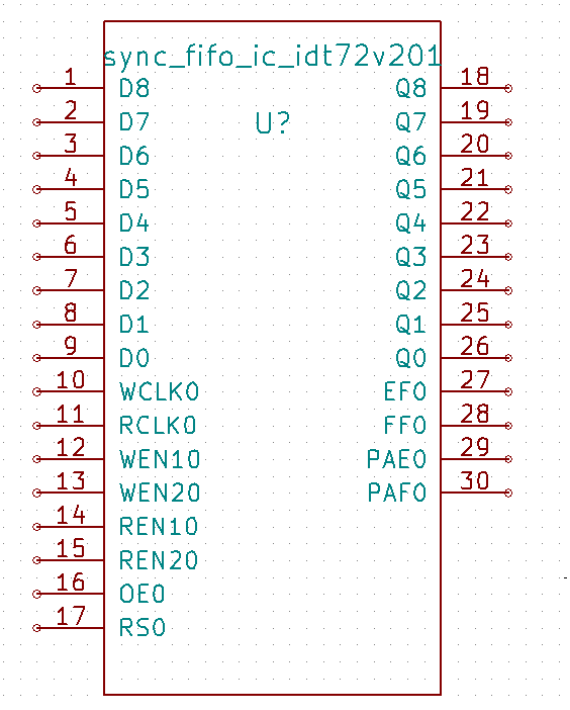



Figure 5.3: NgVeri Model of IDT72V201 Sync FIFO

### 5.1.7 Test Circuit

Below is the test circuit for the IDT72V201, 256 x 9 CMOS Sync FIFO, designed to validate independent read and write operations of the Synchronous FIFO memory.

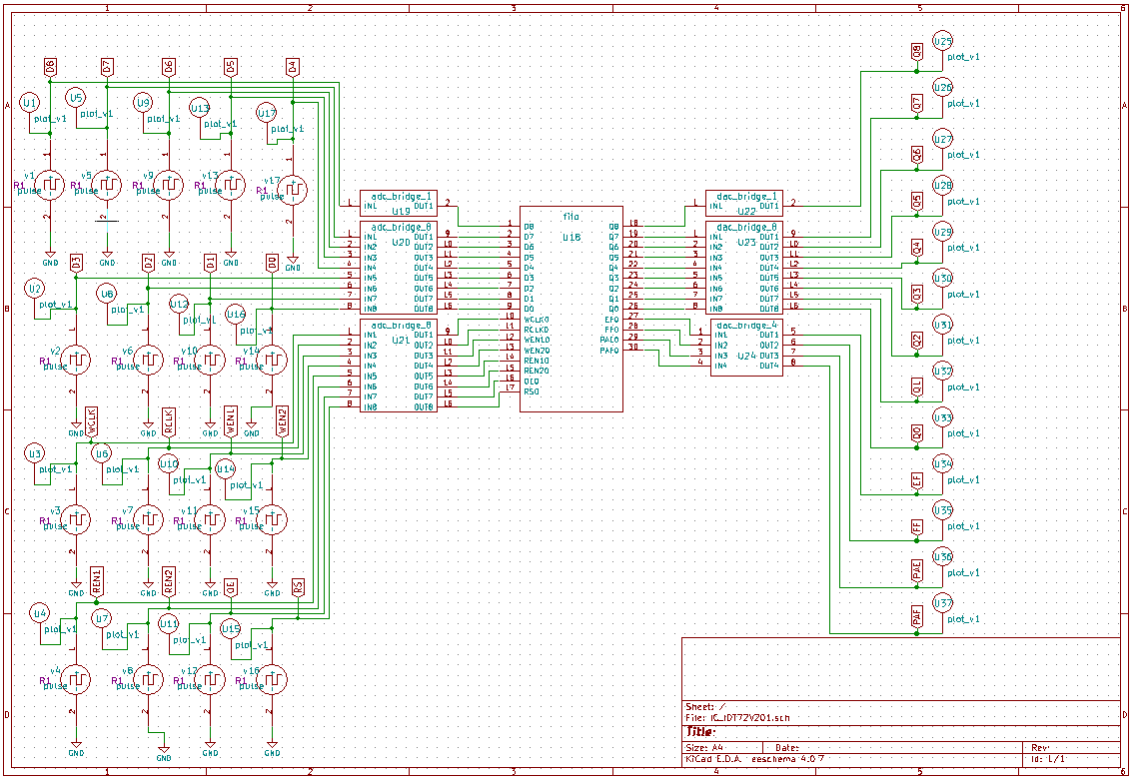


Figure 5.4: Test Circuit of IDT72V201 Sync FIFO

### 5.1.8 NgSpice Simulation Results

Below are the NgSpice simulation results for the above Test Circuit of IDT72V201 - Synchronous FIFO memory.

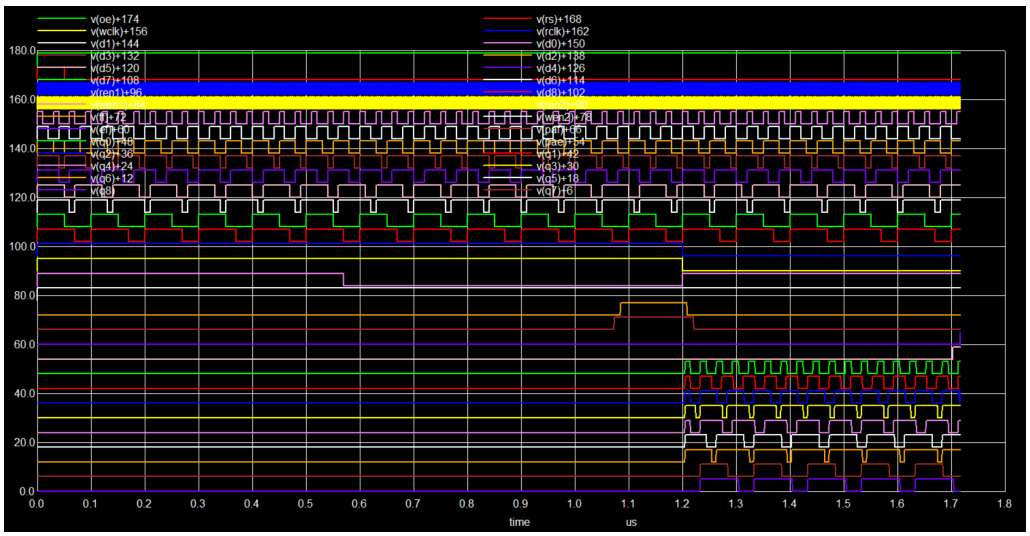



Figure 5.5: NgSpice Simulation result of IDT72V201

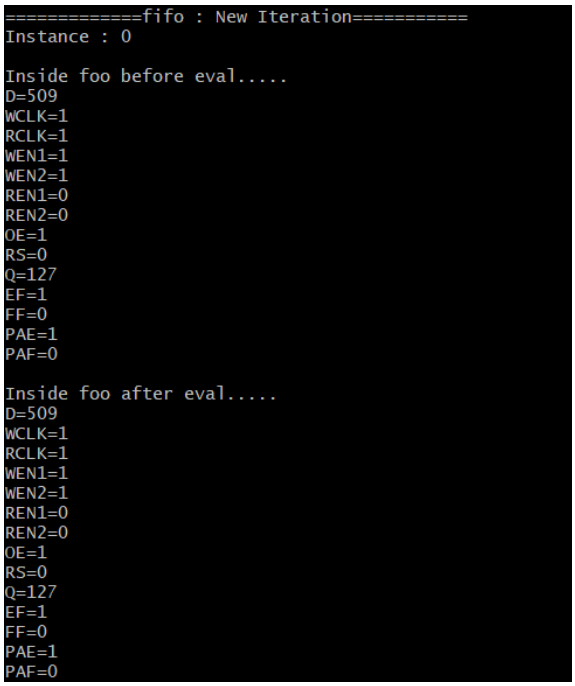



Figure 5.6: Ngspice Simulation result of IDT72V201

### 5.1.9 Conclusion

The IDT72V201 FIFO serves as a robust and efficient memory solution in digital system design, offering high-speed, reliable, and low-latency data handling. Its use in this project enables seamless interfacing between asynchronous modules, helping maintain data integrity and overall system performance.

## 5.2 DS90CR285

**Description:** Rising Edge Data Strobe LVDS 28-Bit Channel Link - Serializer

### 5.2.1 General Description

The **DS90CR285** is a high-speed **28-bit LVCMOS/LVTTL-to-LVDS serializer** designed for robust data transmission in digital systems. It converts parallel input data into four serialized LVDS (Low Voltage Differential Signaling) streams, synchronized with a phase-locked transmit clock transmitted over a fifth LVDS link. This architecture make it ideal for high-bandwidth applications like video interfaces and network equipment.[16]

Key innovations include an **80% cable reduction** (from 58 conductors to just 11) through LVDS multiplexing, significantly lowering system costs and EMI. The DS90CR285 pairs with the **DS90CR286 deserializer** to form a complete Channel Link™ solution.

### 5.2.2 Functional Block Diagram

Below is the Functional Block Diagram of the DS90CR285, Rising Edge Data Strobe LVDS 28-Bit Channel Link - Serializer.

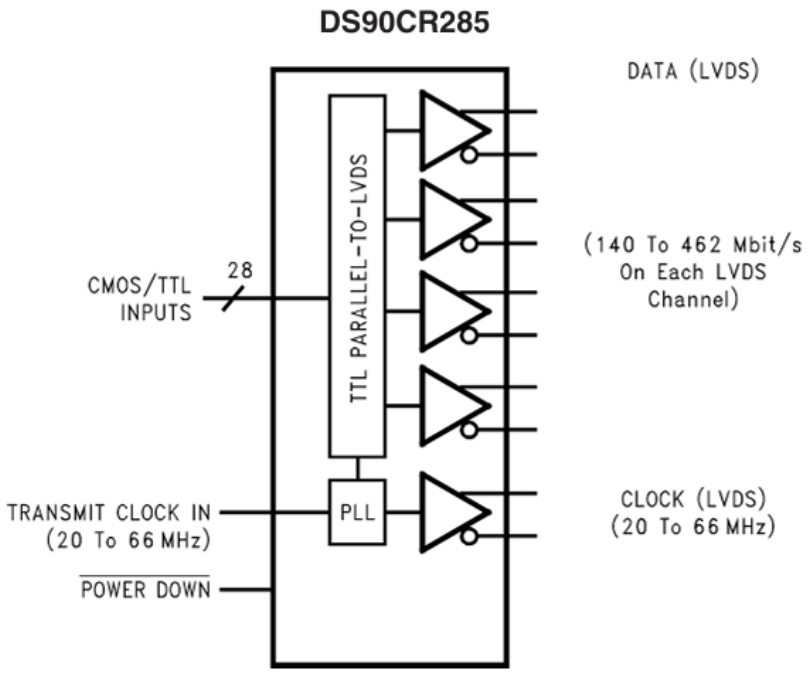



Figure 5.7: Functional Block Digram of DS90CR285

### 5.2.3 Features

- 28-bit parallel-to-4x LVDS serialization
- 5V-tolerant CMOS/TTL inputs
- 80% cable reduction (11 conductors vs. 58 single-ended)
- **7:1 Multiplexing Ratio**: Each LVDS channel carries 7 bits per clock cycle (4 channels $\times$ 7 bits = 28 total bits)
- **Rising Edge Clocking**: Samples data on rising edge of transmit clock (20MHz to 66MHz range) synchronized with data streams
- **7:1 Clock Scaling**: Serializes 28-bit parallel data sampled at input clock frequency $f_{in}$ (20-66MHz) into 4 LVDS channels transmitting at $7 \times f_{in}$ (140-462Mbps per channel)

### 5.2.4 Verilog Code

```
module ds90cr285(
    input wire clk_in,
    input wire clk_in_7x,
    input wire reset,
    input wire [27:0] data_in,
    output reg [3:0] lvds_data_p,
    output reg [3:0] lvds_data_n,
    output wire clk_out_p,
    output wire clk_out_n
);

    reg [6:0] ch0, ch1, ch2, ch3;
    reg [2:0] bit_idx;
    reg load;

    always @(posedge clk_in or posedge reset) begin
        if (reset) begin
            ch0 <= 7'd0;
            ch1 <= 7'd0;
            ch2 <= 7'd0;
            ch3 <= 7'd0;
            bit_idx <= 3'd0;
            load <= 1'b0;
        end else begin
            ch0 <= data_in[6:0];
            ch1 <= data_in[13:7];
            ch2 <= data_in[20:14];
            ch3 <= data_in[27:21];
            bit_idx <= 3'd0;
            load <= 1'b1;
        end
    end

```

```
34      always @(posedge clk_in_7x or posedge reset) begin
35          if (reset) begin
36              lvds_data_p <= 4'b0000;
37              lvds_data_n <= 4'b1111;
38              bit_idx <= 3'd0;
39              load <= 1'b0;
40          end else if (load) begin
41              lvds_data_p[0] <= ch0[6 - bit_idx];
42              lvds_data_p[1] <= ch1[6 - bit_idx];
43              lvds_data_p[2] <= ch2[6 - bit_idx];
44              lvds_data_p[3] <= ch3[6 - bit_idx];
45
46              lvds_data_n[0] <= ~ch0[6 - bit_idx];
47              lvds_data_n[1] <= ~ch1[6 - bit_idx];
48              lvds_data_n[2] <= ~ch2[6 - bit_idx];
49              lvds_data_n[3] <= ~ch3[6 - bit_idx];
50
51
52              if (bit_idx == 3'd6) begin
53                  load <= 1'b0;
54              end else begin
55                  bit_idx <= bit_idx + 1;
56              end
57          end
58      end
59
60      assign clk_out_p = clk_in_7x;
61      assign clk_out_n = ~clk_in_7x;
62
63  endmodule
```

Listing 5.2: Verilog Code for DS90CR285 LVDS 28-Bit Channel Link Serializer

### 5.2.5 Simulation Waveforms

Below are the Simulation Waveforms of the Icarus Verilog, which is showcasing the accurate functional behaviour of the DS90CR285, Rising Edge Data Strobe LVDS 28-Bit Channel Link - Serializer.

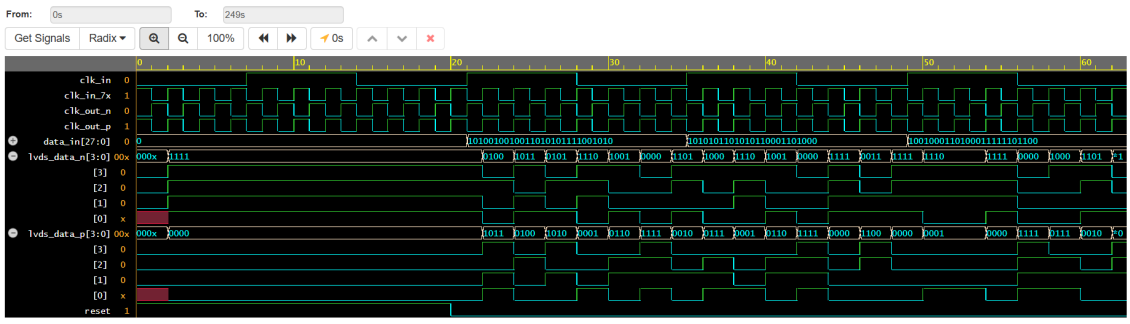



Figure 5.8: Simulation result from Icarus Verilog

### 5.2.6 NgVeri Model

Below is the NgVeri Model created for the IC - DS90CR285.

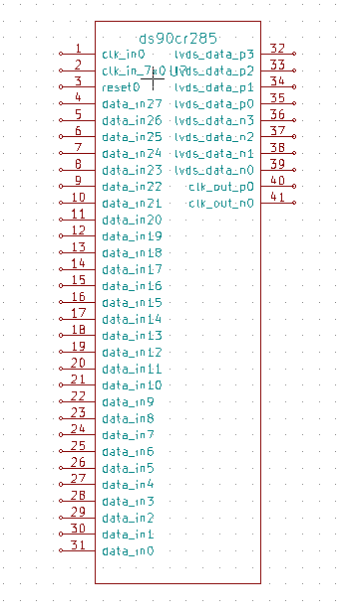



Figure 5.9: NgVeri Model of DS90CR285

### 5.2.7 Test Circuit

Below is the test circuit for the DS90CR285 Rising Edge Data Strobe LVDS 28-Bit Channel Link - Serializer, designed to validate Parallel - to - Serial Conversion for high speed data transmission.

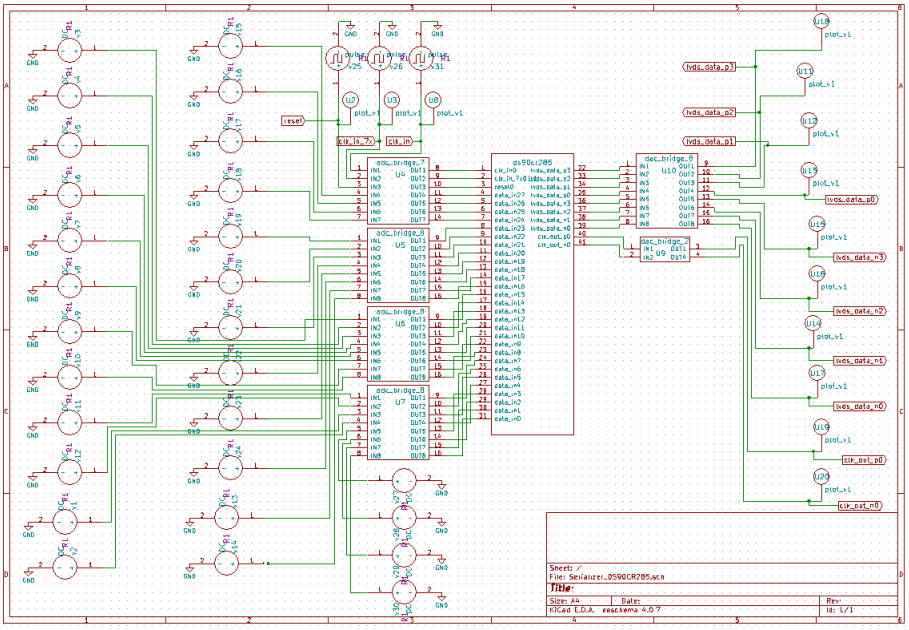


Figure 5.10: Test Circuit of DS90CR285

### 5.2.8 NgSpice Simulation Results

Below are the NgSpice simulation results for the above Test Circuit of DS90CR285 - Rising Edge Data Strobe LVDS 28-Bit Channel Link - Serializer.

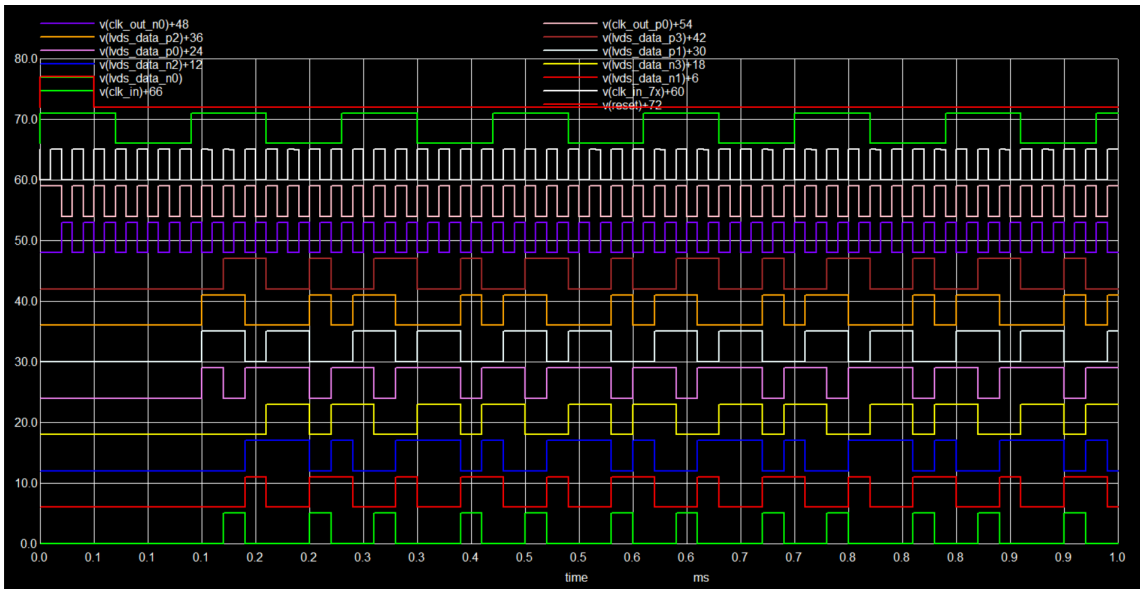



Figure 5.11: NgSpice Simulation result of DS90CR285

```
==========ds90cr285 : New Iteration========
Instance : 0

Inside foo before eval.....
clk_in=1
clk_in_7x=1
reset=0
data_in=106477149
lvds_data_p=1
lvds_data_n=14
clk_out_p=1
clk_out_n=0

Inside foo after eval.....
clk_in=1
clk_in_7x=1
reset=0
data_in=106477149
lvds_data_p=1
lvds_data_n=14
clk_out_p=1
clk_out_n=0
```

Figure 5.12: Ngspice Simulation result of DS90CR285

### 5.2.9 Conclusion

The DS90CR285 serializer serves as a high-performance interface solution in digital system design, offering high-speed, low-EMI, and cable-efficient data transmission. Its use in this project enables reliable parallel-to-serial conversion for long-distance signaling, helping maintain signal integrity and reducing system interconnect complexity while maximizing bandwidth efficiency.

## 5.3 DS90CR286

**Description:** Rising Edge Data Strobe LVDS 28-Bit Channel Link - Deserializer

### 5.3.1 General Description

The DS90CR286 is a high-speed LVDS-to-28-bit LVCMOS/LVTTL deserializer designed to complement the DS90CR285 in robust data transmission systems. It reconstructs parallel data from four serialized LVDS streams using a LVDS clock received via a fifth LVDS link, enabling seamless conversion back to 28-bit wide parallel output.[17]

### 5.3.2 Functional Block Diagram

Below is the Functional Block Diagram of the DS90CR286, Rising Edge Data Strobe LVDS 28-Bit Channel Link - Deserializer.

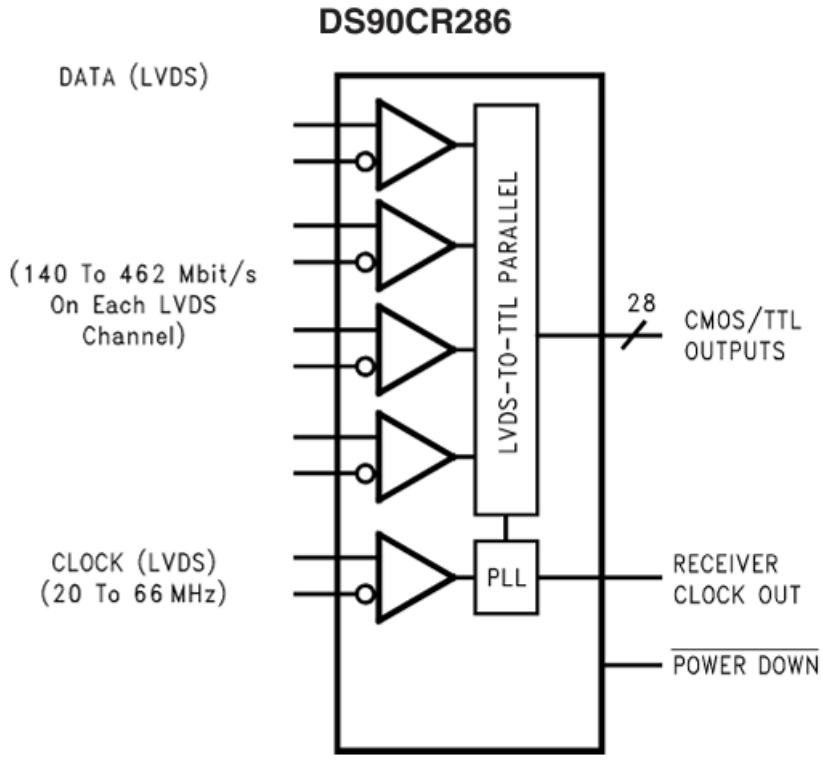



Figure 5.13: Functional Block Digram of DS90CR286

### 5.3.3 Features

- 4x LVDS-to-28-bit parallel deserialization
- Maintains 80% cable reduction benefit (11 conductors)
- **1:7 Demultiplexing Ratio**: Each LVDS channel reconstructs 7 bits per clock cycle (4 channels $\times$ 7 bits = 28 total bits)

- **1:7 Clock Descaling**: Receives 4 LVDS channels at $7 \times f_{in}$ (140-462Mbps) and outputs 28-bit parallel data at base frequency $f_{in}$

### 5.3.4 Verilog Code

```
1
2  module ds90cr286(
3      input wire clk_in,
4      input wire clk_lvds_p,
5      input wire clk_lvds_n,
6      input wire reset,
7      input wire [3:0] lvds_data_p,
8      input wire [3:0] lvds_data_n,
9      output reg [27:0] data_out,
10     output wire clk_out
11 );
12
13     reg [6:0] ch0, ch1, ch2, ch3;
14     reg [2:0] bit_idx;
15     reg load;
16
17     always @(posedge clk_in or posedge reset) begin
18         if (reset)
19             load <= 1'b0;
20         else
21             load <= 1'b1;
22     end
23
24     always @(posedge clk_lvds_p or posedge reset) begin
25         if (reset) begin
26             bit_idx <= 3'd0;
27             ch0 <= 7'd0;
28             ch1 <= 7'd0;
29             ch2 <= 7'd0;
30             ch3 <= 7'd0;
31         end else if (load) begin
32             ch0[6 - bit_idx] <= lvds_data_p[0];
33             ch1[6 - bit_idx] <= lvds_data_p[1];
34             ch2[6 - bit_idx] <= lvds_data_p[2];
35             ch3[6 - bit_idx] <= lvds_data_p[3];
36
37             if (bit_idx == 3'd6)
38                 bit_idx <= 3'd0;
39             else
40                 bit_idx <= bit_idx + 1;
41         end
42     end
43
44     always @(posedge clk_in or posedge reset) begin
45         if (reset)
46             data_out <= 28'd0;
```

```
47          else if (bit_idx == 3'd0 && load)  // bit_idx wrapped:
                7 bits done
48              data_out <= {ch3, ch2, ch1, ch0};
49      end
50
51      assign clk_out = clk_in;
52  endmodule
```

Listing 5.3: Verilog Code for DS90CR286 LVDS 28-Bit Channel Link Deserializer

### 5.3.5 Simulation Waveforms

Below are the Simulation Waveforms of the Icarus Verilog, which is showcasing the accurate functional behaviour of the DS90CR286, Rising Edge Data Strobe LVDS 28-Bit Channel Link - Deserializer.

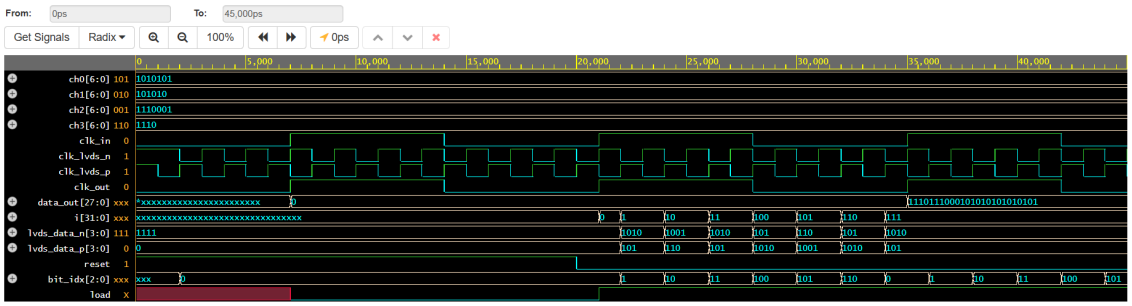



Figure 5.14: Simulation result from Icarus Verilog

### 5.3.6 NgVeri Model

Below is the NgVeri Model created for the IC - DS90CR286.

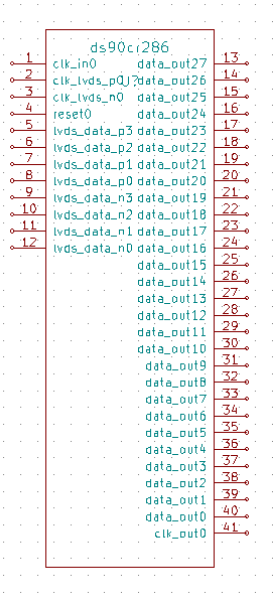



Figure 5.15: NgVeri Model of DS90CR286

### 5.3.7 Test Circuit

Below is the test circuit for the DS90CR286 Rising Edge Data Strobe LVDS 28-Bit Channel Link - Serializer, designed to validate Serial - to - Parallel Conversion for high speed data transmission.

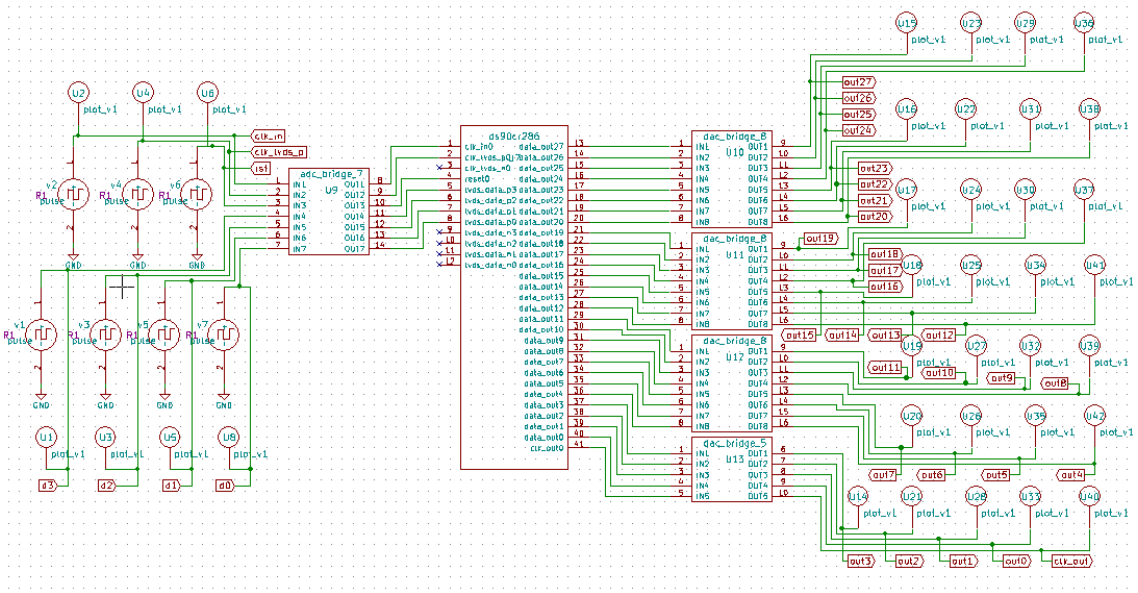


Figure 5.16: Test Circuit of DS90CR286

### 5.3.8 NgSpice Simulation Results

Below are the NgSpice simulation results for the above Test Circuit of DS90CR286 - Rising Edge Data Strobe LVDS 28-Bit Channel Link - Deserializer.

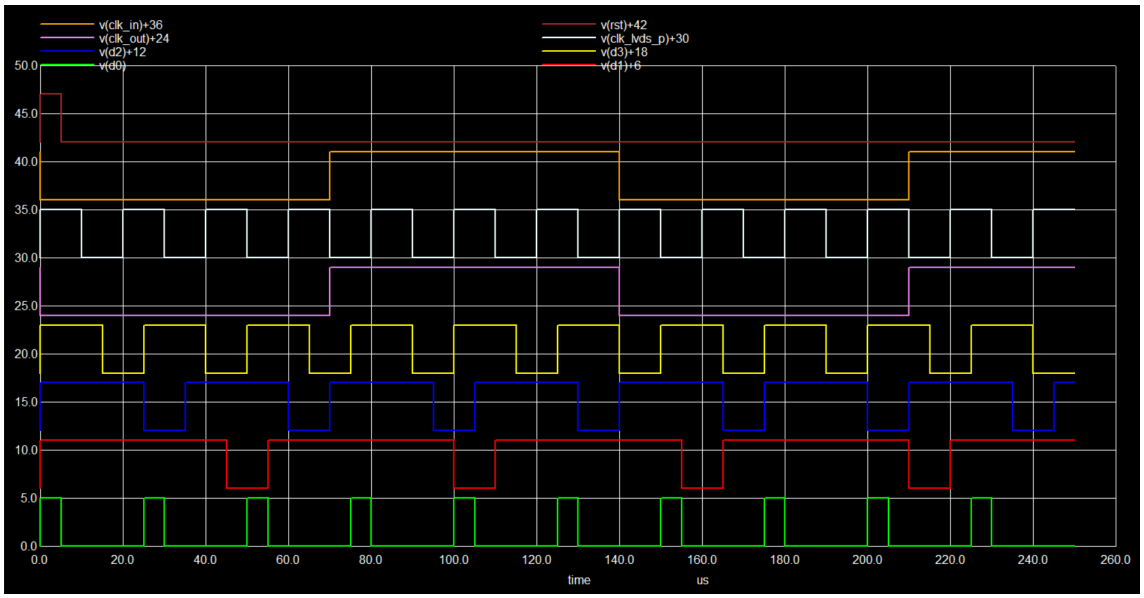



Figure 5.17: NgSpice Simulation result of DS90CR286

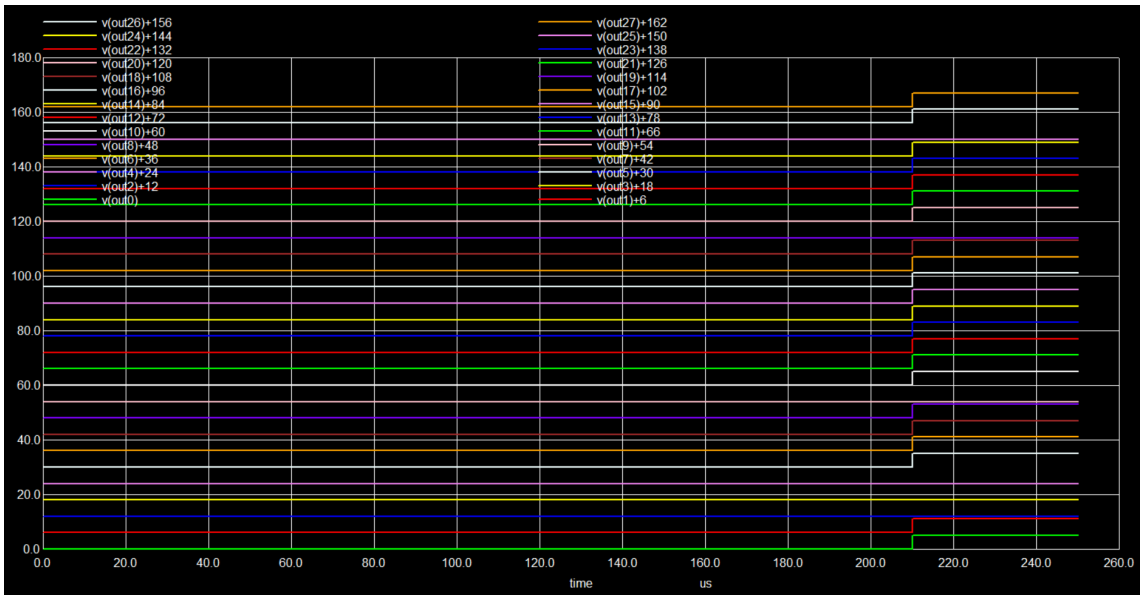



Figure 5.18: NgSpice Simulation result of DS90CR286

```
=============ds90cr286 : New Iteration===========
Instance : 0

Inside foo before eval.....
clk_in=1
clk_lvds_p=1
clk_lvds_n=0
reset=0
lvds_data_p=2
lvds_data_n=0
data_out=234356195
clk_out=1

Inside foo after eval.....
clk_in=1
clk_lvds_p=1
clk_lvds_n=0
reset=0
lvds_data_p=6
lvds_data_n=0
data_out=234356195
clk_out=1
```

Figure 5.19: Ngspice Simulation result of DS90CR286

### 5.3.9 Conclusion

The DS90CR286 deserializer serves as a critical signal reconstruction solution in digital system design, offering high-fidelity serial-to-parallel conversion with exceptional noise immunity and timing accuracy. Its implementation in this project enables robust data recovery over extended distances, ensuring precise signal regeneration while maintaining the serializer's cable efficiency advantages and completing the high-speed transmission link with optimal signal integrity.

# Chapter 6

# Device Modeling

The Device Modeling feature of eSim allows users to create custom semiconductor device models based on datasheet parameters. Using the built-in Model Editor, users can define device parameters such as current gains, saturation currents, breakdown voltages, capacitances, and resistances. The generated models can then be integrated into the eSim library and used for circuit simulation and validation. This feature enables flexibility in simulating devices accurately as per their real-world specifications.

## 6.1 ZTX1048A

**Description:** NPN Silicon Planar medium Power High Gain Transistor.

### 6.1.1 General Description

The ZTX1048A is an NPN silicon planar medium-power transistor designed for high-gain and low saturation voltage applications. This device is particularly suited for power switching and amplification in circuits such as DC-DC converters, LCD backlight drivers, and emergency lighting systems.[18]

### 6.1.2 Typical Applications

- DC-DC converters
- LCD backlight drivers
- Power switching circuits

### 6.1.3 SPICE Model Implementation

#### 6.1.3.1 SPICE Model Parameters

Below is the Spice model parameter list with their corresponding Description, Values and units.

Table 6.1: SPICE Model Parameters of ZTX1048A NPN Transistor

| Parameter | Description | Value | Unit |
|---|---|---|---|
| IS | Saturation current | $13.73 \times 10^{-13}$ | A |
| NF | Forward emission coefficient | 1.0 | – |
| BF | Forward beta (current gain) | 550 | – |
| IKF | Corner for high injection | 8.0 | A |
| VAF | Forward Early voltage | 120 | V |
| ISE | Base-emitter leakage saturation current | $2.6 \times 10^{-13}$ | A |
| NE | B-E leakage emission coefficient | 1.38 | – |
| NR | Reverse emission coefficient | 1.0 | – |
| BR | Reverse beta | 300 | – |
| IKR | Corner for reverse high injection | 6.0 | A |
| VAR | Reverse Early voltage | 15 | V |
| ISC | Base-collector leakage saturation current | $1.6 \times 10^{-12}$ | A |
| RB | Base resistance | 0.1 | Ω |
| RE | Emitter resistance | 0.022 | Ω |
| RC | Collector resistance | 0.010 | Ω |
| CJC | Base-collector junction capacitance | 136 | pF |
| CJE | Base-emitter junction capacitance | 559.1 | pF |
| MJC | Grading coefficient for CJC | 0.267 | – |
| VJC | Junction potential (B-C) | 0.420 | V |
| VJE | Junction potential (B-E) | 0.533 | V |
| TF | Forward transit time | 600 | ps |
| TR | Reverse transit time | 3 | ns |
| Vceo | Collector-emitter breakdown voltage | 17.5 | V |
| Icrating | Maximum collector current rating | 5 | A |
| NC | Base-collector capacitance coefficient | 1.4 | – |
| MJE | Grading coefficient for CJE | 0.299 | – |
| mfg | Manufacturer | Zetex | – |

#### 6.1.3.2 SPICE Model

The Gummel poom model for the ZTX1048A NPN Transistor is as follows:

**SPICE Model: ZTX1048A NPN Silicon Planar Transistor**

```
.MODEL ZTX1048A NPN( IS=13.73E-13 NF=1.0 BF=550 IKF=8.0
VAF=120 ISE=2.6E-13 NE=1.38 NR=1.0 BR=300 IKR=6 VAR=15
ISC=1.6E-12 RB=0.1 RE=0.022 RC=0.010 CJC=136E-12
CJE=559.1E-12 MJC=0.267 VJC=0.420 VJE=0.533 TF=600E-12
TR=3E-9 Vceo=17.5 Icrating=5 NC=1.4 MJE=0.299 mfg=Zetex
)
```

### 6.1.4 Device Model Characterization

The ZTX1048A is a high-gain, low-saturation NPN transistor optimized for low-power switching and amplification applications. Its behavior is analyzed through input/output characteristics and frequency response under both common-emitter (CE) and common-base (CB) configurations.

#### 6.1.4.1 Common-Emitter Configuration

##### 6.1.4.1.1 Input Characteristics:

In the CE configuration, the base-emitter junction acts as a forward-biased diode. The base current ($I_B$) rises exponentially with the base-emitter voltage ($V_{BE}$), following the diode equation:

$$I_B = \frac{I_S}{\beta}\left(e^{\frac{V_{BE}}{nV_T}} - 1\right)$$

Here, $I_S$ is the reverse saturation current, $\beta$ is the current gain, $n$ is the emission coefficient, and $V_T$ is the thermal voltage. For the ZTX1048A, high $\beta$ ensures significant amplification with minimal base current, making it ideal for low-drive signal inputs.

The following is the input characteristic analysis setup for the ZTX1048A NPN transistor configured in common-emitter mode. The circuit is designed to observe the variation of base current ($I_B$) with base-emitter voltage ($V_{BE}$) at constant collector-emitter voltage.

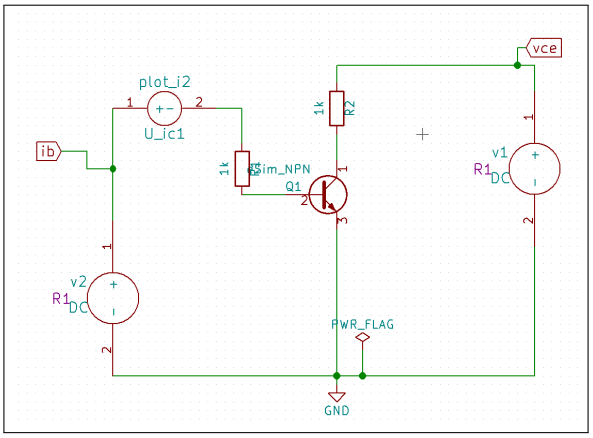



Figure 6.1: Input characteristic circuit for ZTX1048A in CE configuration

Below is the NgSpice simulation result of the input characteristics circuit. The plot shows the exponential relationship between $I_B$ and $V_{BE}$.

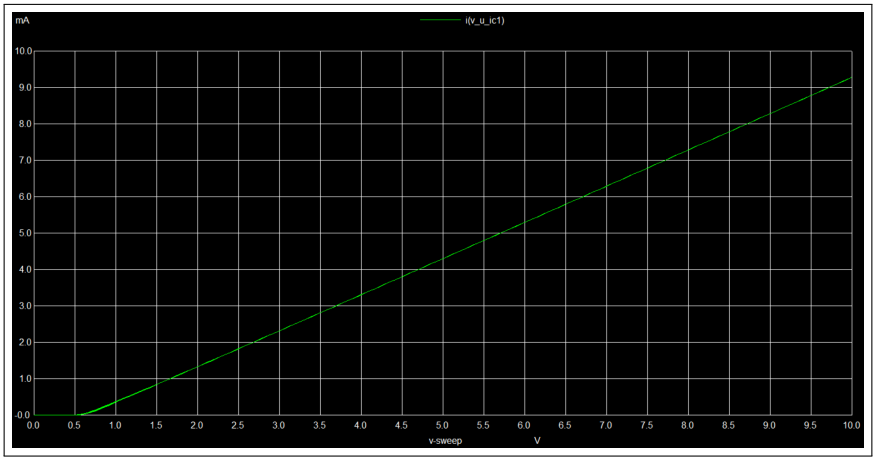



Figure 6.2: NgSpice simulation of input characteristics for ZTX1048A in CE configuration

#### 6.1.4.1.2 Output Characteristics:

The collector current ($I_C$) is controlled by $I_B$ and varies with collector-emitter voltage ($V_{CE}$), as described by:

$$I_C = I_S e^{\frac{V_{BE}}{V_T}} \left(1 + \frac{V_{CE}}{V_A}\right)$$

where $V_A$ is the Early voltage. The output characteristics exhibit three regions—cutoff ($I_C \approx 0$), active (linear amplification), and saturation (both junctions forward-biased). The ZTX1048A exhibits a pronounced active region and low $V_{CE(sat)}$, ensuring sharp switching and efficient analog gain. The output resistance due to the Early effect is given by:

$$r_o = \frac{V_A}{I_C}$$

The following is the output characteristic analysis setup for the ZTX1048A NPN transistor in common-emitter configuration. The circuit is designed to observe the variation of collector current ($I_C$) with collector-emitter voltage ($V_{CE}$) at constant base current ($I_B$).

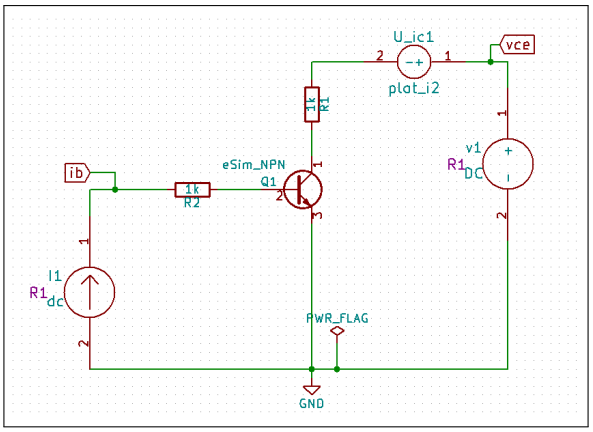



Figure 6.3: Output characteristic circuit for ZTX1048A in CE configuration

Below is the NgSpice simulation result of the output characteristics circuit. The plot demonstrates the transistor's operating regions: cutoff, active, and saturation.

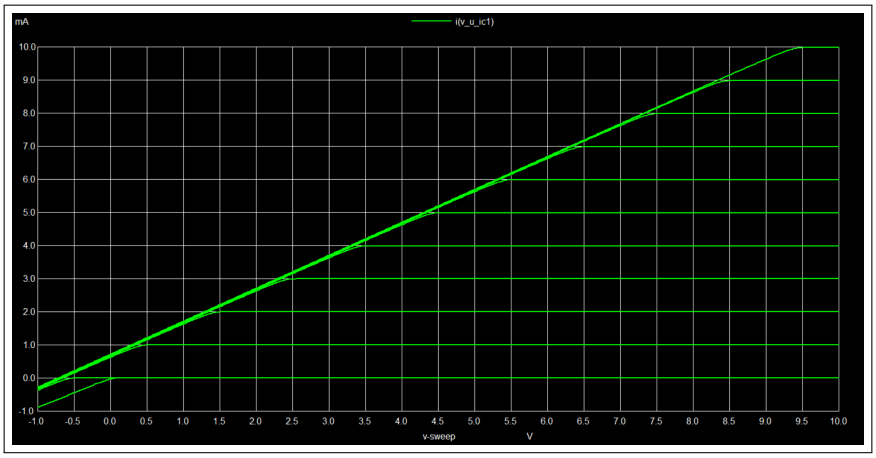



Figure 6.4: NgSpice simulation of output characteristics for ZTX1048A in CE configuration

#### 6.1.4.2 Common-Base Configuration

##### 6.1.4.2.1 Input Characteristics:

In the CB configuration, the input is applied between the emitter and base. The emitter current ($I_E$) increases exponentially with emitter-base voltage ($V_{EB}$), following:

$$I_E = I_S \left( e^{\frac{V_{EB}}{nV_T}} - 1 \right)$$

Due to low input resistance and high current gain ($\alpha \approx 1$), this configuration is suited for high-frequency operation. The ZTX1048A provides fast response and low input delay, benefiting RF amplifier applications.

The following setup is used to analyze the input characteristics of the ZTX1048A NPN transistor in common-base mode. The circuit examines the variation of emitter current ($I_E$) with emitter-base voltage ($V_{EB}$) while maintaining a constant collector-base voltage ($V_{CB}$).

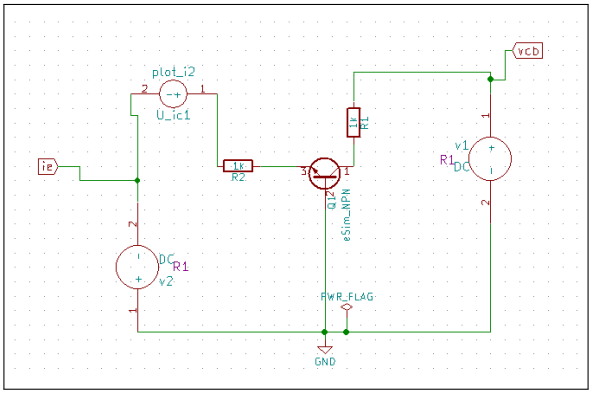



Figure 6.5: Input characteristic circuit for ZTX1048A in CB configuration

Below is the NgSpice simulation result of the above circuit, showing the exponential relationship between $I_E$ and $V_{EB}$.

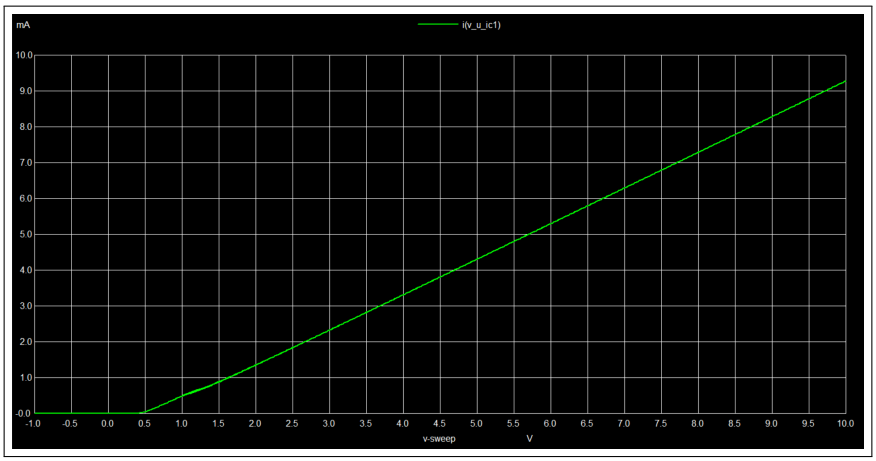



Figure 6.6: NgSpice simulation of input characteristics for ZTX1048A in CB configuration

#### 6.1.4.2.2 Output Characteristics:

In the CB output curves, the collector current ($I_C$) is primarily a function of emitter current ($I_E$) and collector-base voltage ($V_{CB}$). The active region behavior is given by:

$$I_C = \alpha I_E + I_{CBO}$$

where $I_{CBO}$ is the leakage current with the emitter open. The nearly flat output curves reflect the high output impedance, low gain variation, and improved linearity of the ZTX1048A in CB mode, which is particularly beneficial in wideband amplification.

This circuit is designed to evaluate the output characteristics of the ZTX1048A transistor in common-base configuration. It shows how the collector current ($I_C$) varies with collector-base voltage ($V_{CB}$) at different emitter current ($I_E$) levels.

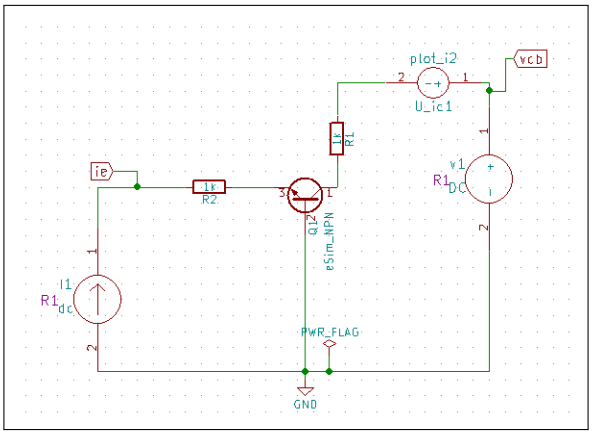



Figure 6.7: Output characteristic circuit for ZTX1048A in CB configuration

The plot below from NgSpice simulation highlights the transistor's active region behavior and nearly constant $I_C$ for a given $I_E$.

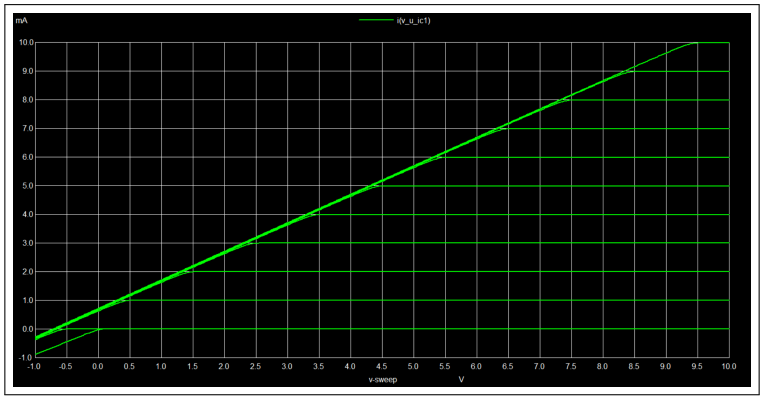



Figure 6.8: NgSpice simulation of output characteristics for ZTX1048A in CB configuration

#### 6.1.4.3 Frequency Response

The frequency response is a key performance metric of the ZTX1048A. The transistor maintains high gain up to its transition frequency ($f_T$), defined as the frequency at which the current gain drops to unity:

$$f_T = \frac{1}{2\pi(r_b + r_e)(C_{be} + C_{bc})}$$

Here, $r_b$ and $r_e$ are the base and emitter resistances, and $C_{be}$, $C_{bc}$ are the internal junction capacitances. The ZTX1048A achieves high $f_T$ due to low parasitic elements, making it suitable for RF, fast-switching, and pulse amplification circuits.

In CE configuration, bandwidth is reduced due to Miller multiplication of $C_{bc}$. However, the CB configuration avoids this effect, offering significantly higher bandwidth. This makes the ZTX1048A ideal for use in high-speed analog interfaces, mixers, and communication front-ends.

The circuit shown below is used to analyze the frequency response of the ZTX1048A in a common-emitter amplifier configuration. The analysis helps determine the gain variation with frequency and the upper cut-off point beyond which the gain drops significantly.

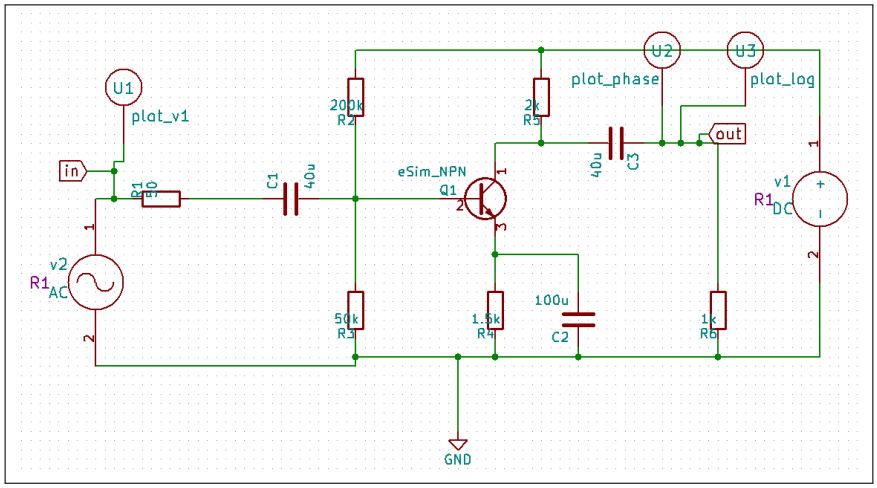



Figure 6.9: Circuit used for frequency response analysis of ZTX1048A

The simulation below illustrates the frequency response obtained via AC analysis in NgSpice, showing the gain (in dB) versus frequency curve.

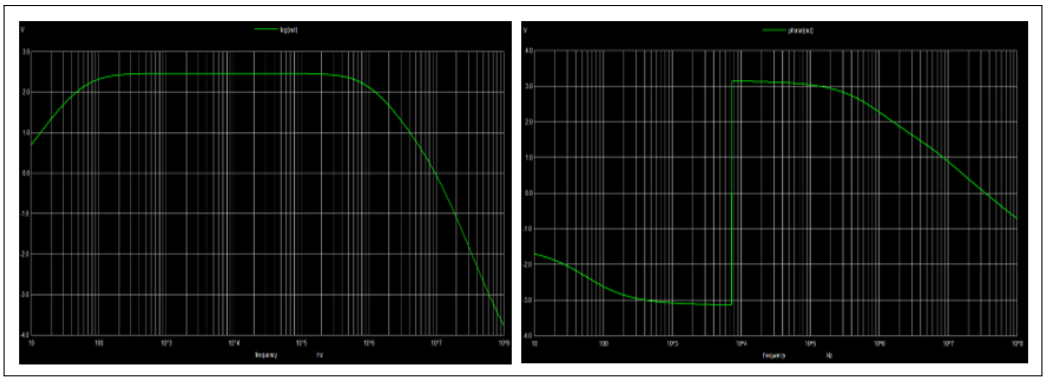


Figure 6.10: NgSpice simulation result showing frequency response of ZTX1048A

### 6.1.5 Application Circuit: Amplifier Design

The ZTX1048A transistor is used in a common-emitter configuration to form an inverting amplifier. The input signal is applied to the base, and the output is taken from the collector. This setup provides voltage gain with a 180° phase shift between input and output, making it suitable for small-signal amplification. This setup is widely used in analog signal amplification.

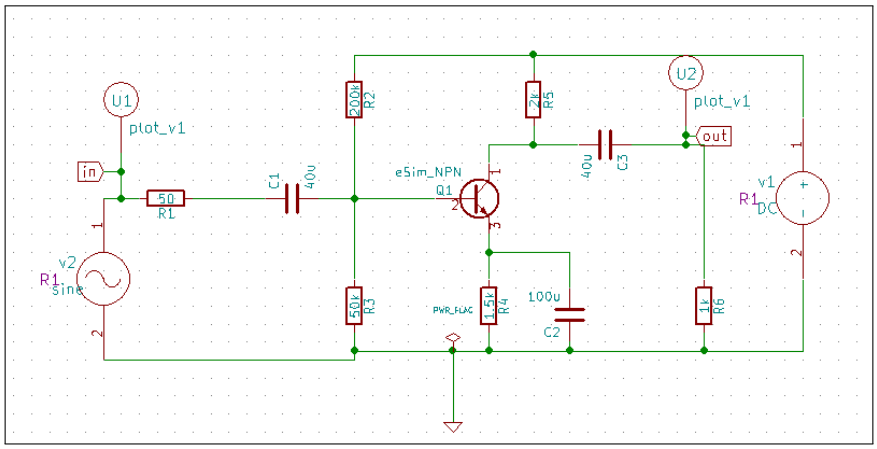



Figure 6.11: Common-emitter inverting amplifier using ZTX1048A

The figure below shows the NgSpice simulation result, where the output waveform exhibits amplified signal characteristics with a 180° phase shift relative to the input.

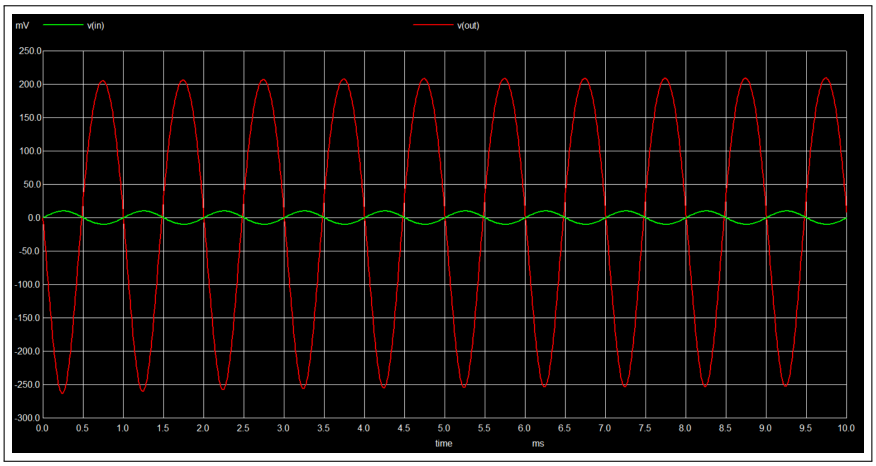



Figure 6.12: NgSpice simulation showing output waveform of ZTX1048A in amplifier configuration

## 6.2 2N3055

**Description:** NPN Silicon Power Transistor

### 6.2.1 General Description

The **2N3055** is a silicon NPN power transistor manufactured using epitaxial-base planar technology. It is widely used in general-purpose applications such as linear and switching power amplifiers. The device features high collector current capability and low collector-emitter saturation voltage, making it suitable for high-power audio, driver, and output stages.[19]

This transistor is offered in a robust TO-3 metal package and is commonly paired with its complementary PNP counterpart, the MJ2955. Its high reliability, thermal performance, and current handling make it a standard choice in industrial and consumer electronic designs.

### 6.2.2 Typical Applications

- Power amplifiers (especially in audio output stages)
- Linear voltage regulators and power supplies
- DC motor control circuits
- Switching regulators and converters
- Battery chargers
- Inverter circuits

### 6.2.3 SPICE Model Implementation

#### 6.2.3.1 SPICE Model Parameters

Below is the SPICE model parameter list, providing a detailed overview of each parameter used in the simulation. It includes the parameter name, its physical meaning or description, corresponding value, and the associated unit. This information is essential for accurately modeling and analyzing electronic device behavior. Proper interpretation of these parameters ensures realistic and reliable circuit simulation results

Table 6.2: SPICE Model Parameters of 2N3055 NPN Transistor

| Parameter | Description | Value | Unit |
|---|---|---|---|
| BF | Forward beta (DC current gain) | 73 | – |
| BR | Reverse beta | 2.66 | – |
| RB | Base resistance | 0.81 | Ω |
| RC | Collector resistance | 0.0856 | Ω |
| RE | Emitter resistance | 0.000856 | Ω |
| CJC | Base–collector junction capacitance | 1000 | pF |
| PC | Capacitance coefficient (CJC) | 0.75 | – |
| MC | Grading coefficient for CJC | 0.33 | – |
| b TR | Reverse transit time | 0.5703 | s |
| IS | Saturation current | $2.37 \times 10^{-8}$ | A |
| CJE | Base–emitter junction capacitance | 415 | pF |
| PE | Junction potential (B–E) | 0.75 | V |
| ME | Grading coefficient for CJE | 0.5 | – |
| TF | Forward transit time | 99.52 | ns |
| NE | Emission coefficient | 1.26 | – |
| IK | Corner current for high injection | 1 | A |
| Vceo | Collector–emitter breakdown voltage | 60 | V |
| Icrating | Maximum collector current rating | 10 | A |
| mfg | Manufacturer | STMicro | – |

#### 6.2.3.2 SPICE Model

The Gummel poom model for the 2N3055 Silicon NPN Power Transistor is as follows:

**SPICE Model: 2N3055 Silicon NPN Power Transistor**

```
.MODEL 2N3055 NPN( Bf=73 Br=2.66 Rb=0.81 Rc=0.0856
Re=0.000856 CJC=1000P PC=0.75 MC=0.33 Tr=0.5703U
Is=2.37E-8 CJE=415P PE=0.75 ME=0.5 TF=99.52N NE=1.26
IK=1 Vceo=60 Icrating=10 mfg=STMicro )
```

### 6.2.4 Device Model Characterization

The 2N3055 is a silicon NPN power transistor designed for high-current, medium-power linear and switching applications. Its performance is evaluated through its input/output characteristics and frequency response under both common-emitter (CE) and common-base (CB) configurations.

#### 6.2.4.1 Common-Emitter Configuration

##### 6.2.4.1.1 Input Characteristics

In the CE configuration, the base-emitter junction of the 2N3055 exhibits typical diode-like behavior. The base current ($I_B$) increases exponentially with base-emitter voltage ($V_{BE}$), governed by:

$$I_B = \frac{I_S}{\beta}\left(e^{\frac{V_{BE}}{nV_T}} - 1\right)$$

Here, $I_S$ is the reverse saturation current, $\beta$ is the DC current gain, $n$ is the emission coefficient, and $V_T$ is the thermal voltage. Being a power transistor, the 2N3055 requires comparatively higher base current than small-signal BJTs, but still achieves significant collector current due to moderate current gain.

The following setup demonstrates the input characteristics of the 2N3055 transistor in a common-emitter configuration. The circuit investigates the relationship between base current ($I_B$) and base-emitter voltage ($V_{BE}$) at constant $V_{CE}$.

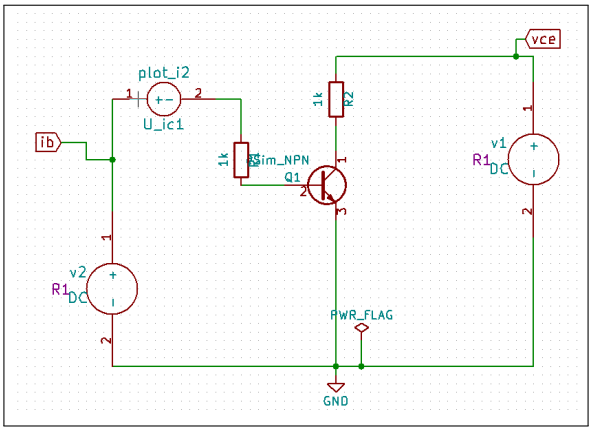



Figure 6.13: Input characteristic circuit for 2N3055 in CE configuration

The plot below shows NgSpice simulation of input characteristics, indicating an exponential rise of $I_B$ with $V_{BE}$.

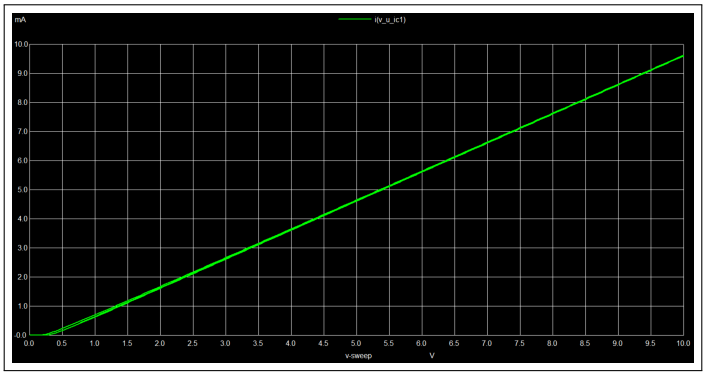



Figure 6.14: NgSpice simulation of CE input characteristics for 2N3055

#### 6.2.4.1.2 Output Characteristics

The collector current ($I_C$) response to collector-emitter voltage ($V_{CE}$) is given by:

$$I_C = I_S e^{\frac{V_{BE}}{V_T}} \left(1 + \frac{V_{CE}}{V_A}\right)$$

The 2N3055 displays three distinct operating regions: cutoff, active, and saturation. In the active region, the device provides linear amplification with good thermal stability, while in saturation, it operates efficiently for switching. The output resistance influenced by the Early effect is expressed as:

$$r_o = \frac{V_A}{I_C}$$

This circuit is used to analyze how collector current ($I_C$) varies with $V_{CE}$ for different $I_B$ values in the 2N3055 common-emitter configuration.

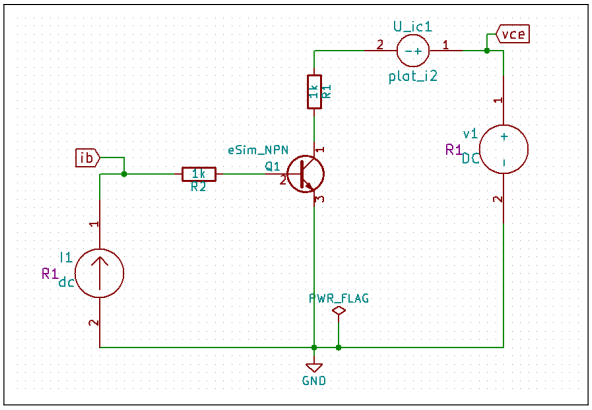



Figure 6.15: Output characteristic circuit for 2N3055 in CE configuration

The NgSpice simulation below displays the $I_C$–$V_{CE}$ curve across multiple $I_B$ levels.

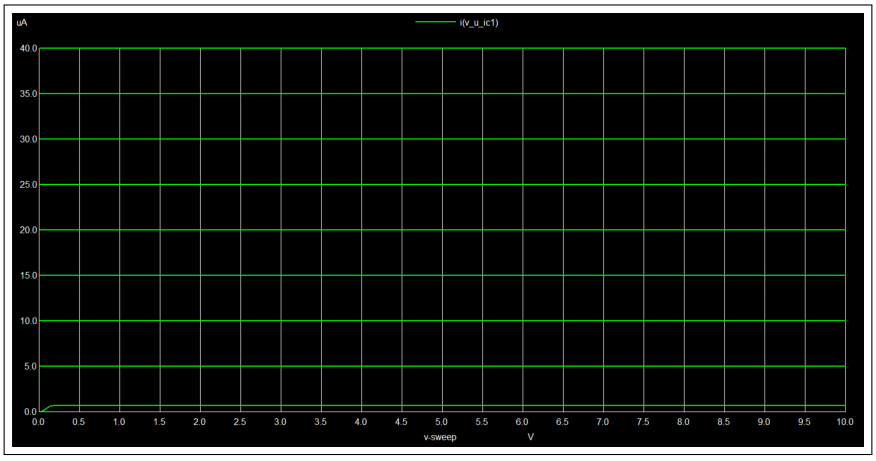



Figure 6.16: NgSpice simulation of CE output characteristics for 2N3055

#### 6.2.4.2 Common-Base Configuration

##### 6.2.4.2.1 Input Characteristics

In CB mode, the emitter current ($I_E$) increases exponentially with emitter-base voltage ($V_{EB}$), following:

$$I_E = I_S \left( e^{\frac{V_{EB}}{nV_T}} - 1 \right)$$

The 2N3055 exhibits low input resistance in this mode and is suitable for applications where low-impedance signal sources are used.

This CB configuration circuit evaluates how emitter current ($I_E$) varies with emitter-base voltage ($V_{EB}$) for constant $V_{CB}$.

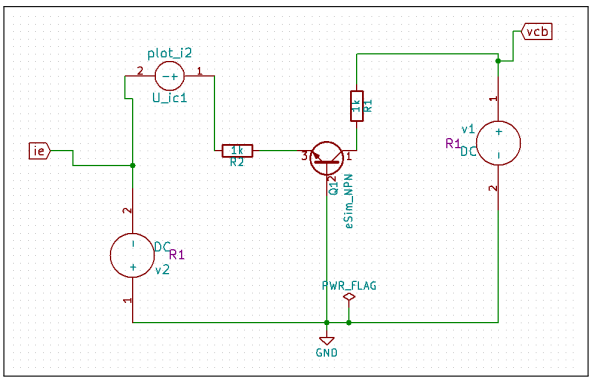



Figure 6.17: Input characteristic circuit for 2N3055 in CB configuration

The simulation below shows the exponential rise of $I_E$ with $V_{EB}$ in CB mode.

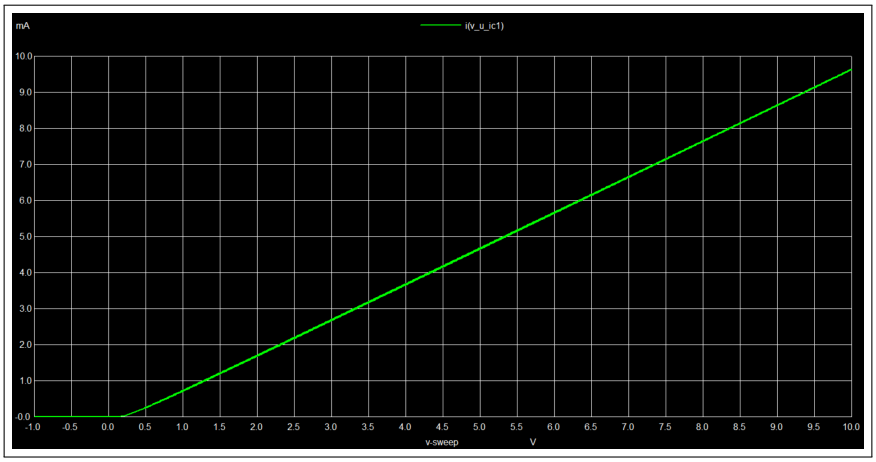



Figure 6.18: NgSpice simulation of CB input characteristics for 2N3055

#### 6.2.4.2.2 Output Characteristics

In the active region of CB configuration, the collector current is related to the emitter current via:

$$I_C = \alpha I_E + I_{CBO}$$

where $\alpha$ is the common-base current gain, and $I_{CBO}$ is the collector-base leakage current. The 2N3055 provides relatively flat $I_C$–$V_{CB}$ curves in active mode, with good power handling capability and low voltage drop in saturation.

In this CB output configuration, the collector current ($I_C$) is analyzed as a function of $V_{CB}$ for fixed $I_E$.

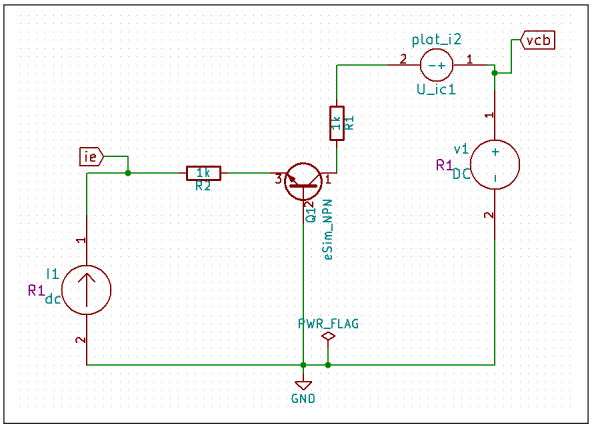



Figure 6.19: Output characteristic circuit for 2N3055 in CB configuration

The NgSpice output shows nearly constant $I_C$ across a range of $V_{CB}$.

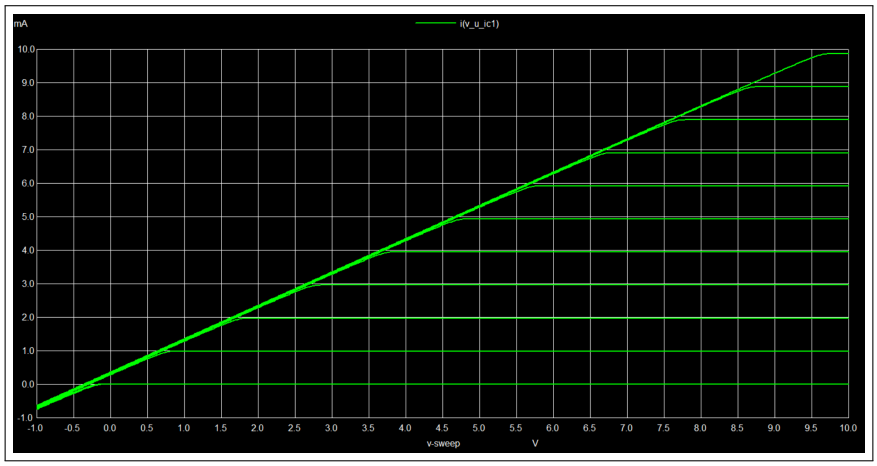



Figure 6.20: NgSpice simulation of CB output characteristics for 2N3055

#### 6.2.4.3 Frequency Response

The frequency response of the 2N3055 is limited by its junction capacitances and transit time. The transition frequency ($f_T$) is relatively low compared to small-signal transistors and is given by:

$$f_T = \frac{1}{2\pi(r_b + r_e)(C_{be} + C_{bc})}$$

Due to larger capacitances and internal resistance, the 2N3055 is generally used below a few hundred kHz. Its frequency response is sufficient for audio amplification, linear power control, and slow switching operations. CE configuration suffers from Miller effect, while CB provides slightly better bandwidth at the cost of lower input impedance.

This circuit setup is used to examine the small-signal frequency response of the 2N3055 configured as a CE amplifier. The analysis identifies gain falloff with frequency and determines the upper cutoff point.

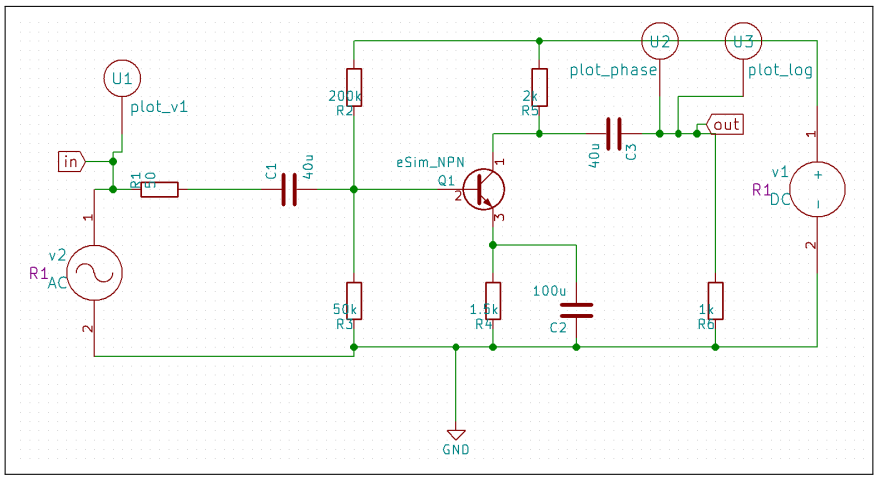



Figure 6.21: Frequency response circuit using 2N3055 in CE mode

The simulation below plots gain (dB) vs. frequency using AC analysis in NgSpice.

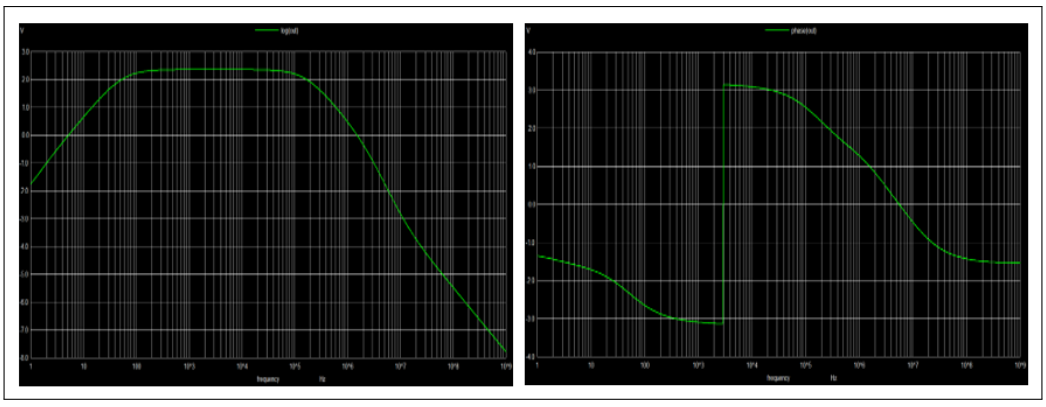


Figure 6.22: NgSpice simulation showing frequency response of 2N3055

### 6.2.5 Application Circuit: Amplifier Design

The 2N3055 can be used in a common-emitter inverting amplifier configuration for medium-power signal amplification. The input signal is applied to the base through a coupling capacitor, and the output is taken across a load connected to the collector. This configuration provides a voltage gain with a 180° phase shift between input and output. Due to its high current capacity and power dissipation, the 2N3055 is suitable for driving low-impedance loads such as motors or speakers in audio amplifiers.

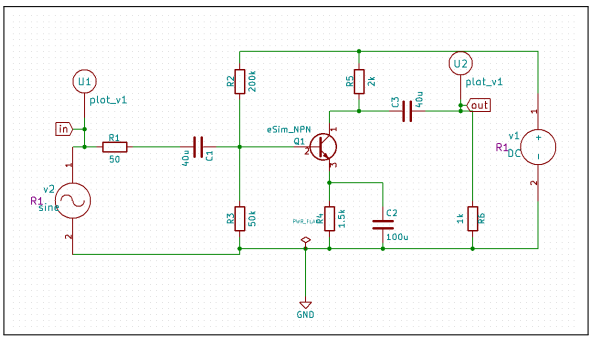



Figure 6.23: Inverting amplifier circuit using 2N3055 in CE configuration

mm The NgSpice waveform below confirms gain and 180° phase shift between input and output.

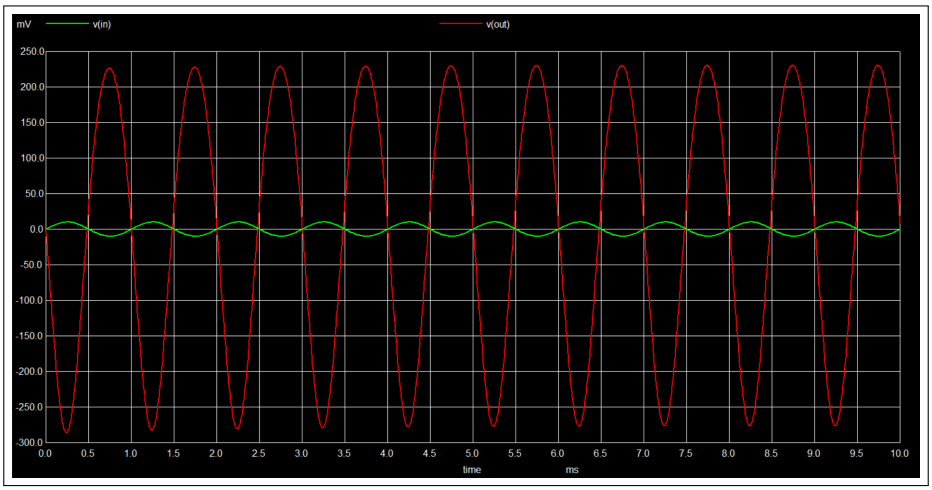



Figure 6.24: NgSpice simulation of amplifier output using 2N3055

## 6.3 2N5401

**Description:** PNP Silicon Epitaxial Planar Transistors

### 6.3.1 General Description

The **2N5401** is a PNP silicon epitaxial planar transistor designed for high-voltage, general-purpose amplification applications. It is optimized for use in audio frequency amplifier stages and other linear circuits where reliable high-voltage operation is essential. Manufactured in a TO-92 plastic package, the device offers good gain characteristics and low saturation voltages, making it suitable for a wide range of applications.[20]

### 6.3.2 Typical Applications

- Audio frequency amplifier stages
- Signal processing circuits
- High-voltage driver stages
- General-purpose switching
- Small motor control circuits
- Complementary pair configuration with NPN transistors (e.g., 2N5551)

### 6.3.3 SPICE Model Implementation

#### 6.3.3.1 SPICE Model Parameters

Below is the Spice model parameter list with their corresponding Description, Values and units.

Table 6.3: SPICE Model Parameters of 2N5401 PNP Transistor

| Parameter | Description | Value | Unit |
|---|---|---|---|
| IS | Saturation current | $2.148 \times 10^{-14}$ | A |
| XTI | Temperature exponent for IS | 3 | – |
| EG | Energy gap | 1.11 | eV |
| VAF | Forward Early voltage | 100 | V |
| BF | Forward beta | 132.1 | – |
| NE | Emission coefficient | 1.375 | – |
| ISE | B-E leakage saturation current | $2.148 \times 10^{-14}$ | A |
| IKF | Corner current for beta roll-off | 0.1848 | A |
| XTB | Temperature coefficient of beta | 1.5 | – |
| BR | Reverse beta | 3.661 | – |
| NC | Base–collector capacitance exponent | 2 | – |
| ISC | B-C leakage saturation current | 0 | A |

| Parameter | Description | Value | Unit |
|---|---|---|---|
| IKR | Corner current for reverse beta roll-off | 0 | A |
| RC | Collector resistance | 1.6 | Ω |
| CJC | Collector–base junction capacitance | 17.63 | pF |
| MJC | Grading coefficient for CJC | 0.5312 | – |
| VJC | Junction potential (B–C) | 0.75 | V |
| FC | Forward-bias depletion coefficient | 0.5 | – |
| CJE | Base–emitter junction capacitance | 73.39 | pF |
| MJE | Grading coefficient for CJE | 0.3777 | – |
| VJE | Junction potential (B–E) | 0.75 | V |
| TR | Reverse transit time | 1.476 | ns |
| TF | Forward transit time | 641.9 | ps |
| ITF | High-current TF corner | 0 | A |
| VTF | TF knee voltage | 0 | V |
| XTF | TF exponential factor | 0 | – |
| RB | Base resistance | 10 | Ω |
| Vceo | Collector–emitter breakdown voltage | 150 | V |
| Icrating | Maximum collector current | 600 | mA |
| mfg | Manufacturer | Fairchild | – |

#### 6.3.3.2 SPICE Model

The Gummel poom model for the 2N5401 PNP Silicon Epitaxial Planar Transistors is as follows:

**SPICE Model: 2N5401 PNP Silicon Epitaxial Planar Transistors**

```
.MODEL 2N5401 PNP( Is=21.48f Xti=3 Eg=1.11 Vaf=100
Bf=132.1 Ne=1.375 Ise=21.48f Ikf=.1848 Xtb=1.5
Br=3.661 Nc=2 Isc=0 Ikr=0 Rc=1.6 Cjc=17.63p Mjc=.5312
Vjc=.75 Fc=.5 Cje=73.39p Mje=.3777 Vje=.75 Tr=1.476n
Tf=641.9p Itf=0 Vtf=0 Xtf=0 Rb=10 Vceo=150 Icrating=600m
mfg=Fairchild )
```

### 6.3.4 Device Model Characterization

The 2N5401 is a PNP silicon epitaxial planar transistor designed for low-noise, medium-voltage amplification in audio and general-purpose circuits. Its performance is analyzed through input/output characteristics and frequency response under both common-emitter (CE) and common-base (CB) configurations, considering its PNP polarity.

#### 6.3.4.1 Common-Emitter Configuration

##### 6.3.4.1.1 Input Characteristics

In the CE configuration, the emitter-base junction of the 2N5401 behaves like a forward-biased diode. For a PNP transistor, the emitter is more positive than the base, and the emitter current ($I_E$) increases exponentially with emitter-base voltage ($V_{EB}$):

$$I_E = \frac{I_S}{\beta}\left(e^{\frac{V_{EB}}{nV_T}} - 1\right)$$

Here, $I_S$ is the reverse saturation current, $\beta$ is the current gain, $n$ is the emission coefficient, and $V_T$ is the thermal voltage. The 2N5401, with its moderate gain and low noise profile, is ideal for signal amplification applications.

The circuit below is used to analyze the input characteristics of the 2N5401 transistor in a common-emitter configuration. It illustrates how the base current ($I_B$) changes with base-emitter voltage ($V_{BE}$) at a fixed $V_{CE}$.

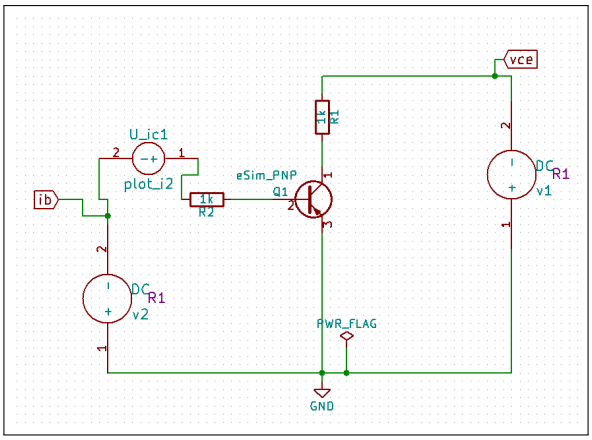



Figure 6.25: Input characteristic circuit for 2N5401 in CE configuration

The NgSpice simulation below shows the exponential variation of $I_B$ with $V_{BE}$, characteristic of a forward-biased PNP junction.

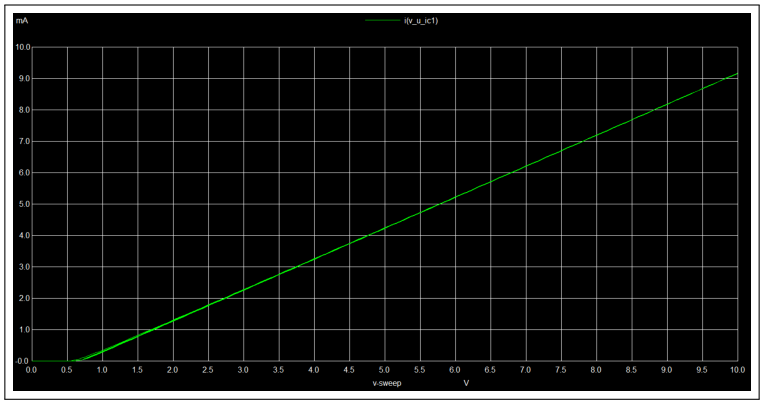



Figure 6.26: NgSpice simulation of CE input characteristics for 2N5401

#### 6.3.4.1.2 Output Characteristics

The collector current ($I_C$) in a PNP device decreases (flows into the collector) as the collector-emitter voltage ($V_{EC}$) becomes more negative. The expression is:

$$I_C = I_S e^{\frac{V_{EB}}{V_T}} \left(1 + \frac{V_{EC}}{V_A}\right)$$

The output characteristics show cutoff, active, and saturation regions, with good linearity in the active region. The Early effect is modeled by:

$$r_o = \frac{V_A}{I_C}$$

The 2N5401 offers stable gain in the active region, and its low saturation voltage ensures efficient operation in low-power amplifier stages.

This configuration studies the variation of collector current ($I_C$) with $V_{CE}$ at fixed base current levels. For a PNP transistor like 2N5401, current direction is reversed compared to NPN.

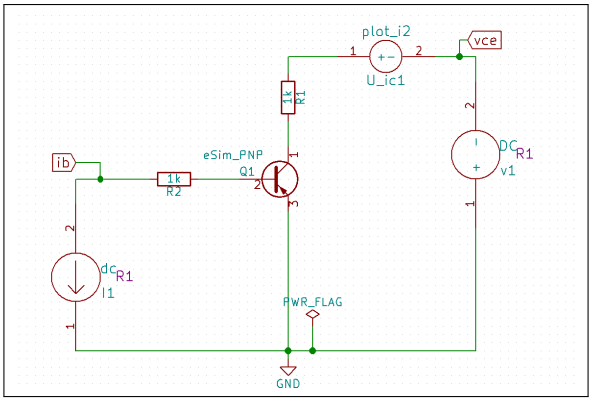



Figure 6.27: Output characteristic circuit for 2N5401 in CE configuration

Below is the simulation result depicting how $I_C$ increases with decreasing $V_{CE}$ (since PNP conduction is opposite to NPN).

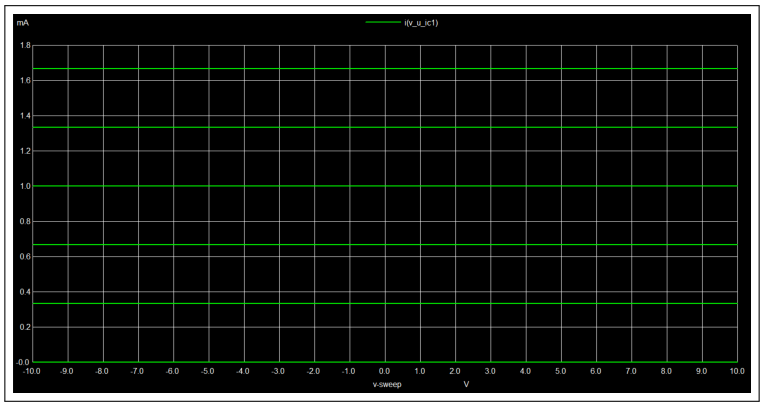



Figure 6.28: NgSpice simulation of CE output characteristics for 2N5401

#### 6.3.4.2 Common-Base Configuration

##### 6.3.4.2.1 Input Characteristics

In CB configuration, the emitter current ($I_E$) depends on the emitter-base voltage ($V_{EB}$), and the junction must be forward-biased (emitter positive relative to base):

$$I_E = I_S \left( e^{\frac{V_{EB}}{nV_T}} - 1 \right)$$

Due to the low input resistance, the 2N5401 is suited for wideband signal input and buffering applications in this configuration.

This setup observes how the emitter current ($I_E$) varies with emitter-base voltage ($V_{EB}$) at a fixed $V_{CB}$ in a common-base configuration.

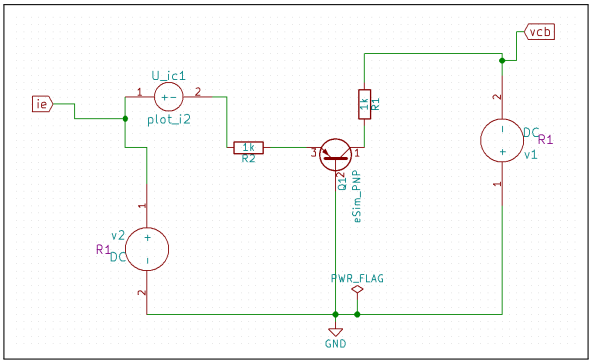



Figure 6.29: Input characteristic circuit for 2N5401 in CB configuration

The simulation result reflects a diode-like exponential rise of $I_E$ with $V_{EB}$ in the forward-biased mode.

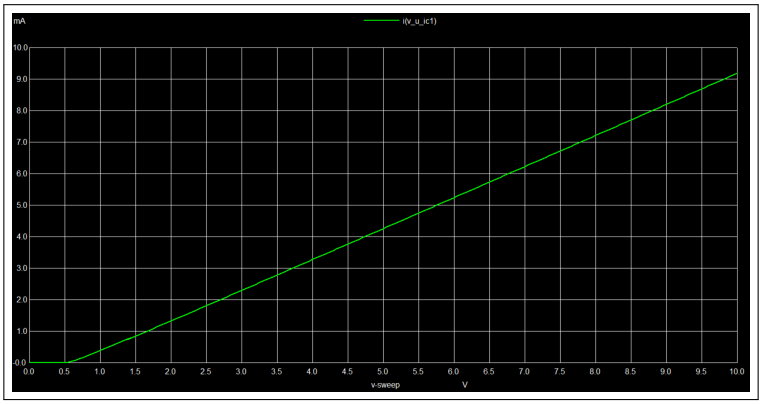



Figure 6.30: NgSpice simulation of CB input characteristics for 2N5401

#### 6.3.4.2.2 Output Characteristics

The collector current in the CB configuration is determined by the emitter current and collector-base voltage ($V_{CB}$):

$$I_C = \alpha I_E + I_{CBO}$$

where $\alpha$ is the common-base gain (close to 1), and $I_{CBO}$ is the leakage current. The 2N5401 exhibits stable output behavior with high output resistance, ideal for small-signal high-gain amplifier stages.

This section evaluates collector current variation with collector-base voltage ($V_{CB}$) at fixed emitter current ($I_E$) in CB mode.

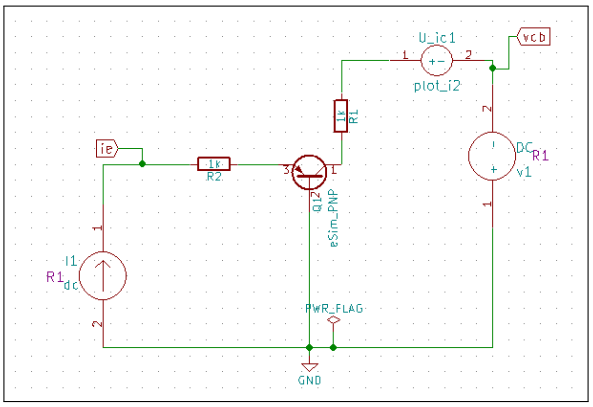



Figure 6.31: Output characteristic circuit for 2N5401 in CB configuration

The plot below shows nearly constant $I_C$ values in the active region, demonstrating good current transfer at high output impedance.

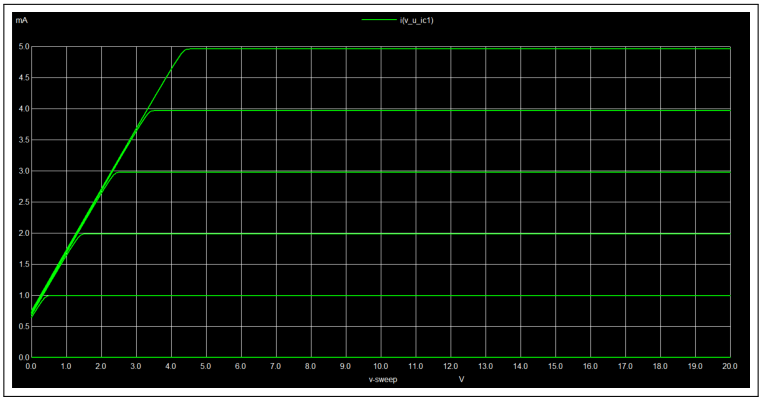



Figure 6.32: NgSpice simulation of CB output characteristics for 2N5401

#### 6.3.4.3 Frequency Response

The 2N5401 offers good high-frequency performance for its class, with low junction capacitances. Its transition frequency ($f_T$), though lower than RF-grade transistors, is adequate for audio and low-MHz analog signal processing:

$$f_T = \frac{1}{2\pi(r_b + r_e)(C_{eb} + C_{cb})}$$

Where $r_b$ and $r_e$ are internal resistances, and $C_{eb}$ and $C_{cb}$ are junction capacitances. The CE configuration is affected by the Miller effect, reducing bandwidth. The CB configuration, having negligible Miller multiplication, supports higher bandwidth operation. These traits make 2N5401 suitable for signal chain stages such as preamplifiers and filters.

This setup investigates the frequency response of the 2N5401 in CE mode. It helps determine bandwidth and gain variation over frequency.

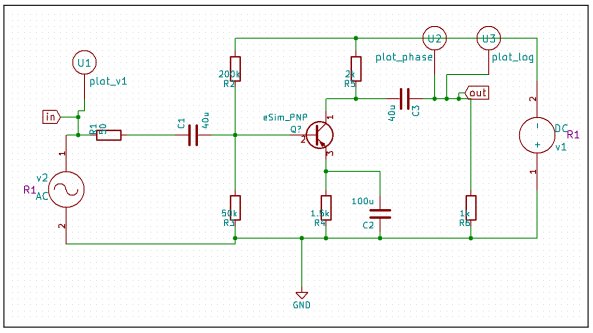



Figure 6.33: Frequency response circuit using 2N5401 in CE mode

The AC sweep result shows gain decreasing with frequency, indicating the -3dB cutoff and transition frequency.

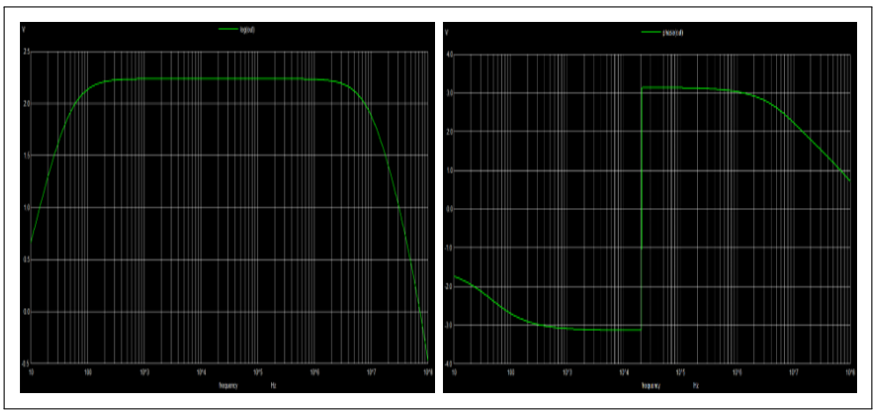


Figure 6.34: NgSpice simulation of frequency response for 2N5401

### 6.3.5 Application Circuit: Amplifier Design

The 2N5401 can be configured as a common-emitter inverting amplifier, where the input signal is applied to the base, and the output is taken from the collector through a load resistor. For PNP transistors, the collector is biased more negative than the emitter. The amplifier provides voltage gain with 180° phase shift, suitable for small-signal audio applications and low-frequency analog front-ends. Its low noise and good linearity make it effective in preamp and tone control stages.

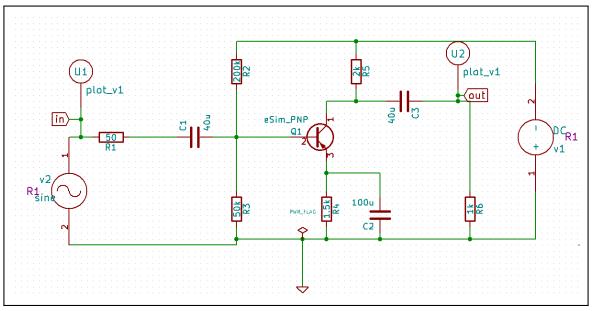



Figure 6.35: Inverting amplifier circuit using 2N5401

NgSpice output waveform demonstrates the 180° phase shift and voltage amplification.

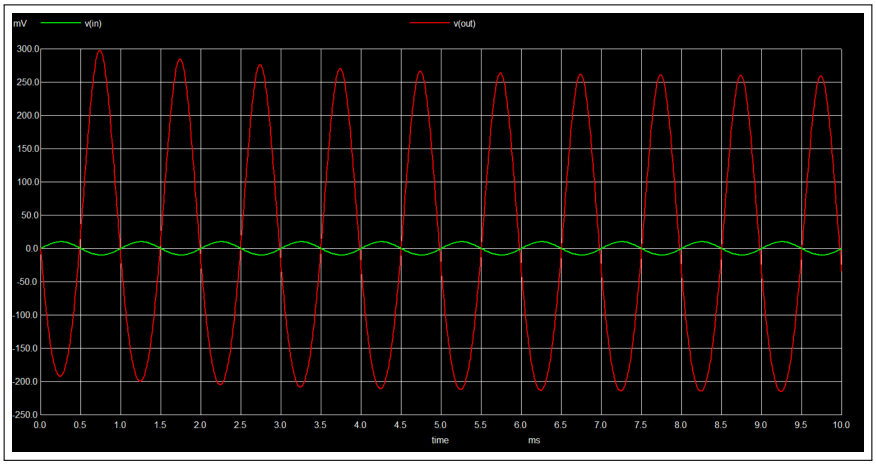



Figure 6.36: NgSpice simulation of amplifier response using 2N5401

## 6.4 PMEG2005EB

**Description:** Low VF MEGA Schottky barrier diode

### 6.4.1 General Description

The **PMEG2005EB** is a low forward voltage (Low VF) MEGA Schottky barrier diode developed by Philips Semiconductors. It is designed using planar technology and housed in an ultra-small SMD SOD523 (SC-79) plastic package, making it ideal for compact, high-density circuit designs.[21]

This diode supports a continuous forward current with extremely low forward voltage drop and minimal reverse leakage. The PMEG2005EB is particularly well-suited for ultra high-speed switching, low-current rectification, voltage clamping, and protection applications in low-power electronic systems such as handheld devices.

### 6.4.2 Typical Applications

- Reverse polarity protection
- Low voltage rectification
- Signal demodulation
- DC-to-DC converter circuits

### 6.4.3 SPICE Model Implementation

#### 6.4.3.1 SPICE Model Parameters

Below is the Spice model parameter list with their corresponding Description, Values and units.

Table 6.4: SPICE Model Parameters of PMEG2005EB Schottky Diode

| Parameter | Description | Value | Unit |
|---|---|---|---|
| IS | Saturation current | $9.985 \times 10^{-7}$ | A |
| RS | Series resistance | 0.2146 | Ω |
| N | Emission coefficient | 0.9283 | – |
| CJO | Zero-bias junction capacitance | 61.05 | pF |
| M | Grading coefficient | 0.4159 | – |
| VJ | Junction potential | 0.1 | V |
| BV | Breakdown voltage | 32 | V |
| IBV | Reverse breakdown current | $1.0 \times 10^{-3}$ | A |
| Bv | Secondary breakdown voltage | 100 | V |
| Ibv | Secondary breakdown current | $1.0 \times 10^{-4}$ | A |
| EG | Energy gap | 0.69 | eV |
| XTI | Saturation current temp. factor | 2 | – |
| MFG | Manufacturer | NXP | – |

#### 6.4.3.2 SPICE Model

The Spice model for the PMEG2005EB Low VF MEGA Schottky barrier diode:

**SPICE Model: PMEG2005EB Low VF MEGA Schottky barrier diode**

```
.MODEL PMEG2005EB D( Is=.9985u Rs=.2146 N=.9283
Cjo=61.05p M=.4159 Vj=.1 Bv=1.000E+02 Ibv=1.000E-04
Eg=.69 Xti=2 BV=32 IBV=.001 MFG=NXP )
```

### 6.4.4 Device Model Characterization

The PMEG2005EB is a low forward voltage Schottky barrier diode optimized for high-efficiency, fast-switching rectification. Its behavior is analyzed through forward and reverse bias characteristics using standard current-voltage relationships.

#### 6.4.4.1 Forward Bias Characteristics

In forward bias, the current through the diode follows the modified diode equation:

$$I = I_S \left( e^{\frac{qV}{nkT}} - 1 \right)$$

where $I_S$ is the reverse saturation current, $V$ is the forward voltage across the diode, $n$ is the ideality factor, $q$ is the electronic charge, $k$ is Boltzmann's constant, and $T$ is the absolute temperature.

Due to its metal–semiconductor junction, the PMEG2005EB exhibits a lower turn-on voltage compared to PN-junction diodes, with conduction beginning at approximately 0.2–0.3V. This low forward voltage improves conduction efficiency, especially in power-sensitive and low-voltage applications. The forward I–V curve (Fig. X) reflects this behavior, showing a steep increase in current after threshold.

The following circuit analyzes the forward bias behavior of the PMEG2005EB Schottky diode. It illustrates how the diode current increases with applied forward voltage ($V_F$), following the Schottky diode's exponential conduction behavior.

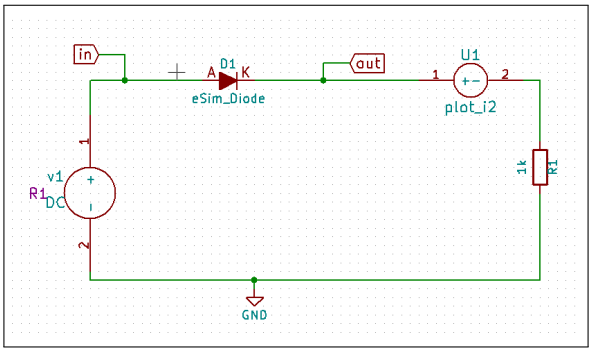



Figure 6.37: Forward bias circuit for PMEG2005EB Schottky diode

Below is the simulated I-V response showing the diode's low turn-on voltage and exponential current rise.

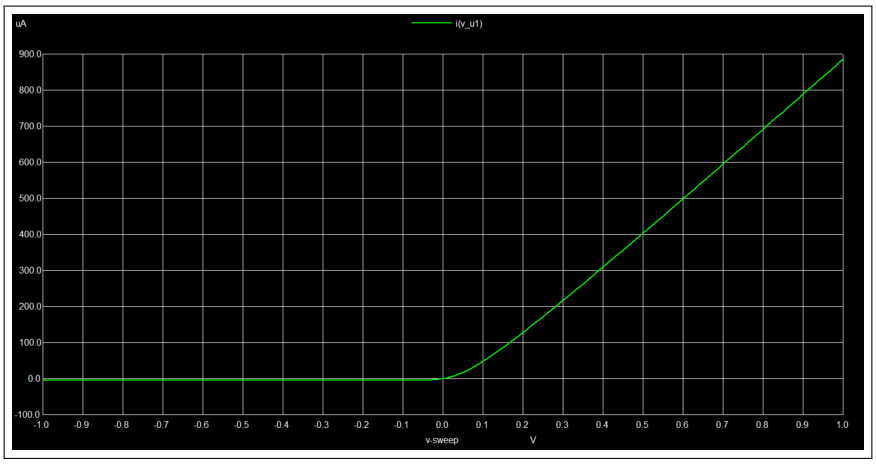



Figure 6.38: NgSpice simulation of forward I-V characteristics for PMEG2005EB

#### 6.4.4.2 Reverse Bias Characteristics

Under reverse bias, the Schottky diode maintains a small leakage current until the reverse voltage limit is reached. Unlike conventional PN-junction diodes, Schottky diodes do not undergo avalanche breakdown but may fail due to thermal effects. At moderate reverse voltages, the current approximates:

$$I \approx -I_S$$

The PMEG2005EB demonstrates reliable blocking up to 20V with minimal leakage, making it ideal for reverse polarity protection and high-speed switching. The reverse I–V plot confirms stable operation with no sharp breakdown knee.

The reverse bias setup examines the leakage current and breakdown behavior of the PMEG2005EB diode. The circuit helps study its blocking capability and reverse leakage under increasing negative voltage.

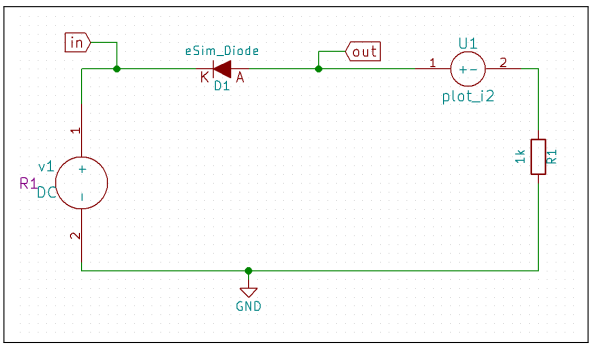



Figure 6.39: Reverse bias circuit for PMEG2005EB Schottky diode

Simulation shows minimal leakage current until breakdown, demonstrating Schottky behavior with low reverse leakage and no avalanche effect.

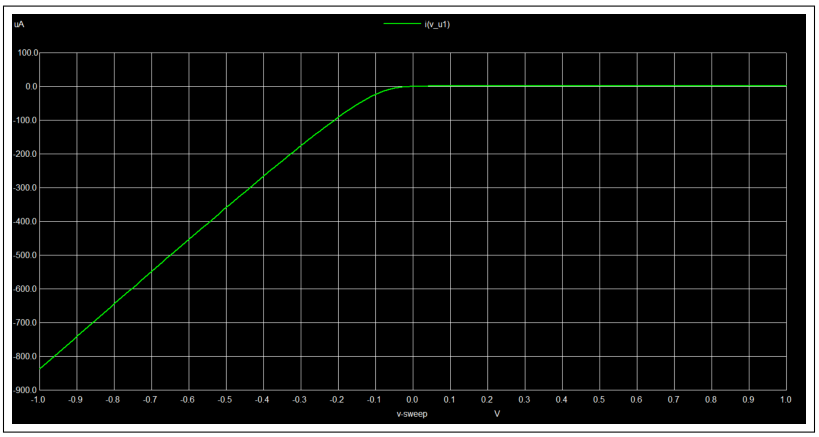



Figure 6.40: NgSpice simulation of reverse I-V characteristics for PMEG2005EB

### 6.4.5 Application Circuit: Half Wave Rectifier

The PMEG2005EB is implemented in a half-wave rectifier configuration, where it conducts during the positive half-cycles of an AC signal and blocks during the negative half. Its low forward voltage drop reduces conduction losses, improving efficiency in DC power supply stages, battery chargers, and portable electronics.

The PMEG2005EB is used in a basic half-wave rectifier configuration to demonstrate its rectification capability. The diode allows current only during the positive half-cycles of the AC input.

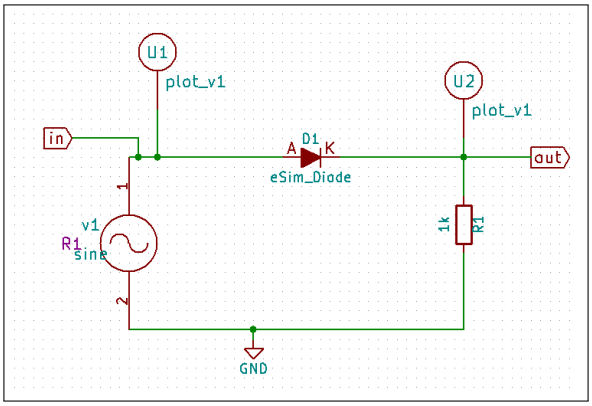



Figure 6.41: Half-wave rectifier using PMEG2005EB

The simulation below displays the rectified output waveform, showing conduction during positive cycles and blocking during negative half-cycles.

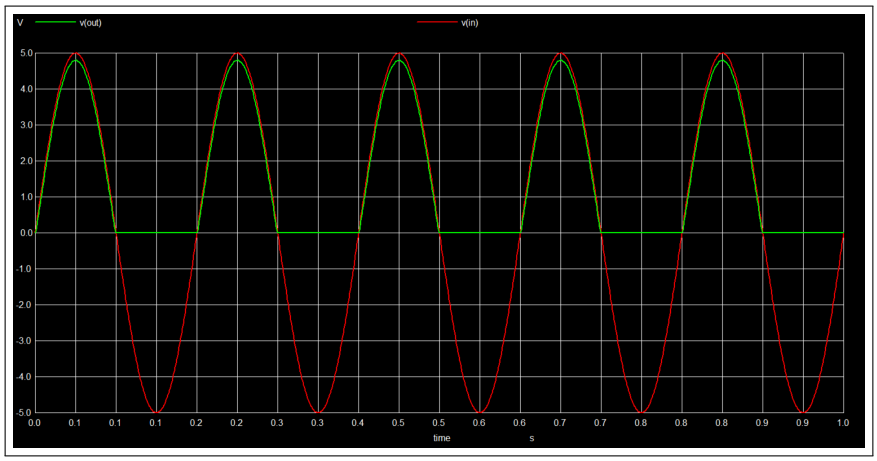



Figure 6.42: NgSpice simulation of half-wave rectifier using PMEG2005EB

## 6.5 LS5907

**Description:** Low Leakage Low Drift Monolithic N-Channel JFET

### 6.5.1 General Description

The LS5907 is a dual matched N-channel JFET (Junction Field-Effect Transistor) designed by Linear Integrated Systems for precision analog applications. It is part of a series (LS5906–LS5909, LS5905) optimized for low drift, ultra-low leakage, and high matching performance, making it suitable for sensitive signal processing tasks.[22]

### 6.5.2 Typical Applications

- Low-noise preamplifiers for audio and instrumentation
- Differential amplifier front-ends
- Active filters and analog signal conditioning
- Low-level signal detection in sensor interfaces

### 6.5.3 SPICE Model Implementation

#### 6.5.3.1 SPICE Model Parameters

Below is the Spice model parameter list with their corresponding Description, Values and units.

Table 6.5: SPICE Model Parameters of LS5907 N-Channel JFET

| Parameter | Description | Value | Unit |
|---|---|---|---|
| Beta | Transconductance parameter | $1.0 \times 10^{-4}$ | $A/V^2$ |
| Betatce | Temp. coefficient of beta | -0.5 | – |
| Rd | Drain resistance | 16 | Ω |
| Rs | Source resistance | 20 | Ω |
| Lambda | Channel-length modulation | $4.14 \times 10^{-3}$ | 1/V |
| Vto | Threshold voltage | -1.99 | V |
| Vtotc | Temp. coefficient of Vto | $-2.5 \times 10^{-3}$ | V/°C |
| Is | Saturation current | $1.14 \times 10^{-15}$ | A |
| Xti | Temperature exponent for Is | 0 | – |
| Cgd | Gate–drain capacitance | 1 | pF |
| M | Grading coefficient (junction) | 0.5 | – |
| Pb | Built-in potential | 0.8 | V |
| Fc | Forward-bias depletion coefficient | 0.5 | – |
| Cgs | Gate–source capacitance | 1 | pF |
| Kf | Flicker noise coefficient | 0 | – |
| Af | Flicker noise exponent | 1 | – |

#### 6.5.3.2 SPICE Model

The Spice model for the LS5907 Low Leakage Low Drift Monolithic N-Channel JFET is as follows:

**SPICE Model: LS5907 N-Channel JFET**

```
.MODEL LS5907 NJF( Beta=0.10m Betatce=-0.5 Rd=16 Rs=20
Lambda=4.14m Vto=-1.99 Vtotc=-2.5m Is=1.14f Xti=0 Cgd=1p
M=500m Pb=0.8 Fc=.5 Cgs=1p Kf=0 Af=1 )
```

### 6.5.4 Device Model Characterization

The LS5907 is a low-leakage, low-drift monolithic N-channel JFET designed for precision analog applications. It operates in depletion mode, offering high input impedance and low noise, making it ideal for signal amplification. Its behavior is analyzed through drain characteristics, transfer characteristics, and frequency response.

#### 6.5.4.1 Drain Characteristics

The drain characteristics describe the relationship between the drain current ($I_D$) and drain-source voltage ($V_{DS}$) for various gate-source voltages ($V_{GS}$). In the active region, the current saturates and follows:

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

for $V_{GS} < 0$ and $V_{DS} > V_{GS} - V_P$, where $I_{DSS}$ is the drain current with $V_{GS} = 0$, and $V_P$ is the pinch-off voltage. The LS5907 exhibits low $I_D$ leakage and stable saturation characteristics, making it suitable for precision low-current analog circuits.

The following circuit demonstrates the drain characteristics of the LS5907 N-channel JFET. It illustrates the variation of drain current ($I_D$) with drain-source voltage ($V_{DS}$) for different gate-source voltages ($V_{GS}$), revealing the ohmic, saturation, and cutoff regions.

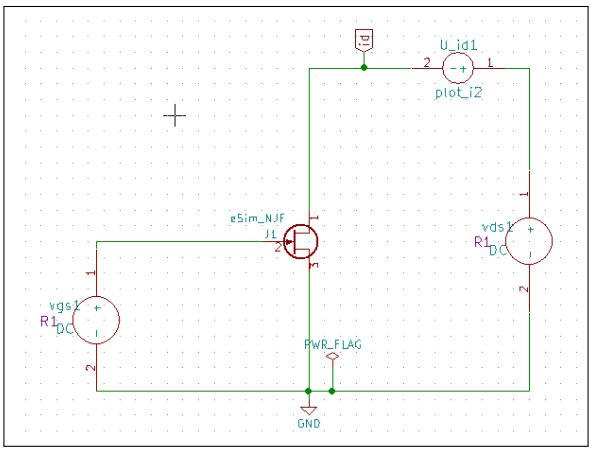



Figure 6.43: Drain characteristics test circuit for LS5907 JFET

Below is the NgSpice simulation results for the Test Circuit showcasing Drain Characteritics.

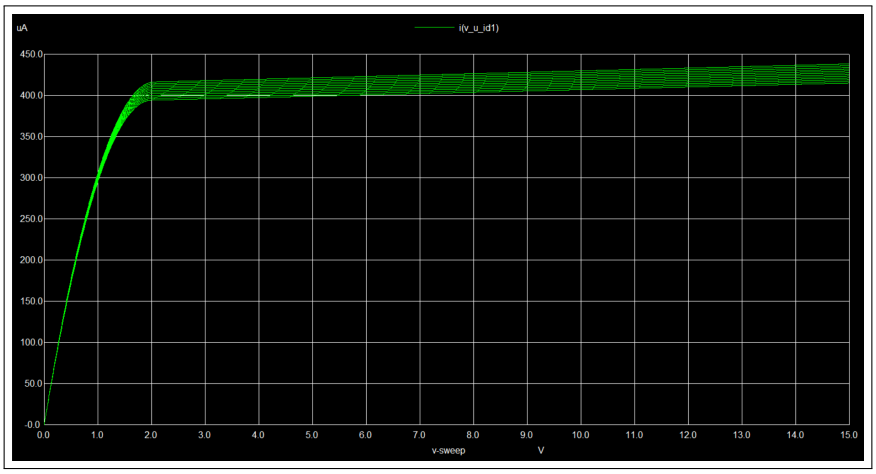



Figure 6.44: NgSpice simulation of $I_D$ vs. $V_{DS}$ for LS5907 at various $V_{GS}$

#### 6.5.4.2 Frequency Response

The LS5907 offers excellent high-frequency performance due to its small capacitances and low gate leakage. Its frequency response remains stable across temperature and bias variations, and it supports high-impedance, low-noise signal amplification over a wide bandwidth. This makes it suitable for low-level signal detection and wideband preamplifiers.

The frequency response setup for LS5907 evaluates its voltage gain over a range of input signal frequencies. As a low-noise JFET, LS5907 shows flat gain up to MHz range with slight roll-off due to internal capacitances.

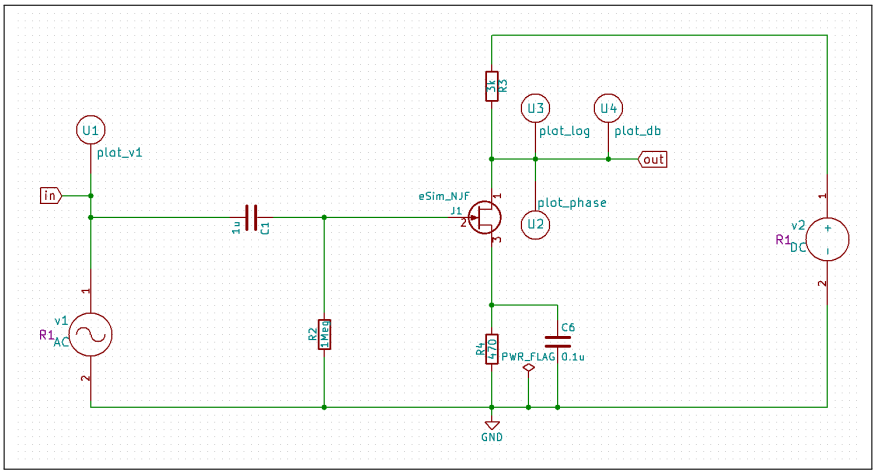



Figure 6.45: AC analysis setup for LS5907 JFET

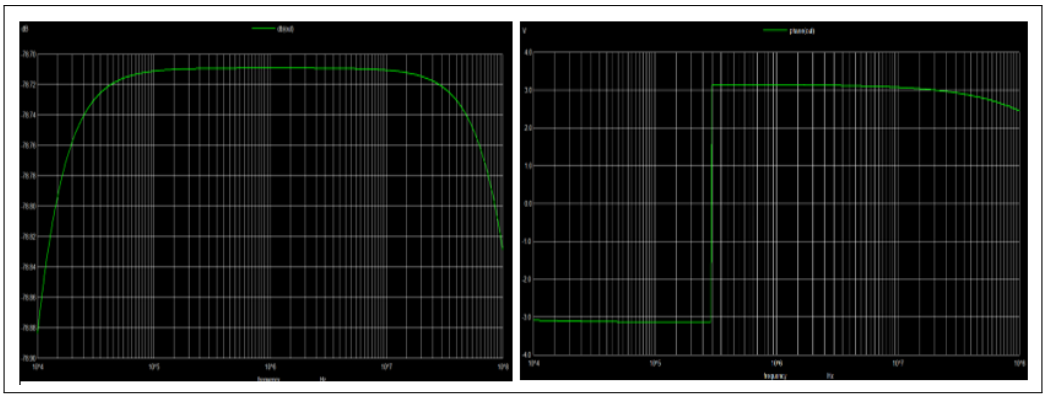


Figure 6.46: NgSpice simulation of frequency response for LS5907

### 6.5.5 Application Circuit: Amplifier Design

The LS5907 can be used in a common-source amplifier configuration where the input signal is applied to the gate, and the output is taken from the drain. This configuration provides voltage amplification with high input impedance and phase inversion.

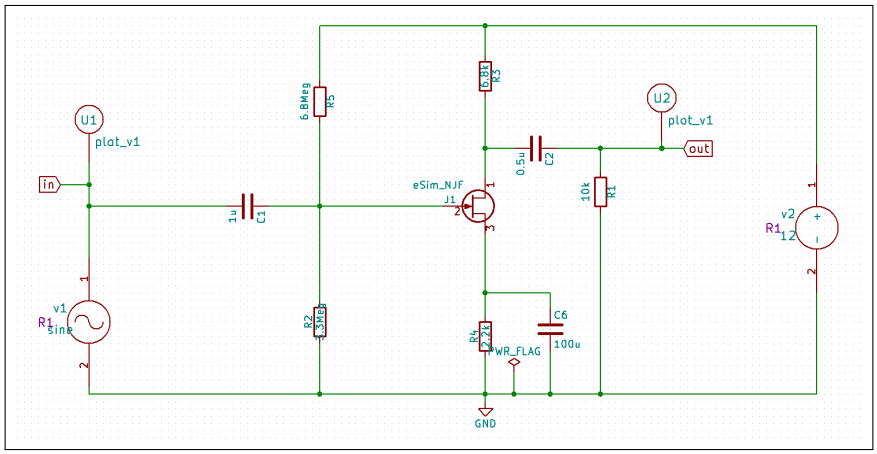



Figure 6.47: Common-source amplifier using LS5907

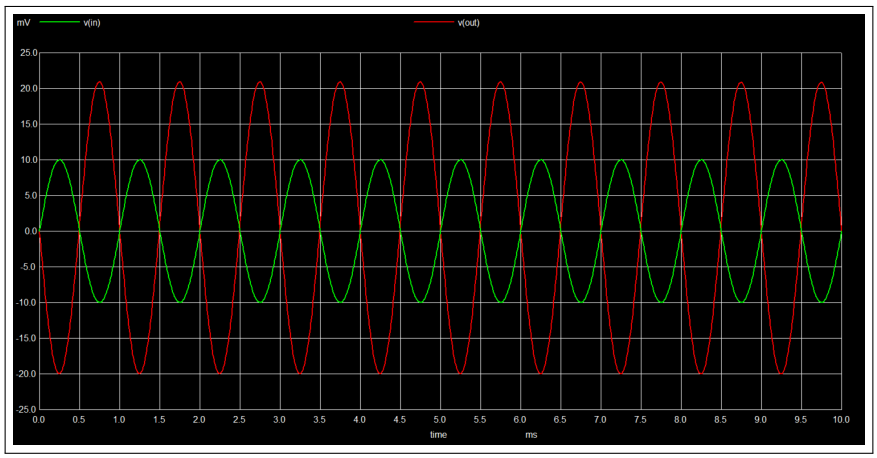



Figure 6.48: NgSpice simulation output for LS5907 amplifier

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