Summer Fellowship Report

On

Integrated Circuit Design using SubCircuit feature of eSim

Submitted by

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Under the guidance of

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Acknowledgment

We take this occasion to offer our heartfelt gratitude to the FOSSEE, IIT Bombay Team for offering us this wonderful opportunity to work on the design and integration of multiple sub-circuits in eSim. Working on eSim has provided us with invaluable insights into various open-source EDA tools for circuit simulation and their applications in the practical world.

We extend our sincere regards to Prof. Kannan M. Moudgalya for his valuable guidance and motivation throughout this fellowship program.

We would like to express our heartfelt appreciation to the entire FOSSEE team, including our mentors Mr. Sumanto Kar for constantly guiding and mentoring us throughout the duration of our internship

It is with their support that we have been able to fulfill our project demands successfully. Whenever faced with an issue, our mentors were always accessible to help us assess and debug them. Our learnings from them have been invaluable and shall be of paramount importance to us in the future

Overall, it was a delightful experience interning at FOSSEE and contributing to its growth and I take away some great insights and knowledge from it. As enthusiastic beginners in the semiconductor industry, this internship is a milestone for us in our pursuit of a successful career.

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Chapter 1

Introduction

FOSSEE, which stands for Free/Libre and Open Source Software for Education, is an initiative based at IIT Bombay that plays a pivotal role in promoting the use of open-source software in the fields of education and research. This organization was founded with the vision of minimizing reliance on proprietary software by encouraging the adoption of open-source alternatives. FOSSEE supports a broad spectrum of academic and professional domains through its diverse set of tools and resources.

It offers extensive documentation, interactive tutorials, training workshops, and practical sessions designed to equip students, educators, and professionals with the skills to effectively utilize open-source software in their academic work and projects. The organizations strong dedication to nurturing a collaborative and inclusive ecosystem has greatly advanced the democratization of technology, paving the way for increased innovation, accessibility, and learning opportunities across disciplines.

1.1 eSim

eSim, developed by the FOSSEE project at IIT Bombay, is a powerful and flexible open-source software tool designed for electronic circuit design and simulation. It seamlessly integrates multiple open-source software packages into a unified platform, simplifying the process of designing, simulating, and analyzing electronic circuits. This makes it an ideal choice for students, educators, and professionals seeking a cost-effective and easily accessible alternative to proprietary circuit design tools.

With capabilities for schematic creation, circuit simulation, and PCB layout design, eSim provides a comprehensive suite of features, along with a rich library of electronic components. One of its standout features is the Subcircuit functionality, which allows users to build complex systems by combining and managing simpler subcircuits. Through eSim, FOSSEE actively promotes the adoption of open-source solutions within engineering education and the professional sector, fostering a spirit of innovation, collaboration, and self-reliance.

1.2 Ngspice

NgSpice is a robust open-source SPICE simulator used for the analysis of electrical and electronic circuits. It supports the simulation of a wide range of circuit elements, including JFETs, bipolar junction transistors (BJTs), MOSFETs, passive components such as resistors, inductors, and capacitors (R, L, C), as well as diodes and various other devices, all connected through a structured netlist.
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In addition to analog components, NgSpice is capable of simulating digital circuits, from basic logic gates to highly complex systems, and even mixed-signal circuits that incorporate both analog and digital elements. It offers an extensive library of device models to represent a variety of active, passive, analog, and digital components accurately. Users define their circuits in the form of netlists, and NgSpice generates outputs such as graphical plots of voltages, currents, and other electrical parameters, or exports the results into data files for further analysis.

1.3 MakerChip

Makerchip is a versatile platform that provides user-friendly and accessible tools for digital circuit design. It offers both web-based and desktop environments that enable users to write, compile, simulate, and debug Verilog-based designs with ease. Supporting Verilog, SystemVerilog, and Transaction-Level Verilog, Makerchip combines open-source and proprietary tools to deliver a comprehensive and powerful design experience.

To enhance its usability, eSim is integrated with Makerchip through a Python-based interface known as Makerchip-App, which launches the Makerchip IDE directly from within eSim. This integration allows for a smooth workflow between analog and digital design environments. Makerchip is designed to cater to users of all experience levels, offering an intuitive interface, streamlined workflows, and a range of supportive features that simplify digital circuit development and boost user engagement.

However, a major limitation in the landscape of open-source electronic design automation (EDA) tools is the lack of an all-in-one solution. While certain tools like KiCad focus on PCB layout and others like gEDA specialize in circuit simulation, no single open-source platform traditionally provides a unified environment for circuit design, simulation, and layout. eSim fills this gap by integrating all these essential capabilities into a single cohesive tool, offering a complete solution for electronics design and simulation.

Chapter 2

Features of eSim

The development of eSim is driven by the goal of providing an open-source Electronic Design Automation (EDA) solution tailored for electronics and electrical engineers. It serves as a comprehensive tool capable of schematic creation, PCB layout design, and circuit simulationcovering analog, digital, and mixed-signal circuits. Additionally, it offers the flexibility to create custom models and components, making it a versatile platform for academic, professional, and research applications.eSim offers the following key features:

1. Schematic Creation: eSim includes a user-friendly graphical interface for designing circuit schematics. It allows users of all skill levels to drag and drop components from an extensive library, making circuit creation intuitive and efficient. The editing tools enable easy modifications, such as moving, rotating, and labeling components, ensuring clarity and accuracy in design.

2. Circuit Simulation: Built on the SPICE (Simulation Program with Integrated Circuit Emphasis) framework, eSim supports both analog and digital simulations. It facilitates various types of analysesincluding transient, AC, and DCto provide a deep understanding of circuit performance over time and frequency. The integrated waveform viewer enhances the debugging process by visually representing simulation outputs like voltage and current waveforms.

3. PCB Design: The PCB layout editor in eSim enables precise placement of components and trace routing. It features Design Rule Check (DRC) tools to verify that the layout complies with electrical and manufacturing standards. Users can also generate standard Gerber files directly from their designs, which are essential for PCB fabrication.

4. Subcircuit Feature: This powerful feature allows users to build complex circuits by incorporating smaller, modular subcircuits. It supports a hierarchical design methodology and promotes reuse of circuit blocks, thereby saving time and reducing repetitive work across projects.

5. Open Source Integration: eSim combines multiple open-source tools such as KiCad (for PCB layout), NgSpice (for circuit simulation), and GHDL (for digital simulation) into a unified platform. Its open-source nature ensures that it is freely available, eliminating the need for costly licenses while still offering professional-grade capabilities.

By integrating all essential elements of the circuit design process, eSim addresses the gap in open-source EDA tools and offers an all-in-one, accessible solution for engineers, students, and educators alike.

Chapter 3

Problem Statement

To design and develop various Analog and Digital Integrated Circuit Models in the form of sub-circuits using device model files already present in the eSim library. These IC models should be useful in the future for circuit designing purposes by developers and users, once they get successfully integrated into the eSim subcircuit Library.

3.1 Approach

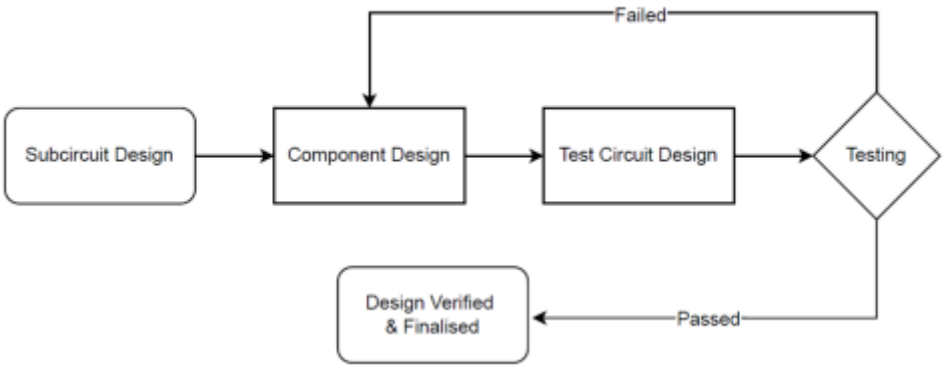

Figure 3.1: Flowchart of IC Design Approach Followed

Our approach to implementing the problem statement began with examining datasheets from prominent Integrated Circuit (IC) manufacturers such as Texas Instruments, Analog Devices, and NXP Semiconductors. we selected ICs that offer a diverse range of functionalities, including precision amplifiers, comparators, encoders, and audio amplifiers. After building the subcircuits, we tested them to verify basic circuit configurations using NgSpice simulations. The step-by-step roadmap of this process is outlined below :

1. Analyzing Datasheets: The first and most crucial step involves thoroughly reviewing a variety of analog and digital IC datasheets. The objective is to identify circuits that can be implemented in eSim but are not currently available in its component library. This includes examining detailed schematics of the ICs, determining the appropriate component values, and analyzing truth tables. Once a comprehensive understanding is gained and a viable IC is identified, it is finalized for implementation.

2. Subcircuit Creation: After selecting the IC, the next step is to model it as a subcircuit within eSim using only the model files provided in the eSim device model library. The design process strictly follows the specifications outlined in the official datasheet of the IC. This stage also involves creating the symbol and pin diagram of the IC, ensuring that the layout accurately reflects the package type and pin configuration described in the datasheet.

3. Test Circuit Design: With the IC component now modeled, test circuits are developed in accordance with the test configurations provided in the datasheet. This phase involves constructing appropriate test cases and connecting the IC in various configurations to validate its functionality under different input conditions.

4. Schematic Testing: Once the test circuits are completed, simulation is performed to analyze the circuits behavior. The outputs are obtained in the form of waveform plots using eSims simulation capabilities, which include KiCad to NgSpice conversion. If the results do not align with the expected behavior, it indicates a failed test case. In such situations, the schematic design of either the IC or the test circuit is re-examined for potential errors. Necessary corrections are made, and the testing process is repeated.

When the simulation results match the expected outputs as described in the datasheet, the IC is deemed successfully implemented. The test case is considered verified, and the design process is concluded.

Chapter 4

SN74278

The SN74278 IC consist of four data latches, full priority output gating, and a cascading gate. The highest-order data applied at a D latch input is transferred to the appropriate Y output while the strobe input is high, and when the strobe goes low all data is latched. The cascading input PO is fully overriding and on the highest-order package this input must be held at a low logic level. The P1 output is intended for connection to the PO input of the next lower-order package and will provide a "busy" (high-level) signal to inhibit all subsequent lower-order packages.

After the overriding PO input, the order of priority is D1, D2, D3, and D4, respectively,

4.1 Pin Diagram

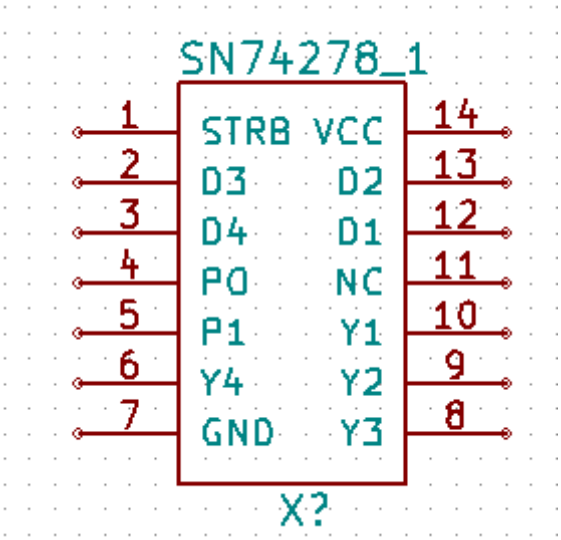

Figure 4.1: Pin Configuration of SN74278

4.2 Sub Circuit Schematic

The Subcircuit layout presented here represents the detailed design of IC SN74278. The design consists of all the essential components required for the stable operation and the optimal performance of the IC in various different applications.

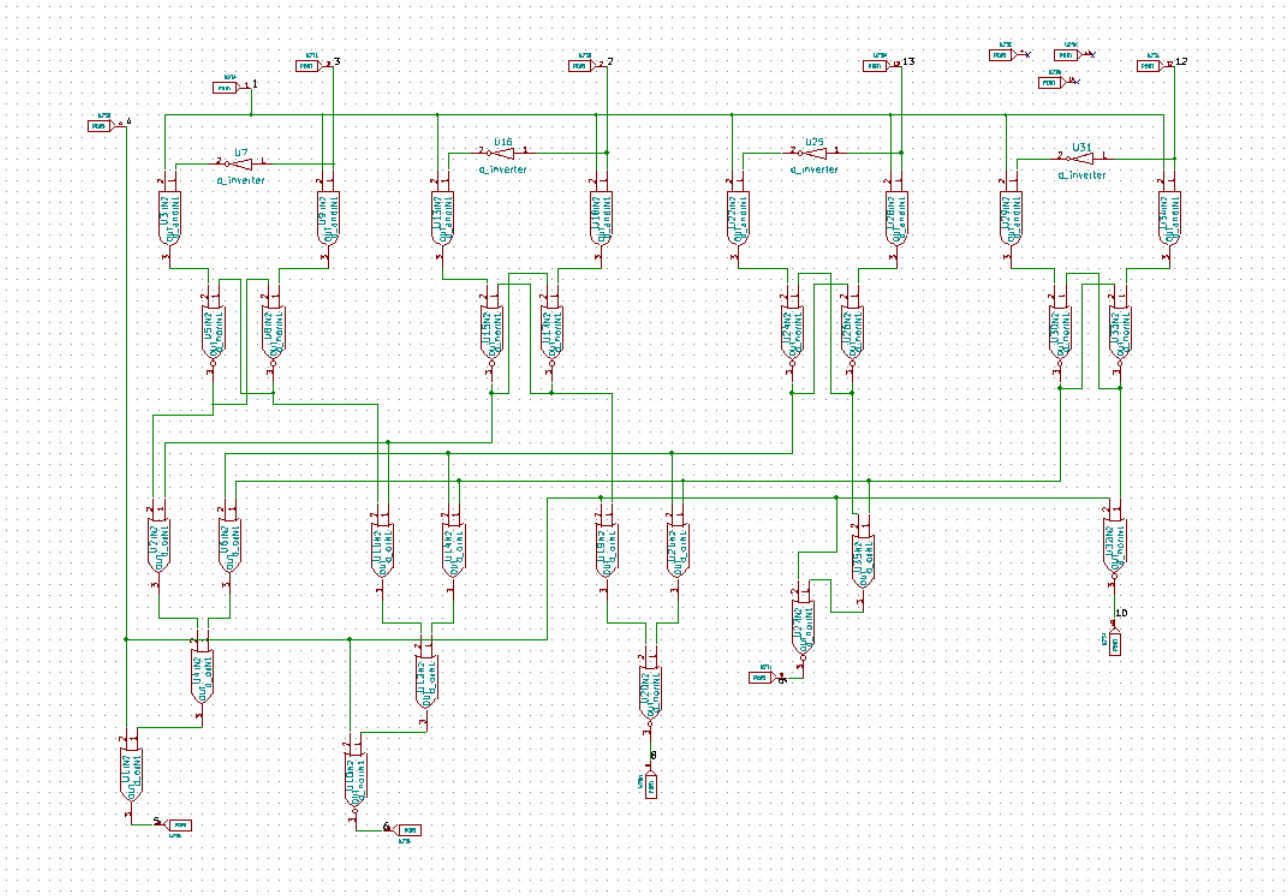

Figure 4.2: SubCircuit Schematic of SN74278 IC

4.3 Test Circuit

The test circuit for the SN74278 is designed to evaluate the performance and functionality of the IC using the subcircuit approach. By utilizing the Subcircuit feature, this test circuit can be easily integrated into simulation and analysis environments to verify the ICs behavior under various conditions before final implementation.

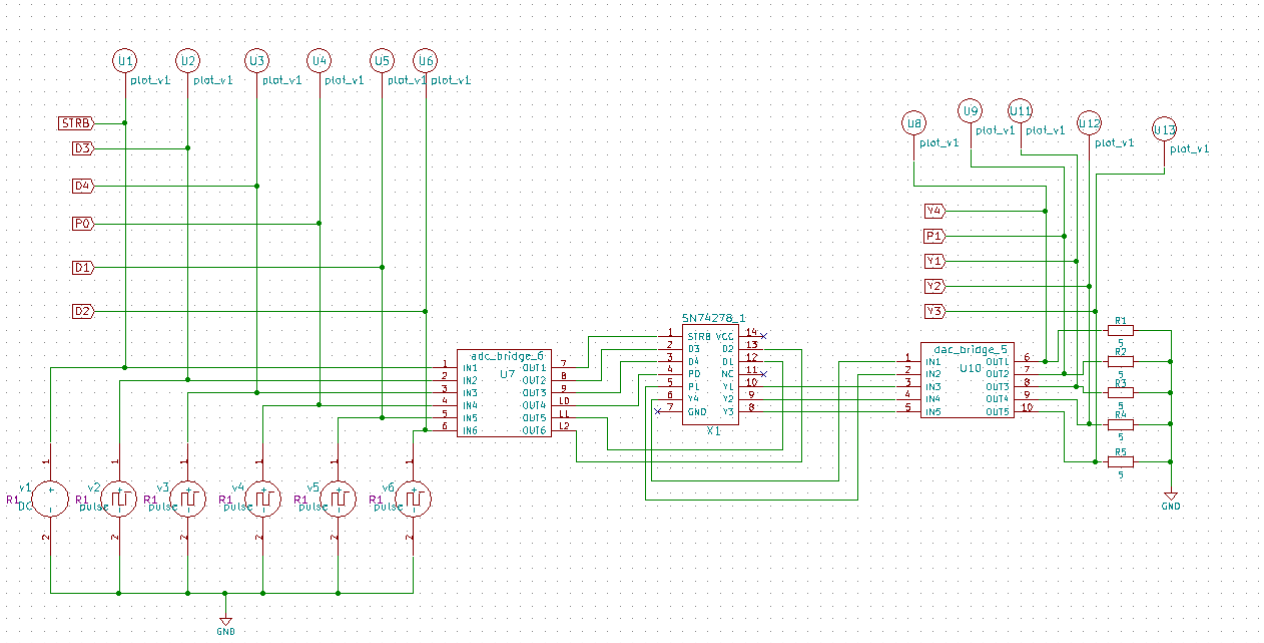

Figure 4.3: Test Circuit Schematic of SN74278 IC

4.4 Input Waveforms

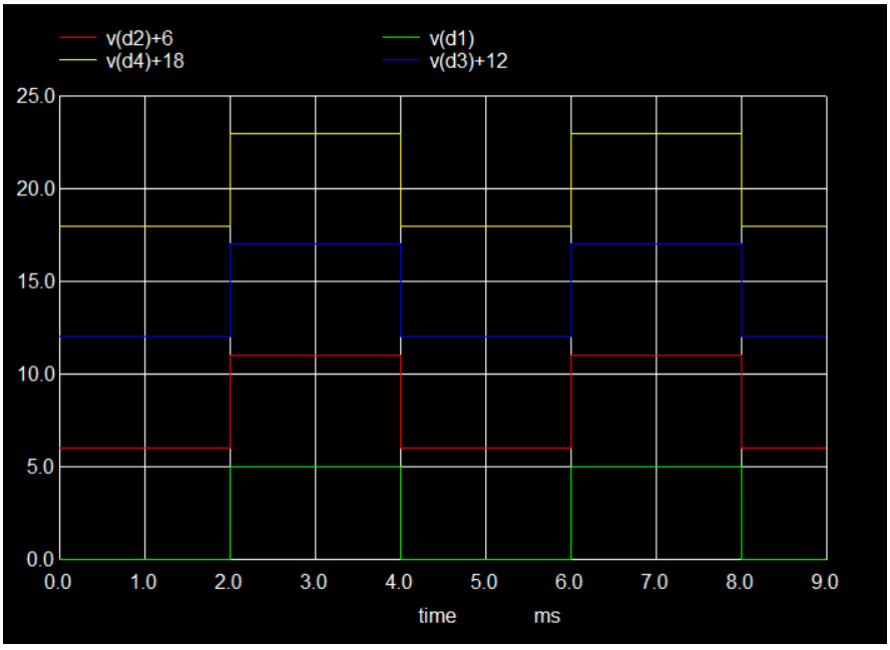

Figure 4.4: Data signals of SN74278 IC

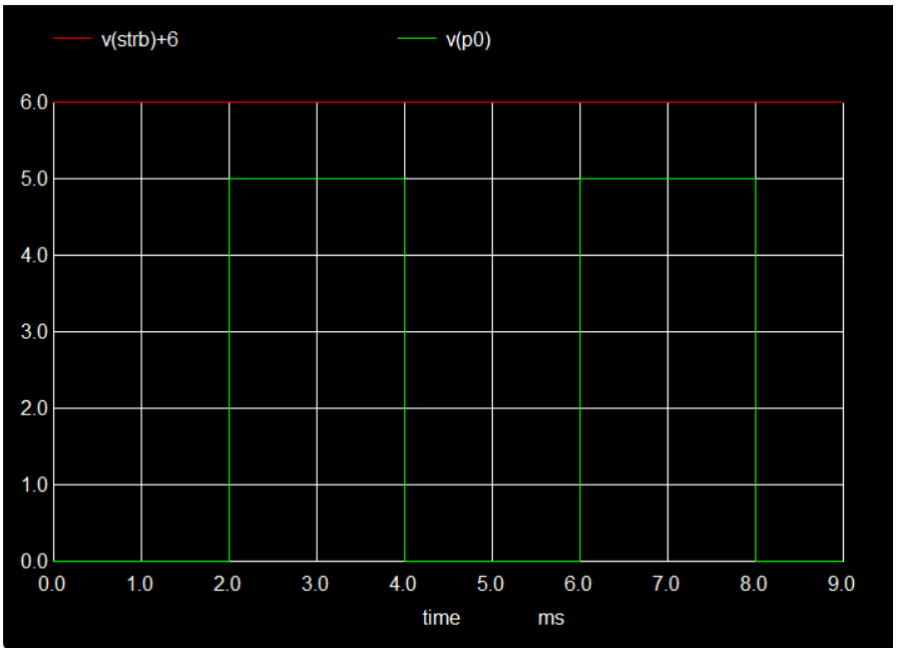

Figure 4.5: Input and strobe signal of SN74278 IC

4.5 Output Waveform

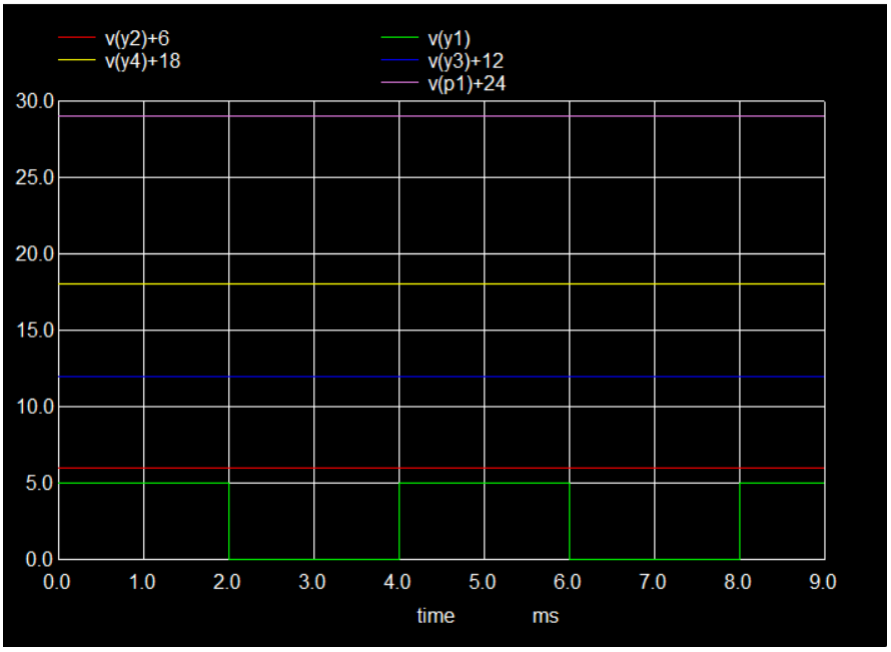

Figure 4.6: Output signals of SN74278 IC

Chapter 5

SN74199

These registers feature parallel inputs, parallel outputs, J-K serial inputs, shift/load control input, a direct overriding clear line, and gated clock inputs. The register has three modes of operation: Inhibit Clock, Shift, Parallel loading

Parallel loading is accomplished by applying the eight bits of data and taking the shift/load control input low when the clock input is not inhibited. The data is loaded into the associated flip-flop and appears at the outputs after the positive transition of the clock input. During loading, serial data flow is inhibited.

Shifting is accomplished synchronously when shift/load is high and the clock input is not inhibited. Serial data for this mode is entered at the J and K inputs

5.1 Pin Diagram

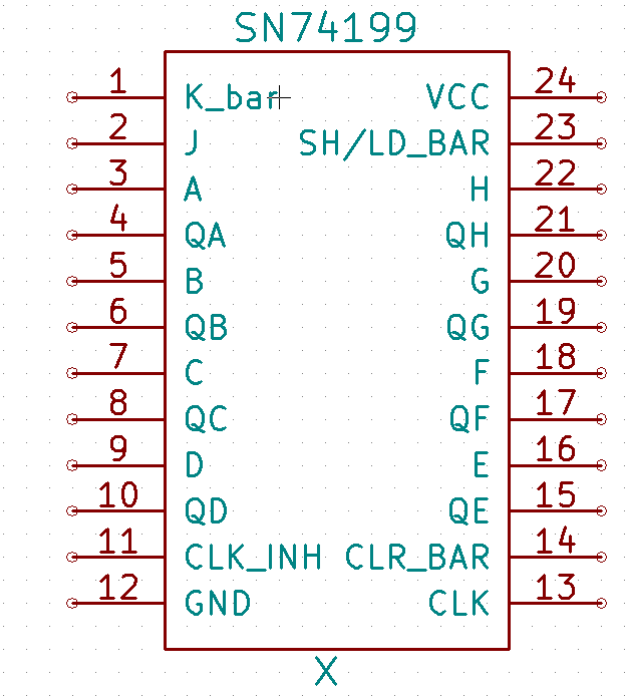

Figure 5.1: Pin Configuration of SN74199

5.2 Sub Circuit Schematic

The Subcircuit layout presented here represents the detailed design of IC SN74199. The design consists of all the essential components required for the stable operation and the optimal performance of the IC in various different applications.

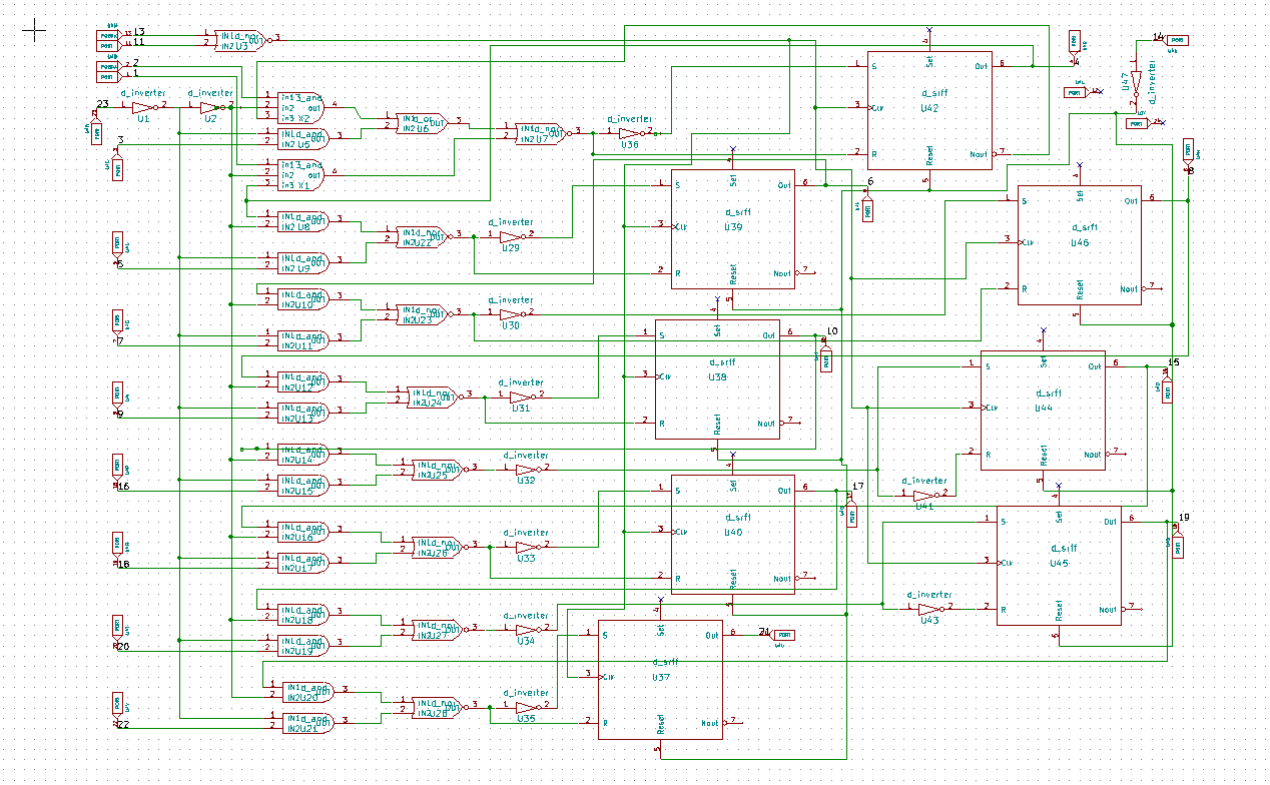

Figure 5.2: SubCircuit Schematic of SN74199 IC

5.3 Test Circuit

The test circuit for the SN74199 is designed to evaluate the performance and functionality of the IC using the subcircuit approach. By utilizing the Subcircuit feature, this test circuit can be easily integrated into simulation and analysis environments to verify the ICs behavior under various conditions before final implementation.

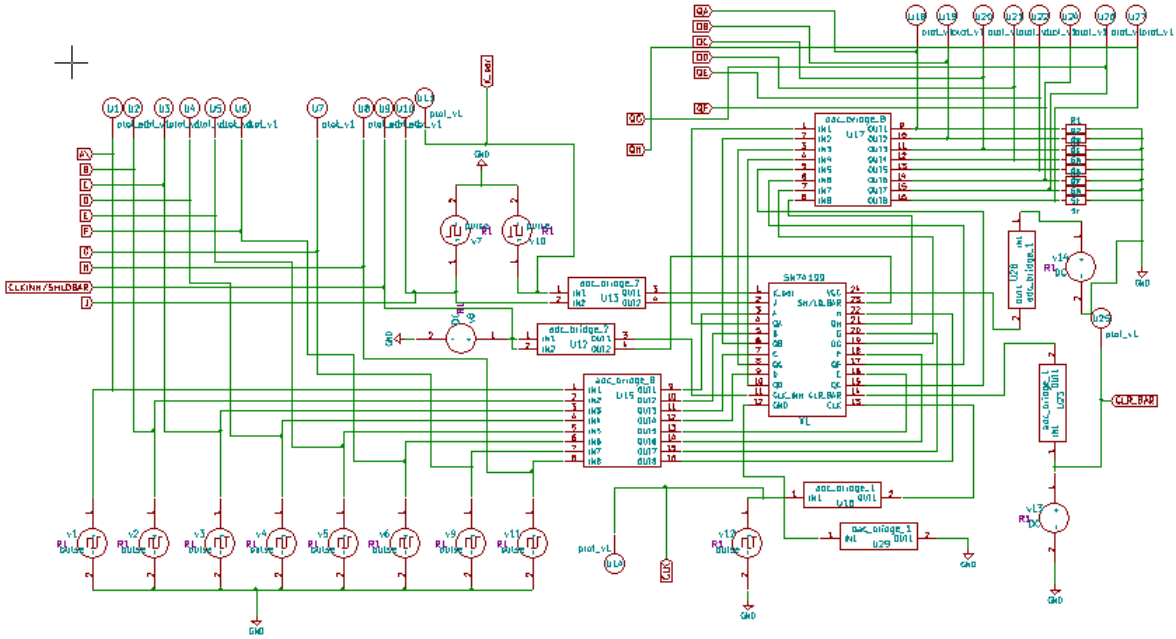

Figure 5.3: Test Circuit Schematic of SN74199 IC

5.4 Input Waveforms

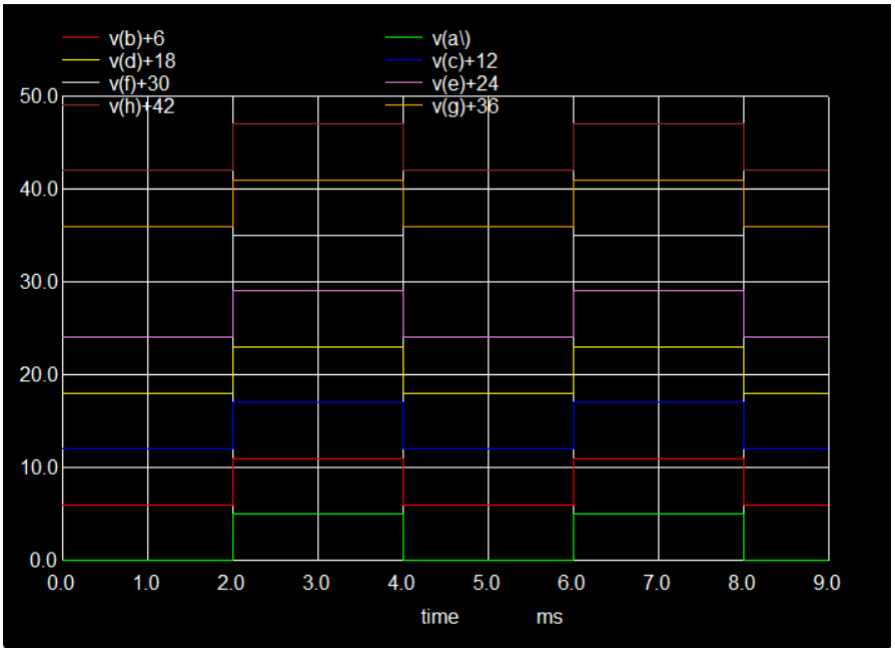

Figure 5.4: Input Data signals of SN74199 IC

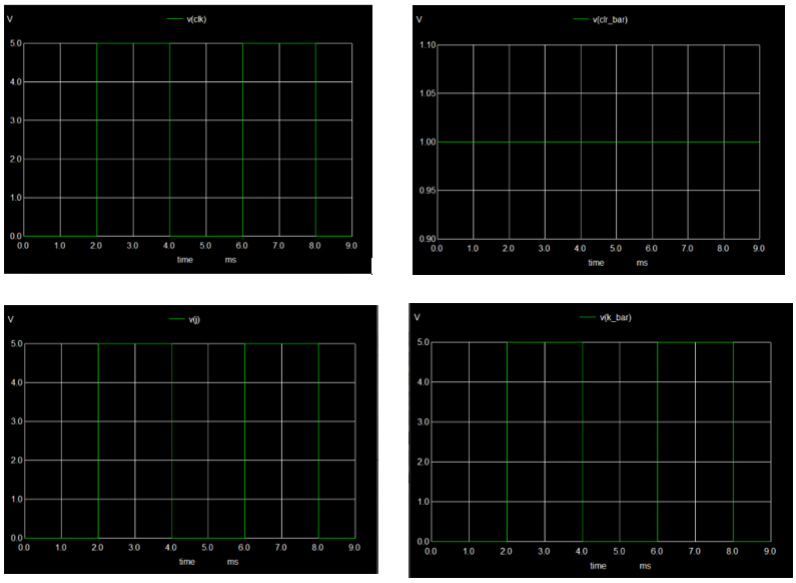

Figure 5.5: CLK,CLR,J-K Signals of SN74199 IC

5.5 Output Waveform

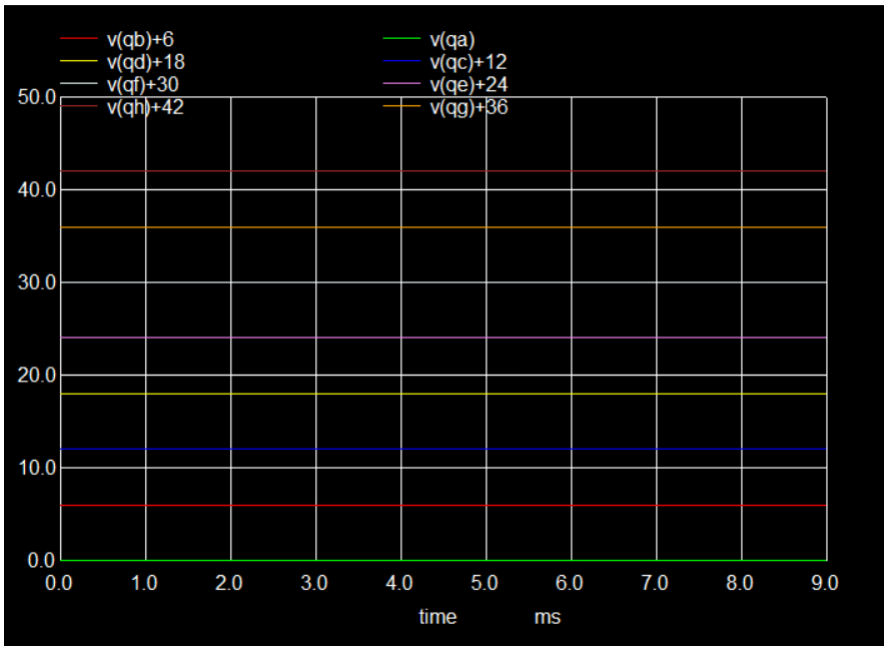

Figure 5.6: Output signals of SN74199 IC

Chapter 6

SN54L98

These monolithic data selectors/storage registers are composed of four S-R master-slave flip-flops, four AND-OR-INVERT gates, one buffer, and six inverter/drivers.

When the word select input is low, word 1 (A1, B1, C1, D1) is applied to the flip-flops. A high input to word select will cause the selection of word 2 (A2, B2, C2, D2). The selected word is shifted to the output terminals on the negative-going edge of the clock pulse.

6.1 Pin Diagram

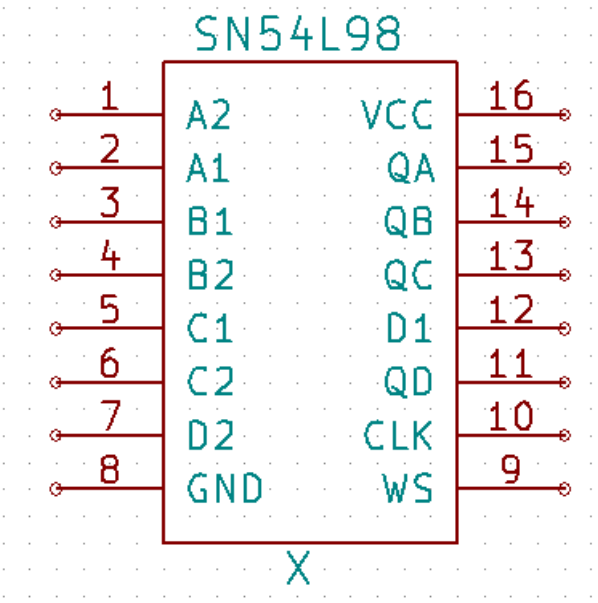

Figure 6.1: Pin Configuration of SN54L98

6.2 Sub Circuit Schematic

The Subcircuit layout presented here represents the detailed design of IC SN54L98. The design consists of all the essential components required for the stable operation and the optimal performance of the IC in various different applications.

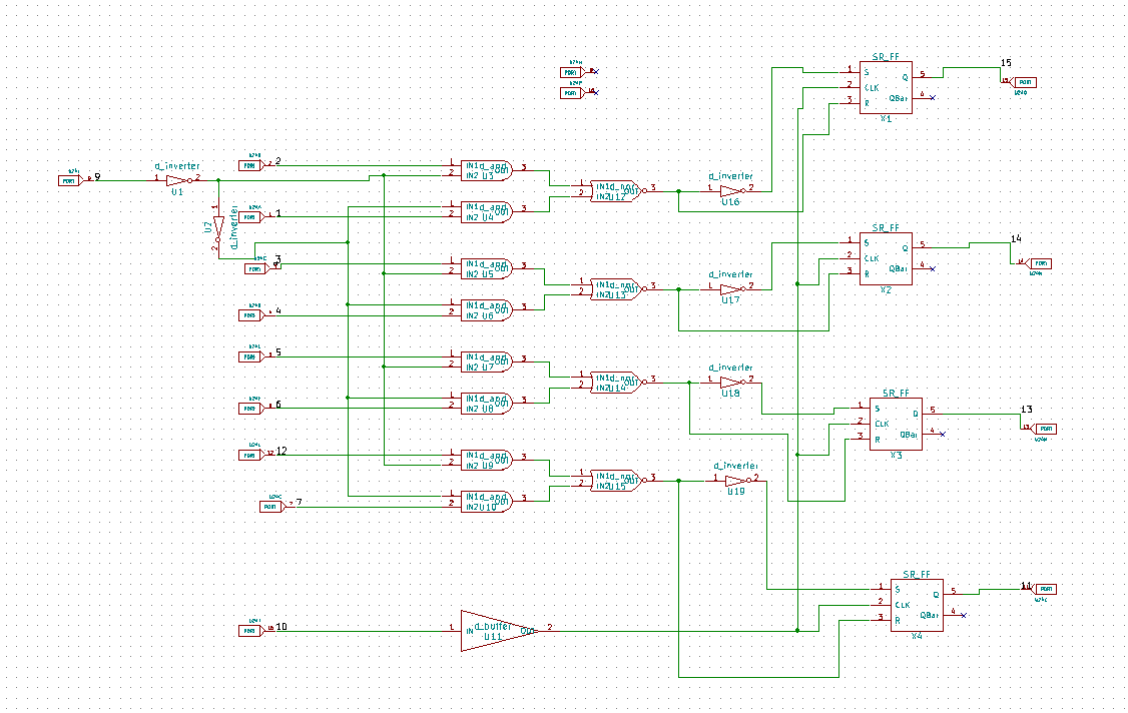

Figure 6.2: SubCircuit Schematic of SN54L98 IC

6.3 Test Circuit

The test circuit for the SN54L98 is designed to evaluate the performance and functionality of the IC using the subcircuit approach. By utilizing the Subcircuit feature, this test circuit can be easily integrated into simulation and analysis environments to verify the ICs behavior under various conditions before final implementation.

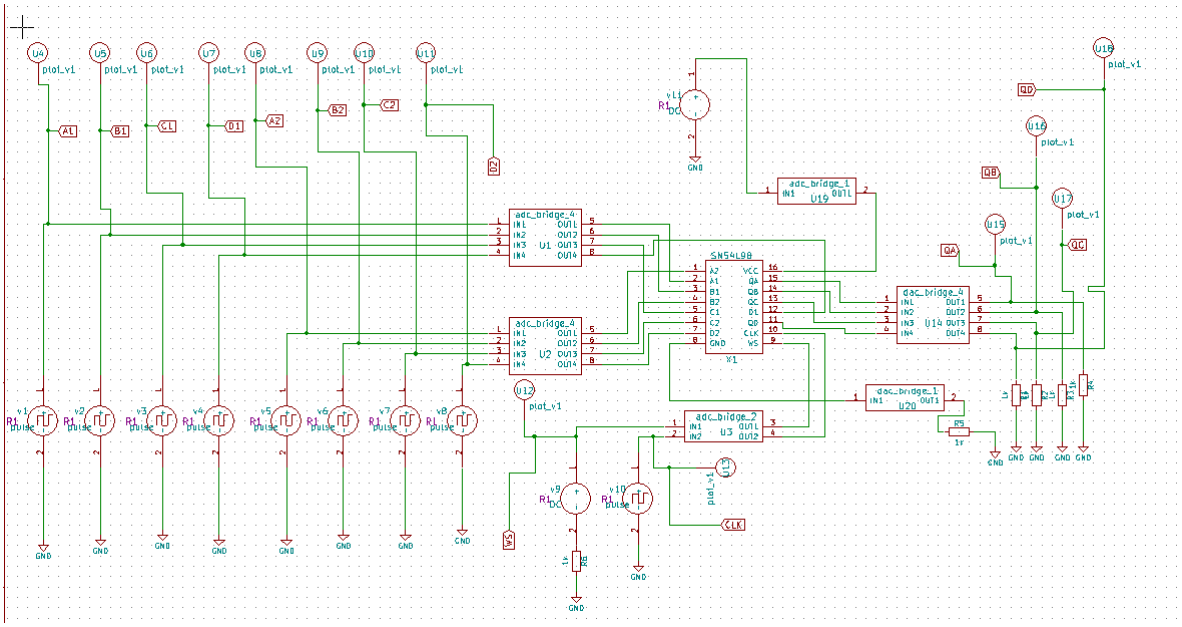

Figure 6.3: Test Circuit Schematic of SN54L98 IC

6.4 Input Waveforms

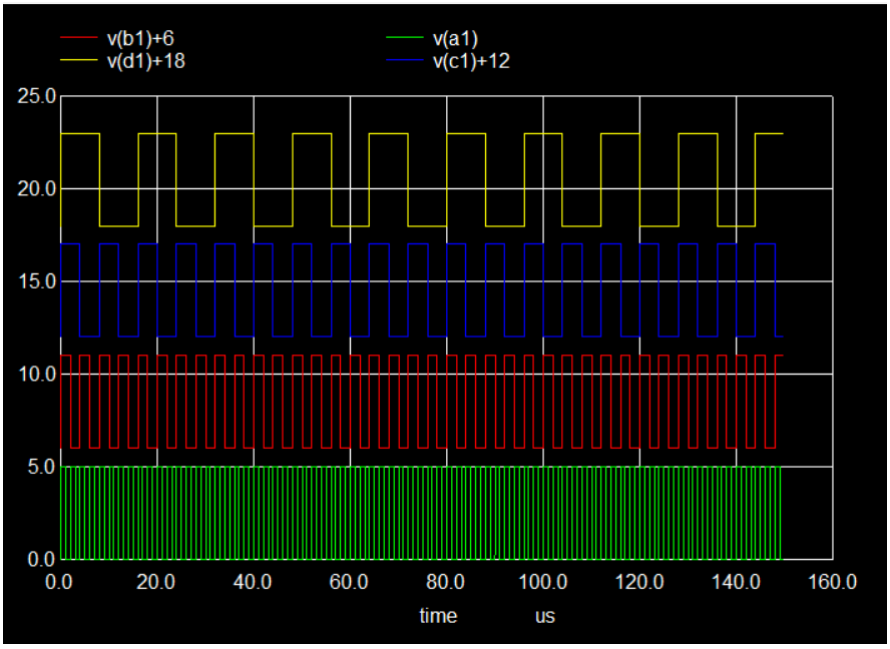

Figure 6.4: 1st Input Word signal of SN54L98 IC

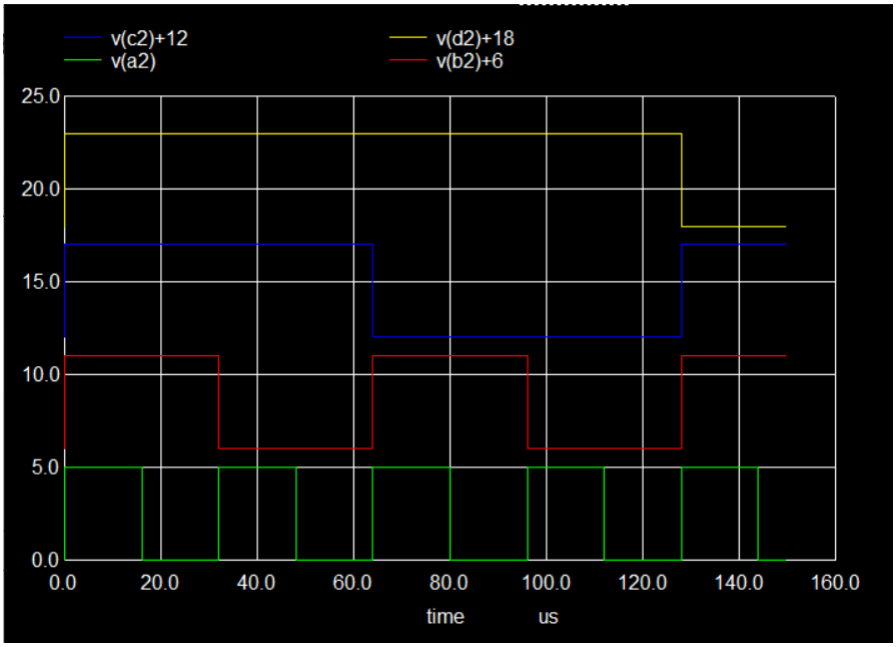

Figure 6.5: 2nd Input Word signal of SN54L98 IC

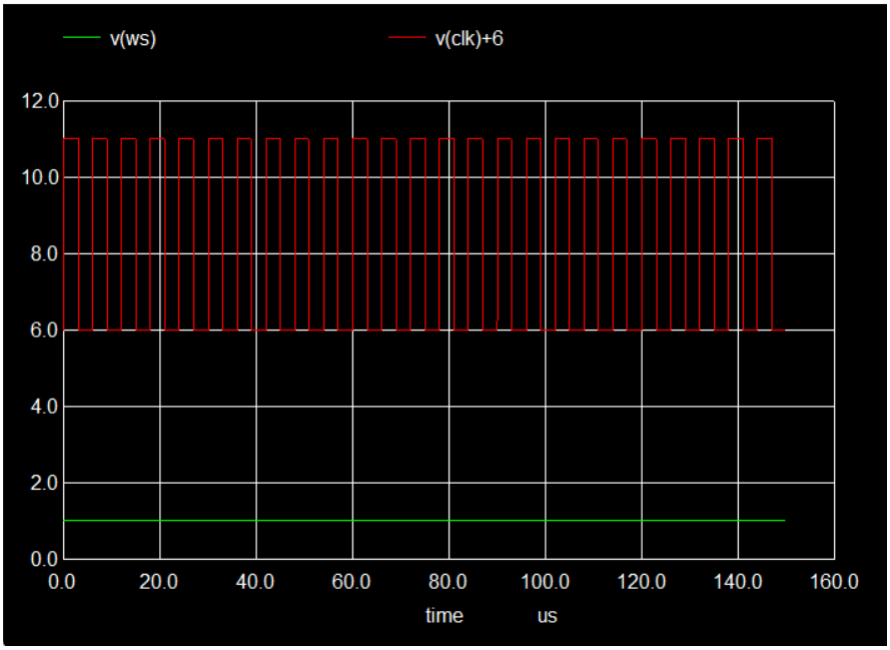

Figure 6.6: Input signals of SN54L98 IC

6.5 Output Waveform

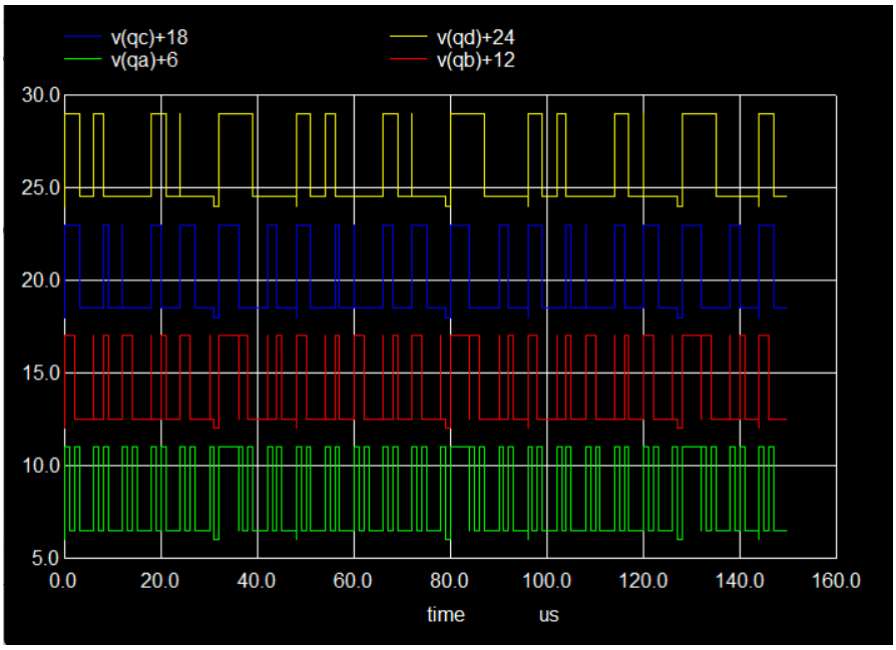

Figure 6.7: Output signals of SN54L98 IC

Chapter 7

SN74177

These high-speed monolithic counters consist of four d-c coupled master-slave flip-flops which are internally interconnected to provide either a divide-by-two and a divide-by-eight counter (SN54177, SN74177). These counters are fully programmable; that is, the outputs may be preset to any state by placing a low on the count/load input and entering the desired data at the data inputs. The outputs will change to agree with the data inputs independent of the state of the clocks.

These counters may also be used as 4-bit latches by using the count/load input as the strobe and entering data at the data inputs. The outputs will directly follow the data inputs when the count/loadis low, but will remain unchanged when the count/load is high and the clock inputs are inactive.

7.1 Pin Diagram

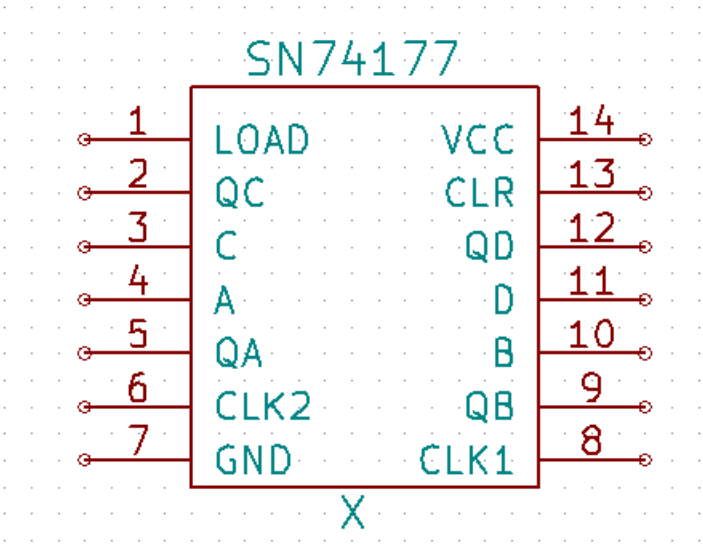

Figure 7.1: Pin Configuration of SN74177

7.2 Sub Circuit Schematic

The Subcircuit layout presented here represents the detailed design of IC SN74177. The design consists of all the essential components required for the stable operation and the optimal performance of the IC in various different applications.

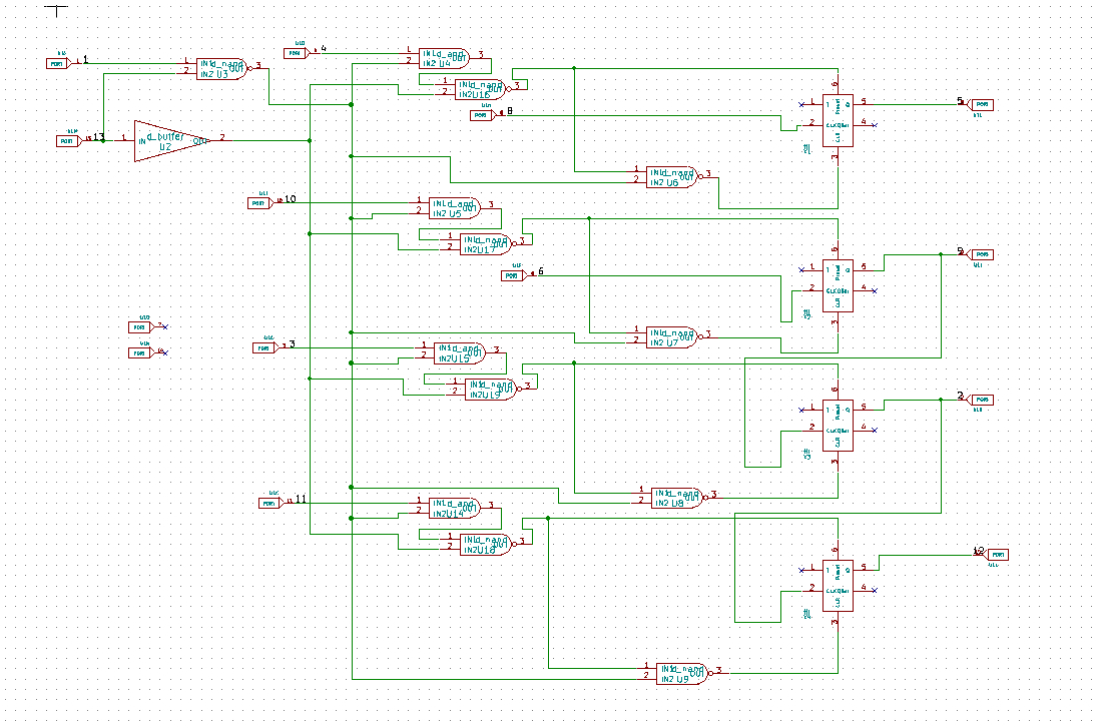

Figure 7.2: SubCircuit Schematic of SN74177 IC

7.3 Test Circuit

The test circuit for the SN74177 is designed to evaluate the performance and functionality of the IC using the subcircuit approach. By utilizing the Subcircuit feature, this test circuit can be easily integrated into simulation and analysis environments to verify the ICs behavior under various conditions before final implementation.

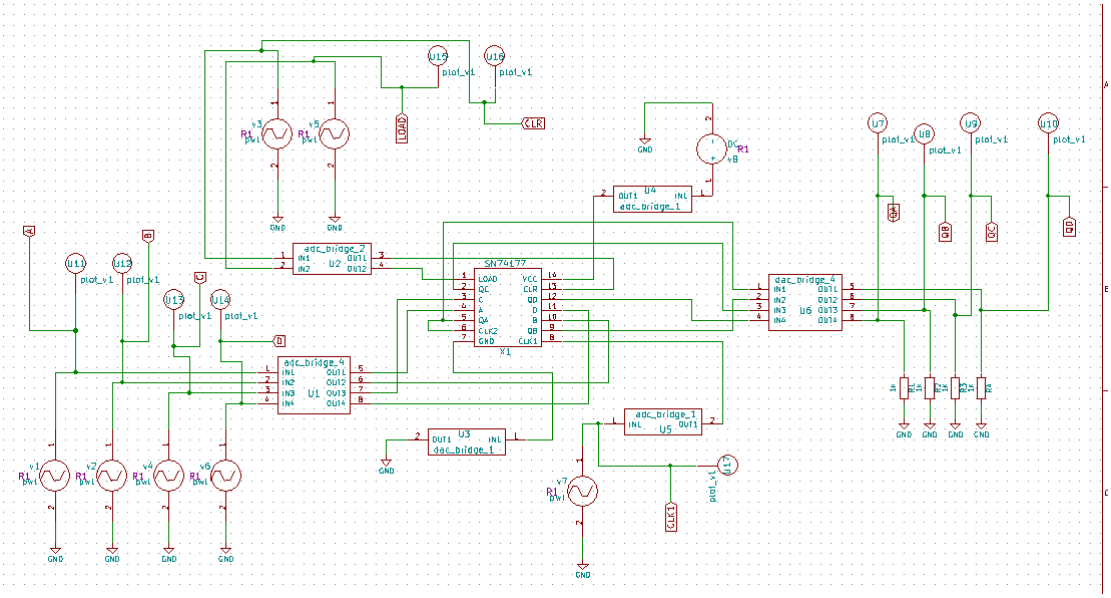

Figure 7.3: Test Circuit Schematic of SN74177 IC

7.4 Input Waveforms

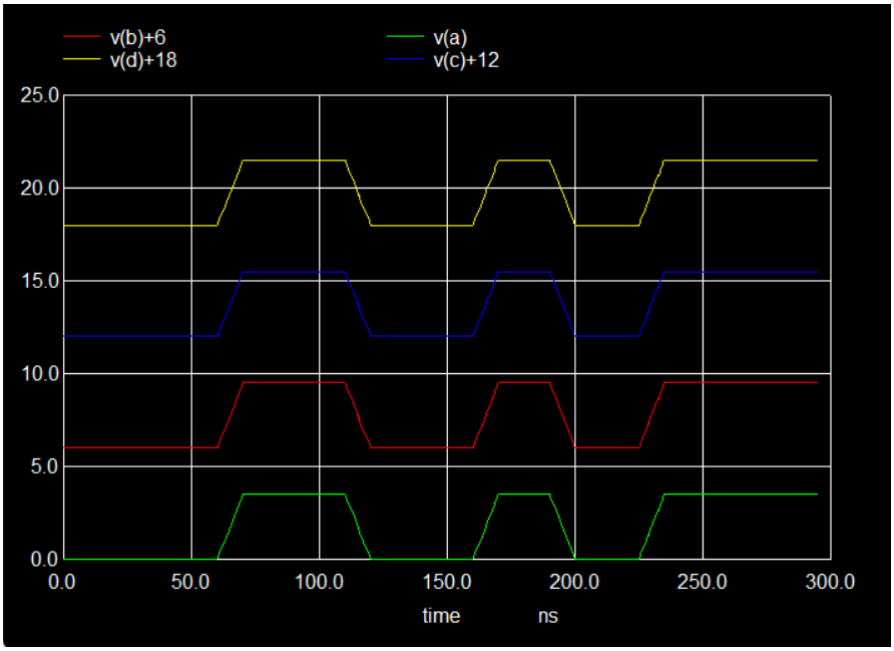

Figure 7.4: Input Data Signal of SN74177 IC

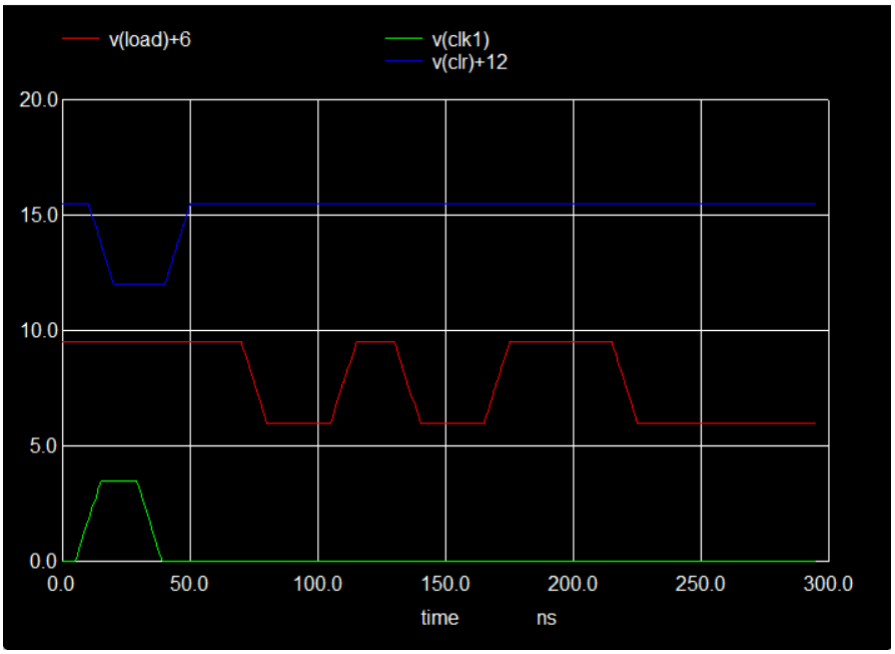

Figure 7.5: Input signals of SN74177 IC

7.5 Output Waveform

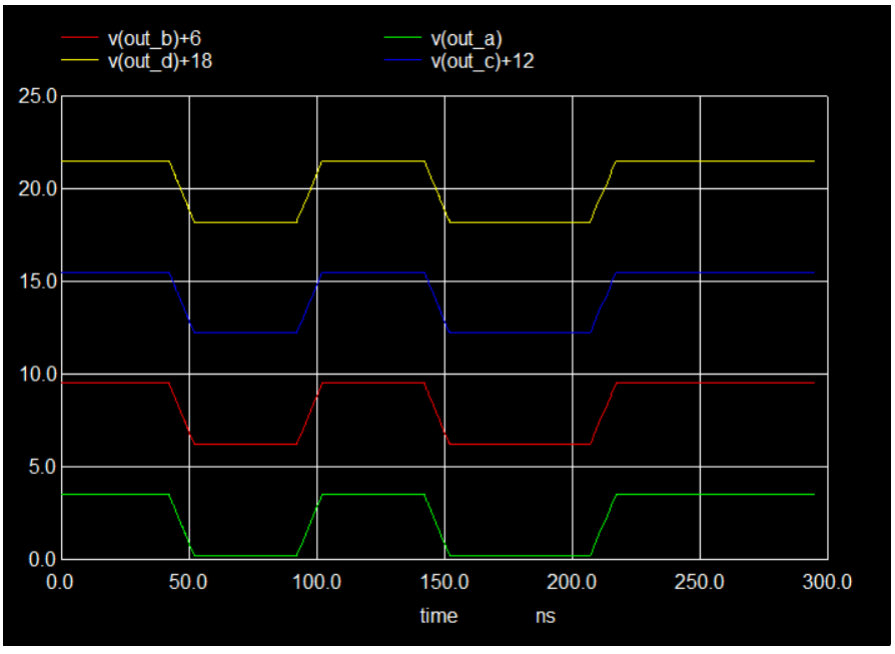

Figure 7.6: Output signals of SN74177 IC

Chapter 8

SN74LS396

These octal registers are organized as two 4-bit bytes of storage. Upon application of a positive-going clock signal, the information stored in byte 1 is transferred into byte 2 as a new 4-bit byte is loaded into the byte 1 location via the four data lines. The full 8-bit word is available at the outputs after two clock cycles. Both the clock and the strobe lines are fully buffered,

8.1 Pin Diagram

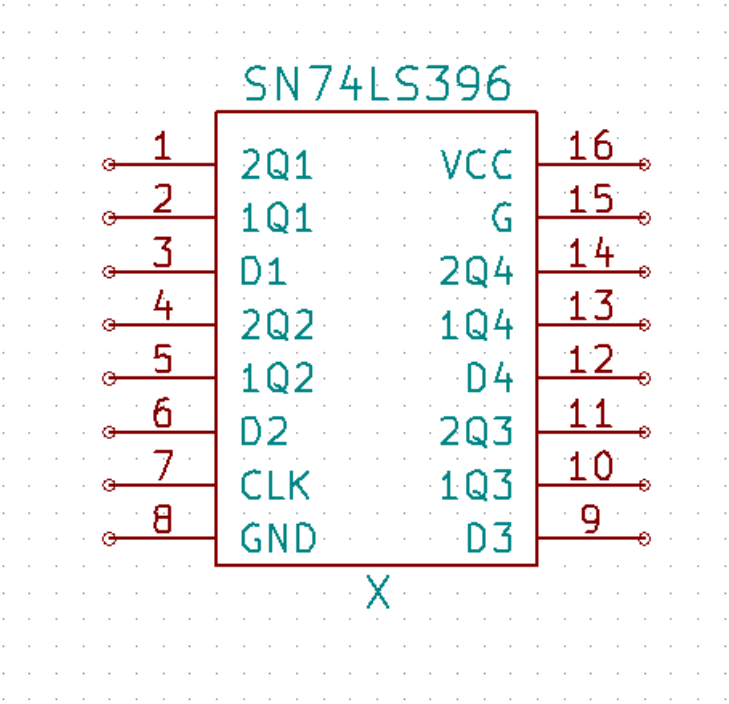

Figure 8.1: Pin Configuration of SN74LS396

8.2 Sub Circuit Schematic

The Subcircuit layout presented here represents the detailed design of IC SN74LS396. The design consists of all the essential components required for the stable operation and the optimal performance of the IC in various different applications.

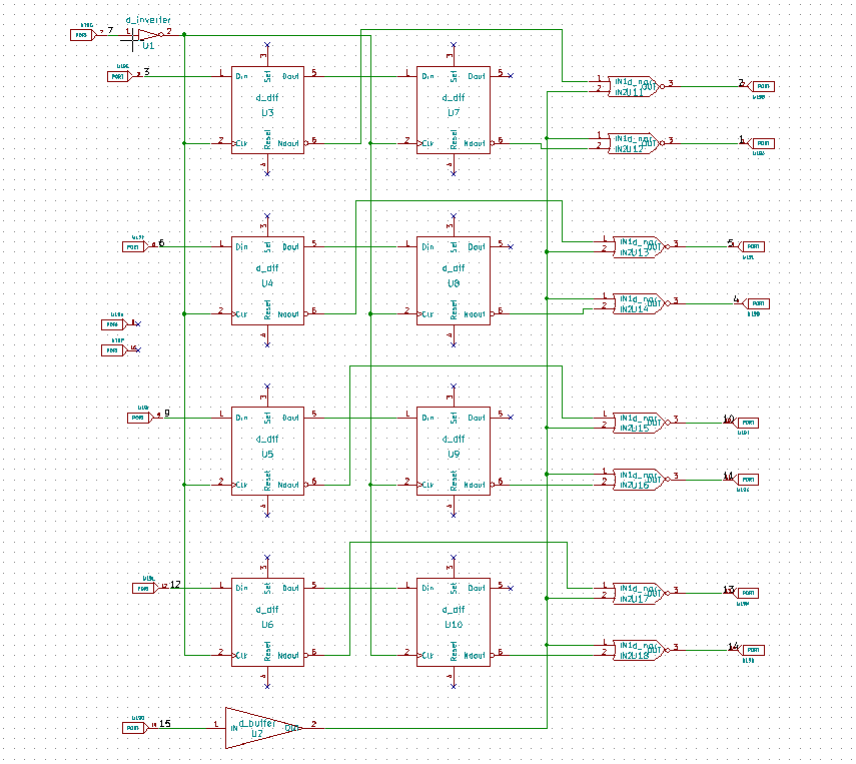

Figure 8.2: SubCircuit Schematic of SN74LS396 IC

8.3 Test Circuit

The test circuit for the SN74LS396 is designed to evaluate the performance and functionality of the IC using the subcircuit approach. By utilizing the Subcircuit feature, this test circuit can be easily integrated into simulation and analysis environments to verify the ICs behavior under various conditions before final implementation.

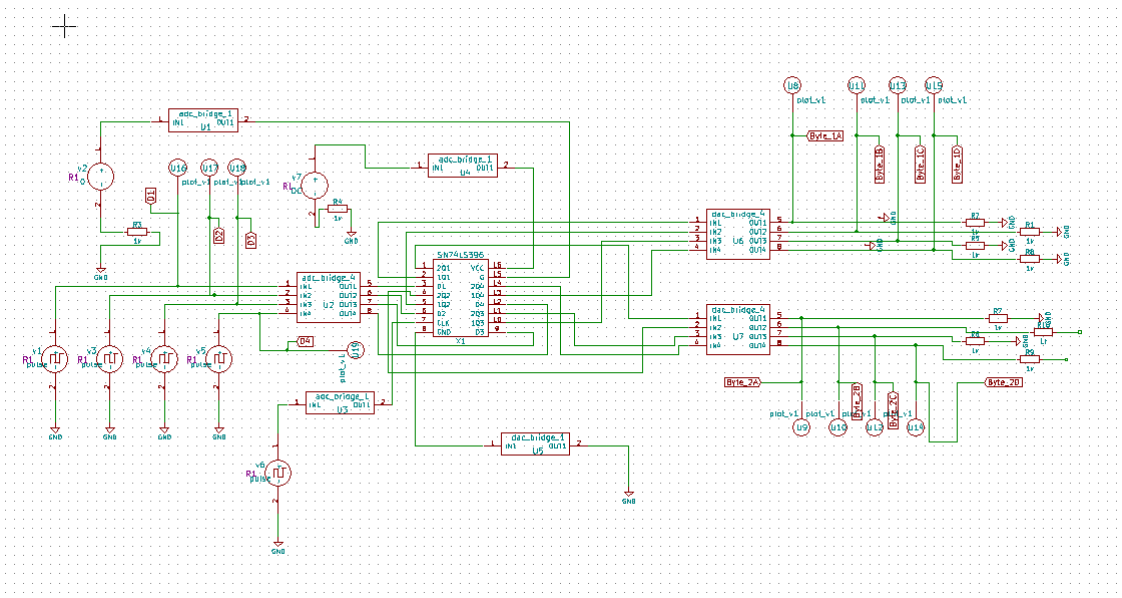

Figure 8.3: Test Circuit Schematic of SN74LS396 IC

8.4 Input Waveforms

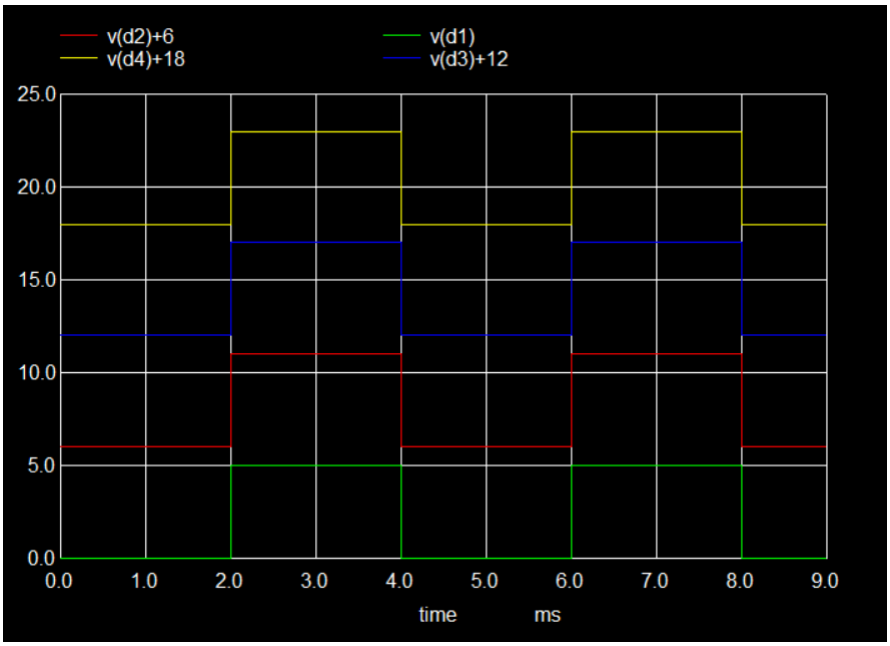

Figure 8.4: Input Data Signal of SN74LS396 IC

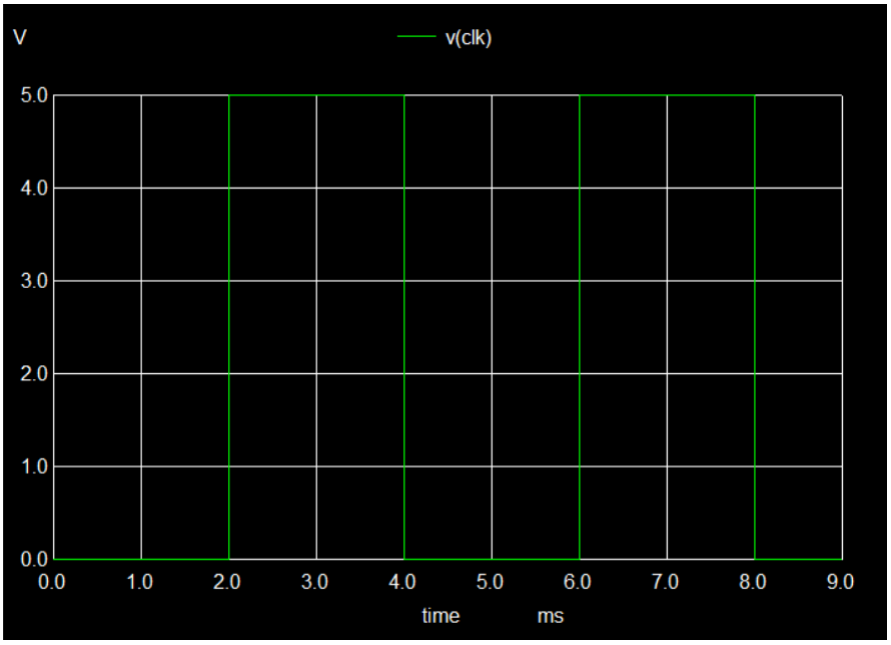

Figure 8.5: CLK signal of SN74LS396‘ IC

8.5 Output Waveform

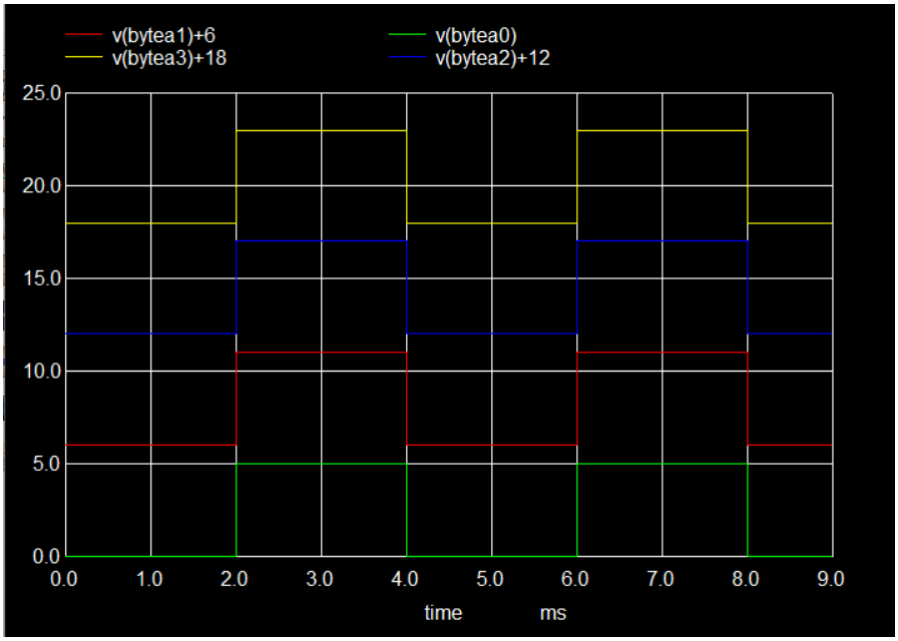

Figure 8.6: 1st Output Byte Signal of SN74LS396 IC

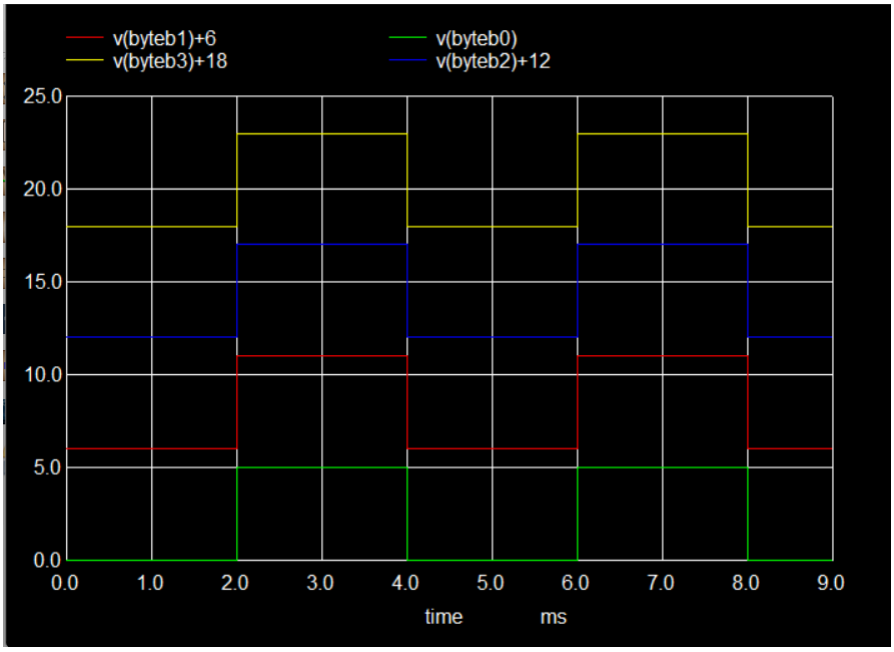

Figure 8.7: 2nd Output Byte Signal of SN74LS396 IC

Chapter 9

74HC563

The 'HC563, and CD74HCT563 are high-speed Octal Transparent Latches. The outputs are transparent to the inputs when the latch enable (LE is high. When the latch enable (LE) goes low the data is latched. The output enable (OE) controls the three-state outputs. When the output enable (OE) is high the outputs are in the high impedance state. The latch operation is independent of the state of the output enable

9.1 Pin Diagram

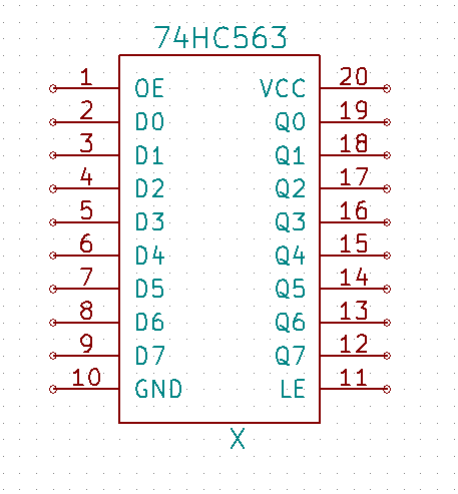

Figure 9.1: Pin Configuration of 74HC563 IC

9.2 Sub Circuit Schematic

The Subcircuit layout presented here represents the detailed design of IC 74HC563. The design consists of all the essential components required for the stable operation and the optimal performance of the IC in various different applications.

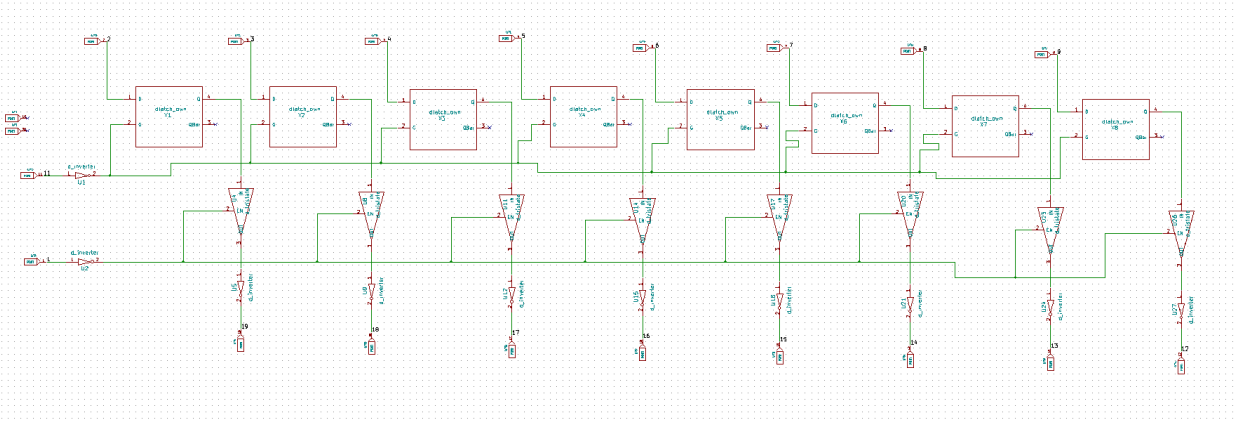

Figure 9.2: SubCircuit Schematic of 74HC563 IC

9.3 Test Circuit

The test circuit for the 74HC563 is designed to evaluate the performance and functionality of the IC using the subcircuit approach. By utilizing the Subcircuit feature, this test circuit can be easily integrated into simulation and analysis environments to verify the ICs behavior under various conditions before final implementation.

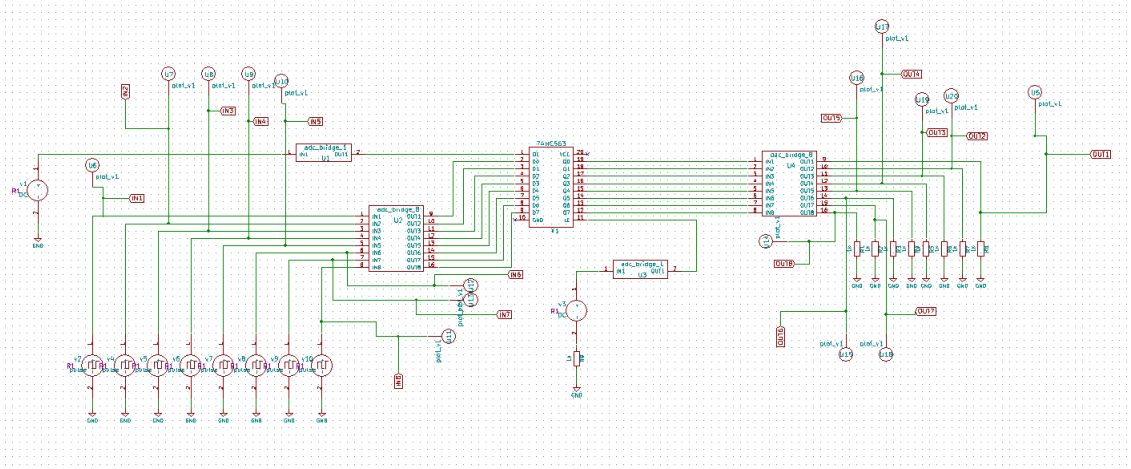

Figure 9.3: Test Circuit Schematic of 74HC563 IC

9.4 Input Waveforms

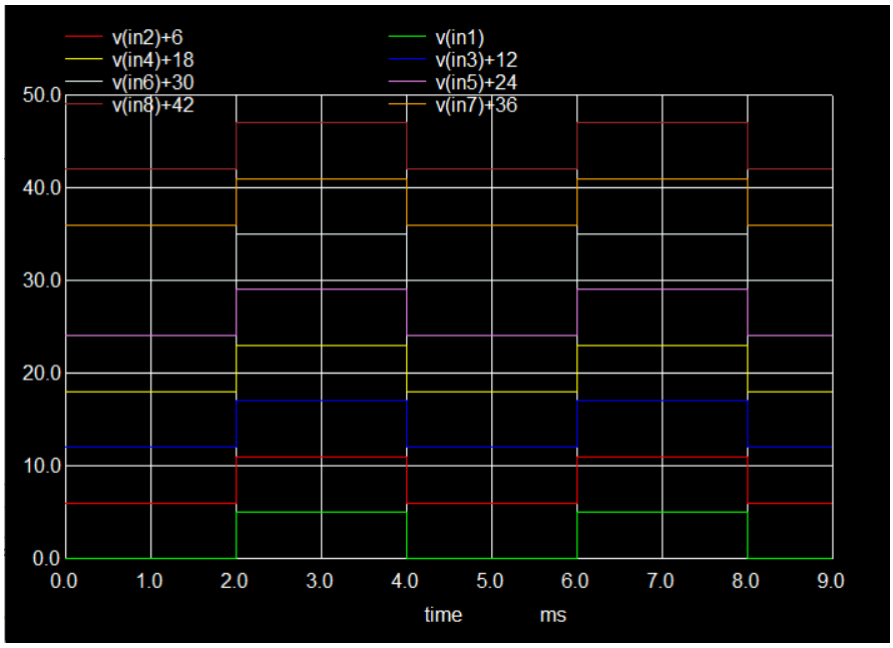

Figure 9.4: Input Data Signal of 74HC563 IC

9.5 Output Waveform

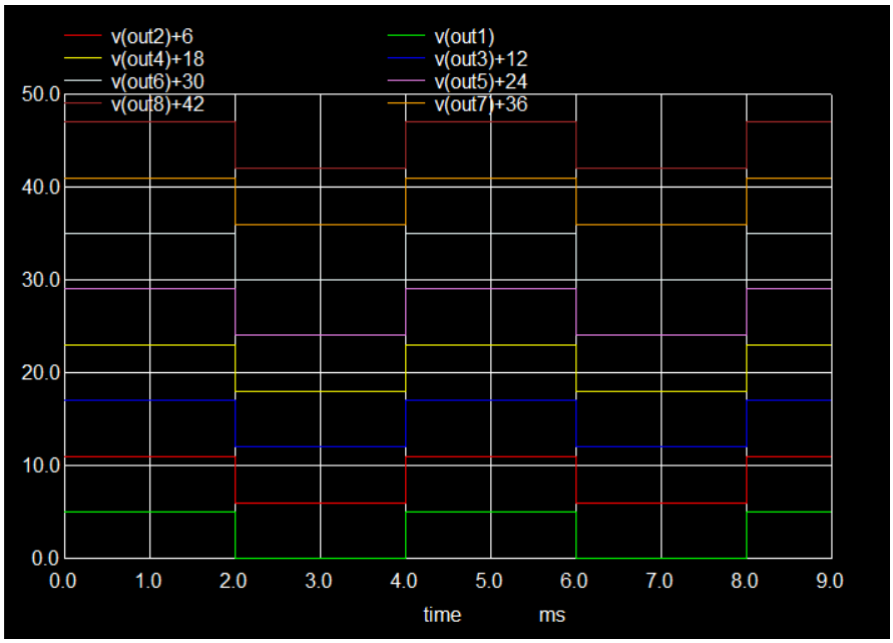

Figure 9.5: Output Signal of 74HC563 IC

Chapter 10

74AHC1G4210

74AHC1G4210 is a 10-stage divider and oscillator. It consists of a chain of 10 flip-flops. Each flip-flop divides the frequency of the previous flip-flop by two, consequently the 74AHC1G4210 counts up to 210 = 1024. The single inverting stage (X1 to X2) functions as a crystal oscillator or an input buffer for an external oscillator. When used as a buffer the output X2 should be left floating. The frequency of the output (Q) is the frequency applied to X1 divided by 1024. The divider advances on the negative-going transition of X1.

The X1 input is overvoltage tolerant. This feature allows the use of this device as a voltage level translator in mixed voltage environments.

10.1 Pin Diagram

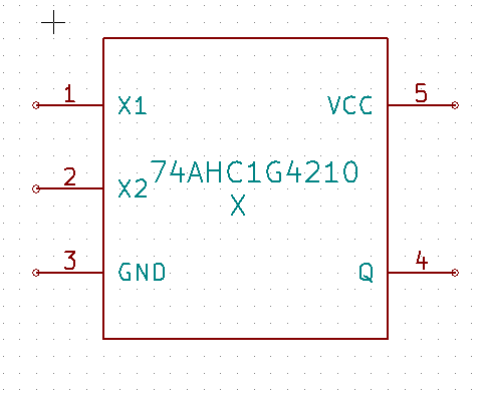

Figure 10.1: Pin Configuration of 74AHC1G4210

10.2 Sub Circuit Schematic

The Subcircuit layout presented here represents the detailed design of IC 74AHC1G4210. The design consists of all the essential components required for the stable operation and the optimal performance of the IC in various different applications.

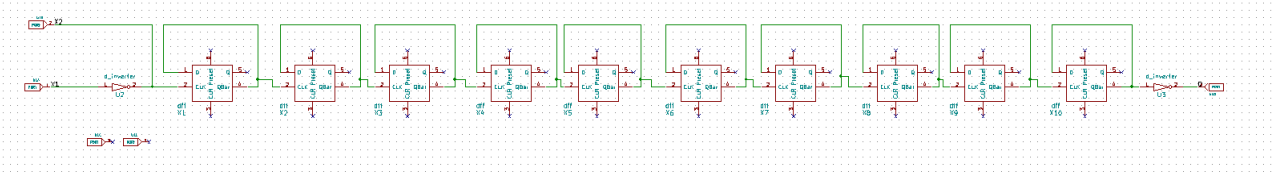

Figure 10.2: SubCircuit Schematic of 74AHC1G4210 IC

10.3 Test Circuit

The test circuit for the 74AHC1G4210 is designed to evaluate the performance and functionality of the IC using the subcircuit approach. By utilizing the Subcircuit feature, this test circuit can be easily integrated into simulation and analysis environments to verify the ICs behavior under various conditions before final implementation. In this circuit we will demonstrate the divider operation of 74AHC1G4210 IC

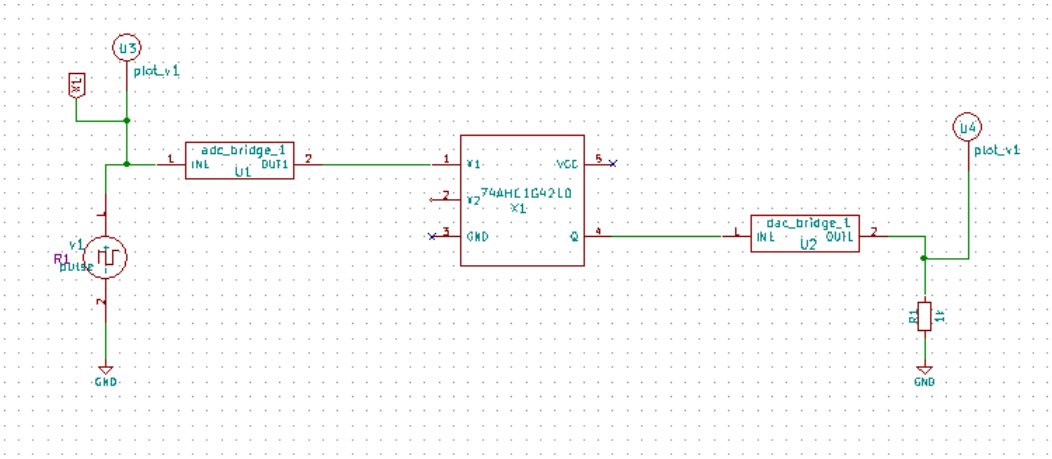

Figure 10.3: Test Circuit Schematic of 74AHC1G4210 IC

10.4 Input Waveforms

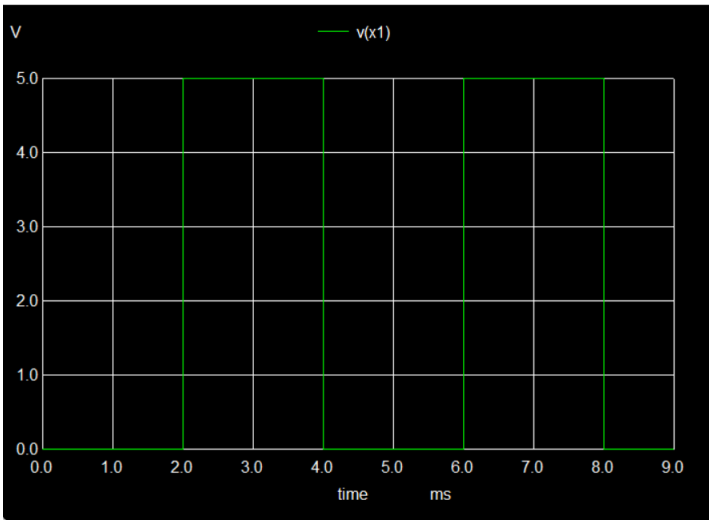

Figure 10.4: Input Data Signal of 74AHC1G4210 IC

10.5 Output Waveform

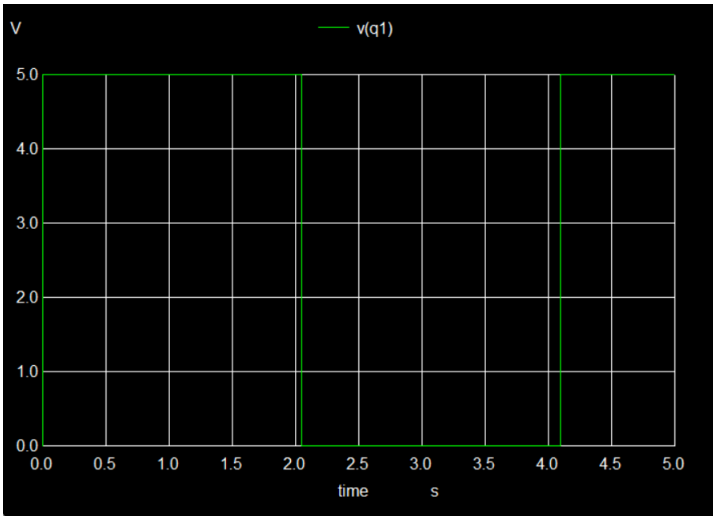

Figure 10.5: Output Signal of 74AHC1G4210 IC

Chapter 11

SN7482

SN7482 IC is a 2-bit binary full adder. These full adders perform the addition of two 2-bit binary numbers. The sum outputs (sigma1 and sigma2) are provided for each bit and the resultant carry (C2) is obtained from the second bit

11.1 Pin Diagram

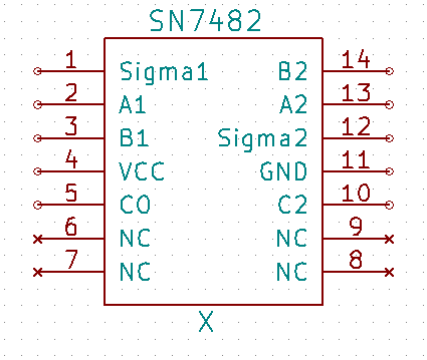

Figure 11.1: Pin Configuration of SN7482

11.2 Sub Circuit Schematic

The Subcircuit layout presented here represents the detailed design of IC SN7482. The design consists of all the essential components required for the stable operation and the optimal performance of the IC in various different applications.

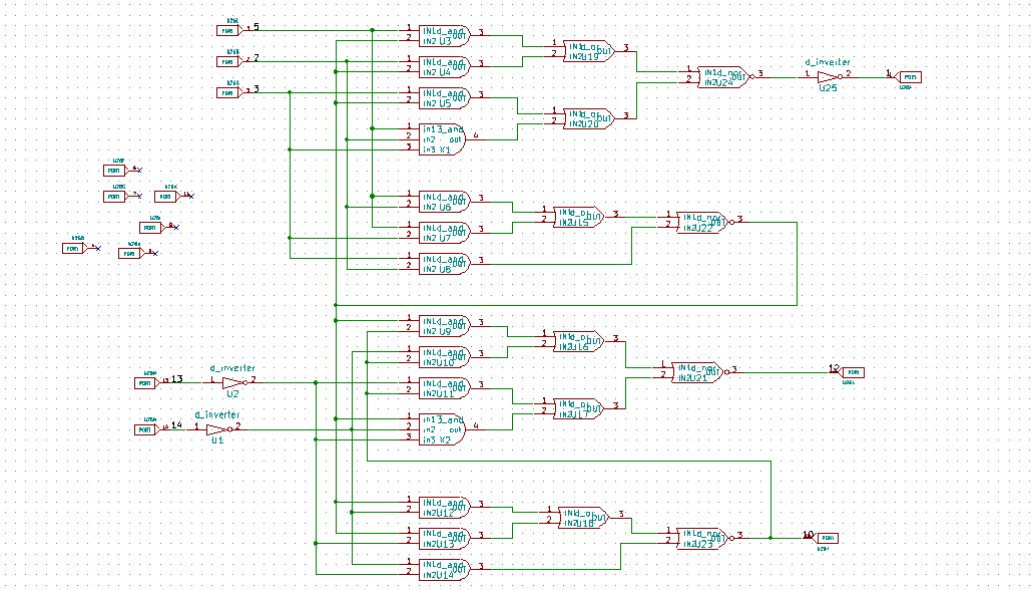

Figure 11.2: SubCircuit Schematic of SN7482 IC

11.3 Test Circuit

The test circuit for the SN7482 is designed to evaluate the performance and functionality of the IC using the subcircuit approach. By utilizing the Subcircuit feature, this test circuit can be easily integrated into simulation and analysis environments to verify the ICs behavior under various conditions before final implementation. In this circuit we will demonstrate the adder operation of SN7482 IC by giving the inputs Bit1 and Bit2 as two binary inputs and a carry in input(C0) and the output is obtained at Sigma1 and Sigma2 along with a carry out(C2)

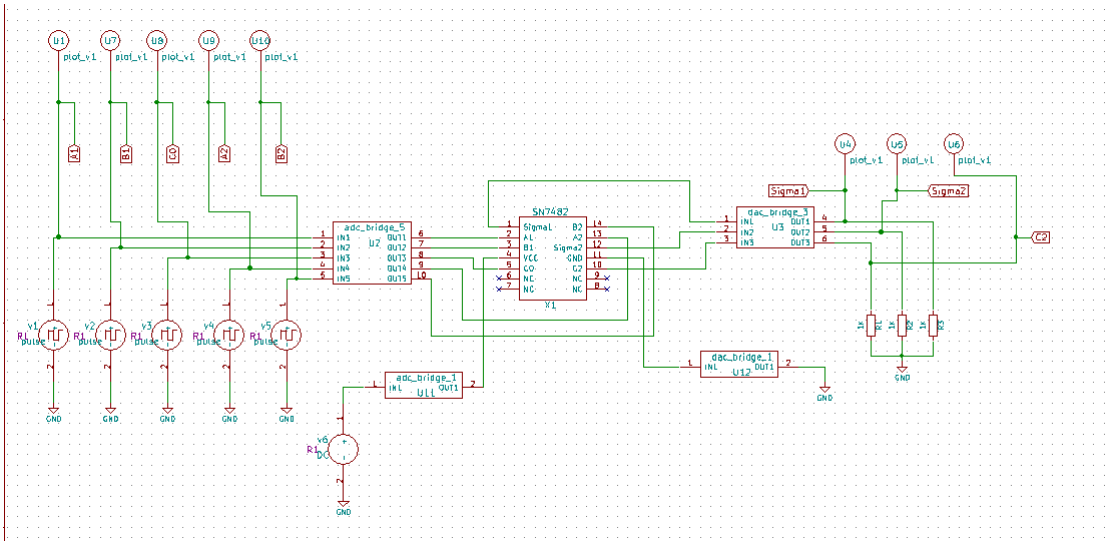

Figure 11.3: Test Circuit Schematic of SN7482 IC

11.4 Input Waveforms

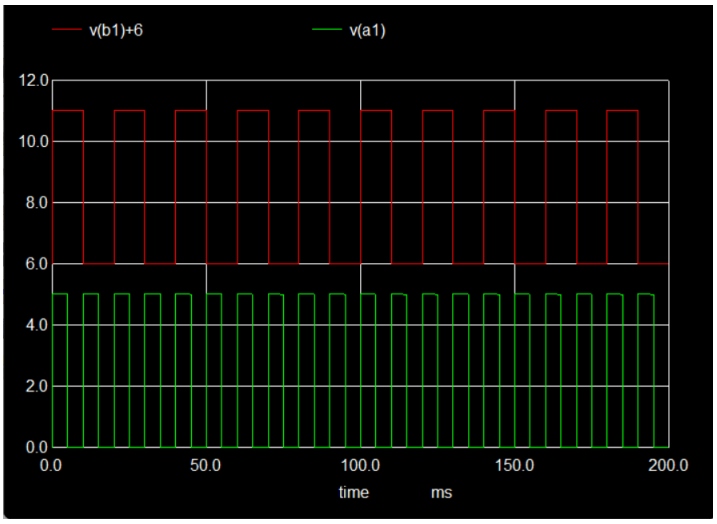

Figure 11.4: 1st Input Bit - Bit1 of SN7482 IC

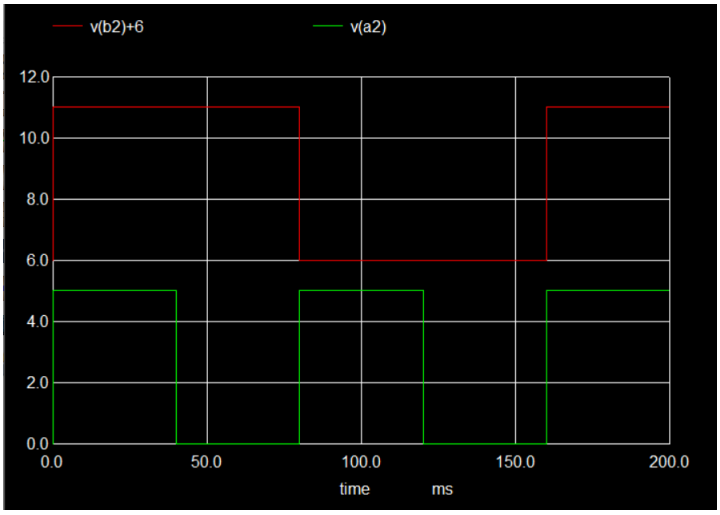

Figure 11.5: 2nd Input Bit - Bit2 of SN7482 IC

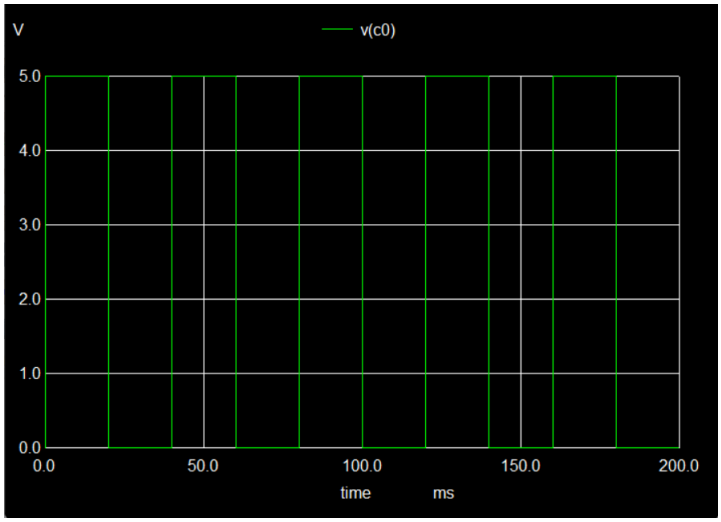

Figure 11.6: Carry in signal(C0) of SN7482 IC

11.5 Output Waveform

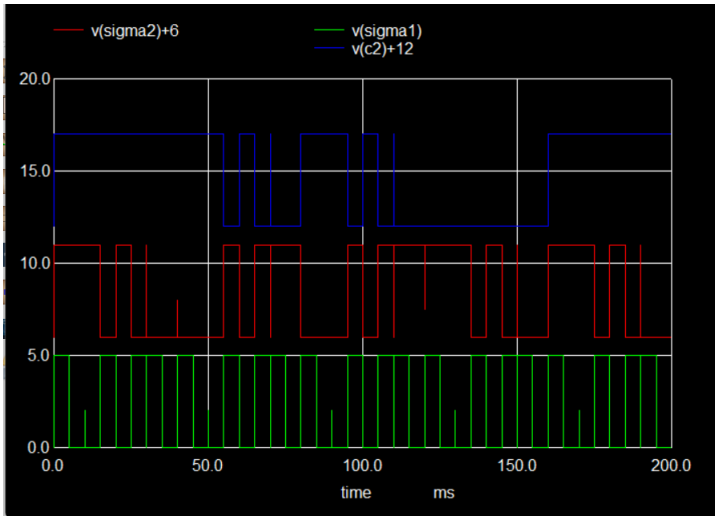

Figure 11.7: Output Signals of SN7482 IC

Chapter 12

74AHC1G4212

74AHC1G4212 is a 12-stage divider and oscillator. It consists of a chain of 12 flip-flops. Each flip-flop divides the frequency of the previous flip-flop by two, consequently the 74AHC1G4212 counts up to 212 = 4096. The single inverting stage (X1 to X2) functions as a crystal oscillator or an input buffer for an external oscillator. When used as a buffer the output X2 should be left floating. The frequency of the output (Q) is the frequency applied to X1 divided by 4096. The divider advances on the negative-going transition of X1.

The X1 input is overvoltage tolerant. This feature allows the use of this device as a voltage level translator in mixed voltage environments.

12.1 Pin Diagram

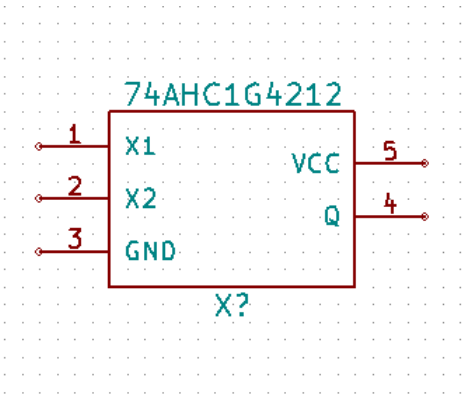

Figure 12.1: Pin Configuration of 74AHC1G4212

12.2 Sub Circuit Schematic

The Subcircuit layout presented here represents the detailed design of IC 74AHC1G4212. The design consists of all the essential components required for the stable operation and the optimal performance of the IC in various different applications.

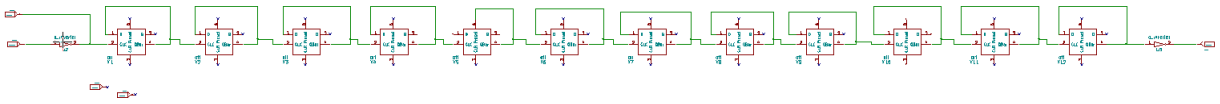

Figure 12.2: SubCircuit Schematic of 74AHC1G4212 IC

12.3 Test Circuit

The test circuit for the 74AHC1G4212 is designed to evaluate the performance and functionality of the IC using the subcircuit approach. By utilizing the Subcircuit feature, this test circuit can be easily integrated into simulation and analysis environments to verify the ICs behavior under various conditions before final implementation. In this circuit we will demonstrate the divider operation of 74AHC1G4210 IC

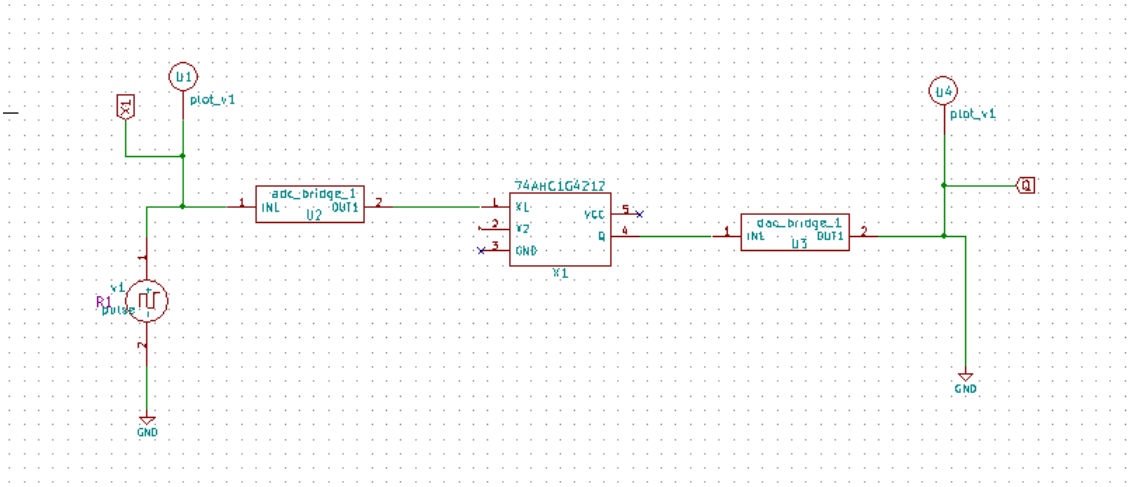

Figure 12.3: Test Circuit Schematic of 74AHC1G4210 IC

12.4 Input Waveforms

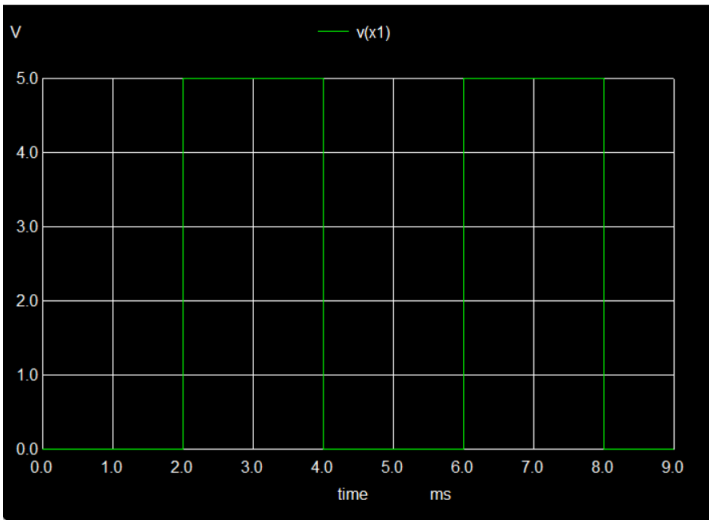

Figure 12.4: Input Data Signal of 74AHC1G4212 IC

12.5 Output Waveform

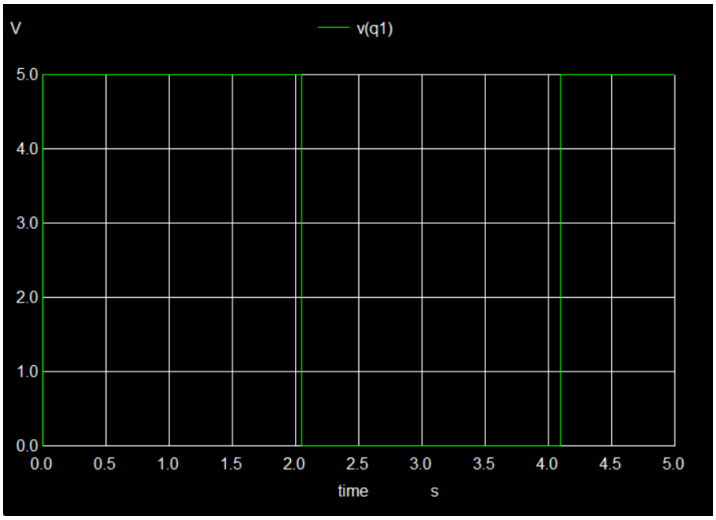

Figure 12.5: Output Signal of 74AHC1G4212 IC

Chapter 13

SN74S350

The 'S350 is operationally equivalent to a 4-input multiplexer with the inputs connected so that the select code causes shifts of the data word. This makes it possible to perform shifts of 0, 1 , 2, or 3 places on words of any length, with suitable interconnection.

A 7-bit data word is introduced at the D inputs and is shifted according to the code applied to the select inputs SO and S1 . Y0 through Y3 are 3 -state outputs controlled by an output enable, OE. When OE is low, the outputs follow the selected data inputs; when OE is high, the outputs are in a high-impedance state. This feature allows shifters to be cascaded on the same output lines or to a common bus. The shift function can be logical with zeroes pulled in at either or both ends of the shifting field, arithmetic with the sign bit repeated during a shift down, or end-around with the data word forming a continuous loop.

13.1 Pin Diagram

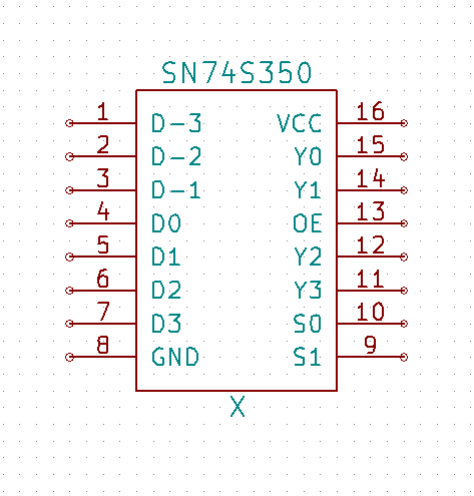

Figure 13.1: Pin Configuration of SN74S350 IC

13.2 Sub Circuit Schematic

The Subcircuit layout presented here represents the detailed design of IC SN74S350. The design consists of all the essential components required for the stable operation and the optimal performance of the IC in various different applications.

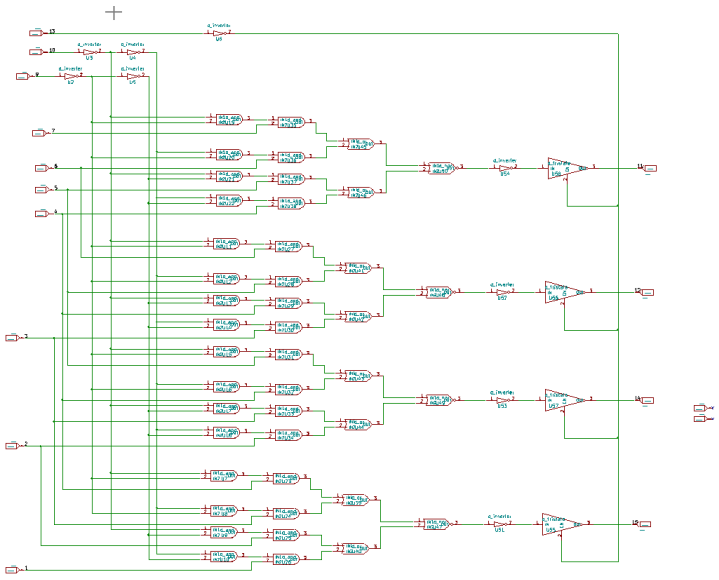

Figure 13.2: SubCircuit Schematic of SN74S350 IC

13.3 Test Circuit

The test circuit for the SN74S350 is designed to evaluate the performance and functionality of the IC using the subcircuit approach. By utilizing the Subcircuit feature, this test circuit can be easily integrated into simulation and analysis environments to verify the ICs behavior under various conditions before final implementation. Here the first case is tested and the outputs are verified

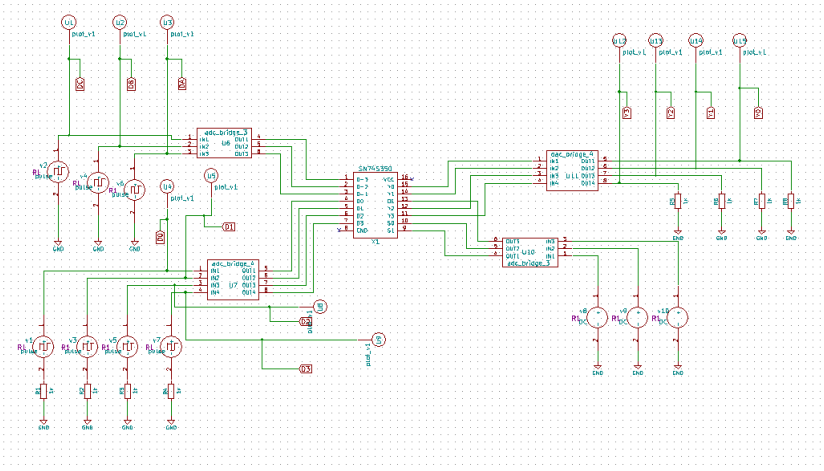

Figure 13.3: Test Circuit Schematic of SN74S350 IC

13.4 Input Waveforms

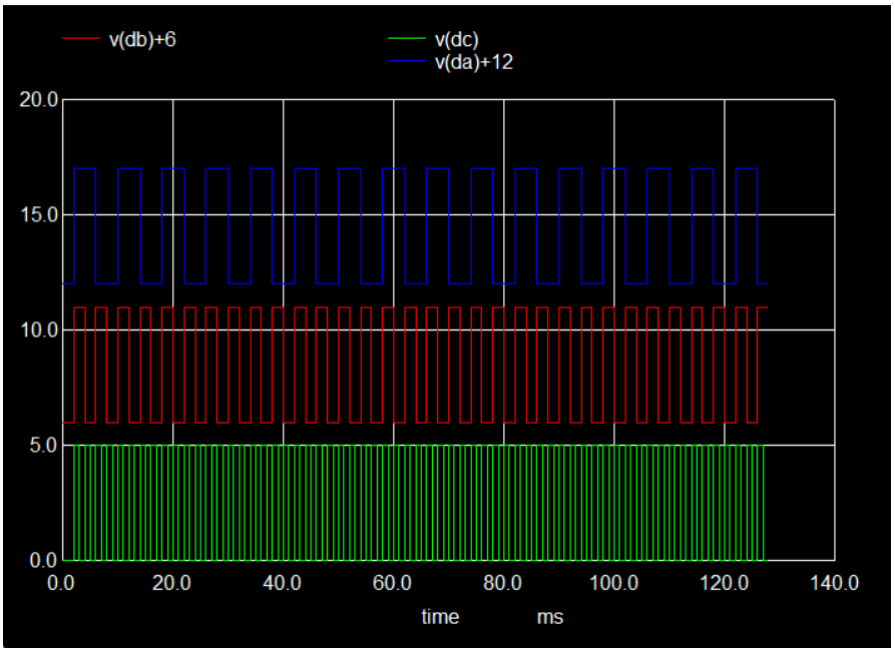

Figure 13.4: Input Data Signal of SN74S350 IC

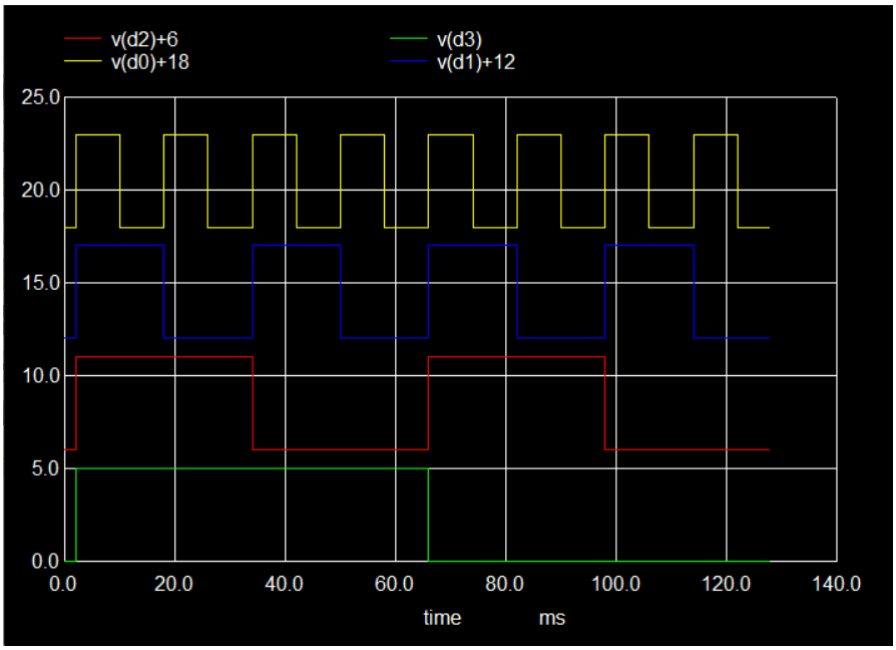

Figure 13.5: Input Data Signal of SN74S350 IC

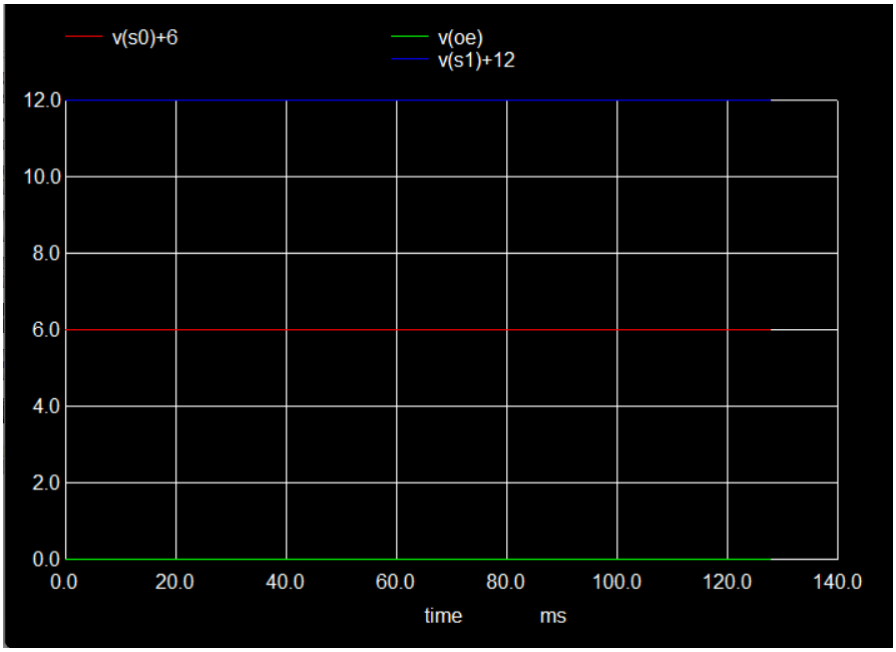

Figure 13.6: Output Enable and Select lines of SN74S350 IC

13.5 Output Waveform

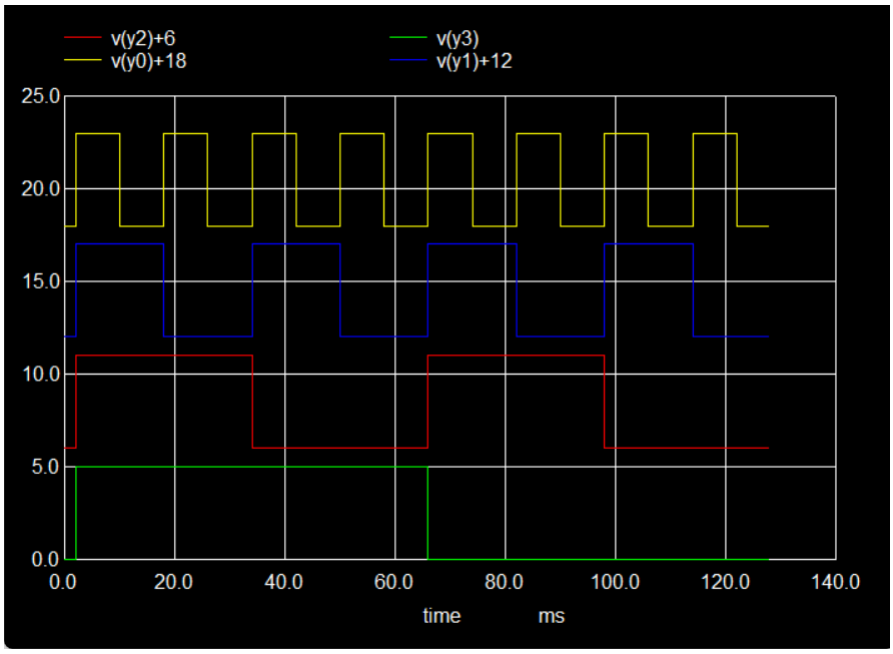

Figure 13.7: Output Signal of SN74S350 IC

Chapter 14

Conclusion and Future Scope

The project successfully met its goal of creating a wide variety of subcircuits of various digital ICs. Each IC model was carefully designed using details from official datasheets and tested thoroughly with suitable test circuits to ensure they work correctly. The components developed include essential building blocks like Shift Registers, Divider, Multiplexers, De-Multiplexers, and various Logic other IC's.

These IC models are now ready to be added to the eSim subcircuit library, making them easily accessible to developers, students, and researchers. Their inclusion will greatly improve the capabilities of eSim by allowing users to use these standard ICs directly in their projects and circuit designs.

This project also lays the groundwork for further expansion of the eSim library. In the future, more such ready-to-use IC models are expected to be developed, helping to grow the collection of components available. This ongoing effort will support both academic and research work, while also strengthening the open-source EDA (Electronic Design Automation) ecosystem.

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