Summer Fellowship Report

On

Integrated Circuit Design using Subcircuit feature of eSim

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Acknowledgment

I take this opportunity to express my heartfelt gratitude to the FOSSEE, IIT Bombay team for offering me this wonderful opportunity to work on the design and integration of multiple sub-circuits in eSim. Working on eSim has provided me with invaluable insights into various open-source EDA tools for circuit simulation and their practical applications.

I am sincerely thankful to Prof. Kannan M. Moudgalya for his invaluable guidance and motivation throughout this fellowship program.

I would also like to express my deep appreciation to the entire FOSSEE team, including my mentors Mr. Sumanto Kar, Mrs. Vineeta Ghavri, and Mrs. Usha Vishwanathan, for constantly guiding and mentoring me throughout the duration of the internship.

It was with their unwavering support that I was able to successfully meet the demands of the project. Whenever I faced an issue, my mentors were always accessible and eager to help me assess and debug the problems. The insights and knowledge I gained from them have been invaluable and will continue to benefit me in the future.

Overall, it was a delightful experience interning at FOSSEE and contributing to its growth. As an enthusiastic beginner in the semiconductor industry, this internship marks an important milestone in my pursuit of a successful career.

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Chapter 1

Introduction

FOSSEE, which stands for Free/Libre and Open Source Software for Education, is an organization based at IIT Bombay, as a remarkable initiative aimed at promoting the use of open-source software in education and research. It was established with the mission to reduce the dependency on proprietary software and to encourage the adoption of open-source alternatives. FOSSEE offers a wide range of tools and resources that cater to various academic and professional needs.

It provides comprehensive documentation, tutorials, workshops, and hands-on training sessions, for empowering students, educators, and professionals to leverage open-source software for their projects and coursework. The organizations commitment to fostering a collaborative and inclusive environment has significantly contributed to the democratization of technology and has opened up new avenues for innovation and learning.

1.1 eSim

eSim, created by the FOSSEE project at IIT Bombay, is a versatile open-source software tool for circuit design and simulation. It combines various open-source software packages into one cohesive platform, making it easier to design, simulate, and analyze electronic circuits. This tool is particularly useful for students, educators, and professionals who need an affordable and accessible alternative to proprietary software.

eSim offers features for schematic creation, circuit simulation, PCB design, and includes an extensive library of components. The Subcircuit feature is a significant enhancement, enabling users to design complex circuits by integrating simpler subcircuits. Through eSim, FOSSEE promotes the use of open-source solutions in engineering education and professional fields, encouraging innovation and collaboration.

1.2 NgSpice

NgSpice is the open-source spice simulator for electric and electronic circuits. Such a circuit may comprise JFETs, bipolar and MOS transistors, passive elements like

R, L, or C, diodes, transmission lines, and other devices, all interconnected in a netlist.

Digital circuits are simulated as well, event-driven and fast, from single gates to complex circuits and the combination of both analog and digital as well as mixed-signal circuits. NgSpice offers a wealth of device models for active, passive, analog, and digital elements. Model parameters are provided by our collections, by the semiconductor device manufacturers, or from semiconductor foundries. The user adds her circuits as a netlist, and the output is one or more graphs of currents, voltages, and other electrical quantities or is saved in a data file.

1.3 Makerchip

Makerchip is a platform that offers convenient and accessible access to various tools for digital circuit design. It provides both browser-based and desktop-based environments for coding, compiling, simulating, and debugging Verilog designs. Makerchip supports a combination of open-source tools and proprietary ones, ensuring a comprehensive range of capabilities.

One can simulate Verilog/SystemVerilog/Transaction-Level Verilog code in Makerchip. eSim is interfaced with Makerchip using a Python-based application called Makerchip-App, which launches the Makerchip IDE. Makerchip aims to make circuit design easy and enjoyable for users of all skill levels. The platform provides a user-friendly interface, intuitive workflows, and a range of helpful features that simplify the design process and enhance the overall user experience.

The main drawback of these open-source tools is that they are not comprehensive. Some of them are capable of PCB design (e.g., KiCad) while some of them are capable of performing simulations (e.g., gEDA). To the best of my knowledge, there is no open-source software that can perform circuit design, simulation, and layout design together. eSim is capable of doing all of the above.

1.4 Current Date and Time

The current date and time of this report preparation is Monday 30$^{\text{th}}$ June, 2025 at 2:49 PM IST on Monday, June 30, 2025.

Chapter 2

Features Of eSim

The objective behind the development of eSim is to provide an open source EDA solution for electronics and electrical engineers. The software should be capable of performing schematic creation, PCB design and circuit simulation (analog, digital and mixed-signal). It should provide facilities to create new models and components. Thus, eSim offers the following features -

1. Schematic Creation: eSim provides an easy-to-use graphical interface for drawing schematic diagrams, making it accessible for users of all levels. I can drag and drop components from the library onto the schematic, simplifying the design process. Comprehensive editing tools allow me to easily modify schematics, including moving, rotating, and labeling components.

2. Circuit Simulation: eSim supports SPICE (Simulation Program with Integrated Circuit Emphasis), a standard for simulating analog and digital circuits. I can perform various types of analysis such as transient, AC, and DC, providing insights into circuit behavior over time and frequency. An integrated waveform viewer helps me visualize simulation results, aiding in the analysis and debugging of circuit designs.

3. PCB Design: The PCB layout editor allows me to place components and route traces with precision. eSim includes DRC (Design Rule Check) capabilities to ensure that the PCB design adheres to manufacturing constraints and electrical rules. I can generate Gerber files, which are standard for PCB fabrication, directly from my designs.

4. Subcircuit Feature: This feature enables me to create complex circuits by integrating simpler subcircuits, promoting modular design approaches. Subcircuits can be reused in different projects, saving time and effort in redesigning common circuit elements.

5. Open Source Integration: eSim integrates several open-source tools like KiCad, Ngspice, and GHDL, providing a comprehensive suite for electronic design automation. Being open-source, eSim is free to use, making advanced circuit design tools accessible without the need for expensive licenses.

Chapter 3

Problem Statement

To design and develop various Analog and Digital Integrated Circuit Models in the form of sub-circuits using device model files already present in the eSim library. These IC models should be useful in the future for circuit designing purposes by developers and users, once I get them successfully integrated into the eSim subcircuit library.

3.1 Approach

My approach to implementing the problem statement began with examining datasheets from prominent Integrated Circuit (IC) manufacturers such as Texas Instruments, Analog Devices, and NXP Semiconductors. I selected ICs that offer a diverse range of functionalities, including precision amplifiers, comparators, encoders, and audio amplifiers. After building the subcircuits, I tested them to verify basic circuit configurations.

The step-by-step roadmap of this process is outlined below:

1. Analyzing Datasheets: The primary step is to browse through various available datasheets and hence find suitable circuits to implement in eSim that are not previously included into the eSim library. I check for the detailed schematic of the ICs and once I ascertain the component values and the truth table, I then finalize the IC to be created.

2. Subcircuit Creation: After deciding the IC, I start modeling it as a subcircuit in eSim, using the model files present in the eSim device model library only. The design is strictly according to the information given in the official datasheets of the ICs. This step also includes building the Symbol/Pin diagram of the IC according to the packaging and pin description given in the datasheets only.

3. Test Circuit Design: Once the component of the IC is ready, I now can build the test circuits, according to the datasheets. In this step, I build the test cases and test circuits using the component IC.

4. Schematic Testing: Once the test circuits are ready, now it is time to simulate the test circuits so that the output can be obtained in the form of waveforms and plots. Here I take help of KiCad to NgSpice conversion and Simulation feature in eSim.

If the output of the test circuit is not as per expectation, this implies that the test case has failed, and there is some error in the schematic. In such cases, I go back to the design phase of the IC or the test circuits, to look for possible errors and then repeat the testing process again after making required changes.

Once the expected output of the test cases are correct and satisfy the expected results, then in such a case the IC is declared successfully working. The test case has been verified and the designing process is complete.

Chapter 4

Integrated Circuit Design

4.1 74HC27

The 74HC27 is used in digital logic applications where a triple 3-input NOR function is needed. It is commonly used in arithmetic circuits, control systems, and data processing applications. Its high-speed operation and compact logic implementation make it ideal for modern logic systems requiring efficient performance.

4.1.1 Truth Table

Table 3. Function table

H = HIGH voltage level; L = LOW voltage level; X = don't care.

Inputs			Outputs
nA	**nB**	**nC**	**nY**
L	L	L	H
X	X	H	L
X	H	X	L
H	X	X	L

Figure 4.1: Truth Table of 74HC27

The figure shows the truth table for the 74HC27 IC, detailing the output for all possible combinations of the three input signals.

4.1.2 Pin Diagram

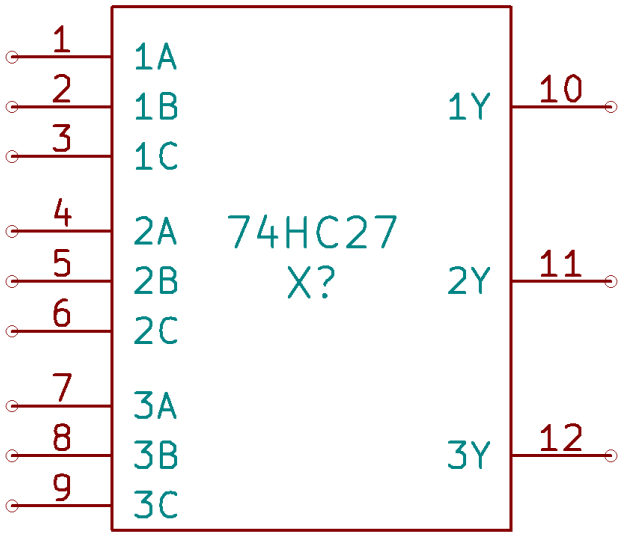

Figure 4.2: Pin Diagram of 74HC27

The figure shows the physical representation of the 74HC27 IC, indicating the arrangement of its pins. It includes input pins, an output pin, a power supply pin, and a ground pin. The pin diagram is essential for correctly integrating the IC into a circuit, ensuring proper connections and functionality in digital applications.

4.1.3 Sub Circuit Layout

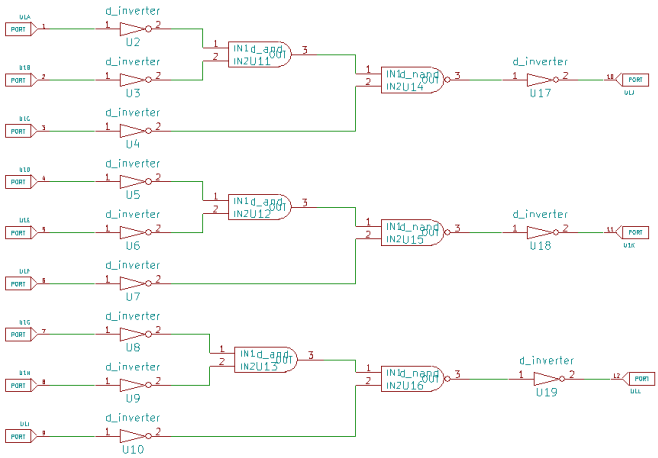

Figure 4.3: Sub Circuit Layout of 74HC27

The figure represents the internal design of the 74HC27 IC, showing how logic gates and components are interconnected within the chip. This layout determines how the

IC processes input signals to generate the required output. Understanding the sub-circuit helps in optimizing circuit performance and ensuring efficient logic operation.

4.1.4 Test Circuit

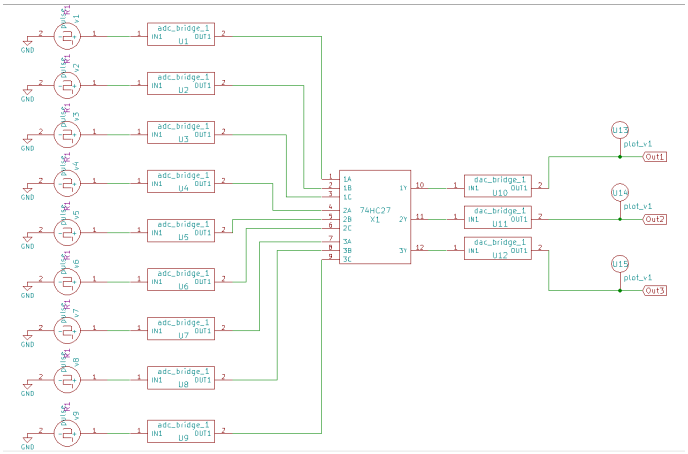

Figure 4.4: Test Circuit of 74HC27

The figure illustrates a test setup used to verify the performance of the 74HC27 IC. A test circuit includes a power source, input signal generators, and output monitoring devices such as oscilloscopes or logic analyzers. This setup helps evaluate response time, signal integrity, and overall functionality under different conditions.

4.1.5 Input Waveform

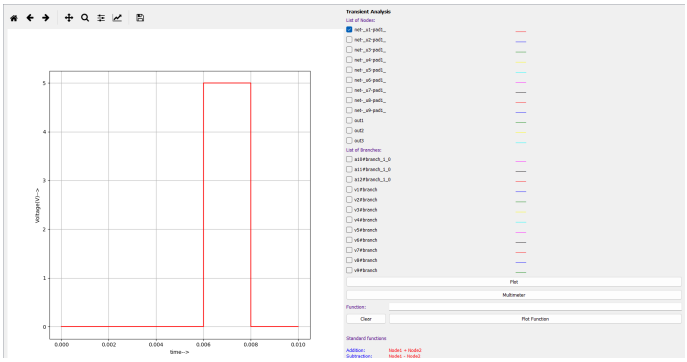

Figure 4.5: Input Waveform of 74HC27

The figure shows the input signals applied to the 74HC27 IC.

4.1.6 Output Waveform

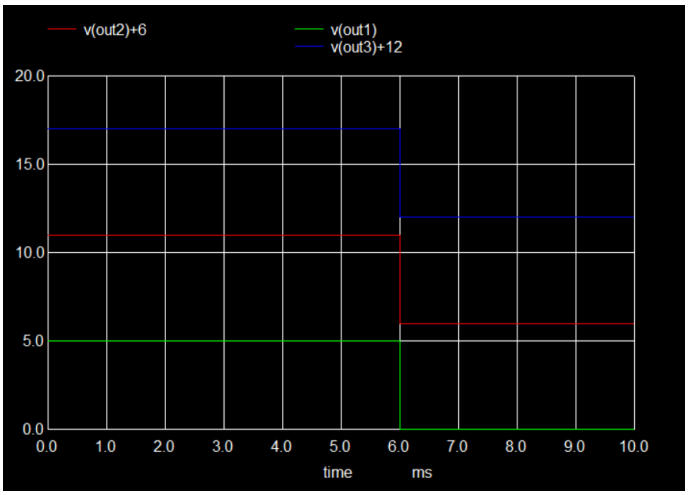

Figure 4.6: Output Waveform of 74HC27

The figure shows the signal produced at the output pin of the 74HC27 IC after processing the input signals. This waveform represents the NOR logic operation performed by the IC.

4.2 74HC30

The 74HC30 is an 8-input AND gate IC, designed for digital logic applications requiring a single output based on the AND operation of eight input signals. It is widely used in control systems, data processing, and logic circuits where multiple conditions must be met simultaneously. Its high-speed performance and robust design make it suitable for complex logic implementations.

4.2.1 Truth Table

Table 3. Function table

H = HIGH voltage level; L = LOW voltage level; X = don't care.

Input								Output
A	B	C	D	E	F	G	H	Y
L	X	X	X	X	X	X	X	H
X	L	X	X	X	X	X	X	H
X	X	L	X	X	X	X	X	H
X	X	X	L	X	X	X	X	H
X	X	X	X	L	X	X	X	H
X	X	X	X	X	L	X	X	H
X	X	X	X	X	X	L	X	H
X	X	X	X	X	X	X	L	H
H	H	H	H	H	H	H	H	L

Figure 4.7: Truth Table of 74HC30

The figure shows the truth table for the 74HC30 IC, detailing the output for all possible combinations of the eight input signals.

4.2.2 Pin Diagram

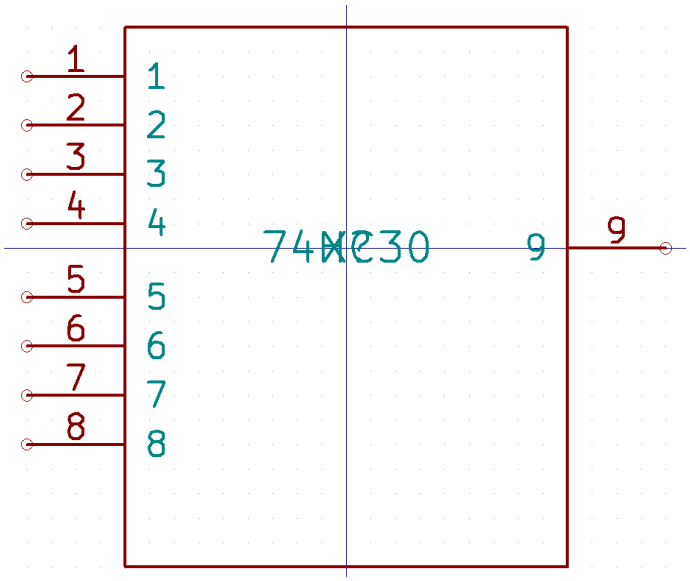

Figure 4.8: Pin Diagram of 74HC30

The figure shows the physical representation of the 74HC30 IC, indicating the arrangement of its eight input pins, a single output pin, a power supply pin, and a ground pin. The pin diagram is essential for correctly integrating the IC into a circuit, ensuring proper connections and functionality in digital applications.

4.2.3 Sub Circuit Layout

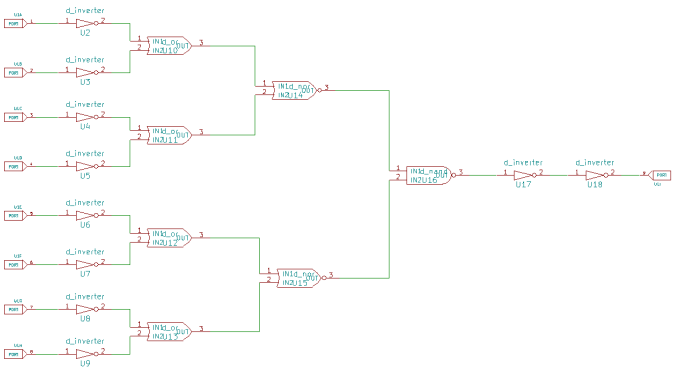

Figure 4.9: Sub Circuit Layout of 74HC30

The figure represents the internal design of the 74HC30 IC, showing how the eight inputs are combined through AND gates to produce a single output. This layout determines how the IC processes input signals to generate the required AND operation. Understanding the sub-circuit helps in optimizing circuit performance and ensuring efficient logic operation.

4.2.4 Test Circuit

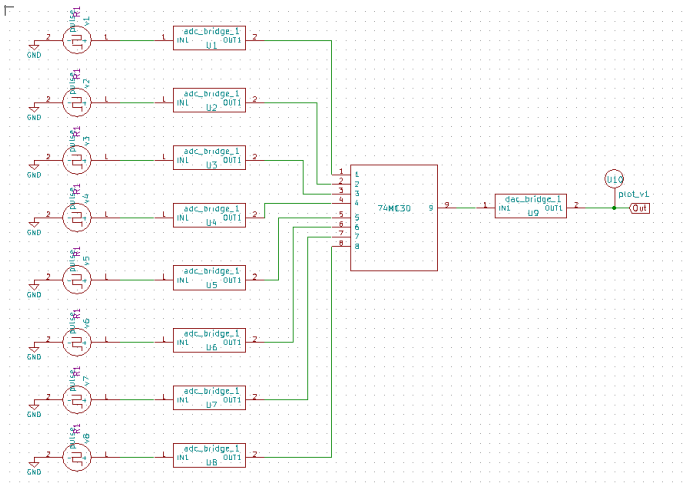

Figure 4.10: Test Circuit of 74HC30

The figure illustrates a test setup used to verify the performance of the 74HC30 IC. A test circuit includes a power source, input signal generators for all eight inputs, and output monitoring devices such as oscilloscopes or logic analyzers. This setup helps evaluate response time, signal integrity, and overall functionality under different conditions.

4.2.5 Input Waveform

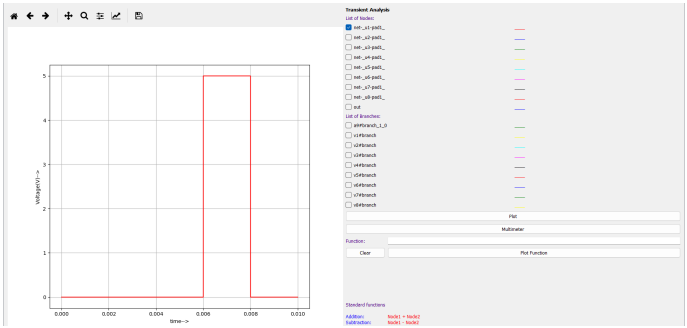

Figure 4.11: Input Waveform of 74HC30

The figure shows the input signals applied to the 74HC30 IC.

4.2.6 Output Waveform

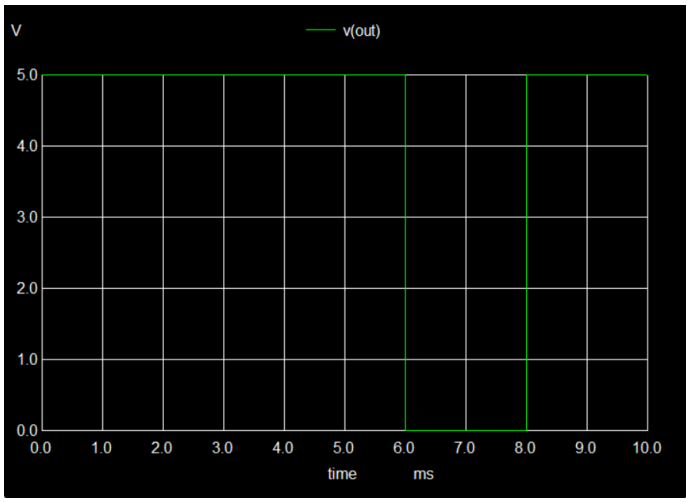

Figure 4.12: Output Waveform of 74HC30

The figure shows the signal produced at the output pin of the 74HC30 IC after processing the eight input signals. This waveform represents the AND logic operation performed by the IC.

4.3 74HC32

The 74HC32 is a quad 2-input OR gate IC, designed for digital logic applications requiring multiple OR operations. It is commonly used in control systems, data processing, and arithmetic circuits where the output is true if at least one input is true. Its high-speed performance and compact design make it an efficient choice for modern logic implementations.

4.3.1 Truth Table

Table 3. Function table

H = HIGH voltage level; L = LOW voltage level; X = don't care.

Input		Output
nA	nB	nY
L	L	L
L	H	H
H	L	H
H	H	H

Figure 4.13: Truth Table of 74HC32

The figure shows the truth table for the 74HC32 IC, detailing the output for all possible combinations of the two input signals for each of the four gates.

4.3.2 Pin Diagram

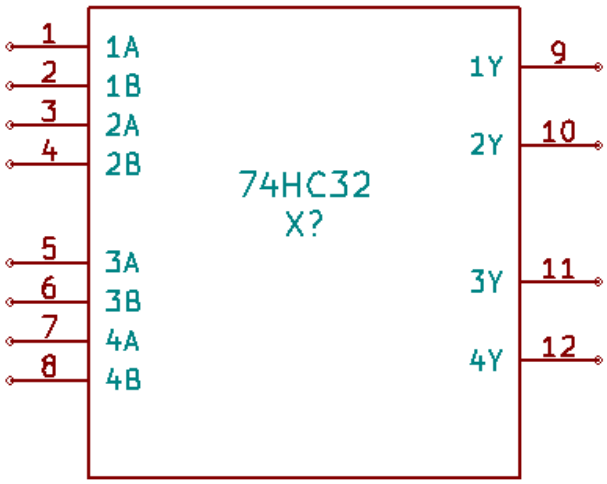

Figure 4.14: Pin Diagram of 74HC32

The figure shows the physical representation of the 74HC32 IC, indicating the arrangement of its eight input pins (two per gate), four output pins, a power supply pin, and a ground pin. The pin diagram is essential for correctly integrating the IC into a circuit, ensuring proper connections and functionality in digital applications.

4.3.3 Sub Circuit Layout

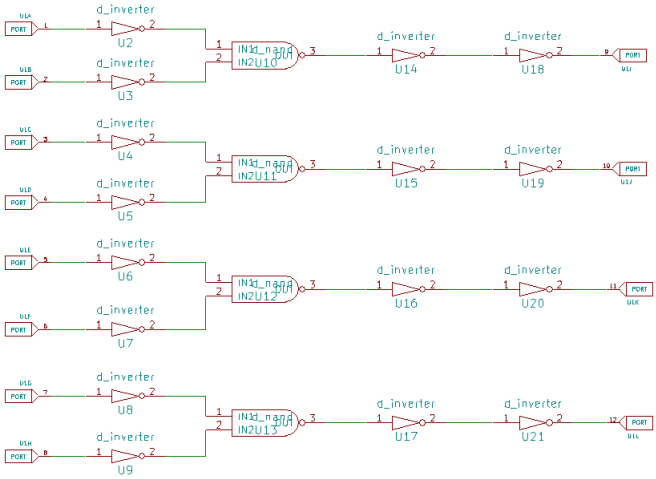

Figure 4.15: Sub Circuit Layout of 74HC32

The figure represents the internal design of the 74HC32 IC, showing how the four pairs of inputs are combined through OR gates to produce four outputs. This layout determines how the IC processes input signals to generate the required OR operation. Understanding the sub-circuit helps in optimizing circuit performance and ensuring efficient logic operation.

4.3.4 Test Circuit

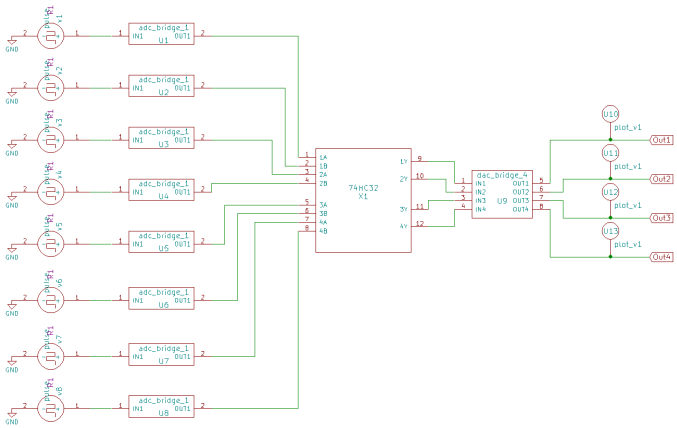

Figure 4.16: Test Circuit of 74HC32

The figure illustrates a test setup used to verify the performance of the 74HC32 IC. A test circuit includes a power source, input signal generators for all eight inputs, and output monitoring devices such as oscilloscopes or logic analyzers. This setup helps evaluate response time, signal integrity, and overall functionality under different conditions.

4.3.5 Input Waveform

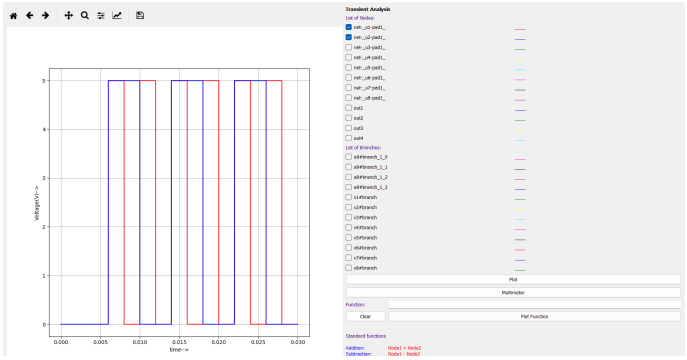

Figure 4.17: Input Waveform of 74HC32

The figure shows the input signals applied to the 74HC32 IC.

4.3.6 Output Waveform

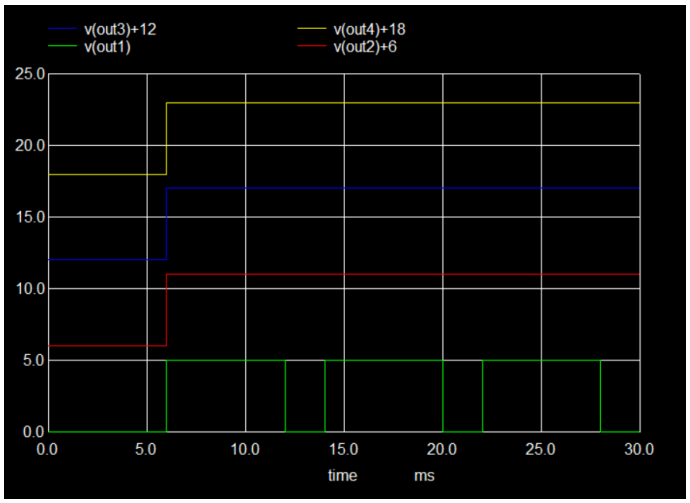

Figure 4.18: Output Waveform of 74HC32

The figure shows the signals produced at the four output pins of the 74HC32 IC after processing the input signals. This waveform represents the OR logic operation performed by the IC.

4.4 74HC266

The 74HC266 is a quad 2-input XNOR gate IC, designed for digital logic applications requiring the exclusive NOR operation. It produces a high output when the number of high inputs is even, making it useful for parity checking, data comparison, and control systems. Its high-speed performance and compact design make it suitable for efficient logic implementations.

4.4.1 Truth Table

Table 8-1. Function Table

INPUTS		OUTPUT
A	B	Y
L	L	Z
L	H	L
H	L	L
H	H	Z

Figure 4.19: Truth Table of 74HC266

The figure shows the truth table for the 74HC266 IC, detailing the output for all possible combinations of the two input signals for each of the four gates.

4.4.2 Pin Diagram

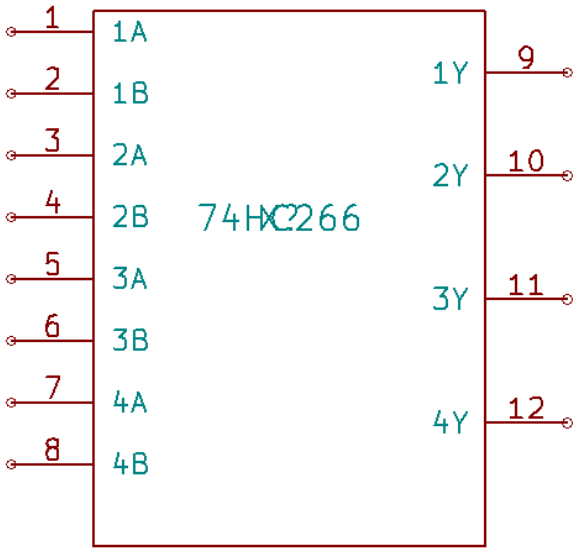

Figure 4.20: Pin Diagram of 74HC266

The figure shows the physical representation of the 74HC266 IC, indicating the arrangement of its eight input pins (two per gate), four output pins, a power supply pin, and a ground pin. The pin diagram is essential for correctly integrating the IC into a circuit, ensuring proper connections and functionality in digital applications.

4.4.3 Sub Circuit Layout

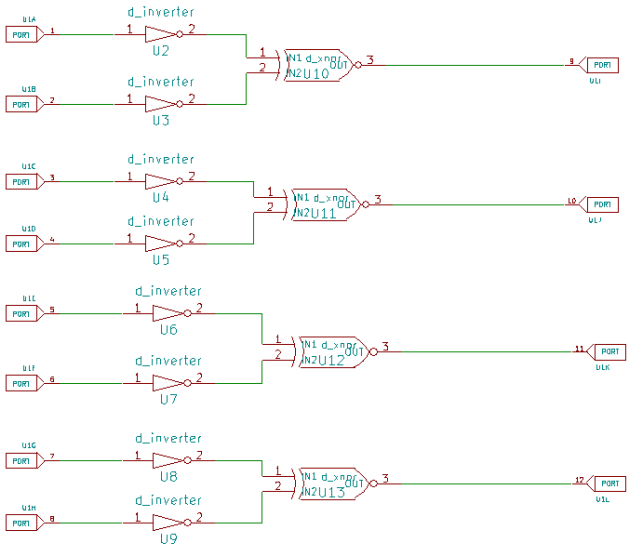

Figure 4.21: Sub Circuit Layout of 74HC266

The figure represents the internal design of the 74HC266 IC, showing how the four pairs of inputs are combined through XNOR gates to produce four outputs. This layout determines how the IC processes input signals to generate the required XNOR operation. Understanding the sub-circuit helps in optimizing circuit performance and ensuring efficient logic operation.

4.4.4 Test Circuit

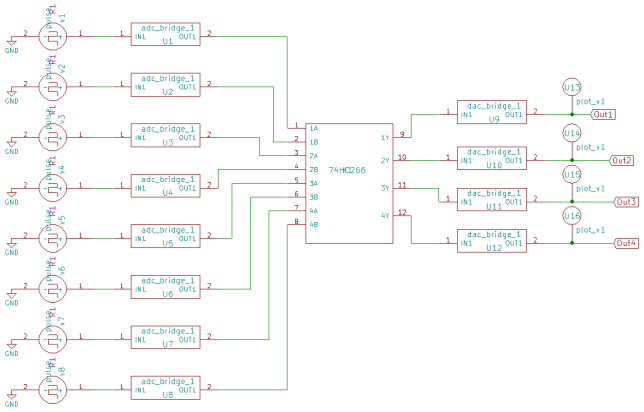

Figure 4.22: Test Circuit of 74HC266

The figure illustrates a test setup used to verify the performance of the 74HC266 IC. A test circuit includes a power source, input signal generators for all eight inputs, and output monitoring devices such as oscilloscopes or logic analyzers. This setup helps evaluate response time, signal integrity, and overall functionality under different conditions.

4.4.5 Input Waveform

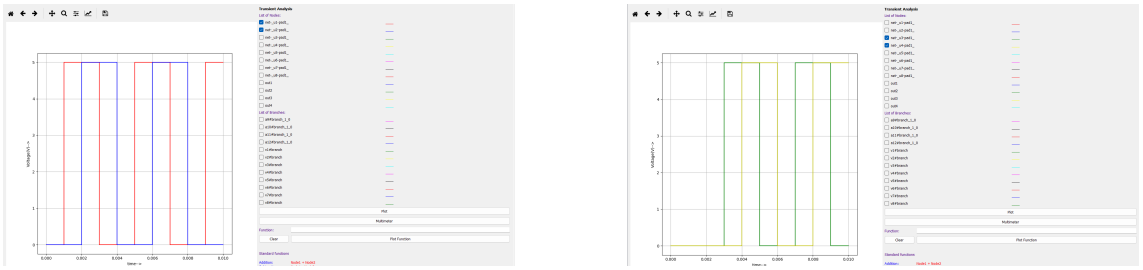

Figure 4.23: Input Waveform of 74HC266

The figure shows the input signals applied to the 74HC266 IC.

4.4.6 Output Waveform

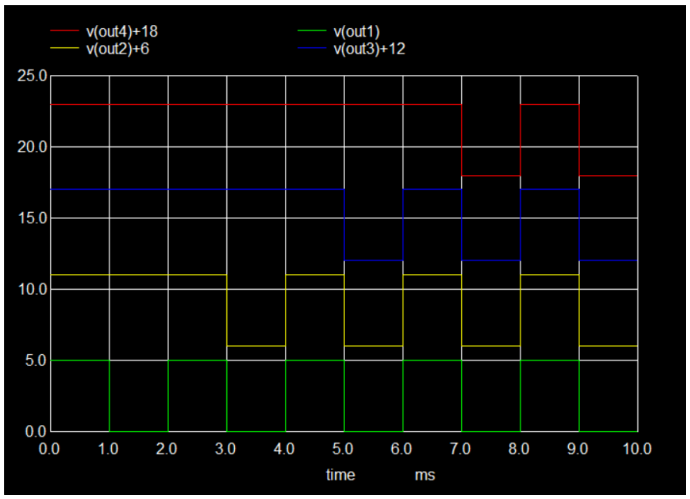

Figure 4.24: Output Waveform of 74HC266

The figure shows the signals produced at the four output pins of the 74HC266 IC after processing the input signals. This waveform represents the XNOR logic operation performed by the IC.

4.5 CD4068B

The CD4068B is an 8-input AND gate IC, designed for digital logic applications requiring a single output based on the AND operation of eight input signals. It is commonly used in control systems, data processing, and logic circuits where all input conditions must be met to produce a high output. Its robust design and versatility make it suitable for a wide range of logic implementations.

4.5.1 Truth Table

DATA INPUTS								DATA OUTPUTS	
A	B	C	D	E	F	G	H	J	K
0	X	X	X	X	X	X	X	1	0
X	0	X	X	X	X	X	X	1	0
X	X	0	X	X	X	X	X	1	0
X	X	X	0	X	X	X	X	1	0
X	X	X	X	0	X	X	X	1	0
X	X	X	X	X	0	X	X	1	0
X	X	X	X	X	X	0	X	1	0
X	X	X	X	X	X	X	0	1	0
1	1	1	1	1	1	1	1	0	1

Figure 4.25: Truth Table of CD4068B

The figure shows the truth table for the CD4068B IC, detailing the output for all possible combinations of the eight input signals.

4.5.2 Pin Diagram

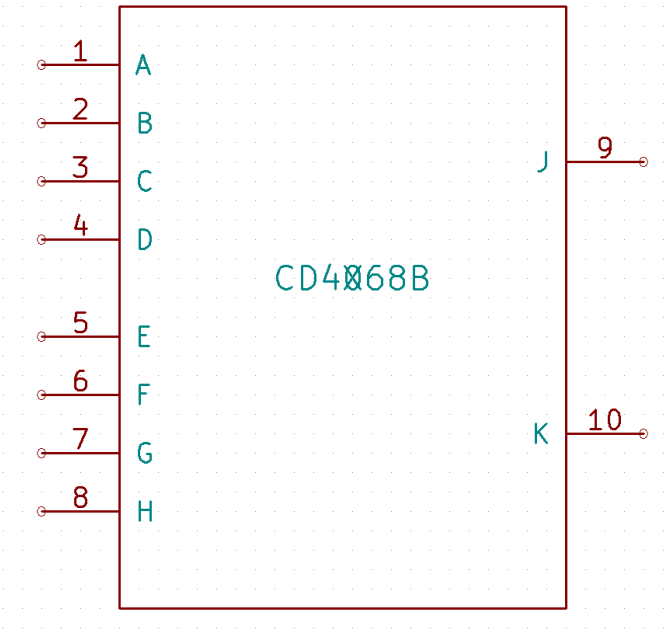

Figure 4.26: Pin Diagram of CD4068B

The figure shows the physical representation of the CD4068B IC, indicating the arrangement of its eight input pins, a single output pin, a power supply pin, and a ground pin. The pin diagram is essential for correctly integrating the IC into a circuit, ensuring proper connections and functionality in digital applications.

4.5.3 Sub Circuit Layout

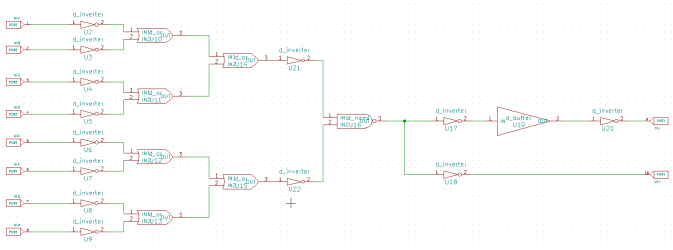

Figure 4.27: Sub Circuit Layout of CD4068B

The figure represents the internal design of the CD4068B IC, showing how the eight inputs are combined through AND gates to produce a single output. This

layout determines how the IC processes input signals to generate the required AND operation. Understanding the sub-circuit helps in optimizing circuit performance and ensuring efficient logic operation.

4.5.4 Test Circuit

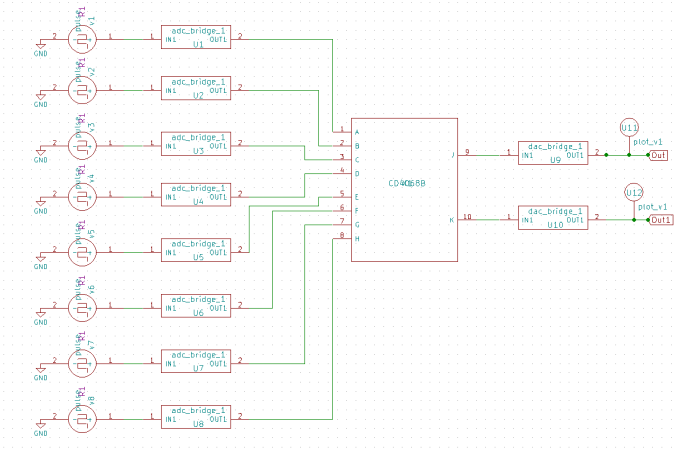

Figure 4.28: Test Circuit of CD4068B

The figure illustrates a test setup used to verify the performance of the CD4068B IC. A test circuit includes a power source, input signal generators for all eight inputs, and output monitoring devices such as oscilloscopes or logic analyzers. This setup helps evaluate response time, signal integrity, and overall functionality under different conditions.

4.5.5 Input Waveform

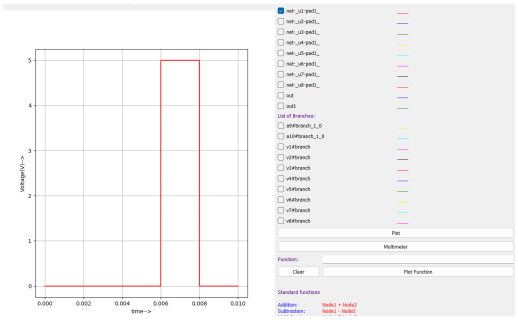

Figure 4.29: Input Waveform of CD4068B

The figure shows the input signals applied to the CD4068B IC.

4.5.6 Output Waveform

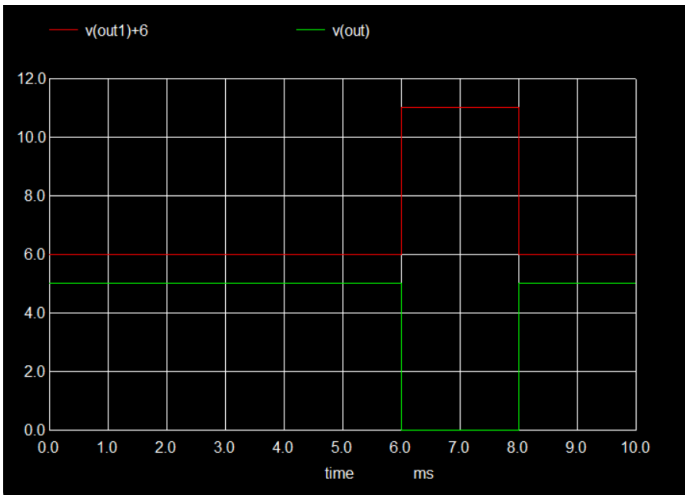

Figure 4.30: Output Waveform of CD4068B

The figure shows the signal produced at the output pin of the CD4068B IC after processing the eight input signals. This waveform represents the AND logic operation performed by the IC.

4.6 CD4082B

The CD4082B is a dual 4-input AND gate IC, designed for digital logic applications where two independent AND operations with four inputs each are required. It is commonly used in control systems, data processing, and logic circuits where multiple conditions must be simultaneously satisfied to produce a high output. Its reliable performance and dual-gate configuration make it a versatile component for complex logic designs.

4.6.1 Truth Table

4 Input AND gate				
A	B	C	D	A.B.C.D
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	0
0	1	0	1	0
0	1	1	0	0
0	1	1	1	0
1	0	0	0	0
1	0	0	1	0
1	0	1	0	0
1	0	1	1	0
1	1	0	0	0
1	1	0	1	0
1	1	1	0	0
1	1	1	1	1

Figure 4.31: Truth Table of CD4082B

The figure shows the truth table for the CD4082B IC, detailing the output for all possible combinations of the four input signals for each of the two gates.

4.6.2 Pin Diagram

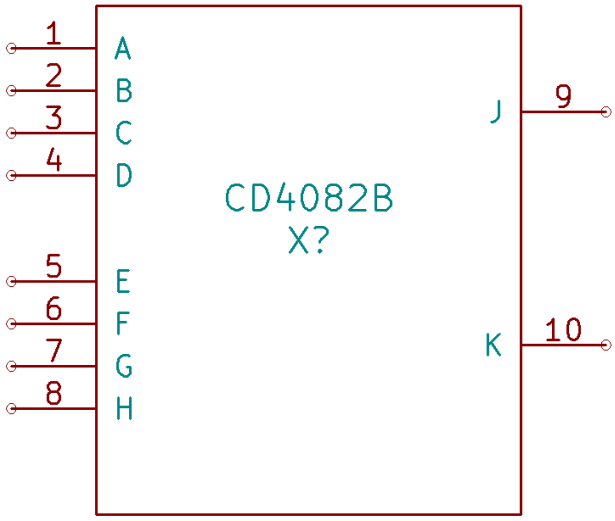

Figure 4.32: Pin Diagram of CD4082B

The figure shows the physical representation of the CD4082B IC, indicating the arrangement of its eight input pins (four per gate), two output pins, a power supply pin, and a ground pin. The pin diagram is essential for correctly integrating the IC into a circuit, ensuring proper connections and functionality in digital applications.

4.6.3 Sub Circuit Layout

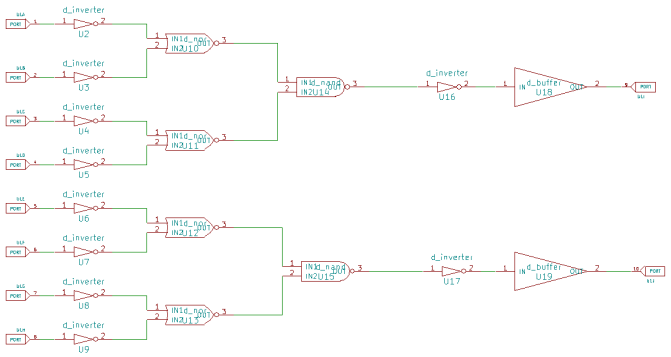

Figure 4.33: Sub Circuit Layout of CD4082B

The figure represents the internal design of the CD4082B IC, showing how the two sets of four inputs are combined through AND gates to produce two outputs. This layout determines how the IC processes input signals to generate the required AND

operation. Understanding the sub-circuit helps in optimizing circuit performance and ensuring efficient logic operation.

4.6.4 Test Circuit

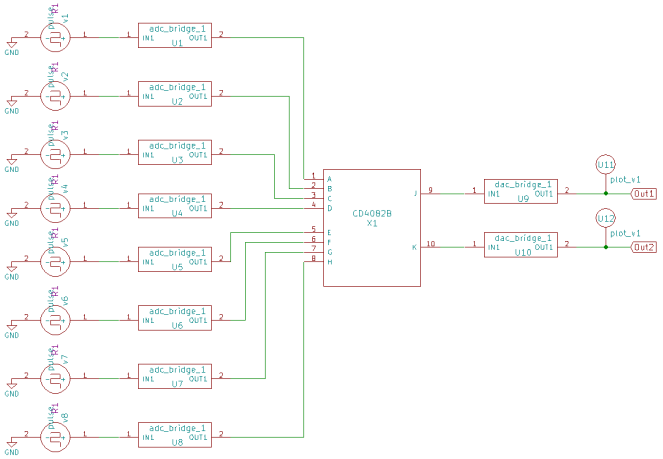

Figure 4.34: Test Circuit of CD4082B

The figure illustrates a test setup used to verify the performance of the CD4082B IC. A test circuit includes a power source, input signal generators for all eight inputs, and output monitoring devices such as oscilloscopes or logic analyzers. This setup helps evaluate response time, signal integrity, and overall functionality under different conditions.

4.6.5 Input Waveform

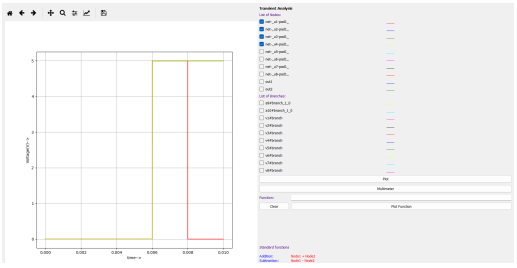

Figure 4.35: Input Waveform of CD4082B

The figure shows the input signals applied to the CD4082B IC.

4.6.6 Output Waveform

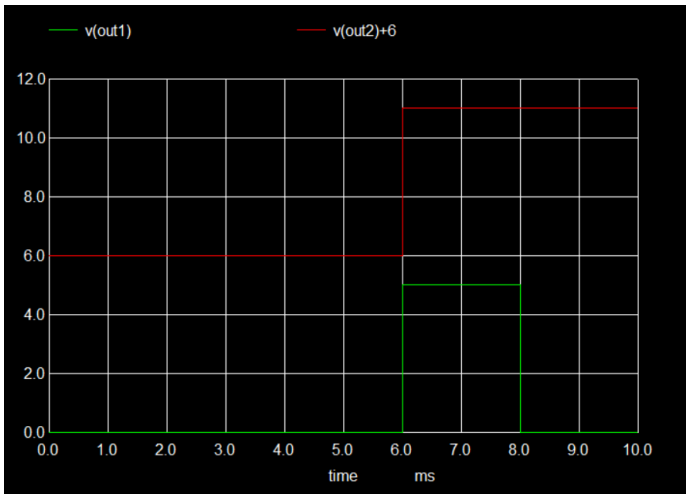

Figure 4.36: Output Waveform of CD4082B

The figure shows the signals produced at the two output pins of the CD4082B IC after processing the input signals. This waveform represents the AND logic operation performed by the IC.

4.7 74HC21

The 74HC21 is a dual 4-input AND gate IC, designed for digital logic applications requiring two independent AND operations with four inputs each. It is widely used in control systems, data processing, and logic circuits where all four inputs per gate must be high to produce a high output. Its high-speed performance and dual-gate design make it suitable for efficient and compact logic implementations.

4.7.1 Truth Table

Table 3. Function table

H = HIGH voltage level; L = LOW voltage level; X = don't care.

Input				Output
nA	nB	nC	nD	nY
L	X	X	X	L
X	L	X	X	L
X	X	L	X	L
X	X	X	L	L
H	H	H	H	H

Figure 4.37: Truth Table of 74HC21

The figure shows the truth table for the 74HC21 IC, detailing the output for all possible combinations of the four input signals for each of the two gates.

4.7.2 Pin Diagram

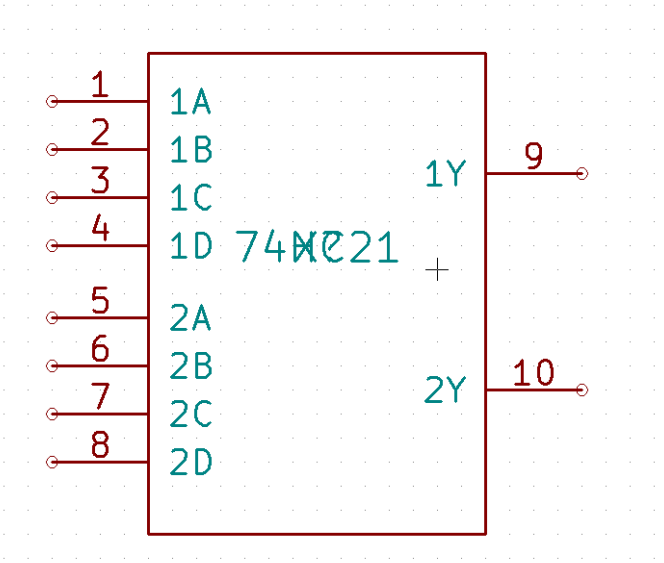

Figure 4.38: Pin Diagram of 74HC21

The figure shows the physical representation of the 74HC21 IC, indicating the arrangement of its eight input pins (four per gate), two output pins, a power supply pin, and a ground pin. The pin diagram is essential for correctly integrating the IC into a circuit, ensuring proper connections and functionality in digital applications.

4.7.3 Sub Circuit Layout

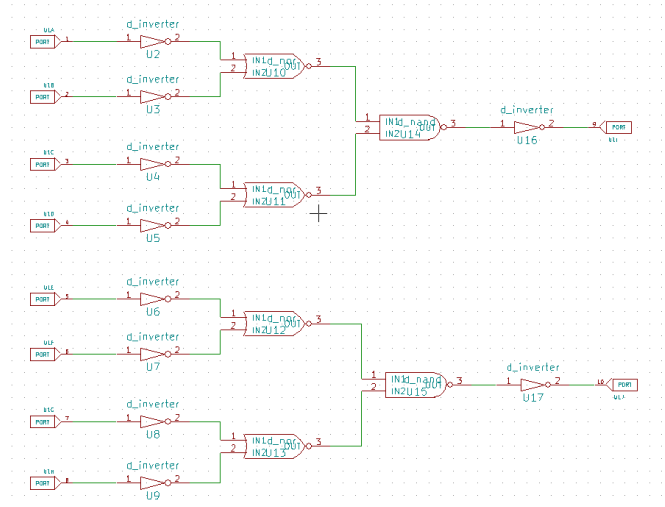

Figure 4.39: Sub Circuit Layout of 74HC21

The figure represents the internal design of the 74HC21 IC, showing how the two sets of four inputs are combined through AND gates to produce two outputs. This layout determines how the IC processes input signals to generate the required AND operation. Understanding the sub-circuit helps in optimizing circuit performance and ensuring efficient logic operation.

4.7.4 Test Circuit

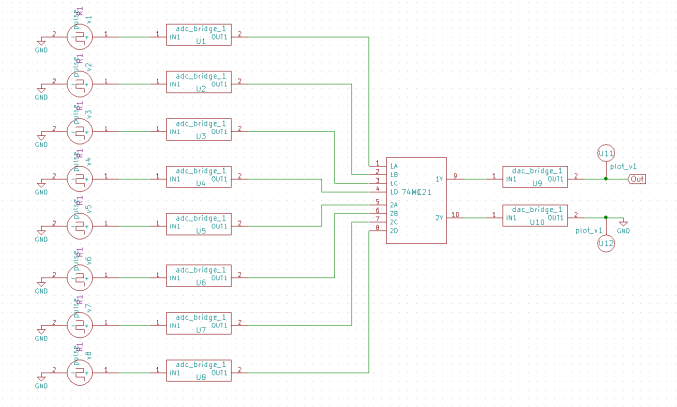

Figure 4.40: Test Circuit of 74HC21

The figure illustrates a test setup used to verify the performance of the 74HC21 IC. A test circuit includes a power source, input signal generators for all eight inputs, and output monitoring devices such as oscilloscopes or logic analyzers. This setup helps evaluate response time, signal integrity, and overall functionality under different conditions.

4.7.5 Input Waveform

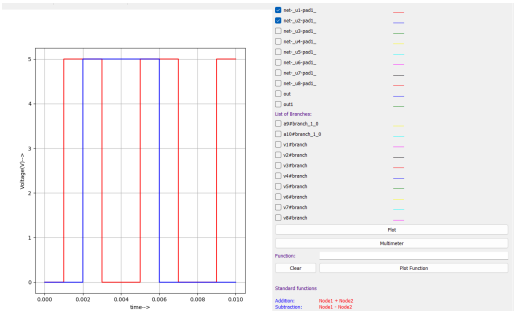

Figure 4.41: Input Waveform of 74HC21

The figure shows the input signals applied to the 74HC21 IC.

4.7.6 Output Waveform

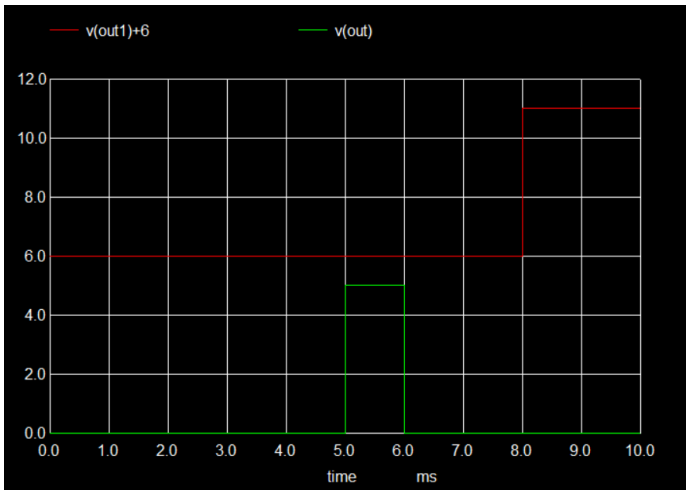

Figure 4.42: Output Waveform of 74HC21

The figure shows the signals produced at the two output pins of the 74HC21 IC after processing the input signals. This waveform represents the AND logic operation performed by the IC.

4.8 74HC4072

The 74HC4072 is a dual 4-input OR gate IC, designed for digital logic applications requiring two independent OR operations with four inputs each. It is commonly used in control systems, data processing, and logic circuits where the output is high if at least one of the four inputs per gate is high. Its high-speed performance and dual-gate design make it suitable for efficient and versatile logic implementations.

4.8.1 Truth Table

TRUTH TABLE

A	B	C	D	Y
L	L	L	L	L
H	X	X	X	H
X	H	X	X	H
X	X	H	X	H
X	X	X	H	H

Figure 4.43: Truth Table of 74HC4072

The figure shows the truth table for the 74HC4072 IC, detailing the output for all possible combinations of the four input signals for each of the two gates.

4.8.2 Pin Diagram

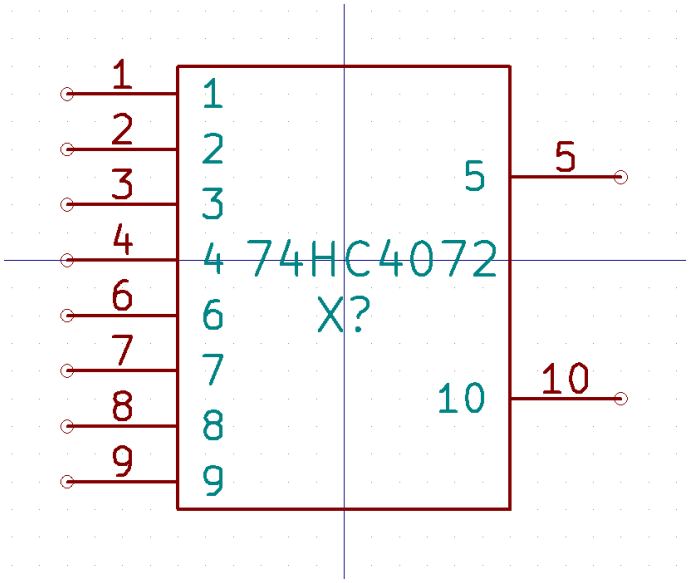

Figure 4.44: Pin Diagram of 74HC4072

The figure shows the physical representation of the 74HC4072 IC, indicating the arrangement of its eight input pins (four per gate), two output pins, a power supply pin, and a ground pin. The pin diagram is essential for correctly integrating the IC into a circuit, ensuring proper connections and functionality in digital applications.

4.8.3 Sub Circuit Layout

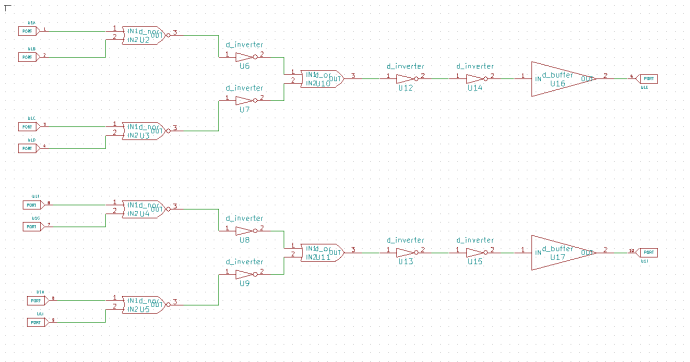

Figure 4.45: Sub Circuit Layout of 74HC4072

The figure represents the internal design of the 74HC4072 IC, showing how the two sets of four inputs are combined through OR gates to produce two outputs. This

layout determines how the IC processes input signals to generate the required OR operation. Understanding the sub-circuit helps in optimizing circuit performance and ensuring efficient logic operation.

4.8.4 Test Circuit

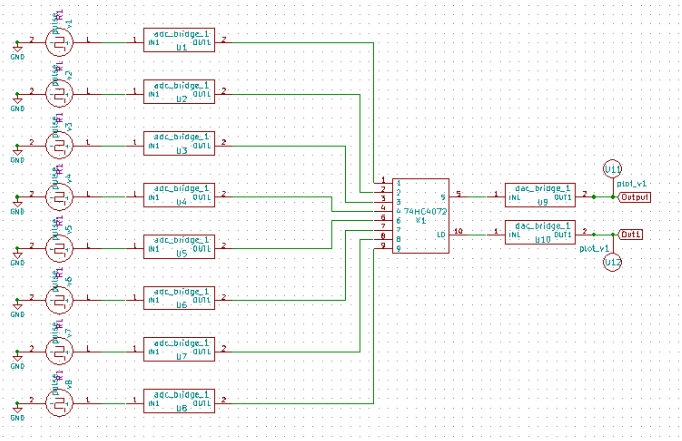

Figure 4.46: Test Circuit of 74HC4072

The figure illustrates a test setup used to verify the performance of the 74HC4072 IC. A test circuit includes a power source, input signal generators for all eight inputs, and output monitoring devices such as oscilloscopes or logic analyzers. This setup helps evaluate response time, signal integrity, and overall functionality under different conditions.

4.8.5 Input Waveform

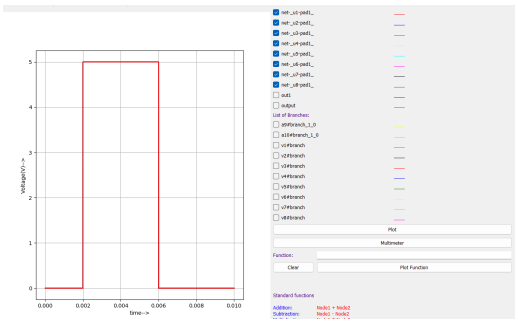

Figure 4.47: Input Waveform of 74HC4072

The figure shows the input signals applied to the 74HC4072 IC.

4.8.6 Output Waveform

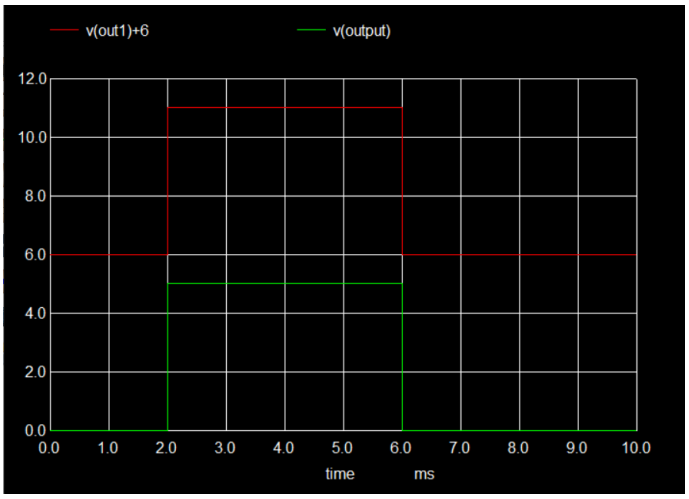

Figure 4.48: Output Waveform of 74HC4072

The figure shows the signals produced at the two output pins of the 74HC4072 IC after processing the input signals. This waveform represents the OR logic operation performed by the IC.

4.9 74HC4075

The 74HC4075 is a triple 3-input OR gate IC, designed for digital logic applications requiring three independent OR operations with three inputs each. It is commonly used in control systems, data processing, and logic circuits where the output is high if at least one of the three inputs per gate is high. Its high-speed performance and triple-gate design make it suitable for efficient and versatile logic implementations.

4.9.1 Truth Table

Inputs			Outputs
nA	nB	nC	nY
L	L	L	L
X	X	H	H
X	H	X	H
H	X	X	H

Figure 4.49: Truth Table of 74HC4075

The figure shows the truth table for the 74HC4075 IC, detailing the output for all possible combinations of the three input signals for each of the three gates.

4.9.2 Pin Diagram

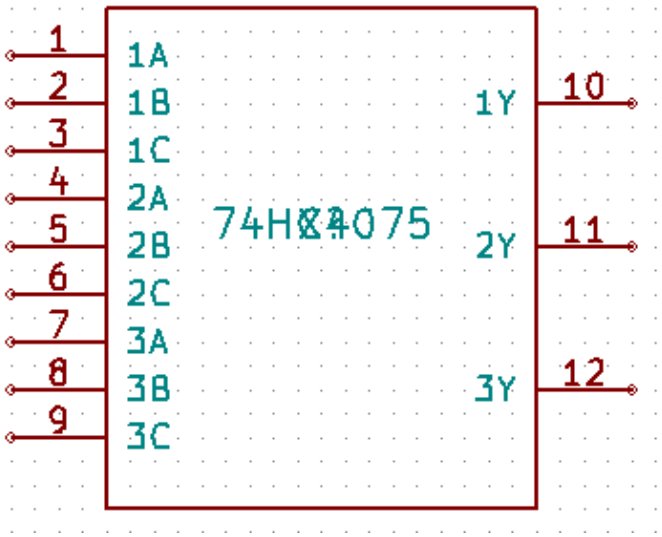

Figure 4.50: Pin Diagram of 74HC4075

The figure shows the physical representation of the 74HC4075 IC, indicating the arrangement of its nine input pins (three per gate), three output pins, a power supply pin, and a ground pin. The pin diagram is essential for correctly integrating the IC into a circuit, ensuring proper connections and functionality in digital applications.

4.9.3 Sub Circuit Layout

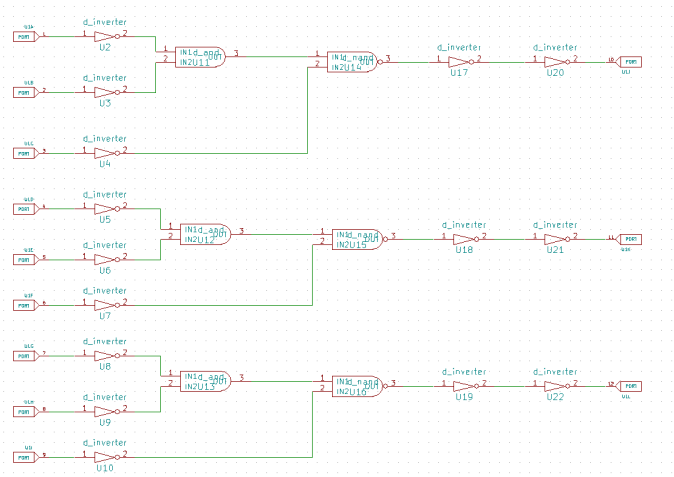

Figure 4.51: Sub Circuit Layout of 74HC4075

The figure represents the internal design of the 74HC4075 IC, showing how the three sets of three inputs are combined through OR gates to produce three outputs. This

layout determines how the IC processes input signals to generate the required OR operation. Understanding the sub-circuit helps in optimizing circuit performance and ensuring efficient logic operation.

4.9.4 Test Circuit

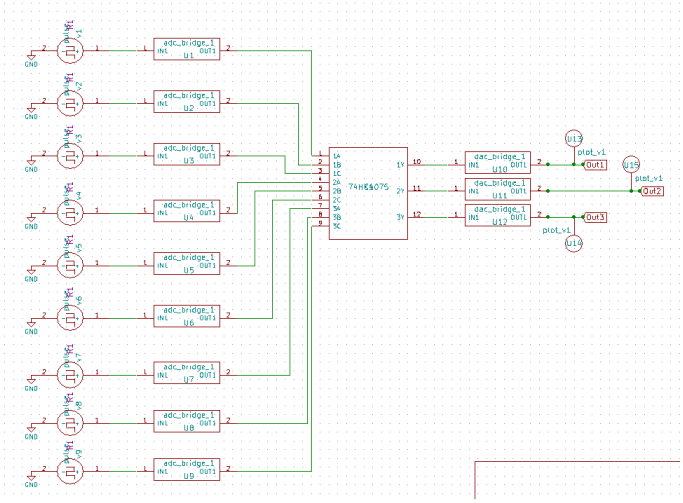

Figure 4.52: Test Circuit of 74HC4075

The figure illustrates a test setup used to verify the performance of the 74HC4075 IC. A test circuit includes a power source, input signal generators for all nine inputs, and output monitoring devices such as oscilloscopes or logic analyzers. This setup helps evaluate response time, signal integrity, and overall functionality under different conditions.

4.9.5 Input Waveform

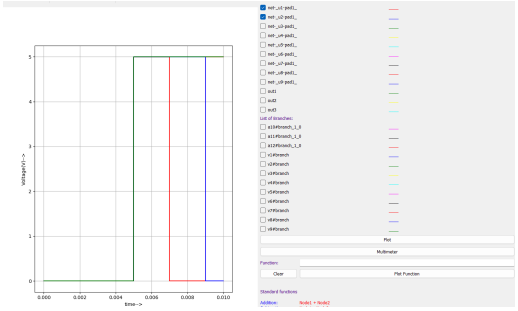

Figure 4.53: Input Waveform of 74HC4075

The figure shows the input signals applied to the 74HC4075 IC.

4.9.6 Output Waveform

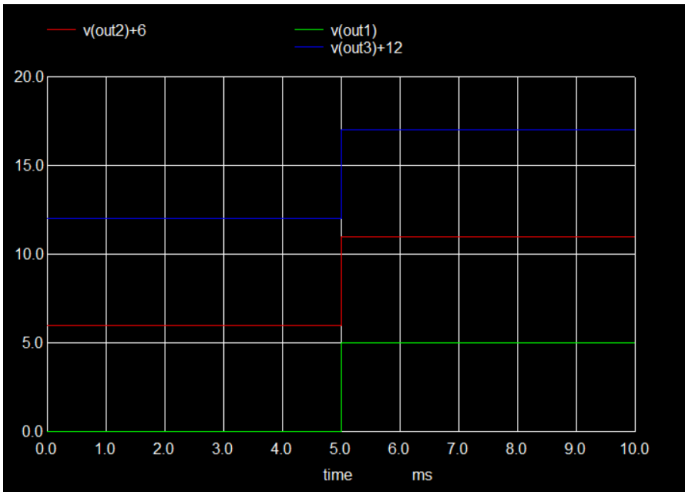

Figure 4.54: Output Waveform of 74HC4075

The figure shows the signals produced at the three output pins of the 74HC4075 IC after processing the input signals. This waveform represents the OR logic operation performed by the IC.

4.10 74HC4078

The 74HC4078 is a triple 3-input NOR gate IC, designed for digital logic applications requiring three independent NOR operations with three inputs each. It produces a high output only when all three inputs are low, making it useful in control systems, data processing, and logic circuits where the absence of high inputs is critical. Its high-speed performance and triple-gate configuration make it an efficient choice for complex logic designs.

4.10.1 Truth Table

TRUTH TABLE

INPUTS	OUTPUTS	
	X	Y
ALL INPUTS "L"	H	L
OTHER POSSIBILITIES	L	H

Figure 4.55: Truth Table of 74HC4078

The figure shows the truth table for the 74HC4078 IC, detailing the output for all possible combinations of the three input signals for each of the three gates.

4.10.2 Pin Diagram

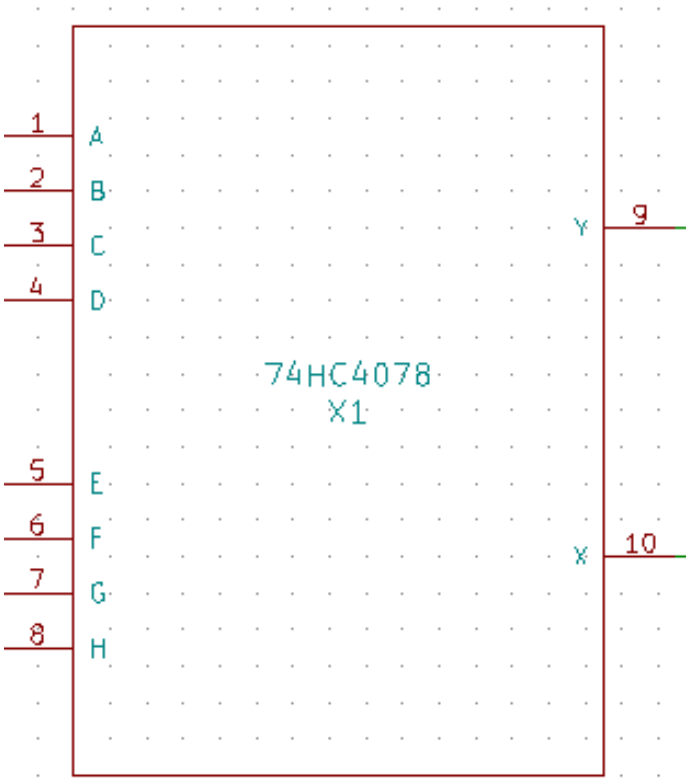

Figure 4.56: Pin Diagram of 74HC4078

The figure shows the physical representation of the 74HC4078 IC, indicating the arrangement of its nine input pins (three per gate), three output pins, a power supply pin, and a ground pin. The pin diagram is essential for correctly integrating the IC into a circuit, ensuring proper connections and functionality in digital applications.

4.10.3 Sub Circuit Layout

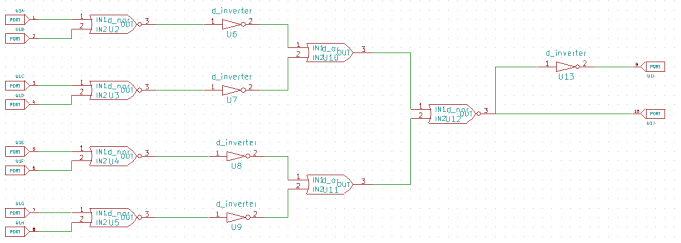

Figure 4.57: Sub Circuit Layout of 74HC4078

The figure represents the internal design of the 74HC4078 IC, showing how the three sets of three inputs are combined through NOR gates to produce three outputs. This

layout determines how the IC processes input signals to generate the required NOR operation. Understanding the sub-circuit helps in optimizing circuit performance and ensuring efficient logic operation.

4.10.4 Test Circuit

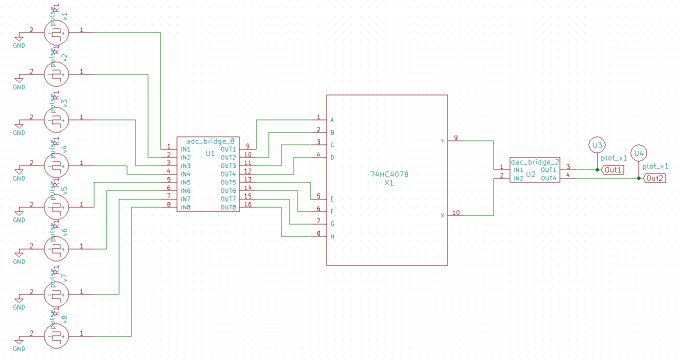

Figure 4.58: Test Circuit of 74HC4078

The figure illustrates a test setup used to verify the performance of the 74HC4078 IC. A test circuit includes a power source, input signal generators for all nine inputs, and output monitoring devices such as oscilloscopes or logic analyzers. This setup helps evaluate response time, signal integrity, and overall functionality under different conditions.

4.10.5 Input Waveform

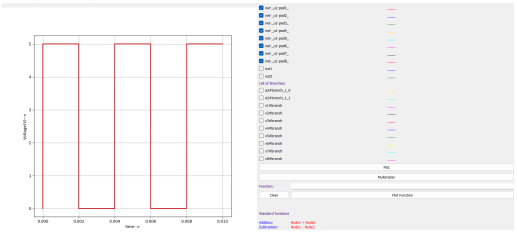

Figure 4.59: Input Waveform of 74HC4078

The figure shows the input signals applied to the 74HC4078 IC.

4.10.6 Output Waveform

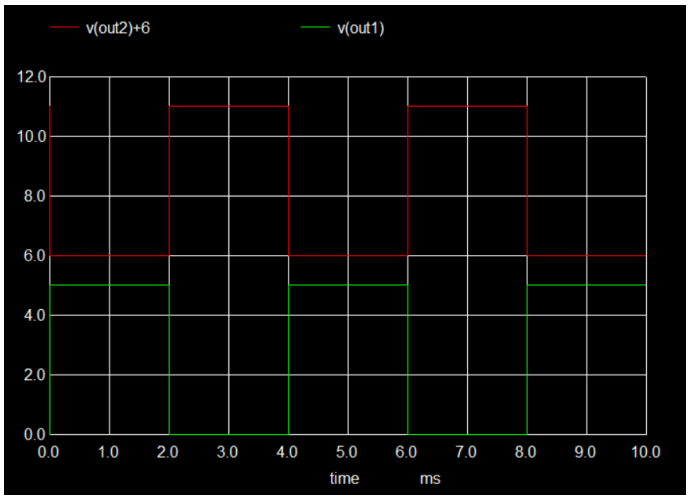

Figure 4.60: Output Waveform of 74HC4078

The figure shows the signals produced at the three output pins of the 74HC4078 IC after processing the input signals. This waveform represents the NOR logic operation performed by the IC.

4.11 CD4019B

The CD4019B is a quad 2-input AND-OR gate IC, designed for digital logic applications requiring four independent AND-OR logic operations. It combines two 2-input AND gates per OR gate, making it useful in control systems, data processing, and logic circuits where complex combinational logic is needed. Its versatile design and robust performance make it suitable for a variety of logic implementations.

4.11.1 Truth Table

TRUTH TABLE

Ka	Kb	An	Bn	Dn
1	0	1	X	1
1	0	0	X	0
0	1	X	1	1
0	1	X	0	0
0	0	X	X	0
1	1	0	0	0
1	1	0	1	1
1	1	1	0	1
1	1	1	1	1

X = Don't Care

Figure 4.61: Truth Table of CD4019B

The figure shows the truth table for the CD4019B IC, detailing the output for all possible combinations of the two input signals for each of the four AND-OR gate pairs.

4.11.2 Pin Diagram

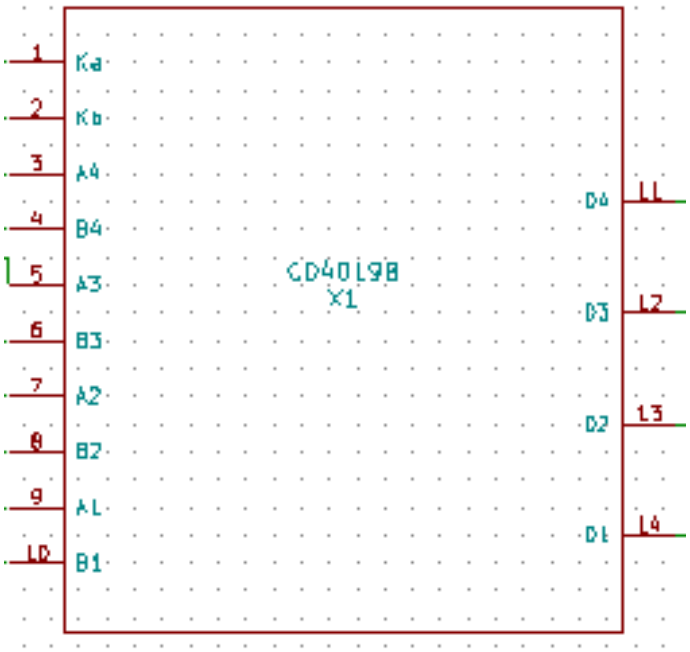

Figure 4.62: Pin Diagram of CD4019B

The figure shows the physical representation of the CD4019B IC, indicating the arrangement of its eight input pins (two per AND gate), four output pins (one per OR gate), a power supply pin, and a ground pin. The pin diagram is essential for correctly integrating the IC into a circuit, ensuring proper connections and functionality in digital applications.

4.11.3 Sub Circuit Layout

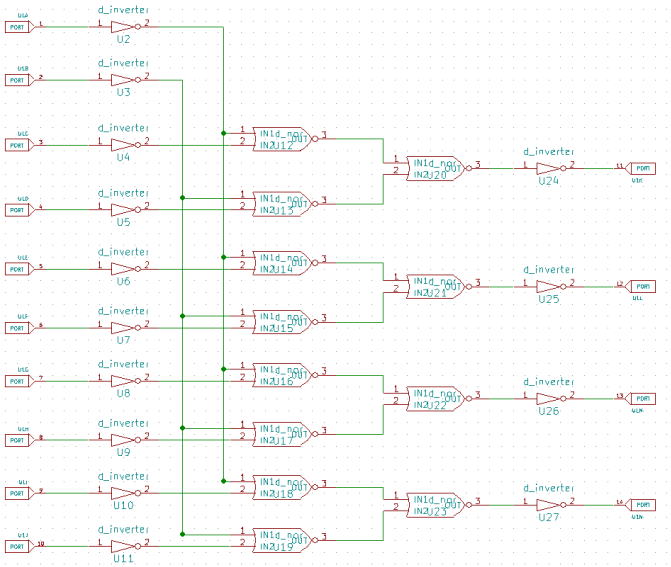

Figure 4.63: Sub Circuit Layout of CD4019B

The figure represents the internal design of the CD4019B IC, showing how the four pairs of two inputs are combined through AND gates and then OR gates to produce four outputs. This layout determines how the IC processes input signals to generate the required AND-OR operation. Understanding the sub-circuit helps in optimizing circuit performance and ensuring efficient logic operation.

4.11.4 Test Circuit

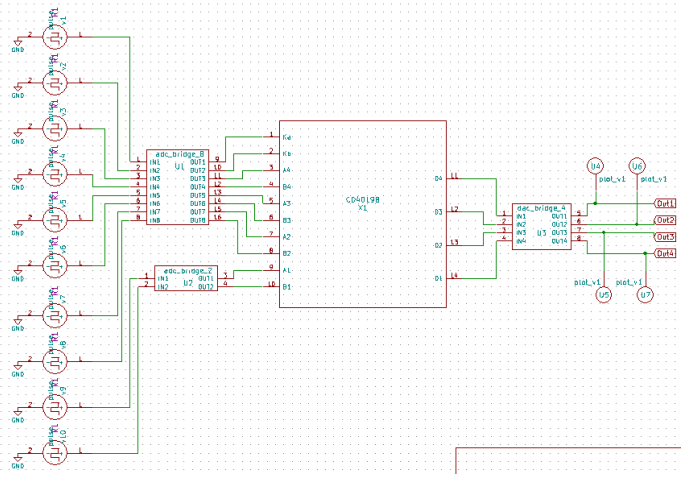

Figure 4.64: Test Circuit of CD4019B

The figure illustrates a test setup used to verify the performance of the CD4019B IC. A test circuit includes a power source, input signal generators for all eight inputs, and output monitoring devices such as oscilloscopes or logic analyzers. This setup helps evaluate response time, signal integrity, and overall functionality under different conditions.

4.11.5 Input Waveform

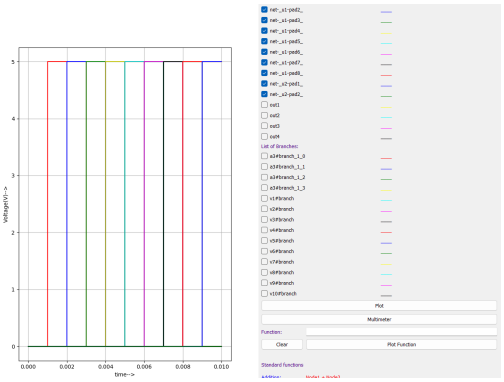

Figure 4.65: Input Waveform of CD4019B

The figure shows the input signals applied to the CD4019B IC.

4.11.6 Output Waveform

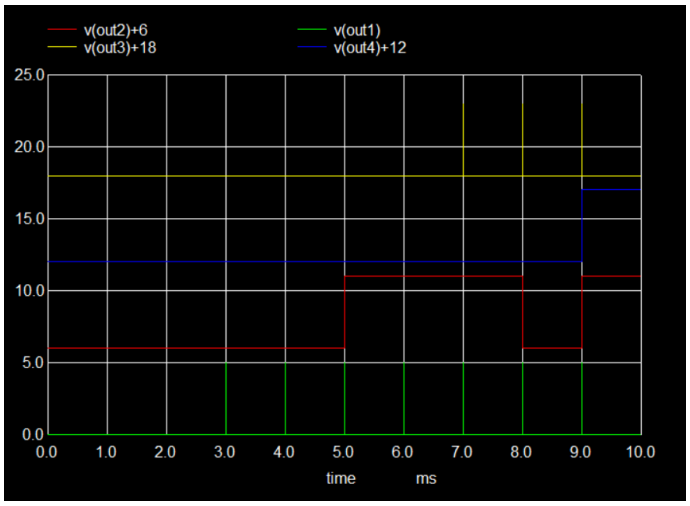

Figure 4.66: Output Waveform of CD4019B

The figure shows the signals produced at the four output pins of the CD4019B IC after processing the input signals. This waveform represents the AND-OR logic operation performed by the IC.

Chapter 5

16-Bit ALU Design

5.1 Verilog Code

The following Verilog code implements a 16-bit Arithmetic Logic Unit (ALU) with various operations.

```
module ALU_16bit(
    input  [15:0] A,
    input  [15:0] B,
    input  [3:0]  opcode,
    output [15:0] out,
    output zero
);

    reg [15:0] result;

    assign out = result;
    assign zero = (result == 16'b0);

    always @(*) begin
        case(opcode)
            4'b0000: result = A + B;
            4'b0001: result = A - B;
            4'b0010: result = A & B;
            4'b0011: result = A | B;
            4'b0100: result = A ^ B;
            4'b0101: result = ~A;
            4'b0110: result = A << 1;
            4'b0111: result = A >> 1;
            4'b1000: result = B << 1;
            4'b1001: result = B >> 1;
            4'b1010: result = A * B;
            4'b1011: result = (B != 0) ? A / B : 16'b0;
            default: result = 16'b0;
        endcase
    end

endmodule
```

Figure 5.1: Verilog Code of 16-bit ALU

5.1.1 Test Circuit

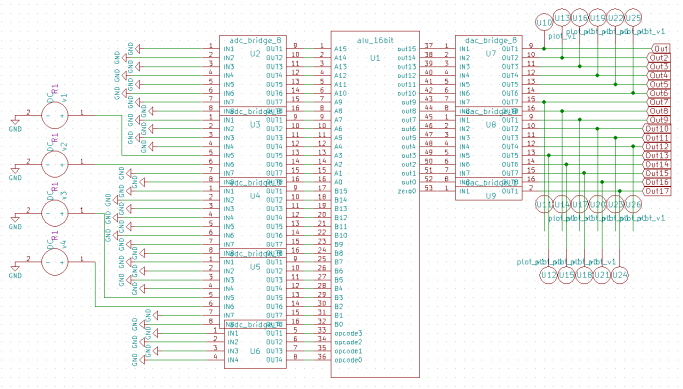

Figure 5.2: Test Circuit of 16-bit ALU

The test circuit for the 16-bit ALU was designed to validate its addition functionality by inputting values 12 and 12, which should yield a result of 24 in decimal. The output is represented in a 16-bit binary format, where the bits correspond to powers of 2. The result of 24 is correctly reflected by the high states of the output bits out12 and out13, representing the $16(2^4)$ and $8(2^3)$ bits respectively. This is confirmed by two separate waveform images for out12 and out13, demonstrating that these specific output bits are active, aligning with the binary representation of 24 (binary 11000, where the 5th and 4th bits from the right are high). This successful test validates the ALU's ability to perform accurate arithmetic operations as intended.

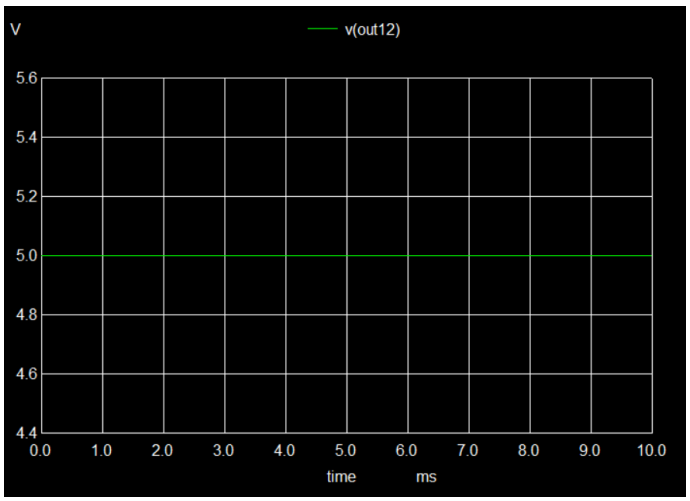

Figure 5.3: Output Waveform of out12 for 16-bit ALU

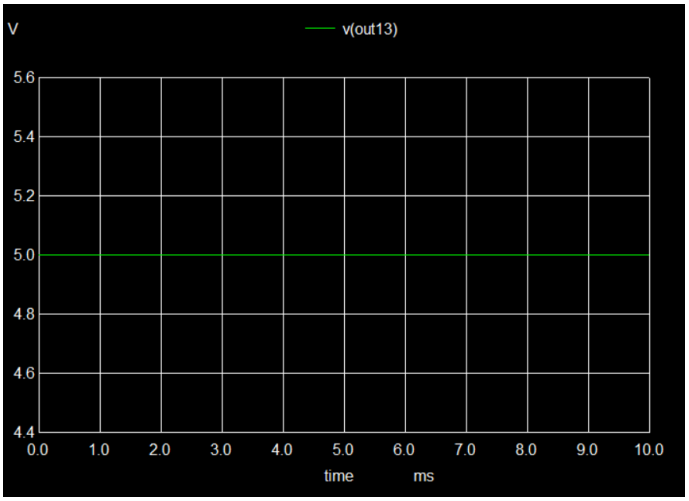

Figure 5.4: Output Waveform of out13 for 16-bit ALU

The figures above display the output waveforms for bits out12 and out13, respectively, confirming the high states that contribute to the result of 24.

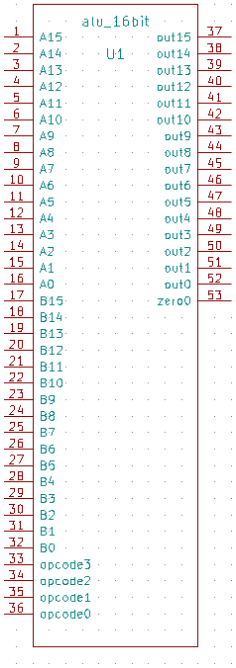

Figure 5.5: Pin Diagram of 16-bit ALU

The figure shows the Pin Diagram of the 16-bit ALU.

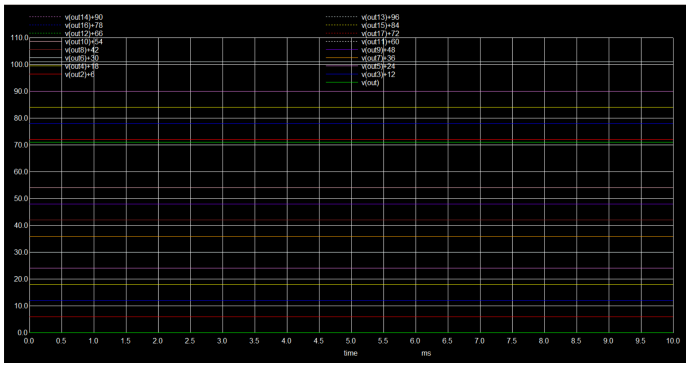

Figure 5.6: Output Waveform of 16-bit ALU

The figure shows the output signals produced by the 16-bit ALU after processing the input signals.

Chapter 6

Conclusion and Future Scope

Developed a range of subcircuits for Digital Integrated Circuits (ICs), strictly following the specifications from their official datasheets. These include essential components like digital ICs. Each IC model was thoroughly tested using appropriate test circuits to ensure accurate performance. These IC models are now ready for integration into eSim's subcircuit library, providing a comprehensive set of building blocks for developers and students to use in a wide array of circuit designs and simulations. With continued development, more such IC models are expected to enhance the library's offerings.

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