Semester Long Internship Report

On

Analog and Digital IC Design in eSim

Submitted by

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Under the guidance of

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Acknowledgment

I would like to express my sincere gratitude to the FOSSEE team at IIT Bombay for providing me with this valuable opportunity to work as a part of the eSim project. Being selected for this fellowship was a moment of pride, and the experience has truly been enriching, both technically and personally.

My heartfelt thanks to **Prof. Kannan M. Moudgalya** for initiating and leading this impactful platform that empowers students like me to explore the world of open-source electronics.

I am especially grateful to **Mr. Sumanto Kar** for his constant guidance, patience, and encouragement throughout the project. From understanding datasheets and research articles to navigating tools like GitHub and effectively using eSim, your support has been instrumental in shaping my learning experience. Your constructive feedback during reviews helped me approach problems with clarity and confidence. When I started, I lacked hands-on experience with simulation tools and was unsure of my ability to complete a project independently. However, through this fellowship, I have not only built technical skills but also developed a sense of discipline, time management, and self-confidence.

I would also like to thank my fellow interns and team members for creating a collaborative, energetic, and friendly environment that made the journey more enjoyable.

This opportunity has significantly contributed to my growth, and I am proud to have been a part of the FOSSEE eSim team. I look forward to applying the knowledge gained here in future endeavors and contributing meaningfully to the open-source community.

Thank you, once again, to everyone who made this experience so memorable and impactful.

Contents

Chapter 1

Introduction

FOSSEE (Free/Libre and Open Source Software for Education) project promotes the use of FLOSS tools to improve the quality of education in our country. It aims to reduce dependency on proprietary software in educational institutions. It encourages the use of FLOSS tools through various activities to ensure commercial software is replaced by equivalent FLOSS tools. It also develops new FLOSS tools and upgrade existing tools to meet requirements in academia and research.[1]

The FOSSEE project is part of the National Mission on Education through Information and Communication Technology (ICT), Ministry of Human Resource Development (MHRD), Government of India.

1.1 eSim

eSim is a CAD tool that helps electronic system designers to design, test, and analyze their circuits. The important feature of this tool is that it is open source, allowing users to modify the source as per their needs. The software provides a generic, modular, and extensible platform for experimenting with electronic circuits. eSim is built using various free/libre and open-source software components in- cluding :

1.1.1 Kicad

Integrated software where all functions of circuit drawing, control, layout, library management, and access to the PCB design software are carried out.

1.1.2 Ngspice

Ngspice is a general-purpose circuit simulation program for nonlinear dc, nonlinear transient, and linear ac analysis.

1.1.3 KiCad to Ngspice converter

Analysis parameters,source details are provided through this module. It allows us to add and edit the device models and subcircuits included in the circuit schematic.

1.1.4 Subcircuit Builder

This module allows the user to create a subcircuit for a component. Once the subcircuit for a component is created, the user can use it in other circuits.

1.1.5 NGHDL

A module for mixed signal circuit simulation, is also integrated with eSim. It makes use of VHDL code.

1.1.6 NgVeri

NgVeri, a module for mixed signal circuit simulation, is also integrated with eSim. It makes use of Verilog/System Verilog/Transaction-Level Verilog code.

1.1.7 Makerchip

Makerchip is a cloud-based browser application developed by Redwood EDA to do digital circuit design. One can simulate Verilog/SystemVerilog/Transaction-Level Verilog code in Makerchip.

Chapter 2

Abstract

The objective of this internship was to design and develop various integrated circuits using the Subcircuit Builder Method in eSim. This involved modeling the ICs with eSim library files and subsequently simulating them with different circuits. The goal was to expand the eSim Subcircuit Library for future use, enhancing its utility and application in educational and practical scenarios.

2.1 Approach

- Identify and research an integrated circuit (IC) that is not currently available in the eSim library.
- Obtain and study the datasheet of the selected IC thoroughly.
- Carefully examine the schematic provided in the datasheet.
- Accurately recreate the schematic in eSim using the Subcircuit Builder Method.
- Model the IC in eSim, ensuring all parameters and configurations match those in the datasheet.
- Simulate the integrated circuit within eSim, testing it with various circuits to verify its functionality.
- Document the process and results to contribute to the future use and expansion of the eSim Subcircuit Library.

Chapter 3

Integrated Circuit Design

3.1 SN74LVC1GX04

3.1.1 Description

The **SN74LVC1GX04** device is designed for 1.65-V to 5.5-V VCC operation. This device incorporates the SN74LVC1GU04 (inverter with unbuffered output) and the SN74LVC1G04 (inverter) functions into a single device. The LVC1GX04 is optimized for use in crystal oscillator applications. X1 and X2 can be connected to a crystal or resonator in oscillator applications. The device provides an additional buffered inverter (Y) for signal conditioning.

Features of SN74LVC1GX04

- **Crystal Oscillator Driver:** This chip is primarily designed to drive crystal oscillators, creating stable clock signals for electronic devices.
- **Wide Voltage Range:** It works across a broad power supply range (1.65 V to 5.5 V), making it flexible for various system designs.
- **High Speed & Low Power:** The SN74LVC1GX04 operates quickly (fast propagation delay) while consuming very little power, which is great for efficiency.
- **Small Size:** It comes in tiny packages, ideal for compact designs where space is limited protection and can tolerate 5V input signals even with a lower supply voltage, making it very durable.

3.1.2 Pin Diagram

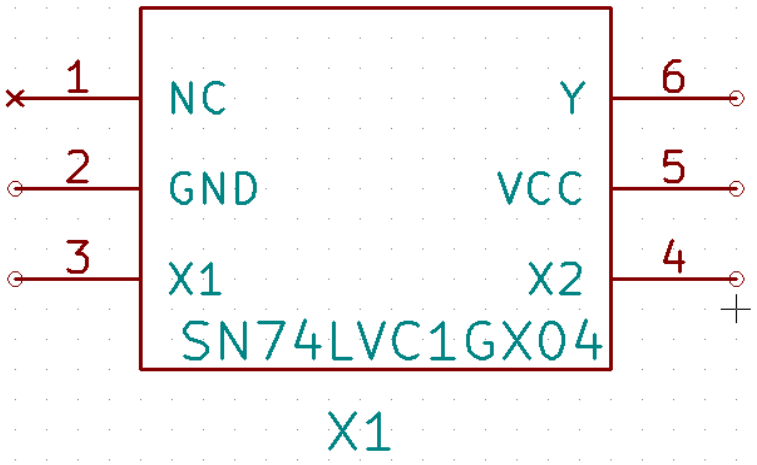

Figure 3.1: Pin Diagram of SN74LVC1GX04

3.1.3 Subcircuit Diagram

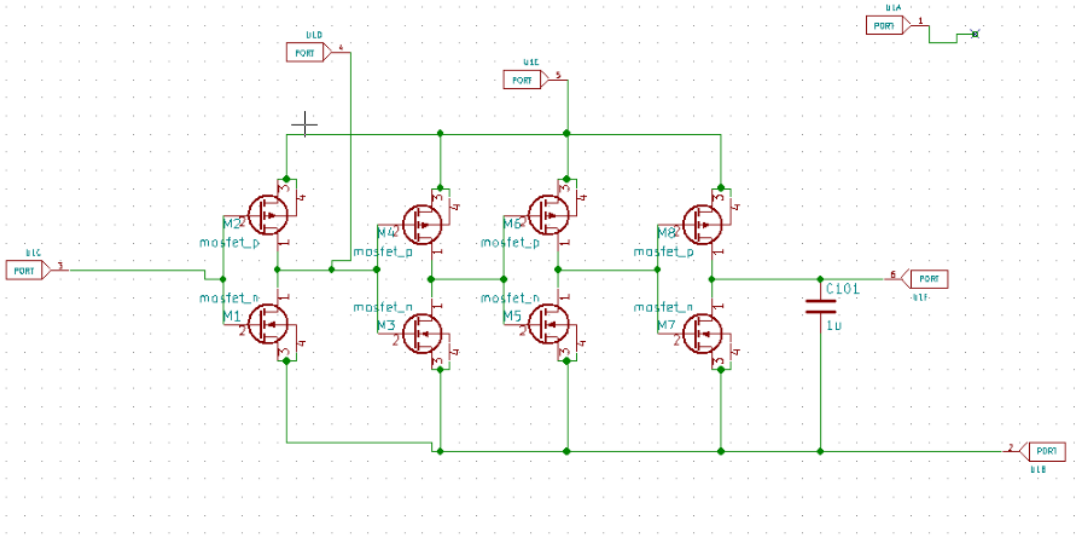

Figure 3.2: Subcircuit of SN74LVC1GX04

3.1.4 Test Circuit

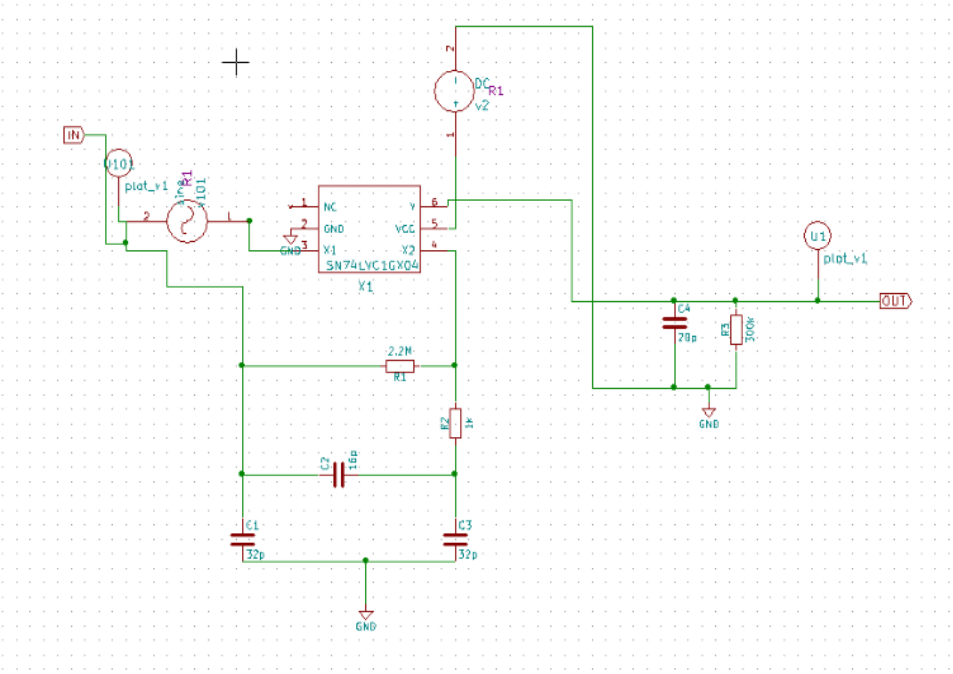

Figure 3.3: Test Circuit of SN74LVC1GX04

3.1.5 NgSpice Plot

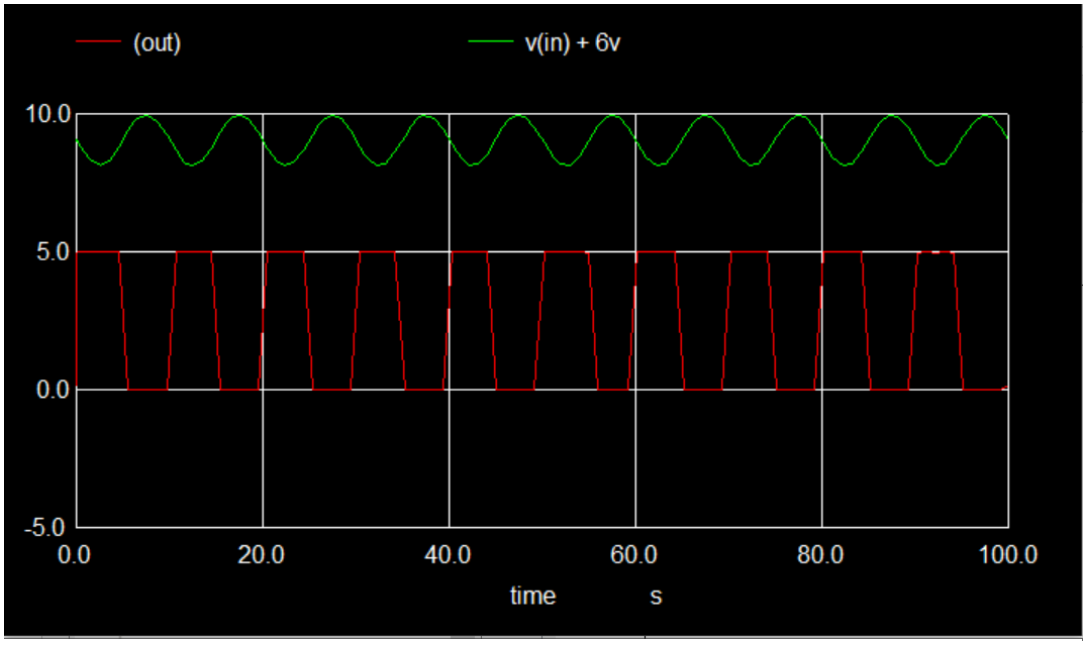

Figure 3.4: Simulation Diagram of SN74LVC1GX04

3.2 CD74HC366

3.2.1 Description

The **CD74HC366** is a **hex (six) inverting buffer/line driver** in the high-speed CMOS family. Its key feature is **three-state outputs**, allowing it to connect or disconnect from a bus, ideal for shared data lines. It strengthens digital signals and inverts them, operating across a wide voltage range for various applications.

Features of CD74HC366

- **Hex Inverting Buffers:** It contains six independent circuits, each acting as an inverter (high input gives low output, and vice-versa).
- **Three-State Outputs:** Each of the six outputs can be actively high, actively low, or in a high-impedance (disconnected) state, crucial for shared bus systems.
- **High-Speed CMOS (HC):** It's part of a fast, low-power logic family, offering efficient operation compared to older technologies.
- **Bus Driver Capability:** It's designed to drive high current loads, making it suitable for connecting to data buses and long signal lines.
- **Wide Operating Voltage:** The IC functions reliably over a broad supply voltage range, typically from 2V to 6V.

3.2.2 Pin Diagram

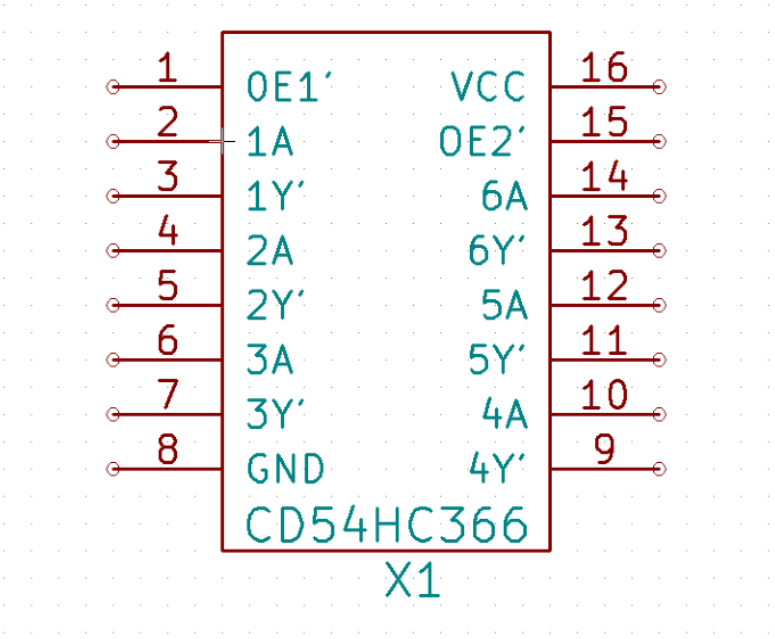

Figure 3.5: Pin Diagram of CD74HC366

3.2.3 Subcircuit Diagram

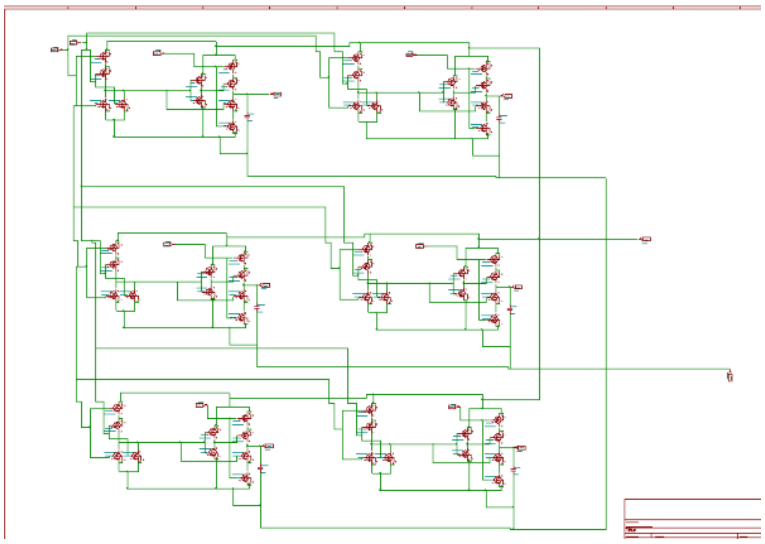

Figure 3.6: Subcircuit of CD74HC366

3.2.4 Test Circuit

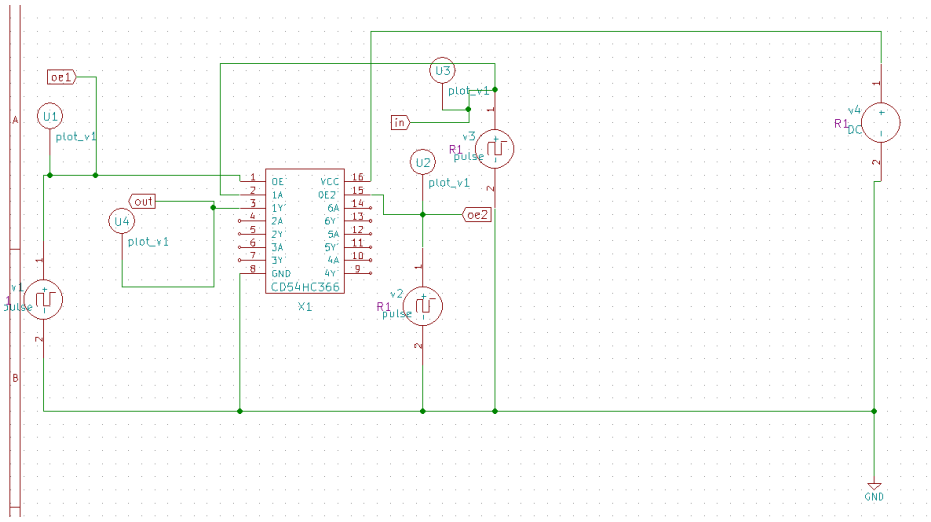

Figure 3.7: Test Circuit of CD74HC366

3.2.5 NgSpice Plot

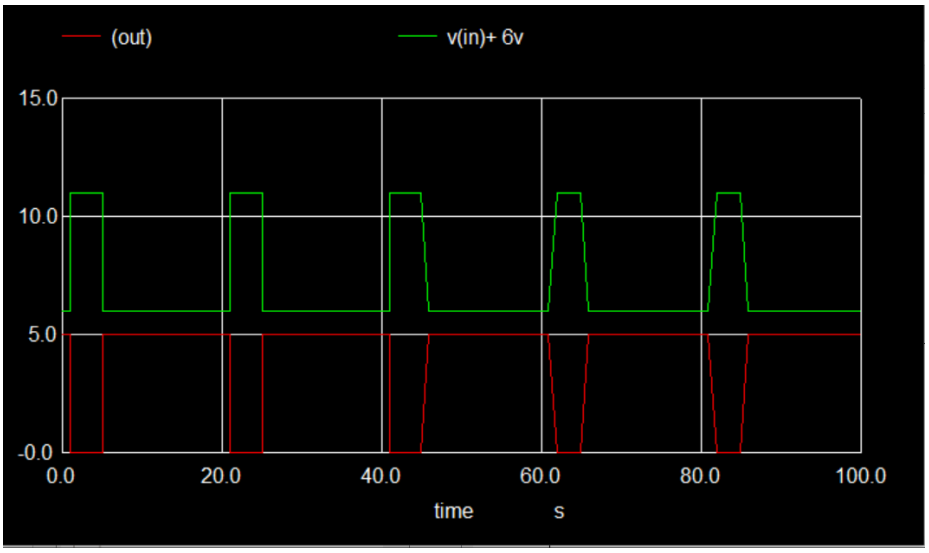

Figure 3.8: Simulation Diagram of CD74HC366

3.3 CD74HC365

3.3.1 Description

The **CD74HC365** is **a high-speed CMOS hex buffer/line driver** with non-inverting three-state outputs. It has six buffers controlled by two active-low enable inputs for easy bus interfacing. It operates efficiently across 2V to 6V with low power consumption and high noise immunity. This IC is ideal for driving data lines in digital systems requiring fast switching and isolation.

Features of CD74HC365

- **High-speed performance** with typical propagation delay around 8 ns at 5v.
- **Three-state non-inverting outputs** for efficient bus interfacing.
- **Wide voltage range** operation from 2V to 6V.
- **High noise immunity**, making it reliable in noisy environments.
- **Low power consumption** due to CMOS technology.

3.3.2 Pin Diagram

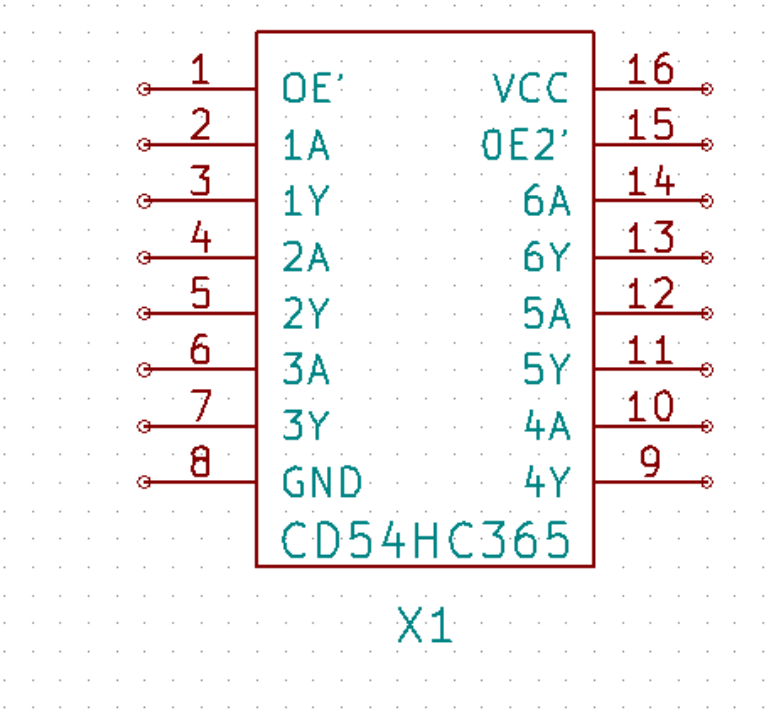

Figure 3.9: Pin Diagram of CD74HC365

3.3.2 Subcircuit Diagram

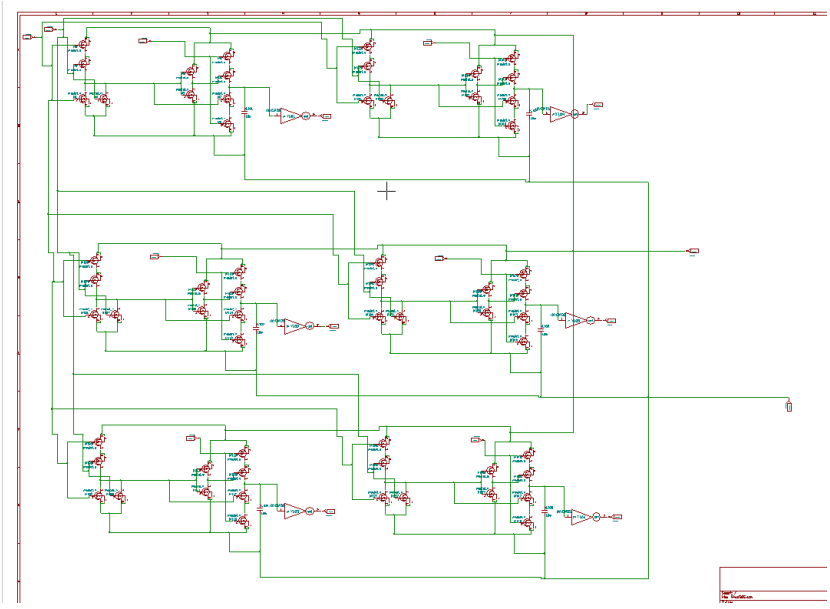

Figure 3.10: Subcircuit of CD74HC365

3.3.3 Test Circuit

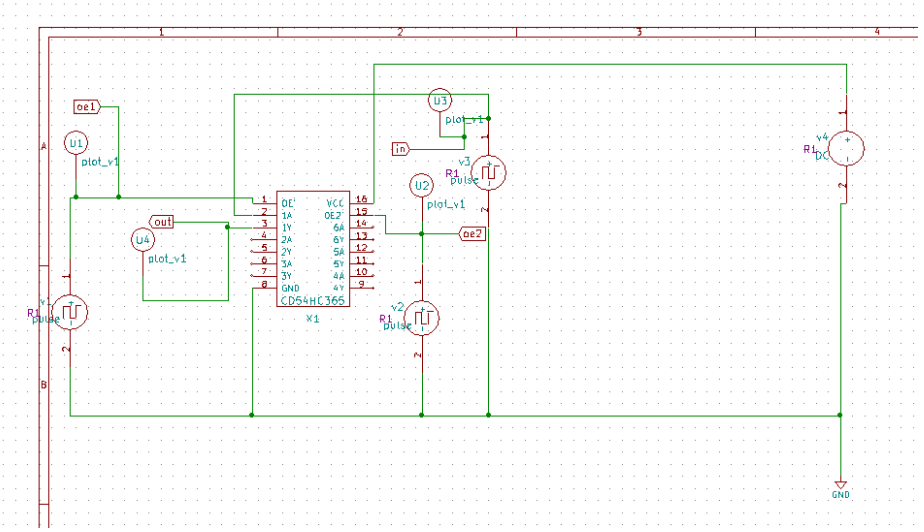

Figure 3.11: Test Circuit of CD74HC365

3.3.4 NgSpice Plot

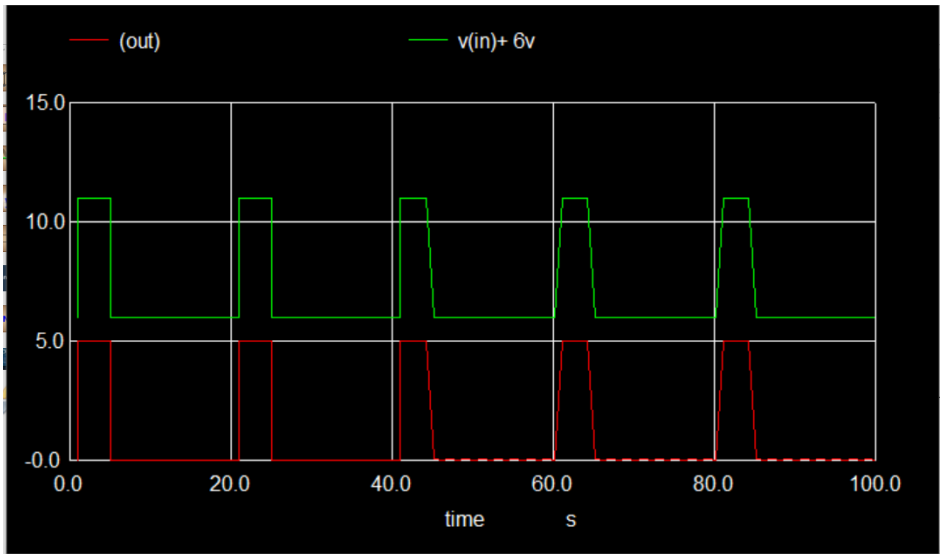

Figure 3.12: Simulation Diagram of CD74HC365

3.4 SN54F71

3.4.1 Description

The **SN74F71/ SN54F71** is a high-speed bipolar logic device that contains **dual 2-wide 2-input AND-OR-invert (AOI) gates**. Each gate performs a logic function where two pairs of inputs are ANDed separately, then the results are ORed together and finally inverted. This makes it useful for implementing complex logic functions in a compact form

Features of SN54F51

- **Dual 2-wide 2-input AOI gates**: Each gate performs (A1 AND A2) OR (B1 AND B2), then inverts the result.
- **High-speed bipolar logic**: Belongs to the 74F series, offering fast switching times.
- **TTL-compatible inputs and outputs**: Easily interfaces with other TTL logic devices.
- **Standard 14-pin DIP/SOIC package**: Convenient for PCB mounting and prototyping.
- **Ideal for complex logic functions**: Useful in arithmetic logic units, control logic, and data path designs.

3.4.2 Pin Diagram

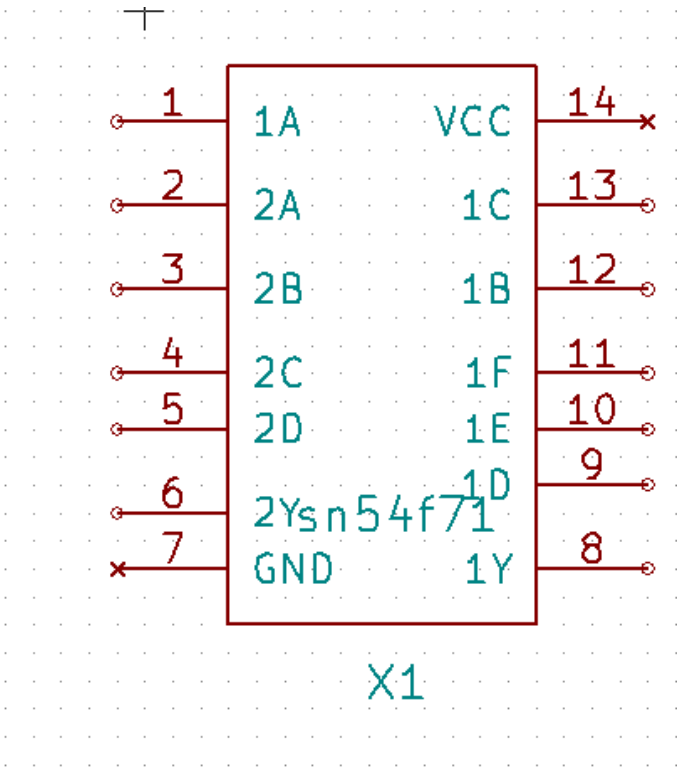

Figure 3.13: Pin Diagram of SN54F71

3.4.3 Subcircuit Diagram

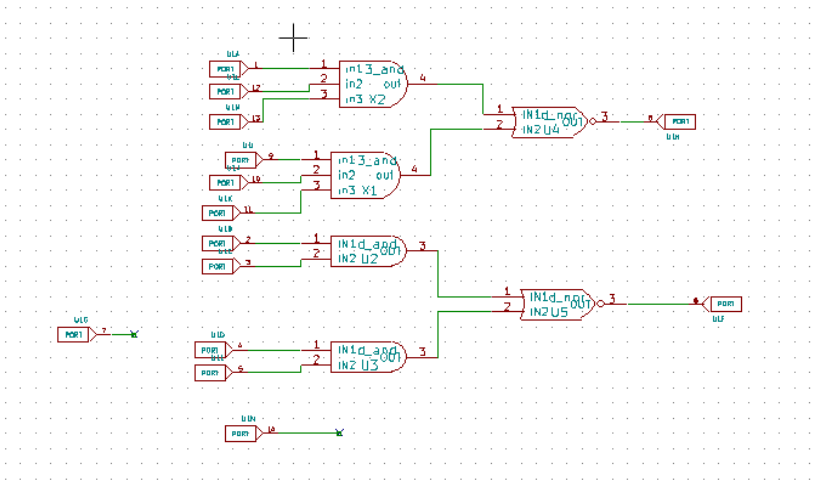

Figure 3.14: Subcircuit of SN54F751

3.4.4 Test Circuit

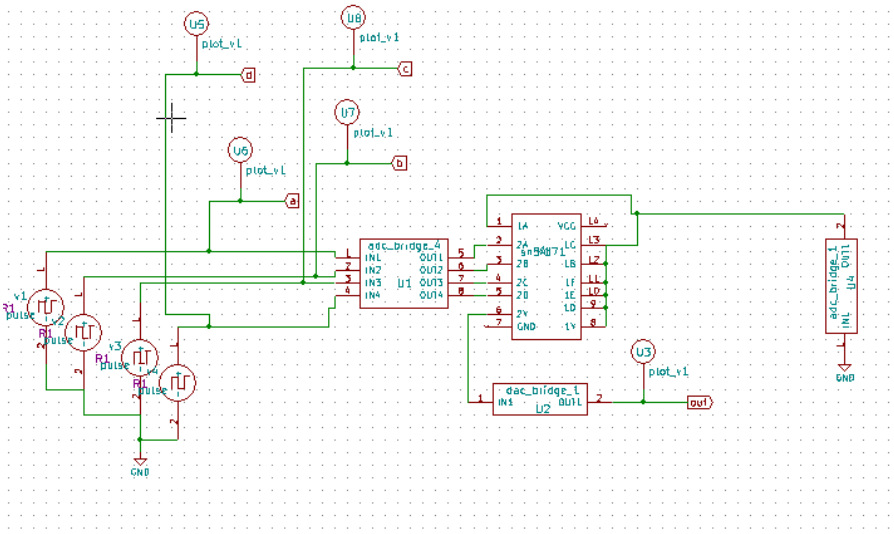

Figure 3.15: Test Circuit of SN54F71

3.4.5 NgSpice Plot

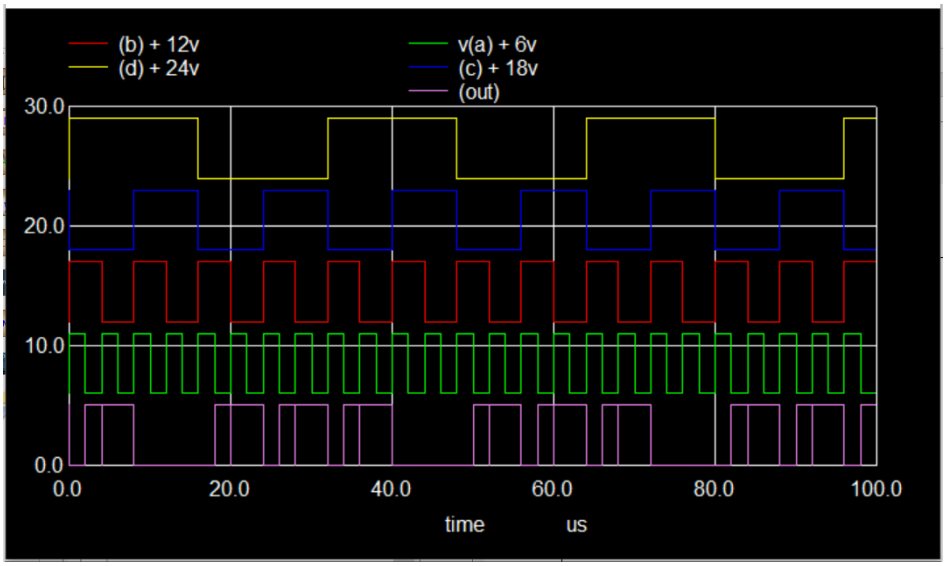

Figure 3.16: Simulation Diagram of SN54F71

3.5 SN54155

3.5.1 Description

The **SN54155** is a high-speed TTL logic IC that contains **dual 2-line to 4-line decoders/demultiplexers**. Each section has two binary select inputs and an enable input, allowing it to decode two input lines into one of four mutually exclusive outputs. It's commonly used in memory address decoding, data routing, and demultiplexing applications.

Features of SN54155

- **Dual 2-to-4 decoding**: Each section decodes 2 binary inputs into 1 of 4 outputs.
- **Independent enable inputs**: Each decoder has its own enable pin for flexible control.
- **High-speed TTL logic**: Designed for fast switching in digital systems.
- **Complementary outputs**: One section provides inverted outputs, the other non-inverted.
- **Wide operating temperature range**: Suitable for military-grade applications (–55°C to 125°C).

3.5.2 Pin Diagram

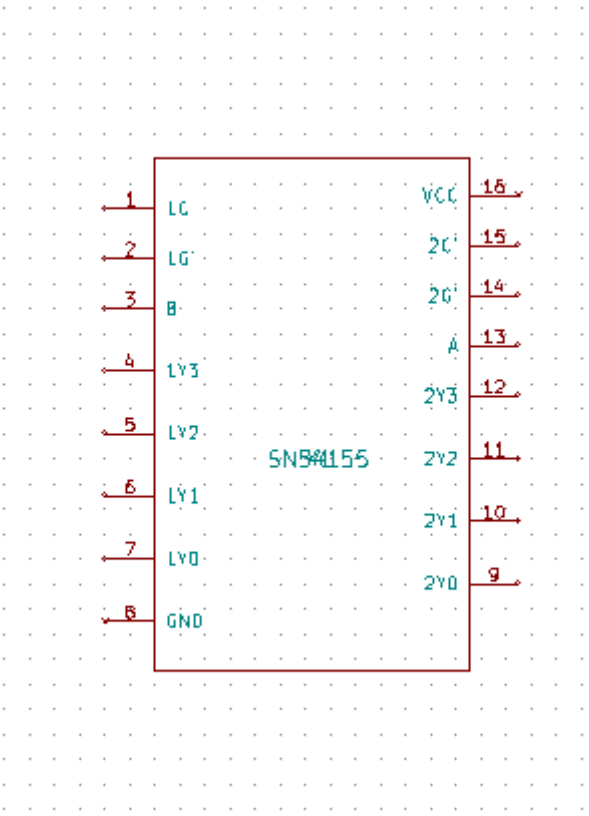

Figure 3.17: Pin Diagram of SN54155

3.5.3 Subcircuit Diagram

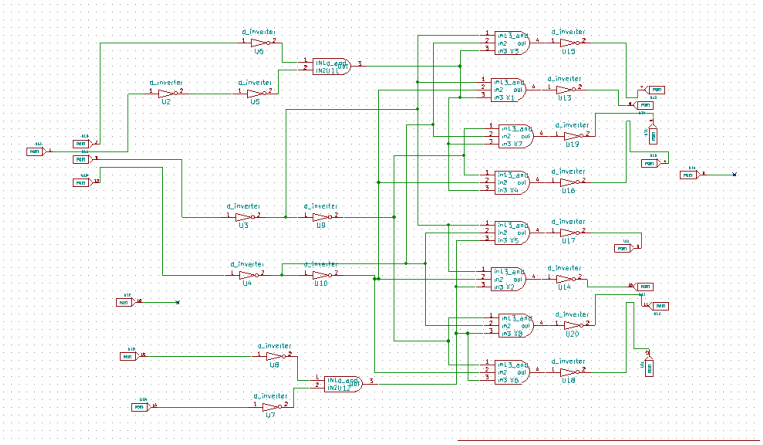

Figure 3.18: Subcircuit of SN54155

3.5.4 Test Circuit

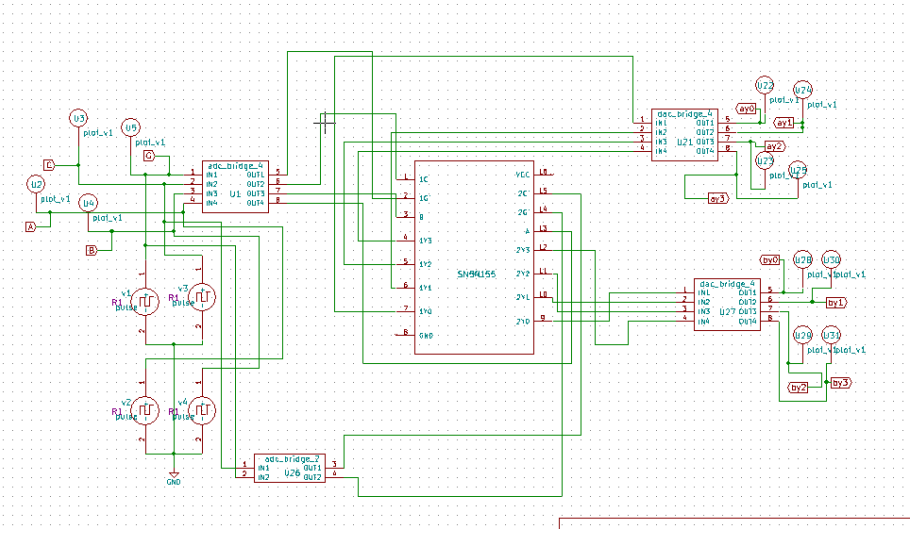

Figure 3.19: Test Circuit of SN54155

3.5.5 NgSpice Plot

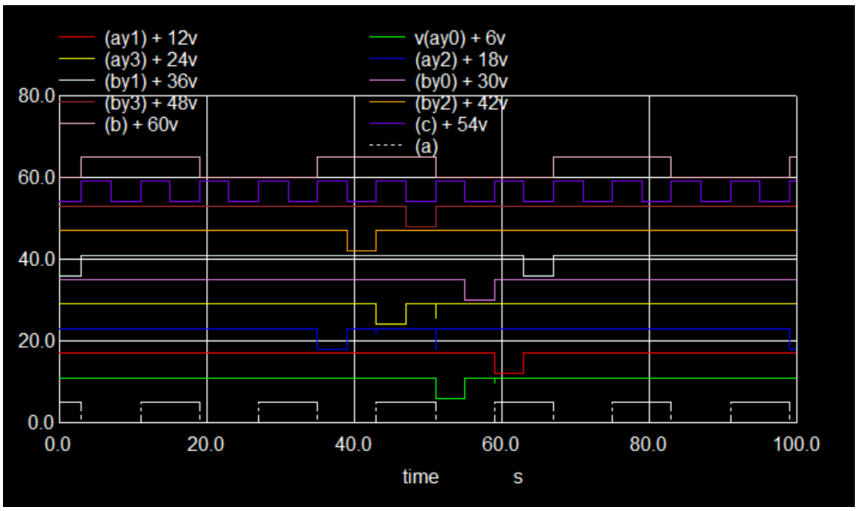

Figure 3.20: Simulation Diagram of SN5415

3.6 MC10H166

3.6.1 Description

The **MC10H166** is a 5-bit magnitude comparator built with MECL 10K logic for ultra-high-speed operation. It compares two 5-bit binary numbers and outputs whether A > B, A = B, or A < B. The device supports **cascading** to compare larger bit-widths. Ideal for high-performance systems, it offers low delay (~2 ns) and high noise immunity.

Features of MC10H166

- **Ultra-fast operation** with a typical propagation delay of just 2.0 ns.
- **Improved noise margin** of 150 mV for reliable performance across conditions.
- **Voltage-compensated design**, ensuring consistent behavior over temperature and supply variations.
- **MECL 10K compatibility**, making it suitable for high-speed ECL systems.
- **Expandable architecture** for comparing binary words larger than 5 bits.

3.6.2 Pin Diagram

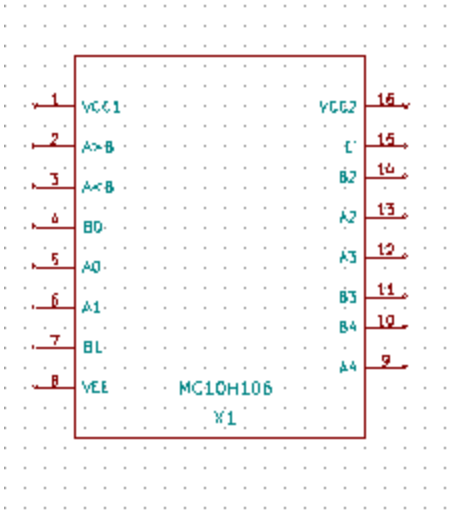

Figure 3.21: Pin Diagram of MC10H166

3.6.3 Subcircuit Diagram

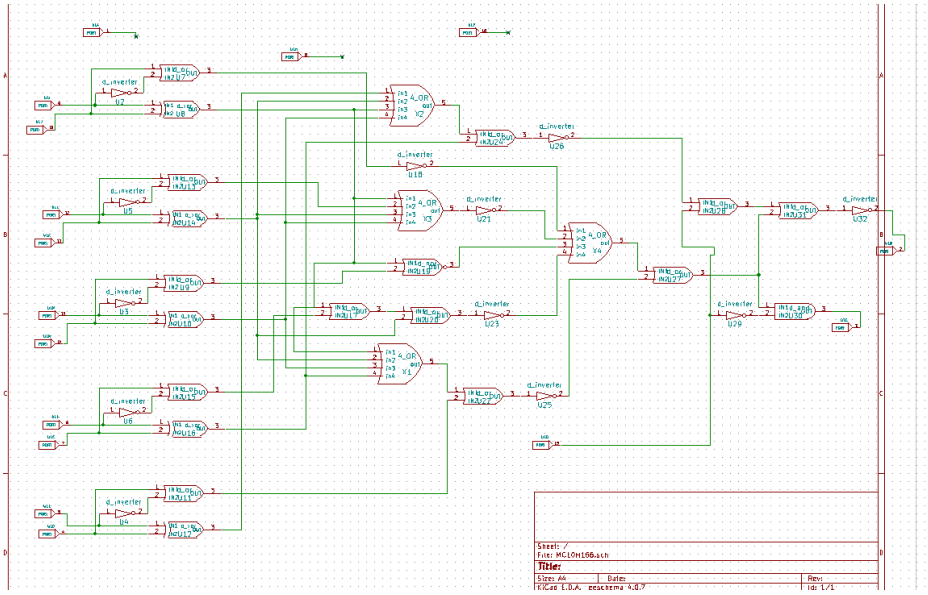

Figure 3.22: Subcircuit of MC10H166

3.6.4 Test Circuit

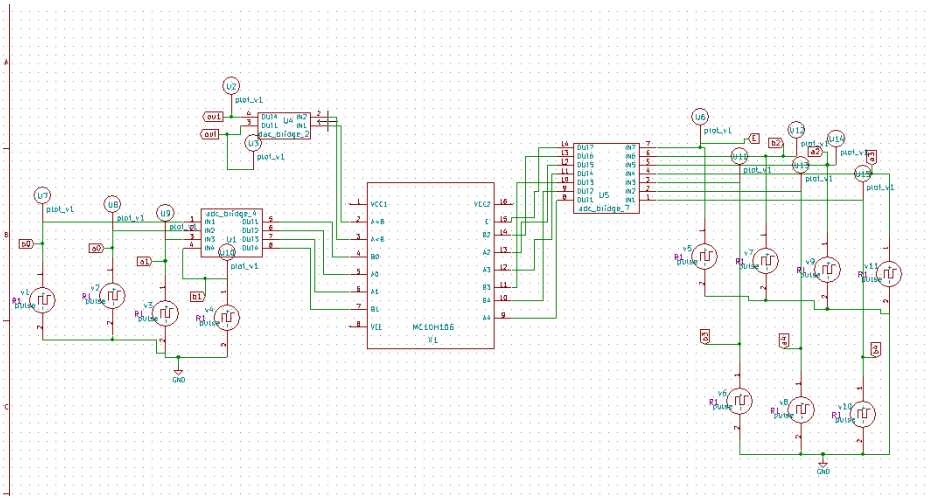

Figure 3.23: Test Circuit of MC10H166

3.6.5 NgSpice Plot

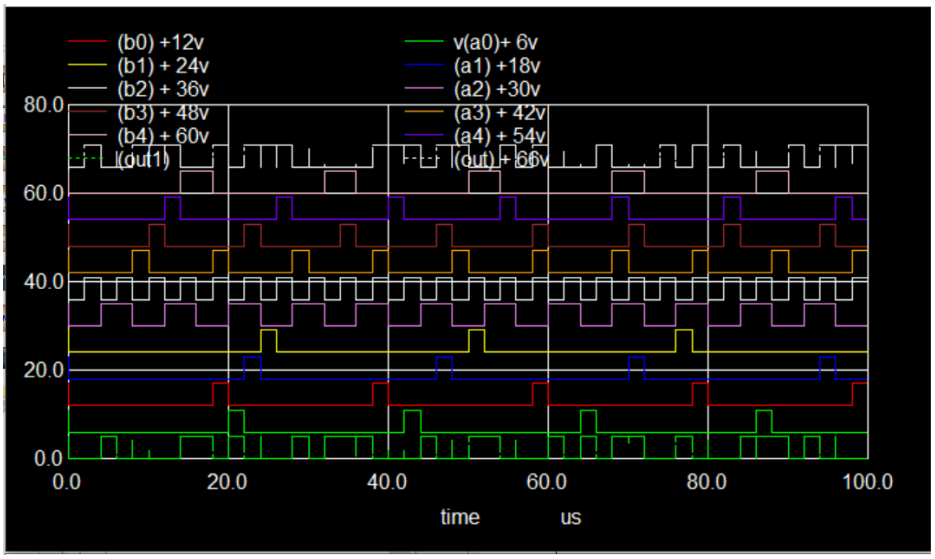

Figure 3.24: Simulation Diagram of MC10H166

3.7 SN74F521

3.7.1 Description

The **SN74F521** is an **8-bit identity comparator** from Texas Instruments. It compares two 8-bit binary or BCD words and outputs a logic LOW when the inputs are equal (P = Q). The device includes an **enable input (OE)** that controls whether the output is active or in a high-impedance state, making it ideal for bus-oriented systems. It's commonly used in digital systems for equality checking, address decoding, and data comparison tasks

Features of SN74F521

- **8-bit comparison**: Compares two 8-bit binary or BCD words and outputs LOW when they are equal.
- **Active-low output**: The output goes LOW only when inputs match, simplifying logic design.
- **Enable input (OE)**: Allows output to be placed in a high-impedance state for bus interfacing.
- **Fast switching**: Typical propagation delay of 10 ns at 5V, ideal for high-speed systems.
- **TTL-compatible**: Operates on 4.5V to 5.5V supply and integrates easily with TTL logiclevels.

3.7.2 Pin Diagram

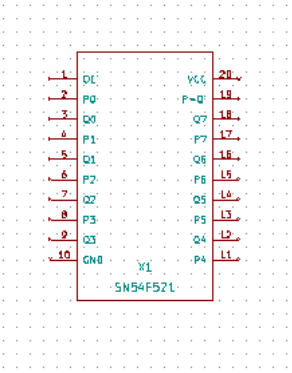

Figure 3.25: Pin Diagram of SN74F521

3.7.3 Subcircuit Diagram

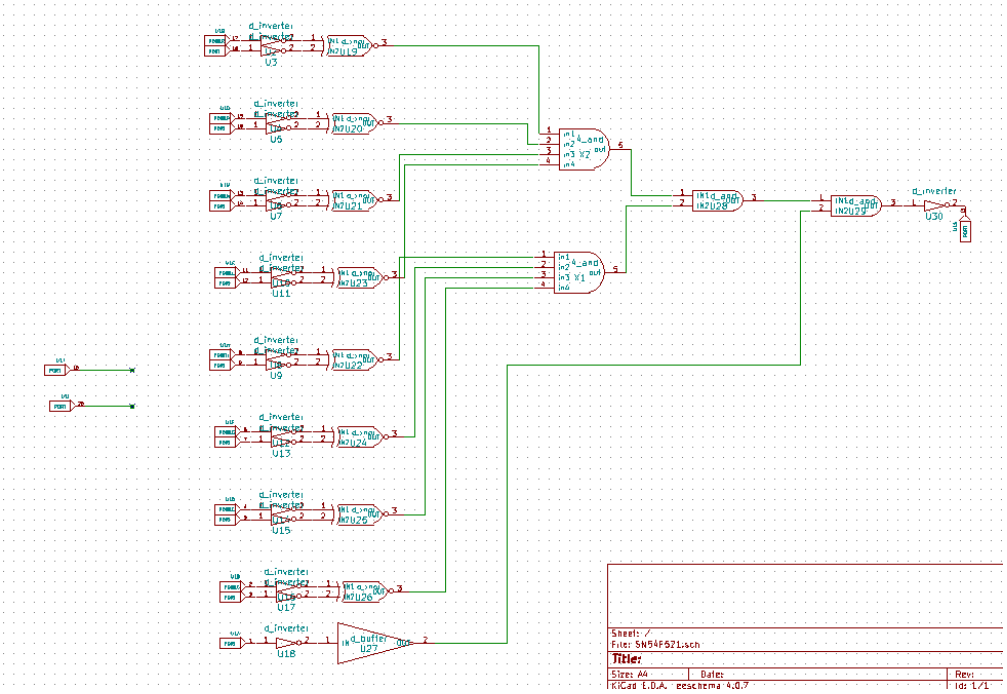

Figure 3.26: Subcircuit of SN74F521

3.7.4 Test Circuit

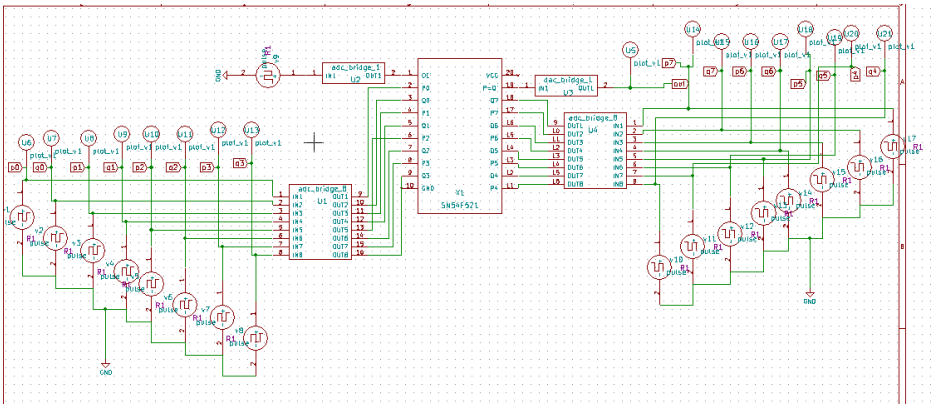

Figure 3.27: Test Circuit of SN74F521

3.7.5 NgSpice Plot

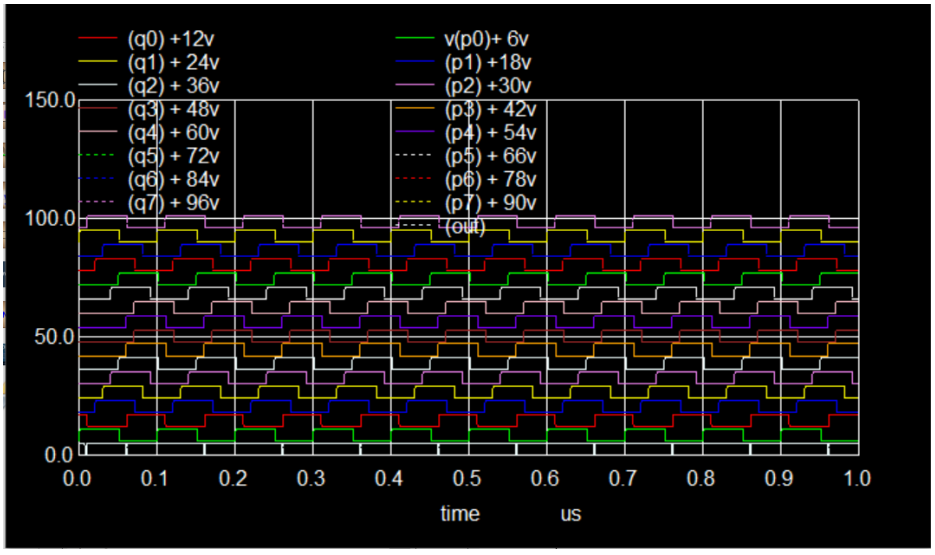

Figure 3.28: Simulation Diagram of SN74F521

3.8 DM74LS460

3.8.1 Description

The **DM74LS460** is a **10-bit digital comparator** from the LS TTL logic family. It compares two 10-bit binary values and provides outputs indicating whether the inputs are equal or not. The device includes both **true and complement outputs** (EQ and NE), making it versatile for logic decision-making. It's commonly used in digital systems for equality checking, sorting, and address comparison.

Features of DM74LS460

- **10-bit comparison capability** with true (EQ) and complement (NE) outputs.
- **Expandable architecture** for comparing wider binary words in cascaded configurations.
- **Standard 24-pin DIP package**, ideal for prototyping and integration.
- **Totem-pole outputs** capable of sourcing and sinking current for direct logic interfacing.
- **Low input loading** due to PNP input structure, reducing power draw from driving circuits.

3.8.2 Pin Diagram

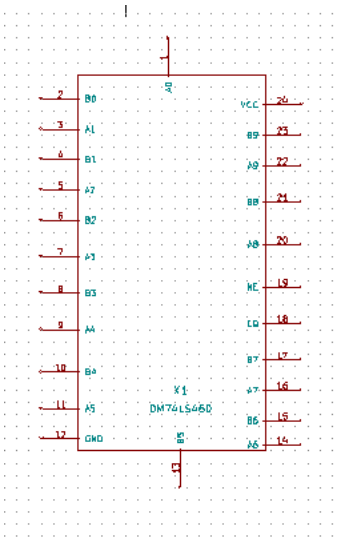

Figure 3.29: Pin Diagram of DM74LS460

3.8.3 Subcircuit Diagram

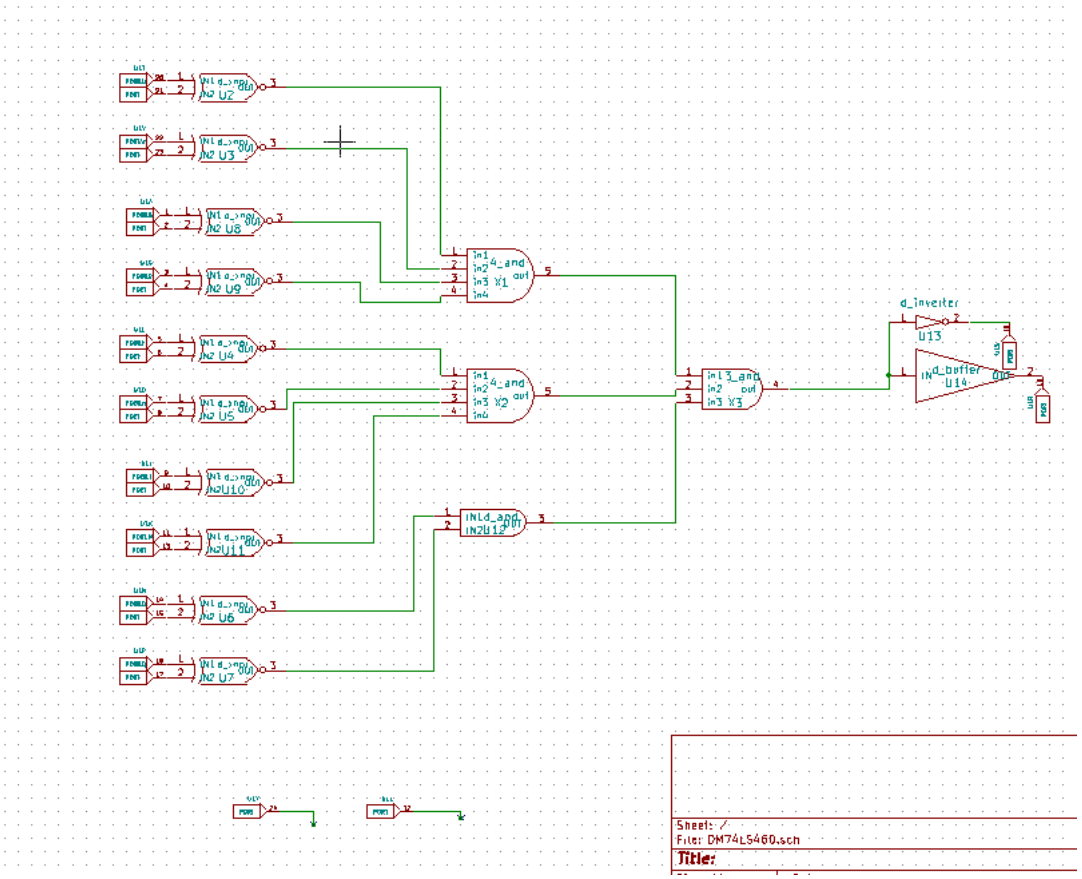

Figure 3.30: Subcircuit of DM74LS460

3.8.4 Test Circuit

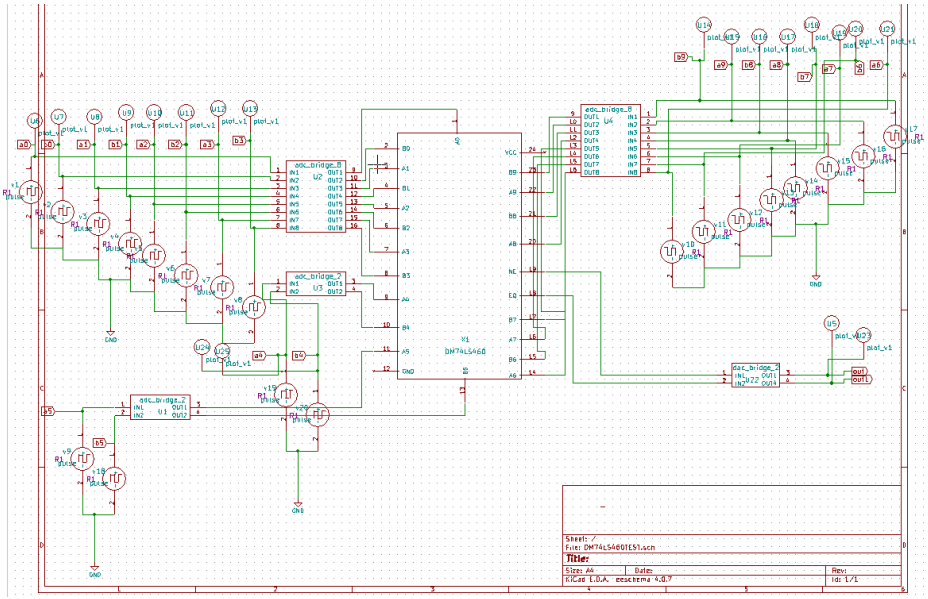

Figure 3.31: Test Circuit of DM74LS460

3.8.5 NgSpice Plot

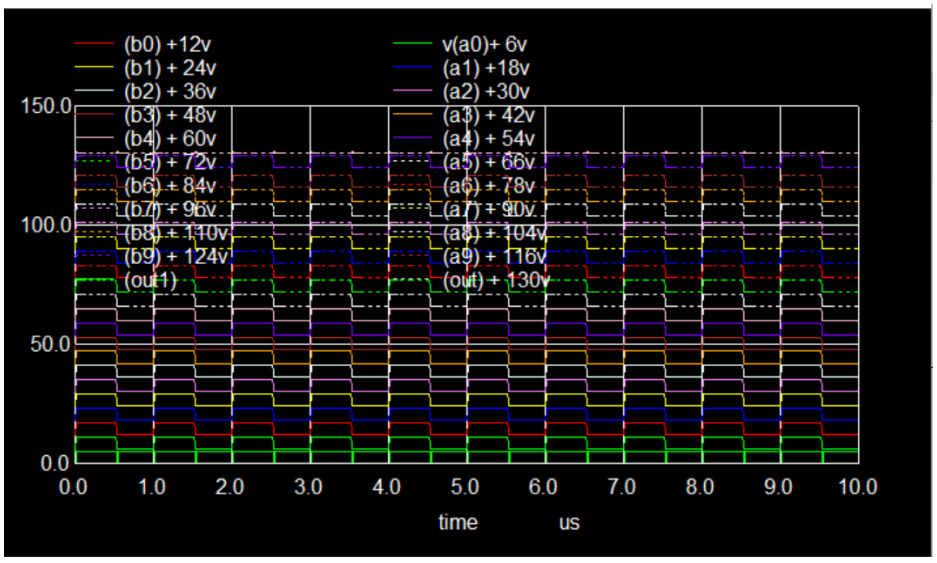

Figure 3.32: Simulation Diagram of DM74LS460

3.9 DM9301

3.9.1 Description

The **DM9301** is a TTL logic device that functions as a **1-of-10 (BCD-to-decimal) decoder**. It takes a 4-bit Binary Coded Decimal (BCD) input and activates one of ten outputs corresponding to decimal digits 0 through 9. Internally, it uses inverters and 4-input NAND gates to decode valid BCD inputs, while ensuring all outputs remain OFF for invalid combinations.

Features of DM9301

- **Decodes 4-bit BCD input** into one of ten active-high outputs (0–9).
- **Built-in inverters and 4-input NAND gates** for full decoding logic.
- **All outputs remain HIGH** for invalid BCD inputs (1010–1111).
- **Diode-clamped TTL-compatible inputs** for reliable interfacing.
- **Typical power dissipation** of 125 mW with a propagation delay of ~20 ns.

3.9.2 Pin Diagram

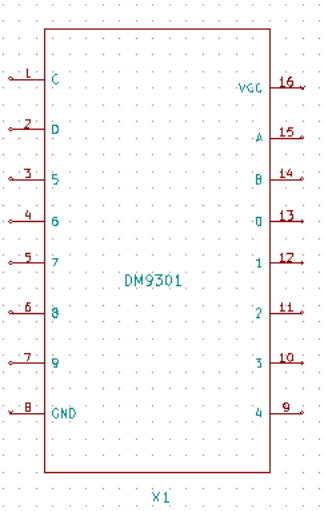

Figure 3.33: Pin Diagram of DM9301

3.9.3 Subcircuit Diagram

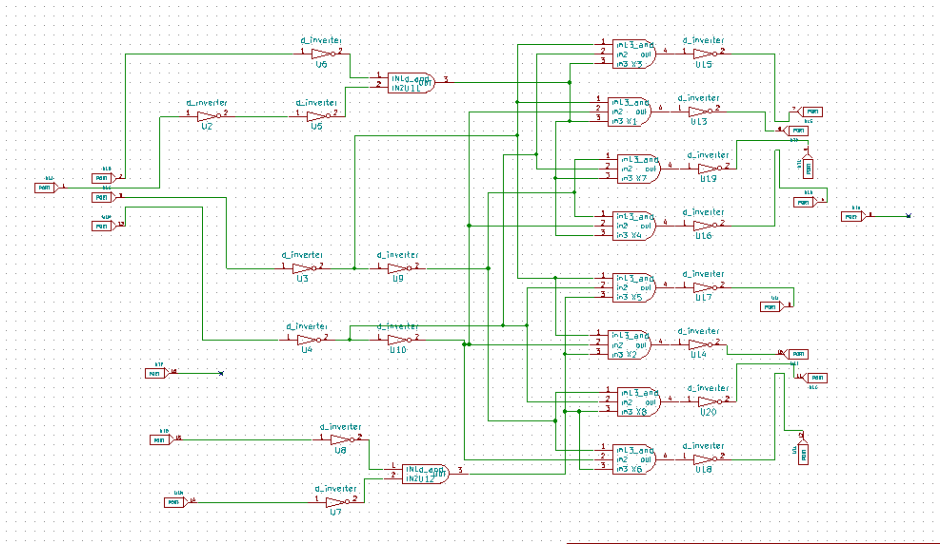

Figure 3.34: Subcircuit of DM9301

3.9.4 Test Circuit

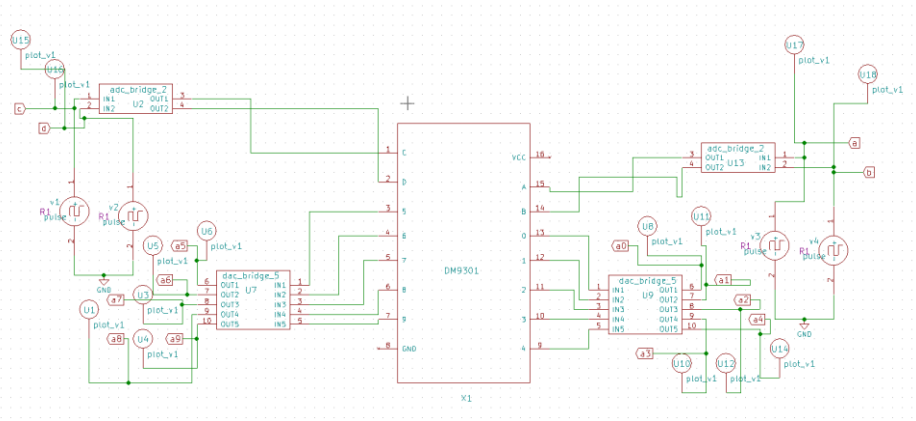

Figure 3.35: Test Circuit of DM9301

3.9.5 NgSpice Plot

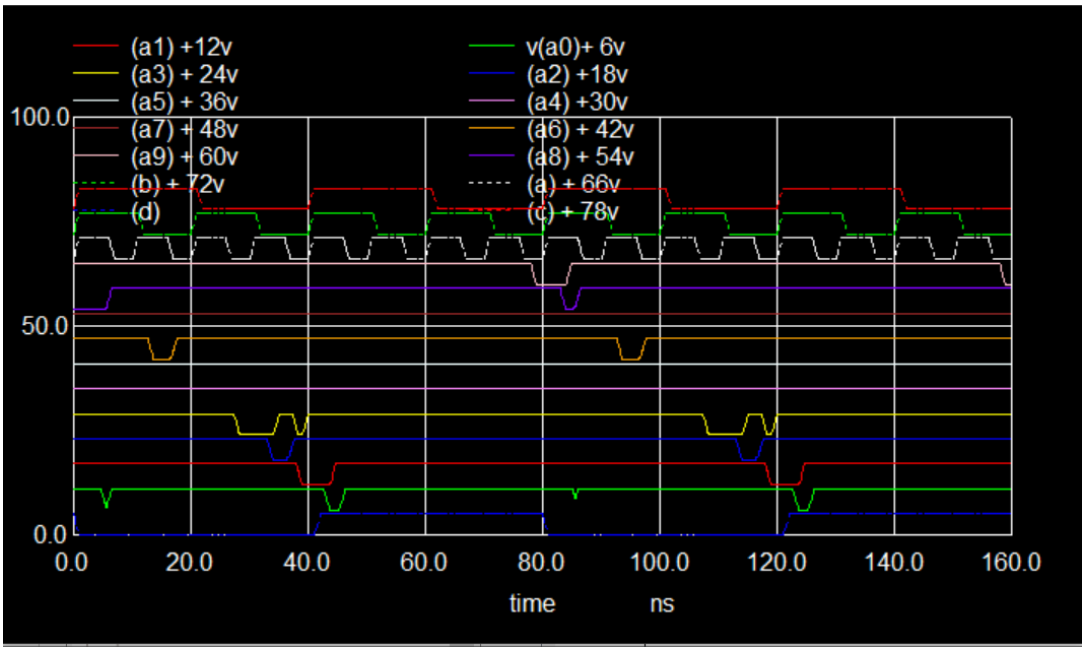

Figure 3.36: Simulation Diagram of DM9301

Chapter 4

Conclusion and Future Scope

The project not only reinforces foundational concepts in design but also highlights the significance of accessible simulation environments in fostering innovation and skill development in electronic design automation.

These digital IC models serve as essential building blocks for designing and simulating complex digital systems, making them valuable resources for students, educators, and researchers.

This project successfully demonstrates the comprehensive design and simulation of a integrated circuits utilizing the eSim platform.

The process encompassed schematic development, component interconnection, and rigorous simulation, culminating in the validation of the circuit's intended functionality.

Through this endeavor, a deeper understanding of digital circuit principles and practical experience with an open-source EDA tool were achieved.

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