Summer Fellowship Report

On

Analog and Digital ICs Design in eSim

Submitted by

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Under the guidance of

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Acknowledgment

I would like to express my heartfelt gratitude to the entire FOSSEE team at IIT Bombay for granting me the invaluable opportunity to participate in the Semester-Long Internship program. Being associated with such a prestigious and impactful open-source initiative has been a truly enlightening experience, both academically and professionally.

I extend my sincere thanks to Prof. Kannan M. Moudgalya, whose visionary leadership and unwavering commitment to promoting open-source tools in education have been truly inspiring. His guidance has laid a strong foundation for students like me to explore the world of simulation and electronic design through tools like eSim.

I am especially thankful to my mentors, Mr. Sumanto Kar and Mrs. Maheswari Raju, for their continuous support, encouragement, and insightful feedback throughout the internship. Their mentorship helped me navigate technical challenges and enabled me to find effective solutions during complex stages of the project.

This internship not only enhanced my understanding of electronic circuit simulation and design, but also significantly strengthened my analytical and problem-solving skills. The experience has played a pivotal role in shaping my career aspirations, particularly in the field of semiconductor and embedded system design.

I am truly grateful for the learning, collaboration, and exposure I gained during this internship. It has been a major milestone in my journey as a budding engineer.

Contents

Chapter 1

Introduction

FOSSEE (Free/Libre and Open Source Software for Education) project promotes the use of FLOSS tools to improve the quality of education in our country. It aims to reduce dependency on proprietary software in educational institutions. It encourages the use of FLOSS tools through various activities to ensure commercial software is replaced by equivalent FLOSS tools. It also develops new FLOSS tools and upgrade existing tools to meet requirements in academia and research[2].

This internship report outlines the work completed as part of the eSim internship conducted by FOSSEE, IIT Bombay. eSim is an open-source EDA (Electronic Design Automation) tool developed as a free alternative to commercial software like OrCAD, PSpice, and LTspice. It is built using open-source tools such as KiCad and Ngspice, and enables schematic creation, circuit simulation, PCB design, and waveform analysis.

Ngspice is an open-source mixed-level/mixed-signal circuit simulator derived from Berkeley SPICE3f5. It supports analog, digital, and mixed-signal simulations and is widely used for verifying circuit behavior before hardware implementation. Ngspice forms the core simulation engine integrated within eSim, enabling accurate transient, DC, and AC analyses of circuits designed in the schematic editor [4].

Makerchip is a web-based integrated development environment (IDE) primarily focused on RISC-V and digital hardware design using Chisel and other hardware description languages. It offers interactive simulation and visualization features for hardware designs. While Makerchip is mainly used for digital logic design and verification, it complements tools like eSim and Ngspice by providing a platform for digital RTL design and testing [1].

KiCad is an open-source software suite for electronic design automation (EDA) which includes tools for schematic capture, PCB layout, and library management. eSim builds upon KiCad's schematic editor and PCB design tools, enhancing them with integrated circuit simulation through Ngspice [3].

Chapter 2

IC LM386M

Designing Subcircuit and Testbench of IC LM386M in eSim

2.1 Circuit details

The LM386M is a low-voltage audio power amplifier IC commonly used in small audio amplification projects. It is designed for battery-powered applications and can drive speakers with output power ranging from 300 mW to 700 mW, depending on the supply voltage and load. The internal circuit includes a differential input stage, gain-setting resistors and capacitors, and an output push-pull amplifier.

This section outlines the internal structure and basic application of the LM386M based on the datasheet and circuit design created in the eSim platform.

2.2 Pin Diagram

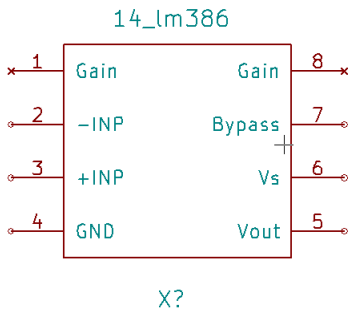

Figure 2.1: Pin out diagram of IC LM386M

Pin No.	Name	Function
1	GAIN	Gain control (used with Pin 8 to adjust gain)
2	IN-	Inverting input of the amplifier
3	IN+	Non-inverting input of the amplifier
4	GND	Ground connection
5	VCC	Power supply input (4V to 12V)
6	VOUT	Amplified audio output
7	BYPASS	Bypass capacitor connection to reduce noise
8	GAIN	Gain control (used with Pin 1)

Table 2.1: LM386M IC Pin Description

2.3 Testbench circuit for IC LM386M

The testbench designed in `eSim` simulates an audio amplifier circuit using the `LM386M` low-power audio amplifier IC. The primary goal of this setup is to analyze the amplification of a small AC input signal and observe the output waveform behavior. A sinusoidal voltage source is used to represent the input audio signal, which is AC-coupled through a 1 µF capacitor (C3) to eliminate any DC offset. This signal then passes through a 10 Ω resistor (R1) and is fed into the non-inverting input (pin 3) of the LM386M. The inverting input (pin 2) is connected directly to ground to ensure stable operation. The amplifier is configured for a default gain of 20, as no capacitor is connected between pins 1 and 8. The IC is powered by a DC supply connected to pin 6 (Vs), while pin 4 is grounded.

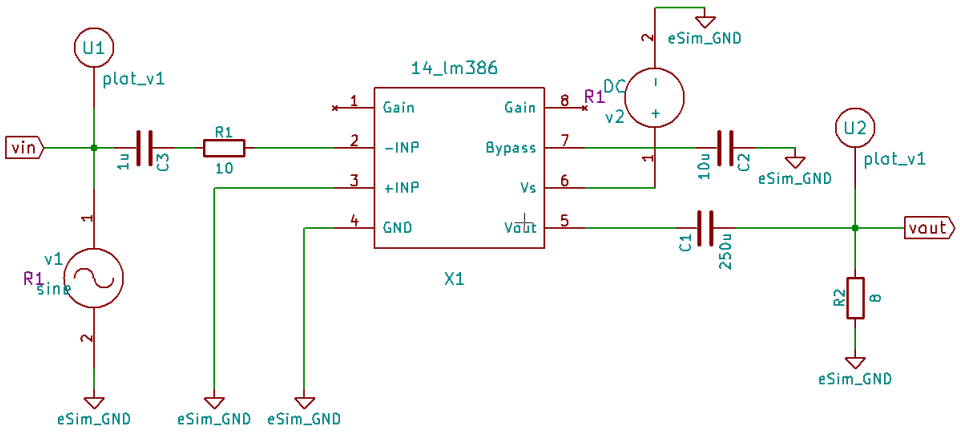

Figure 2.2: Schematic of test bench circuit

2.4 Simulation Output

The amplifier circuit in eSim. The green waveform represents the input signal, which is a low-amplitude sine wave, while the yellow waveform shows the corresponding amplified output. The output waveform exhibits a significantly higher amplitude while maintaining the same frequency as the input, confirming the expected gain and proper functionality of the amplifier. This simulation validates that the designed circuit successfully amplifies the input signal without distortion over the observed time interval of 0 to 10 milliseconds.

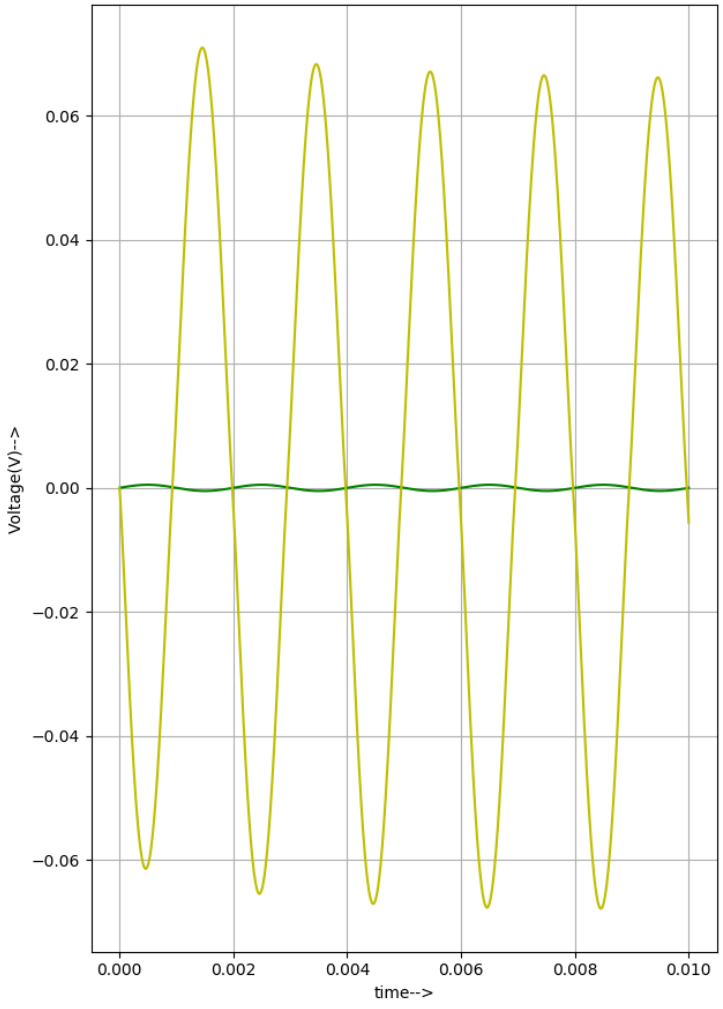

Figure 2.3: The LM386M IC output Python plot.
Green ∼ Input, Yellow ∼ Output

Chapter 3

IC 74LS95B

Designing Subcircuit and Testbench of IC 74LS95B in eSim

3.1 Circuit details

The SN54/74LS95B is a 4-Bit Shift Register with serial and parallel synchronous operating modes. The serial shift right and parallel load are activated by separate clock inputs which are selected by a mode control input. The data is transferred from the serial or parallel D inputs to the Q outputs synchronous with the HIGH to LOW transition of the appropriate clock input.

3.2 Pin Diagram

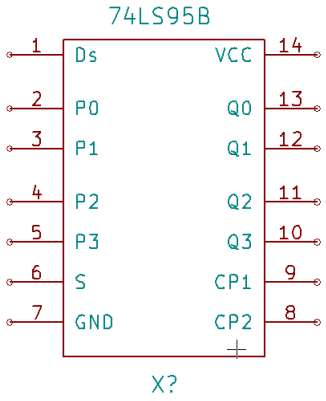

Figure 3.1: Pin out diagram of IC 74LS95B

3.3 Testbench circuit for IC 74LS95B

The testbench for the `74LS95B` shift register demonstrates both **parallel and serial operations**. Initially, with `S = LOW`, data on `P0-P3` (+24V, +18V, +12V, +6V) is loaded into `Q0-Q3` on the rising edge of `CLK2`, as seen by output voltages `O0-O3` (30V to 48V). When `S = HIGH`, the IC enters **serial mode**, and data from `Ds = +54V` is shifted through the register on each rising edge of `CLK1`. The waveform confirms correct shifting behavior. `DAC/ADC` bridges help visualize signal changes, verifying the IC's functionality.

3.4 Pin Diagram

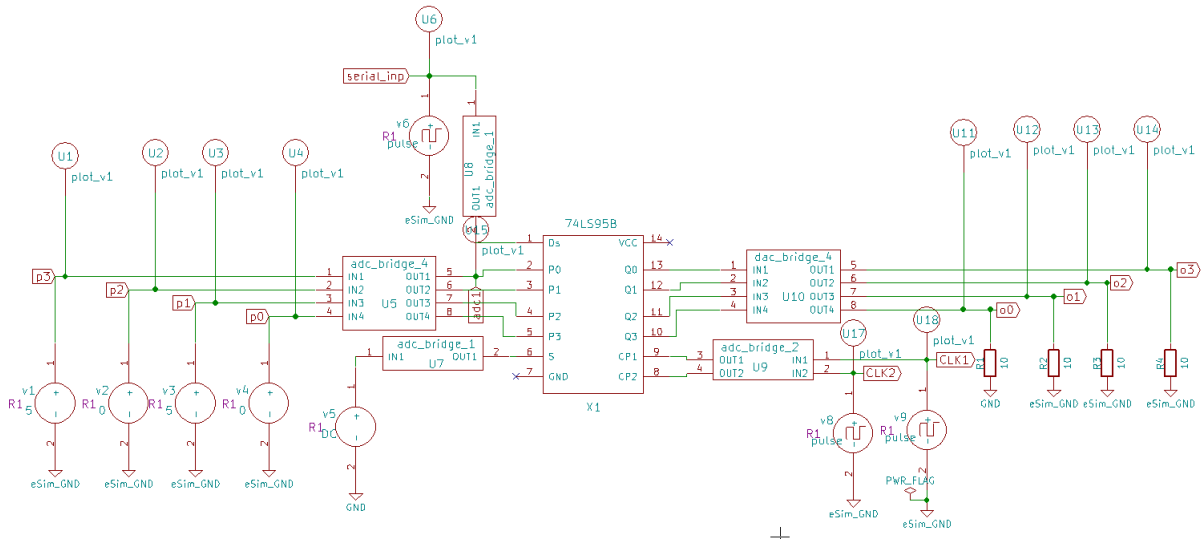

Figure 3.2: Schematic of testbench for IC 74LS95B

3.5 Simulation Output

- The testbench demonstrates **both parallel and serial modes** of the 74LS95B shift register.
- Initially, **S = 0**, enabling **parallel load** on the rising edge of **CLK2**.
- Inputs **P0–P3** are given as +24V, +18V, +12V, and +6V respectively.
- These values are loaded into outputs **Q0–Q3** as seen on **O0–O3** in the waveform.
- Corresponding output voltages are: O0 = 30V, O1 = 36V, O2 = 42V, O3 = 48V.
- After loading, **S = 1**, switching to **serial mode**.
- Serial data **Ds = +54V** (logic high) is shifted on each **CLK1** rising edge.
- The waveform shows the stepwise shift of HIGH bits from O0 to O3.
- The **DAC/ADC bridges** convert digital levels for plotting the outputs.
- The output graph confirms correct **parallel loading** and **serial shifting** operations.

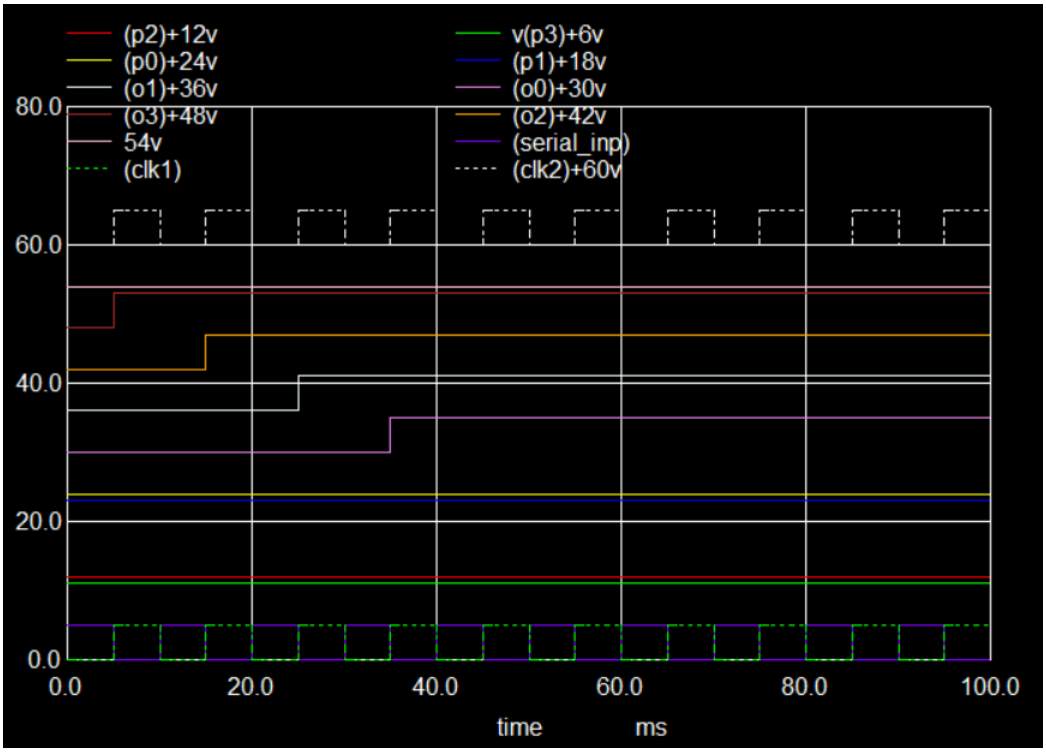

Figure 3.3: Output of IC 74LS95B

Chapter 4

IC TL431

4.1 Circuit Details

I designed and simulated a subcircuit model of the TL431, which is a programmable shunt voltage regulator IC.

To design the subcircuit, I referred to the official datasheet of the TL431 IC. The internal block diagram of the IC consists of the following major functional units:

- Sampling Circuit
- Reference Voltage Generator
- Comparator
- Control Circuit

4.2 Pinout Diagram

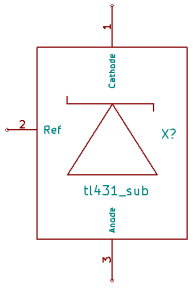

Figure 4.1: Pinout Diagram of IC TL431

The IC TL431 consists of the following three terminals:

- **Anode**
- **Cathode**
- **Reference**

4.3 Testbench circuit for IC TL431

This circuit is a voltage regulator using the TL431 programmable shunt voltage reference and the LM358 operational amplifier. The TL431 maintains a stable reference voltage of 2.5V at its reference pin, and the output voltage is adjusted using a resistor divider. The LM358 op-amp and NPN transistor help regulate the output by controlling the current flow based on feedback. A capacitor is added for output filtering, and a diode provides protection. This setup helps maintain a constant output voltage, making it useful for power supply regulation.

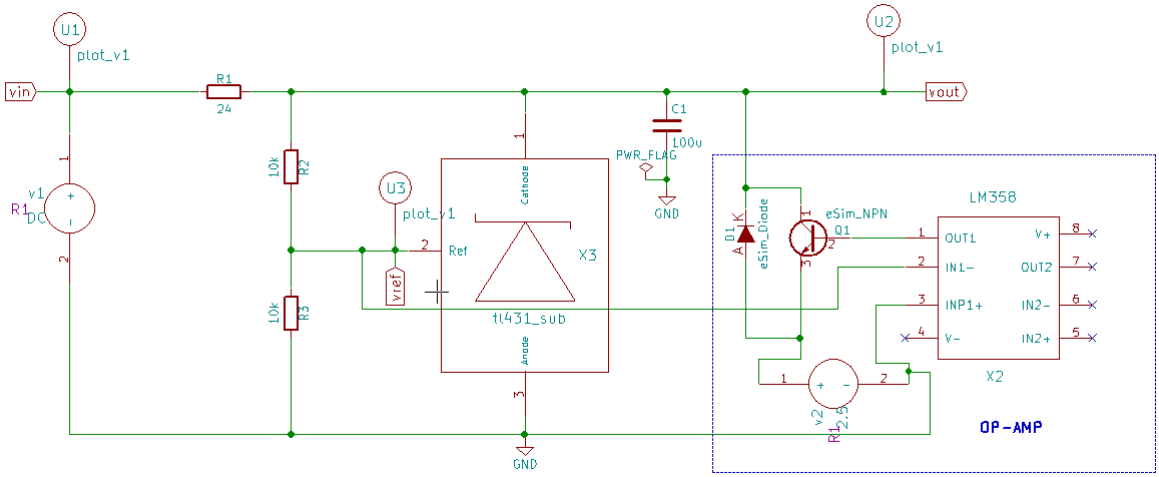

Figure 4.2: Schematic diagram of Testbench
(Shunt voltage regulator as a application)

4.4 Simulation Output

The TL431 maintains a fixed voltage of 2.5V between its Reference and Cathode pins. A resistor divider (R2 and R3) is used to program the output voltage as:

$$V_{\text{OUT}} = V_{\text{REF}} \left(1 + \frac{R_3}{R_2}\right)$$

$$\text{Given } V_{\text{REF}} = 2.5\,\text{V}, \quad R_2 = R_3 = 10\,\text{k}\Omega$$

$$V_{\text{OUT}} = 2.5 \times \left(1 + \frac{10k}{10k}\right) = 5\,\text{V}$$

Observation and Calculations

- Input Voltage, $V_{\text{in}} = 24.423\,\text{V}$
- Reference Voltage, $V_{\text{ref}} = 2.2561\,\text{V}$
- Output Voltage (Practical), $V_{\text{out (practical)}} = 4.5235\,\text{V}$
- Resistors used: $R_1 = R_2 = 10\,\text{k}\Omega$

The practical output voltage of a shunt regulator is given by:

$$V_{\text{out}} = V_{\text{ref}} \left(1 + \frac{R_1}{R_2}\right)$$

Substituting the known values:

$$V_{\text{out}} = 2.2561 \left(1 + \frac{10k}{10k}\right) = 2.2561 \times 2 = 4.5122\,\text{V}$$

Conclusion: The calculated practical value $V_{\text{out}} = 4.5122\,\text{V}$ is very close to the theoretical value $5\,\text{V}$, showing good result.

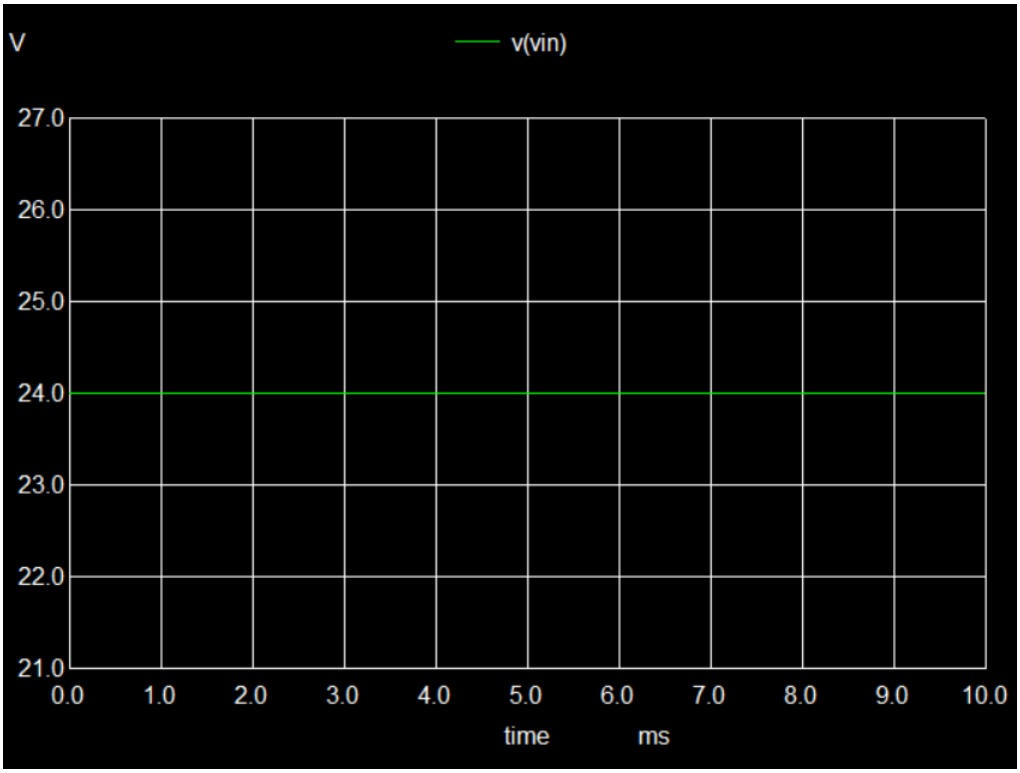

Figure 4.3: Input Voltage

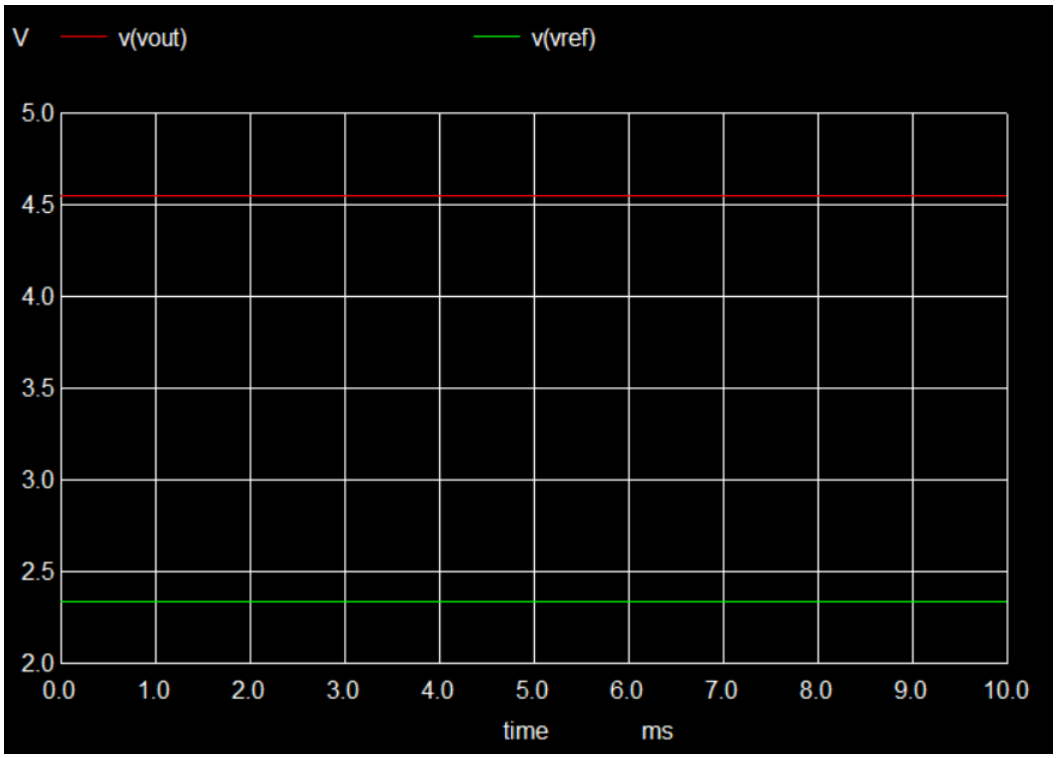

Figure 4.4: Voltage Reference and Voltage Output Plot

Chapter 5

IC ULN2004

5.1 Circuit Details

The ULN2004 is an integrated circuit (IC) consisting of seven Darlington pairs, which are used as high-current drivers. It is commonly used to interface TTL/CMOS logic to high-voltage loads such as relays, motors, lamps, or LEDs.

It is part of the ULN200x series:

- ULN2003: For 5V logic (TTL/CMOS)
- ULN2004: For 6–15V logic input (suitable for CMOS)

5.2 Pinout Diagram

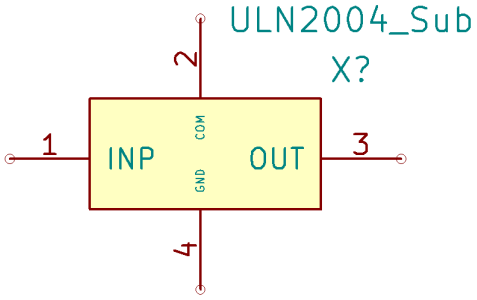

Figure 5.1: Pinout Diagram of IC ULN2004

Pin	Type	Description
INP	Input	Logic input signal to control the Darlington pair
OUT	Output	Open-collector output connected to the load
GND	Ground	Common ground for current sinking
COM	Power	Common freewheeling diode connection for inductive loads

Table 5.1: Pin Description of Single Darlington Pair (ULN2004)

5.3 Testbench circuit for IC ULN2004

- Simulates a single Darlington driver stage of the **ULN2004 IC**.
- A **pulse voltage input (Vin)** is applied to the **INP** pin to test switching behavior.
- The **OUT** pin drives a resistive load connected to a **12V DC supply** via a **1kΩ pull-up resistor**.
- The **COM** pin is connected to 12V to activate the **internal flyback diode** for inductive load protection.
- **Voltage probes** are placed at input and output to monitor the switching waveform during simulation.

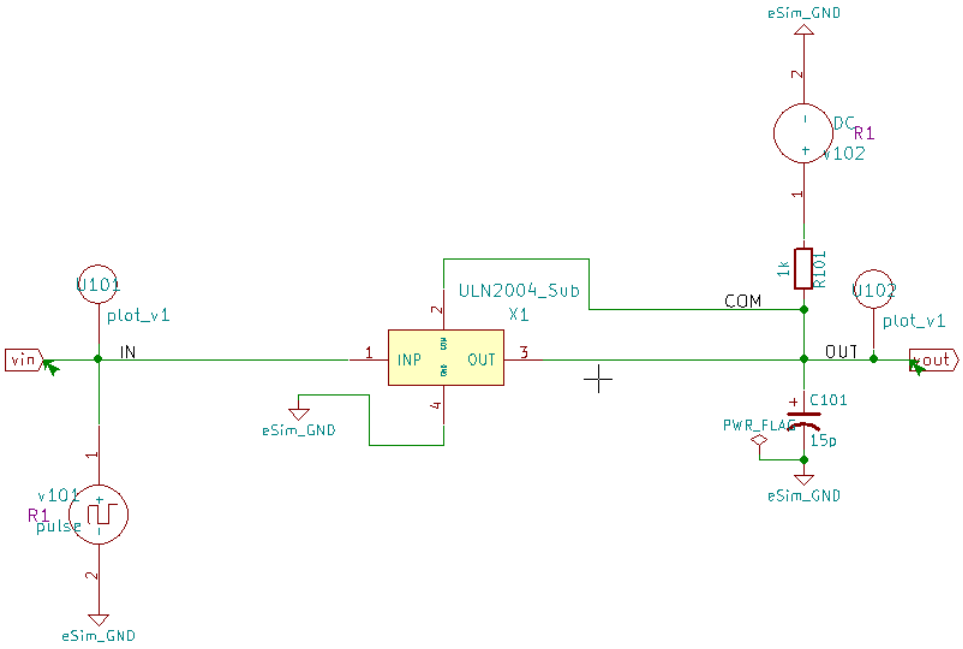

Figure 5.2: Schematic diagram of Testbench IC TL431

5.4 Simulation Output

- The waveform shows the input and output response of the ULN2004 single Darlington pair testbench.
- The **green signal** represents the input pulse (`Vin`), shifted by +6 V for visibility. It alternates between 0 V and 5 V.
- The **red signal** shows the output voltage (`Vout`) at the OUT pin.
- When the **input is high (logic 1)**, the Darlington pair turns **ON**, and the output is pulled **low (near 0 V)**.
- When the **input is low (logic 0)**, the Darlington pair turns **OFF**, and the output is pulled **high (∼12 V)** through the pull-up resistor.
- This confirms the correct **inverting behavior** of the ULN2004's open-collector output and verifies proper operation of the Darlington stage and flyback diode.

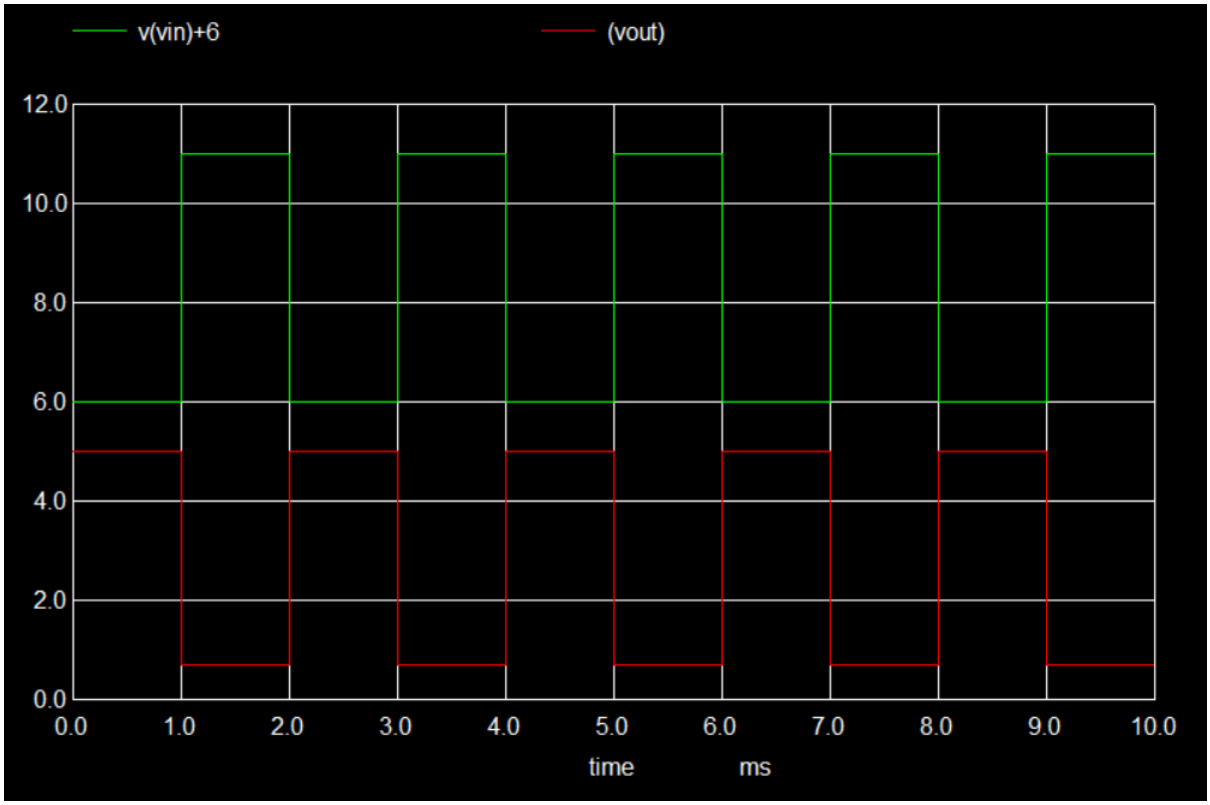

Figure 5.3: Simulation Output of IC ULN2004

Chapter 6

IC 74VHC373-D

6.1 Circuit Details

The VHC373 is an advanced high speed CMOS octal D-type latch with 3-STATE output fabricated with silicon gate CMOS technology. It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

This 8-bit D-type latch is controlled by a latch enable input (LE) and an output enable input (OE). The latches appear transparent to data when latch enable (LE) is HIGH. When LE is LOW, the data that meets the setup time is LATCHED. When the OE input is HIGH, the eight outputs are in a high impedance state. An input protection circuit ensures that 0 V to 5.5 V can be applied to the input pins without regard to the supply voltage. This device can be used to interface 5 V to 3 V systems and two supply systems such as battery back up. This circuit prevents device destruction due to mismatched supply and input voltages.

6.2 Pinout Diagram

- High Speed: $t_{PD} = 5.0$ ns (Typ) at $V_{CC} = 5$ V
- High Noise Immunity: $V_{NIH} = V_{NIL} = 28\% \, V_{CC}$ (Min)
- Power Down Protection is Provided on All Inputs
- Low Noise: $V_{OLP} = 0.6$ V (Typ)
- Low Power Dissipation: $I_{CC} = 4 \, \mu$A (Max) at $T_A = 25 \, ^\circ$C
- Pin and Function Compatible with 74HC373
- This is a Pb-Free Device

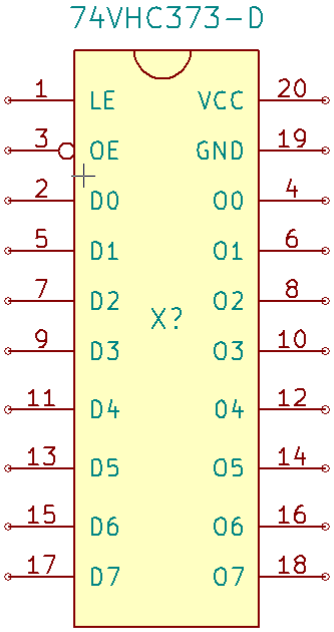

Figure 6.1: Pinout Diagram IC 74VHC373-D

6.3 Testbench circuit for IC 74VHC373-D

This testbench demonstrates the latching behavior of an octal D-type transparent latch, using the 74VHC373 IC. The goal is to validate how input data is latched or passed to the output based on control signals (LE and OE) under digital simulation in eSim.

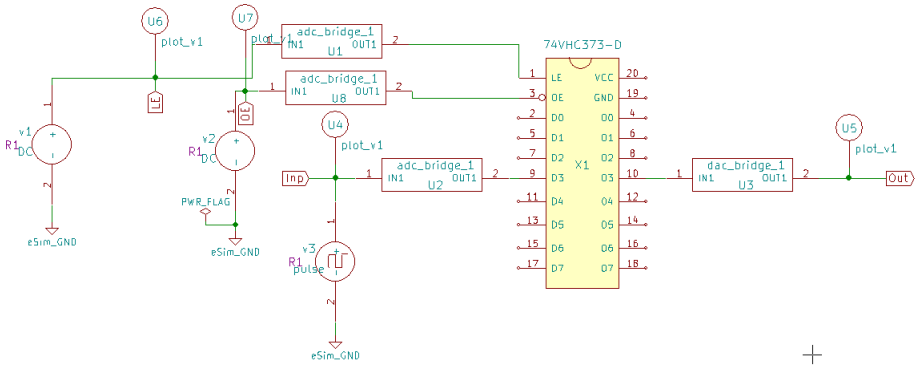

Figure 6.2: Schematic diagram of Testbench IC 74VHC373-D

6.4 Simulation Output

The **VHC373** contains eight D–type latches with **3–STATE** standard outputs. When the **Latch Enable (LE)** input is **HIGH**, data on the $\mathbf{D_n}$ inputs enters the latches. In this condition, the latches are **transparent**, i.e., a latch output will change state each time its D input changes.

When **LE** is **LOW**, the latches store the information that was present on the D inputs a setup time preceding the **HIGH–to–LOW** transition of **LE**. The **3–STATE** standard outputs are controlled by the **Output Enable (OE)** input.

When **OE** is **LOW**, the standard outputs are in the **2–state mode**. When **OE** is **HIGH**, the standard outputs are in the **high impedance mode**, but this does not interfere with entering new data into the latches.

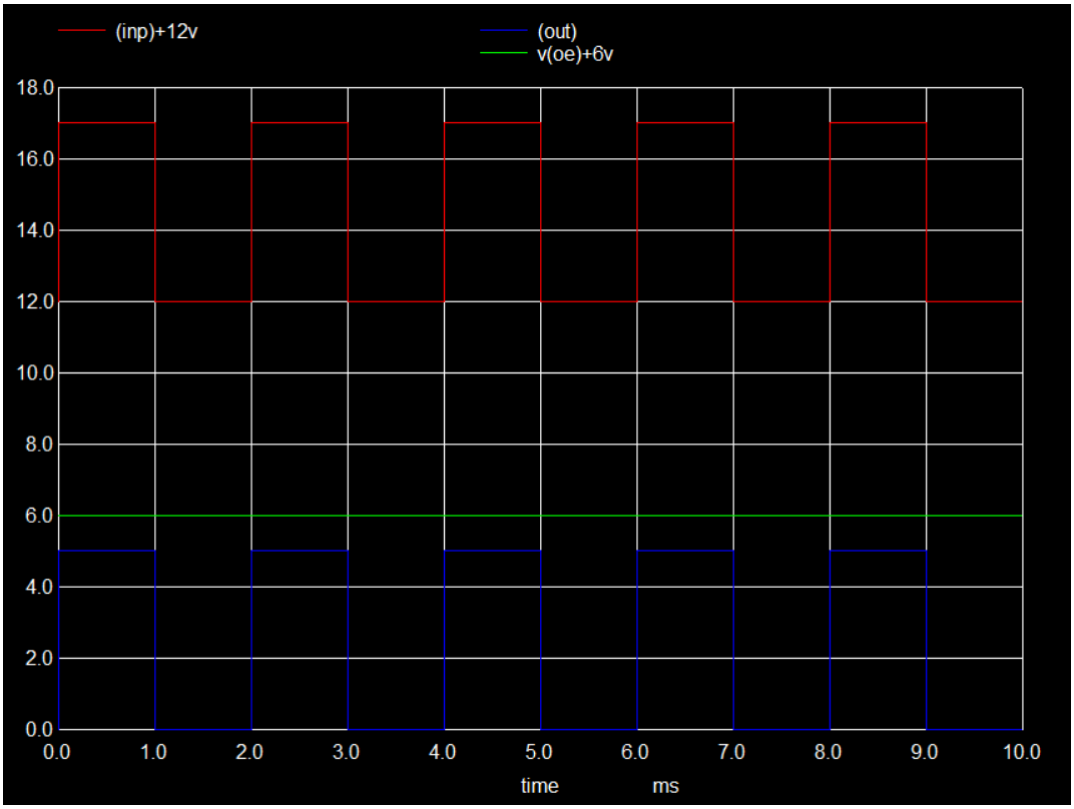

Figure 6.3: Simulation Output of IC 74VHC373

Chapter 7

IC CA3160

7.1 Circuit Details

The CA3160 is a BiMOS operational amplifier combining the advantages of PMOS and CMOS transistors. It features a PMOS input stage for high input impedance and a CMOS output stage that allows rail-to-rail output swing. It can operate from single or dual power supplies and offers low input current, high gain, and fast slew rate. It includes provisions for offset nulling, frequency compensation, and output strobing.

7.2 Transistor level schematic diagram

The internal block diagram of the CA3160 typically includes:

- A differential PMOS input pair
- A bipolar current mirror load
- A bipolar voltage gain stage with frequency compensation
- A CMOS push-pull output stage
- Internal bias circuits for setting operating currents

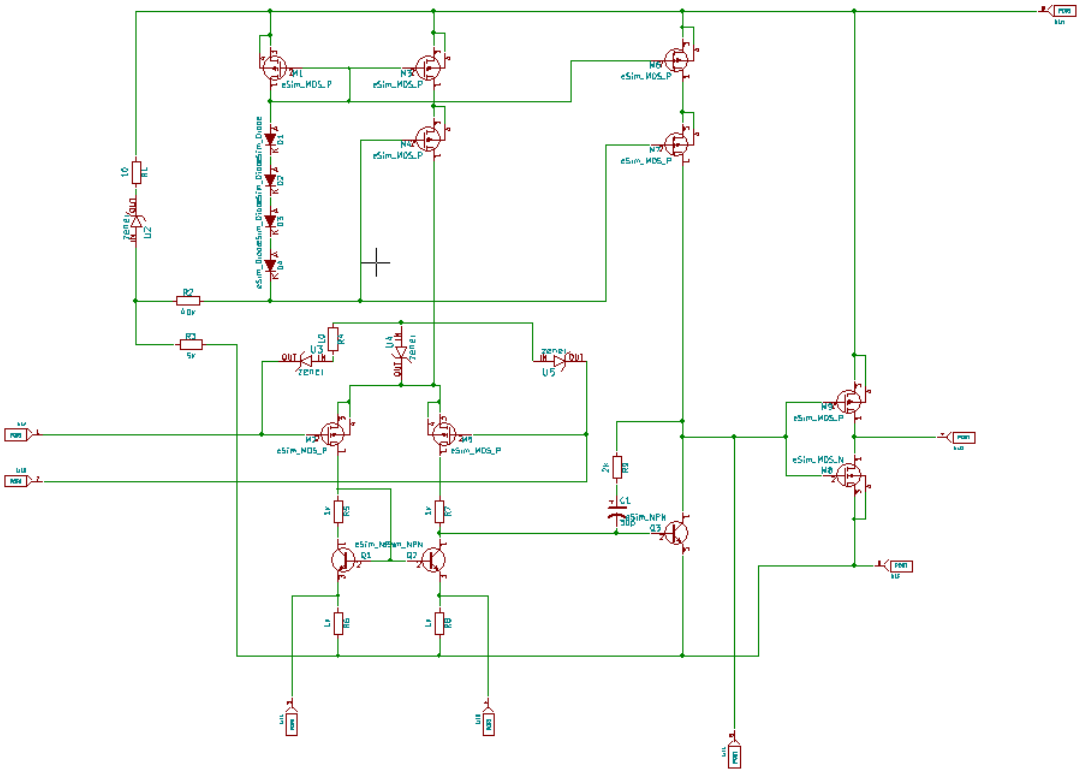

Figure 7.1: Gate level schematic of IC CA3160A

7.3 Pinout diagram

Pin No.	Pin Name	Function
1	IN+	Non-inverting input
2	IN-	Inverting input
3	OFF_NULL	Offset voltage adjustment
4	STROB	Output strobe or second offset null
5	V-	Negative supply (GND)
6	OUT	Output
7	V+	Positive supply
8	NC / COMP	Compensation or No Connect

Table 7.1: CA3160 Pin Description

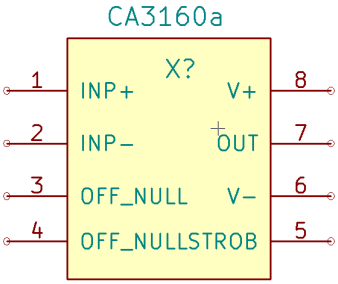

Figure 7.2: Pinout diagram of IC CA3160A

7.4 Testbench circuit for IC CA3160A

- A sine wave is applied at the non-inverting input (IN+) of the CA3160 via a 10kΩ resistor.
- The inverting input (IN-) is connected to a feedback network consisting of a 100kΩ resistor and a parallel RC circuit (2kΩ and 0.1μF), forming a basic integrator/stabilizer.
- Offset null pins (3 and 4) are connected for proper balance using standard offset configuration.
- V^+ and V^- provide the required power supply for the IC.
- Output is taken from pin 6 and connected to a 0.01μF capacitor and a resistive load to ground.
- Voltage probes are placed at the input and output to observe the amplifier's response to the input signal.

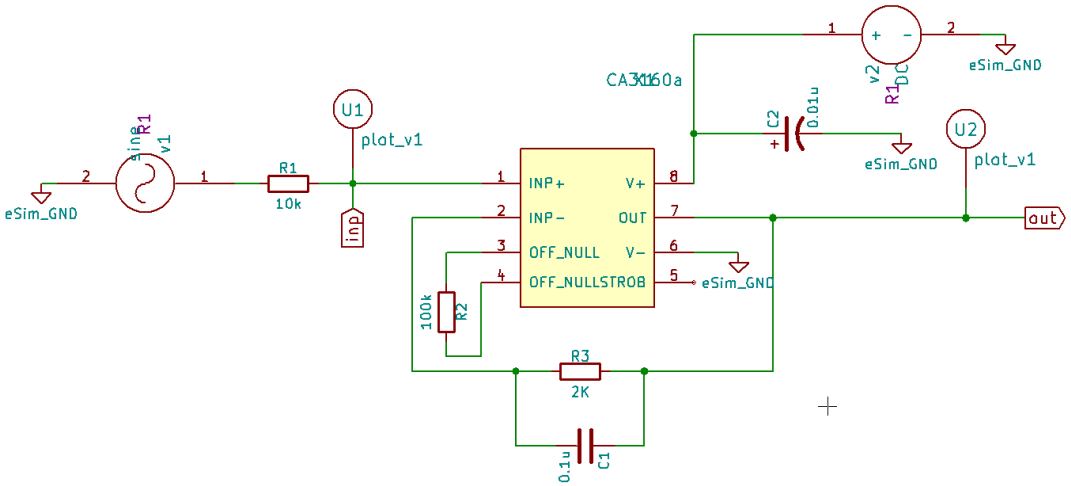

Figure 7.3: CA3160 Testbench Circuit

7.5 Simulation output

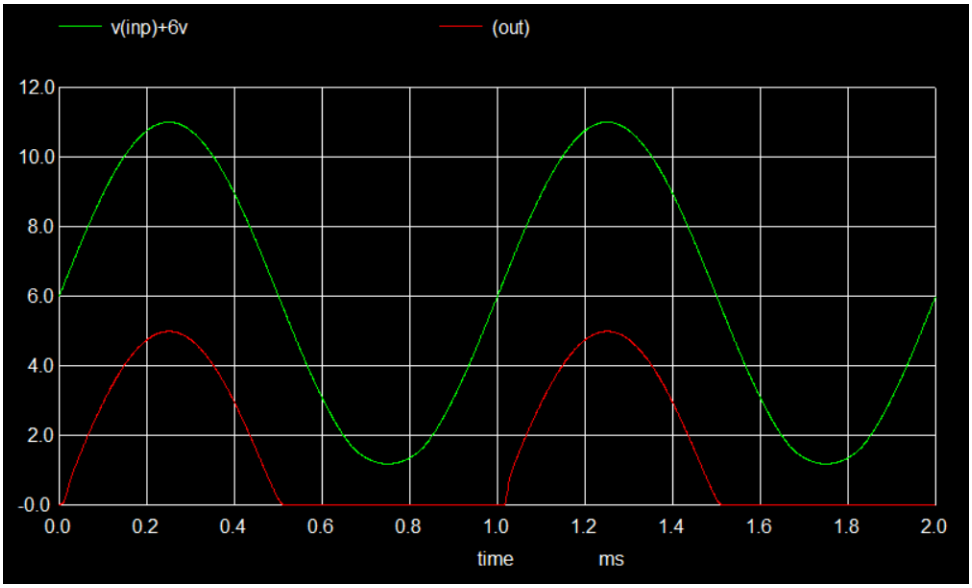

Figure 7.4: Simulation Output of CA3160 Testbench

- The green waveform represents the input voltage (V_{inp}) shifted by +6V for visibility.
- The red waveform shows the output voltage (V_{out}) from the CA3160.
- The output follows the positive half-cycles of the input signal, indicating proper amplification and positive-phase response.
- During the negative half-cycle of the input, the output voltage drops to 0V, showing that the IC operates in a single-supply configuration and clips the negative output.
- The gain appears to be less than 1 due to the feedback network and resistor values used in the testbench.
- The output signal shape remains sinusoidal in the active region, confirming linear operation within that range.

Chapter 8

IC LM13600

8.1 Circuit Details

The LM13600 series consists of two current controlled transconductance amplifiers each with differential inputs and a push-pull output. The two amplifiers share common supplies but otherwise operate independently. Linearizing diodes are provided at the inputs to reduce distortion and allow higher input levels. The result is a 10 dB signal-to-noise improvement referenced to 0.5 percent THD. Controlled impedance buffers which are especially designed to complement the dynamic range of the amplifiers are provided.

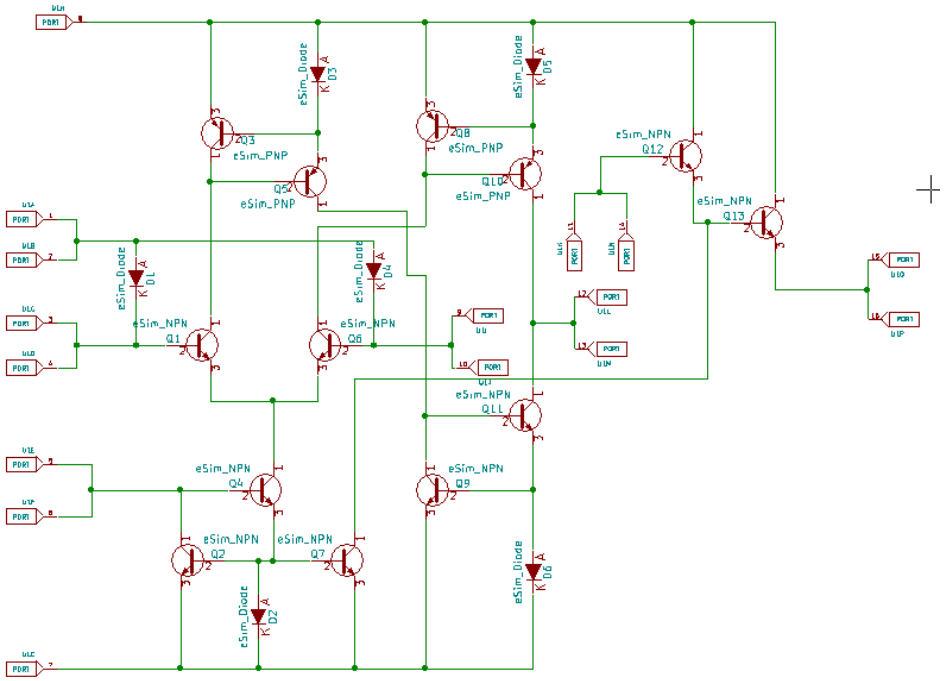

Figure 8.1: Transister level schematic circuit

8.2 Test Circuit for IC LM13600

The given circuit showcases a classic application of the LM13600 as an amplitude modulator. This circuit utilizes the voltage-controllable gain characteristic of the OTA to impress a lower frequency modulating signal onto a higher-frequency carrier signal.

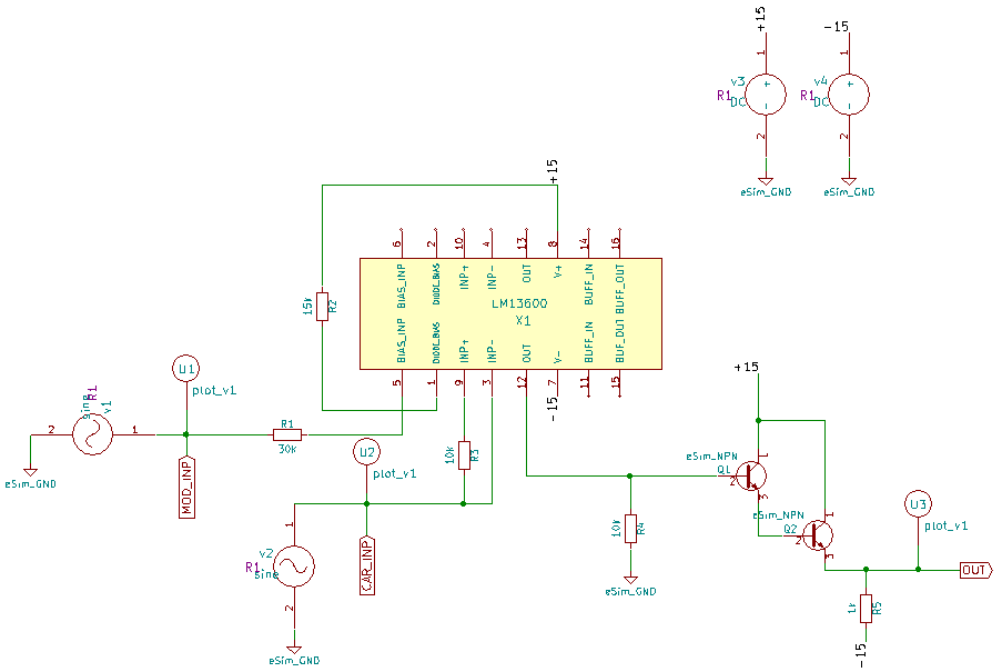

Figure 8.2: Test circuit diagram for IC LM13600

Pin (Amp 1)	Pin (Amp 2)	Function
1	16	Amplifier Bias Input (I_{ABC})
2	15	Diode Bias
3	14	(+) Input
4	13	(-) Input
5	12	Output
6	11	V^- (Negative Supply)
7	10	Buffer Output
8	9	Buffer Input

Table 8.1: LM13600 Pin Functions (per amplifier)

8.3 Simulation Output

The simulation results precisely match the expected behavior of the LM13600 configured as an amplitude modulator. The OTA acts as a multiplier, effectively multiplying the carrier signal by the modulating signal. The resulting output is a DSB-SC AM signal, where the amplitude of the carrier is controlled by the modulating input, and the phase of the carrier indicates the polarity of the modulating signal.

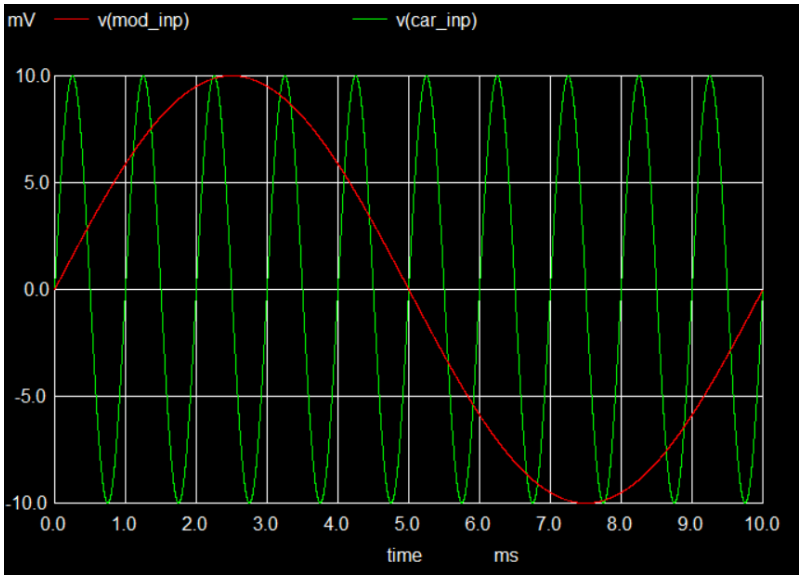

Figure 8.3: Input signals : Carrier signal and Modulating signal

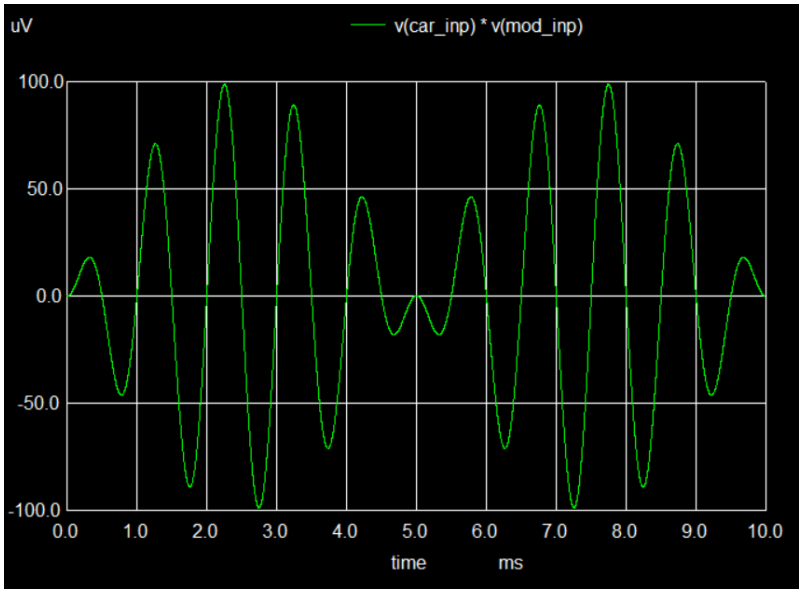

Figure 8.4: Output signals : Amplitude Modulated Signal

Chapter 9

IC CD4066B

9.1 Circuit Details

The CD4066BC is a versatile integrated circuit that contains four independent bilateral switches. These switches are designed for the transmission or multiplexing of both analog and digital signals. A key characteristic of the CD4066BC is its low "ON" state resistance, which remains relatively constant across the full range of the input signal. This device is pin-for-pin compatible with the older CD4016BC, but offers significantly improved performance in terms of its lower and more stable ON resistance.

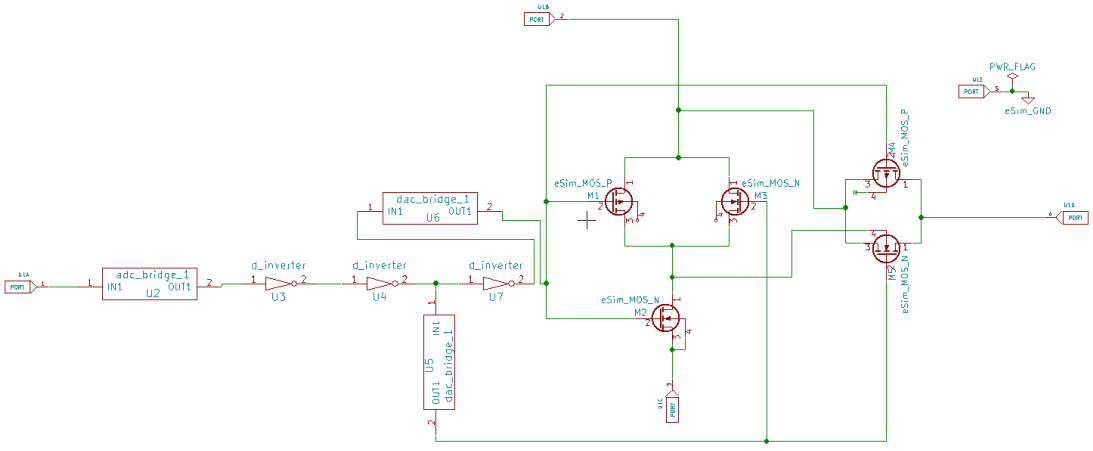

Figure 9.1: Transistor level schematic circuit

9.2 Test Circuit for IC CD4066B

When the control line VC(1) is set to VDD, the corresponding switch (Switch 1) is turned ON, allowing the input signal at VIS(1) to be transmitted to the output VQS(1). The rest of the switches remain off. This behavior is akin to a digitally controlled analog multiplexer.

This configuration is widely used in analog signal routing, audio switching, and measurement systems where multiple analog signals need to be selectively routed to a common output.

- **VIS(1)** is the input analog signal.
- **VC(1)** is the digital control line, set to $V_{\mathrm{DD}} = +5\,\mathrm{V}$ to activate channel 1.
- $V_{\mathrm{DD}} = +5\,\mathrm{V}$, $V_{\mathrm{SS}} = -5\,\mathrm{V}$: Dual supply is used to allow full swing analog operation.
- The output **VQS(1)** is connected to a $1\,\mathrm{k\Omega}$ load resistor R_L to ground.

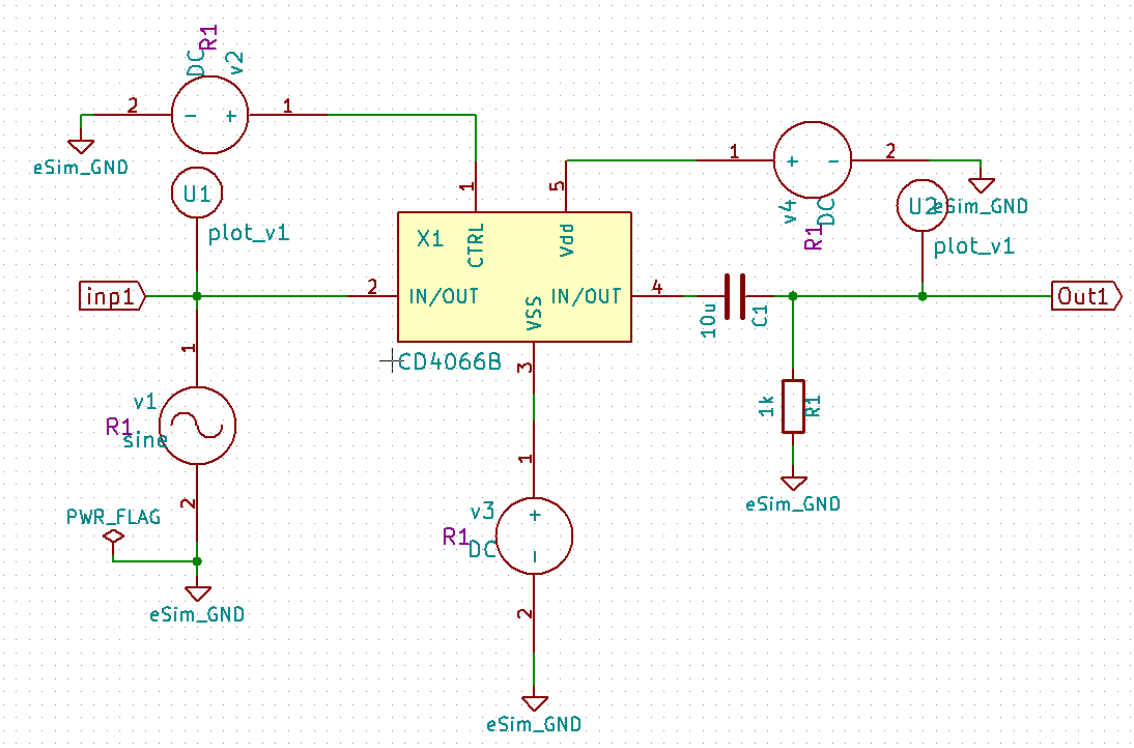

Figure 9.2: Test circuit diagram for IC CD4066B

9.3 Simulation Output

- The output signal is clearly attenuated compared to the input, suggesting inherent resistance and non-linearity within the analog switch.
- Minor distortions in the red waveform are indicative of crosstalk, signal leakage, or parasitic capacitance effects within the IC.
- Crosstalk is evident in the non-linear transitions and clipped peaks, even though only one path is enabled, showing that adjacent inactive paths may still influence the active channel.

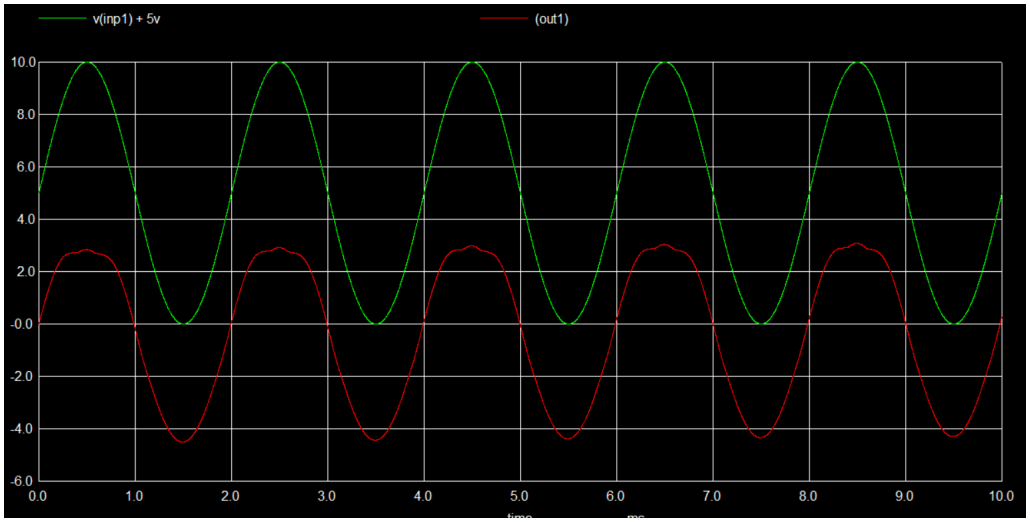

Figure 9.3: Crosstalk of single switch

- Parasitic capacitance between adjacent switches.
- Finite isolation resistance between control lines and analog paths.
- Layout-dependent coupling in integrated circuits.

This simulation helps in understanding the limitations of such analog switches in precision applications and the need for careful channel isolation in sensitive analog designs.

Chapter 10

IC SN74LVC257A

10.1 Circuit Details

The SN74LVC257A is a high-speed CMOS quad 2-to-1 multiplexer with 3-state outputs. It selects data from two 4-bit sources under the control of a common select input (A/B) and outputs the selected data on four output lines. The outputs can be disabled via an active-low output enable (OE) signal, placing them in a high-impedance state. This IC operates over a voltage range of 1.65V to 3.6V and is suitable for both 3.3V and 5V logic inputs, making it ideal for signal switching, bus multiplexing, and level translation in mixed-voltage systems.

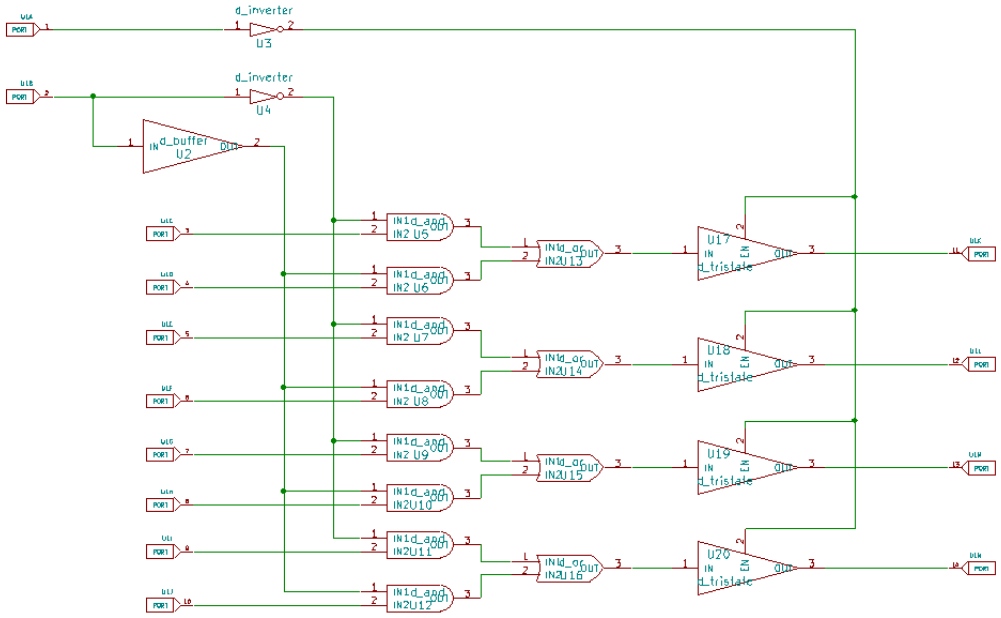

Figure 10.1: Transistor level schematic circuit

10.2 Test circuit for IC SN74LVC257A

- The testbench simulates the SN74LVC257A 2-to-1 multiplexer.
- Two pulse sources (`v1` and `v2`) are used as inputs to A and B lines via ADC bridges.
- The select pin (A/B) is driven by a third pulse source to switch between A and B inputs.
- Output Enable (OE) is kept low to enable the outputs.
- The selected output is passed through a DAC and observed using a plot block.

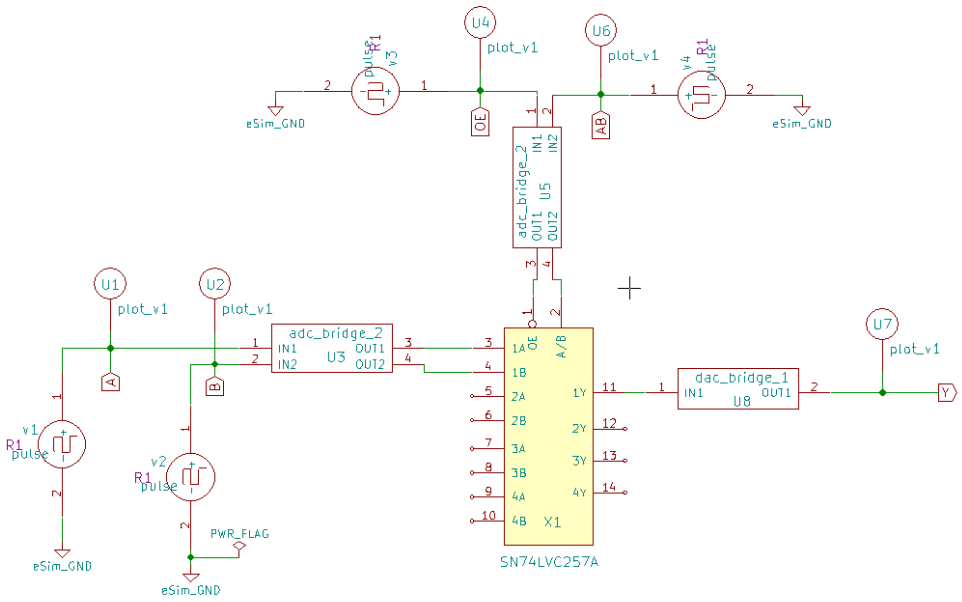

Figure 10.2: Test circuit diagram for IC SN74LVC257A

Pin	Name	Function	Pin	Name	Function
1	1A	Channel 1 input A	9	4B	Channel 4 input B
2	1B	Channel 1 input B	10	4Y	Channel 4 output
3	2A	Channel 2 input A	11	3Y	Channel 3 output
4	2B	Channel 2 input B	12	2Y	Channel 2 output
5	3A	Channel 3 input A	13	1Y	Channel 1 output
6	3B	Channel 3 input B	14	OE	Output Enable (active low)
7	GND	Ground	15	A/B	Select input
8	4A	Channel 4 input A	16	VCC	Power supply

Table 10.1: Pin Functions of SN74LVC257A

10.3 Simulation Output

Inputs can be driven from either 3.3 V or 5 V devices. This feature allows the use of these devices as translators in a mixed 3.3 V and 5 V system environment. The device features a maximum t_{pd} of 4.6 ns, allowing it to be used in high-speed applications as well.

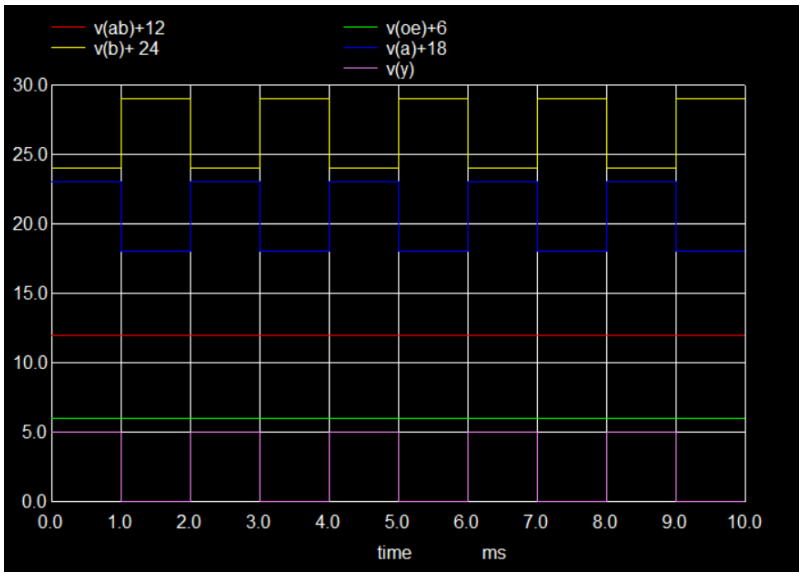

Figure 10.3: **Output waveform when $\overline{\text{OE}}$ and $\overline{\text{A/B}}$ are LOW**

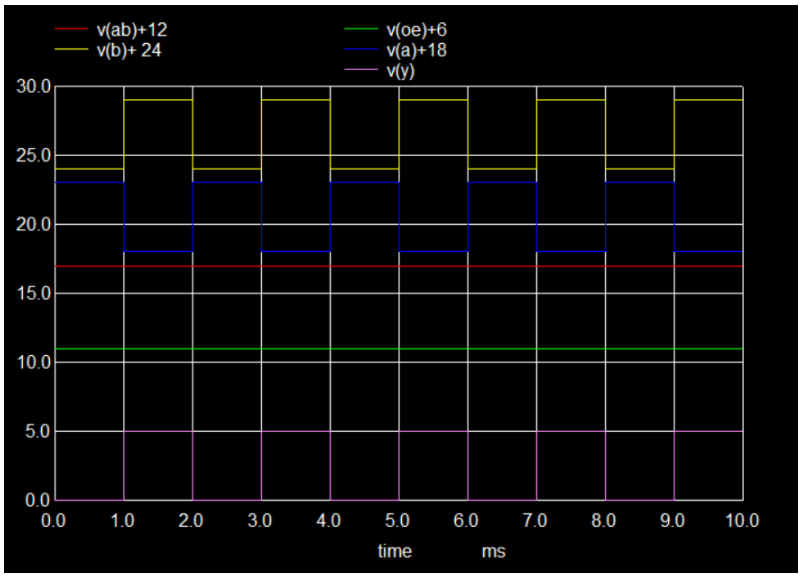

Figure 10.4: **Output waveform when $\overline{\text{OE}}$ and $\overline{\text{A/B}}$ are HIGH**

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