Semester Long Internship Report

On

Adding ICs as Subcircuits in eSim Library

Submitted by

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Under the guidance of

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Acknowledgment

I am sincerely thankful to the FOSSEE team at IIT Bombay for offering me the opportunity to be part of this internship. I would like to express my deepest gratitude to Prof. Kannan M. Moudgalya for his guidance throughout the internship. This experience has been valuable in enhancing my technical skills and understanding of open-source EDA tools and circuit simulation.

It has served as a stepping stone for my technical growth in the domain of electronics. I am particularly grateful to Mr. Sumanto Kar and Dr. Ritu Pahwa, for their expert guidance, continuous support, and insightful feedback throughout the duration of the internship. Their mentorship was instrumental in deepening my knowledge of circuit design and simulation using eSim. Their insights and support helped me navigate challenges.

I extend my thanks to the developers and community behind the eSim project for making such a powerful simulation tool freely accessible, and for their continued efforts in promoting open-source electronics design.

I am grateful to my faculty members, peers, and fellow interns for their constant encouragement and support throughout this journey. This experience has not only improved my technical skills but also instilled in me a deeper appreciation for collaborative learning and open-source contributions.

Contents

Chapter 1

Introduction

The electronics industry relies heavily on the design, simulation, and verification of circuits before physical implementation.

Electronic Design Automation (EDA) tools play a crucial role in ensuring design accuracy and efficiency. eSim, an open-source EDA tool developed by FOSSEE, IIT Bombay, offers a powerful platform for circuit design and simulation. It integrates KiCad for schematic capture and PCB design with Ngspice for simulation, providing an end-to-end solution for electronics engineers and students.

This internship was undertaken with the objective of gaining hands-on experience in circuit simulation using eSim. During the internship, I explored various features of the software, including schematic creation, SPICE simulation, netlist generation, and waveform analysis. The focus was on understanding the workflow of circuit design using open-source tools and applying this knowledge to practical projects and exercises.

The FOSSEE (Free/Libre and Open Source Software for Education) initiative is an effort to enhance educational quality by promoting the adoption of open-source software tools.

The eSim tool, developed as part of the FOSSEE project, provides an integrated platform combining schematic design and simulation. Built on the backbone of Ngspice, eSim is especially useful for engineering students and educators aiming to understand electronics without the cost barriers.

eSim is built by integrating following tools:

- KiCad: Used for drawing circuits, layout design, and component management.
- Ngspice: A circuit simulator capable of handling DC, transient, and AC analysis.
- KiCad to Ngspice Converter: This module helps in mapping the design from KiCad to simulation by setting up analysis parameters and managing device models. 5

- Model Builder: Supports creation of new device models for components like diodes, BJTs, MOSFETs, JFETs, IGBTs, and magnetic cores.
- Subcircuit Builder: Allows users to develop reusable subcircuits which can be used across different projects.
- NGHDL: Facilitates mixed-signal simulation using VHDL.
- NgVeri: Enables simulation using Verilog/ System Verilog.

The internship through FOSSEE aims to not only educate but also enable students to contribute meaningfully to the open-source system while gaining practical skills in circuit design and simulation.

The report outlines the activities performed during the internship, key learnings, challenges encountered, and the skills acquired. It highlights the importance of adopting open-source alternatives in the field of electronics and reflects on how eSim contributes to self-reliant, cost-effective design practices in both academic and professional domains.

Chapter 2

Workflow

The process which was followed can be outlined as follows:

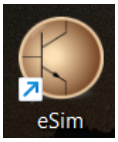
2.1 Orientation and Tool Familiarization:

An introductory session was conducted to understand the work process. Tutorials and documentation provided by FOSSEE were referred during this phase.

2.2 Approach

Using tutorials, creation of subcircuit in eSim was done which involved following steps:

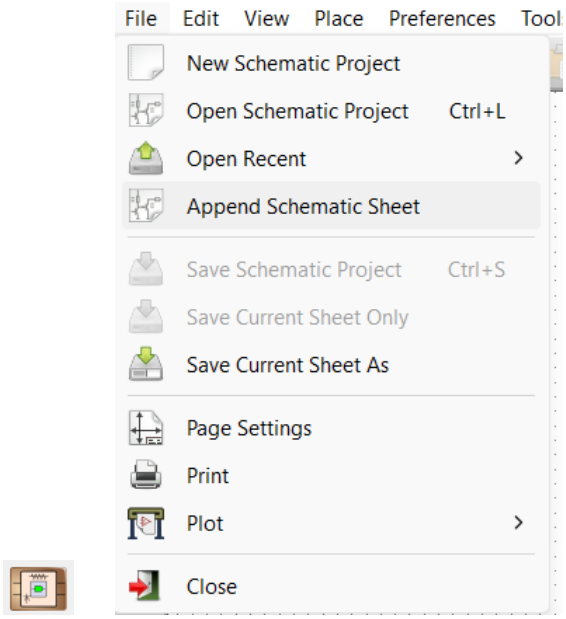
- Opening eSim and selecting the default workspace and location.



- Creating a new project for each IC in the default workspace where we can store the designed circuits.

- Opening the schematic editor and building the circuit as per the datasheet.

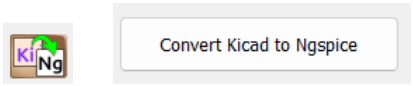
- Use the schematic and update the sheet of subcircuit by creating new subcircuit.



- Annotating the schematic symbols to assign identifiers to all components.

- Generating a netlist, for simulation. The netlist describes all the electrical connections and components in a format readable by the SPICE engine.

- Converting the KiCad schematic to an NgSpice compatible format.



- Creating a symbol for the subcircuit using the Symbol Editor and setting up the pin configuration.

- Designing a test circuit for simulation and validating the results against the datasheet specifications.

Chapter 3

Subcircuits

The IC subcircuits completed are listed below:

Sr. No.	IC Number	Description
1	SN74ALS520N	8-bit magnitude comparator
2	SN74LS42	4-line BCD to 10-line decimal decoder
3	SN74LS151	8:1 Selector / Multiplexer
4	SN74LS148	8:3 Encoder
5	CY74FCT480T	Dual 8-bit parity checker / generator
6	HD74LS139	Dual 2:4 decoder / demultiplexer
7	DM7447A	BCD to 7-segment decoder / driver
8	SN74HC688	8-bit magnitude comparator
9	HD74HC149	8:8 Line priority encoder
10	SN74LVC1G29	2-of-3 decoder / demultiplexer

Table 3.1: List of ICs and their descriptions

3.1 SN74ALS520N- 8-bit Magnitude Comparator

3.1.1 Description

The SN74ALS520N is a high-speed TTL 8-bit magnitude comparator used to compare two 8-bit binary words and determine whether one is equal to the other.

3.1.2 Key Features

- Fully parallel 8-bit comparison
- Expandable for longer word comparison
- High-speed TTL compatibility
- Low power consumption

3.1.3 Input and Output Relationship

- **Inputs: Two 8-bit words (A0-A7 and B0-B7), and Enable (G)**
- **Outputs: A = B**
- Enable is active low; when high, output is low.
- High output is observed when inputs are equal.
- Low output is observed in case of inequality.

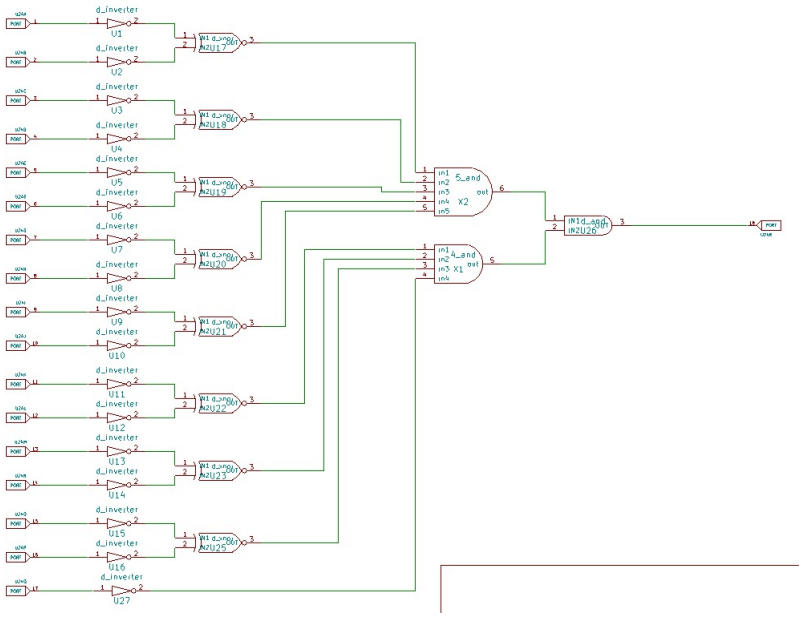


Figure 3.1: Schematic of SN74ALS520N

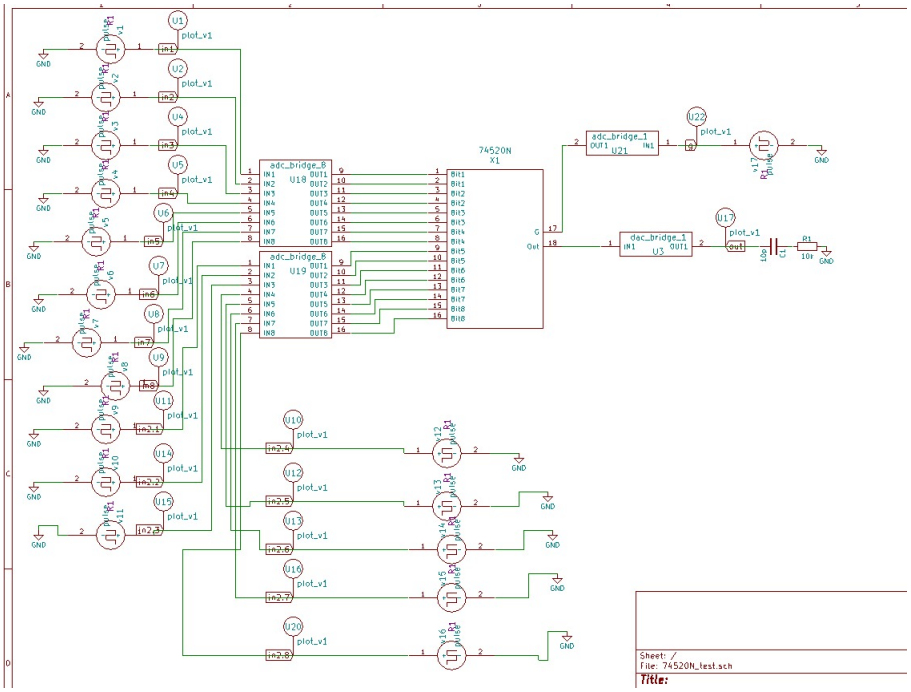


Figure 3.2: Test Circuit of SN74ALS520N

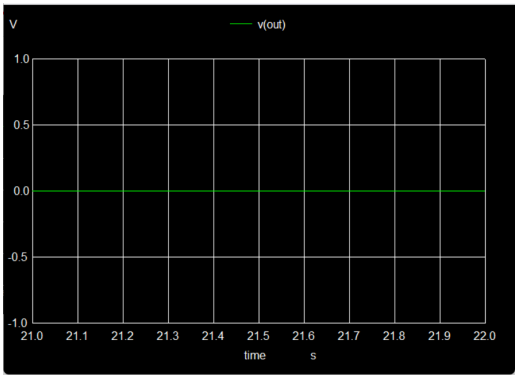


Figure 3.3: Unequal bits

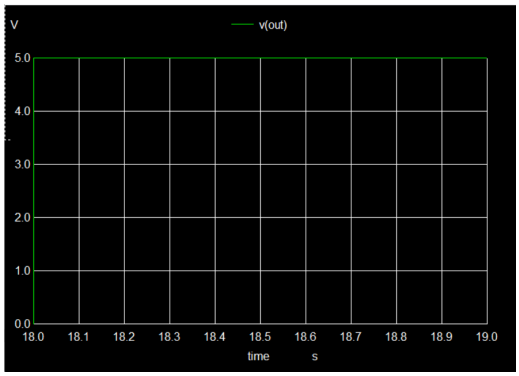


Figure 3.4: Equal bits

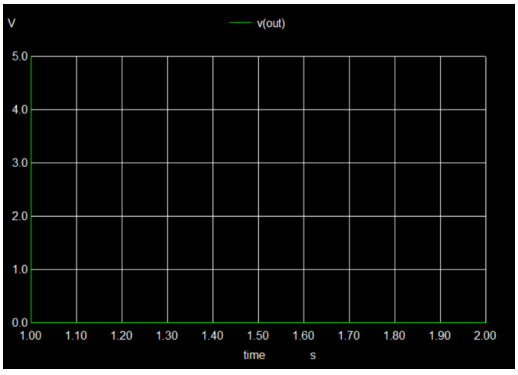


Figure 3.5: Enable High

3.2 SN74LS42- 4:10 BCD to decimal decoder

3.2.1 Description

The SN74LS42 is a BCD to decimal decoder that converts a 4-bit binary-coded decimal input into one of ten active-low outputs.

3.2.2 Key Features

- Converts BCD (0–9) to 10-line decimal output
- Active-low outputs
- TTL-compatible inputs and outputs
- Ideal for digital display and control applications
- High fan-out capability

3.2.3 Input and Output Relationship

- **Inputs: 4-bit BCD (A, B, C, D)**
- **Outputs: OUT1 to OUT10**
- Output is LOW at a time corresponding to the binary input value, others remain HIGH.

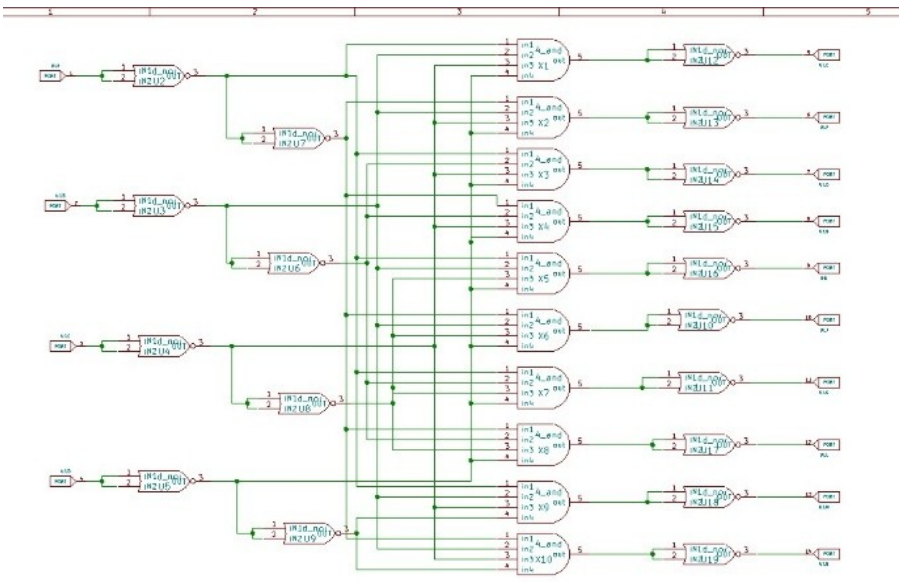


Figure 3.6: Schematic of SN74LS42

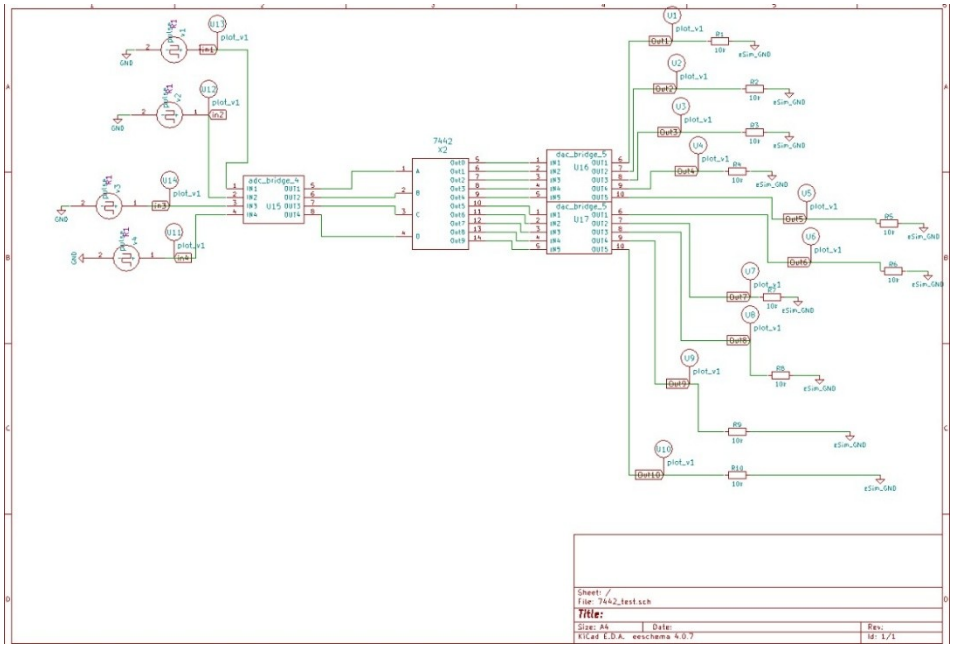


Figure 3.7: Test Circuit of SN74LS42

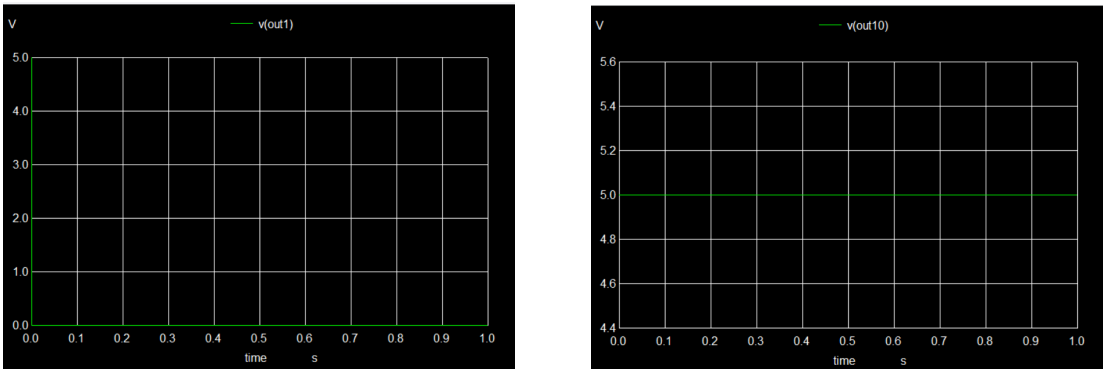


Figure 3.8: Input is 0000 all the outputs from OUT2 to OUT10 are high except 0

3.3 SN74LS151 - 8:1 Multiplexer

3.3.1 Description

The SN74LS151 is an 8-input multiplexer that selects one of eight inputs and transmits it to the output based on three select lines.

3.3.2 Key Features

- 8-input data selector/multiplexer
- 3-bit binary select inputs
- Inverted and non-inverted outputs
- TTL-compatible logic
- Enable pin for output control

3.3.3 Input and Output Relationship

- **Inputs:** D0–D7 (data), A–C (select), Enable (active-low)
- **Outputs:** Y (selected input), W (inverted output)
- Selected input is routed to output Y when Enable is active

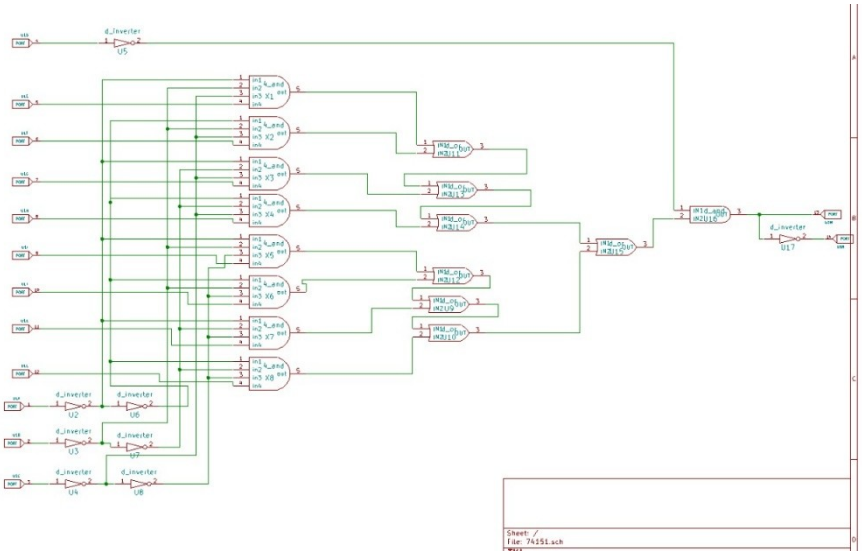


Figure 3.9: Schematic of SN74LS151

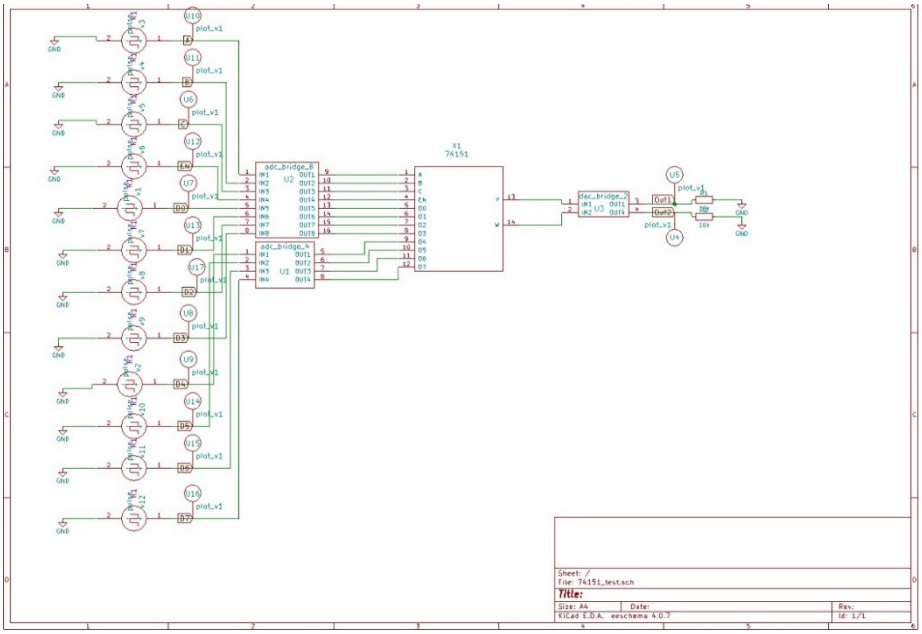


Figure 3.10: Test Circuit of SN74LS151

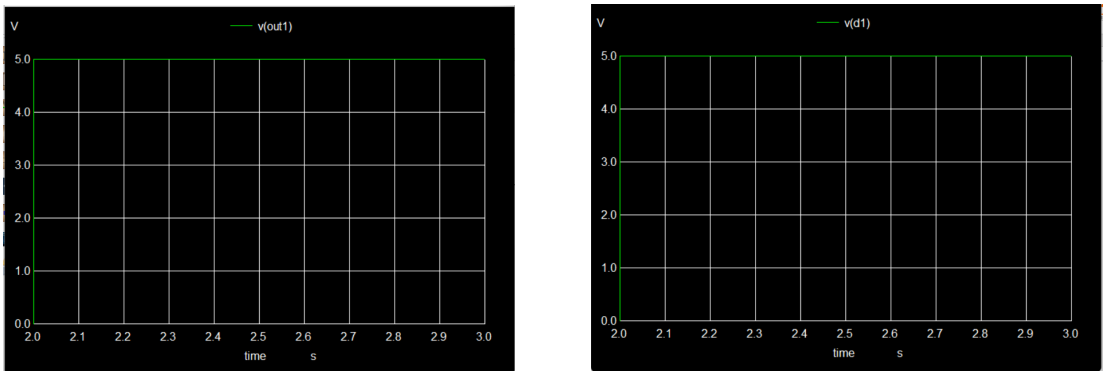


Figure 3.11: A=High, B=Low, C=Low, Output should be D1

3.4 SN74LS148 - 8:3 Priority Encoder

3.4.1 Description

The SN74LS148 is an 8-to-3 priority encoder that encodes the highest-priority active-low input into a 3-bit binary output.

3.4.2 Key Features

- Priority encoding (I7 has highest priority)
- Active-low inputs and outputs
- Cascadable design
- TTL-compatible logic
- Group select and enable output signals

3.4.3 Input and Output Relationship

- **Inputs:** I0–I7 (active-low), EI (Enable input)
- **Outputs:** A0, A1, A2 (binary), GS (group select), EO (enable output)
- Outputs encode the highest-priority LOW input

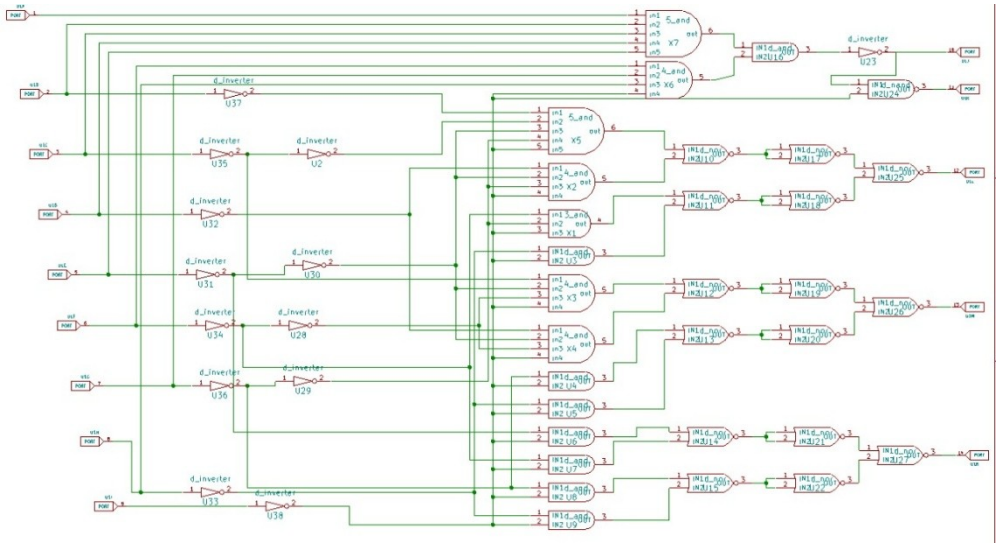


Figure 3.12: Schematic of SN74LS148

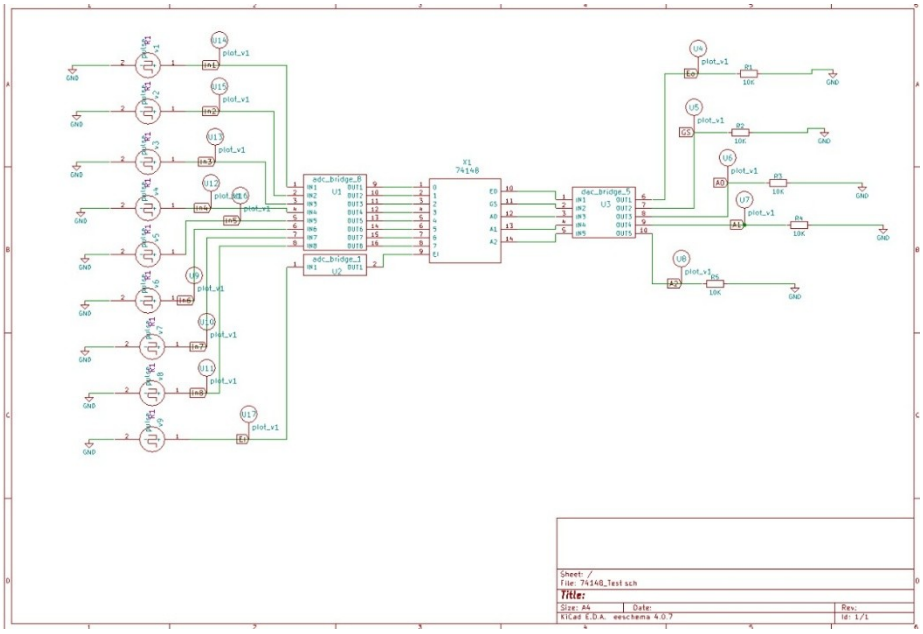


Figure 3.13: Test Circuit of SN74LS148

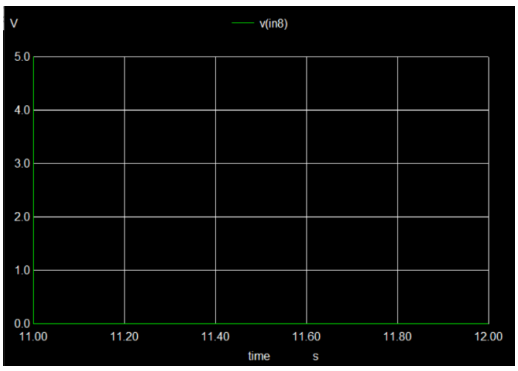


Figure 3.14: I7 is low

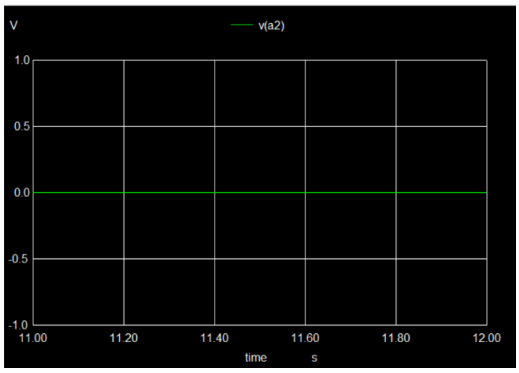


Figure 3.15: A2 select line goes Low

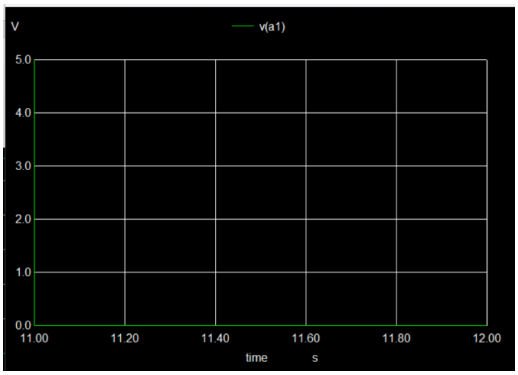


Figure 3.16: A1 select line goes low

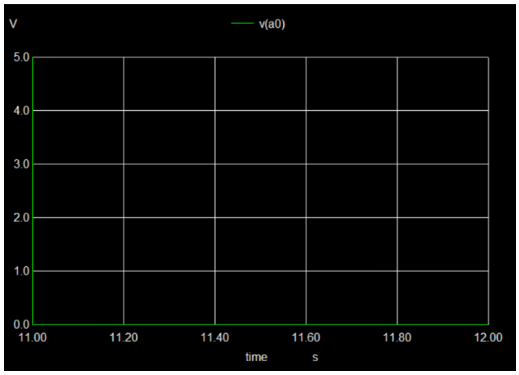


Figure 3.17: A0 select line goes Low

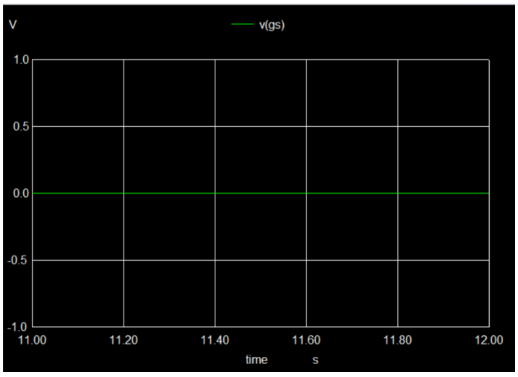


Figure 3.18: GS goes low

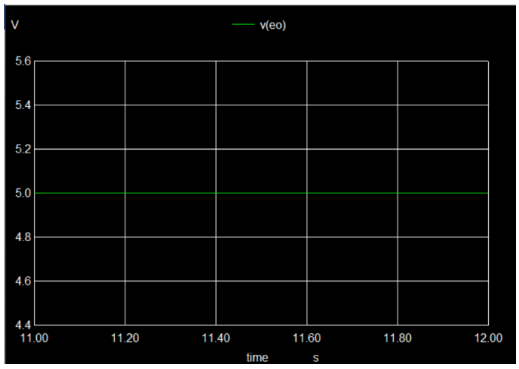


Figure 3.19: E0 goes high

3.5 CY74FCT480T - Dual 8-bit Parity Generator/Checker

3.5.1 Description

The CY74FCT480T is a high-performance dual 8-bit parity generator/checker used for error detection in digital data transmission.

3.5.2 Key Features

- Two independent 8-bit parity blocks
- Even or odd parity generation/checking
- High-speed CMOS technology
- 3-state outputs for bus interfacing
- TTL-compatible I/O

3.5.3 Input and Output Relationship

- **Inputs:** A1–H1, A2–H2 (data inputs)
- **Outputs:** PAR1, PAR2 (parity outputs), odd1, odd2, and error
- Outputs indicate parity match or error based on even/odd mode selection

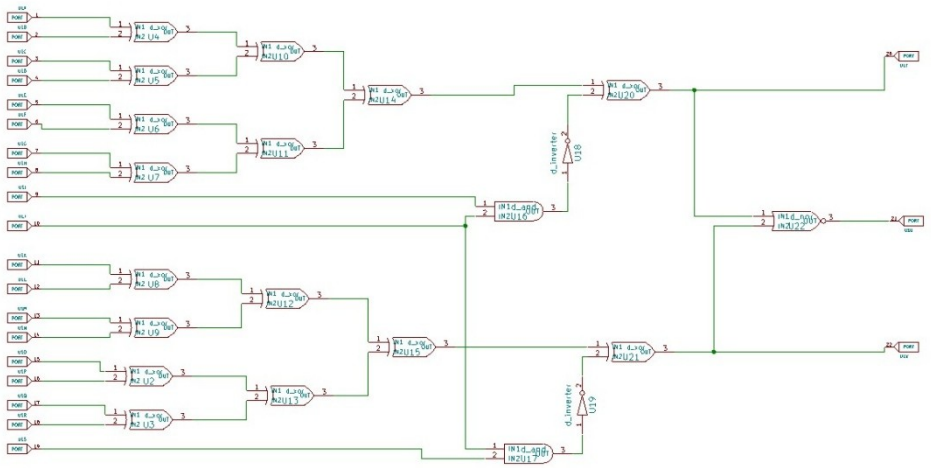


Figure 3.20: Schematic of CY74FCT480T

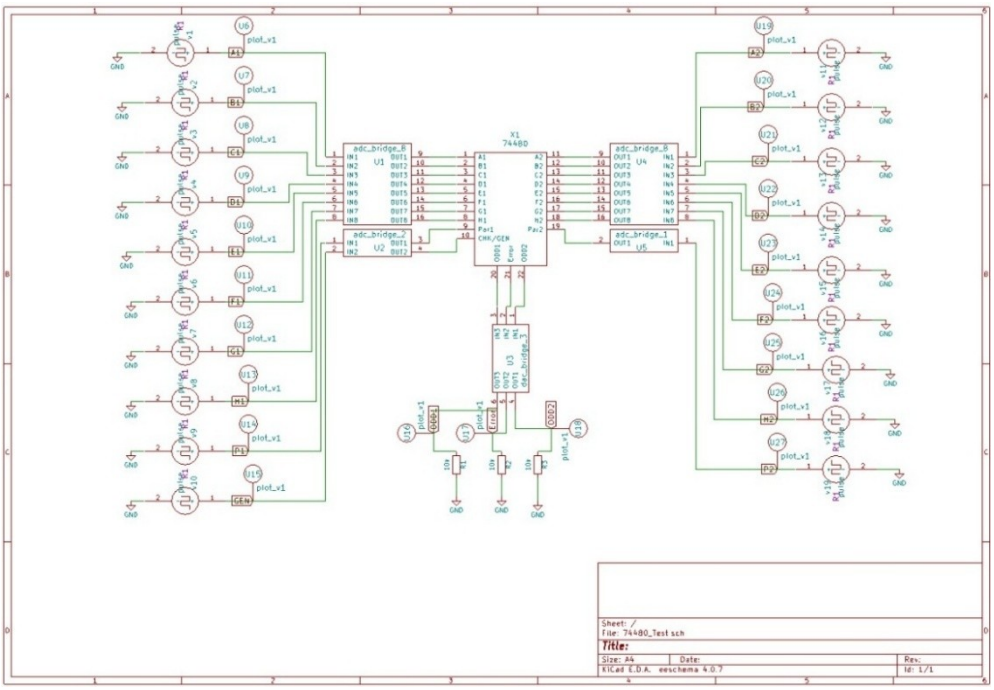


Figure 3.21: Test Circuit of CY74FCT480T

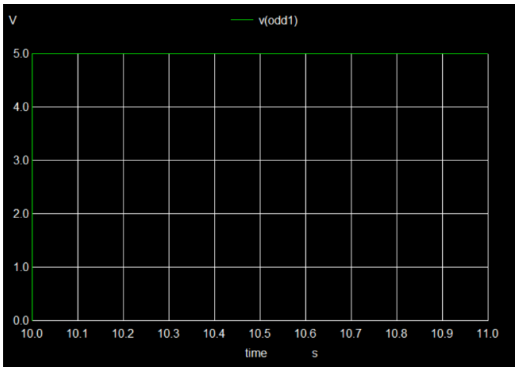


Figure 3.22

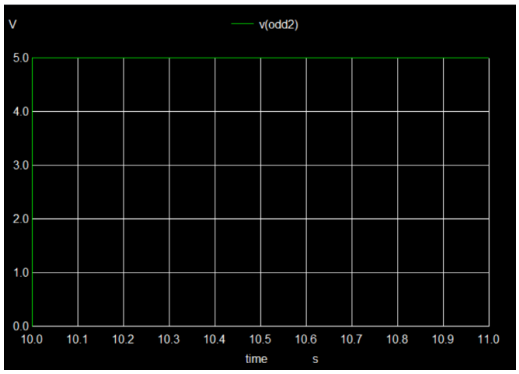


Figure 3.23

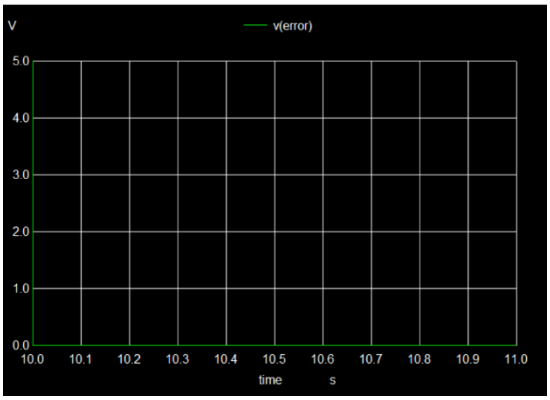


Figure 3.24: When both the inputs are even, gen/chk is high and P1 and P2 are low.

3.6 HD74LS139 - Dual 2:4 Decoder/Demultiplexer

3.6.1 Description

The HD74LS139 contains two independent 2-to-4 line decoders with active-low outputs and enable control.

3.6.2 Key Features

- Dual 2-line to 4-line decoders
- Individual enable inputs
- Active-low outputs
- TTL-compatible logic
- Used for memory decoding and demux applications

3.6.3 Input and Output Relationship

- **Inputs:** A, B (select), EN (enable)
- **Outputs:** Y0 to Y3
- One output is LOW based on A, B values when Enable is active LOW

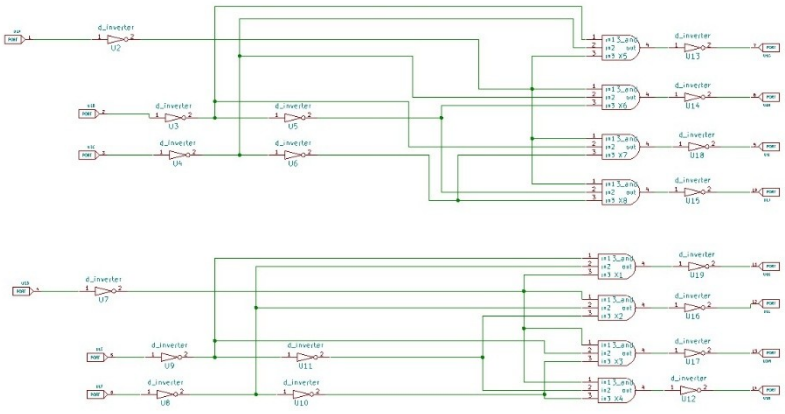


Figure 3.25: Schematic of HD74LS139

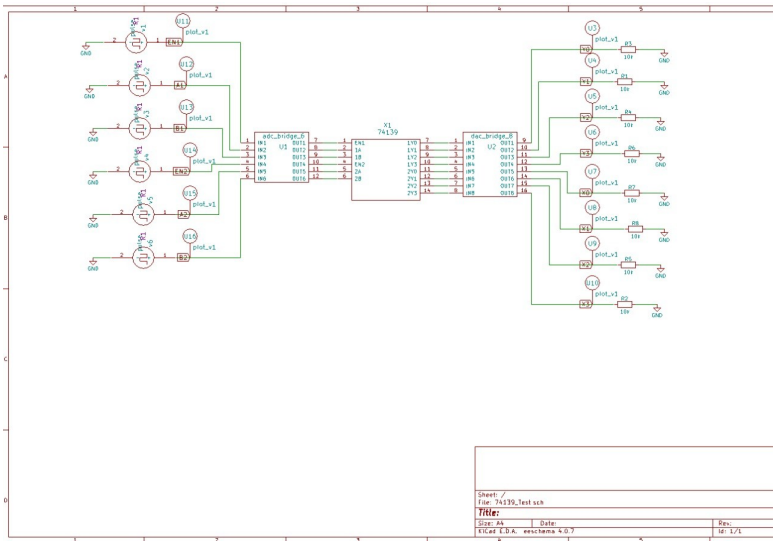


Figure 3.26: Test Circuit of HD74LS139

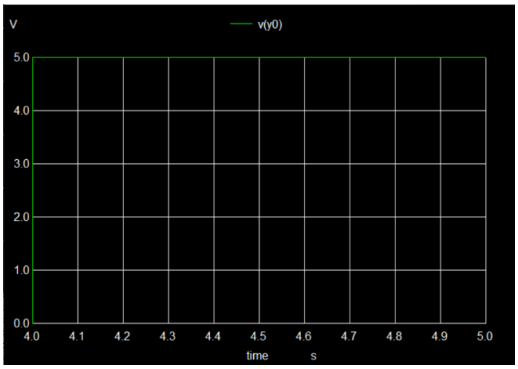


Figure 3.27

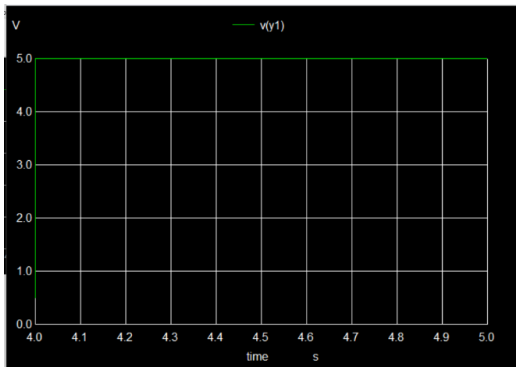


Figure 3.28

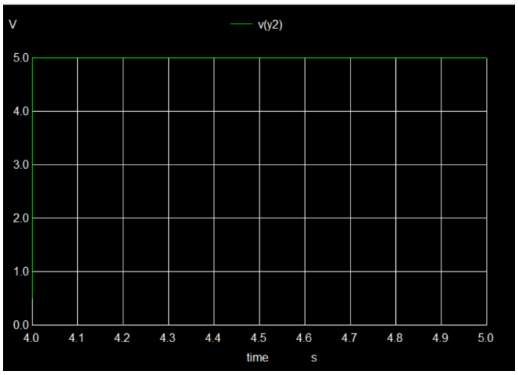


Figure 3.29

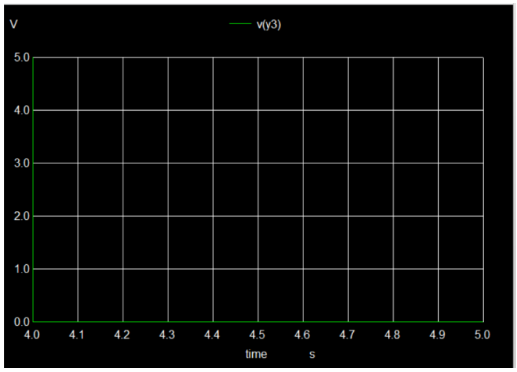


Figure 3.30

Figure 3.31: Both select lines are high

3.7 DM7447A - BCD to 7-Segment Decoder/Driver

3.7.1 Description

The DM7447A is a BCD to 7-segment decoder/driver for driving common anode displays, converting 4-bit binary input to appropriate display outputs.

3.7.2 Key Features

- BCD to 7-segment decoding
- Open-collector outputs
- Ripple blanking and lamp test features
- TTL-compatible logic
- Drives common anode displays

3.7.3 Input and Output Relationship

- **Inputs:** IN0–IN3 (BCD), LT, RBI, BI
- **Outputs:** a to g (segments)
- Outputs activate segments necessary to display digits 0–9 on a 7-segment display

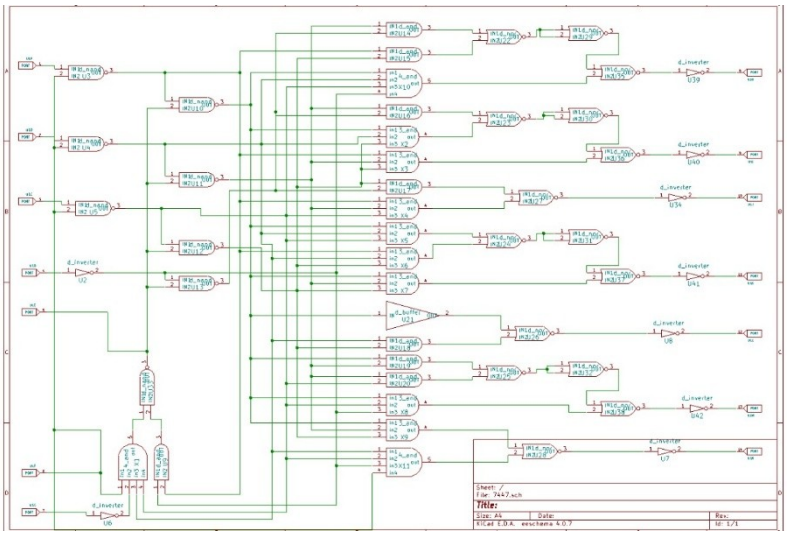


Figure 3.32: Schematic of DM7447A

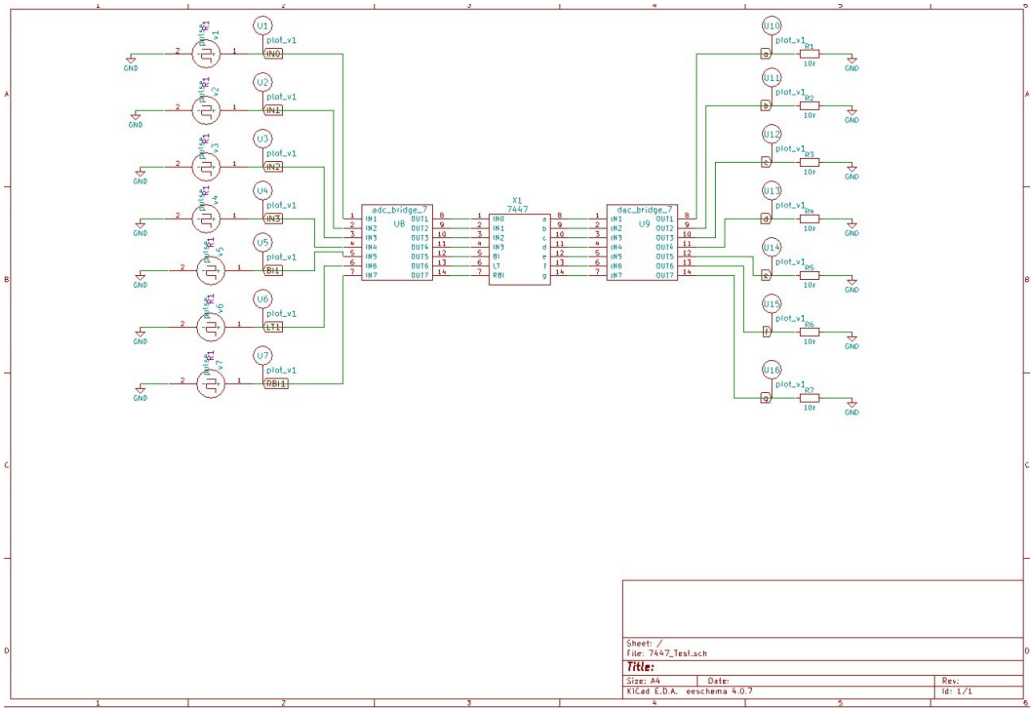


Figure 3.33: Test Circuit of DM7447A

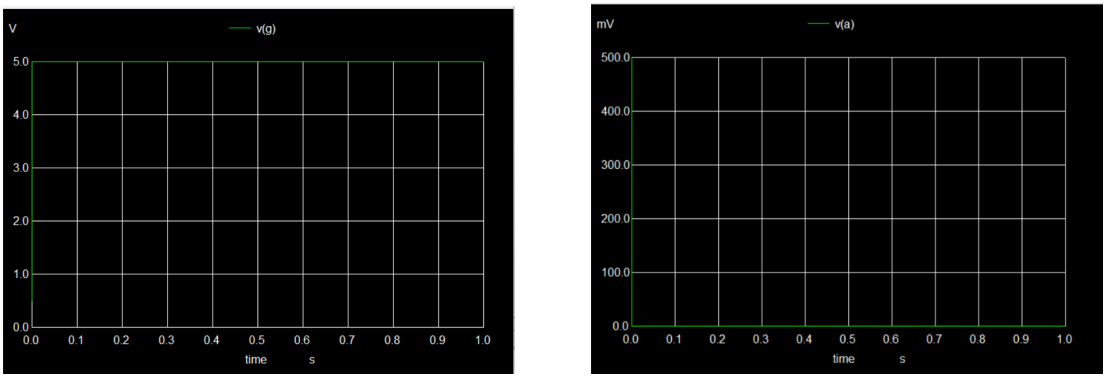


Figure 3.34: All inputs are low, RBI, LT and BI is high then only g is high every other output is low.

3.8 SN74HC688 - 8-bit Magnitude Comparator

3.8.1 Description

The SN74HC688 is an 8-bit comparator that outputs a LOW signal when two 8-bit inputs are exactly equal.

3.8.2 Key Features

- Compares two 8-bit binary values
- Active-low match output
- Expandable for larger comparisons
- High-speed CMOS technology
- TTL input compatibility

3.8.3 Input and Output Relationship

- **Inputs:** P0–P7, Q0–Q7 (input bits), OE (Enable, active-low)
- **Output:** Out Pin
- Output is LOW when all bits match, HIGH otherwise

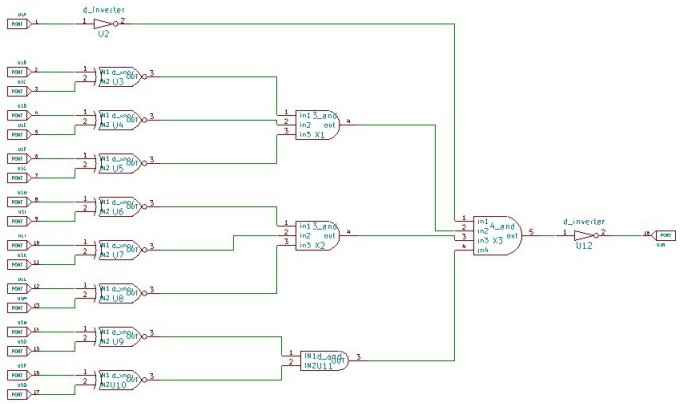


Figure 3.35: Schematic of SN74HC688

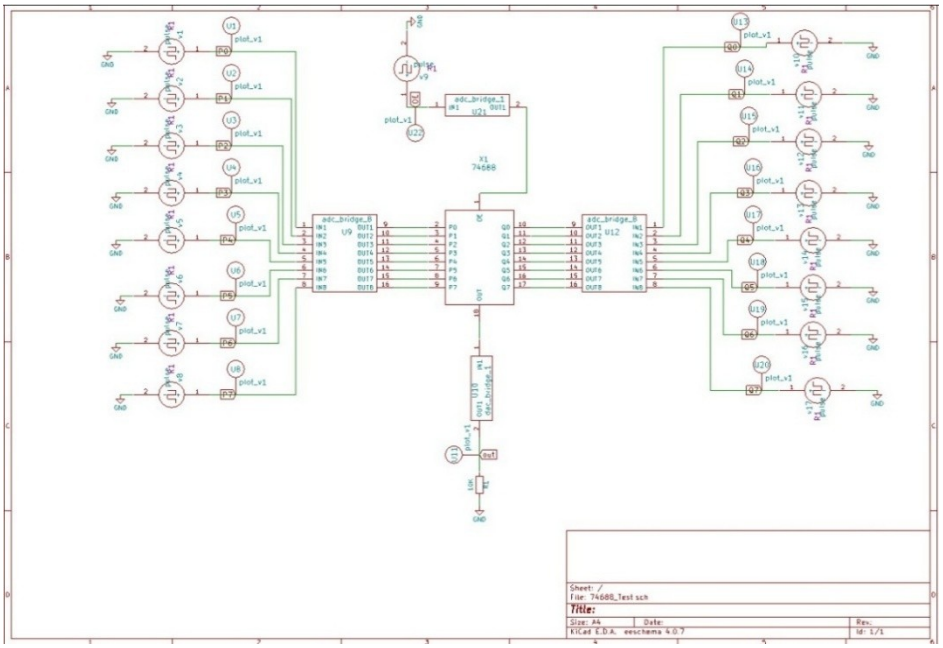


Figure 3.36: Test Circuit of SN74HC688

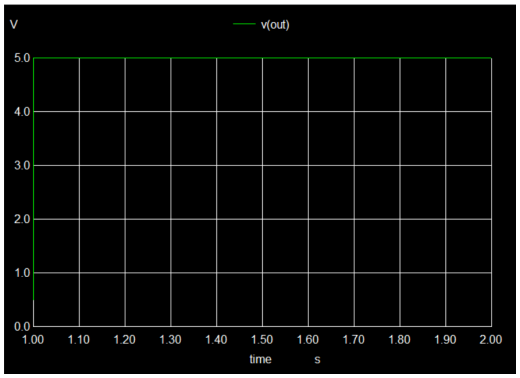


Figure 3.37: P is 00000010 and Q is 00000001

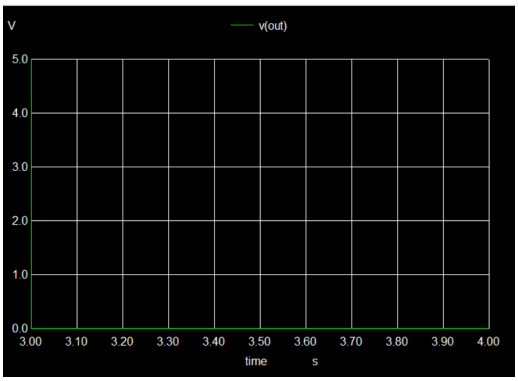


Figure 3.38: P and Q both are low

3.9 HD74HC149 - 8:8 Line Priority Encoder

3.9.1 Description

The HD74HC149 is a priority encoder which has 8 input lines (0–7) and 8 output lines (Y0–Y7). It is a combination of a HD74HC148 8–3 line priority encoder driving a HD74HC138 3–8 line decoder.

3.9.2 Key Features

- High speed operation: Tpd (0–7 to Y) = 16 ns (typical)
- High output current: Fanout of 10 LSTTL loads
- Wide operating voltage: V_{CC} = 2 to 6 V
- Low input current: 1 µA max
- Low quiescent current: I_{CC} = 4 µA max at 25°C

3.9.3 Input and Output Relationship

- **Inputs:** 0–7 (input bits), E (Enable, active-low)
- **Outputs:** Y0–Y7, P (Priority bit)
- Output LOW depends on highest priority active-low input (7 highest, 0 lowest)

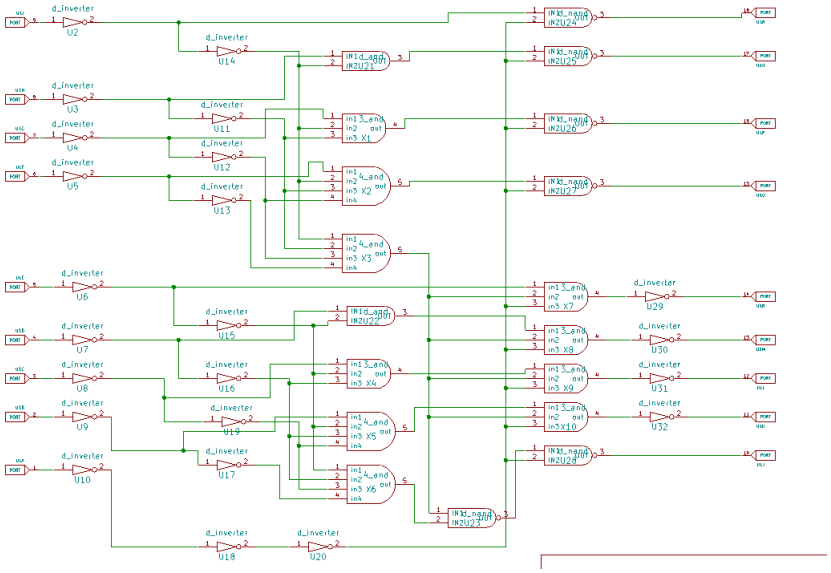


Figure 3.39: Schematic of HD74HC149

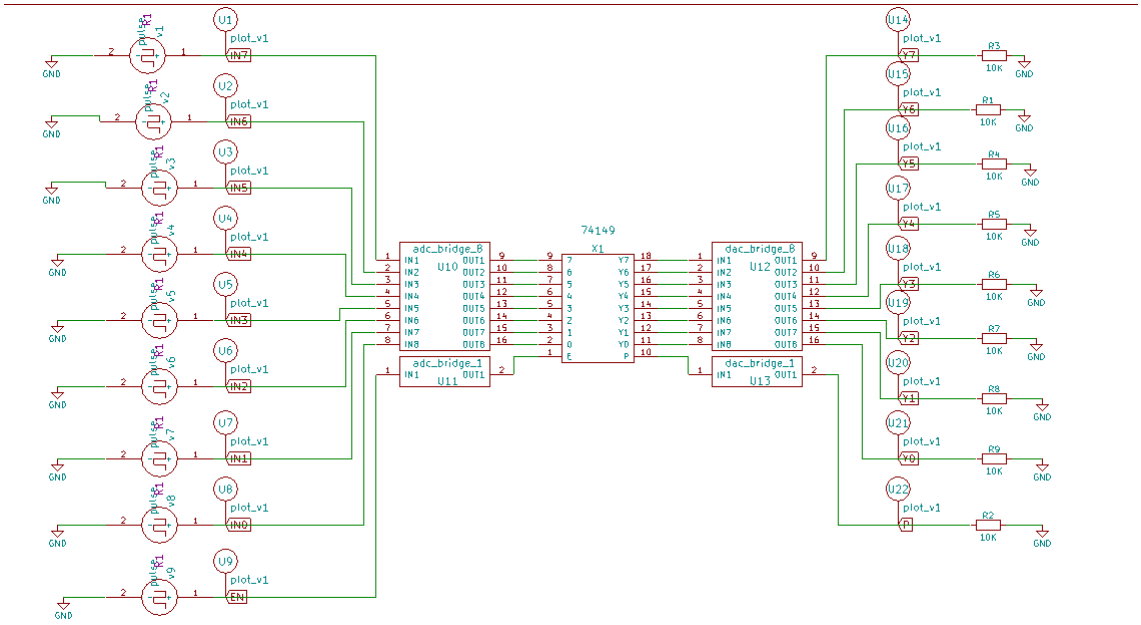


Figure 3.40: Test Circuit of HD74HC149

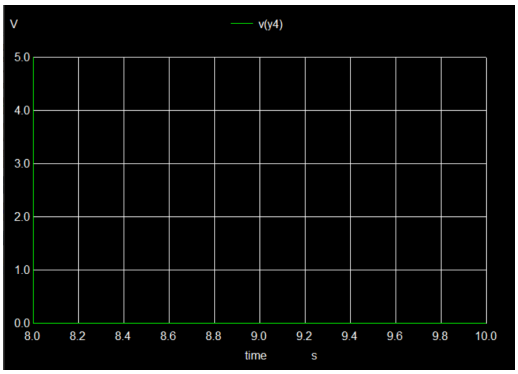


Figure 3.41

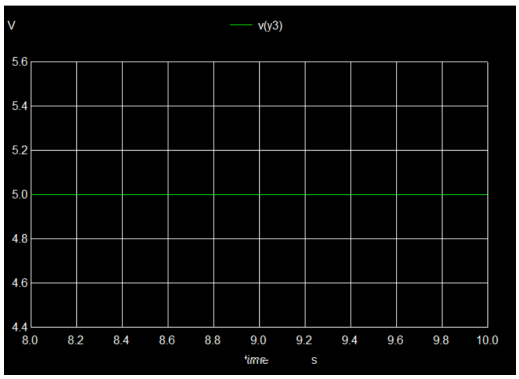


Figure 3.42

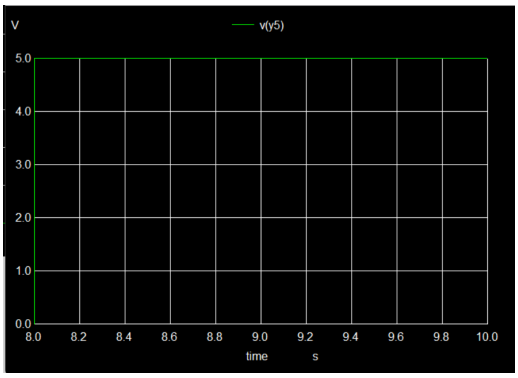


Figure 3.43

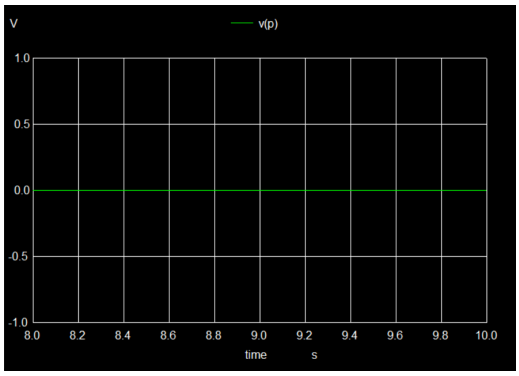


Figure 3.44

Figure 3.45: Input 4 and enable is Low

3.10 SN74LVC1G29 - 2-of-3 Decoder/Demultiplexer

3.10.1 Description

The SN74LVC1G29 is a 2-input, 3-output decoder/demultiplexer with an enable input (G).

3.10.2 Key Features

- Inputs accept voltages up to 5.5 V
- High drive strength: ±32 mA at 4.5 V
- Low power consumption: Max 10 µA
- Max propagation delay (Tpd): 5.1 ns at 3.3 V
- Latch-up immunity: greater than 100 mA per JESD 78, Class II

3.10.3 Input and Output Relationship

- **Inputs:** A0, A1 (select), G (Enable, active-low)
- **Outputs:** Y0–Y2
- Based on inputs A0 and A1 and enable G, one output goes LOW while others remain HIGH

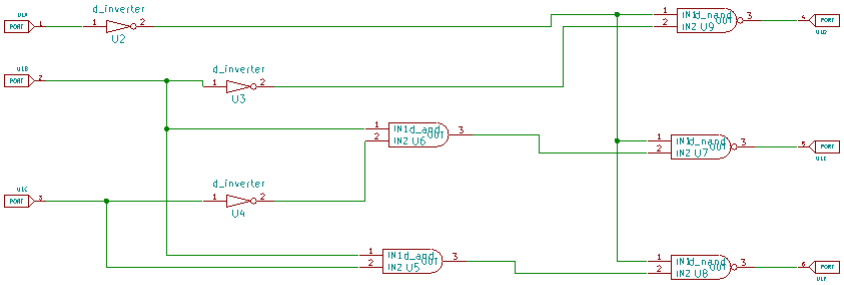


Figure 3.46: Schematic of SN74LVC1G29

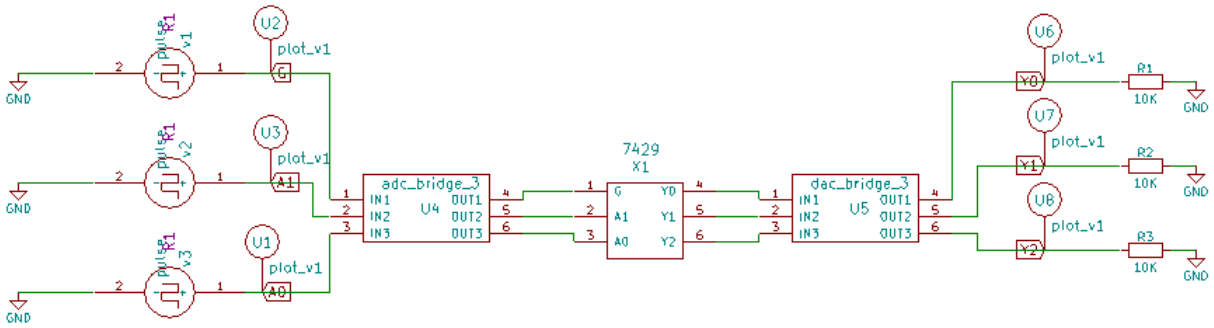


Figure 3.47: Test Circuit of SN74LVC1G29

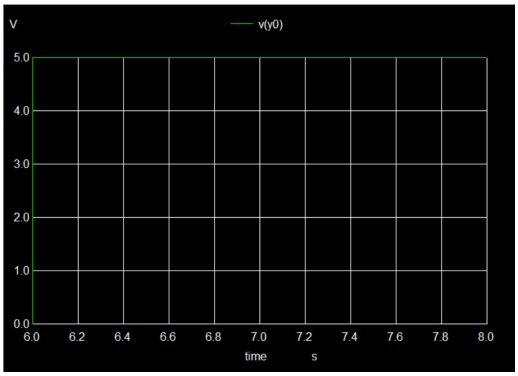


Figure 3.48

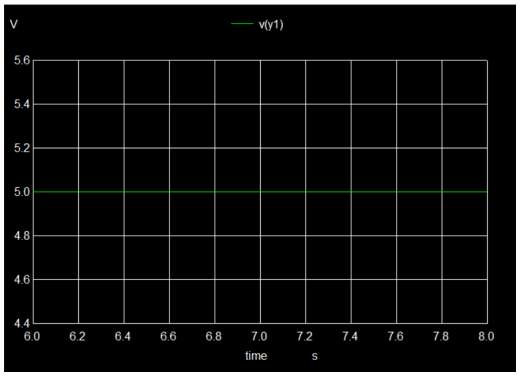


Figure 3.49

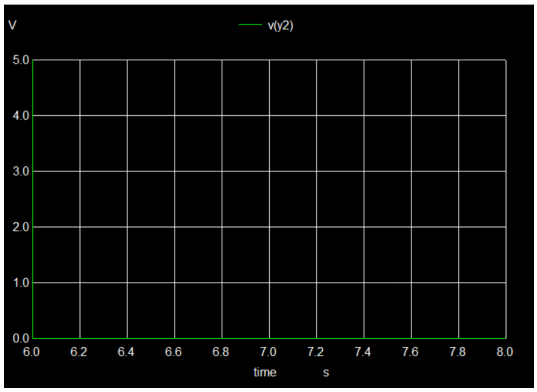


Figure 3.50: Enable is low and both the inputs given high

Chapter 4

Conclusion and Future Scope

The eSim internship provided a strong foundation in circuit design and simulation. Through hands-on practice, I gained valuable experience in creating schematics, mapping SPICE models, generating netlists, and performing various types of circuit simulations. The structured workflow of eSim, helped me understand the end-to-end process of electronic design automation.

This internship not only enhanced my technical proficiency in EDA tools but also emphasized the importance of open-source solutions in promoting accessible and cost-effective learning. The exposure to debugging techniques and simulation analysis has further strengthened my readiness for real-world applications in electronics systems.

We were able to design ICs subcircuits and then transform them into package which can be used in any other circuits for simulation in eSim.

There is scope for contributing to Research and Development in the field of circuit simulation tools, working on improving accuracy and the including more features.

In future we can contribute to the development and improvement of eSim itself by identifying bugs or adding new features.

eSim can be improved by providing more precise and user-friendly error messages that clearly indicate the type and location of issues in circuit designs, enabling users to debug and resolve problems more efficiently.

Chapter 5

References

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URL:https://robu.in/wp-content/uploads/2024/12/sn74als518.pdf

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URL: https://www.ti.com/lit/ds/sdls109/sdls109.pdf

SN74LS151 - 8:1 Multiplexer
URL:https://www.esi.uclm.es/www/isanchez/apuntes/ci/74151.pdf

SN74LS148 - 8:3 Priority Encoder
URL: https://www.ti.com/lit/ds/symlink/sn54ls148.pdf?ts=1746532900250&ref_url=https%253A%252F%252Fwww.google.co.in%252F

CY74FCT480T - Dual 8-bit Parity Generator/Checker
URL: https://www.ti.com/lit/ds/symlink/cy54fct480t.pdf?ts=1746558903692&ref_url=https%253A%252F%252Fwww.google.com%252F

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URL:https://www.ti.com/lit/ds/symlink/sn54ls139a@sp.pdf?ts=1746559318642&ref_url=https%253A%252F%252Fwww.google.com%252F

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URL:https://www.ti.com/lit/gpn/SN74HC688

DM7447A - BCD to 7-Segment Decoder/Driver
URL: https://edn.com/electroschematics/wp0content/uploads/2013/01/7447-datasheet.pdf

HD74HC149 - 8:8 Line Priority Encoder
URL:https://k1.spdns.de/Develop/Hardware/Infomix/ICs%20logic/74xxx/74149.HC.pdf

SN74LVC1G29 - 2-of-3 Decoder/Demultiplexer
URL:https://www.ti.com/lit/ds/symlink/sn74lvc1g29.pdf?ts=1747283339772&ref_url=https%253A%252F%252Fwww.ti.com%252Fproduct%252FSN74LVC1G29