Semester Long Internship Report

Report

On

Adding ICs as Subcircuits in eSim Library

Submitted by

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Acknowledgment

We take this occasion to offer our heartfelt gratitude to the FOSSEE, IIT Bombay Team for offering us this wonderful opportunity to work on the design and integration of multiple sub-circuits in **eSim**. Working on **eSim** has provided us with invaluable insights into various open-source EDA tools for circuit simulation and their applications in the practical world.

We would like to express our heartfelt appreciation to our mentor, Mr. **Sumanto Kar**, for constantly guiding and mentoring us throughout the duration of our internship. It is with his support that we have been able to fulfill our project demands successfully. Whenever faced with an issue, he was always accessible to help us assess and debug them. Our learnings from him have been invaluable and shall be of paramount importance to us in the future.

Overall, it was a delightful experience interning at FOSSEE and contributing to its growth. I take away some great insights and knowledge from it. As enthusiastic beginners in the semiconductor industry, this internship is a milestone for us in our pursuit of a successful career.

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Chapter 1

Introduction

1.1 FOSSEE

FOSSEE, which stands for Free/Libre and Open Source Software for Education, is an organization based at IIT Bombay. It is a remarkable initiative aimed at promoting the use of open-source software in education and research. It was established with the mission to reduce dependency on proprietary software and to encourage the adoption of open-source alternatives. FOSSEE offers a wide range of tools and resources that cater to various academic and professional needs.

It provides comprehensive documentation, tutorials, workshops, and hands-on training sessions to empower students, educators, and professionals to leverage open-source software for their projects and coursework. The organization's commitment to fostering a collaborative and inclusive environment has significantly contributed to the democratization of technology and has opened up new avenues for innovation and learning.

1.2 eSim

eSim, created by the FOSSEE project at IIT Bombay, is a versatile open-source software tool for circuit design and simulation. It combines various open-source software packages into one cohesive platform, making it easier to design, simulate, and analyze electronic circuits. This tool is particularly useful for students, educators, and professionals who need an affordable and accessible alternative to proprietary software.

eSim offers features for schematic creation, circuit simulation, and PCB design, and includes an extensive library of components. The Subcircuit feature is a significant enhancement, enabling users to design complex circuits by integrating simpler subcircuits. Through eSim, FOSSEE promotes the use of open-source solutions in engineering education and professional fields, encouraging innovation and collaboration.

1.3 NgSpice

NgSpice is an open-source SPICE simulator for electric and electronic circuits. It can simulate various circuit elements, including JFETs, bipolar and MOS transistors, passive elements (R, L, C), diodes and other devices, all interconnected in a netlist.

Digital circuits are also simulated, ranging from single gates to complex circuits, including combinations of analog, digital, and mixed-signal circuits. NgSpice offers a wealth of device models for active, passive, analog, and digital elements. Users input their circuits as netlists, and the output is one or more graphs of currents, voltages, and other electrical quantities, or saved in a data file.

1.4 Makechip

Makechip is a platform that offers convenient and accessible tools for digital circuit design. It provides both browser-based and desktop-based environments for coding, compiling, simulating, and debugging Verilog designs. Makechip supports a combination of open-source and proprietary tools, ensuring a comprehensive range of capabilities.

Users can simulate Verilog/SystemVerilog/Transaction-Level Verilog code in Makechip. eSim is interfaced with Makechip using a Python-based application called Makechip-App, which launches the Makechip IDE. Makechip aims to make circuit design easy and enjoyable for users of all skill levels. The platform provides a userfriendly interface, intuitive workflows, and a range of helpful features that simplify the design process and enhance the overall user experience.

The main drawback of these open-source tools is that they are not comprehensive. While some are capable of PCB design (e.g., KiCad), others focus on simulations (e.g., gEDA). To the best of our knowledge, there is no open-source software that combines circuit design, simulation, and layout design in one platform. eSim addresses this gap by integrating all these capabilities.

Chapter 2

Features of eSim

The objective behind the development of eSim is to provide an open-source EDA solution for electronics and electrical engineers. The software is capable of performing schematic creation, PCB design, and circuit simulation (analog, digital, and mixedsignal). It also provides facilities to create new models and components. Thus, eSim offers the following features:

1. Schematic Creation: eSim provides an easy-to-use graphical interface for drawing circuit schematics, making it accessible for users of all levels. Users can drag and drop components from the library onto the schematic, simplifying the design process. Comprehensive editing tools allow for easy modification of schematics, including moving, rotating, and labeling components.

2. Circuit Simulation: eSim supports SPICE (Simulation Program with Integrated Circuit Emphasis), a standard for simulating analog and digital circuits. Users can perform various types of analysis such as transient, AC, and DC, providing insights into circuit behavior over time and frequency. An integrated waveform viewer helps visualize simulation results, aiding in the analysis and debugging of circuit designs.

3. PCB Design: The PCB layout editor allows users to place components and route traces with precision. eSim includes DRC (Design Rule Check) capabilities to ensure that the PCB design adheres to manufacturing constraints and electrical rules. Users can generate Gerber files, which are standard for PCB fabrication, directly from their designs.

4. Subcircuit Feature: This feature enables users to create complex circuits by integrating smaller, simpler subcircuits, promoting modular and hierarchical design approaches. Subcircuits can be reused in different projects, saving time and effort in redesigning common circuit elements.

5. Open Source Integration: eSim integrates several open-source tools like KiCad, NgSpice, and GHDL, providing a comprehensive suite for electronic design automation. Being open-source, eSim is free to use, making advanced circuit design tools accessible without the need for expensive licenses.

Chapter 3

Problem Statement

To design and develop various analog and digital integrated circuit models in the form of sub-circuits using device model files already present in the eSim library. These IC models should be useful for future circuit design purposes by developers and users once they are successfully integrated into the eSim sub-circuit library.

3.1 Approach

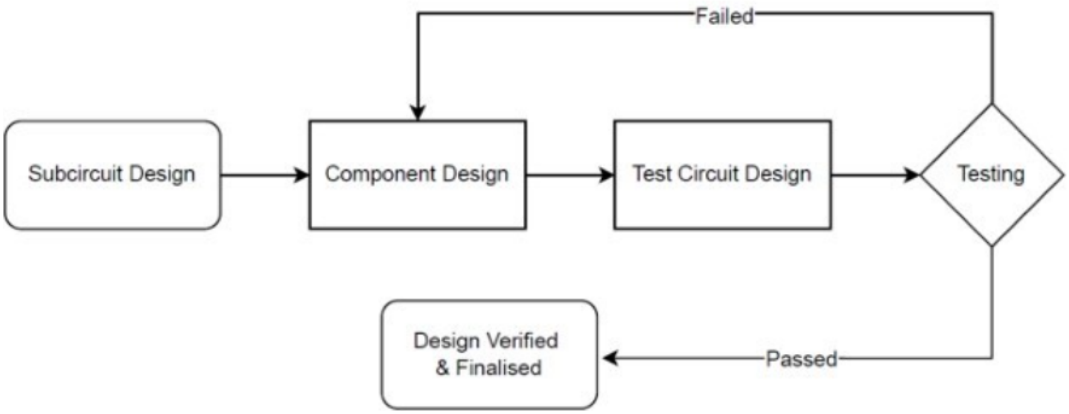

Figure 3.1: Flowchart of IC Design Approach Followed

Our approach to implementing the problem statement involved a systematic process, leveraging datasheets from leading Integrated Circuit (IC) manufacturers such as Texas Instruments, Analog Devices, and NXP Semiconductors. We focused on selecting ICs with diverse functionalities, including precision amplifiers, comparators, encoders, and audio amplifiers. The process is outlined in the following steps:

1. Analyzing Datasheets: The first step involved an in-depth review of datasheets for various analog and digital ICs. We aimed to identify circuits suitable for implementation in eSim that were not already present in the eSim library. This process included scrutinizing the detailed schematics of each IC, evaluating component values, and under-

standing truth tables. The goal was to select ICs that offered unique functionalities or enhancements not yet covered.

2. Subcircuit Creation: After selecting appropriate ICs, we proceeded to model these as sub-circuits within eSim. We utilized the model files available in the eSim device model library and ensured that our designs adhered strictly to the specifications outlined in the official datasheets. This phase also involved creating accurate symbol and pin diagrams for each IC, in accordance with the packaging and pin descriptions provided in the datasheets. This step was crucial for ensuring the fidelity of the subcircuit models.

3. Test Circuit Design: With the sub-circuits created, we then designed and built test circuits based on the datasheets. This step was essential for verifying the functionality of each sub-circuit. We developed a series of test cases and constructed corresponding test circuits to evaluate the performance and accuracy of the implemented IC models.

4. Schematic Testing: Following the construction of test circuits, we conducted simulations to analyze the outputs. This involved generating waveforms and plots to assess the behavior of the circuits. We employed KiCad for converting designs to NgSpice netlists and utilized eSim's simulation features to perform comprehensive testing.

If the simulated outputs deviated from expected results, it signaled potential errors in the schematic. In such instances, we revisited the design phase to identify and correct discrepancies. The iterative process of debugging and re-testing continued until the test cases produced satisfactory results. Once the IC models met the desired performance criteria, they were deemed successful, marking the completion of the design process.

Chapter 4

74LS283

4.1 General Description

The 74LS283 is a 4-bit binary full adder with carry input and output. It adds two 4-bit numbers plus a carry-in and gives a 4-bit sum and carry-out. Built using TTL logic, it features fast carry look-ahead for high-speed performance and supports cascading for multi-bit addition.

It is functionally reliable and commonly used in arithmetic operations in digital systems. The IC is part of the LS (Low Power Schottky) TTL family, known for its speed and power efficiency.

4.2 Key Features

- 4-bit binary addition with carry-in and carry-out
- Fast carry look-ahead for quick operation
- Standard TTL voltage levels (4.75V – 5.25V)
- Cascadable for multi-bit additions
- Low power consumption (LS series)

4.3 Applications

- ALUs and digital processors
- Binary counters and accumulators
- Data path circuits in embedded systems
- Digital signal processing and timing units

4.4 Subcircuit

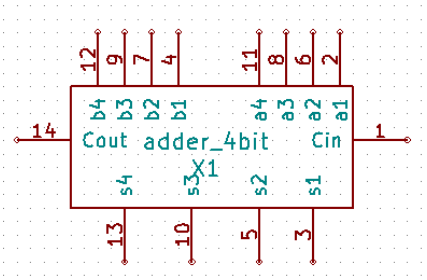

Figure 4.1: Subcircuit of the 74LS283

4.5 Subcircuit Schematic

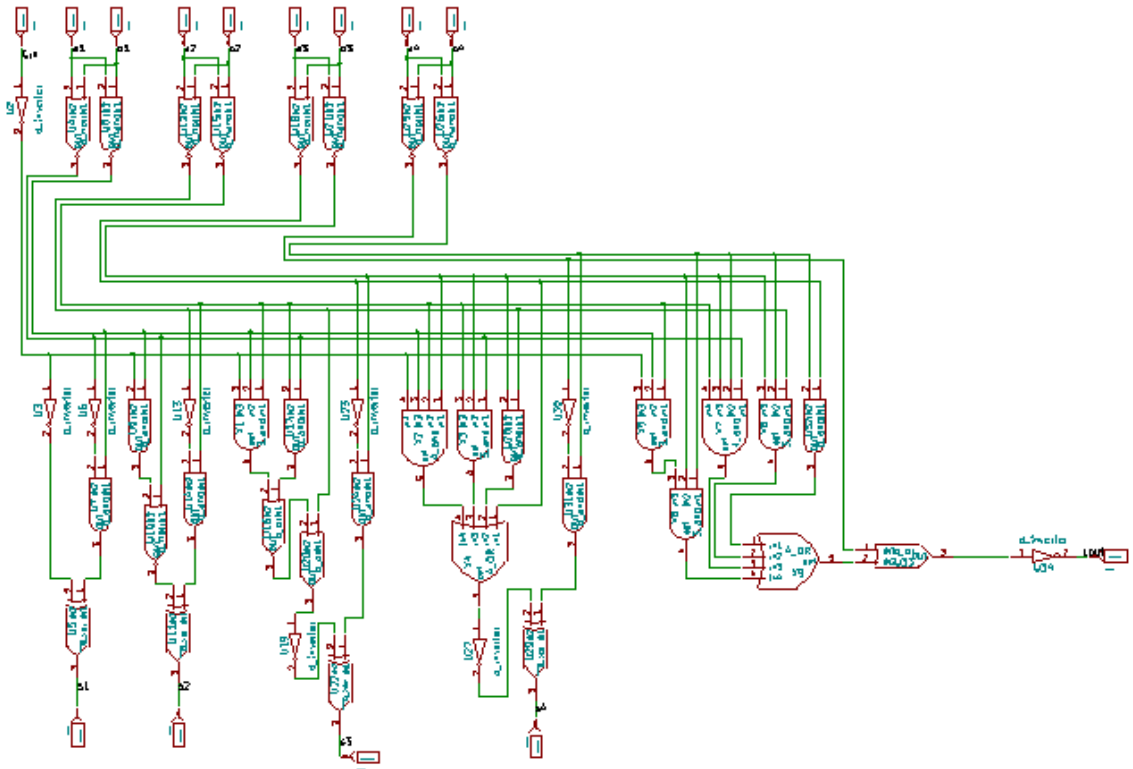

Figure 4.2: Subcircuit Schematic of the 74LS283

4.6 Test Circuit

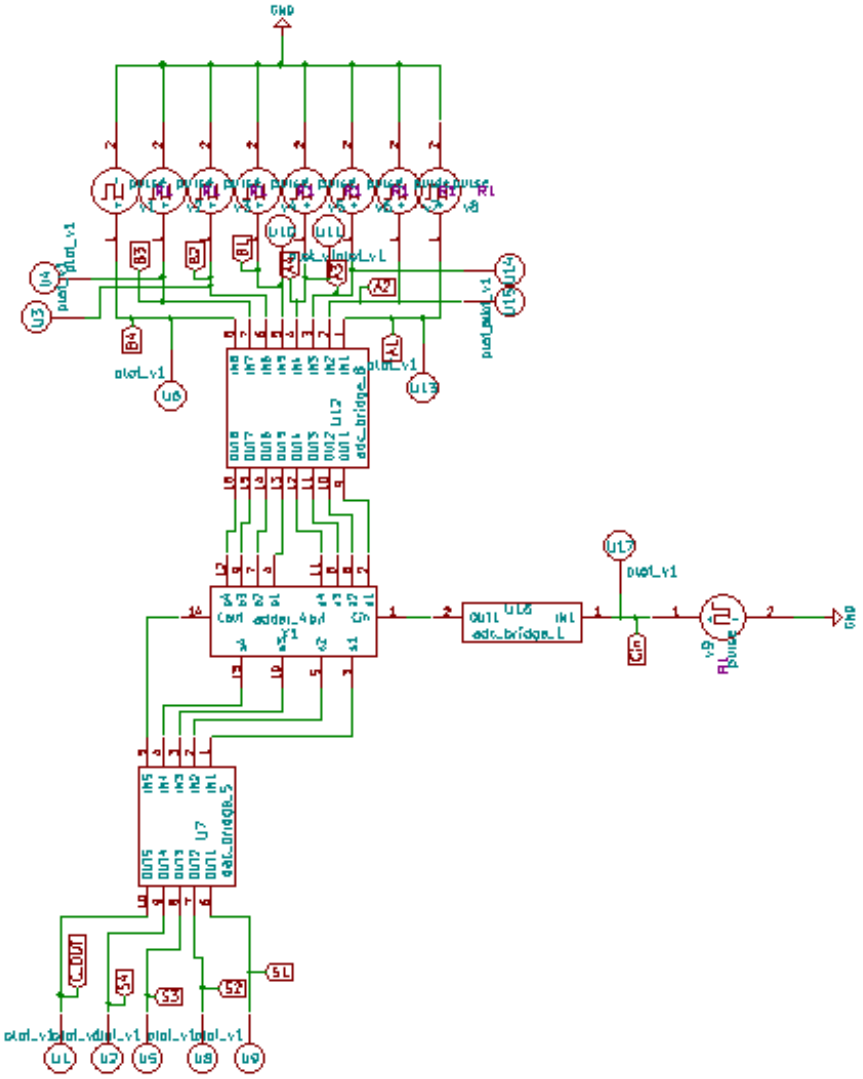

Figure 4.3: Test Circuit of the 74LS283

4.7 Function Table

FUNCTION TABLE

PINS	C_{IN}	A_1	A_2	A_3	A_4	B_1	B_2	B_3	B_4	Σ_1	Σ_2	Σ_3	Σ_4	C_{OUT}
Logic levels	L	L	H	L	H	H	L	L	H	H	H	L	L	H
Active HIGH	0	0	1	0	1	1	0	0	1	1	1	0	0	1
Active LOW	1	1	0	1	0	0	1	1	0	0	0	1	1	0

H = HIGH voltage level
L = LOW voltage level

Example:
1001
1010
10011
(10 + 9 = 19)
(carry + 5 + 6 = 12)

Figure 4.4: Function Table of the 74LS283

4.8 Output Plot

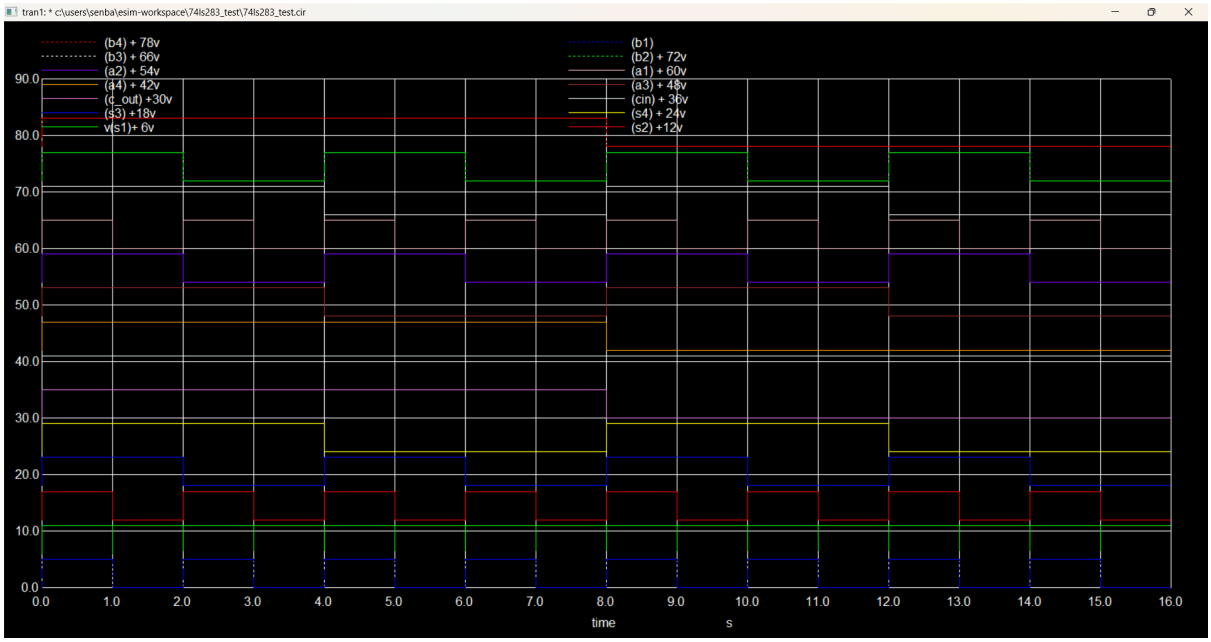

Figure 4.5: Output of the 74LS283

Chapter 5

74HC147N

5.1 General Description

The 74HC147N is a high-speed 10-to-4 priority encoder from the HC (High-speed CMOS) logic family. It accepts up to 10 active LOW inputs and encodes them into a 4-bit binary output, giving priority to the highest-numbered active input. This IC is designed using advanced CMOS technology, ensuring low power consumption and high noise immunity.

It provides TTL-compatible inputs and outputs, making it ideal for interfacing with both TTL and CMOS logic levels.

5.2 Key Features

- 10-to-4 priority encoder with active LOW inputs
- TTL-compatible logic levels
- High-speed CMOS performance
- Low power consumption
- Ideal for input encoding in digital systems

5.3 Applications

- Keyboard or keypad encoders
- Data compression and address decoding
- Digital control systems
- Priority logic handling in embedded applications

5.4 Subcircuit

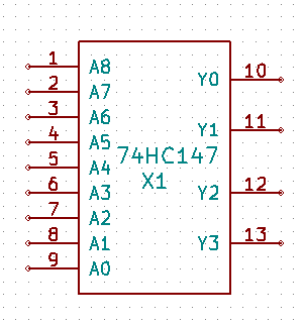

Figure 5.1: Subcircuit of the 74HC147N

5.5 Subcircuit Schematic

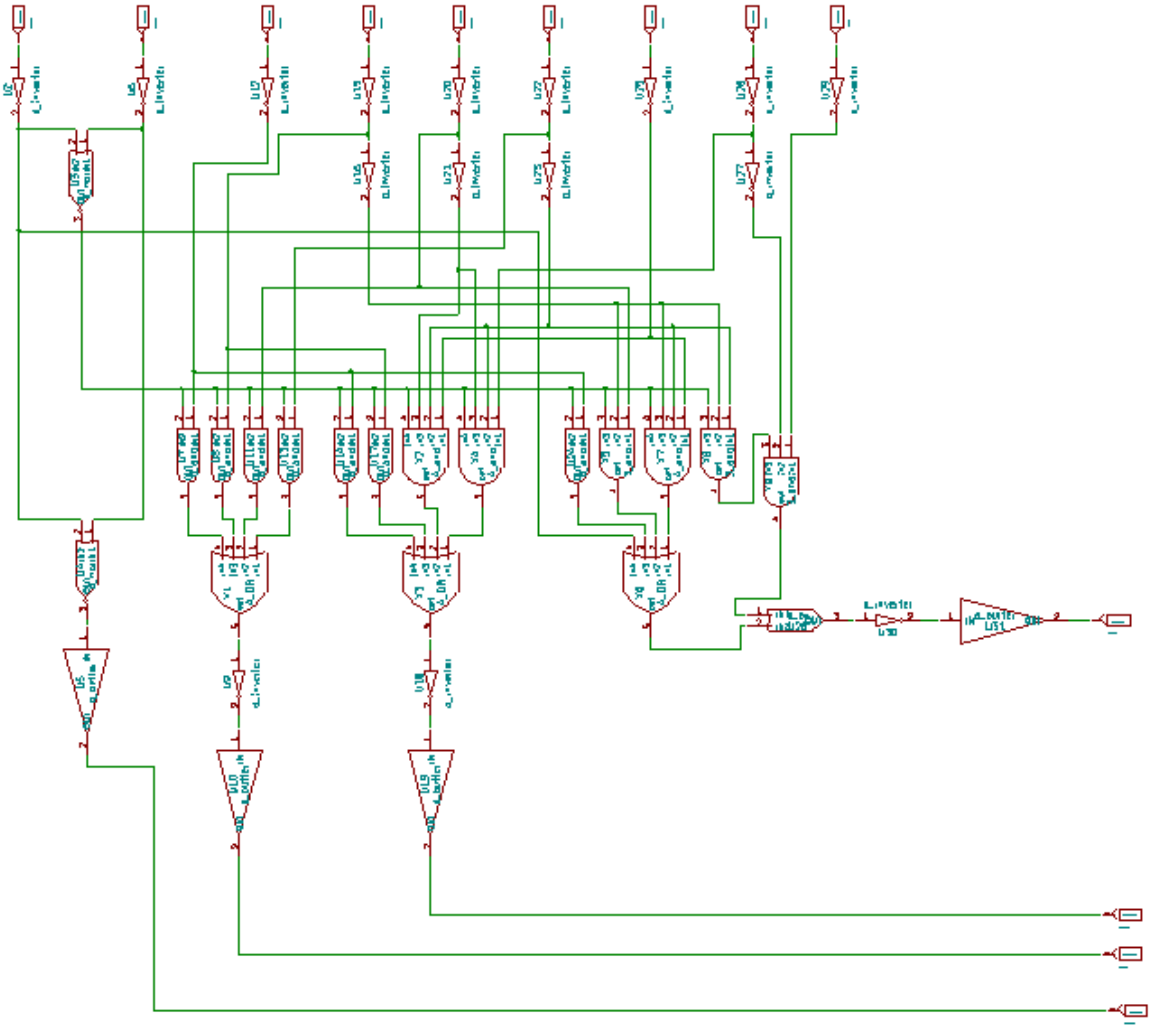

Figure 5.2: Subcircuit Schematic of the 74HC147N

5.6 Test Circuit

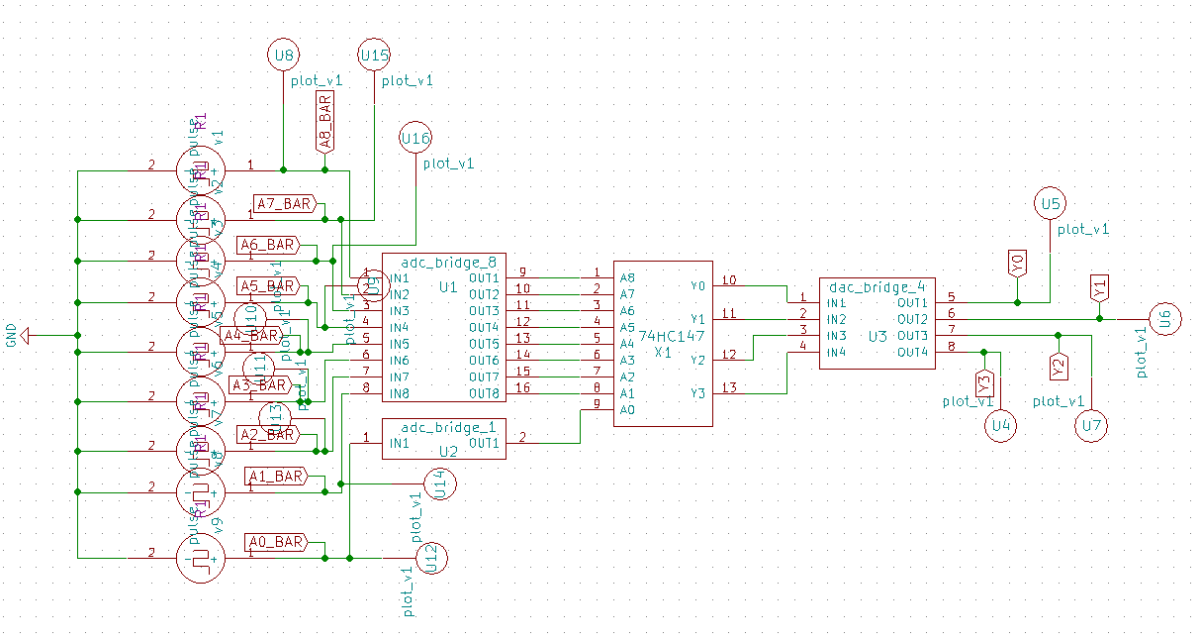

Figure 5.3: Test Circuit of the 74HC147N

5.7 Function Table

FUNCTION TABLE

INPUTS									OUTPUTS			
$\overline{A}_0$	$\overline{A}_1$	$\overline{A}_2$	$\overline{A}_3$	$\overline{A}_4$	$\overline{A}_5$	$\overline{A}_6$	$\overline{A}_7$	$\overline{A}_8$	$\overline{Y}_3$	$\overline{Y}_2$	$\overline{Y}_1$	$\overline{Y}_0$
H	H	H	H	H	H	H	H	H	H	H	H	H
X	X	X	X	X	X	X	X	L	L	H	H	L
X	X	X	X	X	X	X	L	H	L	H	H	H
X	X	X	X	X	X	L	H	H	H	L	L	L
X	X	X	X	X	L	H	H	H	H	L	L	H
X	X	X	X	L	H	H	H	H	H	L	H	L
X	X	X	L	H	H	H	H	H	H	L	H	H
X	X	L	H	H	H	H	H	H	H	H	L	L
X	L	H	H	H	H	H	H	H	H	H	L	H
L	H	H	H	H	H	H	H	H	H	H	H	L

Figure 5.4: Function Table of the 74HC147N

5.8 Output Plot

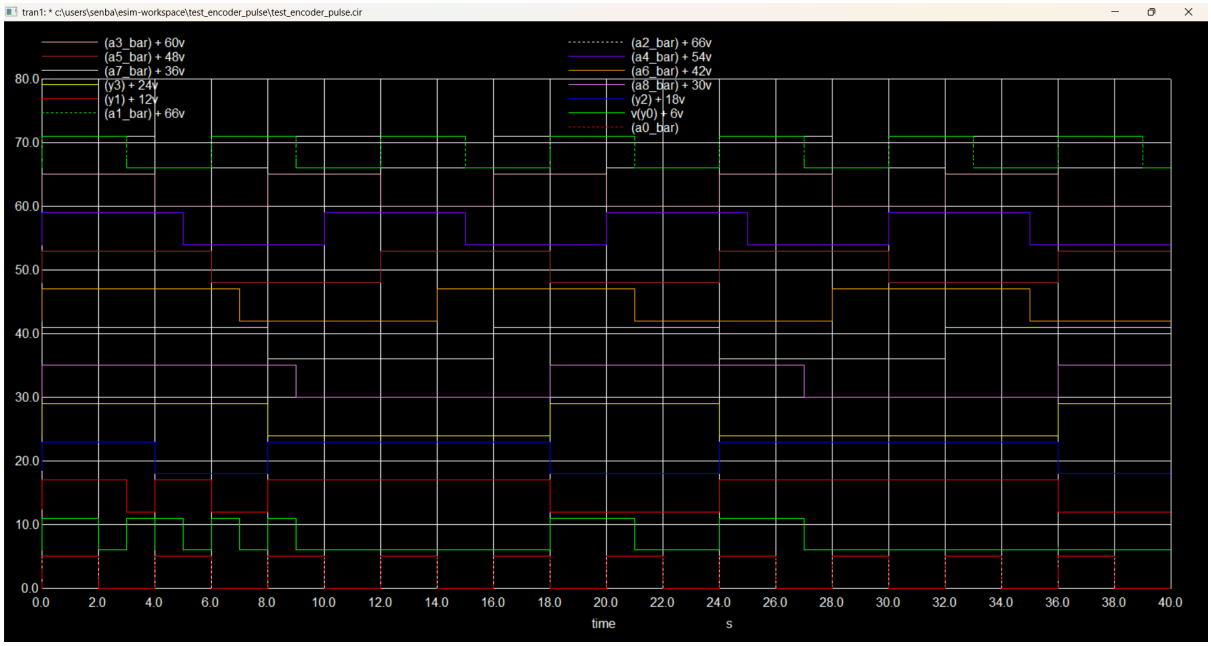

Figure 5.5: Output of the 74HC147N

Chapter 6

SN74LVC1G139

6.1 General Description

The SN74LVC1G139 is a single 2-to-4 line decoder/demultiplexer with active-LOW outputs. It takes two binary select inputs and enables one of four outputs when the enable input is LOW. It belongs to the LVC (Low-Voltage CMOS) family, offering high-speed operation and low power consumption. This IC is optimized for 1.65V to 3.6V supply voltage and is ideal for space-constrained applications due to its small package size.

6.2 Key Features

- 2-to-4 line decoder/demultiplexer
- Active-LOW enable and outputs
- Operates at 1.65V to 3.6V
- High-speed CMOS performance
- Small form factor for portable designs

6.3 Applications

- Address decoding in memory systems
- Data routing in communication circuits
- Control signal demultiplexing
- Logic decoding in embedded systems

6.4 Subcircuit

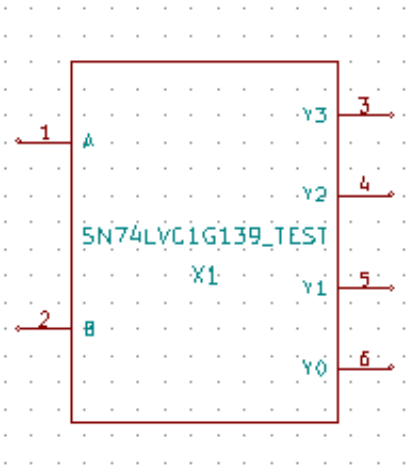

Figure 6.1: Subcircuit of SN74LVC1G139

6.5 Subcircuit Schematic Diagram

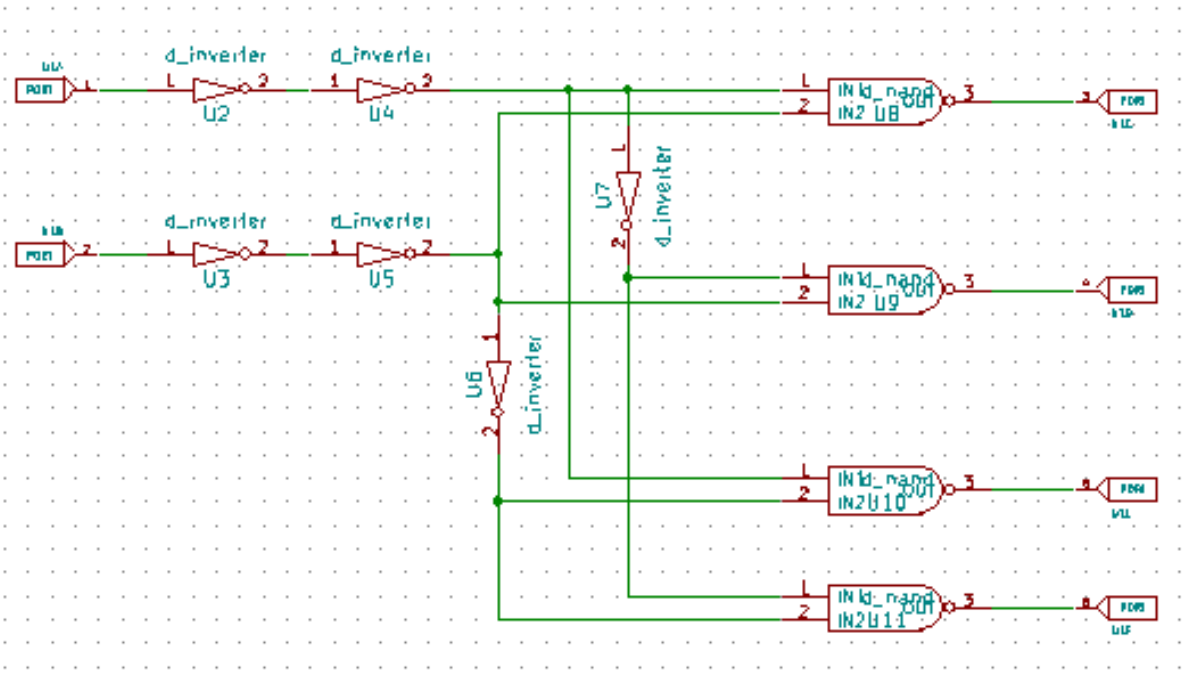

Figure 6.2: Subcircuit Schematic of the SN74LVC1G139

6.6 Test Circuit

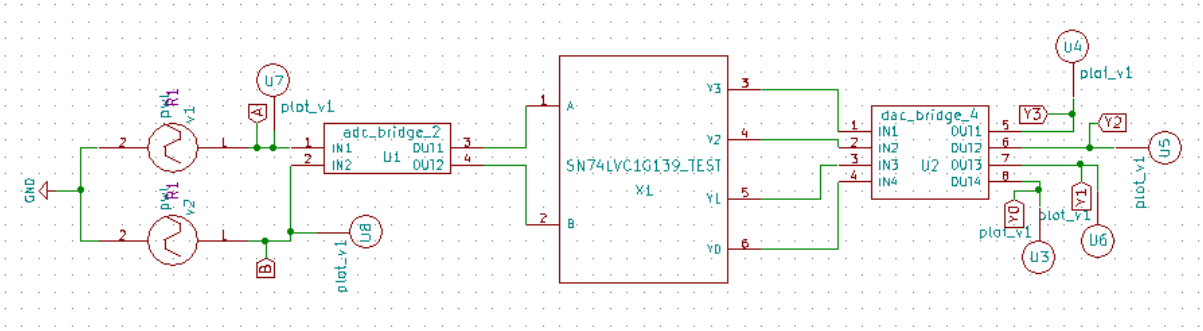

Figure 6.3: Test Circuit of the SN74LVC1G139

6.7 Function Table

INPUTS		OUTPUTS			
B	A	Y_0	Y_1	Y_2	Y_3
L	L	L	H	H	H
L	H	H	L	H	H
H	L	H	H	L	H
H	H	H	H	H	L

Figure 6.4: Function Table of the SN74LVC1G139

6.8 Output Plot

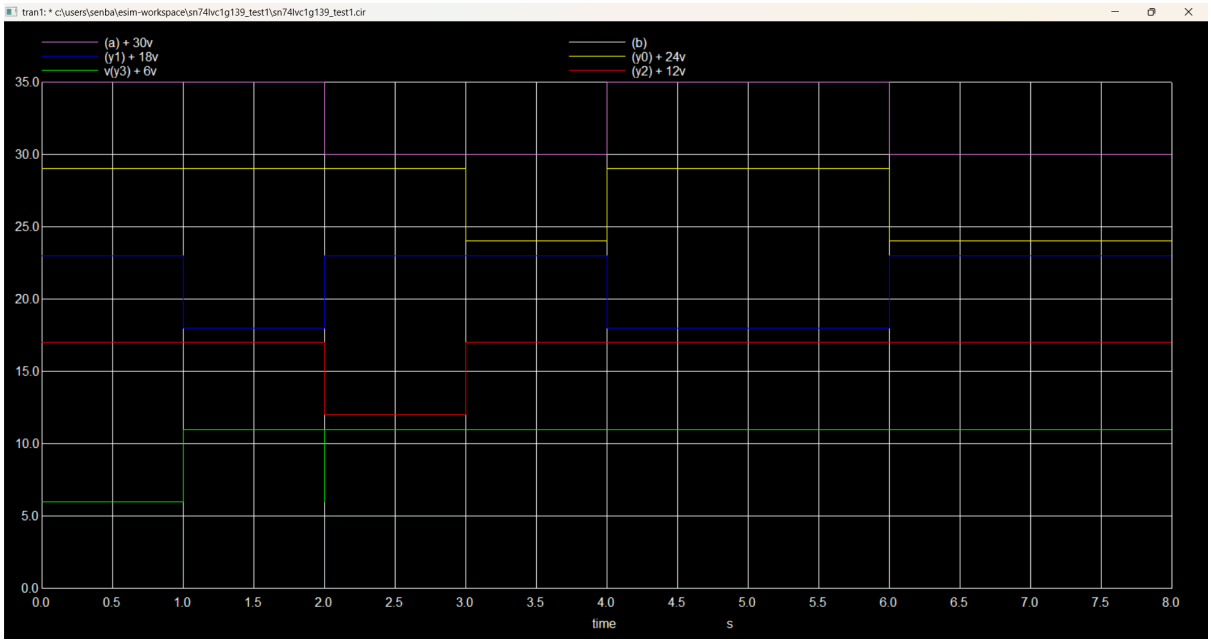

Figure 6.5: Output of the SN74LVC1G139

Chapter 7

DM54154

7.1 General Description

The DM54154 is a 4-line to 16-line decoder/demultiplexer with active-LOW outputs. It decodes four binary inputs into one of sixteen outputs, with only one output LOW at a time when enabled. Designed using TTL logic, the DM54154 features two enable inputs (one active-LOW, one active-HIGH) for flexible control. It is part of the 54-series family, built for military and aerospace use with an extended temperature range (-55°C to 125°C).

7.2 Key Features

- 4-to-16 line decoder/demultiplexer
- Active-LOW outputs with enable control
- Standard TTL voltage levels
- Military-grade temperature range: –55°C to 125°C
- High fan-out capability

7.3 Applications

- Memory address decoding
- Data routing in communication systems
- Control logic in microprocessors
- Signal demultiplexing in digital systems

7.4 Subcircuit

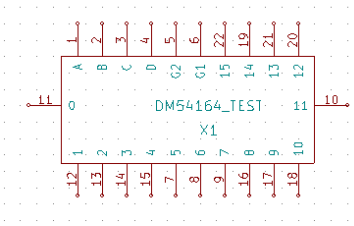

Figure 7.1: Subcircuit of the DM54154

7.5 Subcircuit Schematic

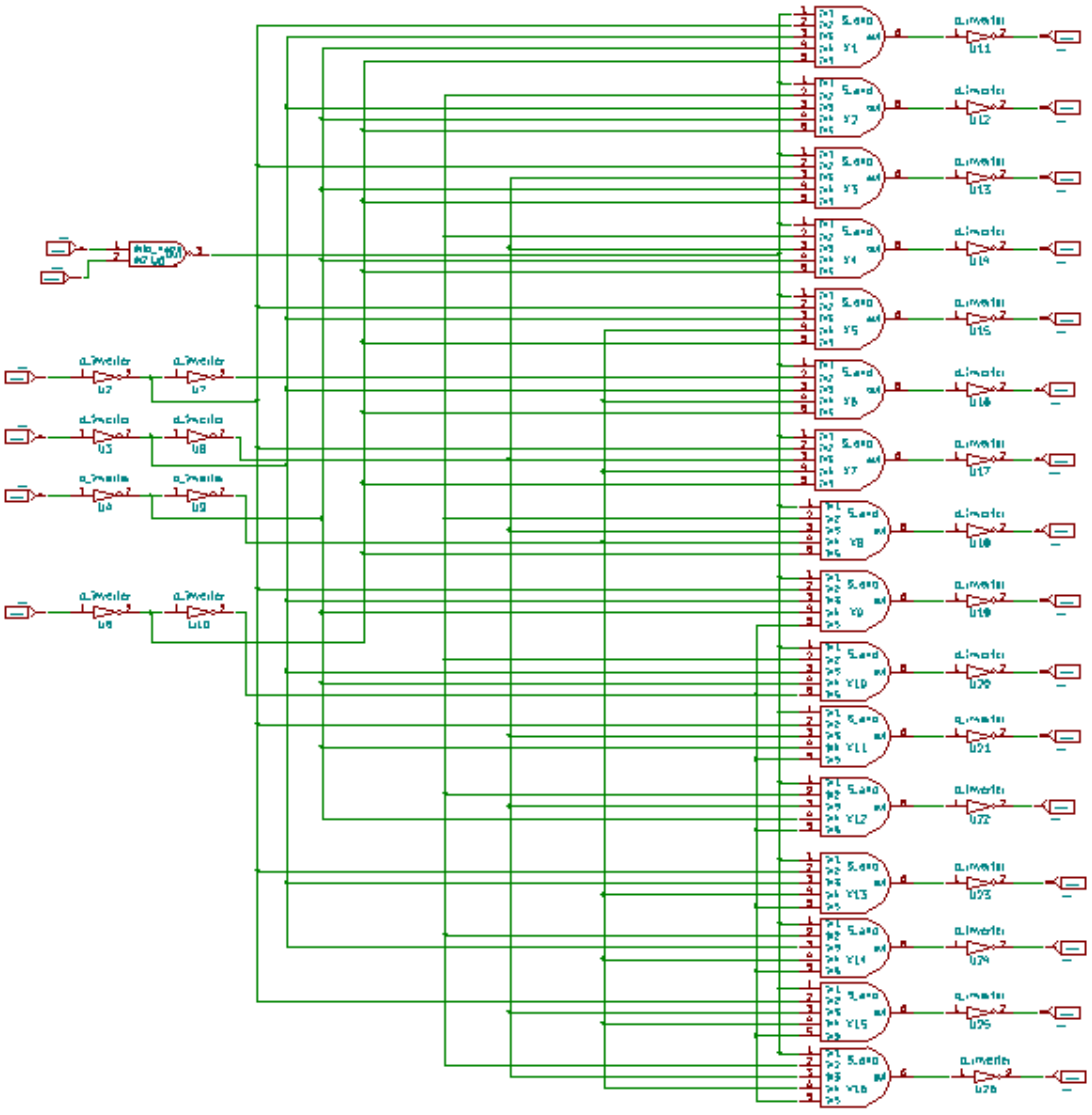

Figure 7.2: Subcircuit Schematic of the DM54154

7.6 Test Circuit

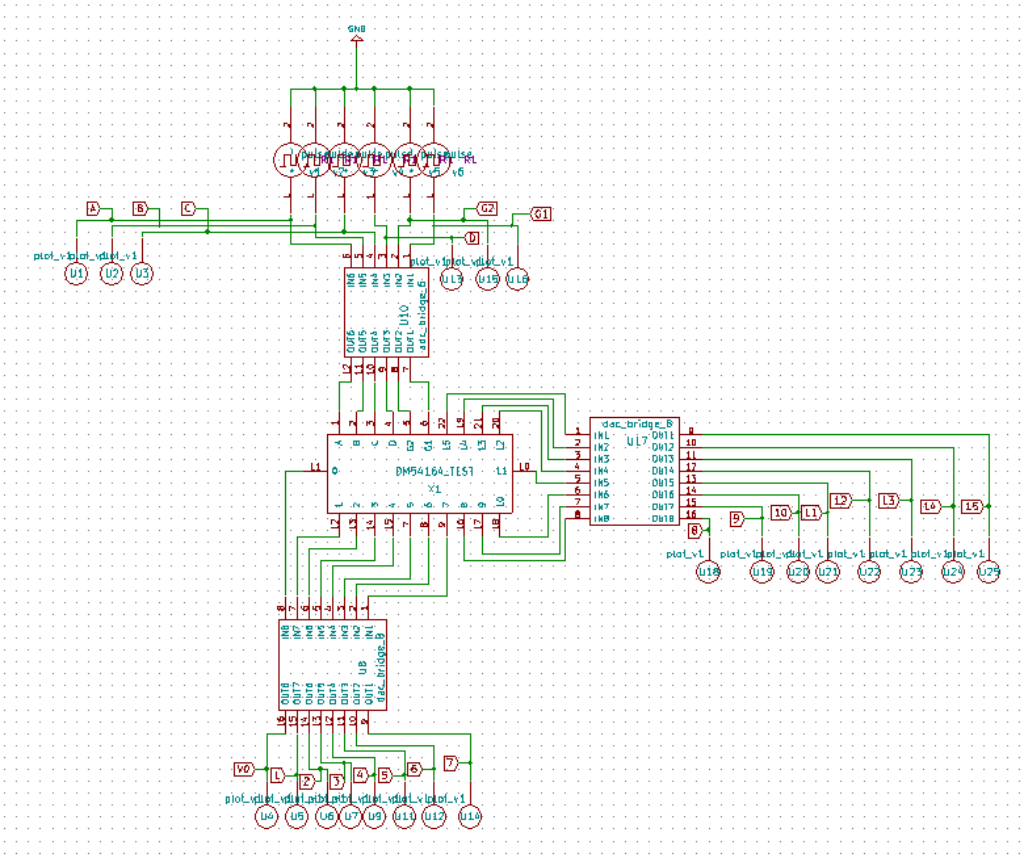

Figure 7.3: Test Circuit of the DM54154

7.7 Function Table

Inputs						Outputs															
G1	G2	D	C	B	A	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	L	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H
L	L	L	H	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H
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L	L	H	L	L	L	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H
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L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L
L	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	L	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H

Figure 7.4: Function Table of the DM54154

7.8 Output Plot

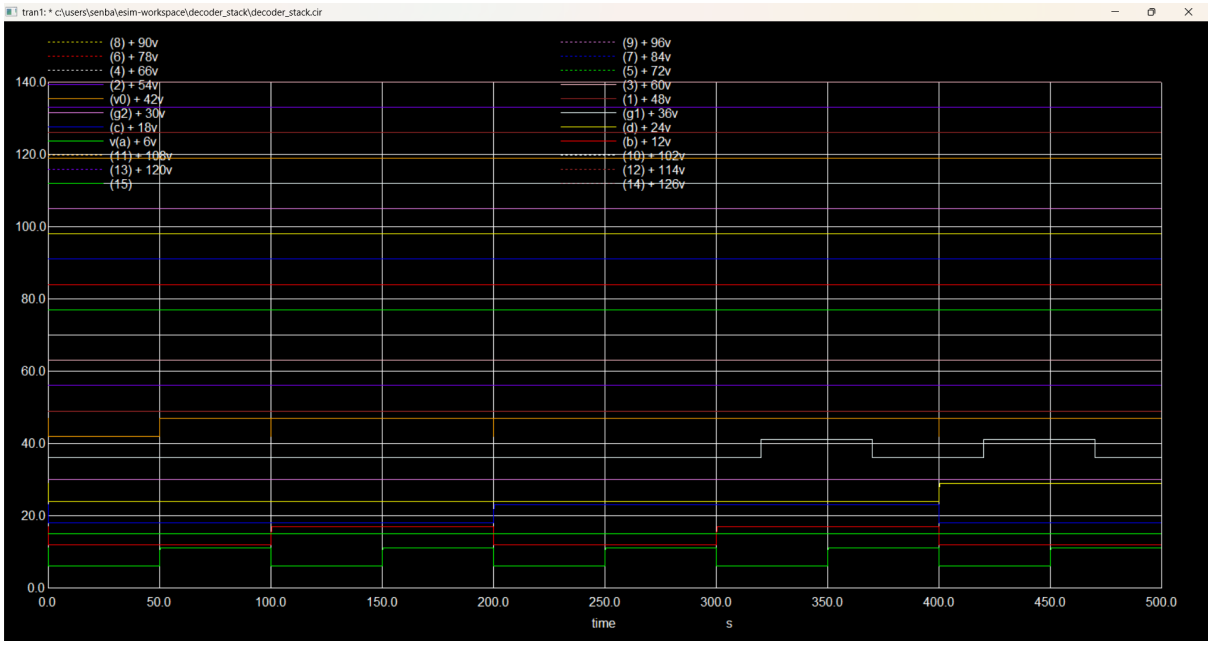

Figure 7.5: Output plot of the DM54154

Chapter 8

SN5485

8.1 General Description

The SN5485 is a 4-bit magnitude comparator that compares two 4-bit binary words (A and B) and provides outputs indicating whether A > B, A = B, or A < B.
It is designed using TTL logic and is part of the SN54 series, intended for military and aerospace environments with an extended operating temperature range (–55°C to 125°C).
The IC can be cascaded with additional comparators to compare words of greater bit length.

8.2 Key Features

- 4-bit binary magnitude comparator
- Provides outputs for $A > B$, $A = B$, $A < B$
- Standard TTL voltage operation
- Cascadable for comparing larger bit-widths
- Military-grade temperature range

8.3 Applications

- Sorting and decision-making logic
- Digital comparators in CPUs and ALUs
- Data prioritization circuits
- Control systems and digital instrumentation

8.4 Subcircuit

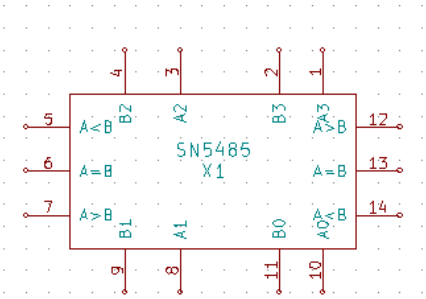

Figure 8.1: Subcircuit of SN5485

8.5 Subcircuit Schematic Diagram

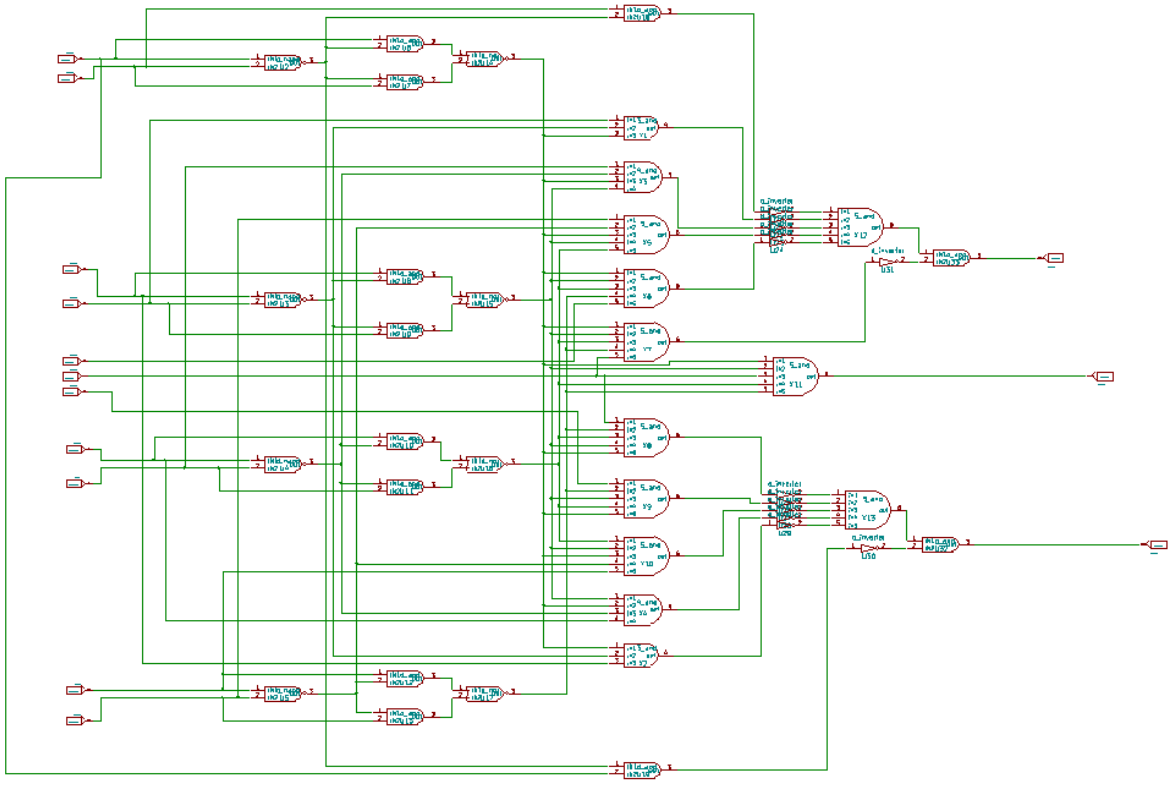

Figure 8.2: Subcircuit Schematic of the SN5485

8.6 Test Circuit

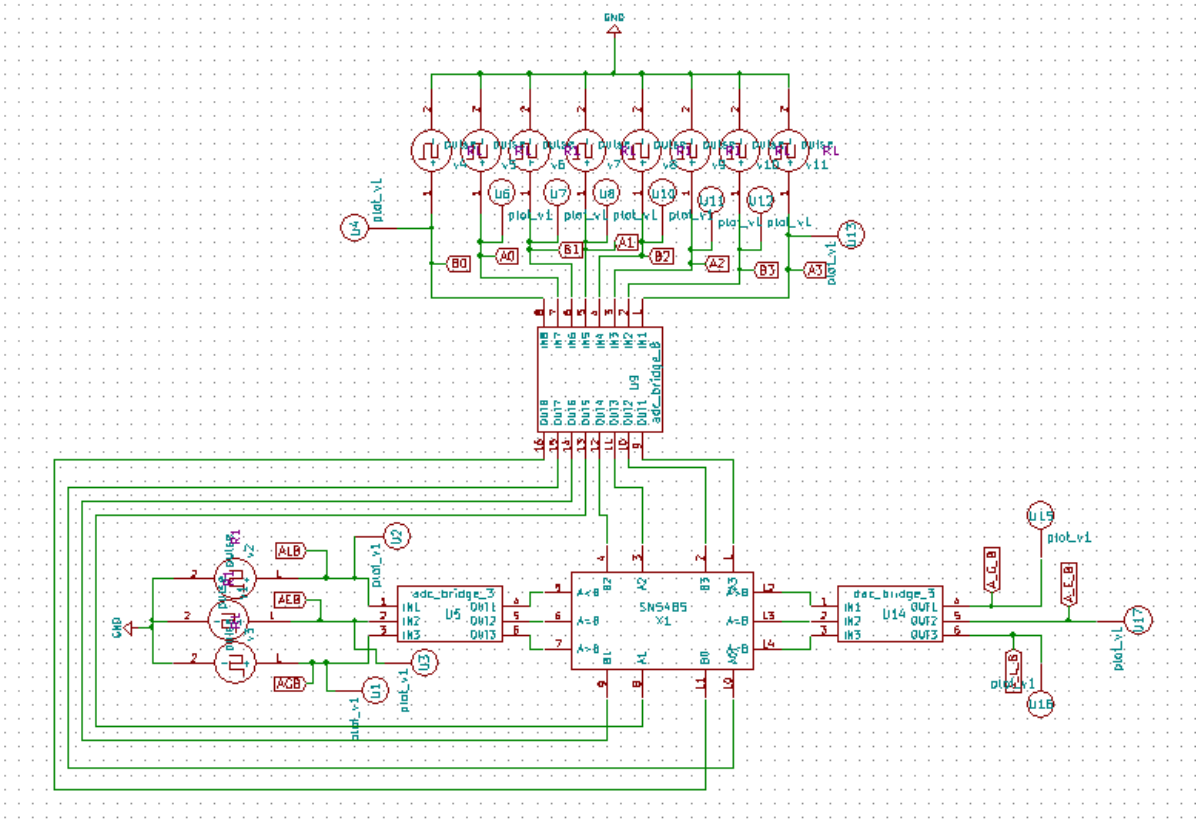

Figure 8.3: Test Circuit of the SN5485

8.7 Function Table

COMPARING INPUTS				CASCADING INPUTS			OUTPUTS		
A3, B3	A2, B2	A1, B1	A0, B0	A > B	A < B	A = B	A > B	A < B	A = B
A3 > B3	X	X	X	X	X	X	H	L	L
A3 < B3	X	X	X	X	X	X	L	H	L
A3 = B3	A2 > B2	X	X	X	X	X	H	L	L
A3 = B3	A2 < B2	X	X	X	X	X	L	H	L
A3 = B2	A2 = B2	A1 > B1	X	X	X	X	H	L	L
A3 = B3	A2 = B2	A1 < B1	X	X	X	X	L	H	L
A2 = B3	A2 = B2	A1 = B1	A0 > B0	X	X	X	H	L	L
A3 = B3	A2 = B2	A1 = B1	A0 < B0	X	X	X	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	H	L	L	H	L	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	L	H	L	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	X	X	H	L	L	H
A3 = B3	A2 = B2	A1 = B1	A0 = B0	H	H	L	L	L	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	L	L	L	H	H	L

Figure 8.4: Function Table of the SN5485

8.8 Output Plot

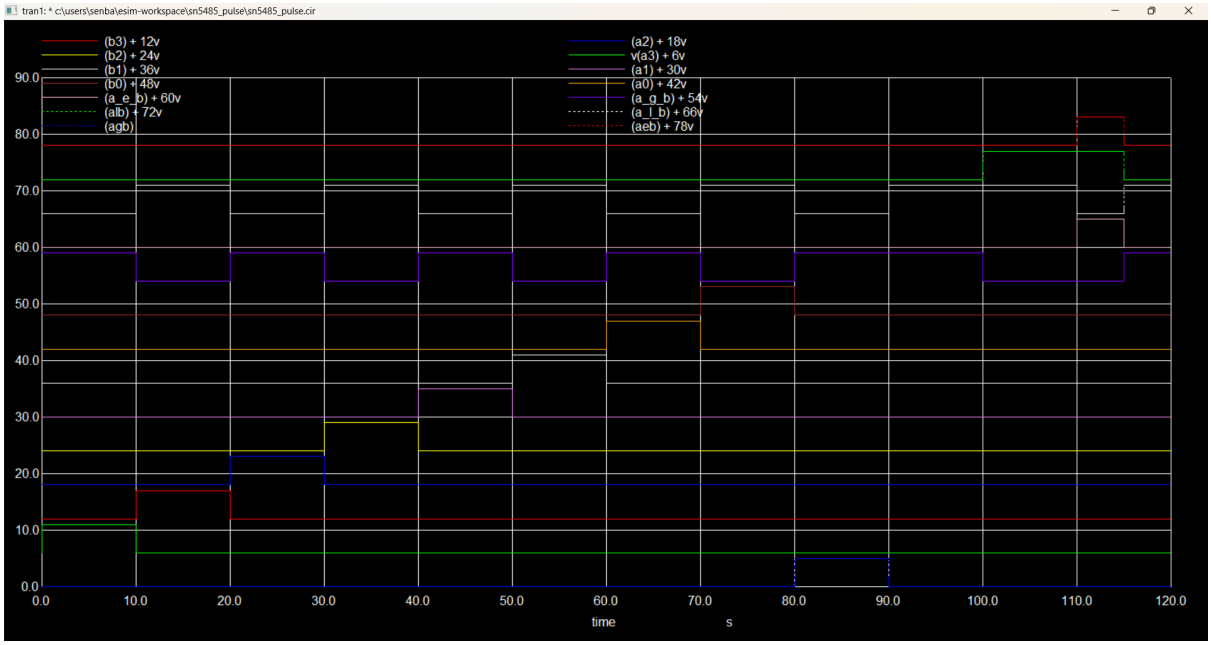

Figure 8.5: Output of the SN5485

Chapter 9

74LVC1G57

9.1 General Description

The 74LVC1G57 is a configurable logic gate that allows implementation of various 2-input logic functions such as AND, OR, NAND, NOR, XOR, and others, based on configuration inputs.
It belongs to the LVC (Low-Voltage CMOS) logic family, offering high-speed operation and low power consumption.
Designed for 1.65V to 5.5V operation, it is ideal for use in mixed-voltage systems and space-constrained applications.

9.2 Key Features

- Configurable 2-input logic gate (AND, OR, XOR, etc.)
- Operates from 1.65V to 5.5V supply
- High-speed CMOS with low power usage
- TTL-compatible inputs
- Small form factor, ideal for portable or dense designs

9.3 Applications

- Logic function replacement in embedded systems
- Signal conditioning and routing
- Compact control logic implementation
- General-purpose logic in space-limited designs

9.4 Subcircuit

Figure 9.1: Subcircuit of 74LVC1G57

9.5 Subcircuit Schematic Diagram

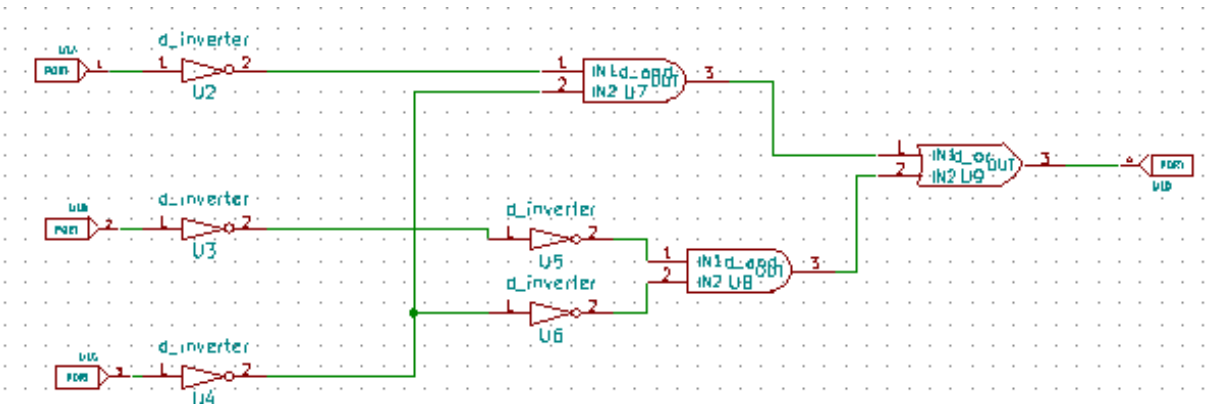

Figure 9.2: Subcircuit Schematic of the 74LVC1G57

9.6 Test Circuit

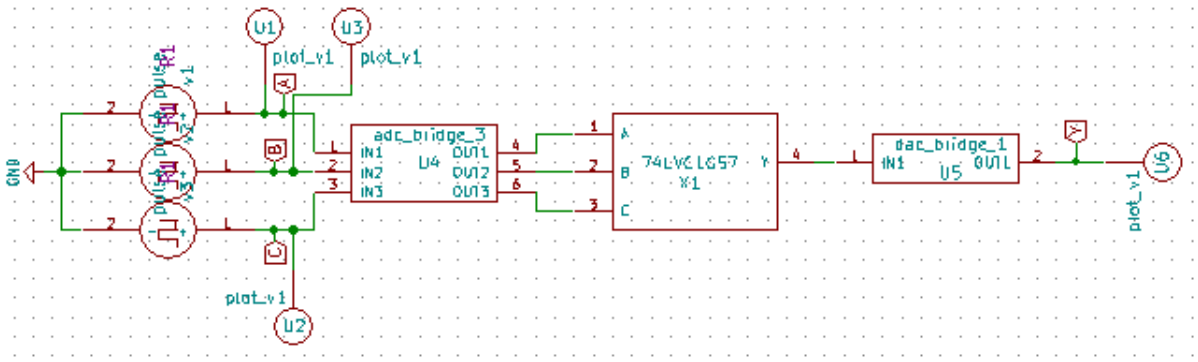

Figure 9.3: Test Circuit of the 74LVC1G57

9.7 Function Table

Input			Output
C	B	A	Y
L	L	L	H
L	L	H	L
L	H	L	H
L	H	H	L
H	L	L	L
H	L	H	L
H	H	L	H
H	H	H	H

Figure 9.4: Function Table of the 74LVC1G57

9.8 Output Plot

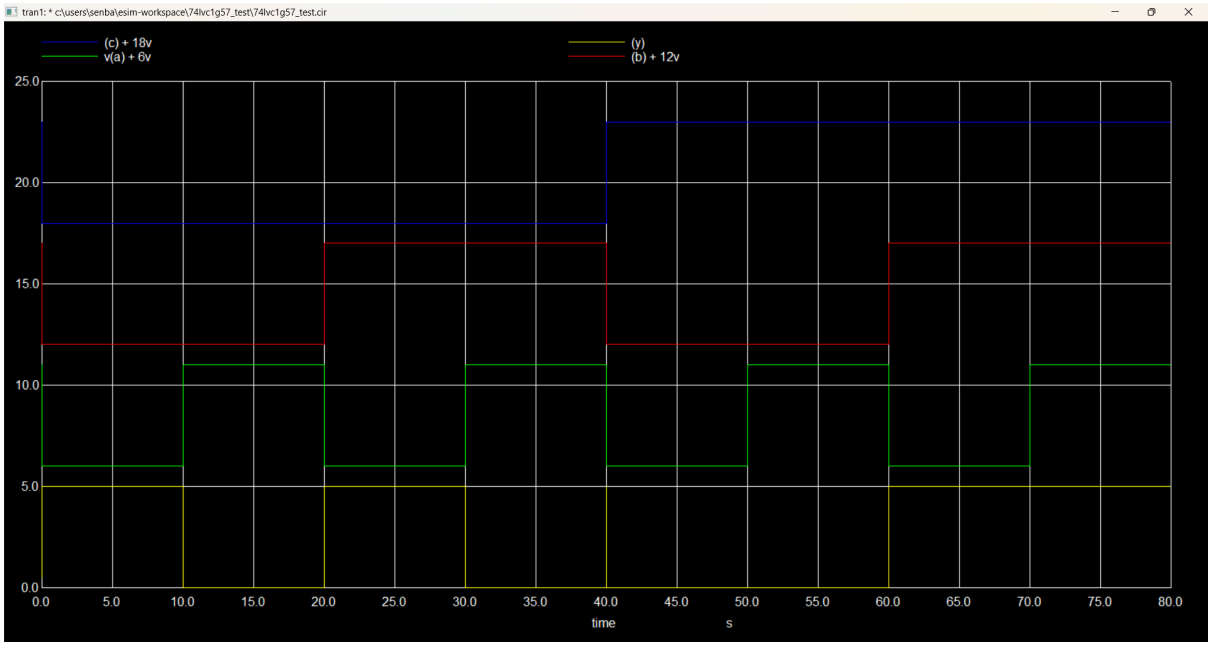

Figure 9.5: Output of the 74LVC1G57

Chapter 10

DM74LS279

10.1 General Description

The DM74LS279 is a quad S-R (Set-Reset) latch IC containing four independent latches with active-LOW S and R inputs. Each latch has a Q output and can be used for simple memory storage, control, or state-holding functions.
Built using low-power Schottky TTL technology, it offers reliable performance with low power consumption.
The IC operates on standard TTL voltage levels and is widely used in sequential logic and control systems.

10.2 Key Features

- Four independent S-R latches with active-LOW inputs
- Standard TTL voltage levels (4.75V – 5.25V)
- Low power consumption (LS family)
- Individual control of each latch
- Direct Q outputs for system interfacing

10.3 Applications

- Flip-flop and memory storage circuits
- Control logic and timing systems
- State holding in sequential digital systems
- Debouncing and signal latching applications

10.4 Subcircuit

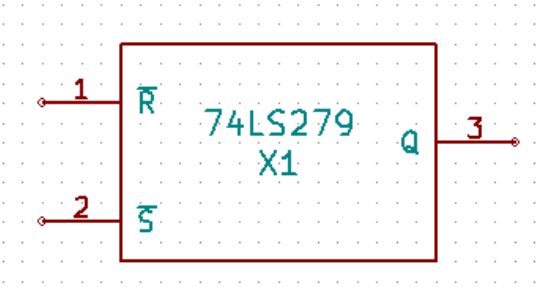

Figure 10.1: Subcircuit of DM74LS279

10.5 Subcircuit Schematic Diagram

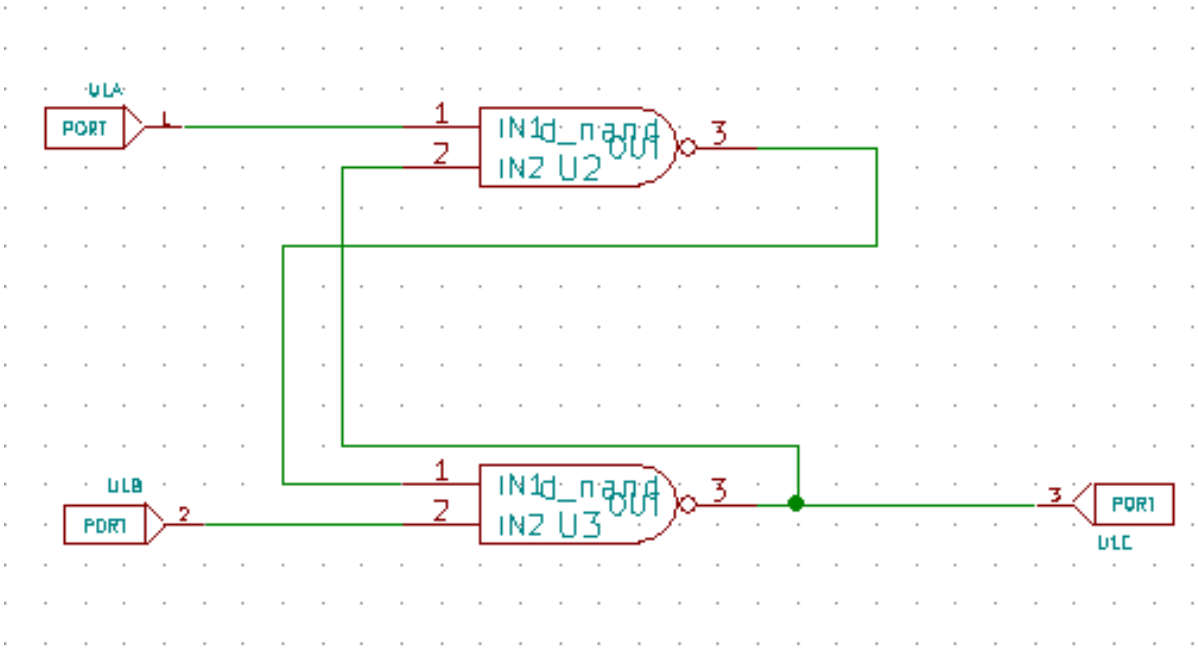

Figure 10.2: Subcircuit Schematic of the DM74LS279

10.6 Test Circuit

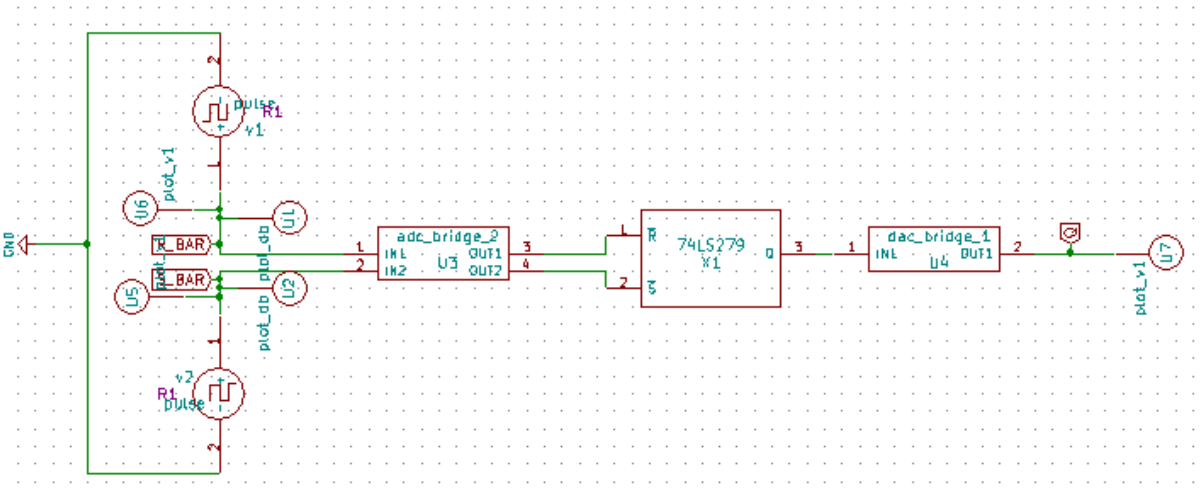

Figure 10.3: Test Circuit of the DM74LS279

10.7 Function Table

Inputs		Output
$\overline{S}$ (Note 1)	$\overline{R}$	Q
L	L	H (Note 2)
L	H	H
H	L	L
H	H	Q_0

Figure 10.4: Function Table of the DM74LS279

10.8 Output Plot

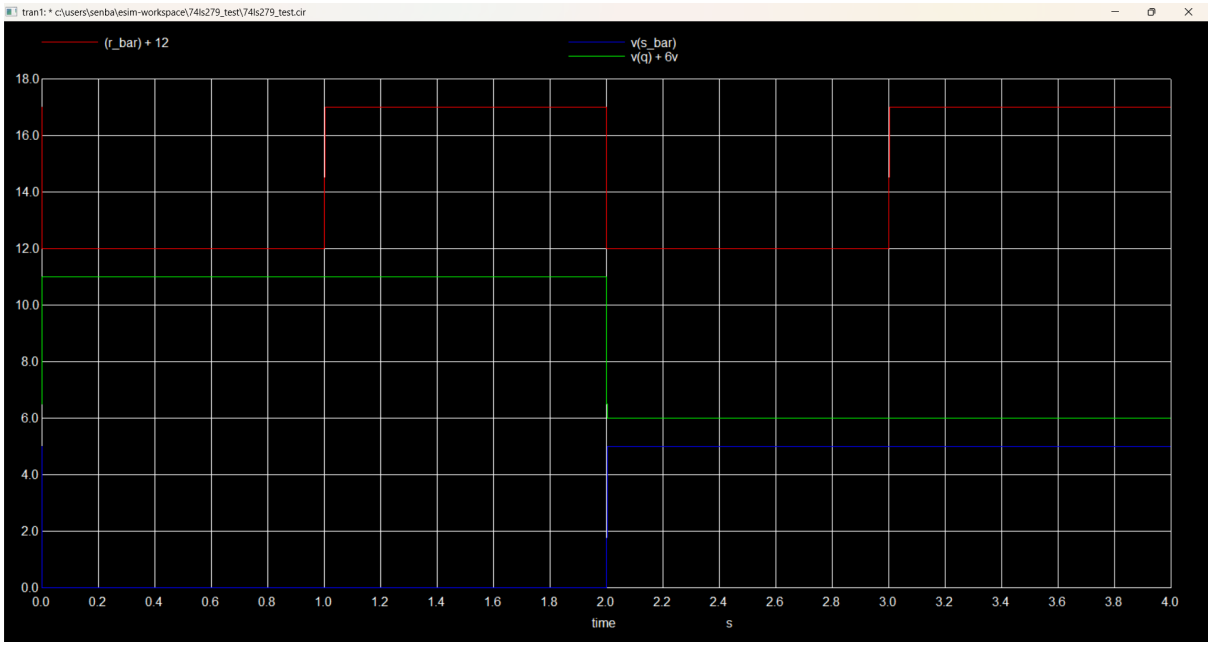

Figure 10.5: Output of the DM74LS279

Chapter 11

SN74LS76

11.1 General Description

The SN74LS76 is a dual J-K flip-flop with clear and preset inputs, featuring edge-triggered operation. Each flip-flop has J, K, clock (CLK), clear (CLR), and preset (PR) inputs along with Q and $\overline{Q}$ outputs.
It operates on standard TTL voltage levels and belongs to the LS (Low Power Schottky) series for reduced power consumption and faster switching speeds.
The IC provides reliable storage and toggling functionality in sequential logic designs.

11.2 Key Features

- Two independent J-K flip-flops with clear and preset
- Edge-triggered on the rising clock edge
- Standard TTL voltage operation (4.75V–5.25V)
- Synchronous toggling and control
- Low power consumption (LS series)

11.3 Applications

- Frequency division and counting
- Data storage and control circuits
- Sequential state machines
- Toggle flip-flop in logic designs

11.4 Subcircuit

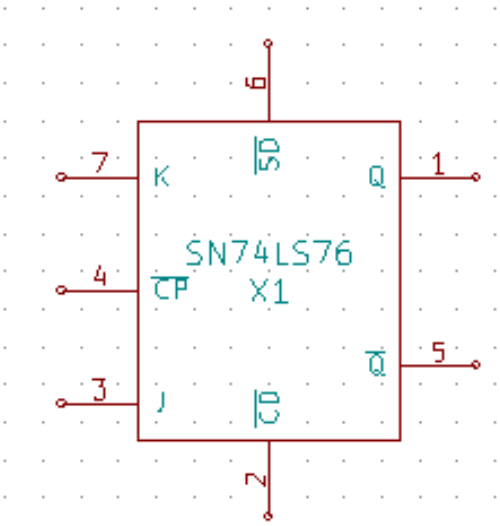

Figure 11.1: Subcircuit of SN74LS76

11.5 Subcircuit Schematic Diagram

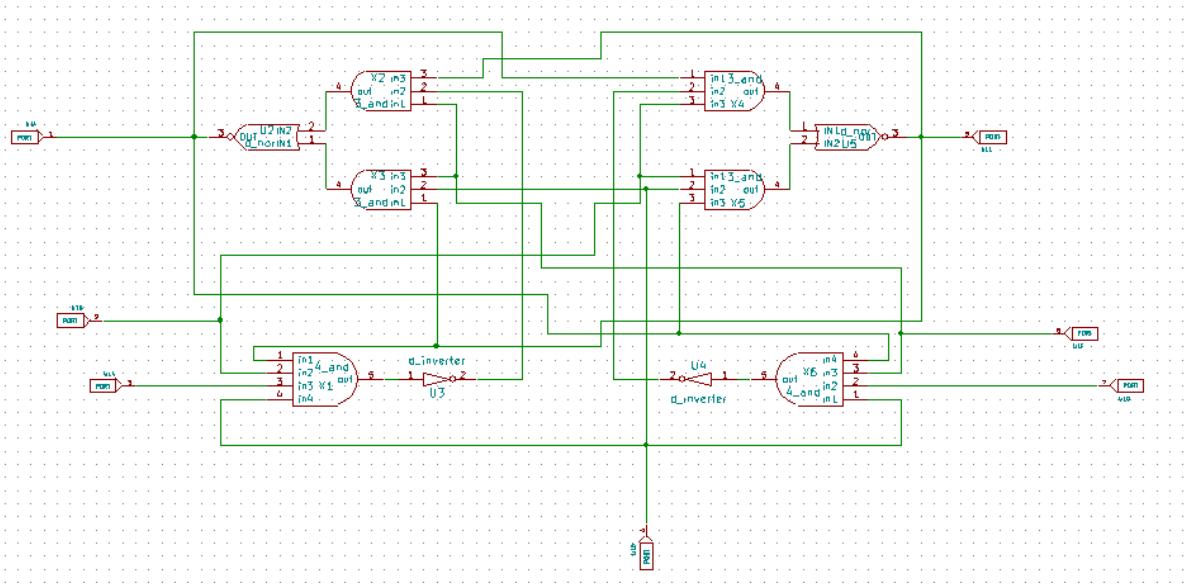

Figure 11.2: Subcircuit Schematic of the SN74LS76

11.6 Test Circuit

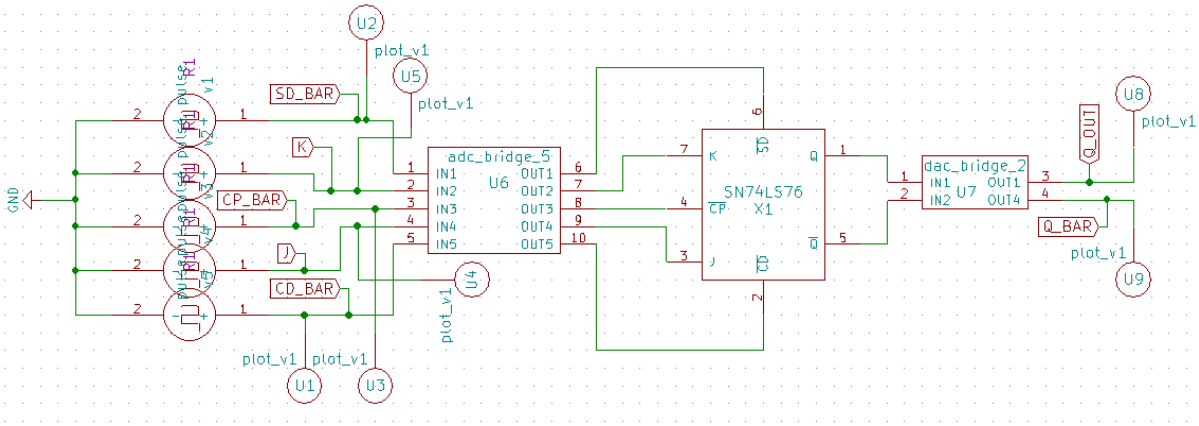

Figure 11.3: Test Circuit of the SN74LS76

11.7 Function Table

OPERATING MODE	INPUTS				OUTPUTS	
	$\overline{S}_D$	$\overline{C}_D$	J	K	Q	$\overline{Q}$
Set	L	H	X	X	H	L
Reset (Clear)	H	L	X	X	L	H
*Undetermined	L	L	X	X	H	H
Toggle	H	H	h	h	$\overline{q}$	q
Load "0" (Reset)	H	H	l	h	L	H
Load "1" (Set)	H	H	h	l	H	L
Hold	H	H	l	l	q	$\overline{q}$

Figure 11.4: Function Table of the SN74LS76

11.8 Output Plot

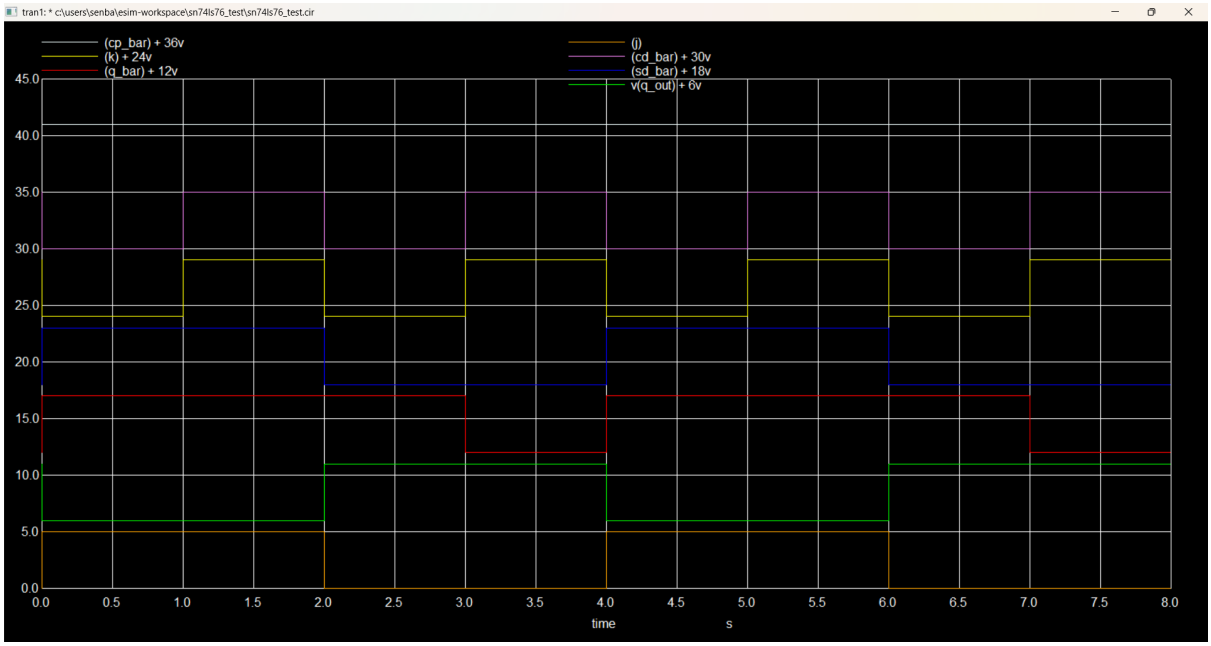

Figure 11.5: Output of the SN74LS76

Chapter 12

SN74LS47

12.1 General Description

The SN74LS47 is a BCD to 7-segment decoder/driver designed for driving common-cathode LED displays. It accepts a 4-bit binary-coded decimal (BCD) input and converts it into signals to display digits 0–9 on a 7-segment display.
Built using TTL logic, it includes features like lamp test, blanking input, and ripple-blanking output. The IC belongs to the LS (Low Power Schottky) series, offering low power consumption and reliable performance.

12.2 Key Features

- BCD to 7-segment decoder/driver
- Drives common-cathode LED displays
- Supports lamp test and blanking functions
- TTL-compatible inputs and outputs
- Low power consumption (LS series)

12.3 Applications

- Digital clocks and counters
- Numerical displays in embedded systems
- Instrumentation and measurement readouts
- LED display control logic

12.4 Subcircuit

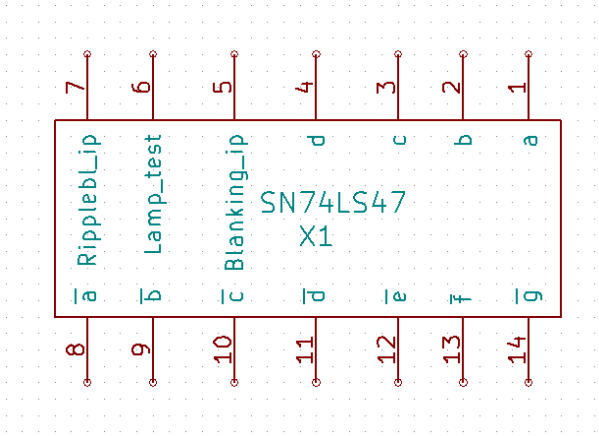

Figure 12.1: Subcircuit of SN74LS47

12.5 Subcircuit Schematic Diagram

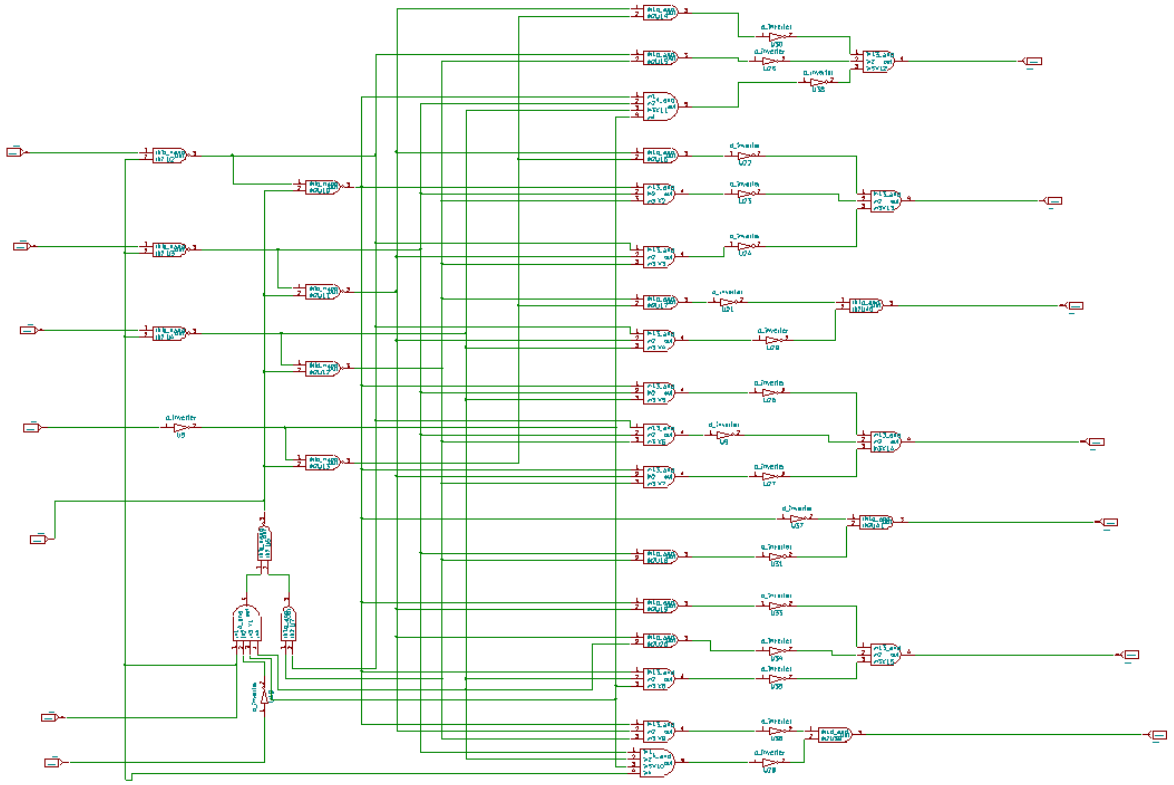

Figure 12.2: Subcircuit Schematic of the SN74LS47

12.6 Test Circuit

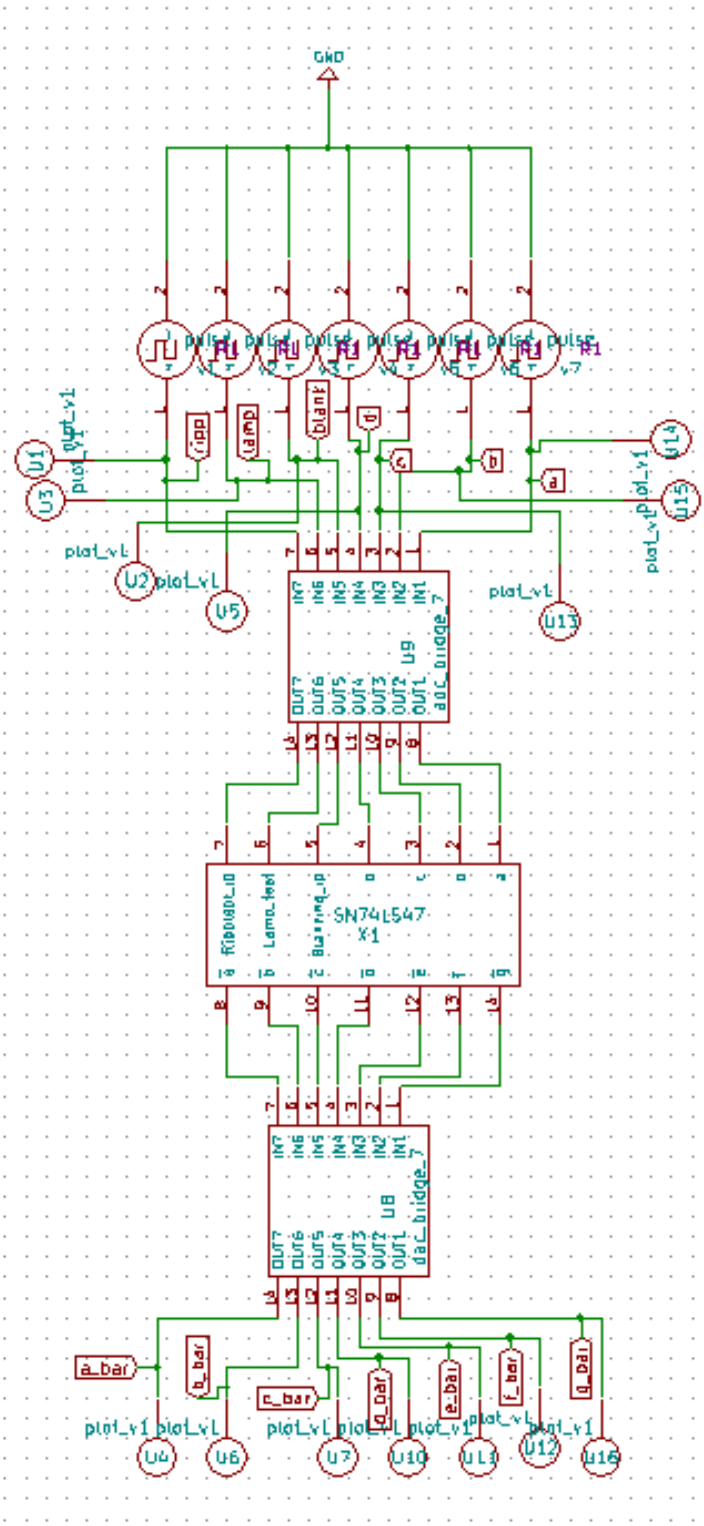

Figure 12.3: Test Circuit of the SN74LS47

12.7 Function Table

DECIMAL OR FUNCTION	INPUTS						$\overline{BI}/\overline{RBO}$†	OUTPUTS							NOTE
	$\overline{LT}$	$\overline{RBI}$	D	C	B	A		a	b	c	d	e	f	g	
0	H	H	L	L	L	L	H	H	H	H	H	H	H	L	1
1	H	X	L	L	L	H	H	L	H	H	L	L	L	L	
2	H	X	L	L	H	L	H	H	H	L	H	H	L	H	
3	H	X	L	L	H	H	H	H	H	H	H	L	L	H	
4	H	X	L	H	L	L	H	L	H	H	L	L	H	H	
5	H	X	L	H	L	H	H	H	L	H	H	L	H	H	
6	H	X	L	H	H	L	H	L	L	H	H	H	H	H	
7	H	X	L	H	H	H	H	H	H	H	L	L	L	L	
8	H	X	H	L	L	L	H	H	H	H	H	H	H	H	
9	H	X	H	L	L	H	H	H	H	H	L	L	H	H	
10	H	X	H	L	H	L	H	L	L	L	H	H	L	H	
11	H	X	H	L	H	H	H	L	L	H	H	L	L	H	
12	H	X	H	H	L	L	H	L	H	L	L	L	H	H	
13	H	X	H	H	L	H	H	H	L	L	H	L	H	H	
14	H	X	H	H	H	L	H	L	L	L	H	H	H	H	
15	H	X	H	H	H	H	H	L	L	L	L	L	L	L	
BI	X	X	X	X	X	X	L	L	L	L	L	L	L	L	2
RBI	H	L	L	L	L	L	L	L	L	L	L	L	L	L	3
LT	L	X	X	X	X	X	H	H	H	H	H	H	H	H	4

Figure 12.4: Function Table of the SN74LS47

12.8 Output Plot

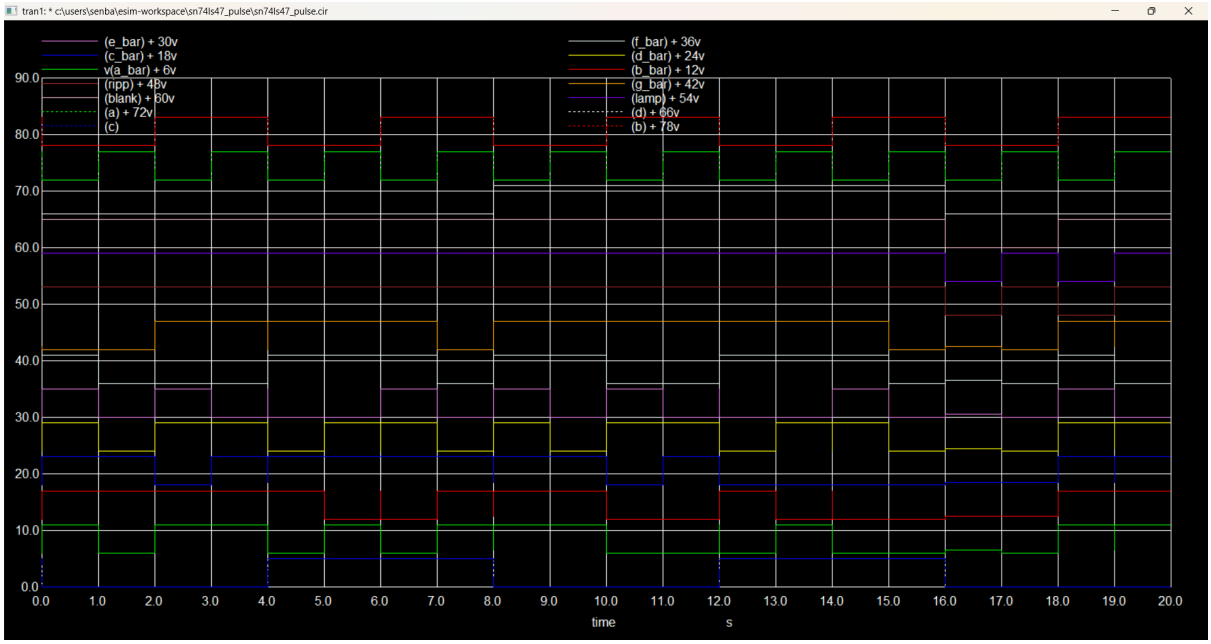

Figure 12.5: Output of the SN74LS47

Chapter 13

SN74LS42

13.1 General Description

The SN74LS42 is a 4-line to 10-line BCD (Binary-Coded Decimal) decoder with active-LOW outputs. It converts a 4-bit BCD input into one of ten mutually exclusive LOW outputs, making it suitable for driving devices like Nixie tubes or LED displays.
This IC is part of the LS (Low Power Schottky) TTL family, offering fast switching speeds and low power consumption for reliable digital decoding applications.

13.2 Key Features

- 4-to-10 line BCD decoder with active-LOW outputs
- Accepts standard TTL input logic levels
- Low power dissipation (LS series)
- High fan-out for driving multiple loads
- Fast decoding performance

13.3 Applications

- Decimal digit decoding
- Display driver circuits (e.g., Nixie or LED)
- Digital counters and timing systems
- Address decoding in control logic

13.4 Subcircuit

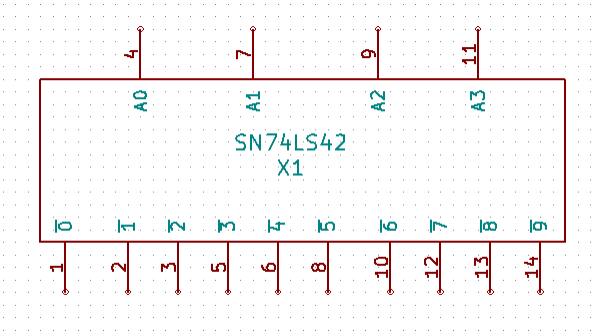

Figure 13.1: Subcircuit of SN74LS42

13.5 Subcircuit Schematic Diagram

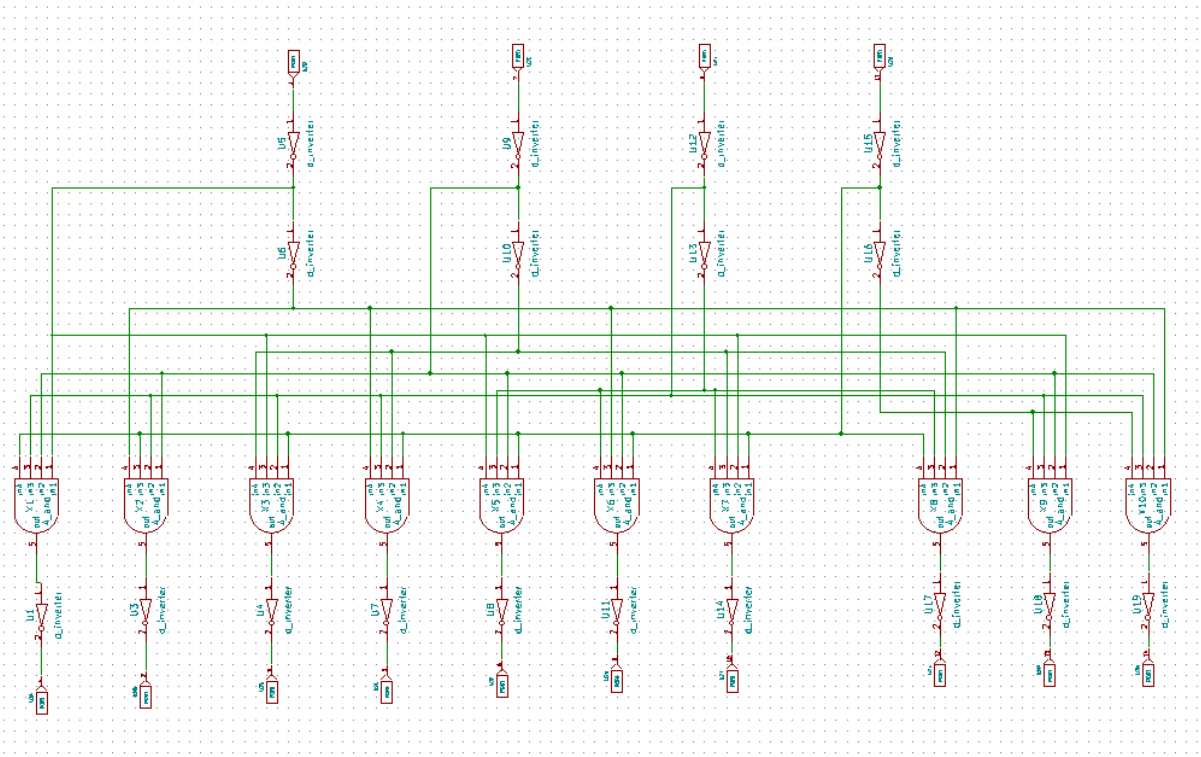

Figure 13.2: Subcircuit Schematic of the SN74LS42

13.6 Test Circuit

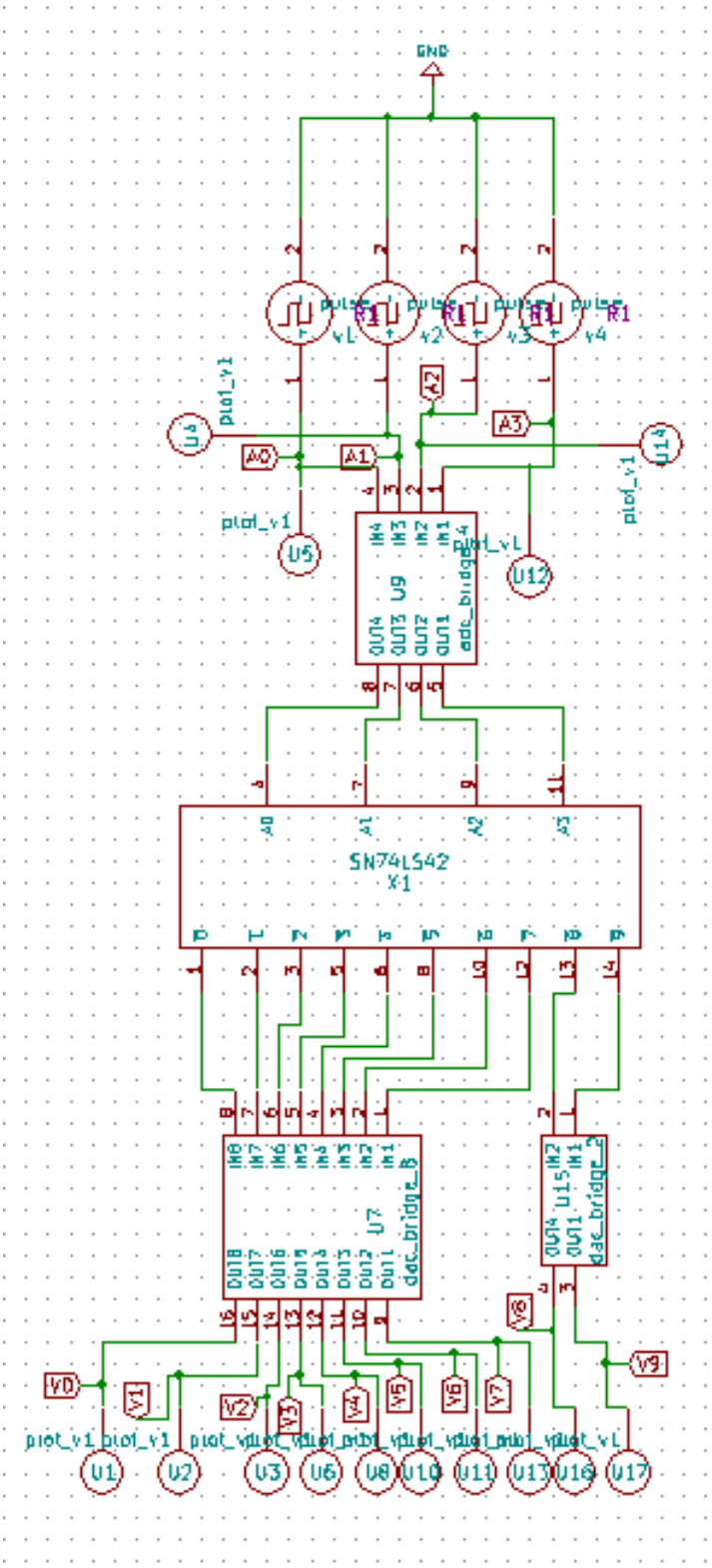

Figure 13.3: Test Circuit of the SN74LS42

13.7 Function Table

NO.	BCD INPUT				DECIMAL OUTPUT									
	D	C	B	A	0	1	2	3	4	5	6	7	8	9
0	L	L	L	L	L	H	H	H	H	H	H	H	H	H
1	L	L	L	H	H	L	H	H	H	H	H	H	H	H
2	L	L	H	L	H	H	L	H	H	H	H	H	H	H
3	L	L	H	H	H	H	H	L	H	H	H	H	H	H
4	L	H	L	L	H	H	H	H	L	H	H	H	H	H
5	L	H	L	H	H	H	H	H	H	L	H	H	H	H
6	L	H	H	L	H	H	H	H	H	H	L	H	H	H
7	L	H	H	H	H	H	H	H	H	H	H	L	H	H
8	H	L	L	L	H	H	H	H	H	H	H	H	L	H
9	H	L	L	H	H	H	H	H	H	H	H	H	H	L
INVALID	H	L	H	L	H	H	H	H	H	H	H	H	H	H
	H	L	H	H	H	H	H	H	H	H	H	H	H	H
	H	H	L	L	H	H	H	H	H	H	H	H	H	H
	H	H	L	H	H	H	H	H	H	H	H	H	H	H
	H	H	H	L	H	H	H	H	H	H	H	H	H	H
	H	H	H	H	H	H	H	H	H	H	H	H	H	H

Figure 13.4: Function Table of the SN74LS42

13.8 Output Plot

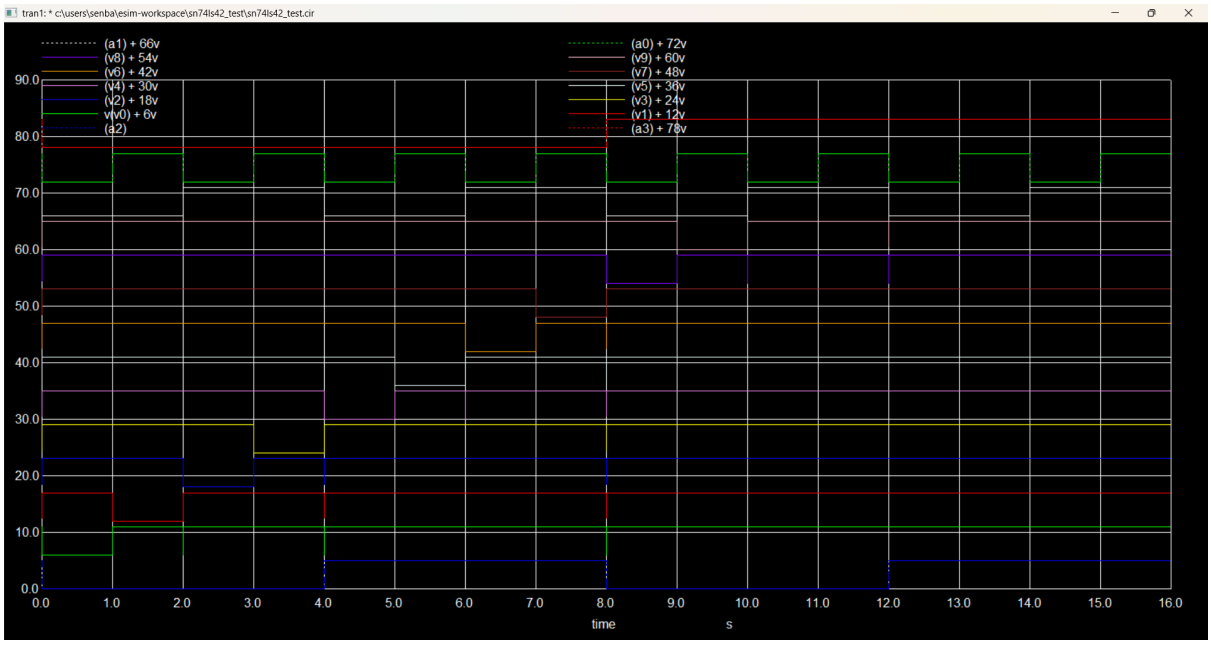

Figure 13.5: Output of the SN74LS42

Chapter 14

Conclusion and Future Scope

The project successfully fulfilled its objective of contributing a diverse set of accurately modeled digital logic ICs to the eSim subcircuit library. Each IC was implemented based on its official datasheet and rigorously tested through appropriate simulation testbenches to ensure its functional correctness and reliability. The contributions include a variety of fundamental digital components such as Adders, Encoders, Decoders, Multiplexers, Flip-Flops, Latches, Comparators, and Display Drivers.

These digital IC models serve as essential building blocks for designing and simulating complex digital systems, making them valuable resources for students, educators, and researchers using eSim. By integrating these verified models into the eSim library, the project has enhanced the platform's capability to support real-world digital logic design and experimentation.

This initiative not only reinforces the importance of open-source EDA tools in academic and research settings but also lays the groundwork for future developments. As the eSim device model library continues to grow, we anticipate a broader adoption among the engineering community and the creation of increasingly sophisticated circuits. The outcomes of this project thus represent a meaningful step forward in strengthening the ecosystem of accessible, open-source circuit simulation tools.

Chapter 15

Circuits Contribution

This chapter lists all the Integrated Circuits (ICs) contributed during the fellowship. Each IC has been carefully modeled and tested, and is now part of the eSim library. The contributions include both analog and digital ICs, covering a wide range of functionalities.

15.1 Senbagaseelan V – List of ICs

1. 74LS283 – 4-Bit Binary Full Adder with Fast Carry
2. 74HC147N – 10-to-4 Line Priority Encoder
3. SN74LVC1G139 – Single 2-to-4 Line Decoder/Demultiplexer
4. DM54154 – 4-Line to 16-Line Decoder/Demultiplexer
5. SN5485 – 4-Bit Magnitude Comparator
6. 74LVC1G57 – Configurable 2-Input Logic Gate
7. DM74LS279 – Quad S-R Latch
8. SN74LS76 – Dual J-K Flip-Flops with Clear and Preset
9. SN74LS47 – BCD to 7-Segment Decoder/Driver
10. SN74LS42 – BCD to Decimal Decoder (4-Line to 10-Line)

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