Semester Long Internship Report

On

IC Design Using subcircuit in eSim

Submitted by

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Under the guidance of

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Acknowledgment

I would like to express my sincere gratitude to the FOSSEE team at IIT Bombay for providing me with this valuable opportunity to work as a part of the eSim project. Being selected for this fellowship was a moment of pride, and the experience has truly been enriching, both technically and personally.

My heartfelt thanks to Prof. Kannan M. Moudgalya for initiating and leading this impactful platform that empowers students like me to explore the world of open-source electronics.

I am especially grateful to Mr. Sumanto Kar for his constant guidance, patience, and encouragement throughout the project. From understanding datasheets and research articles to navigating tools like GitHub and effectively using eSim, your support has been instrumental in shaping my learning experience. Your constructive feedback during reviews helped me approach problems with clarity and confidence.

When I started, I lacked hands-on experience with simulation tools and was unsure of my ability to complete a project independently. However, through this fellowship, I have not only built technical skills but also developed a sense of discipline, time management, and self-confidence.

I would also like to thank my fellow interns and team members for creating a collaborative, energetic, and friendly environment that made the journey more enjoyable.

This opportunity has significantly contributed to my growth, and I am proud to have been a part of the FOSSEE eSim team. I look forward to applying the knowledge gained here in future endeavors and contributing meaningfully to the open-source community.

Thank you, once again, to everyone who made this experience so memorable and impactful.

Contents

Chapter 1

Introduction

FOSSEE (Free/Libre and Open Source Software for Education) project promotes the use of FLOSS tools to improve the quality of education in our country. It aims to reduce dependency on proprietary software in educational institutions. It encourages the use of FLOSS tools through various activities to ensure commercial software is replaced by equivalent FLOSS tools. It also develops new FLOSS tools and upgrade existing tools to meet requirements in academia and research.[1]

The FOSSEE project is part of the National Mission on Education through Information and Communication Technology (ICT), Ministry of Human Resource Development (MHRD), Government of India.

1.1 eSim

eSim is a CAD tool that helps electronic system designers to design, test, and analyze their circuits. The important feature of this tool is that it is open source, allowing users to modify the source as per their needs. The software provides a generic, modular, and extensible platform for experimenting with electronic circuits. eSim is built using various free/libre and open-source software components in- cluding :

1.1.1 Kicad

Integrated software where all functions of circuit drawing, control, layout, library management, and access to the PCB design software are carried out.

1.1.2 Ngspice

Ngspice is a general-purpose circuit simulation program for nonlinear dc, nonlinear transient, and linear ac analysis.

1.1.3 KiCad to Ngspice converter

Analysis parameters,source details are provided through this module. It allows us to add and edit the device models and subcircuits included in the circuit schematic.

1.1.4 Subcircuit Builder

This module allows the user to create a subcircuit for a component. Once the subcircuit for a component is created, the user can use it in other circuits.

1.1.5 NGHDL

A module for mixed signal circuit simulation, is also integrated with eSim. It makes use of VHDL code.

1.1.6 NgVeri

NgVeri, a module for mixed signal circuit simulation, is also integrated with eSim. It makes use of Verilog/System Verilog/Transaction-Level Verilog code.

1.1.7 Makerchip

Makerchip is a cloud-based browser application developed by Redwood EDA to do digital circuit design. One can simulate Verilog/SystemVerilog/Transaction-Level Verilog code in Makerchip.

Chapter 2

Abstract

The objective of this internship was to design and develop various integrated circuits using the Subcircuit Builder Method in eSim. This involved modeling the ICs with eSim library files and subsequently simulating them with different circuits. The goal was to expand the eSim Subcircuit Library for future use, enhancing its utility and application in educational and practical scenarios.

2.1 Approach

- entify and research an integrated circuit (IC) that is not currently available in the eSim library.
- Obtain and study the datasheet of the selected IC thoroughly.
- Carefully examine the schematic provided in the datasheet.
- Accurately recreate the schematic in eSim using the Subcircuit Builder Method.
- Model the IC in eSim, ensuring all parameters and configurations match those in the datasheet.
- Simulate the integrated circuit within eSim, testing it with various circuits to verify its functionality.
- Document the process and results to contribute to the future use and expansion of the eSim Subcircuit Library.

Chapter 3

Integrated Circuit Design

3.1 SN7448A

3.1.1 Description

The 7448 is a BCD-to-7-segment decoder/driver IC. It converts a four-bit Binary Coded Decimal (BCD) input into a 7-segment display pattern. This allows it to display decimal numbers from 0 to 9 on a 7-segment display. The 7448 is commonly used in digital clocks, counters, and other devices that need to display numeric information

Features of SN7448A

- BCD Input: Accepts a 4-bit BCD input (A, B, C, and D).
- 7-Segment Output: Provides seven outputs (a, b, c, d, e, f, and g) to drive the 7-segment display.
- Decoder/Driver: Converts the BCD input into the appropriate 7-segment pattern and provides the necessary current to illuminate the segments.
- Common Cathode: The 7448 is designed for use with common-cathode LED displays.
- Applications: Used in digital clocks, counters, calculators, and other devices requiring numeric displays

3.1.2 Pin Diagram

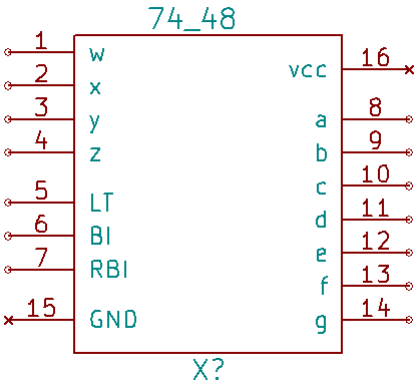


Figure 3.1: Pin Diagram of SN7448A

3.1.3 Subcircuit Diagram

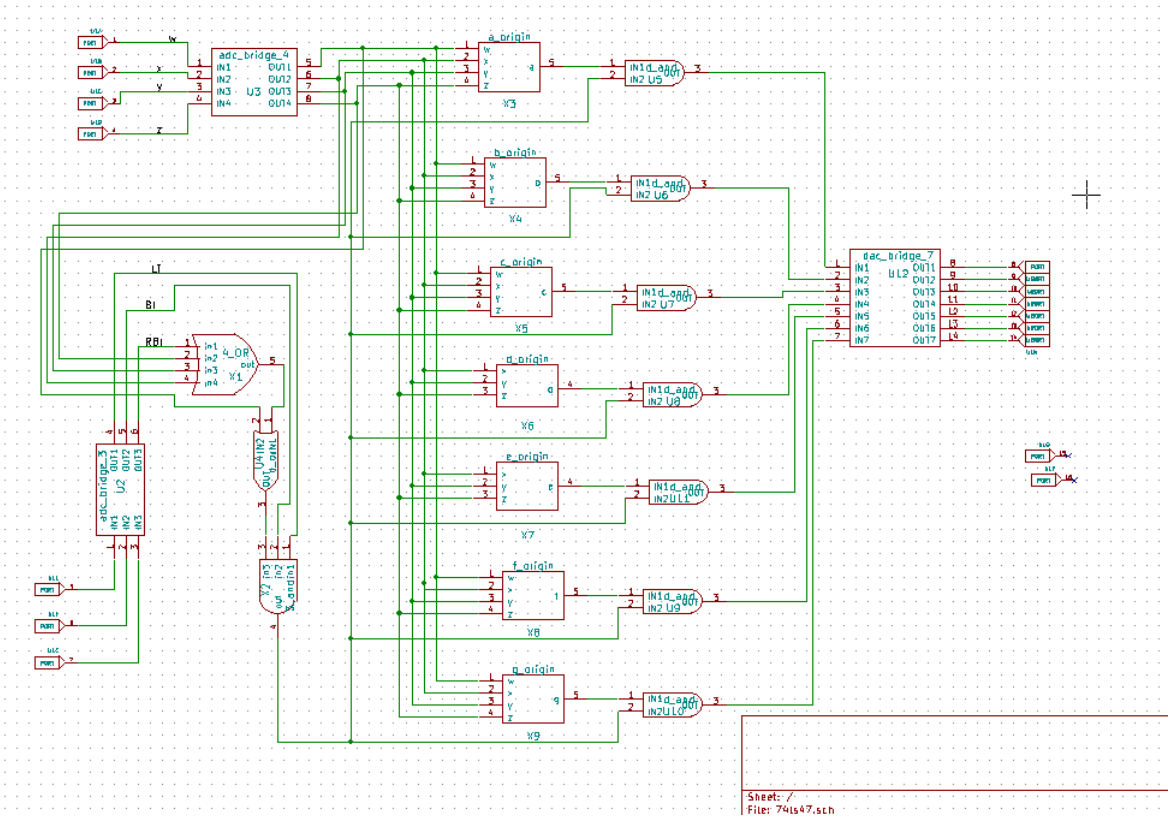
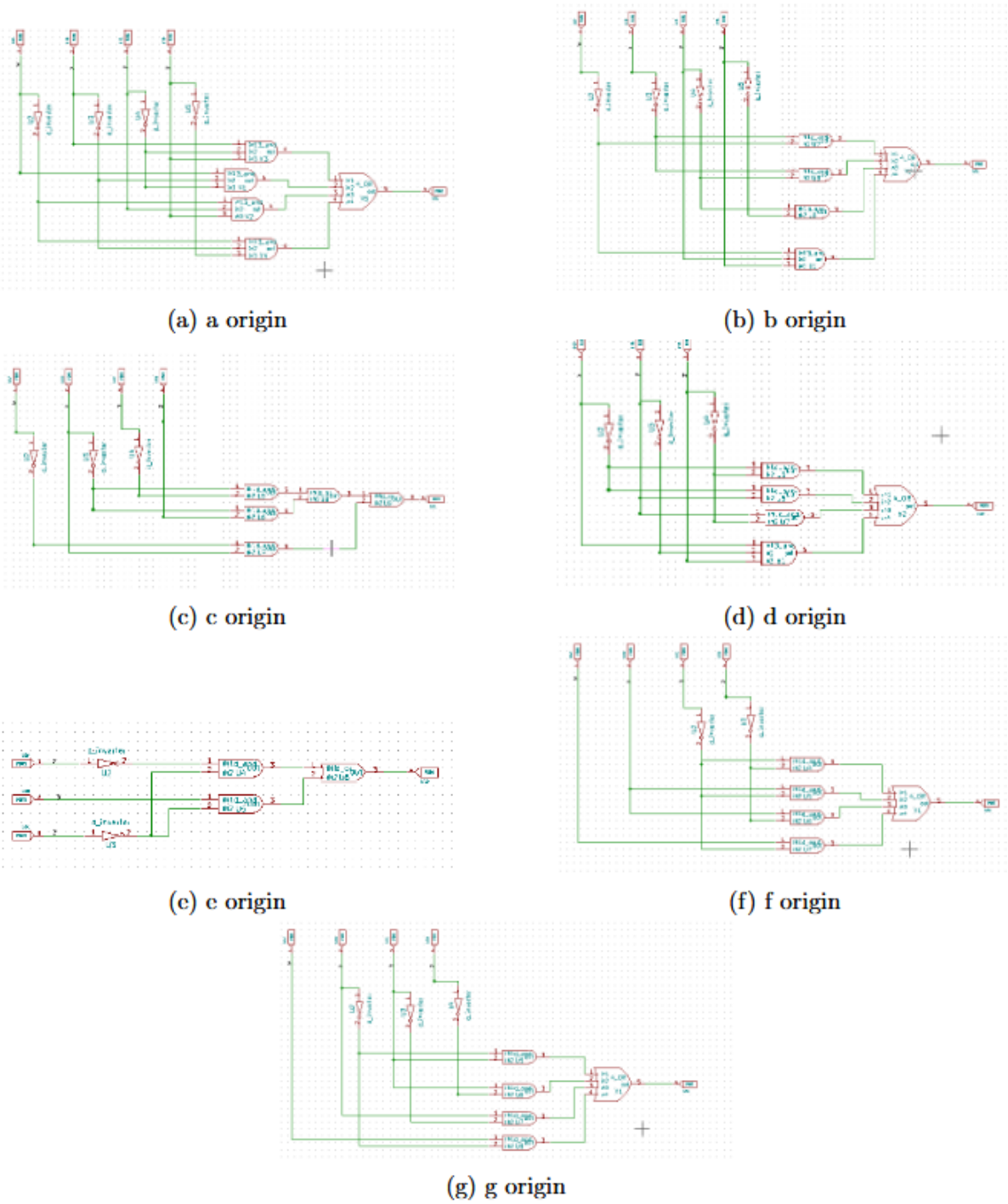


Figure 3.2: Subcircuit of SN7448A

Internal Schematic



(a) a origin

(b) b origin

(c) c origin

(d) d origin

(e) e origin

(f) f origin

(g) g origin

Figure 3.3: Internal Schematic

3.1.4 Test Circuit

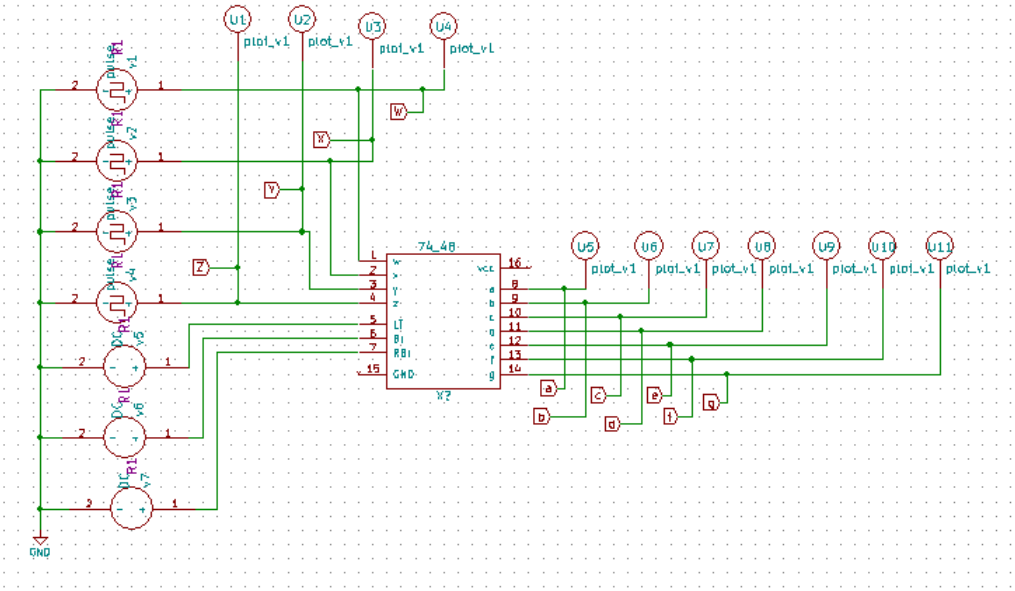


Figure 3.4: Test Circuit of SN7448A

3.1.5 NgSpice Plot

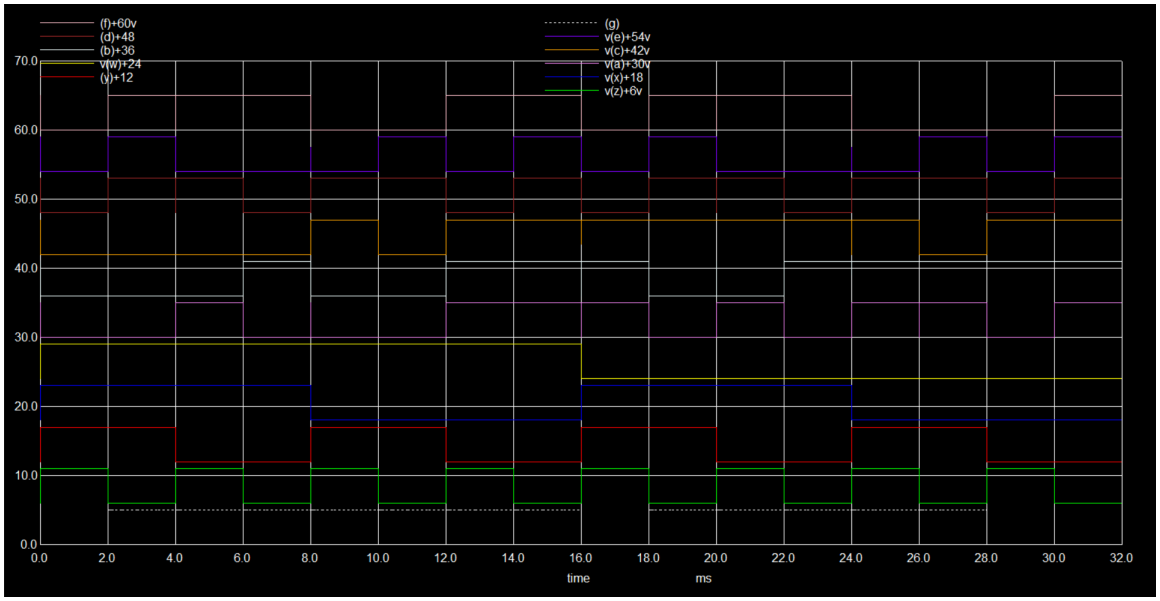


Figure 3.5: Simulation Diagram of SN7448A

3.2 SN53F283

3.2.1 Description

The F283 is a full adder that performs the addition of two 4-bit binary words. The sum outputs are provided for each bit and the resultant carry (C4) output is obtained from the fourth bit.

The device features full internal look-ahead across all four bits generating the carry term C4 in typically 5.7 ns. This capability provides the system designer with partial look-ahead performance at the economy and reduced package count of a ripple-carry implementation.

The adder logic, including the carry, is implemented in its true form. End-around carry can be accomplished without the need for logic or level inversion. The F283 can be used with either all-active-high (positive logic) or all-active-low (negative logic) operands.

Features of SN53F283

- 4-bit Binary Full Adder: It adds two 4-bit binary numbers, along with a carry-in, to produce a 4-bit sum and a carry-out.
- Fast Carry: The device includes an internal look-ahead circuit for fast carry generation, typically within a few nanoseconds. This allows for faster arithmetic operations compared to ripple-carry adders.
- Sum and Carry Outputs: It provides sum outputs for each of the four bits and a carry output (C4) from the fourth bit.
- Versatile Application: The 283 IC can be used in various applications, including arithmetic logic units (ALUs), counters, and other digital circuits where binary addition is needed.
- TTL/CMOS Compatibility: Some variations like the CD74ACT283 are designed for CMOS operation and may also be compatible with TTL logic levels, offering flexibility in circuit design.

3.2.2 Pin Diagram

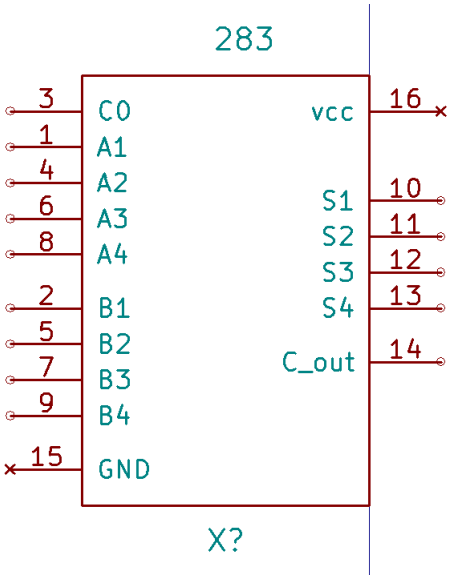


Figure 3.6: Pin Diagram of SN53F283

3.2.3 Subcircuit Diagram

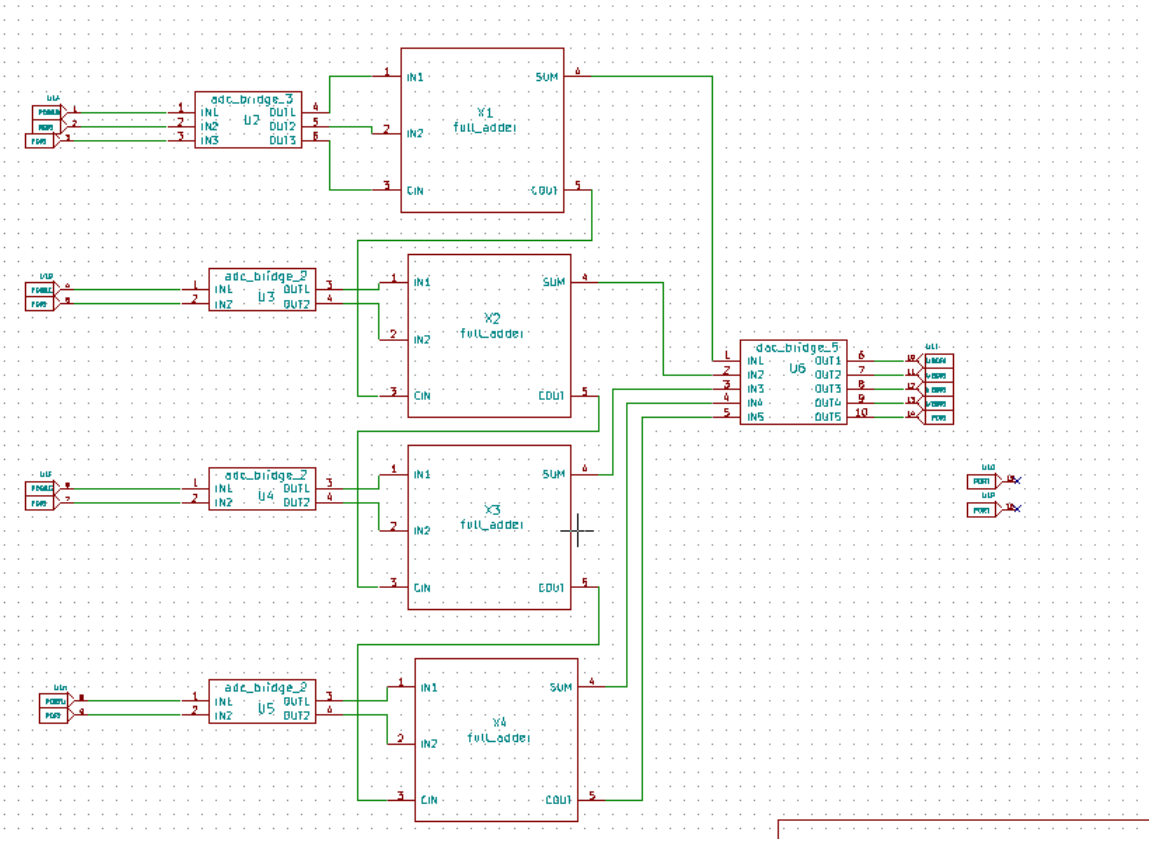


Figure 3.7: Subcircuit of SN53F283

3.2.4 Test Circuit

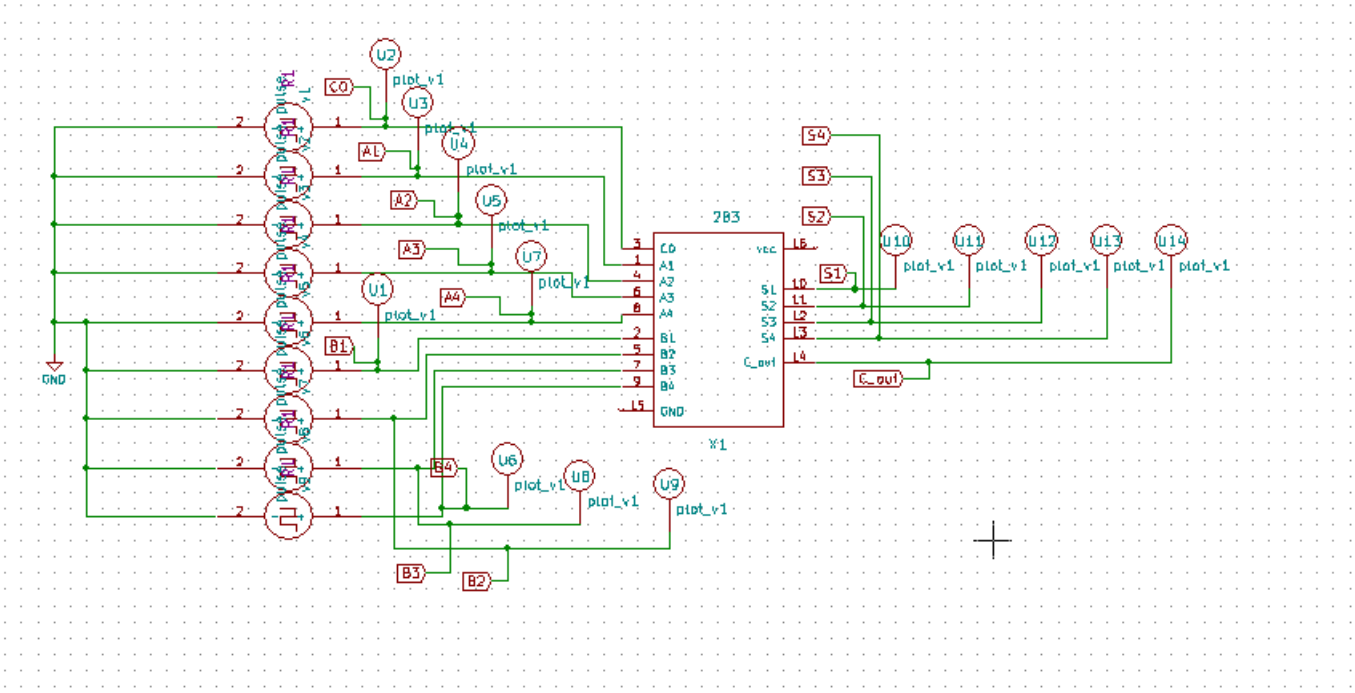


Figure 3.8: Test Circuit of SN53F283

3.2.5 NgSpice Plot

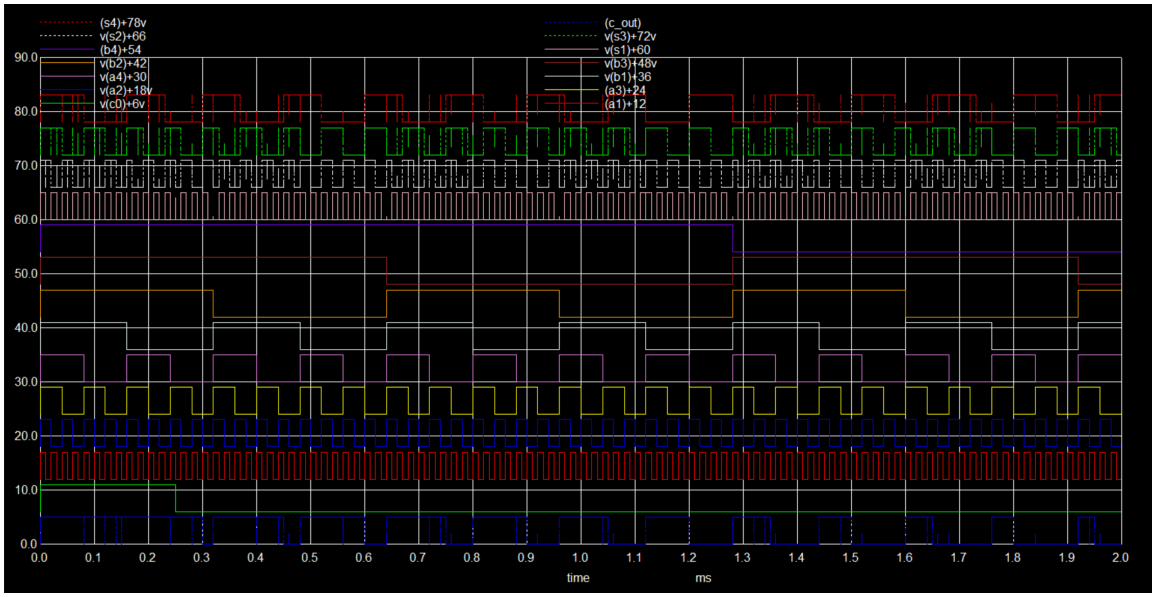


Figure 3.9: Simulation Diagram of SN53F283

3.3 SN54LS375

3.3.1 Description

The SN54 / 74LS375 is a 4-Bit D-Type Latch for use as temporary storage for binary information between processing limits and input /output or indicator units. When the Enable (E) is HIGH, information present at the D input will be transferred to the Q output and, if E is HIGH, the Q output will follow the input. When E goes LOW, the information present at the D input prior to its setup time will be retained at the Q outputs.

Features of SN54LS375

- 4-Bit D-Type Transparent Latch Temporarily stores 4 bits of data with common enable control.
- Transparent Operation When the Enable (C) is high, data at D inputs appears at Q outputs. When Enable goes low, the last input data is latched (stored).
- TTL-Compatible Inputs and Outputs Fully compatible with standard TTL logic levels.
- Fast Switching Speed Typical propagation delay: 5–10 ns.
- Wide Operating Temperature Range Suitable for military use: 55°C to +125°C.
- Low Power Schottky (LS) Design Part of the LS-TTL family, ensuring low power consumption with high speed.
- Diode-Clamped Inputs Helps suppress voltage spikes and minimizes noise.
- Standard Power Supply Requirement Operates at +5V (typically 4.75V to 5.25V).

3.3.2 Pin Diagram

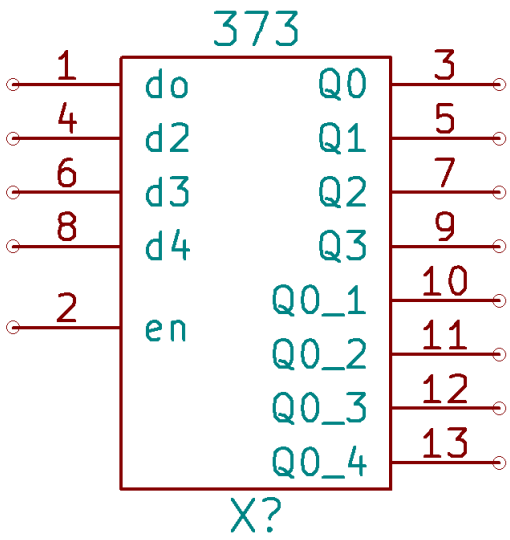


Figure 3.10: Pin Diagram of SN54LS375

3.3.3 Subcircuit Diagram

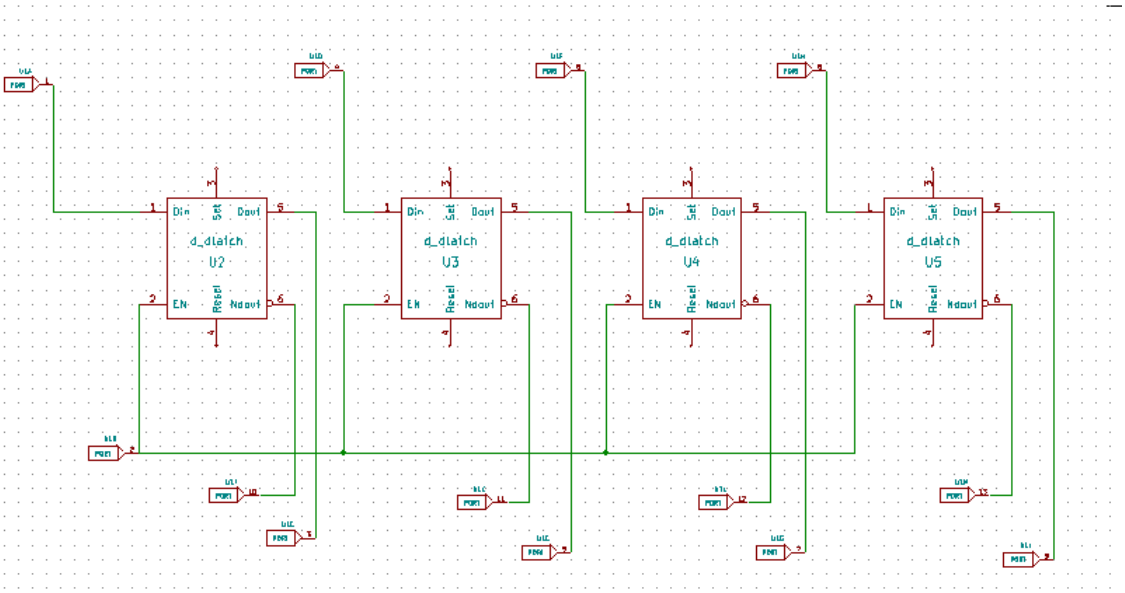


Figure 3.11: Subcircuit of SN54LS375

3.3.4 Test Circuit

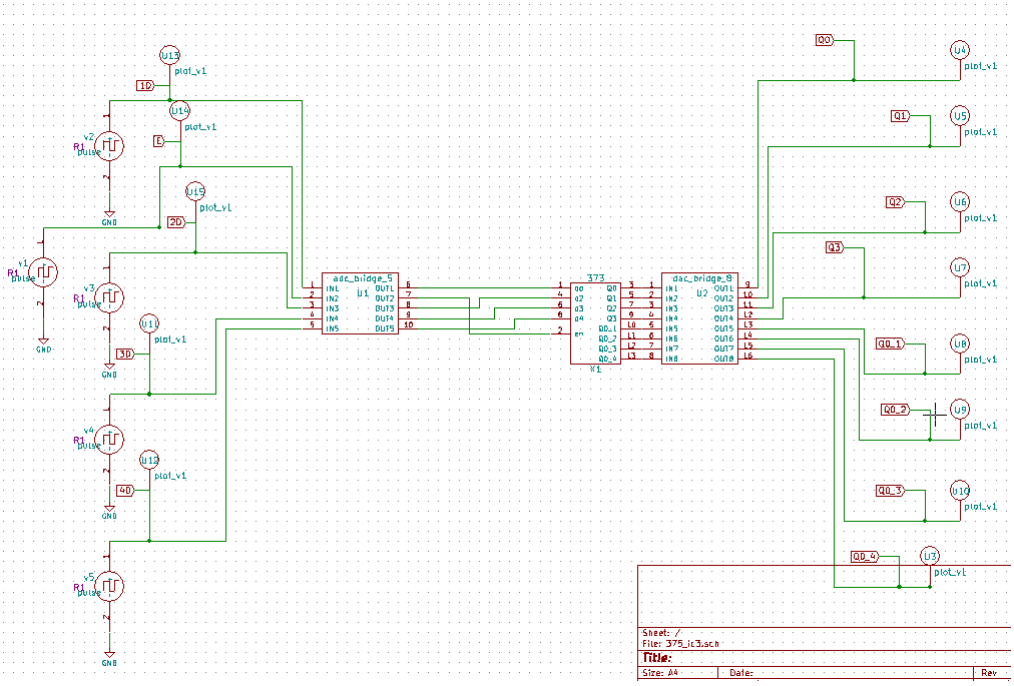


Figure 3.12: Test Circuit of SN54LS375

3.3.5 Python Plot

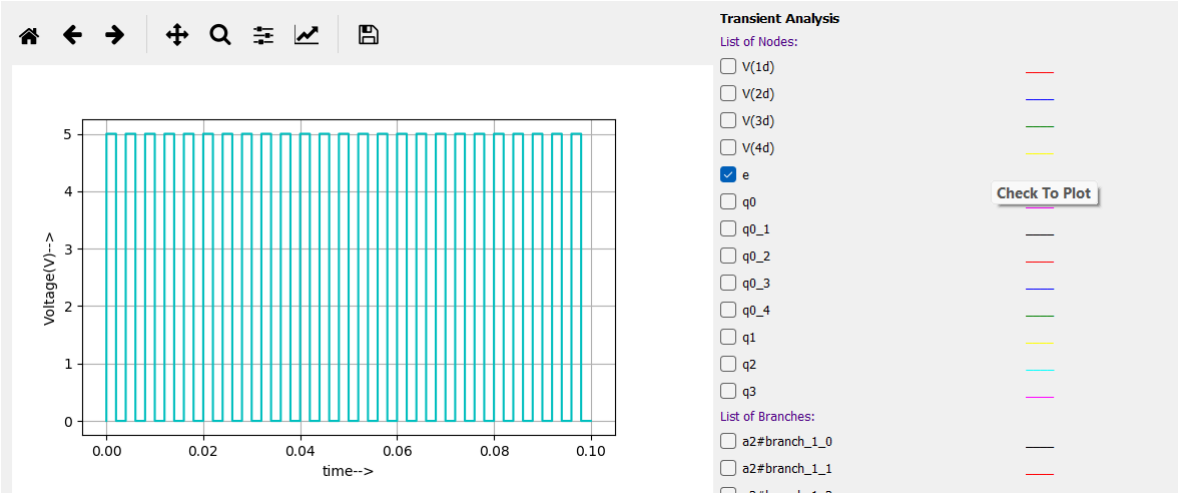


Figure 3.13: enable

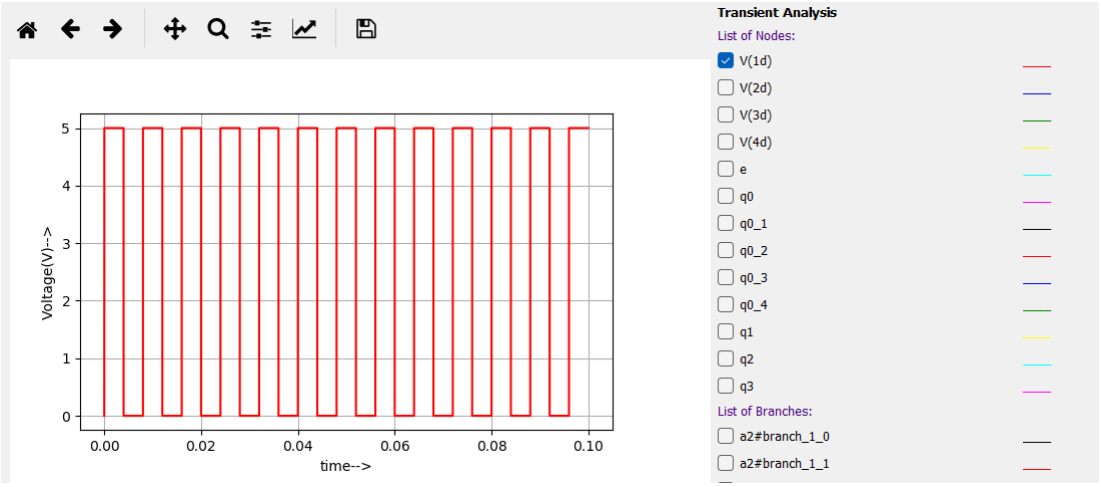


Figure 3.14: D input

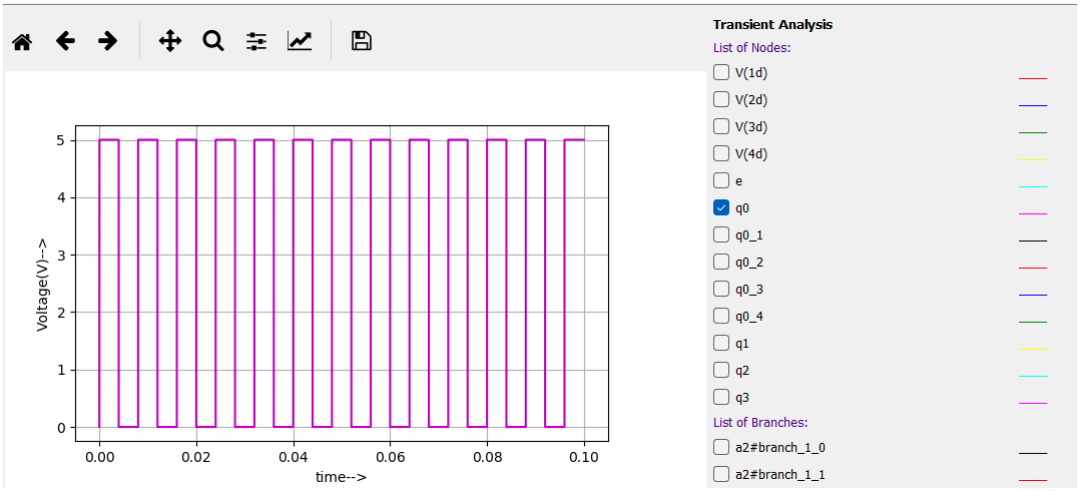


Figure 3.15: D output

3.4 SN4ALS573C

3.4.1 Description

These D-type octal transparent latches feature 3-state outputs designed specifically to drive highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

While the latch-enable (LE) input is high, the outputs (Q) respond to the data (D) input. When LE is low, the outputs are latched to retain the data that was set up.

A buffered output enable (OE) input can be used to place the eight outputs in either a normal logic state (high or low) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high impedance state and the increased drive provide the capability to drive bus lines without interface or pull-up components.

OE does not affect the internal operation of the latches. Old data can be retained, or new data can be entered while the outputs are in the high-impedance state.

Features of SN4ALS573C

- Octal D-Type transparent latch: 8 bit storage capability (D0–D7).
- Data are transparent (i.e., the output follows the input) when the latch enable (LE) is HIGH.
- Acts as a latch between the CPU and data/address bus.
- Allows temporary data storage for multiplexed bus communication.
- Used to latch address or data lines.

3.4.2 Pin Diagram

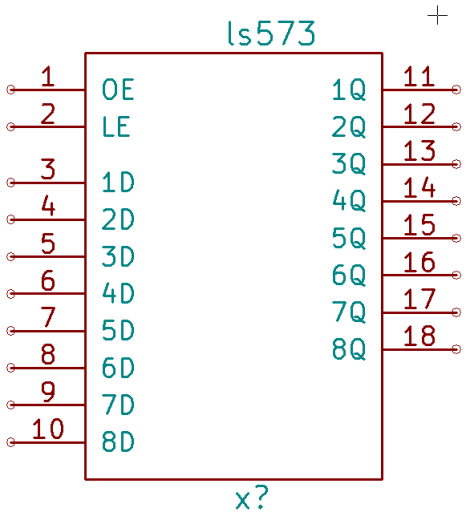


Figure 3.16: Pin Diagram of SN54LS573C

3.4.3 Subcircuit Diagram

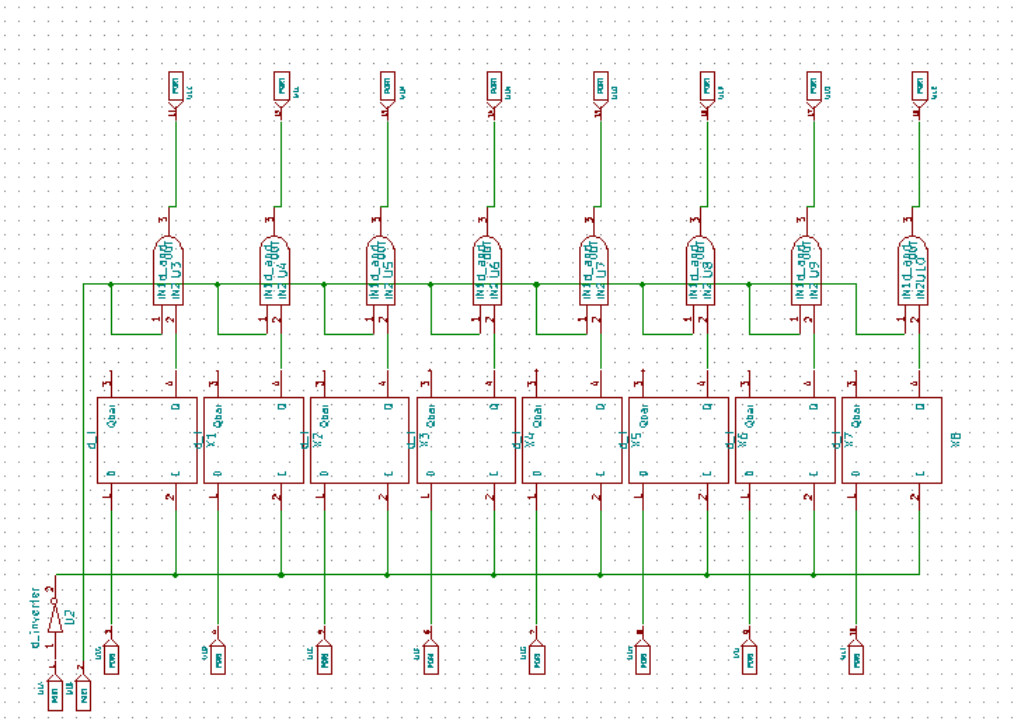


Figure 3.17: Subcircuit of SN54LS573C

3.4.4 Test Circuit

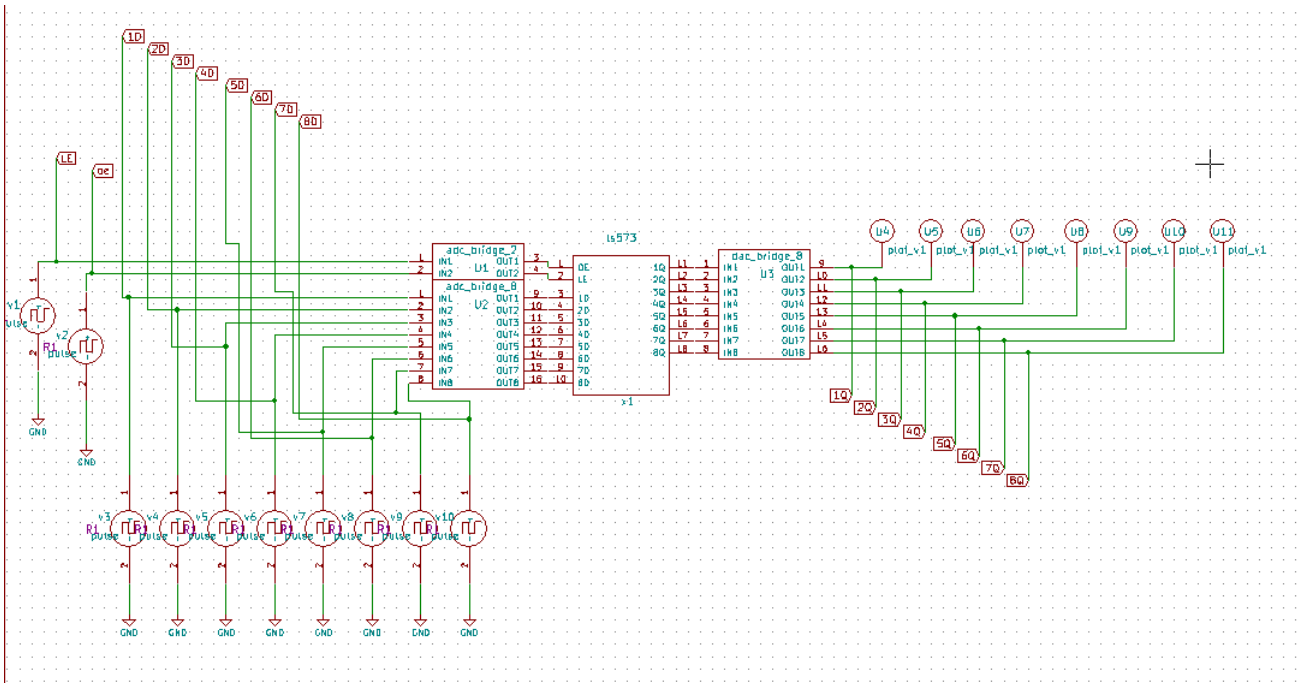


Figure 3.18: Test Circuit of SN54LS573C

3.4.5 Python Plot

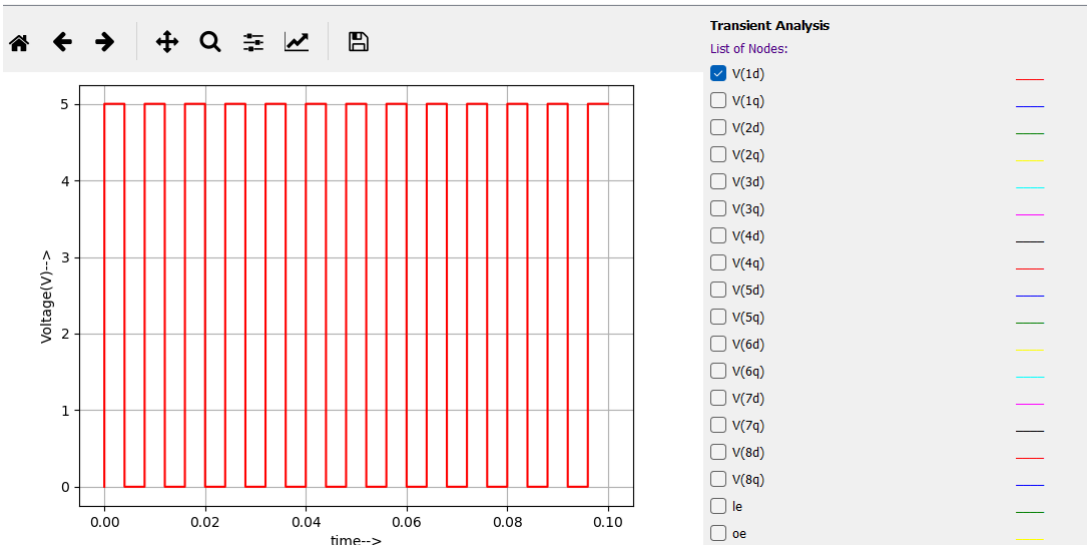


Figure 3.19: D input

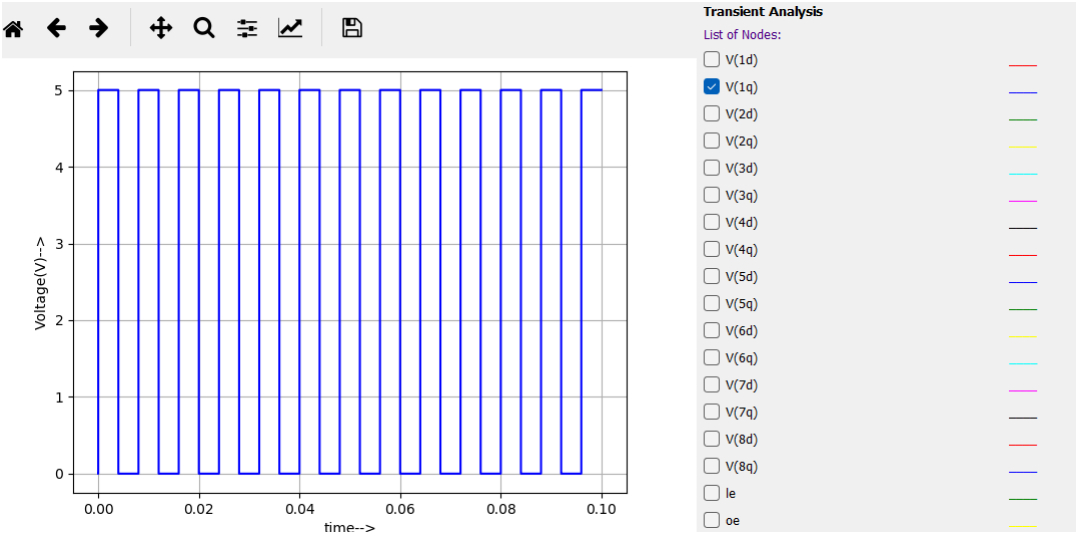


Figure 3.20: Q output

3.5 SN54ALS133

3.5.1 Description

The SN554ALS133 is a 13-input positive-NAND gate, typically used in military and high-reliability applications. It implements a single gate with 13 independent inputs, outputting a logic LOW only when all 13 inputs are at logic HIGH. This IC is part of the ALS (Advanced Low-power Schottky) series, offering faster switching speeds and lower power consumption compared to standard TTL logic.

Features of SN54ALS133

- Single 13-input NAND gate
- TTL-compatible inputs and outputs
- Fast switching speeds due to ALS technology
- Low power consumption
- Schottky clamping for improved performance
- Military-grade (SN554ALS133) variant for high-reliability applications
- Wide operating temperature range: 55°C to +125°C
- Balanced propagation delays Logic control systems where a large number of conditions must be checked simultaneously
- Digital systems requiring wide-input logic decisions

3.5.2 Pin Diagram

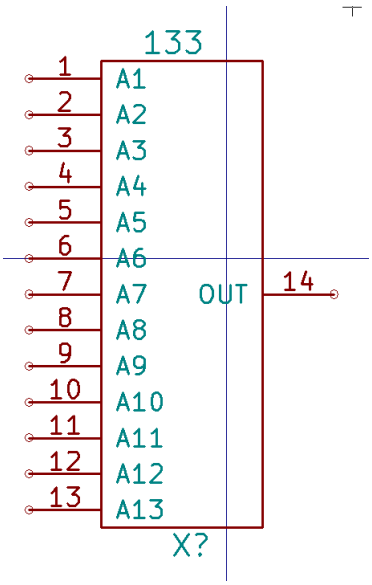


Figure 3.21: Pin Diagram of SN54ALS133

3.5.3 Subcircuit Diagram

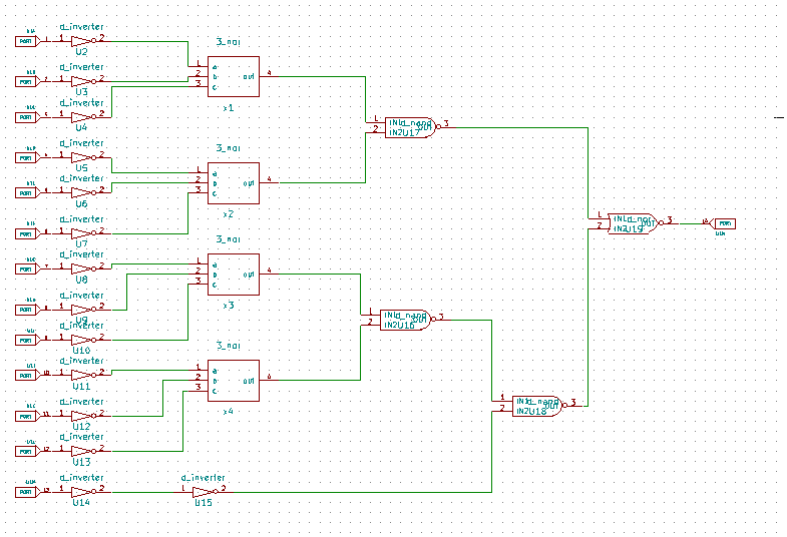


Figure 3.22: Subcircuit of SN54ALS133

3.5.4 Test Circuit

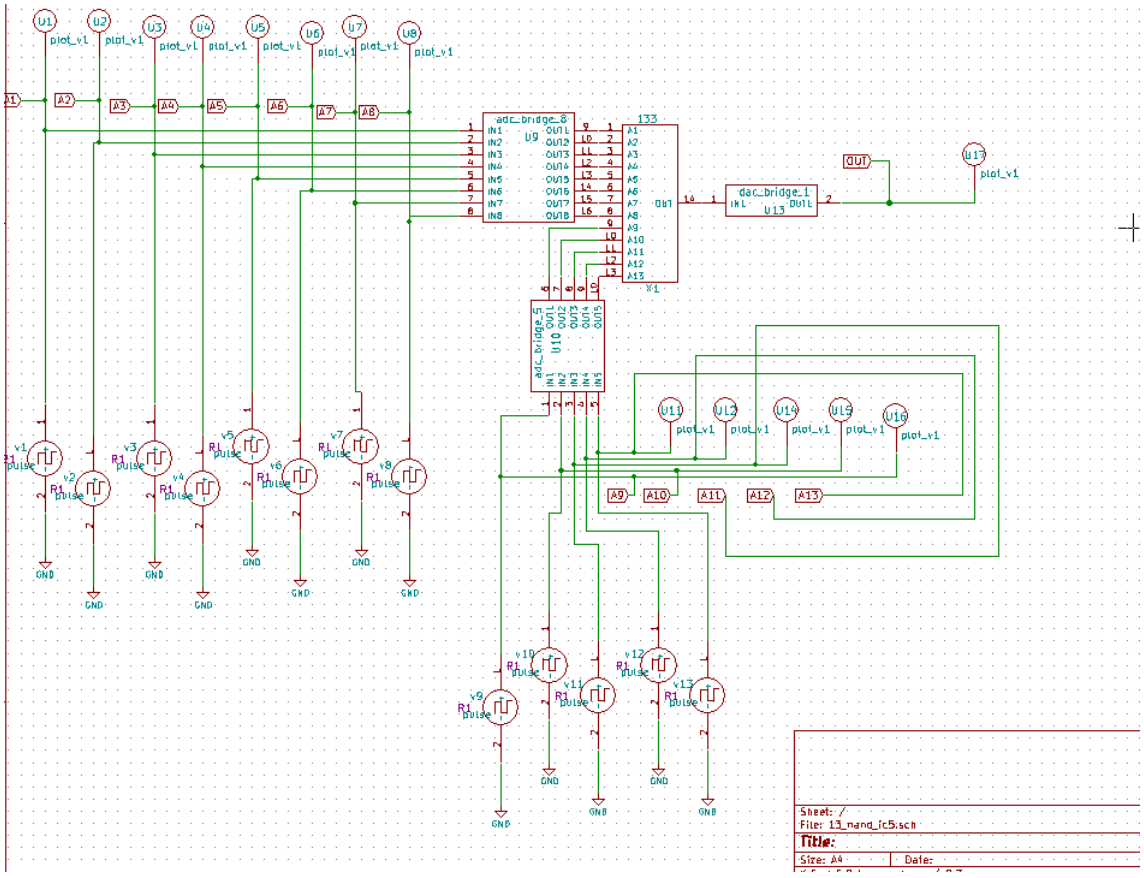


Figure 3.23: Test Circuit of SN54ALS133

3.5.5 NgSpice Plot

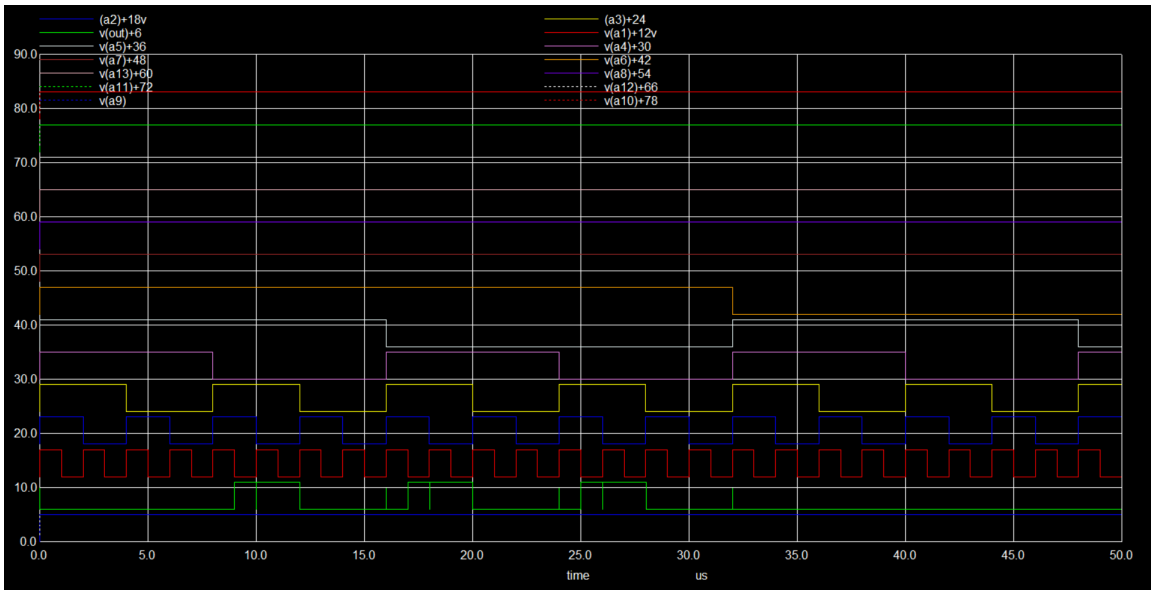


Figure 3.24: Simulation Diagram of SN54ALS133

3.6 SN54LS90

3.6.1 Description

The SN54LS90 is a 4-bit binary decade counter. It is a divide-by-10 counter, also known as a BCD (Binary-Coded Decimal) counter. Internally, it consists of four flip-flops and associated logic to produce a modulo-10 counting sequence.

It can also be configured as a modulo-6 or modulo-5 counter, making it flexible for timing and counting applications.

Features of SN54LS90

- 4-bit binary decade counter (MOD-10)
- TTL-compatible logic levels
- Low power consumption due to Schottky clamping
- Divide-by-2 and divide-by-5 sections can be cascaded
- Asynchronous master reset and set inputs
- Can be configured as divide-by-2, divide-by-5, or divide-by-10
- Applications : Digital clocks (for counting seconds, minutes, etc.),Frequency dividers,Event counters,Digital timers,Sequential timing applications

3.6.2 Pin Diagram

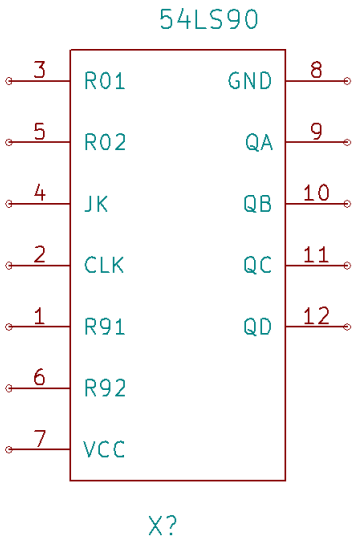


Figure 3.25: Pin Diagram of SN54LS90

3.6.3 Subcircuit Diagram

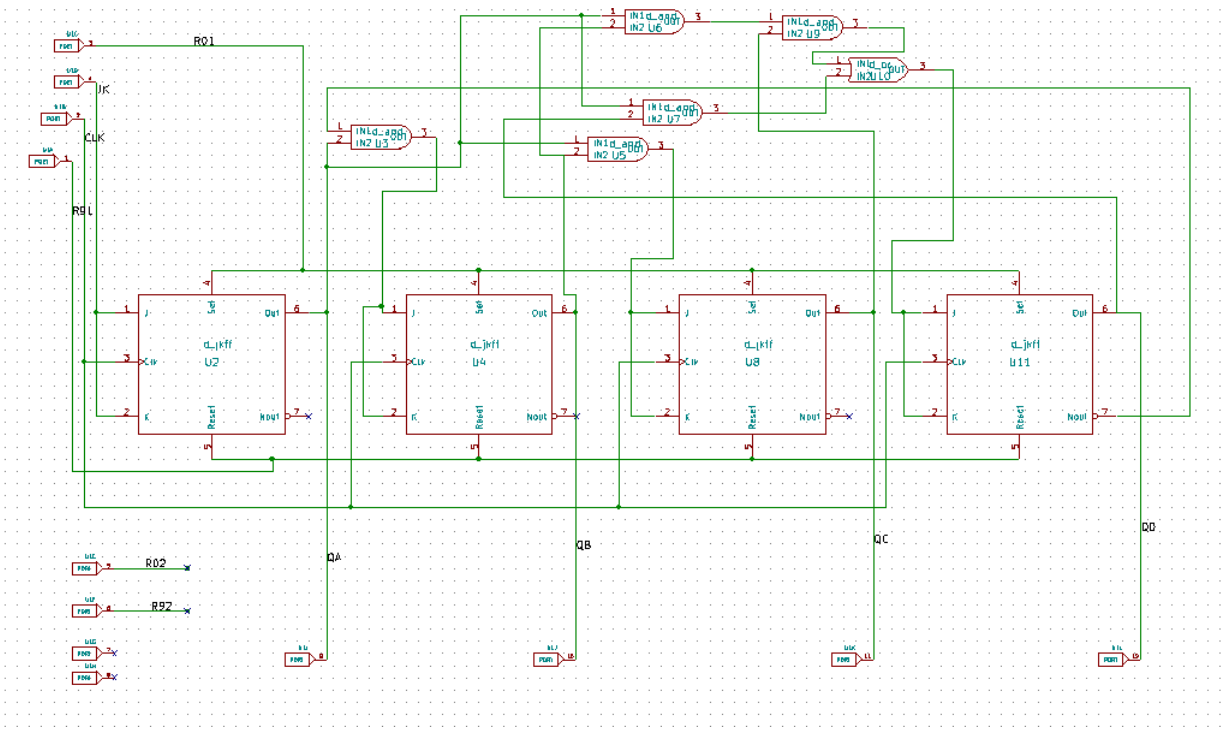


Figure 3.26: Subcircuit of SN54LS90

3.6.4 Test Circuit

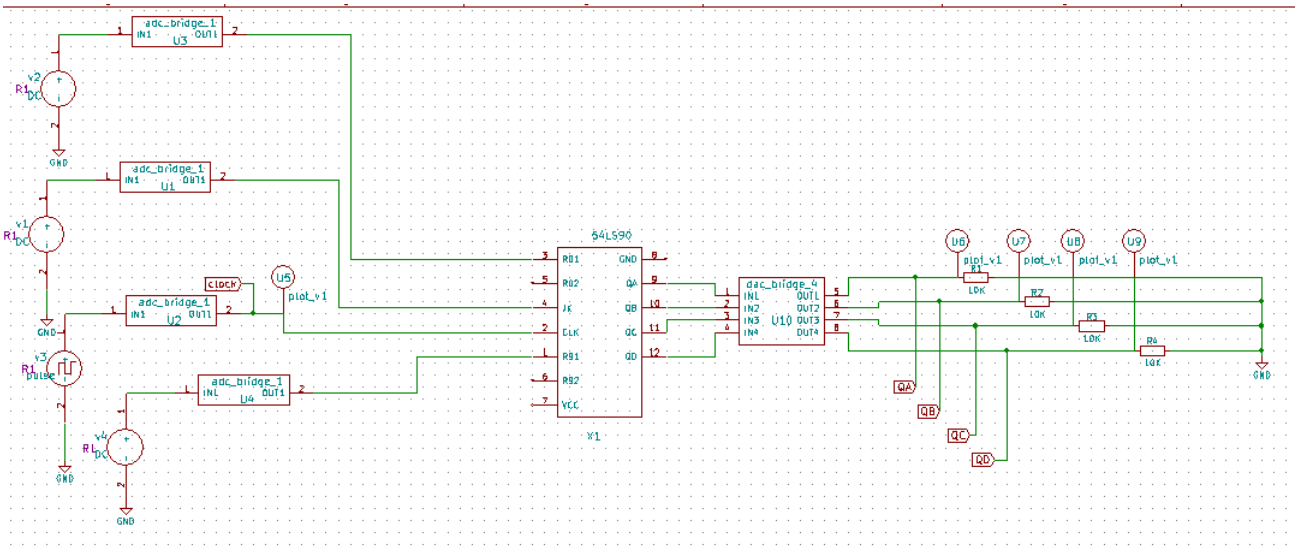


Figure 3.27: Test Circuit of SN54LS90

3.6.5 NgSpice Plot

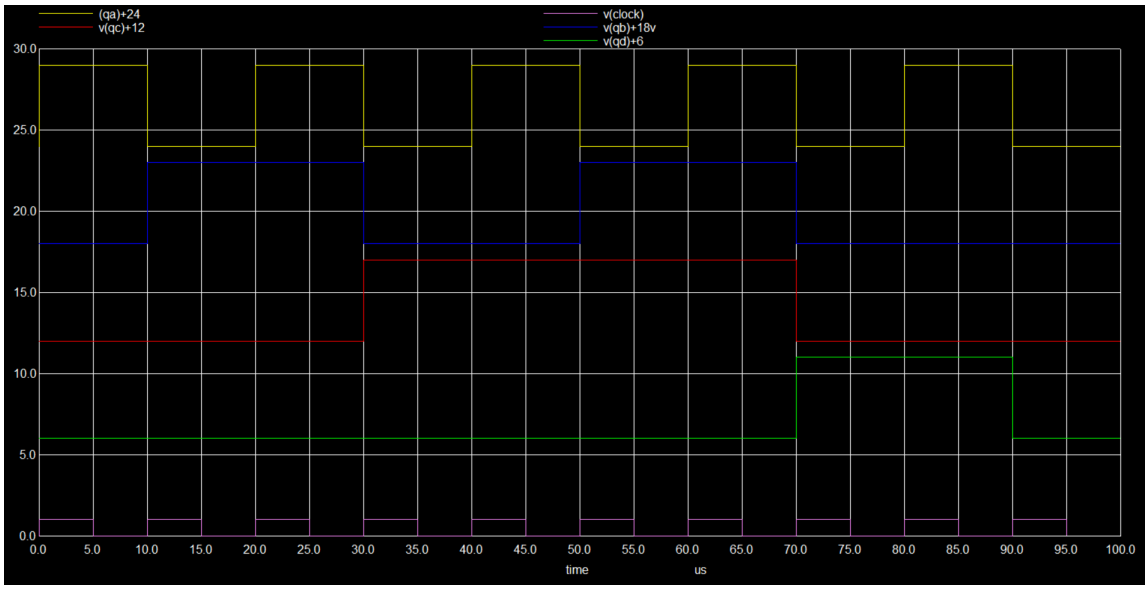


Figure 3.28: Simulation Diagram of SN54LS90

3.7 SN54LS72

3.7.1 Description

The SN54LS72 is a dual positive-edge-triggered J-K Master-Slave flip-flop with asynchronous clear, part of the LS (Low Power Schottky) TTL logic family. Each flip-flop consists of a master-slave configuration, meaning:

- The master latch is enabled during the LOW phase of the clock.
- The slave latch is enabled during the HIGH phase of the clock.

The result is positive-edge triggering—the flip-flop changes state on the rising edge of the clock signal.

Each flip-flop features independent J, K, Clock (clk), and Clear (clr) inputs and Q/$\overline{Q}$ outputs. The Clear input asynchronously forces the output LOW, regardless of other inputs or clock state.

Features of SN54LS72

- Dual J-K Master-Slave flip-flops with asynchronous clear
- Positive-edge triggered
- Operates as toggle flip-flop when J = K = HIGH
- TTL compatible inputs/outputs
- Low power consumption due to Schottky technology
- High speed operation
- Complementary outputs (Q and $\overline{Q}$)
- Applications : Binary counters, Frequency division (toggle mode), Data storage elements, Sequential logic circuits, Clocked control applications, State machines, Debouncing logic for switches.etc.,

3.7.2 Pin Diagram

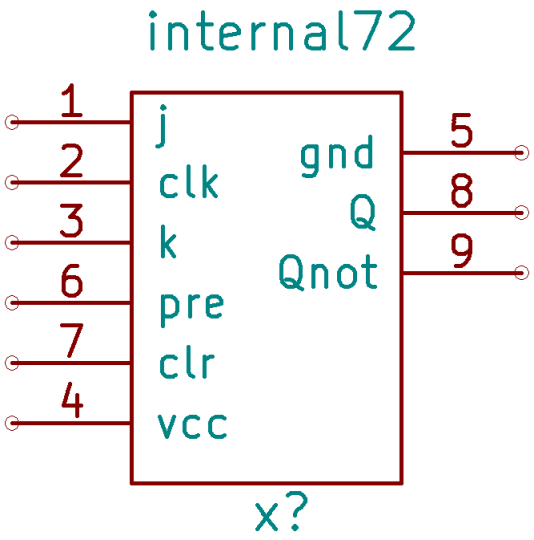


Figure 3.29: Pin Diagram of SN54LS72

3.7.3 Subcircuit Diagram

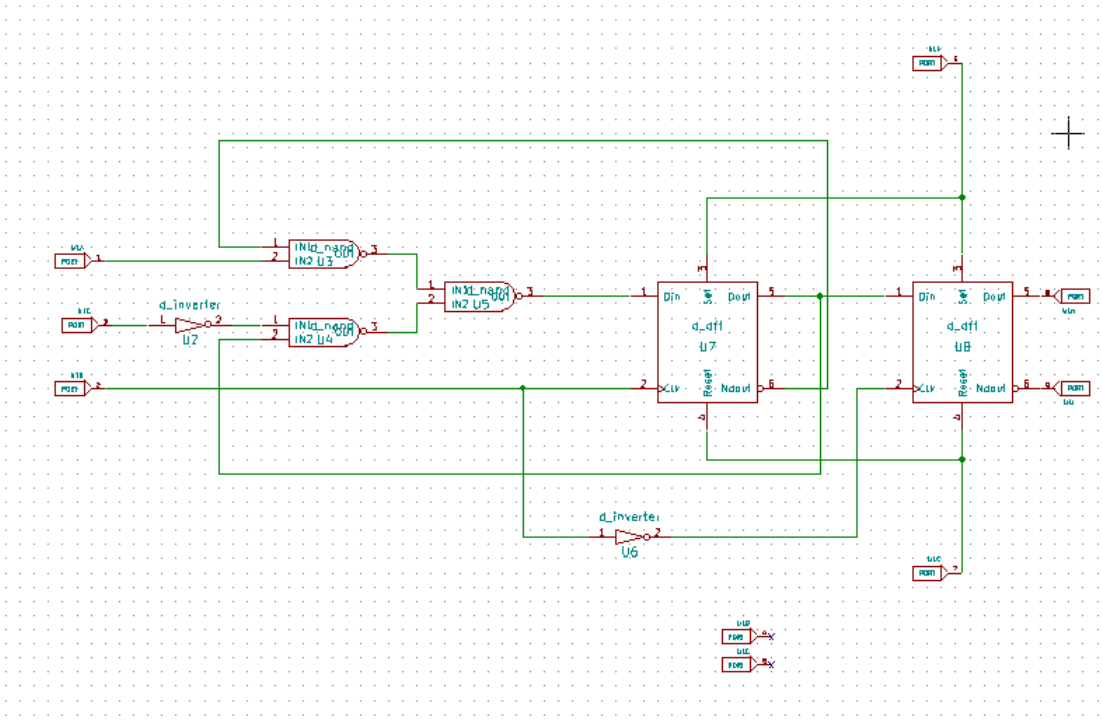


Figure 3.30: Subcircuit of SN54LS72

3.7.4 Test Circuit

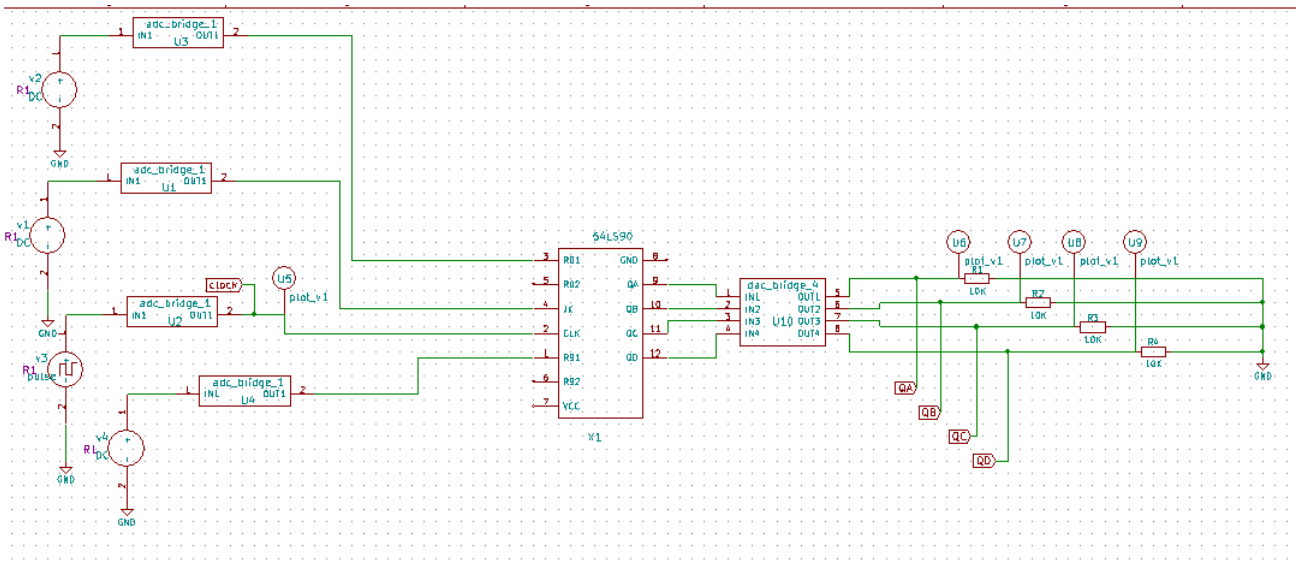


Figure 3.31: Test Circuit of SN54LS72

3.7.5 NgSpice Plot

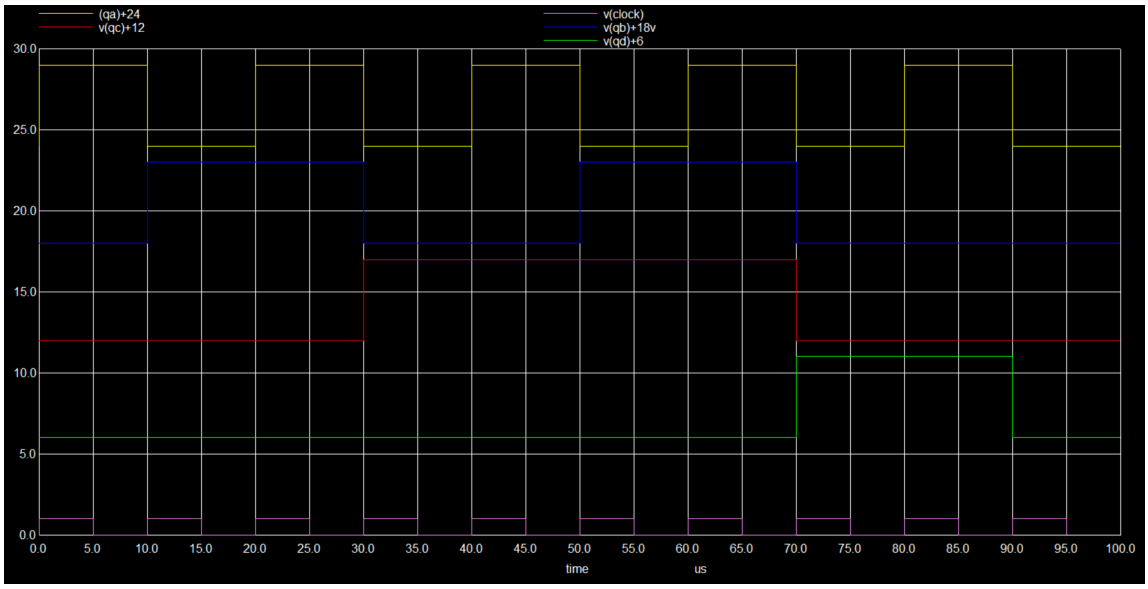


Figure 3.32: Simulation Diagram of SN54LS72

3.8 54ACT11030

3.8.1 Description

An 8-input NAND gate is a single logic gate with 8 inputs and 1 output. It performs the NAND function:

Output = NOT (A · B · C · D · E · F · G · H)

While standard ICs like the 7400 series commonly contain 2-input or 4-input NAND gates, 8-input NAND gates are relatively rare and typically found in higher-end or custom logic families like 74HC30, CD4068, or implemented using multiple gates.

Features of 54ACT11030

- Performs NAND operation with 8 inputs.
- Available in TTL (e.g., 74HC30) or CMOS (e.g., CD4068) logic families.
- High noise immunity.
- Low power consumption (especially in CMOS versions).
- Fast switching time (in high-speed versions).
- Operates over wide voltage ranges (e.g., 3V to 15V for CMOS).
- Combination Logic Design – Simplifies multiple input logic checks.
- Microcontroller Interfacing – Combines multiple sensor outputs into one logical signal.

3.8.2 Pin Diagram

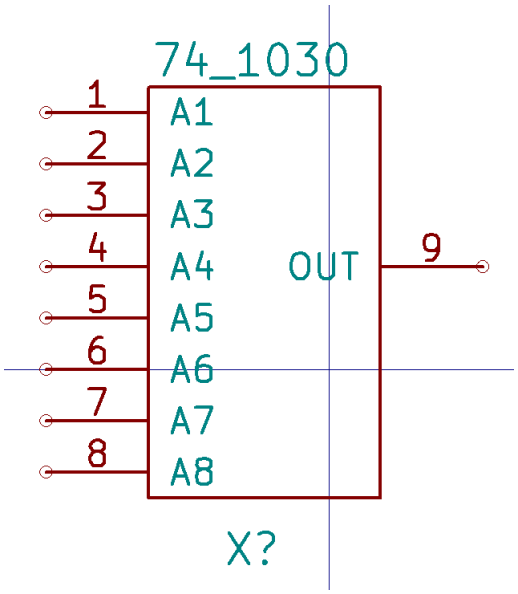


Figure 3.33: Pin Diagram of 54ACT11030

3.8.3 Subcircuit Diagram

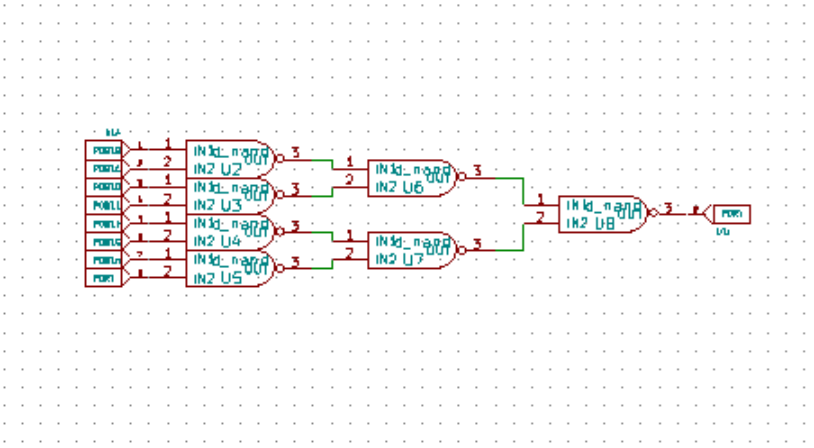


Figure 3.34: Subcircuit of 54ACT11030

3.8.4 Test Circuit

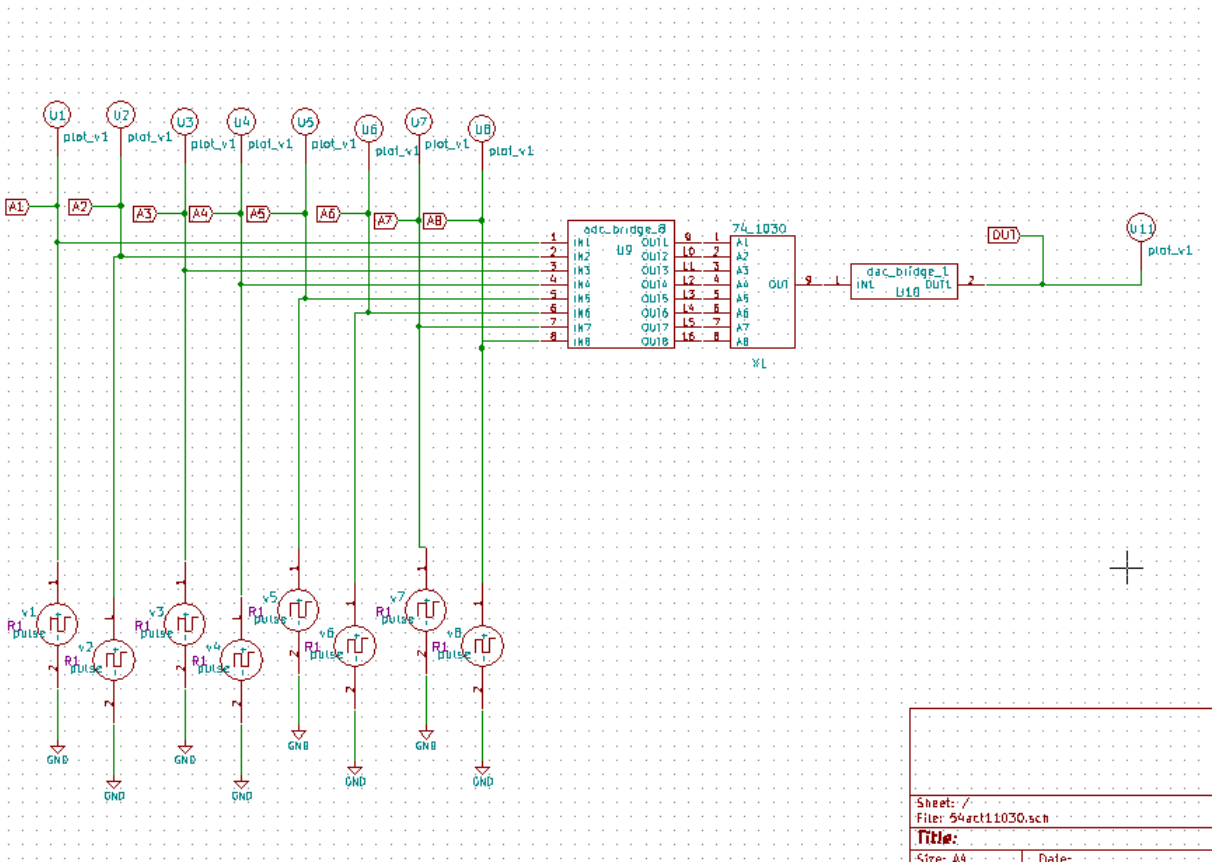


Figure 3.35: Test Circuit of 54ACT11030

3.8.5 NgSpice Plot

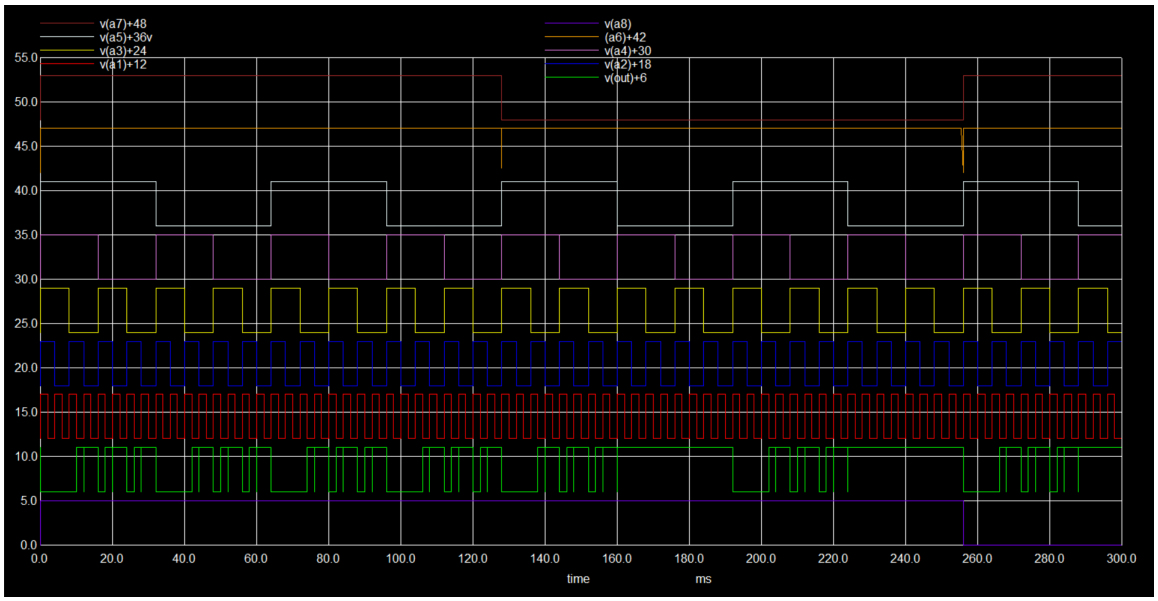


Figure 3.36: Simulation Diagram of 54ACT11030

Chapter 4

Conclusion and Future Scope

This project successfully demonstrates the comprehensive design and simulation of a integrated circuits utilizing the eSim platform. The process encompassed schematic development, component interconnection, and rigorous simulation, culminating in the validation of the circuit's intended functionality. Through this endeavor, a deeper understanding of digital circuit principles and practical experience with an open-source EDA tool were achieved. The project not only reinforces foundational concepts in design but also highlights the significance of accessible simulation environments in fostering innovation and skill development in electronic design automation.

This project highlights the growing importance of open-source EDA tools like eSim, which can be further developed to support more complex designs and automated verification processes, thereby contributing significantly to both educational and industrial domains.

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