eSim Semester Long Internship Report

on

Analog and Digital Circuit Design in eSim

Submitted by

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Acknowledgement

I would like to express my gratitude to the eSim team of IITBombay for giving me an opportunity to work as an Intern as a part of the Semester long Internship. This has given me a platform to understand and analyse the working of Integrated Circuits designed in eSim.

I would to extend my heartfelt appreciation and thank Mr. Sumanto Kar for guiding me throughout the internship. Their guidance and support throughout the internship have been instrumental in my growth.

The internship has provided me an opportunity to interact with my fellow interns from different colleges and I would like to thank them for their support. This friendly working environment has fostered collaboration.

I will utilize the knowledge and skills that I have gained from this internship in my future professional journey.

CONTENTS

1. Introduction

1.1 eSim

eSim is a free/libre and open-source Electronic Design Automation (EDA) tool developed by FOSSEE (Free and Open-Source Software for Education) at IIT Bombay. It provides a comprehensive

platform for circuit design, simulation, analysis, and PCB (Printed Circuit Board) design.

eSim is built using various free/libre and open-source software components, including:

1. KiCad: A popular EDA suite that offers schematic capture and PCB layout tools.

2. Ngspice: A mixed-level/mixed-signal circuit simulator that can perform analog, digital, and mixed-signal simulations.

3. NGHDL: An open source VHDL simulator that enables simulation and analysis of digital circuits.

4. GHDL: Another open source VHDL simulator that supports the IEEE 1076 VHDL standard.

2. Design of ICs in eSim

The integrated circuits are digital, analog, or mixed signal circuits implemented using basic blocks of circuits such as logic gates like AND, OR, NOT, NAND, NOR for digital integrated circuits and transistors, MOSFETs, opamps for analog integrated circuits. eSim has a library of these basic gates and other components which can be used to design complex Integrated Circuits (ICs) and executed in KiCad and NGSpice to analyze the behaviour and working of the circuits. These circuits are finally converted to subcircuit and provided to the library which can be further implemented to build more complex circuits.

The process which is followed to obtain the subcircuit is:

1. Initially, we design the basic internal circuit diagram of the IC. The ICs have certain ports through which the inputs are provided and outputs are obtained. These ports are assigned to the specified wires in the internal circuit diagram.
2. This circuit is now annotated, ERC checked and spice file is obtained.
3. Coming back to the main page of eSim software, we now convert it from KiCad to NGSpice which creates a netlist.
4. In the schematic sheet, choose the open library editor option. Then select the current library as subcircuitlibrary and press on add component. Now provide and name for the subcircuit.
5. Provide a shape and change the orientation of the field value and name as you desire. Then save the subcircuit and click ok to modify the subcircuit library.
6. The subcircuit is ready. Finally implement these subcircuits using a test circuit providing the necessary inputs and observe the obtained results.

3. LTC6603: LTC6603 is a 9th Order Dual channel Butterworth Low Pass Filter for cut off frequency of 2.2kHz

3.1 CIRCUIT DIAGRAM: The internal circuit of the IC is given below.

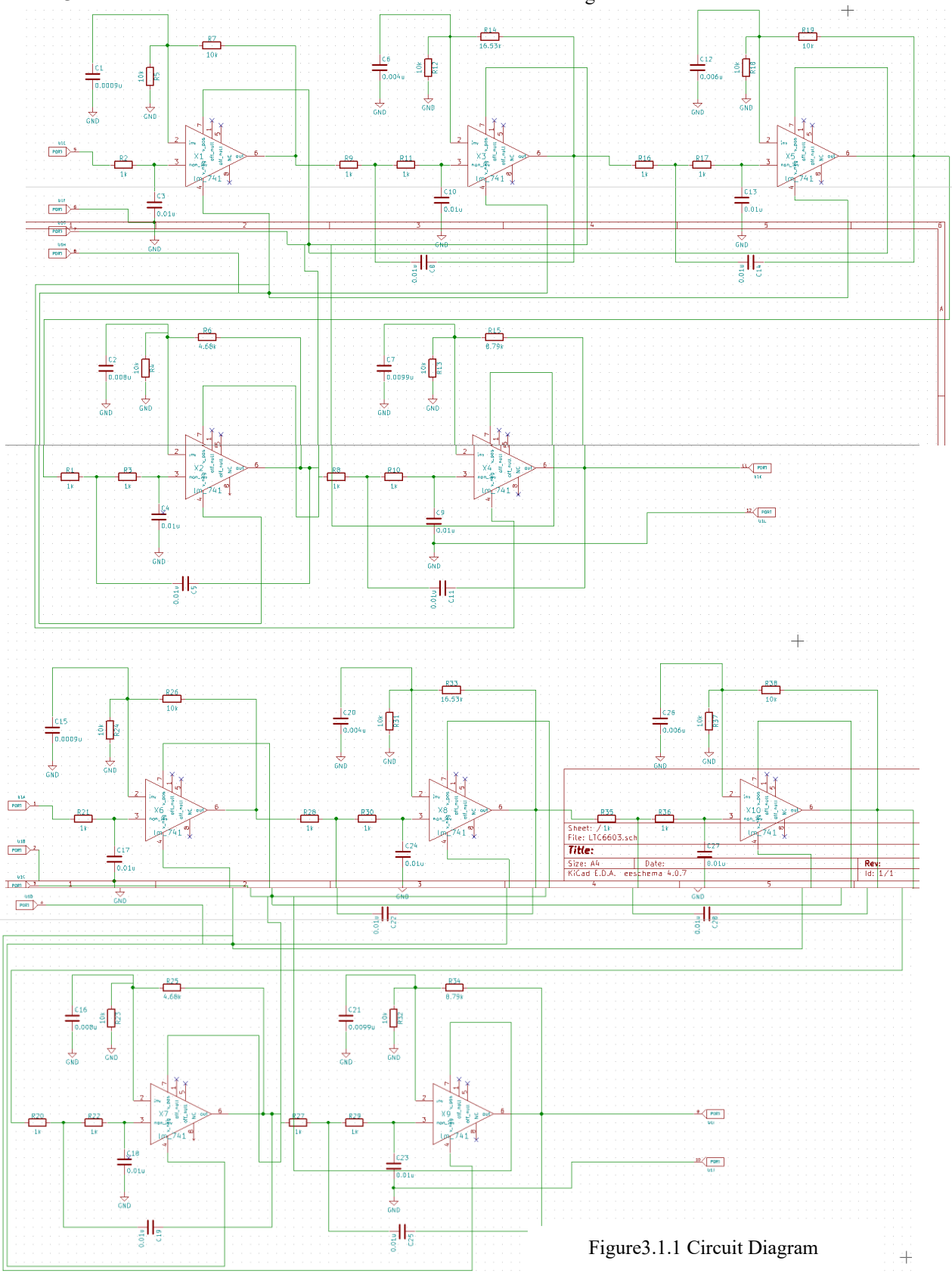

Figure3.1.1 Circuit Diagram

3.2 TEST CIRCUIT USING SUBCIRCUIT: A test circuit is implemented using the subcircuit of IC

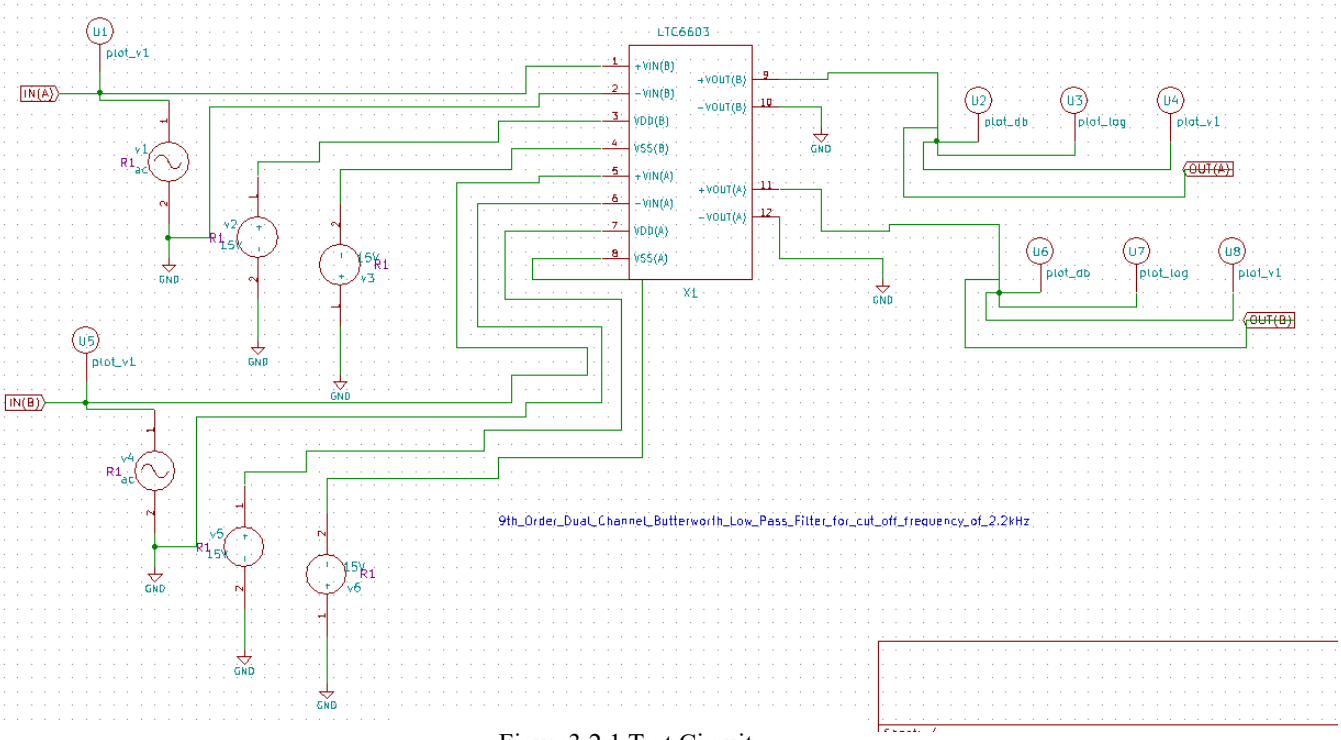

Figure3.2.1 Test Circuit

3.3 INPUT WAVEFORM OF CHANNEL A & B: AC input waveform

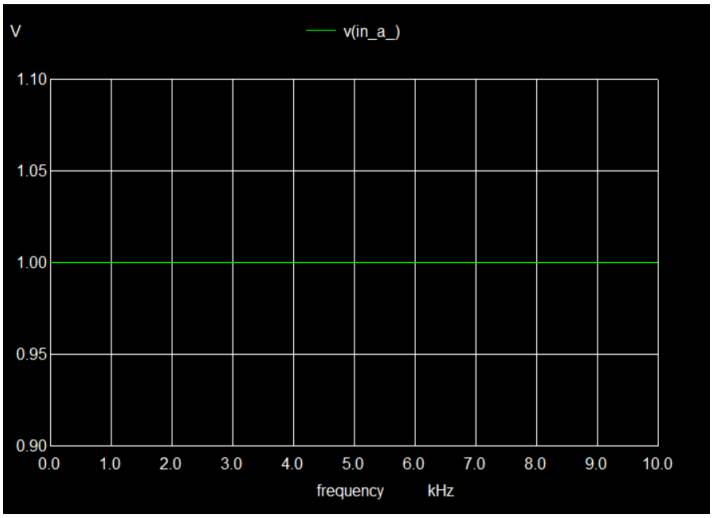

Figure3.3.1 Input waveform

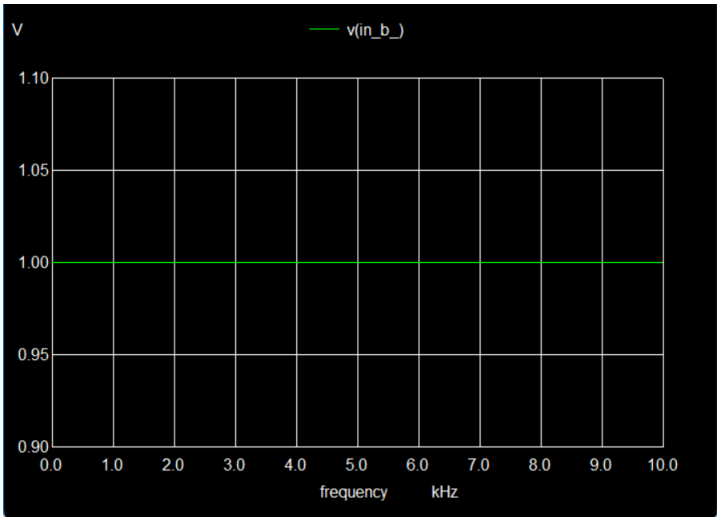

Figure3.3.2 Input waveform

3.4 OUTPUT WAVEFORM OF CHANNEL A & B: Compare the output waveforms with the values given in Analysis table below.

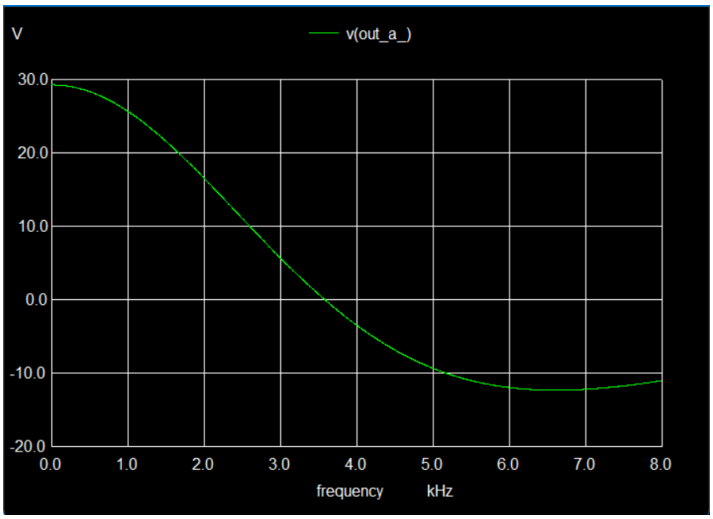

Figure3.4.1 Vout waveform

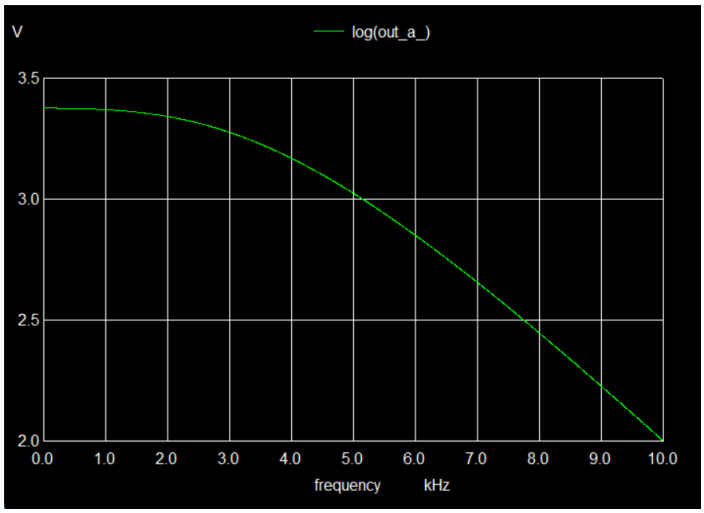

Figure3.4.2 log(out) waveform

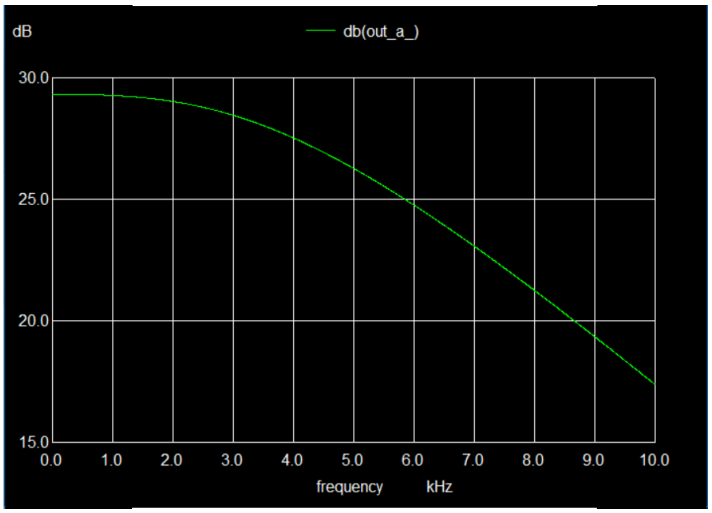

Figure3.4.3 dB(out) waveform

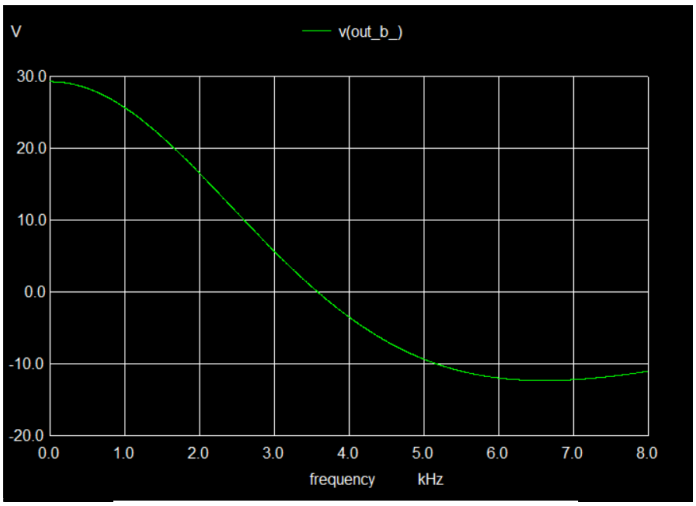

Figure3.4.4 Vout waveform

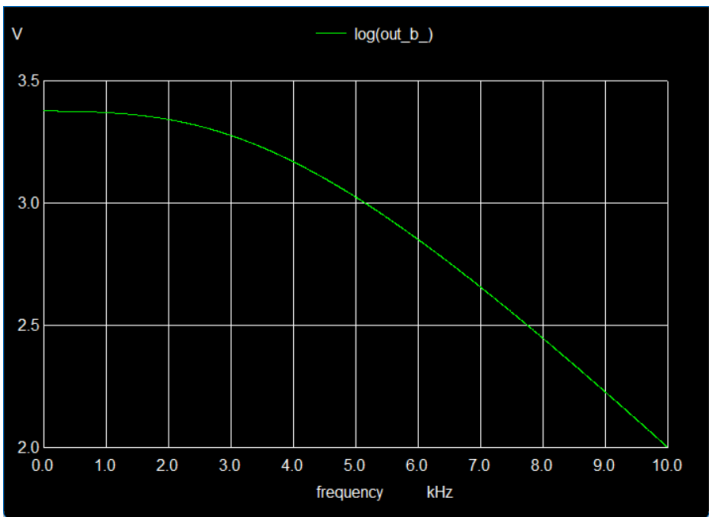

Figure3.4.5 log(out) waveform

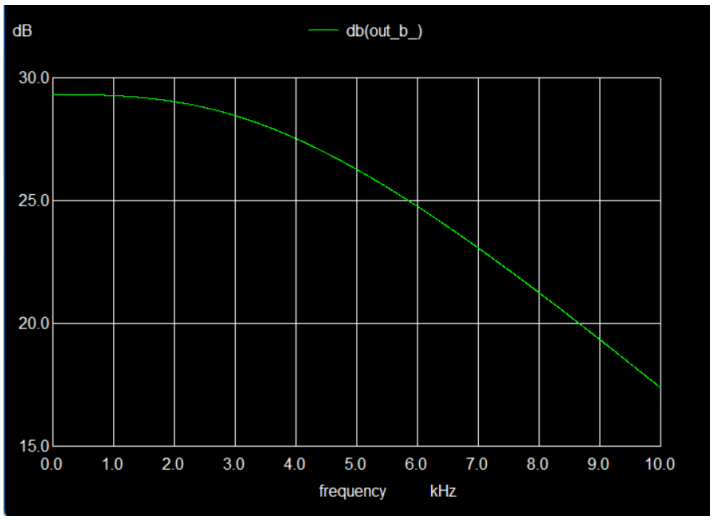

Figure3.4.6 dB(out) waveform

ANALYSIS:

Order	Gain at Stage 1 (at the end of OP-AMP 1)	Gain at Stage 2 (at the end of OP-AMP 2)	Gain at Stage 3 (at the end of OP-AMP 3)	Gain at Stage 4 (at the end of OP-AMP 4)	Gain at Stage 5 (at the end of OP-AMP 5)	Total Gain (at the end of all stages)	Minimum Offset of LM741 OP-AMP	Output voltage (Vout) in V if Vin is 1V	Output voltage (Vout) in dB if Vin is 1V	Output voltage (Vout) in log(out) if Vin is 1V
9	2	2.653	2	1.468	1.879	29.2718	0.5	15.6359	29.3289	3.3766

4. LTC1565-31: LTC156531 is a 7th Order Butterworth Low Pass Filter for cut off frequency of 6kHz

4.1 CIRCUIT DIAGRAM: The internal circuit of the IC is given below.

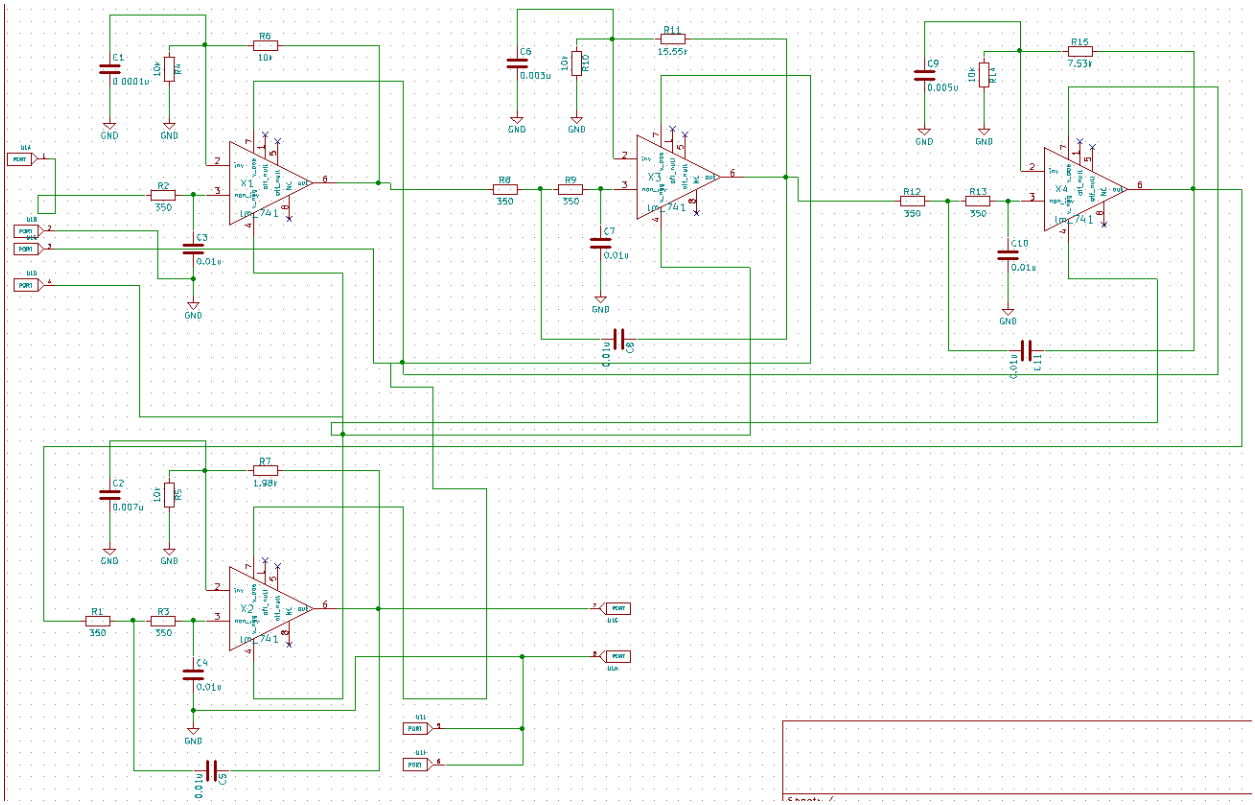

Figure4.1.1 Circuit Diagram

4.2 TEST CIRCUIT USING SUBCIRCUIT: A test circuit is implemented using the subcircuit of IC

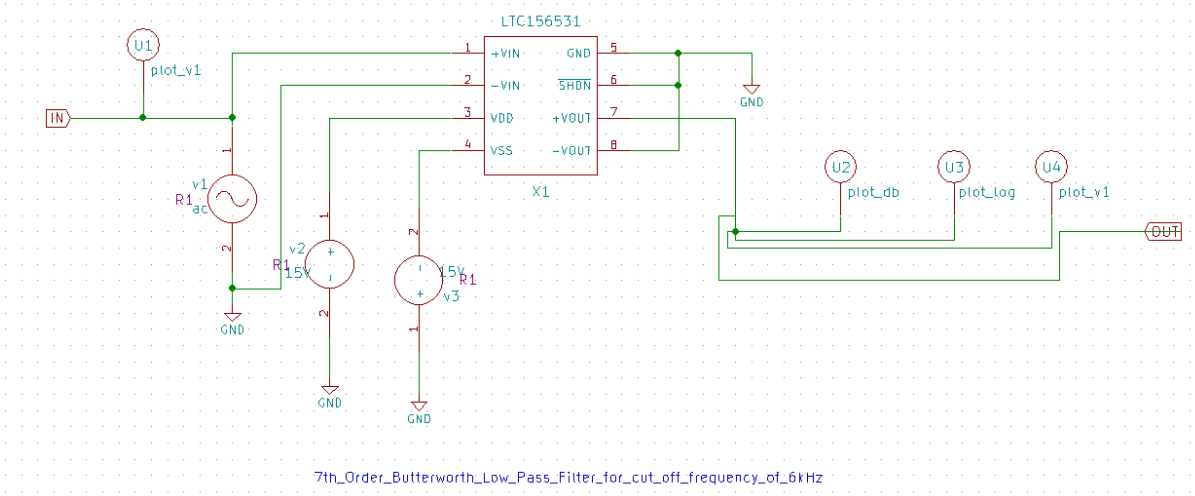

Figure4.2.1 Test Circuit

4.3 INPUT WAVEFORM: AC input waveform

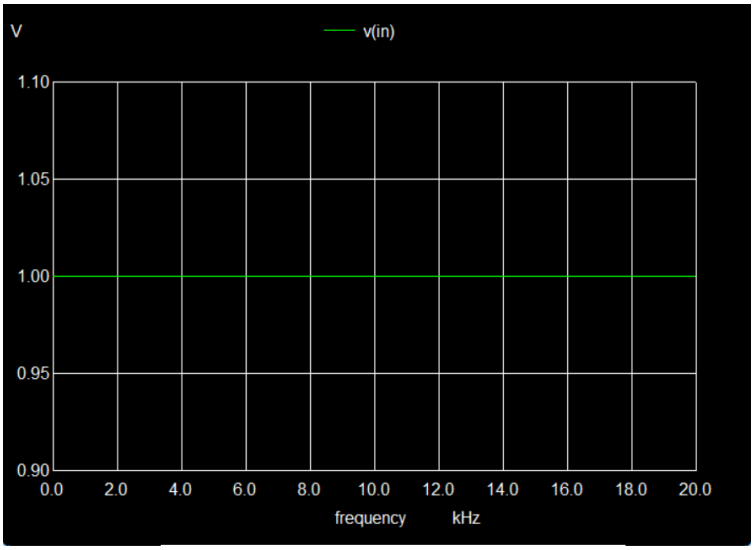

Figure4.3.1 Input waveform

4.4 OUTPUT WAVEFORM: Compare the output waveforms with the values given in Analysis table below.

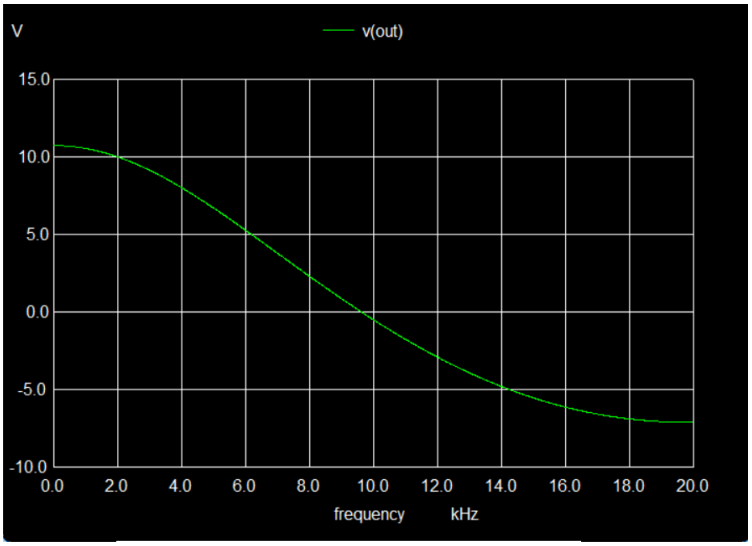

Figure4.4.1 Vout waveform

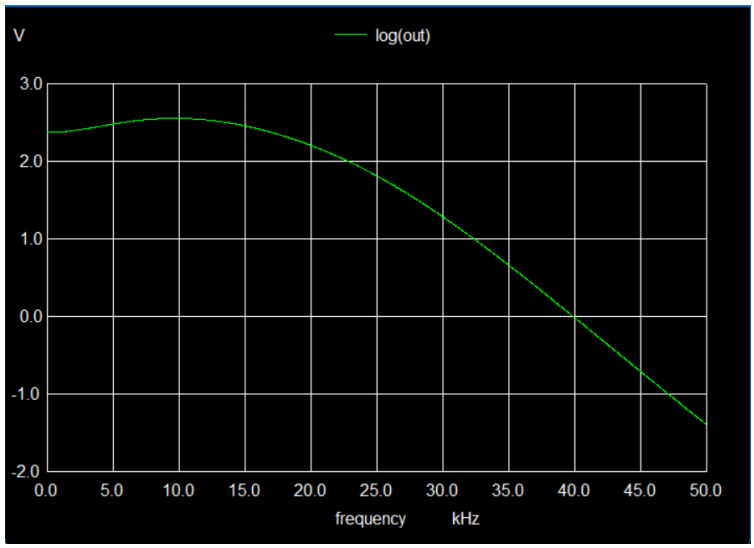

Figure4.4.2 log(out) waveform

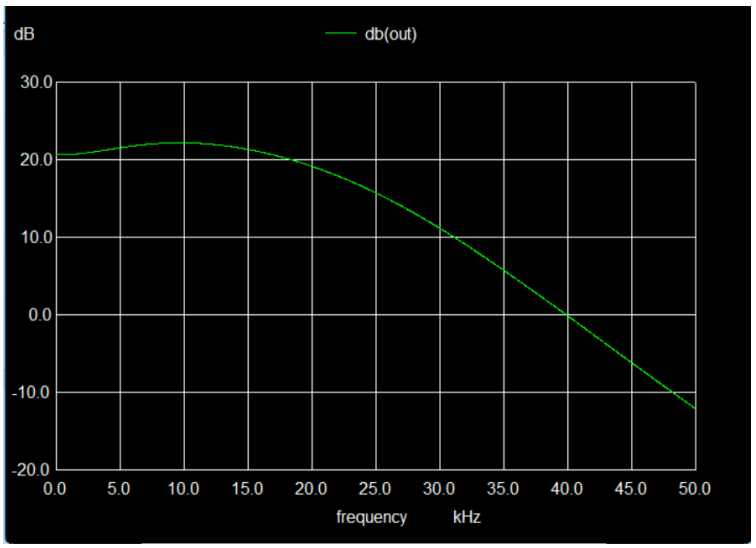

Figure4.4.3 dB(out) waveform

4.5 ANALYSIS:

Order	Gain at Stage 1 (at the end of OP-AMP 1)	Gain at Stage 2 (at the end of OP-AMP 2)	Gain at Stage 3 (at the end of OP-AMP 3)	Gain at Stage 4 (at the end of OP-AMP 4)	Gain at Stage 5 (at the end of OP-AMP 5)	Total Gain (at the end of all stages)	Minimum Offset of LM741 OP-AMP	Output voltage (Vout) in V if Vin is 1V	Output voltage (Vout) in dB if Vin is 1V	Output voltage (Vout) in log(out) if Vin is 1V
7	2	2.555	1.753	1.198	-	10.7314	0.5	5.3657	20.6131	2.3731

5. MAX7414: MAX7414 is 5th Order Switched-Capacitor Butterworth Low Pass Filter for cut off frequency of 2.5kHz & Vin of 2V

5.1 CIRCUIT DIAGRAM: The internal circuit of the IC is given below.

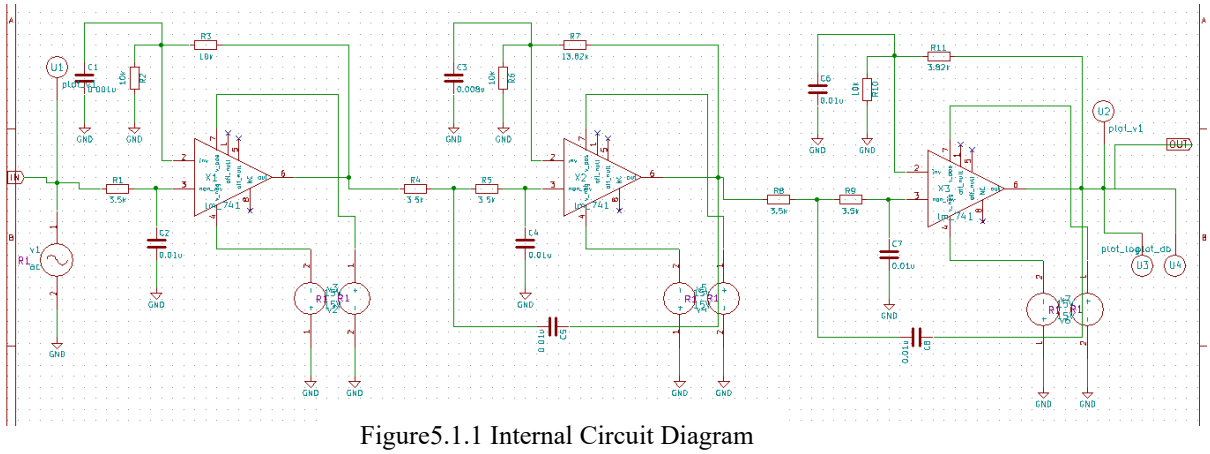

Figure5.1.1 Internal Circuit Diagram

To implement switched capacitor Butterworth Low Pass Filter, replacement of resistors at input terminal with MOSFETs,

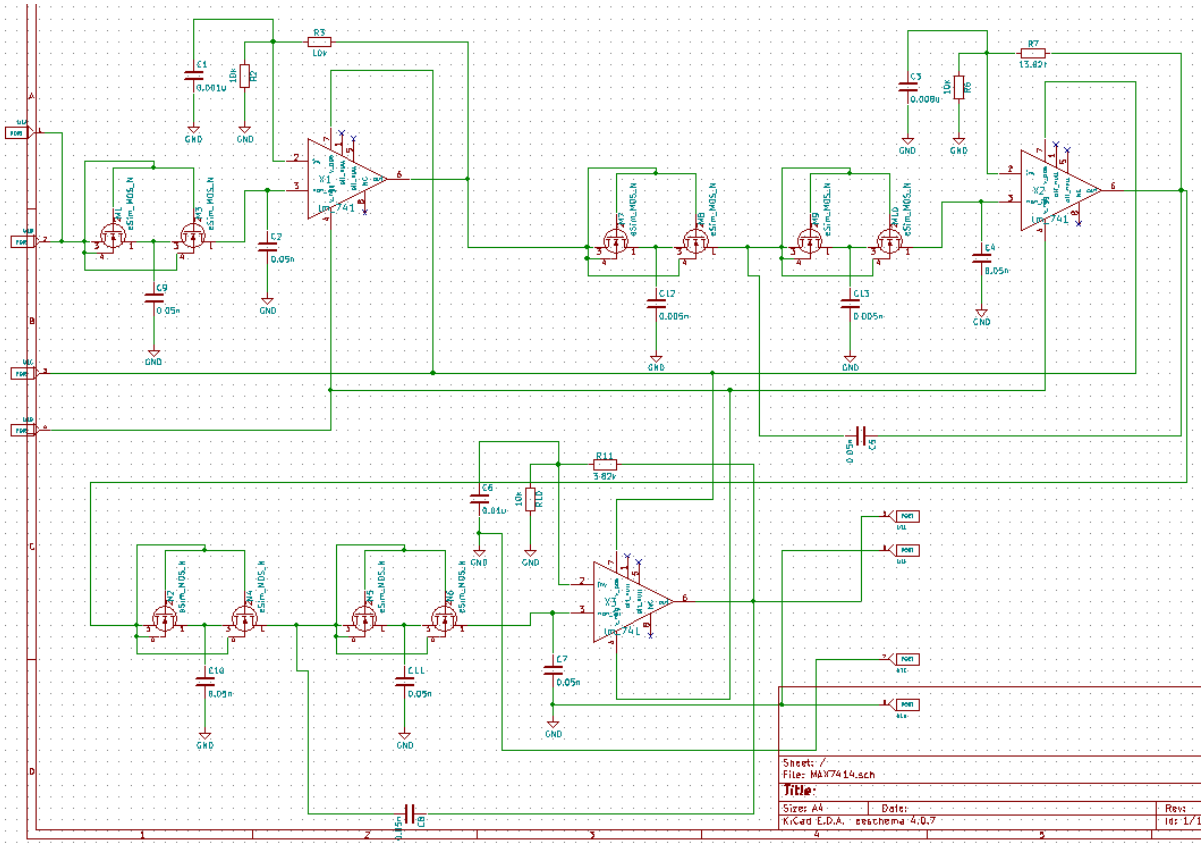

Figure5.1.2 Circuit Diagram

5.2 TEST CIRCUIT USING SUBCIRCUIT: A test circuit is implemented using the subcircuit of IC

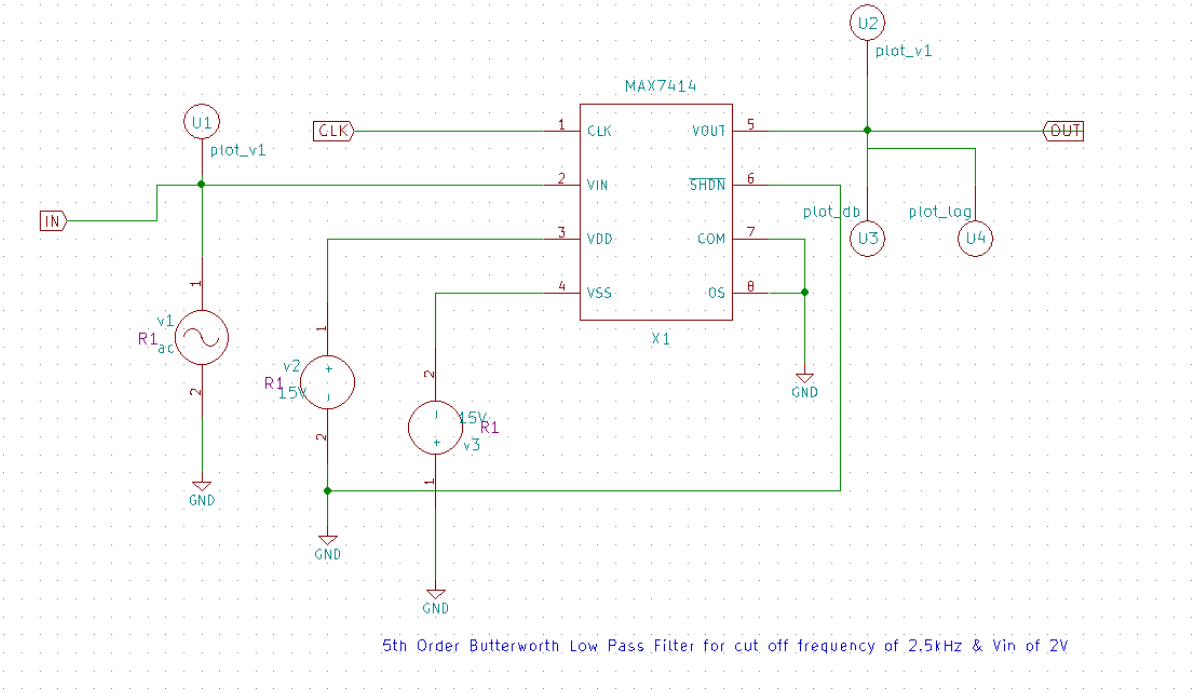

Figure5.2.1 Test Circuit

5.3 INPUT WAVEFORM: AC input waveform

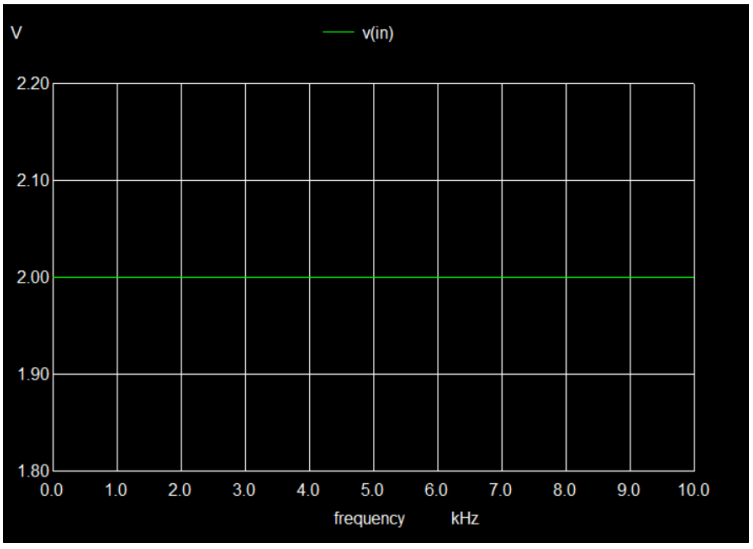

Figure5.3.1 Input waveform

5.4OUTPUT WAVEFORM: Compare the output waveforms with the values given in Analysis table below.

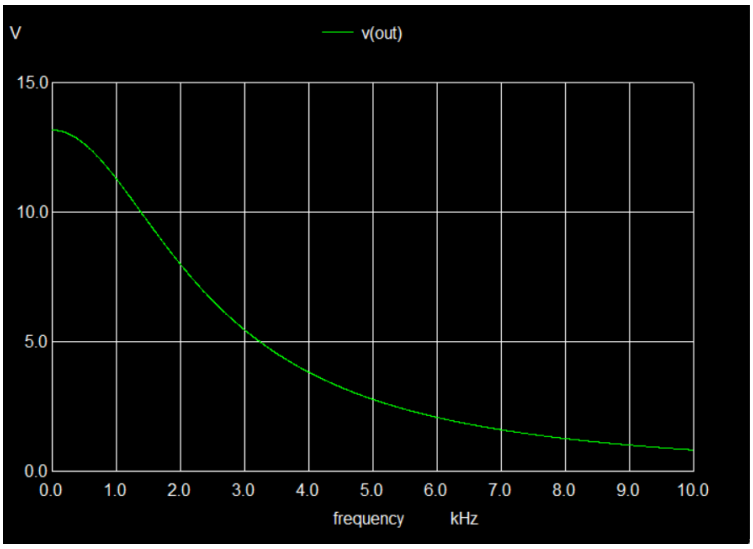

Figure5.4.1 Vout waveform

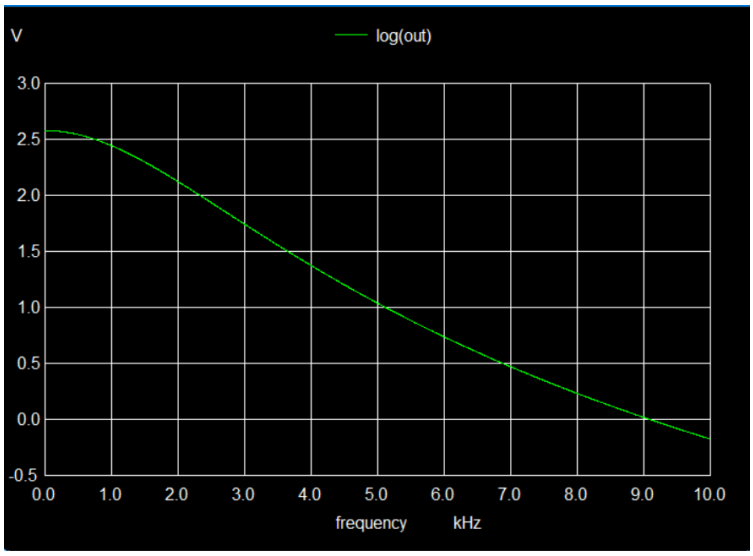

Figure5.4.2 log(out) waveform

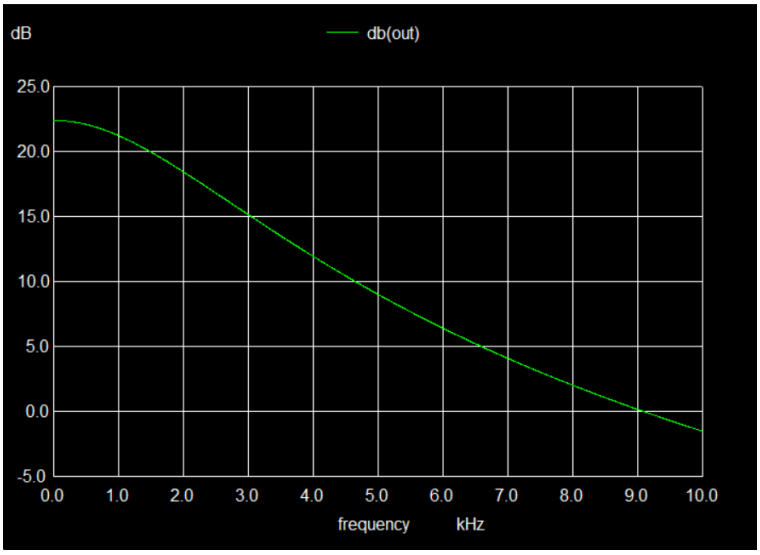

Figure5.4.3 dB(out) waveform

5.5 ANALYSIS:

Order	Gain at Stage 1 (at the end of OP-AMP 1)	Gain at Stage 2 (at the end of OP-AMP 2)	Gain at Stage 3 (at the end of OP-AMP 3)	Gain at Stage 4 (at the end of OP-AMP 4)	Gain at Stage 5 (at the end of OP-AMP 5)	Total Gain (at the end of all stages)	Minimum Offset of LM741 OP-AMP	Output voltage (Vout) in V if Vin is 2V	Output voltage (Vout) in dB if Vin is 2V	Output voltage (Vout) in log(out) if Vin is 2V
5	2	2.2382	1.382	-	-	6.58385	0.5	6.5838	22.39013	2.5778

6. MAX7410: MAX7410 is a 5th Order Switched-Capacitor Butterworth Low Pass Filter for cut off frequency of 2.5kHz & Vin of 4V

6.1 CIRCUIT DIAGRAM: The internal circuit of the IC is given below.

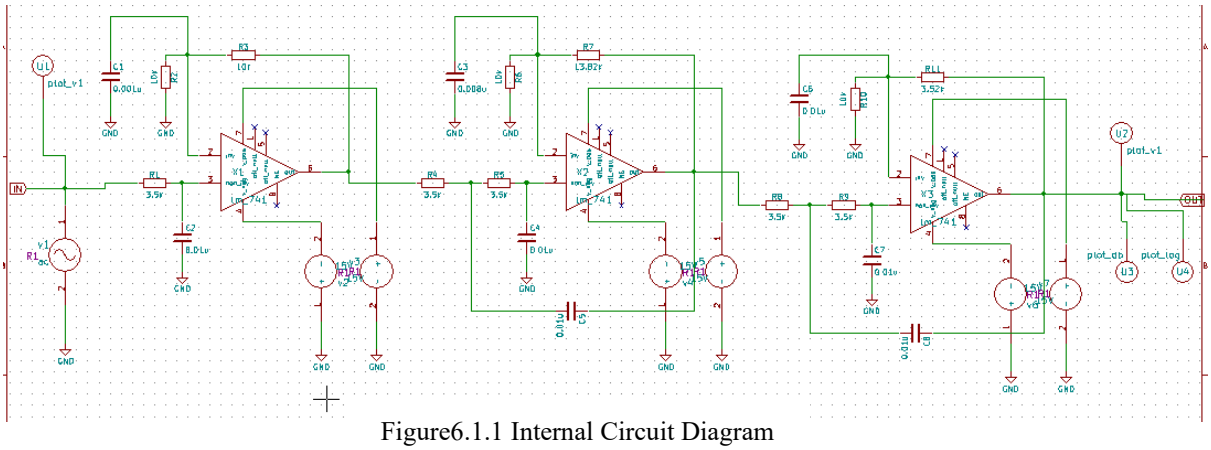

Figure6.1.1 Internal Circuit Diagram

To implement switched capacitor Butterworth Low Pass Filter, replacement of resistors at input terminal with MOSFETs,

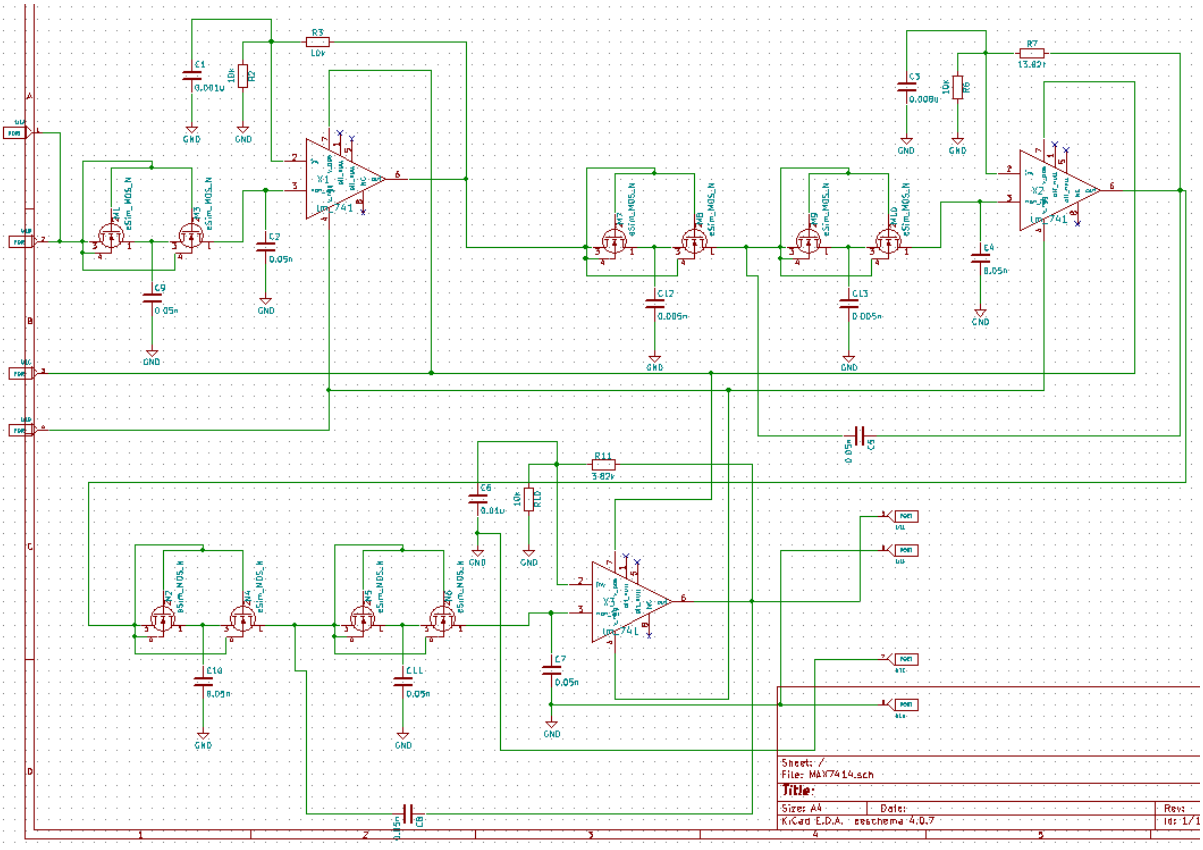

Figure6.1.2 Circuit Diagram

6.2 TEST CIRCUIT USING SUBCIRCUIT: A test circuit is implemented using the subcircuit of IC

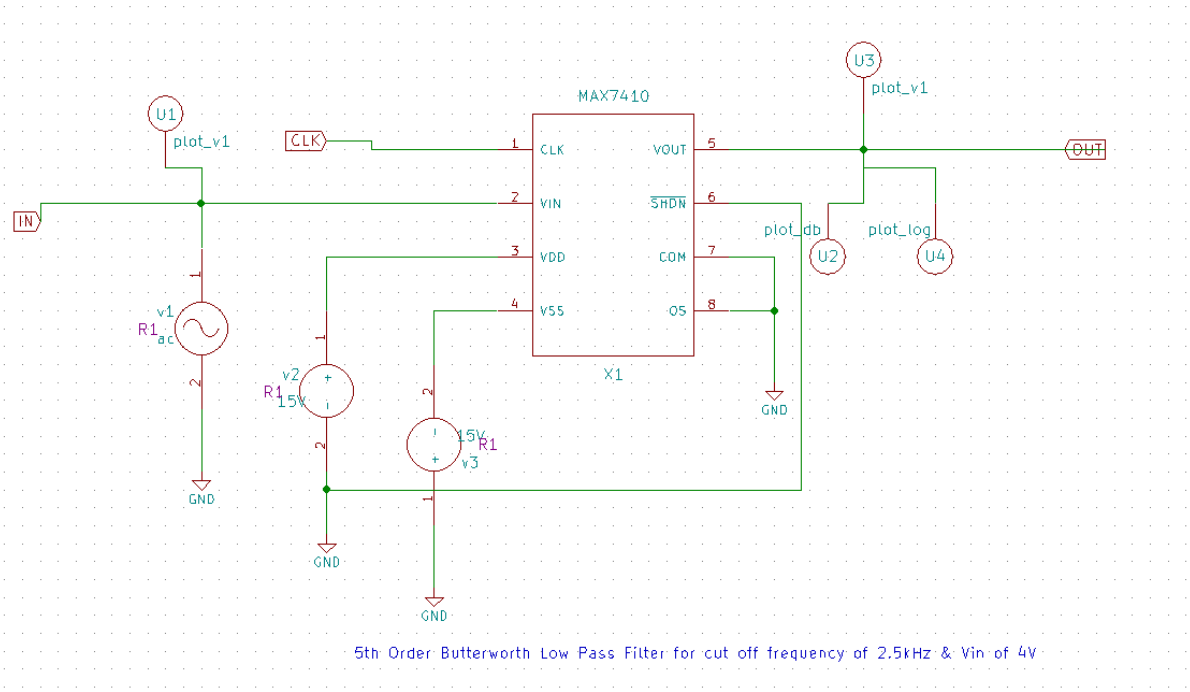

Figure6.2.1 Test Circuit

6.3 INPUT WAVEFORM: AC input waveform

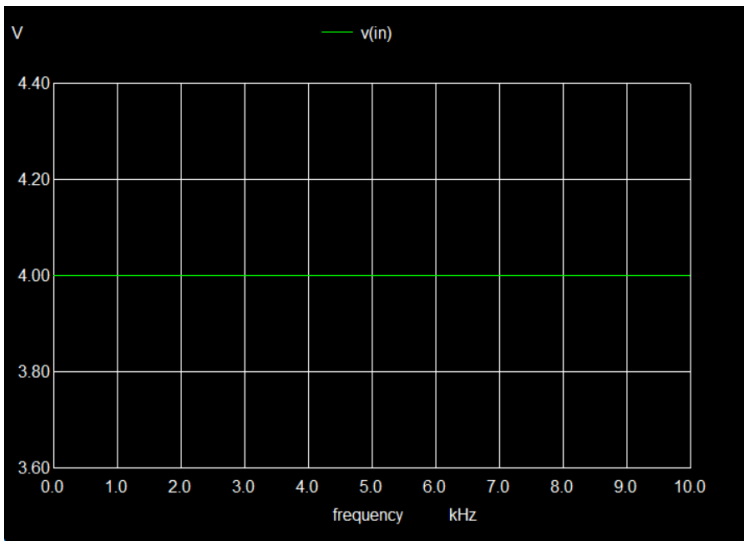

Figure6.3.1 Input waveform

6.4 OUTPUT WAVEFORM: Compare the output waveforms with the values given in Analysis table below.

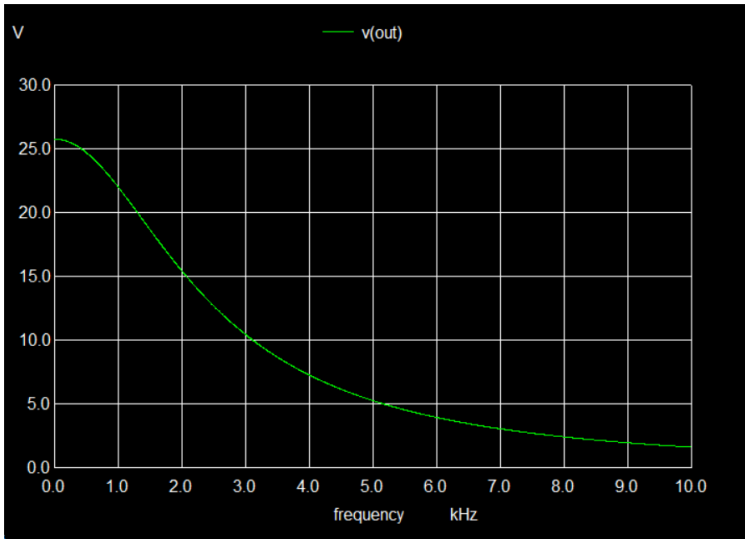

Figure6.4.1 Vout waveform

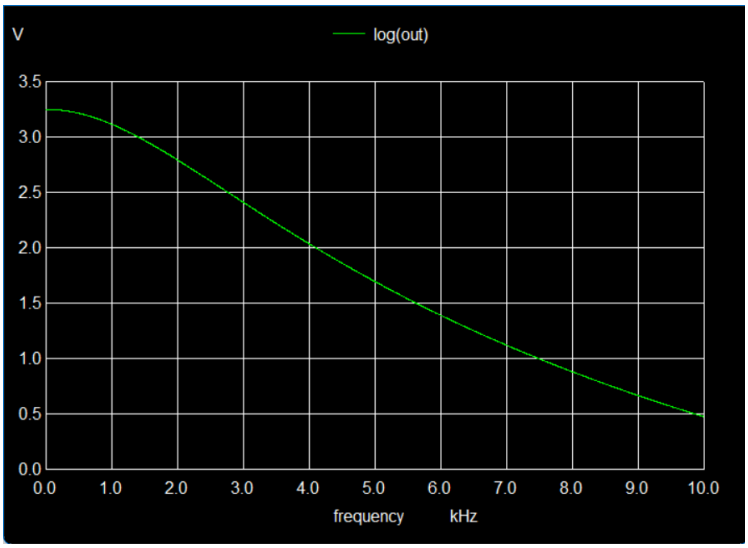

Figure6.4.2 log(out) waveform

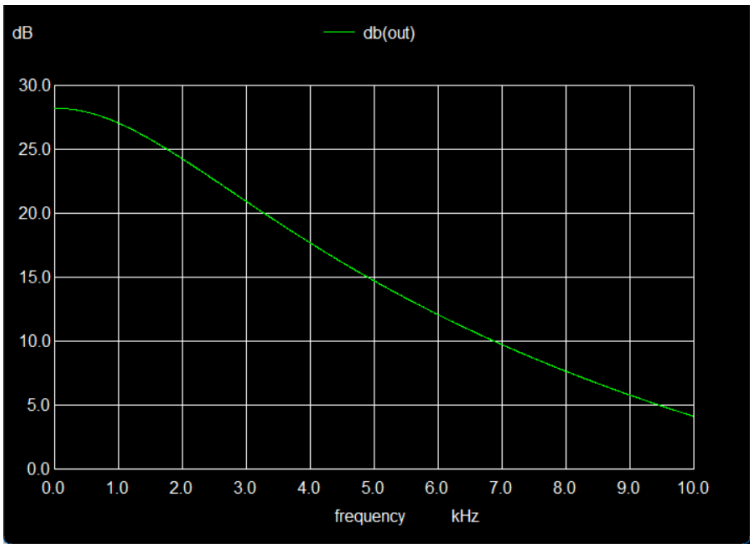

Figure6.4.3 dB(out) waveform

6.5 ANALYSIS:

Order	Gain at Stage 1 (at the end of OP-AMP 1)	Gain at Stage 2 (at the end of OP-AMP 2)	Gain at Stage 3 (at the end of OP-AMP 3)	Gain at Stage 4 (at the end of OP-AMP 4)	Gain at Stage 5 (at the end of OP-AMP 5)	Total Gain (at the end of all stages)	Minimum Offset of LM741 OP-AMP	Output voltage (Vout) in V if Vin is 4V	Output voltage (Vout) in dB if Vin is 4V	Output voltage (Vout) in log(out) if Vin is 4V
5	2	2.2382	1.382	-	-	6.58385	0.5	14.1676	28.4107	3.2709

7. MAX7413: MAX7413 is a 5th Order Switched-Capacitor Bessel Low Pass Filter for cut off frequency of 2.5kHz & Vin of 2V

7.1 CIRCUIT DIAGRAM: The internal circuit of the IC is given below.

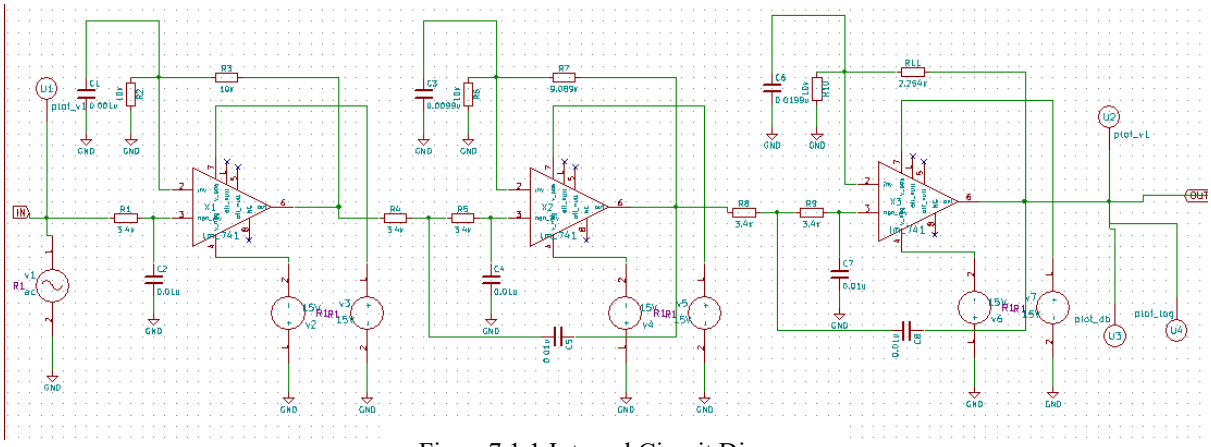

Figure7.1.1 Internal Circuit Diagram

To implement switched capacitor Bessel Low Pass Filter, replacement of resistors at input terminal with MOSFETs,

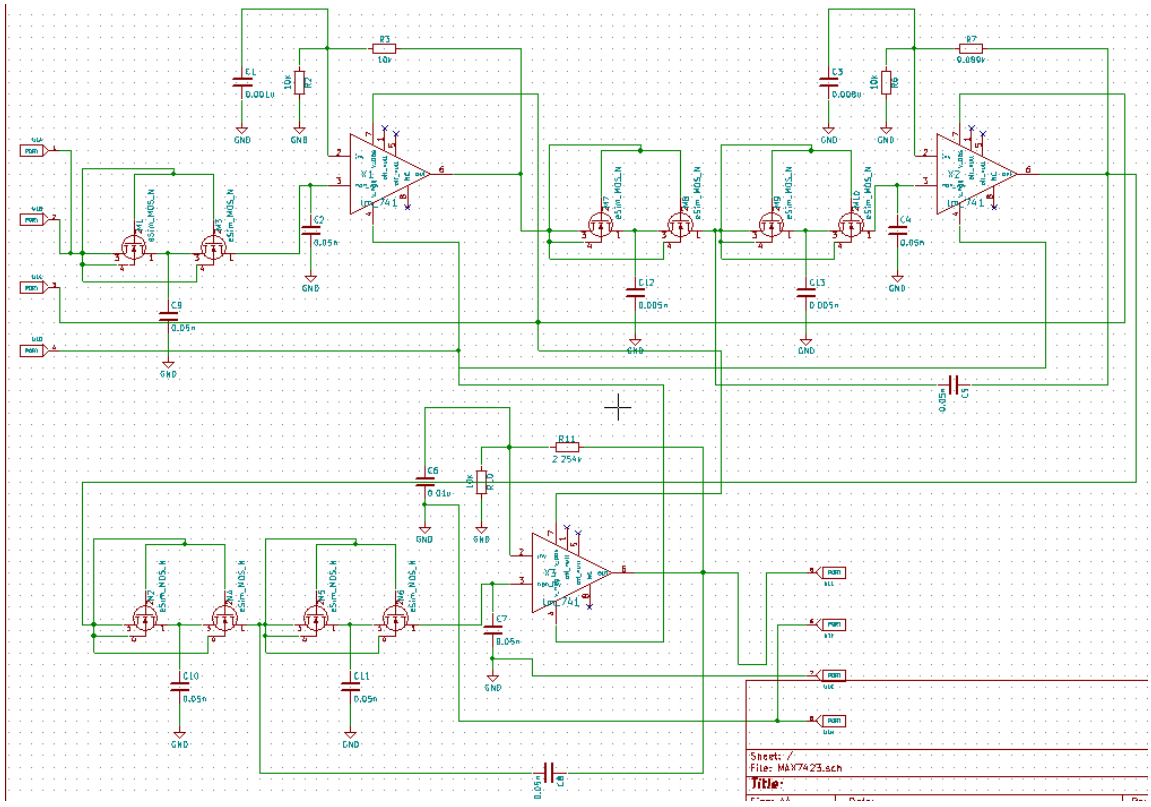

Figure7.1.2 Circuit Diagram

7.2 TEST CIRCUIT USING SUBCIRCUIT: A test circuit is implemented using the subcircuit of IC

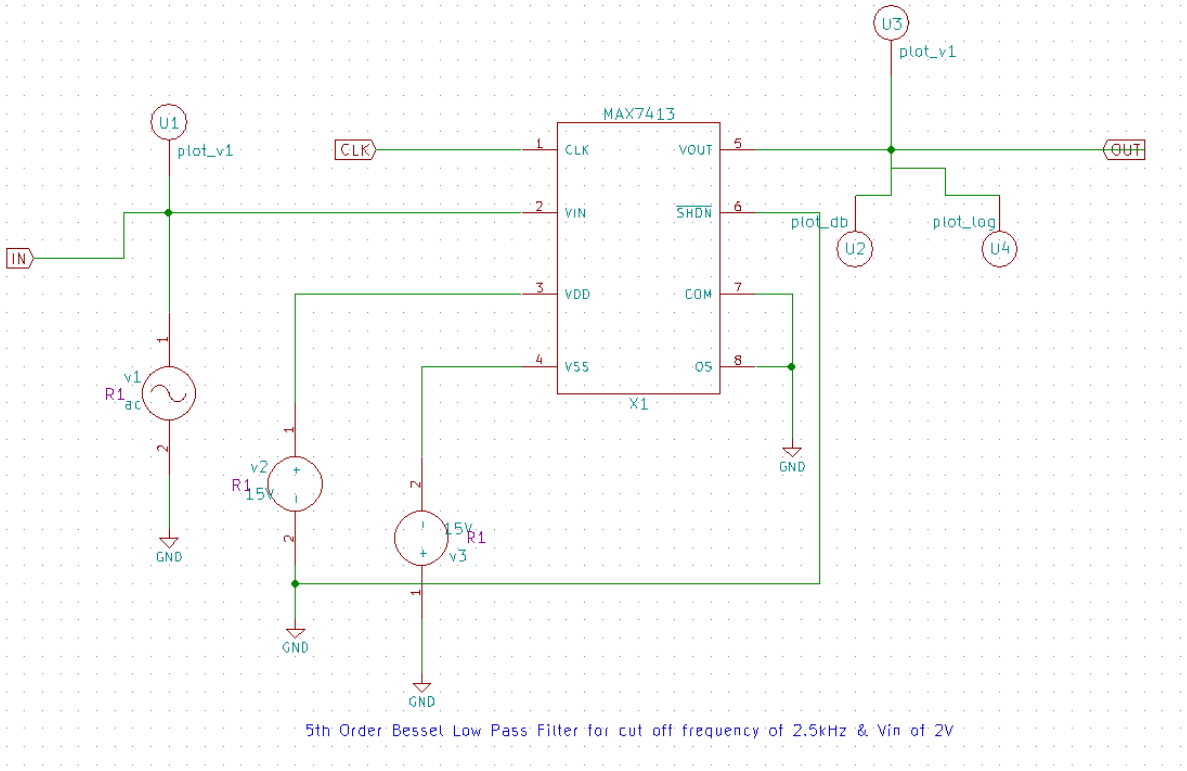

Figure7.2.1 Test Circuit

7.3 INPUT WAVEFORM: AC input waveform

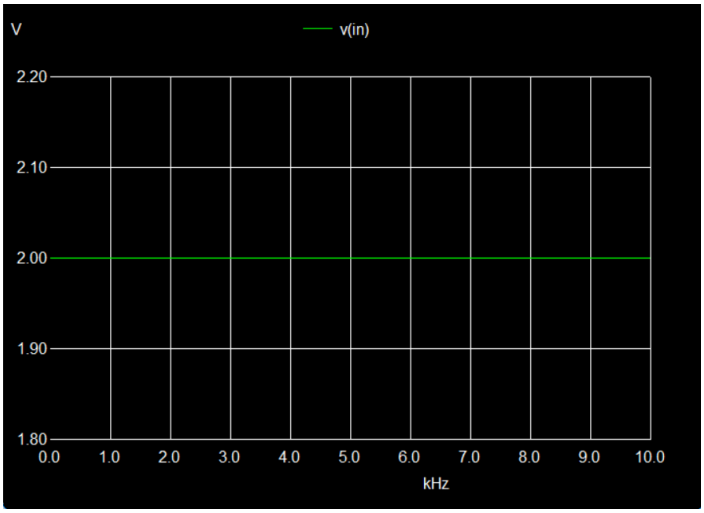

Figure7.3.1 Input waveform

7.4 OUTPUT WAVEFORM: Compare the output waveforms with the values given in Analysis table below.

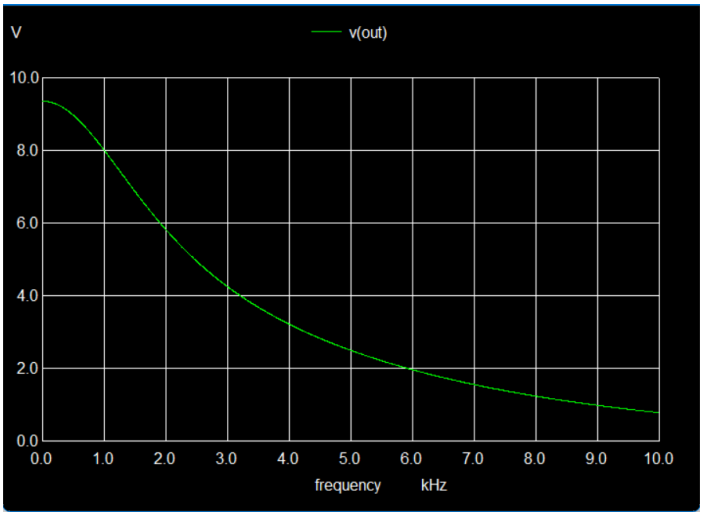

Figure7.4.1 Vout waveform

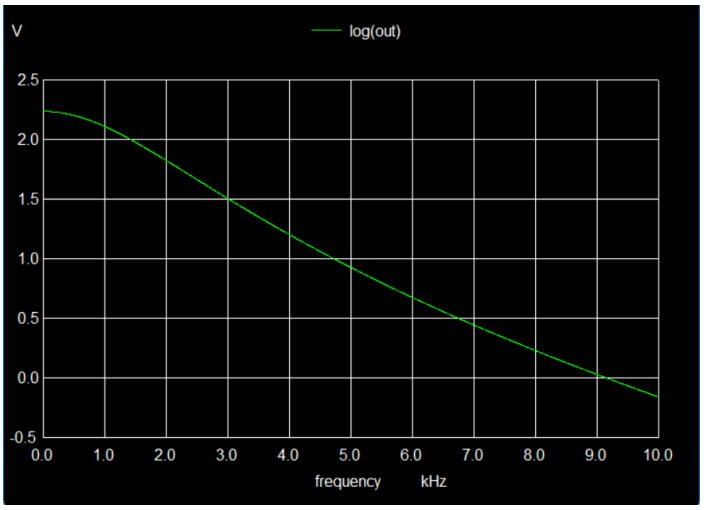

Figure7.4.2 log(out) waveform

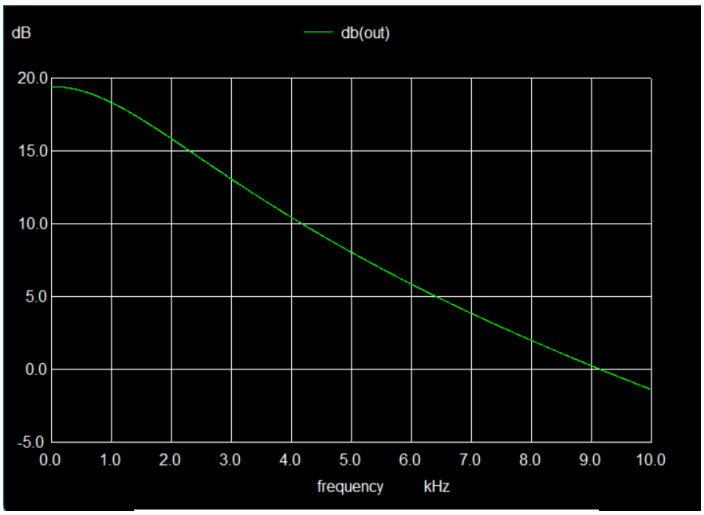

Figure7.4.3 dB(out) waveform

7.5 ANALYSIS:

Order	Gain at Stage 1 (at the end of OP-AMP 1)	Gain at Stage 2 (at the end of OP-AMP 2)	Gain at Stage 3 (at the end of OP-AMP 3)	Gain at Stage 4 (at the end of OP-AMP 4)	Gain at Stage 5 (at the end of OP-AMP 5)	Total Gain (at the end of all stages)	Minimum Offset of LM741 OP-AMP	Output voltage (Vout) in V if Vin is 2V	Output voltage (Vout) in dB if Vin is 2V	Output voltage (Vout) in log(out) if Vin is 2V
5	2	1.9089	1.2254	-	-	4.6783	0.5	5.3638	19.4224	2.2361

8. MAX7409: MAX7409 is a 5th Order Switched-Capacitor Bessel Low Pass Filter for cut off frequency of 2.5kHz & Vin of 4V

8.1 CIRCUIT DIAGRAM: The internal circuit of the IC is given below.

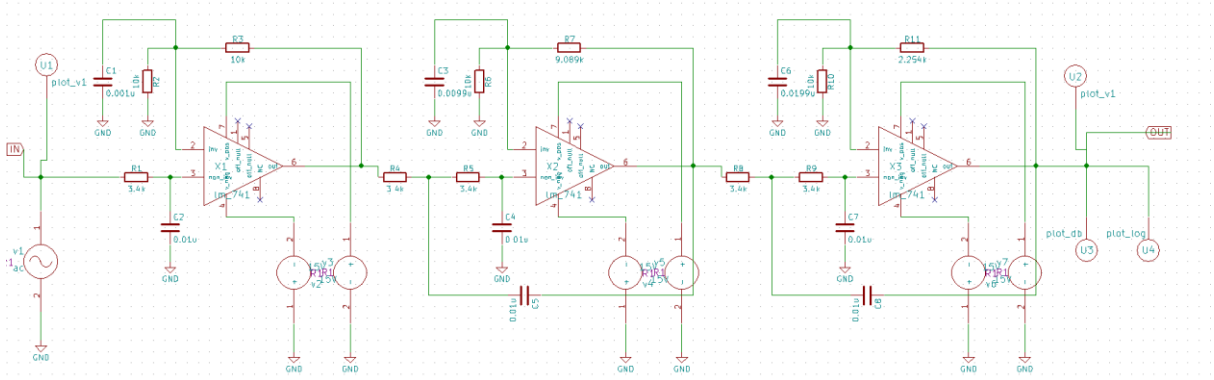

Figure8.1.1 Internal Circuit Diagram

To implement switched capacitor Bessel Low Pass Filter, replacement of resistors at input terminal with MOSFETs,

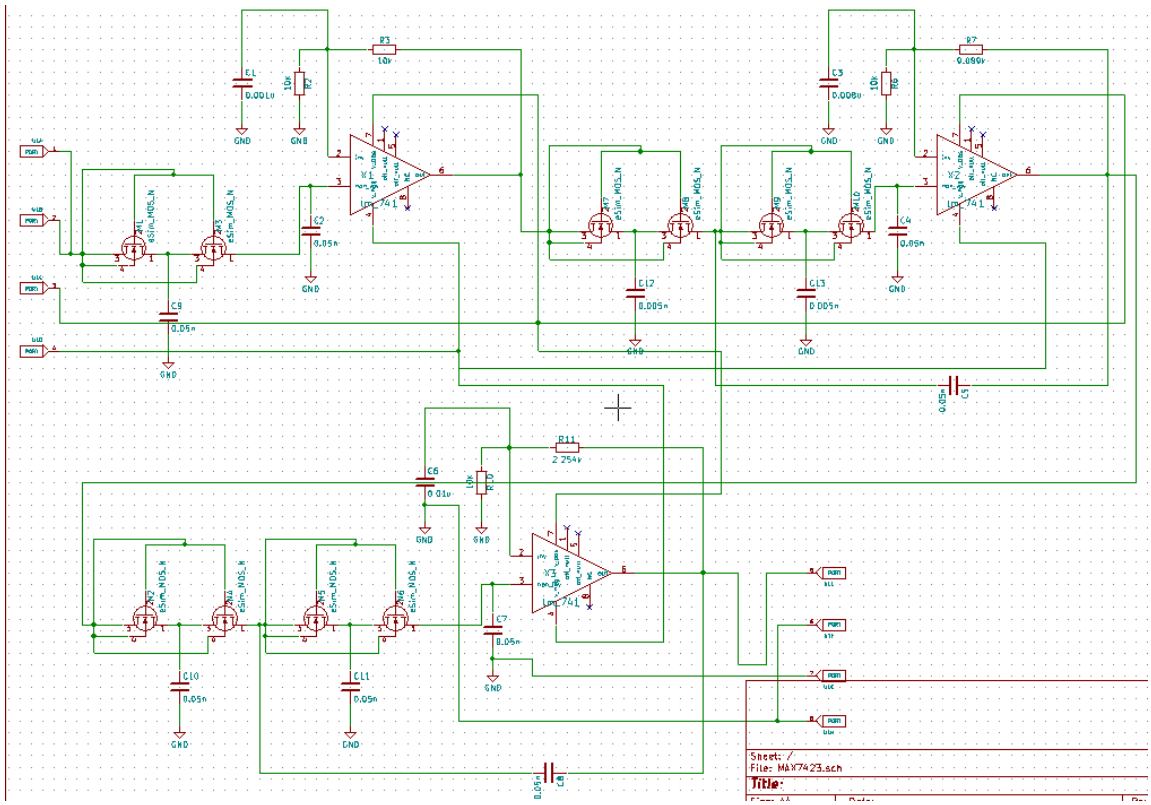

Figure8.1.2 Circuit Diagram

8.2 TEST CIRCUIT USING SUBCIRCUIT: A test circuit is implemented using the subcircuit of IC

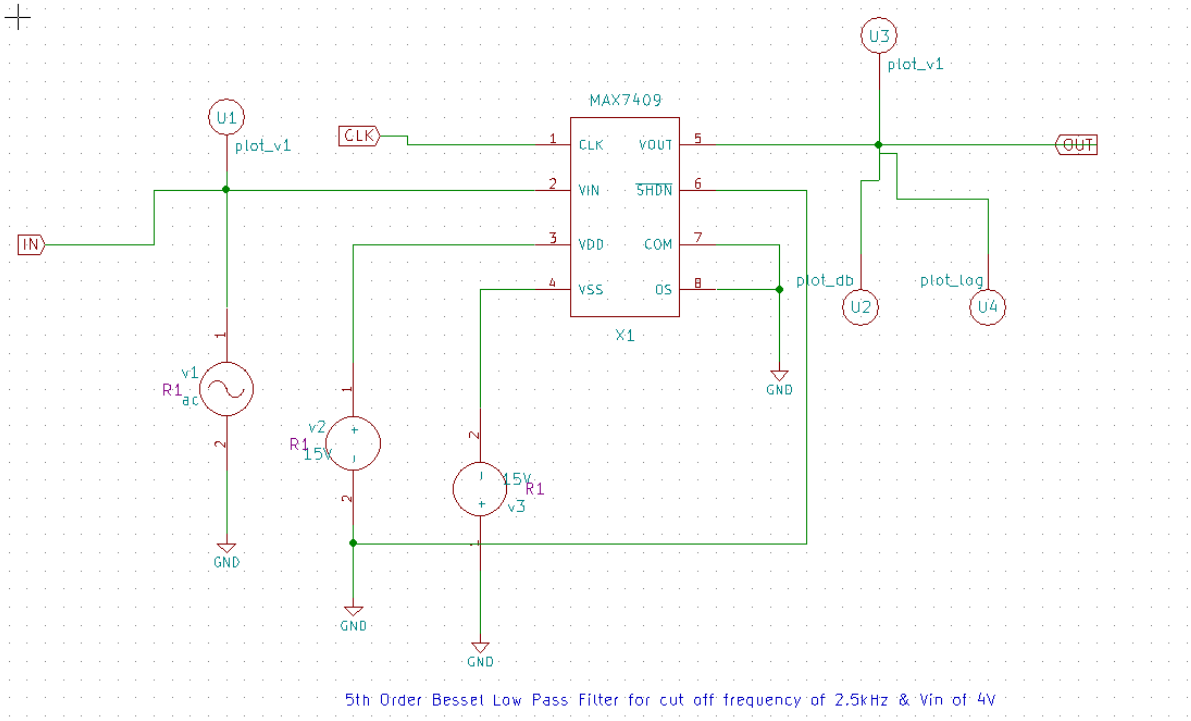

Figure8.2.1 Test Circuit

8.3 INPUT WAVEFORM: AC input waveform

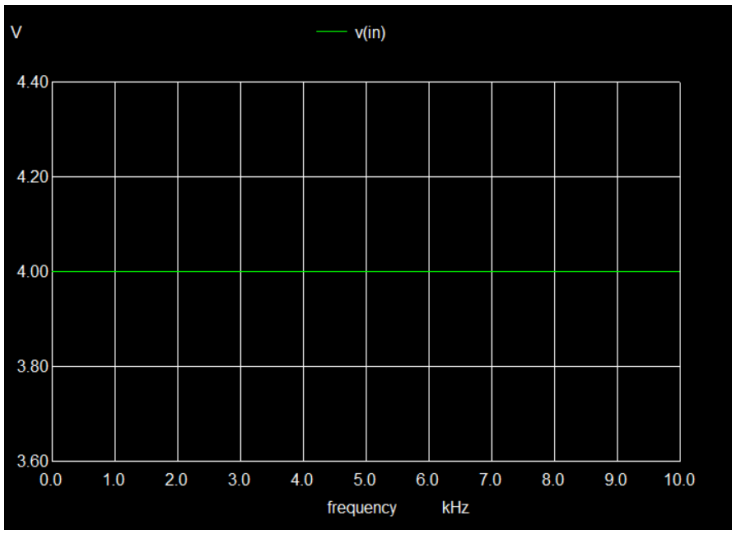

Figure8.3.1 Input waveform

8.4 OUTPUT WAVEFORM: Compare the output waveforms with the values given in Analysis table below.

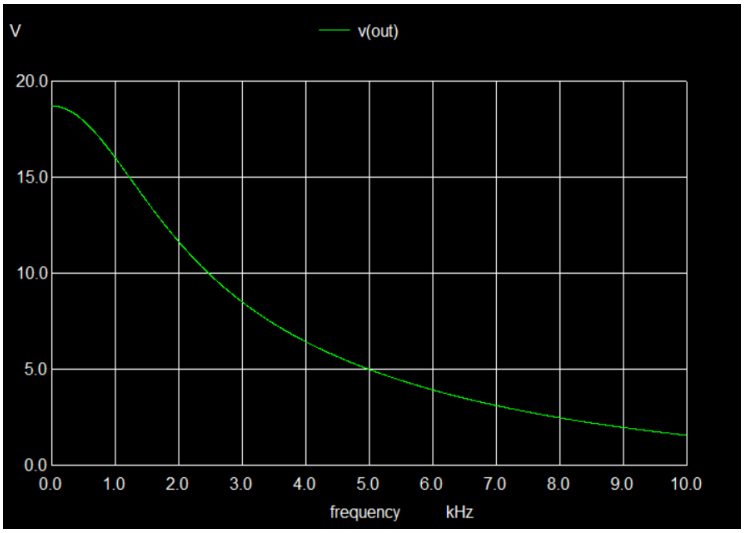

Figure8.4.1 Vout waveform

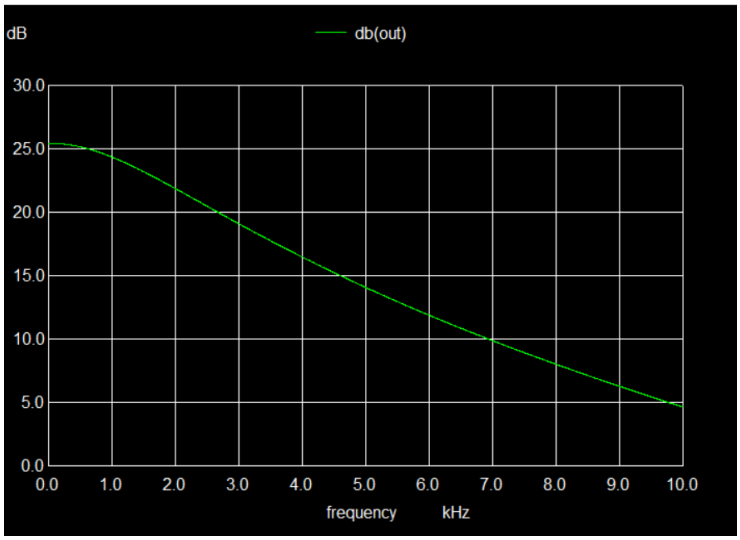

Figure8.4.2 log(out) waveform

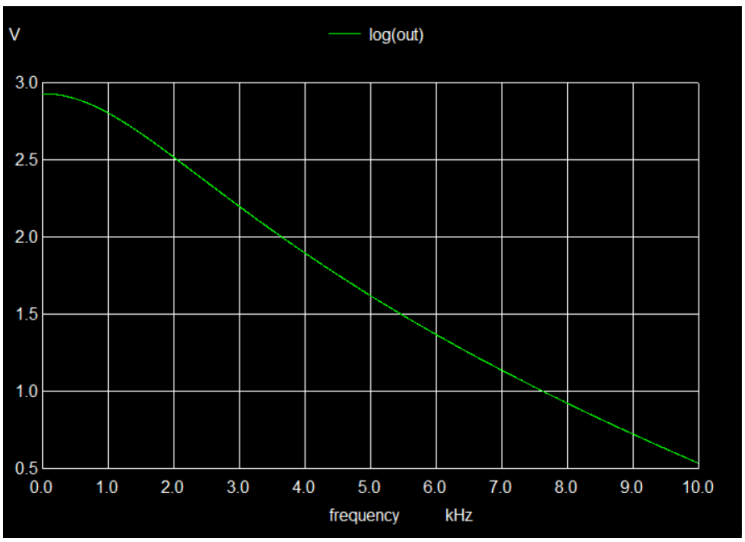

Figure8.4.3 dB(out) waveform

8.5 ANALYSIS:

Order	Gain at Stage 1 (at the end of OP-AMP 1)	Gain at Stage 2 (at the end of OP-AMP 2)	Gain at Stage 3 (at the end of OP-AMP 3)	Gain at Stage 4 (at the end of OP-AMP 4)	Gain at Stage 5 (at the end of OP-AMP 5)	Total Gain (at the end of all stages)	Minimum Offset of LM741 OP-AMP	Output voltage (Vout) in V if Vin is 4V	Output voltage (Vout) in dB if Vin is 4V	Output voltage (Vout) in log(out) if Vin is 4V
5	2	1.9089	1.2254	-	-	4.6783	0.5	9.9716	25.4429	2.9292

9. MAX7420: MAX7420 is a 5th Order Switched-Capacitor Butterworth Low Pass Filter for cut off frequency of 4.5kHz

9.1 CIRCUIT DIAGRAM: The internal circuit of the IC is given below.

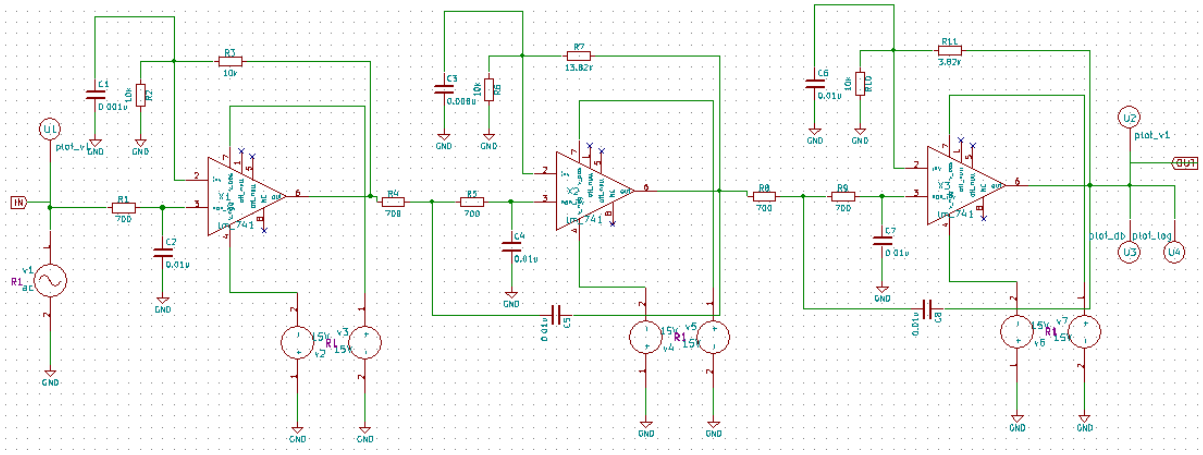

Figure9.1.1 Internal Circuit Diagram

To implement switched capacitor Butterworth Low Pass Filter, replacement of resistors at input terminal with MOSFETs,

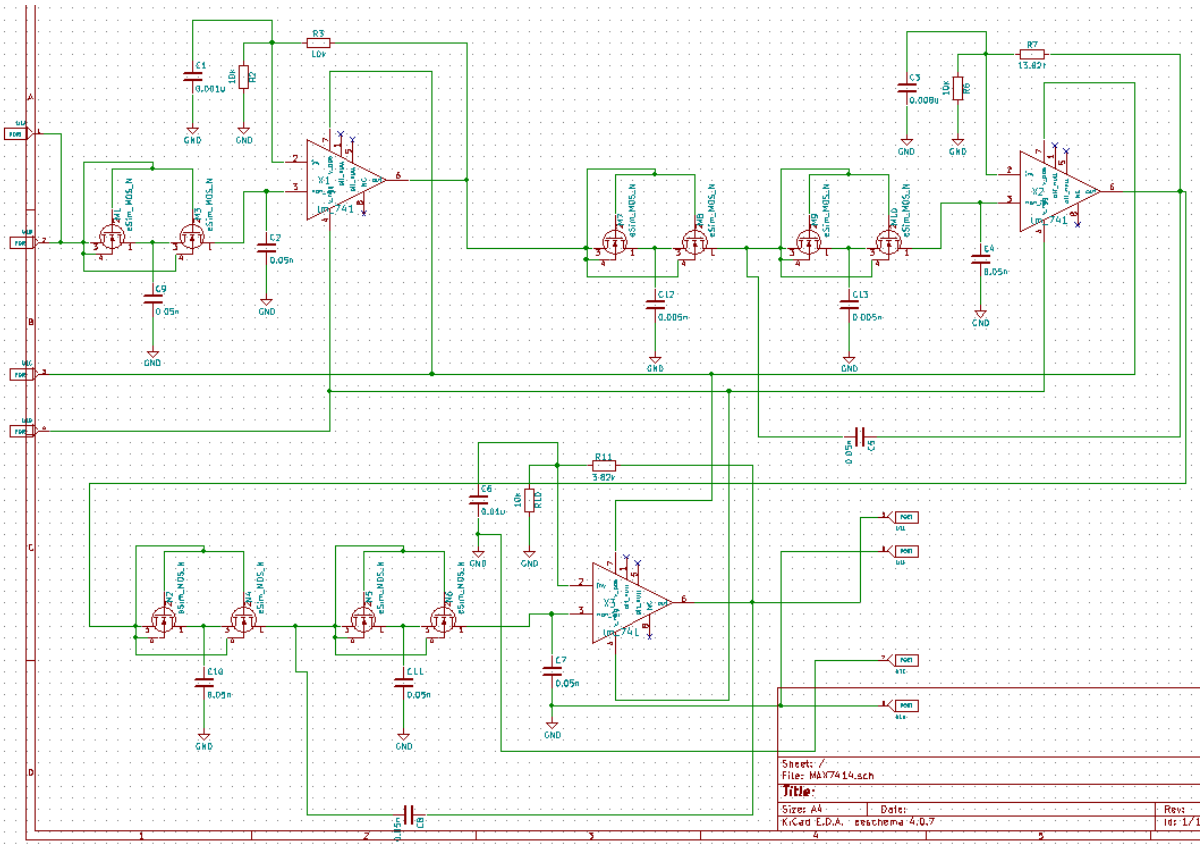

Figure9.1.2 Circuit Diagram

9.2 TEST CIRCUIT USING SUBCIRCUIT: A test circuit is implemented using the subcircuit of IC

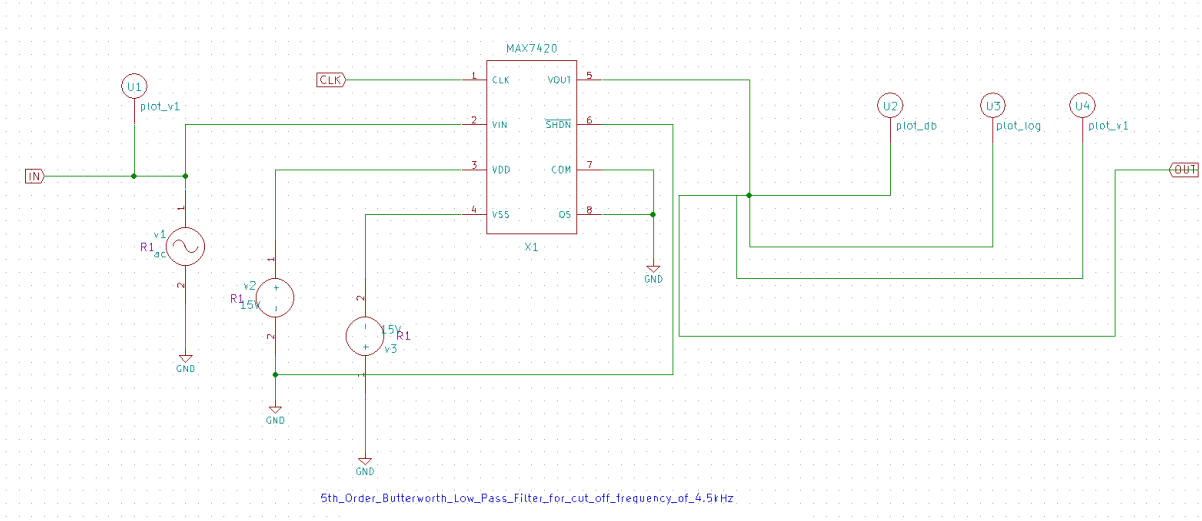

Figure9.2.1 Test Circuit

9.3 INPUT WAVEFORM: AC input waveform

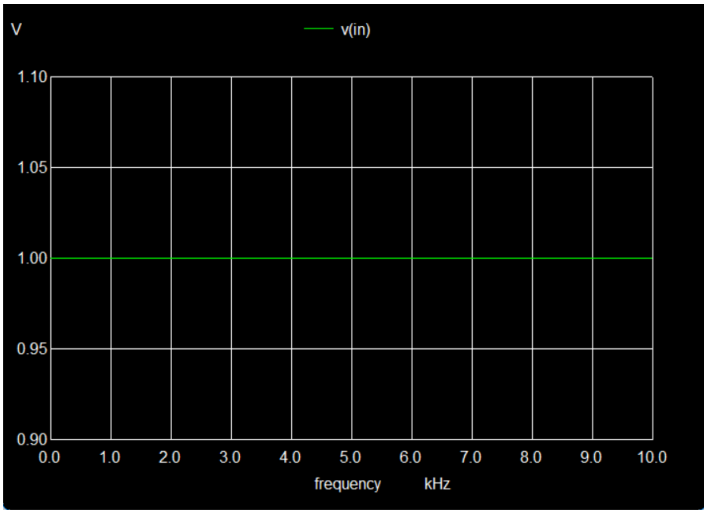

Figure9.3.1 Input waveform

9.4 OUTPUT WAVEFORM: Compare the output waveforms with the values given in Analysis table below.

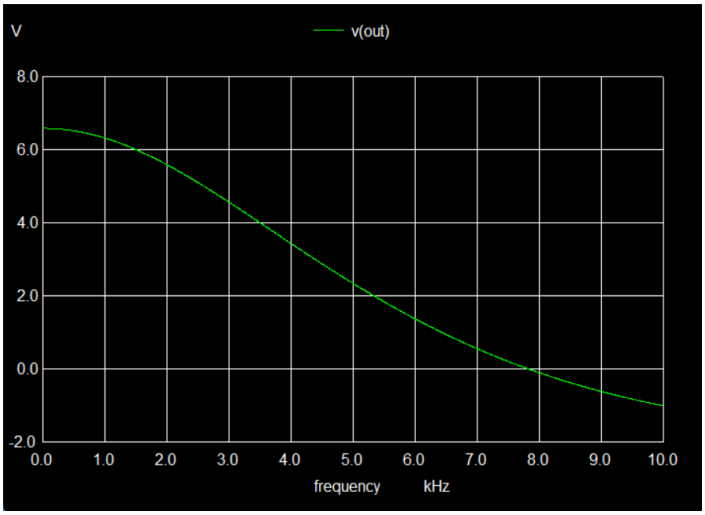

Figure9.4.1 Vout waveform

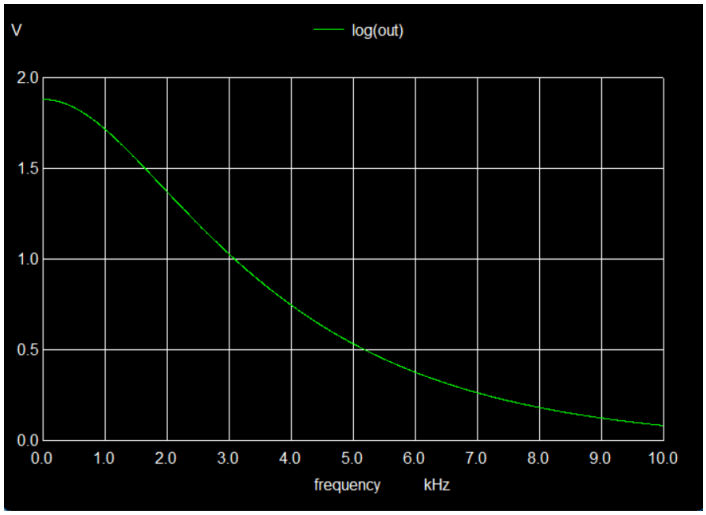

Figure9.4.2 log(out) waveform

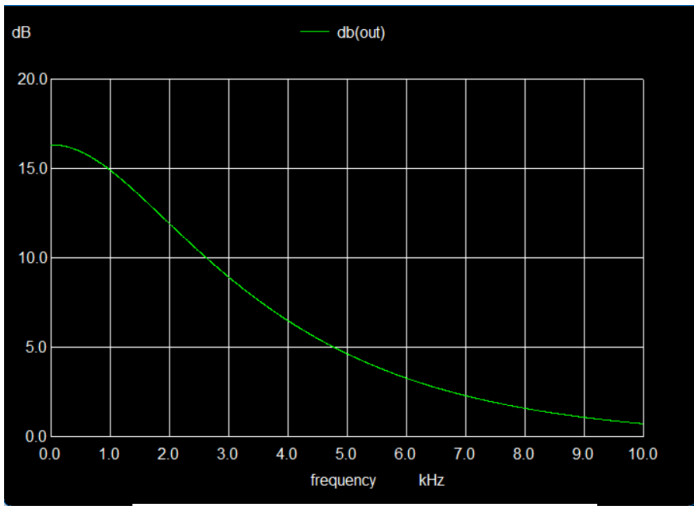

Figure9.4.3 dB(out) waveform

9.5 ANALYSIS:

Order	Gain at Stage 1 (at the end of OP-AMP 1)	Gain at Stage 2 (at the end of OP-AMP 2)	Gain at Stage 3 (at the end of OP-AMP 3)	Gain at Stage 4 (at the end of OP-AMP 4)	Gain at Stage 5 (at the end of OP-AMP 5)	Total Gain (at the end of all stages)	Minimum Offset of LM741 OP-AMP	Output voltage (Vout) in V if Vin is 1V	Output voltage (Vout) in dB if Vin is 1V	Output voltage (Vout) in log(out) if Vin is 1V
5	2	2.2382	1.382	-	-	6.58385	0.5	3.2919	16.3695	1.8846

10. MAX7424: MAX7424 is a 5th Order Switched-Capacitor Butterworth Low Pass Filter for cut off frequency of 5kHz

10.1 CIRCUIT DIAGRAM: The internal circuit of the IC is given below.

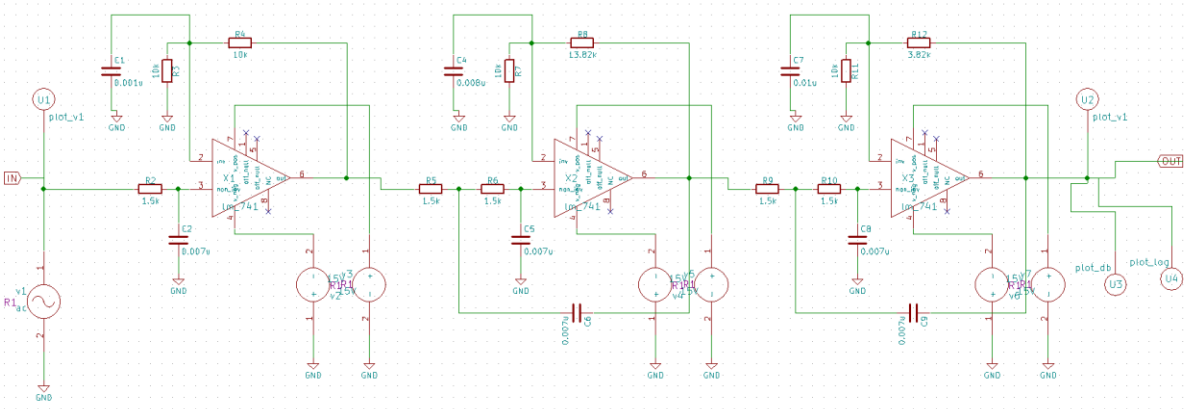

Figure10.1.1 Internal Circuit Diagram

To implement switched capacitor Butterworth Low Pass Filter, replacement of resistors at input terminal with MOSFETs,

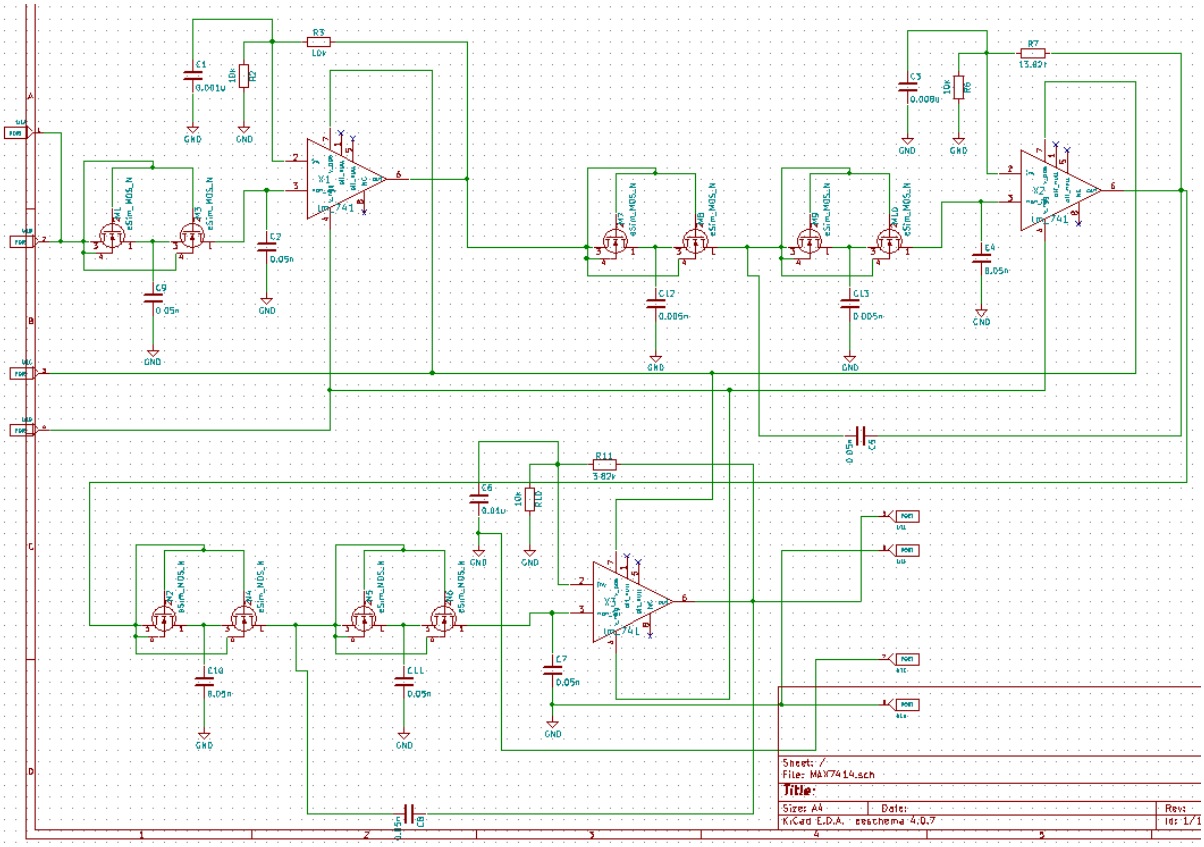

Figure10.1.2 Circuit Diagram

10.2 TEST CIRCUIT USING SUBCIRCUIT: A test circuit is implemented using the subcircuit of IC

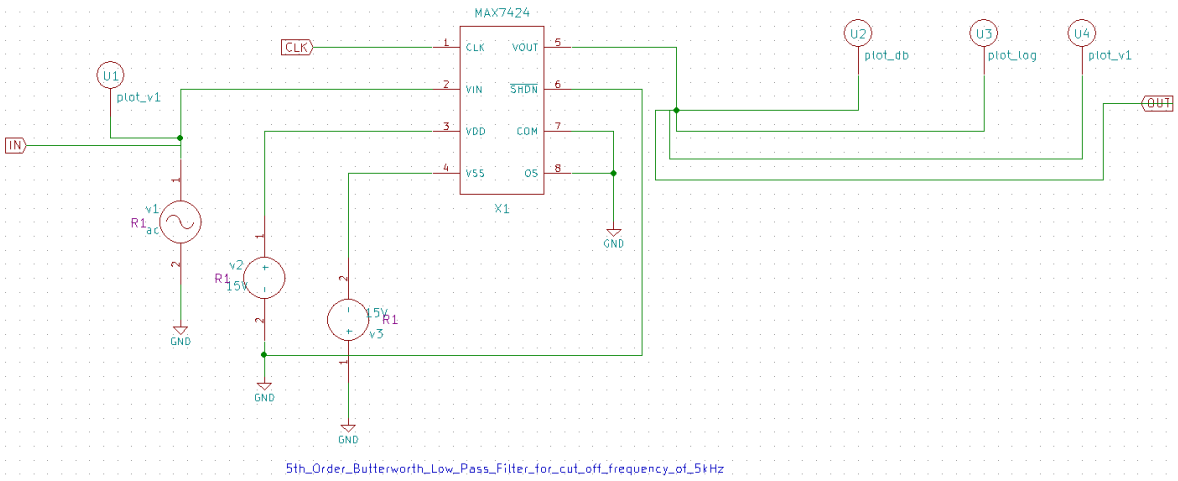

Figure10.2.1 Test Circuit

10.3 INPUT WAVEFORM: AC input waveform

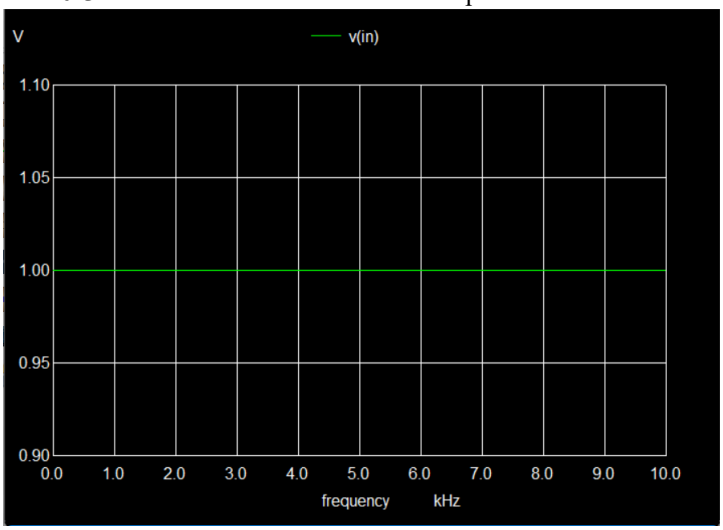

Figure10.3.1 Input waveform

10.4 OUTPUT WAVEFORM: Compare the output waveforms with the values given in Analysis table below.

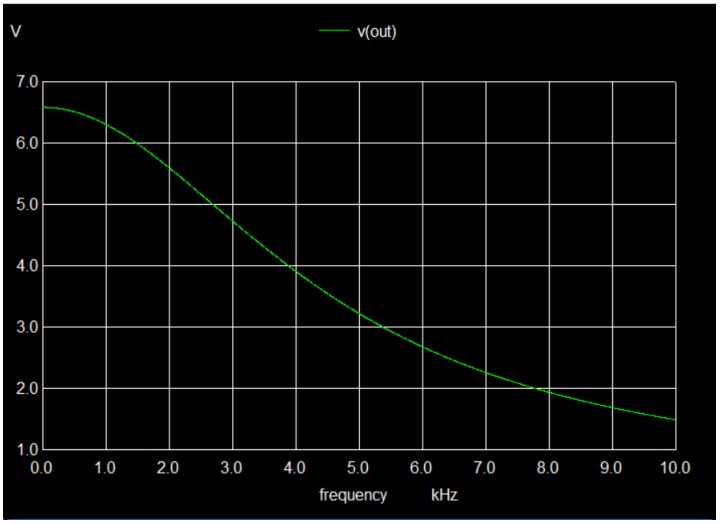

Figure10.4.1 Vout waveform

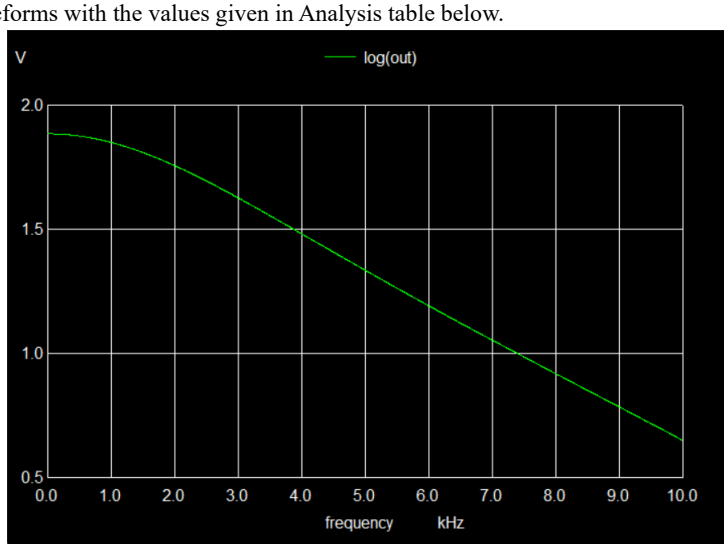

Figure10.4.2 log(out) waveform

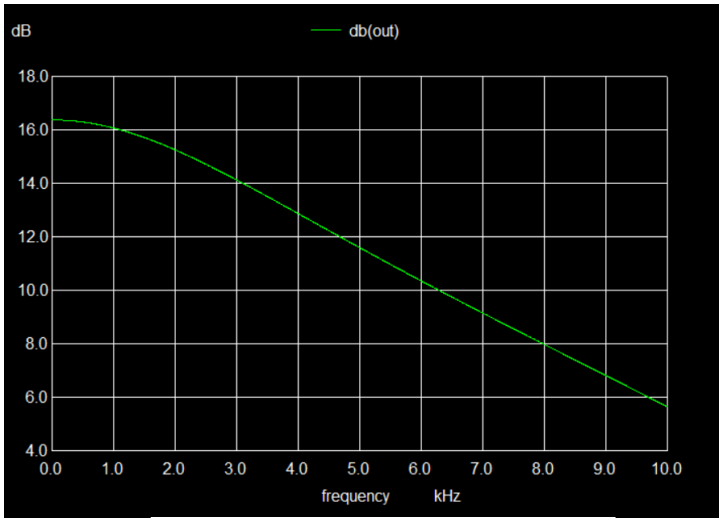

Figure10.4.3 dB(out) waveform

10.5 ANALYSIS:

Order	Gain at Stage 1 (at the end of OP-AMP 1)	Gain at Stage 2 (at the end of OP-AMP 2)	Gain at Stage 3 (at the end of OP-AMP 3)	Gain at Stage 4 (at the end of OP-AMP 4)	Gain at Stage 5 (at the end of OP-AMP 5)	Total Gain (at the end of all stages)	Minimum Offset of LM741 OP-AMP	Output voltage (Vout) in V if Vin is 1V	Output voltage (Vout) in dB if Vin is 1V	Output voltage (Vout) in log(out) if Vin is 1V
5	2	2.2382	1.382	-	-	6.58385	0.5	3.2919	16.3695	1.8846

11. MAX7419: MAX7419 is a 5th Order Switched-Capacitor Bessel Low Pass Filter for cut off frequency of 6.5kHz

11.1 CIRCUIT DIAGRAM: The internal circuit of the IC is given below.

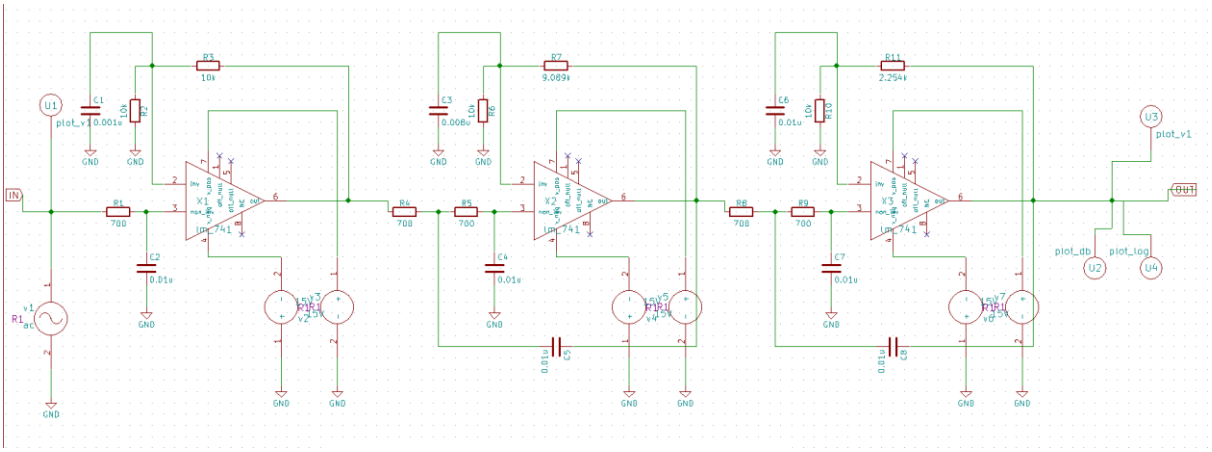

Figure11.1.1 Internal Circuit Diagram

To implement switched capacitor Bessel Low Pass Filter, replacement of resistors at input terminal with MOSFETs,

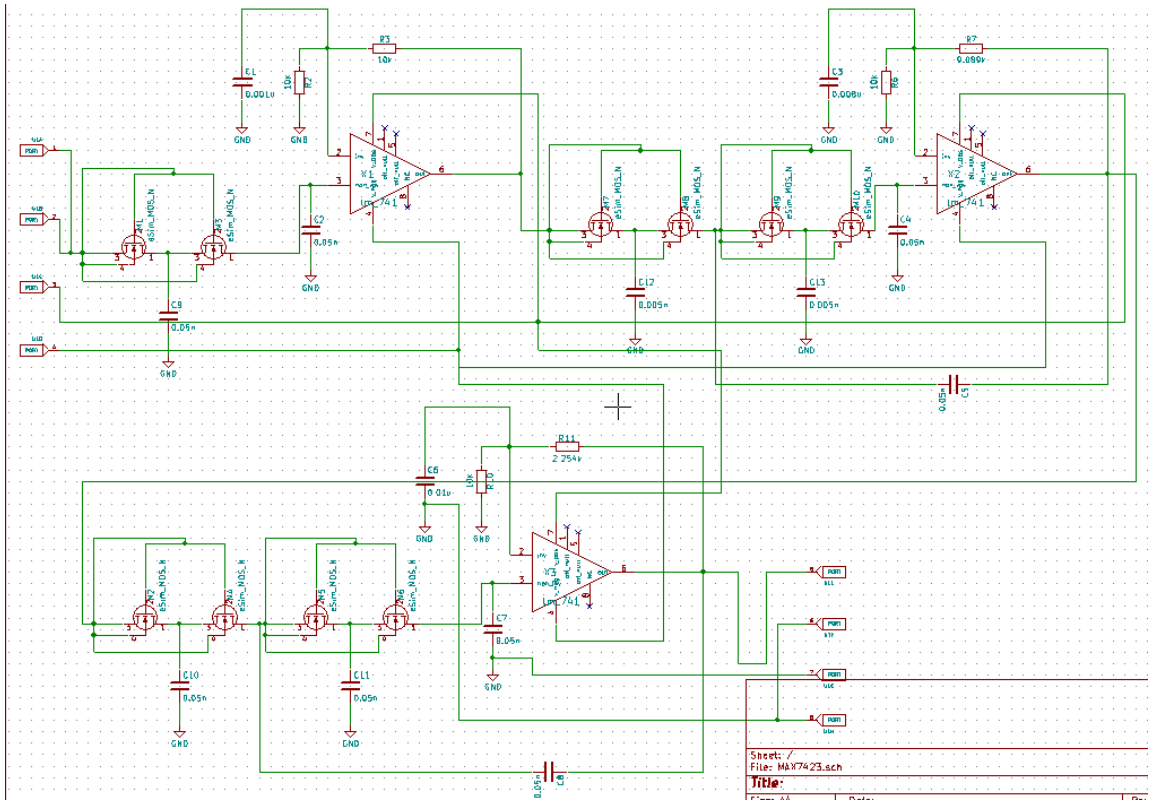

Figure11.1.2 Circuit Diagram

11.2 TEST CIRCUIT USING SUBCIRCUIT: A test circuit is implemented using the subcircuit of IC

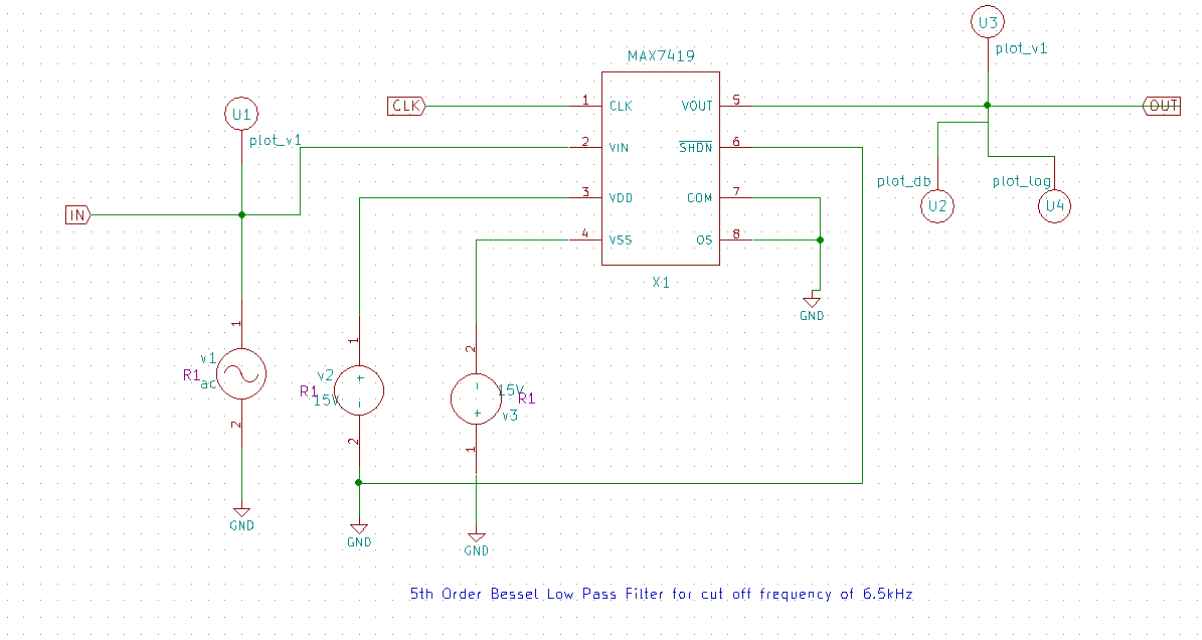

Figure11.2.1 Test Circuit

11.3 INPUT WAVEFORM: AC input waveform

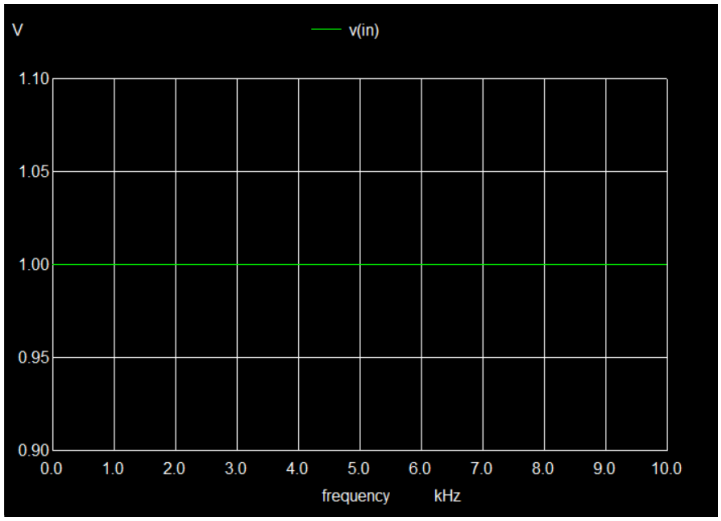

Figure11.3.1 Input waveform

11.4 OUTPUT WAVEFORM: Compare the output waveforms with the values given in Analysis table below.

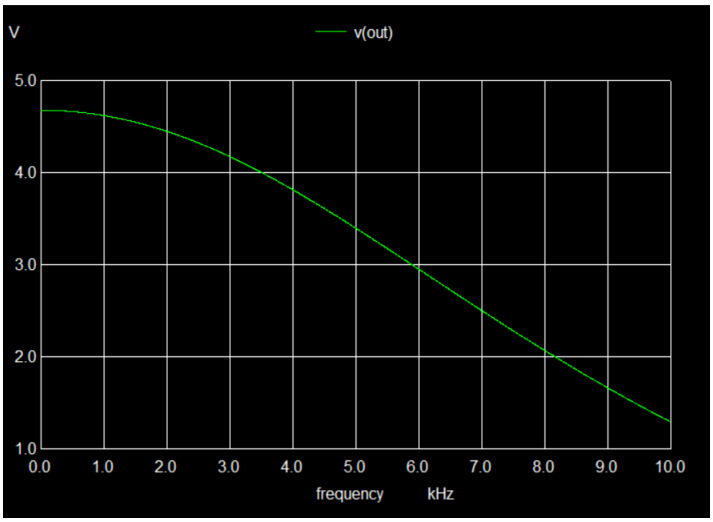

Figure11.4.1 Vout waveform

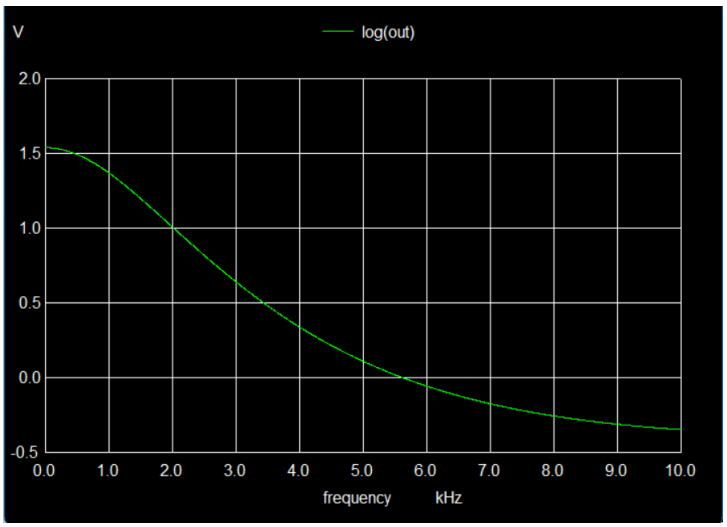

Figure11.4.2 log(out) waveform

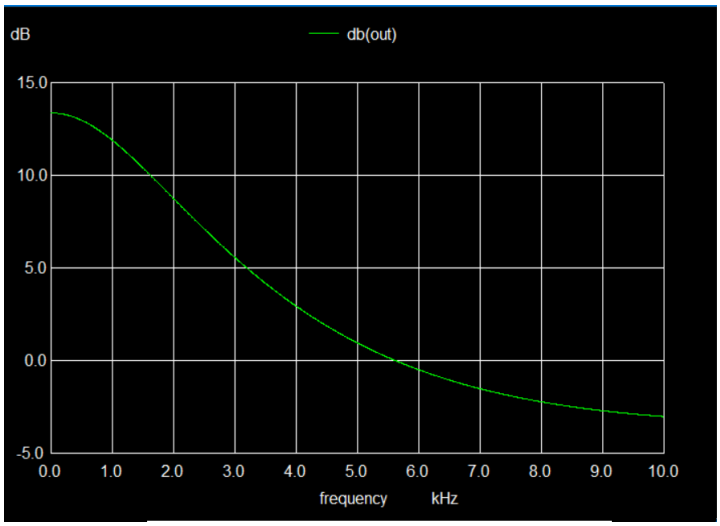

Figure11.4.3 dB(out) waveform

11.5 ANALYSIS:

Order	Gain at Stage 1 (at the end of OP-AMP 1)	Gain at Stage 2 (at the end of OP-AMP 2)	Gain at Stage 3 (at the end of OP-AMP 3)	Gain at Stage 4 (at the end of OP-AMP 4)	Gain at Stage 5 (at the end of OP-AMP 5)	Total Gain (at the end of all stages)	Minimum Offset of LM741 OP-AMP	Output voltage (Vout) in V if Vin is 1V	Output voltage (Vout) in dB if Vin is 1V	Output voltage (Vout) in log(out) if Vin is 1V
5	2	1.9089	1.2254	-	-	4.6783	0.5	2.6819	14.5916	1.5429

12. MAX7423: MAX7423 is a 5th Order Switched-Capacitor Bessel Low Pass Filter for cut off frequency of 7kHz

12.1 CIRCUIT DIAGRAM: The internal circuit of the IC is given below.

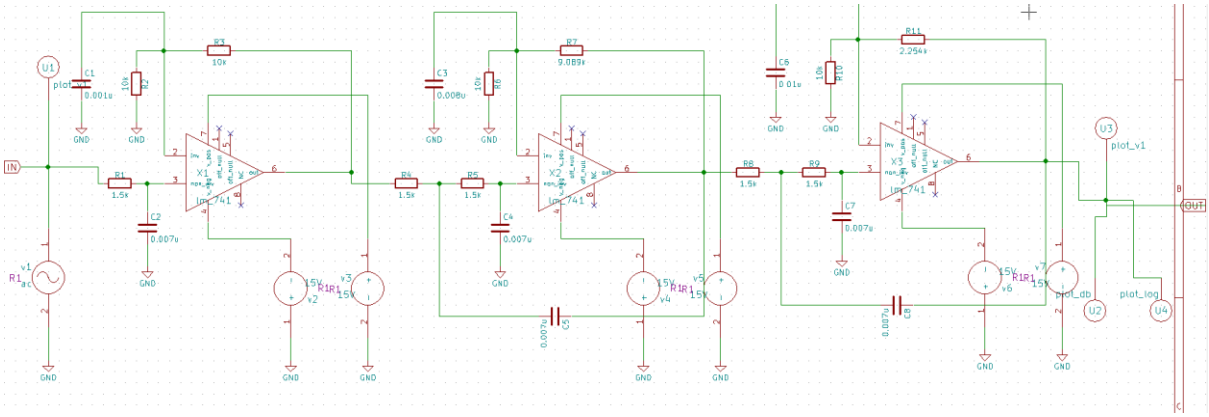

Figure12.1.1 Internal Circuit Diagram

To implement switched capacitor Bessel Low Pass Filter, replacement of resistors at input terminal with MOSFETs,

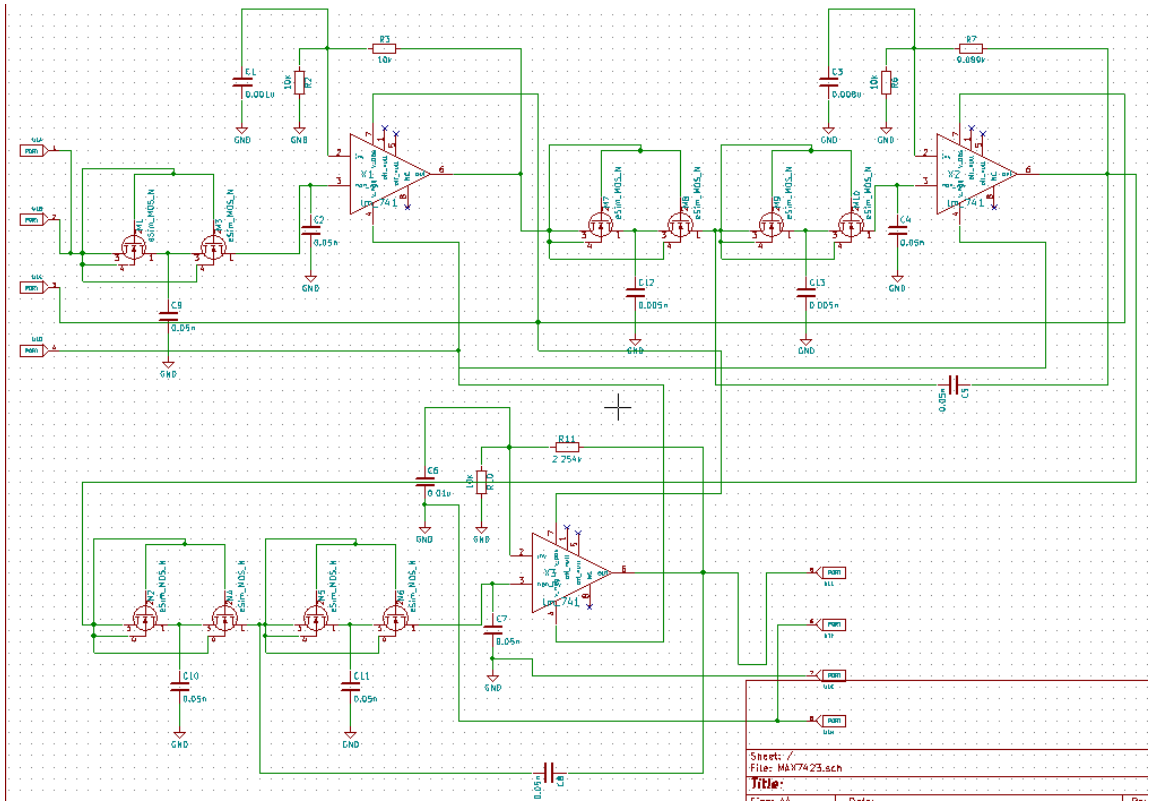

Figure12.1.2 Circuit Diagram

12.2 TEST CIRCUIT USING SUBCIRCUIT: A test circuit is implemented using the subcircuit of IC

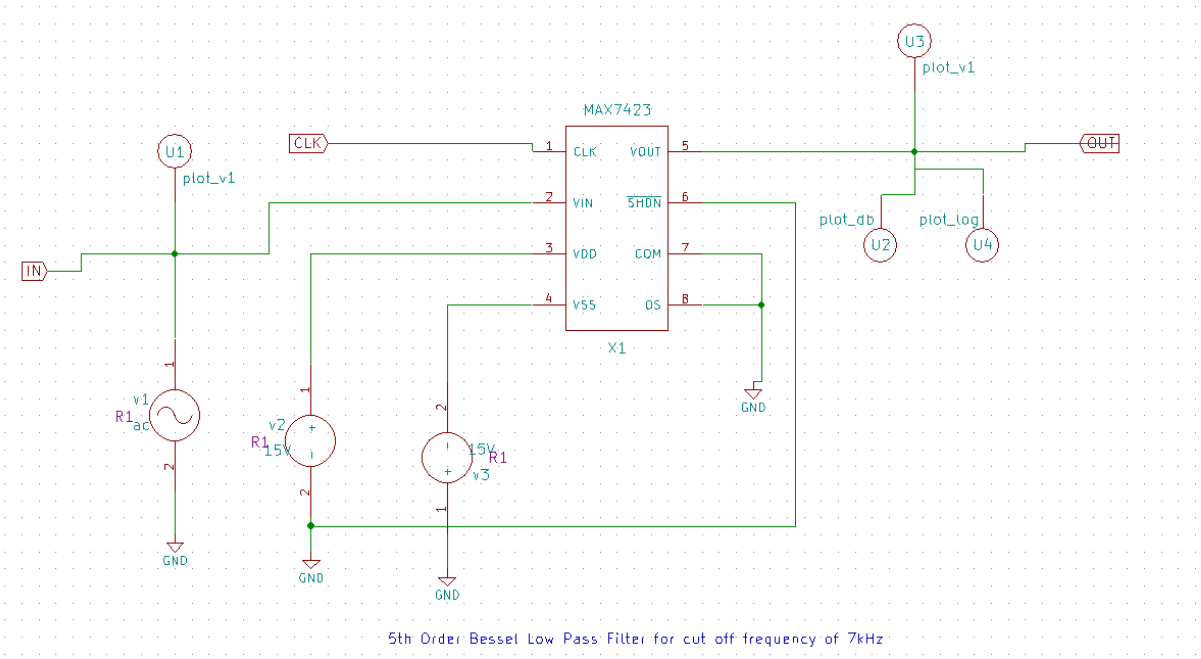

Figure12.2.1 Test Circuit

12.3 INPUT WAVEFORM: AC input waveform

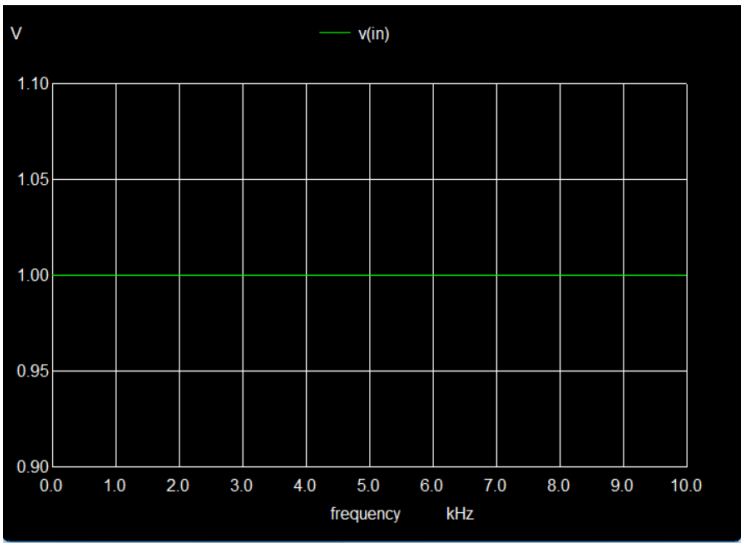

Figure12.3.1 Input waveform

12.4 OUTPUT WAVEFORM: Compare the output waveforms with the values given in Analysis table below.

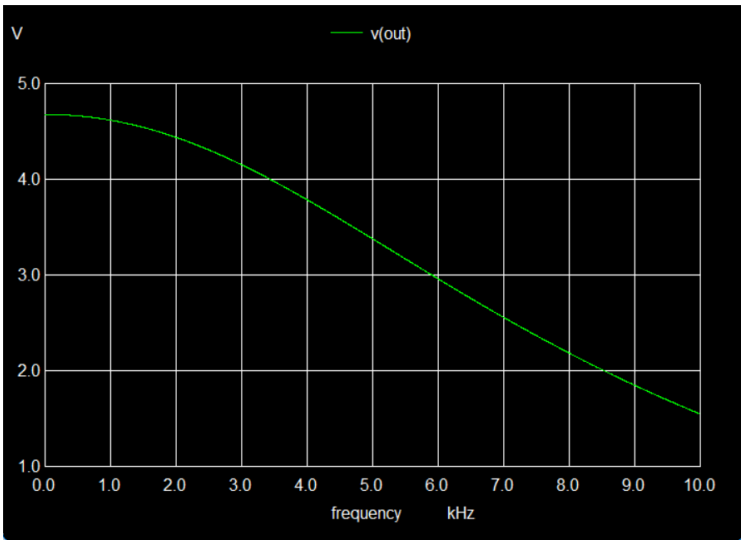

Figure12.4.1 Vout waveform

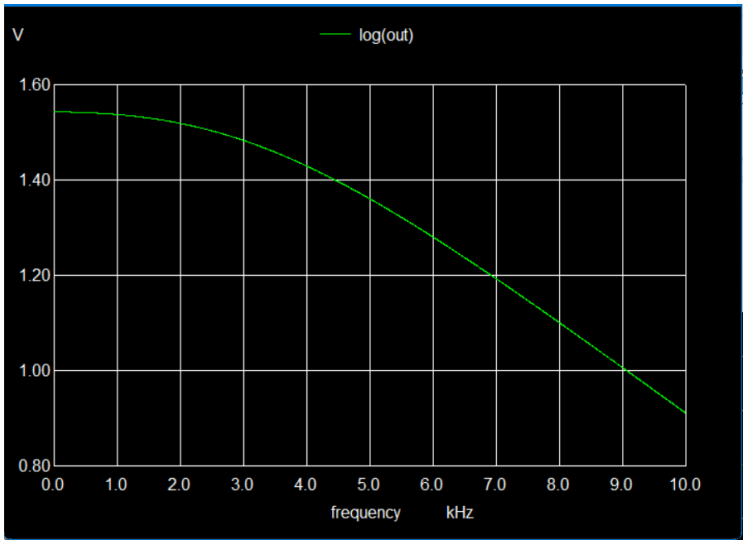

Figure12.4.2 log(out) waveform

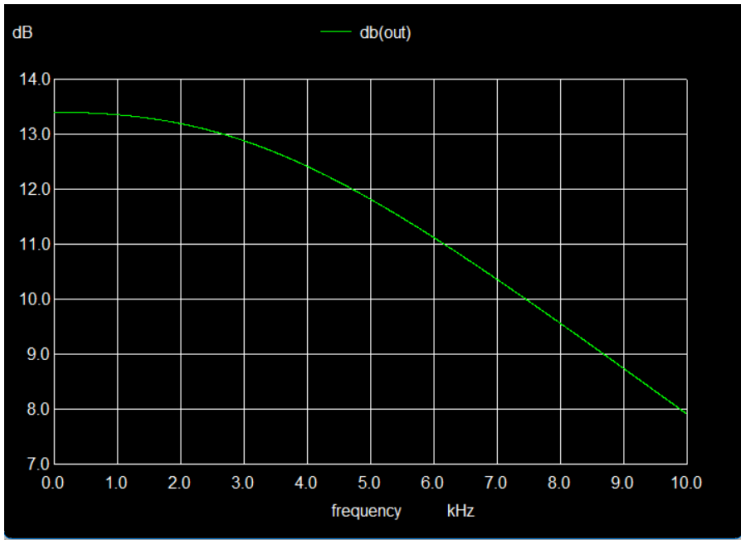

Figure12.4.3 dB(out) waveform

12.5 ANALYSIS:

Order	Gain at Stage 1 (at the end of OP-AMP 1)	Gain at Stage 2 (at the end of OP-AMP 2)	Gain at Stage 3 (at the end of OP-AMP 3)	Gain at Stage 4 (at the end of OP-AMP 4)	Gain at Stage 5 (at the end of OP-AMP 5)	Total Gain (at the end of all stages)	Minimum Offset of LM741 OP-AMP	Output voltage (Vout) in V if Vin is 1V	Output voltage (Vout) in dB if Vin is 1V	Output voltage (Vout) in log(out) if Vin is 1V
5	2	1.9089	1.2254	-	-	4.6783	0.5	2.6819	14.4017	1.5429

13. PIN DESCRIPTION OF ICs

LTC6603:

+VIN(A): Input to Non-Inverting terminal of Channel A
-VIN(A): Input to Inverting terminal of Channel A
+VIN(B): Input to Non-Inverting terminal of Channel B
-VIN(B): Input to Inverting terminal of Channel B
+VOUT(A), -VOUT(A): Outputs of Channel A
+VOUT(B), -VOUT(B): Outputs of Channel B
VDD: Positive DC supply voltage for the IC
VSS: Negative DC supply voltage for the IC

LTC1565-31:

+VIN: Input to Non-Inverting terminal of the filter
-VIN: Input to Non-Inverting terminal of the filter
+VOUT, -VOUT: Outputs of the filter
VDD: Positive DC supply voltage for the IC
VSS: Negative DC supply voltage for the IC
~SHDN: Shutdown. When voltage to this pin is low, it goes to current saving mode. When the pin is open, it is in normal operating mode.
GND: Ground pin.

All MAX series (MAX7409, MAX7410, MAX7413, MAX7414, MAX7419, MAX7420, MAX7423, MAX7424):

VIN: AC Input provided to the filter
VOUT: Output of the filter
VDD: Positive DC supply voltage for the IC
VSS: Negative DC supply voltage for the IC
~SHDN: Shutdown. When voltage to this pin is low, it goes to current saving mode. When the pin is open, it is in normal operating mode.
COM: Common Input Pin. Biased internally at midsupply. Bypass COM externally to GND.
OS: Offset Adjust Input. Connect OS to COM when no offset adjustment is needed.

14. DESIGN OF BUTTERWORTH LOW PASS FILTERS FROM 1ST ORDER TO 10TH ORDER

BUTTERWORTH FILTER TABLE

Order(n)	Normalized Denominator Polynomials in Factored form
1	$1+s$
2	$1+1.414s+s^2$
3	$(1+s)(1+s+s^2)$
4	$(1+0.765s+s^2)(1+1.848s+s^2)$
5	$(1+s)(1+0.618s+s^2)(1+1.618s+s^2)$
6	$(1+0.518s+s^2)(1+1.414s+s^2)(1+1.932s+s^2)$
7	$(1+s)(1+0.445s+s^2)(1+1.247s+s^2)(1+1.802s+s^2)$
8	$(1+0.390s+s^2)(1+1.111s+s^2)(1+1.663s+s^2)(1+1.962s+s^2)$
9	$(1+s)(1+0.347s+s^2)(1+s+s^2)(1+1.532s+s^2)(1+1.879s+s^2)$
10	$(1+0.313s+s^2)(1+0.908s+s^2)(1+1.414s+s^2)(1+1.782s+s^2)(1+1.975s+s^2)$

Table14.1 Butterworth Filter Table

ANALYSIS:

Order	Gain at Stage 1 (at the end of OP-AMP 1)	Gain at Stage 2 (at the end of OP-AMP 2)	Gain at Stage 3 (at the end of OP-AMP 3)	Gain at Stage 4 (at the end of OP-AMP 4)	Gain at Stage 5 (at the end of OP-AMP 5)	Total Gain (at the end of all stages)	Minimum Offset of LM741 OP-AMP	Output voltage (Vout) in V if Vin is 1V	Output voltage (Vout) in dB if Vin is 1V	Output voltage (Vout) in log(out) if Vin is 1V
1	2	-	-	-	-	2	0.5	1	6.0205	0.6931
2	1.586	-	-	-	-	1.586	0.5	0.793	4.0060	0.4612
3	2	2	-	-	-	4	0.5	2	12.0411	1.3863
4	2.2346	1.152	-	-	-	2.5742	0.5	1.2871	8.2128	0.9455
5	2	2.2382	1.382	-	-	6.58385	0.5	3.2919	16.3695	1.8846
6	1.482	0.586	1.068	-	-	4.2041	0.5	2.10205	12.4734	1.4360
7	2	2.555	1.753	1.198	-	10.7314	0.5	5.3657	20.6131	2.3731
8	2.61	1.889	1.337	1.038	-	6.8422	0.5	3.4211	16.7039	1.9231
9	2	2.653	2	1.468	1.879	29.2718	0.5	15.6359	29.3289	3.3766
10	2.687	2.092	1.586	1.218	1.025	11.1302	0.5	5.565	20.9300	2.4097

Table14.2 Butterworth Filter Analysis Table

Explanation of the above analysis table:

Column 1: Order

The order of the Low Pass Filter is specified here.

Column 2: Gain at the end of Stage 1 (at the end of OP-AMP 1)

The coefficient of first variable 's' of the first polynomial in the Normalized Denominator Polynomials in Factored form is used to derive the gain (A_f) where the coefficient is equated to 3-A_f and the resulting gain is specified in this column.

Column 3: Gain at the end of Stage 2 (at the end of OP-AMP 2)

The coefficients of second variable 's' of the second polynomial (if present) in the Normalized Denominator Polynomials in Factored form is used to derive the gain (A_f) where the coefficient is equated to 3-A_f and the resulting gain is specified in this column.

Column 4: Gain at the end of Stage 3 (at the end of OP-AMP 3)

The coefficients of third variable 's' of the third polynomial (if present) in the Normalized Denominator Polynomials in Factored form is used to derive the gain (A_f) where the coefficient is equated to 3-A_f and the resulting gain is specified in this column.

Column 5: Gain at the end of Stage 4 (at the end of OP-AMP 4)

The coefficients of fourth variable 's' of the fourth polynomial (if present) in the Normalized Denominator Polynomials in Factored form is used to derive the gain (A_f) where the coefficient is equated to 3-A_f and the resulting gain is specified in this column.

Column 6: Gain at the end of Stage 5 (at the end of OP-AMP 5)

The coefficients of fifth variable 's' of the fifth polynomial (if present) in the Normalized Denominator Polynomials in Factored form is used to derive the gain (A_f) where the coefficient is equated to 3-A_f and the resulting gain is specified in this column.

Column 7: Total Gain (at the end of all stages)

The total gain is the product of all the gains in different stages.

Column 8: Minimum Offset of LM741 OP-AMP

The offset of the opamp used is 0.5 or -6dB of attenuation where the resulting output voltage at the cut off frequency is observed.

Column 9: Output voltage (Vout) in V

The output voltage is calculated as the product of the Total gain (Column 7) and the Minimum offset of LM741 OP-AMP (Column 8). If Vin is 1V, then 1 is multiplied to the product; if Vin is 2V, then 2 is multiplied to the product and so on.

Column 10: Output voltage (Vout) in dB

The output voltage in dB is calculated using the formula $Vout(dB)=20*\log_{10}(Vout(V))$ where the Vout(V) is replaced by the product of Total gain (Column7) and Vin as specified in Column 9.

Column 11: Output voltage (Vout) in log(out)

The output voltage in log is calculated using the formula $Vout=\log_e(Vout(V))$ where the Vout(V) is replaced by the product of Total gain (Column7) and Vin as specified in Column 9.

Use the above analysis table 14.2 to compare the output waveforms of the filters implemented in the following pages.

14.1 FIRST ORDER BUTTERWORTH LOW PASS FILTER:

CIRCUIT DIAGRAM:

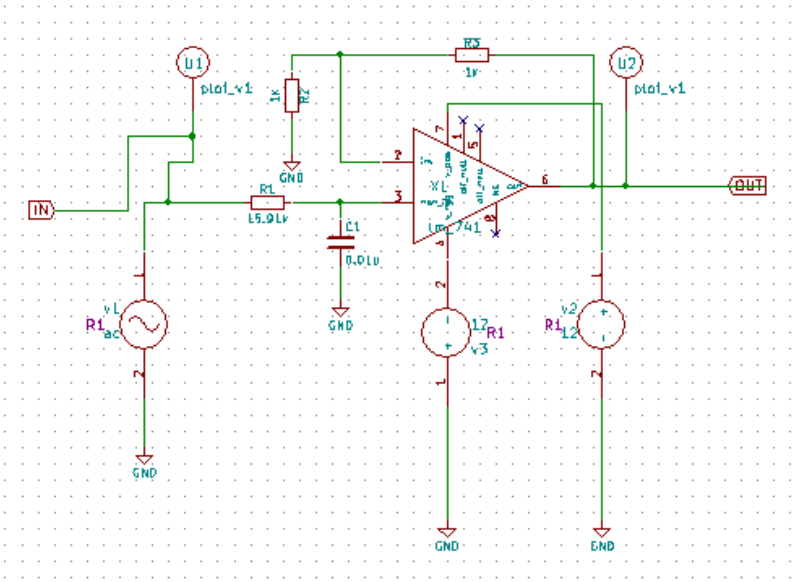

Figure14.1.1 Circuit Diagram

INPUT AND OUTPUT WAVEFORM:

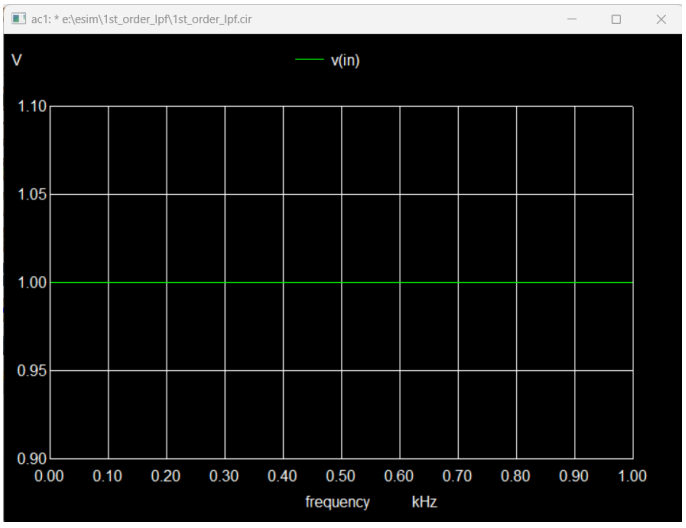

Figure14.1.2 Input waveform

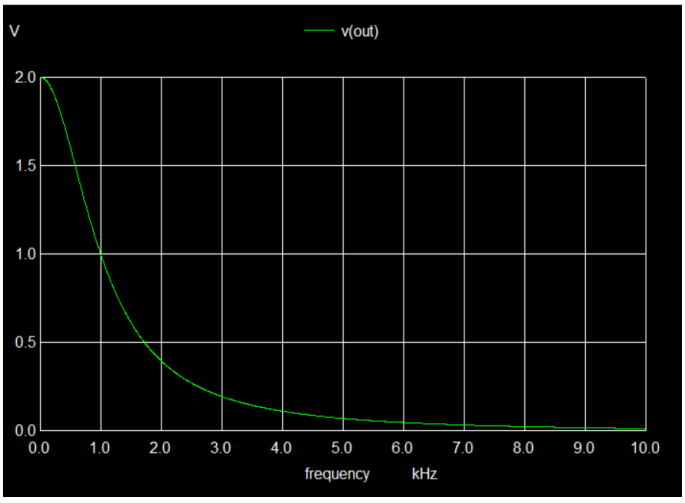

Figure14.1.3 Output waveform

14.2 SECOND ORDER BUTTERWORTH LOW PASS FILTER:

CIRCUIT DIAGRAM:

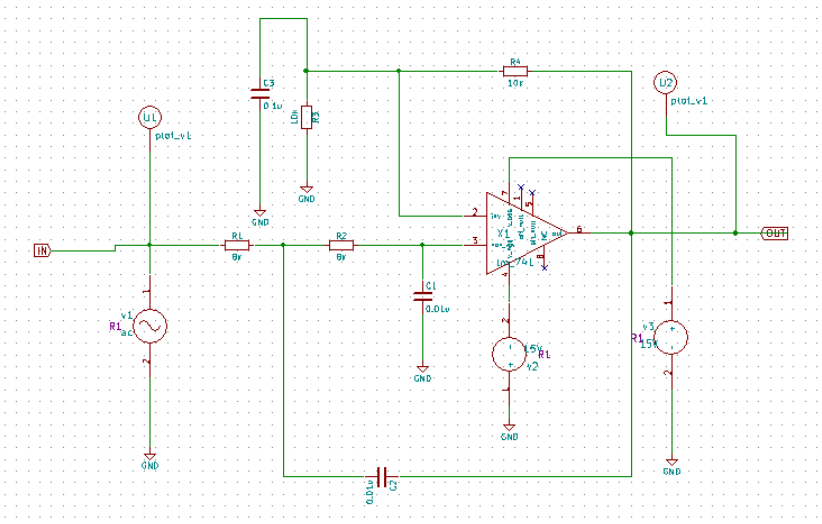

Figure14.2.1 Circuit Diagram

INPUT AND OUTPUT WAVEFORM:

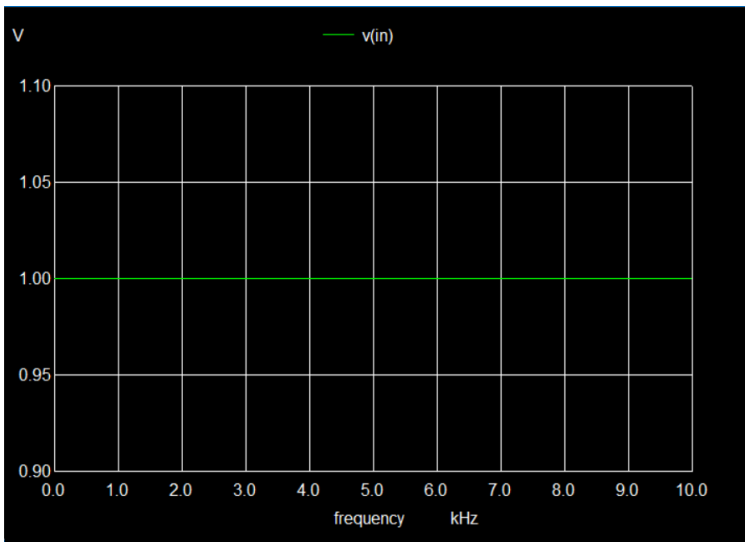

Figure14.2.2 Input waveform

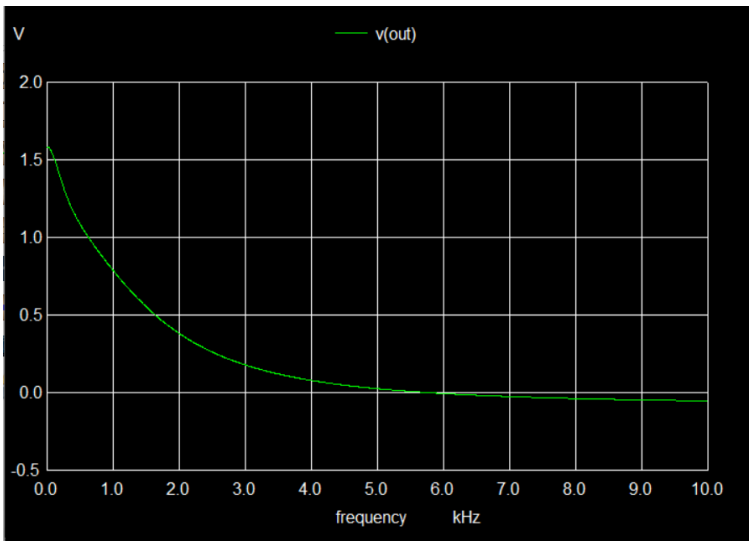

Figure14.2.3 Output waveform

14.3 THIRD ORDER BUTTERWORTH LOW PASS FILTER:

CIRCUIT DIAGRAM:

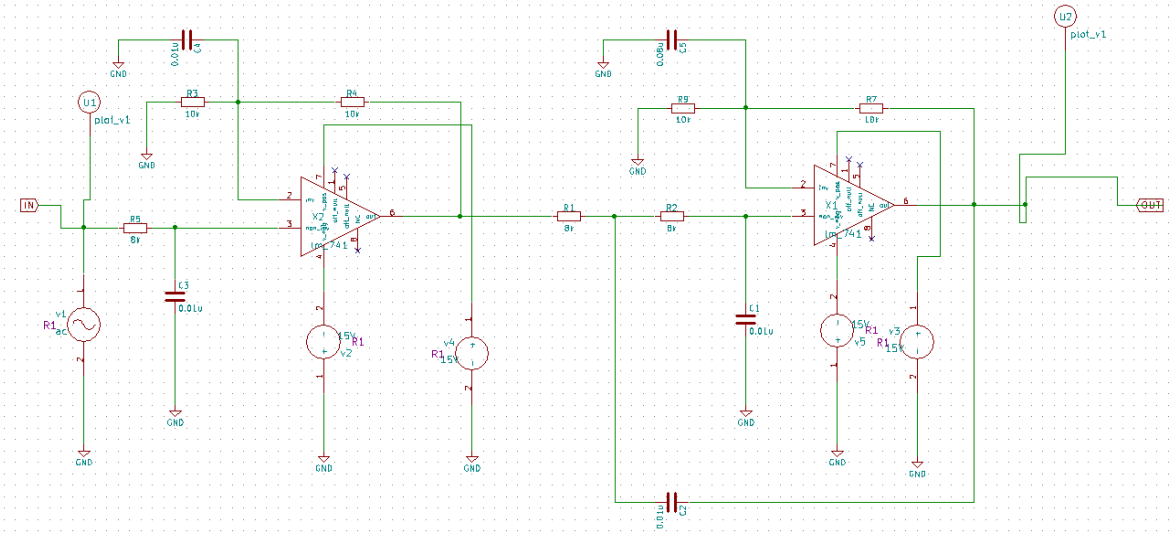

Figure14.3.1 Circuit Diagram

INPUT AND OUTPUT WAVEFORM:

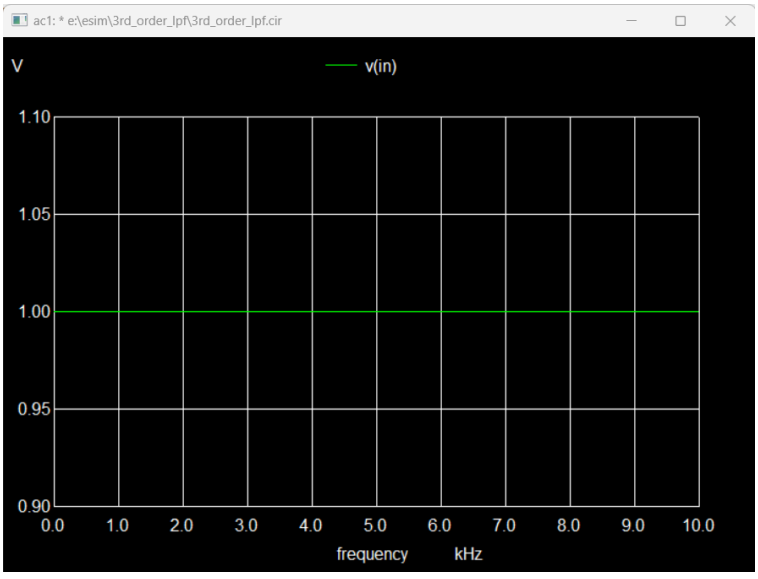

Figure14.3.2 Input waveform

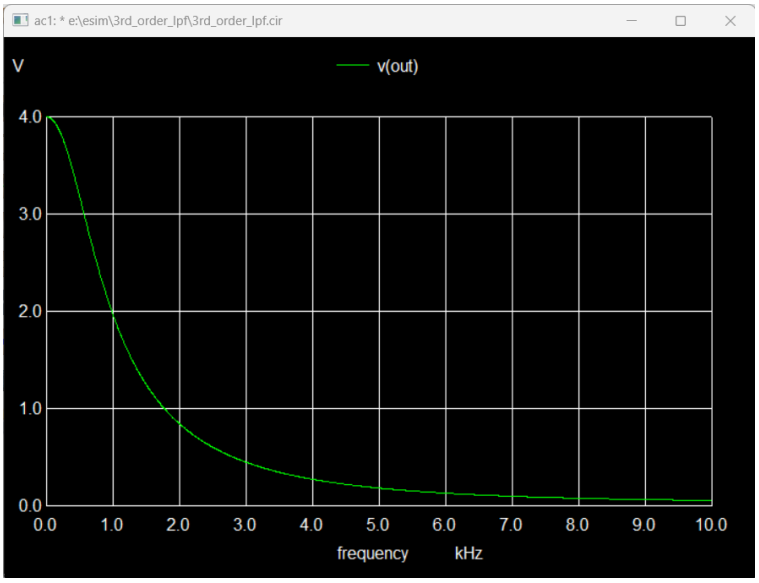

Figure14.3.3 Output waveform

14.4 FOURTH ORDER BUTTERWORTH LOW PASS FILTER:

CIRCUIT DIAGRAM:

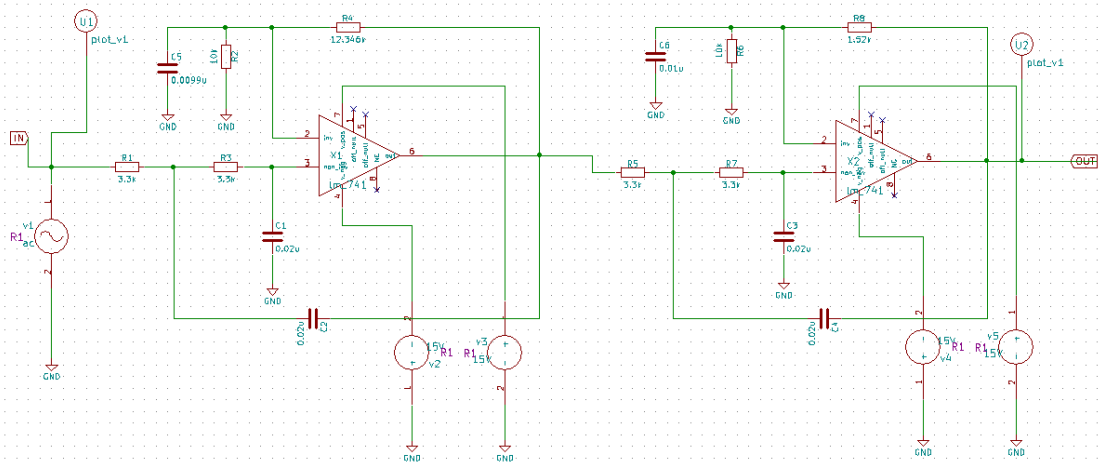

Figure14.4.1 Circuit Diagram

INPUT AND OUTPUT WAVEFORM:

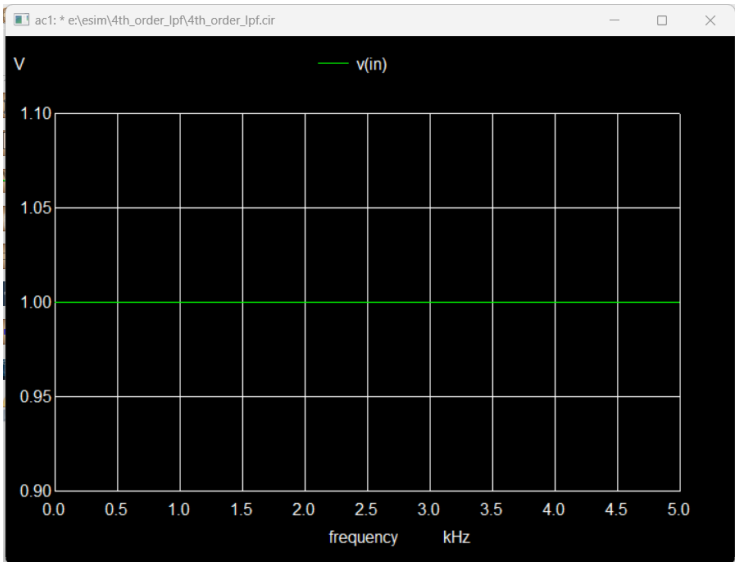

Figure14.4.2 Input waveform

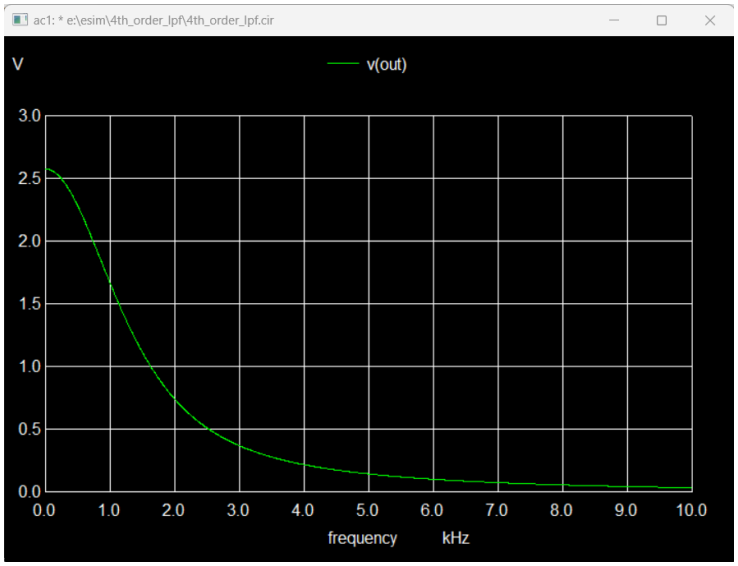

Figure14.4.3 Output waveform

14.5 FIFTH ORDER BUTTERWORTH LOW PASS FILTER:

CIRCUIT DIAGRAM:

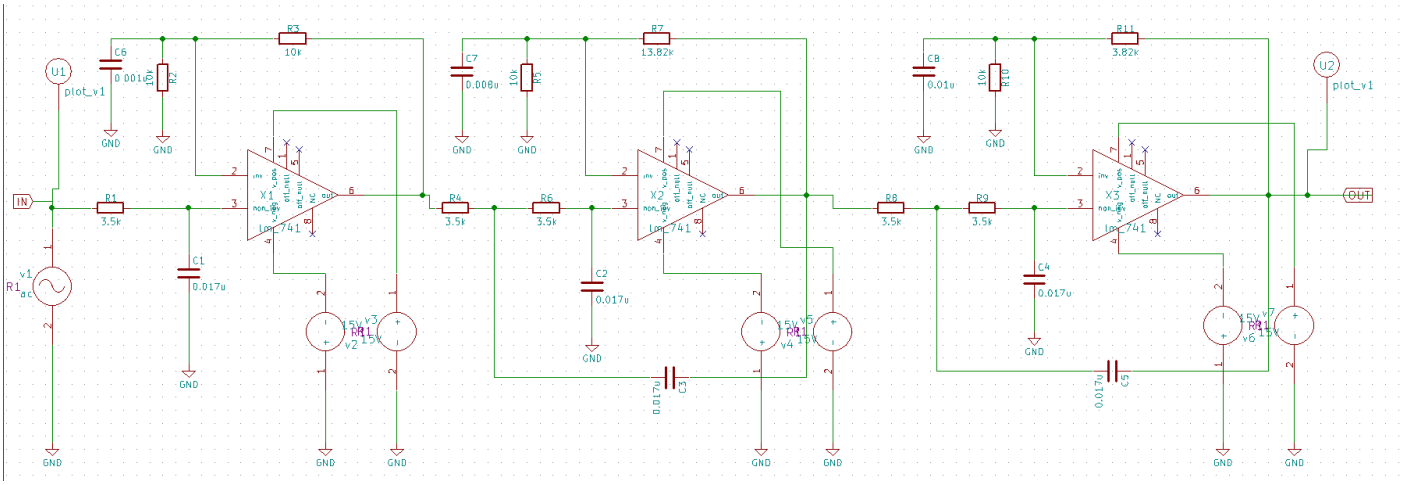

Figure14.5.1 Circuit Diagram

INPUT AND OUTPUT WAVEFORM:

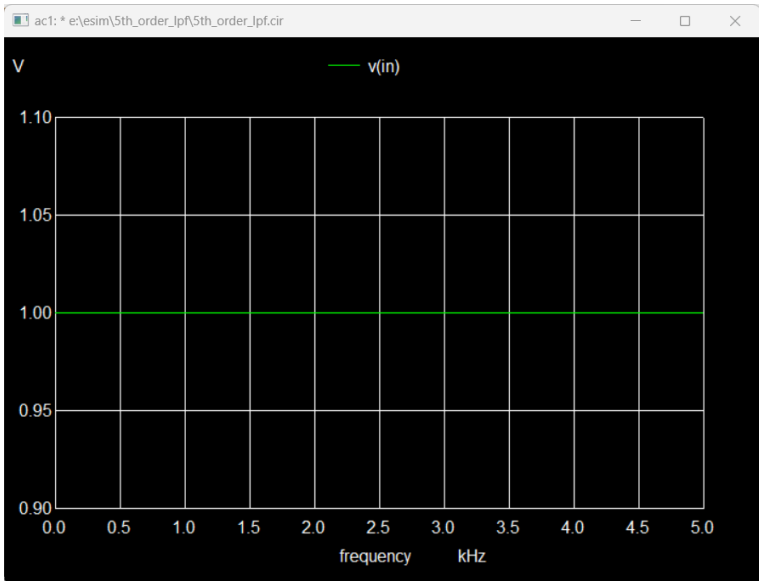

Figure14.5.2 Input waveform

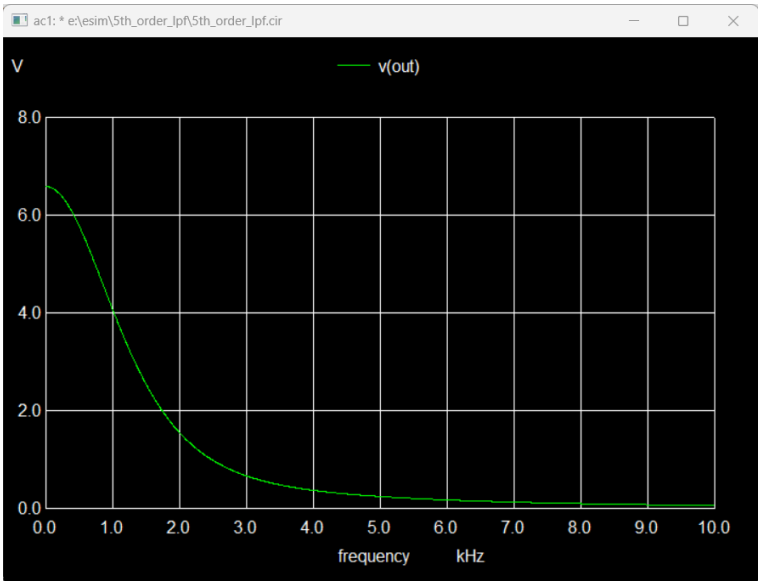

Figure14.2.3 Output waveform

14.6 SIXTH ORDER BUTTERWORTH LOW PASS FILTER

CIRCUIT DIAGRAM:

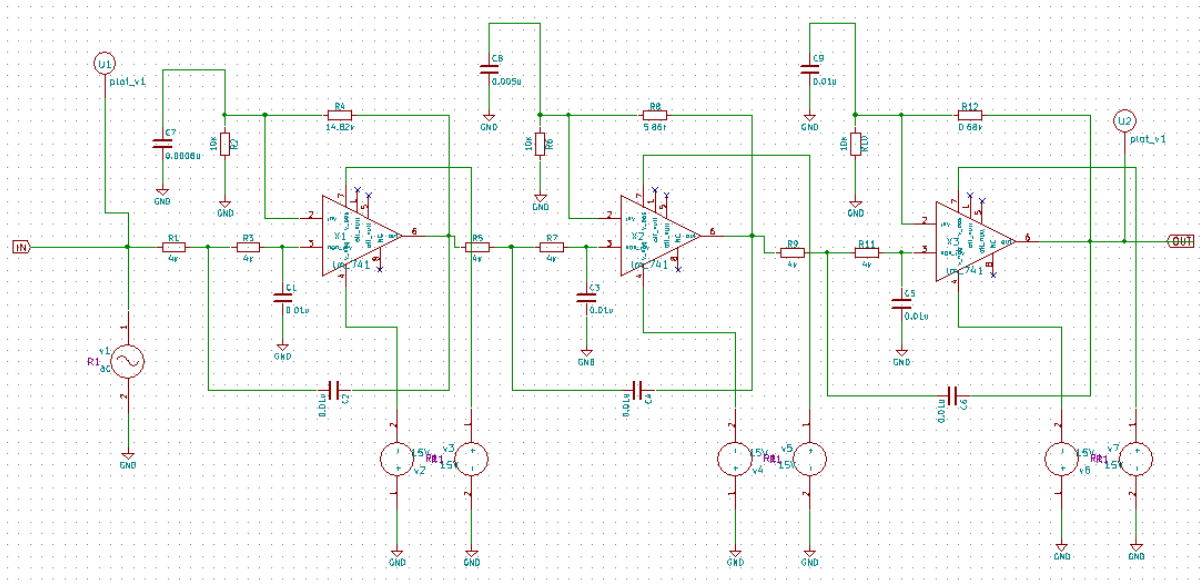

Figure14.6.1 Circuit Diagram

INPUT AND OUTPUT WAVEFORM:

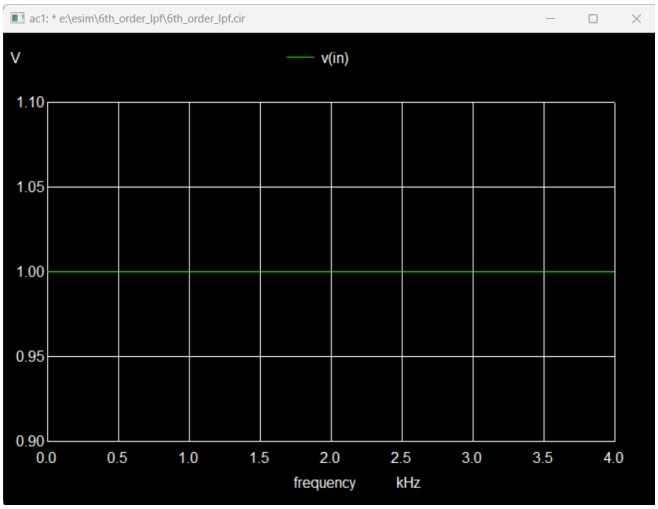

Figure14.6.2 Input waveform

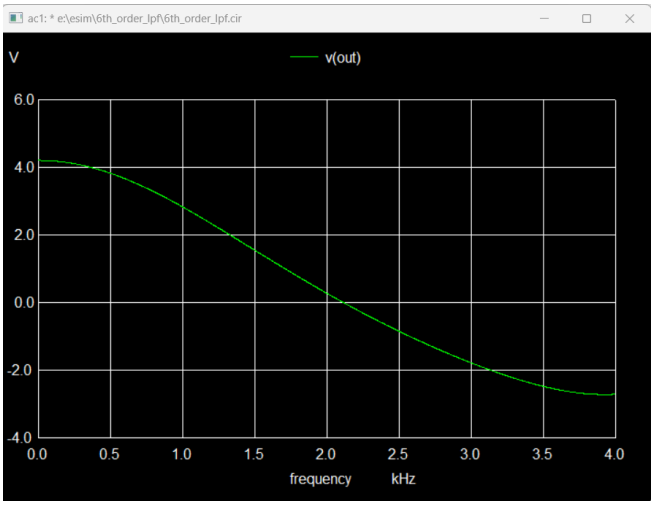

Figure14.6.3 Output waveform

14.7 SEVENTH ORDER BUTTERWORTH LOW PASS FILTER

CIRCUIT DIAGRAM:

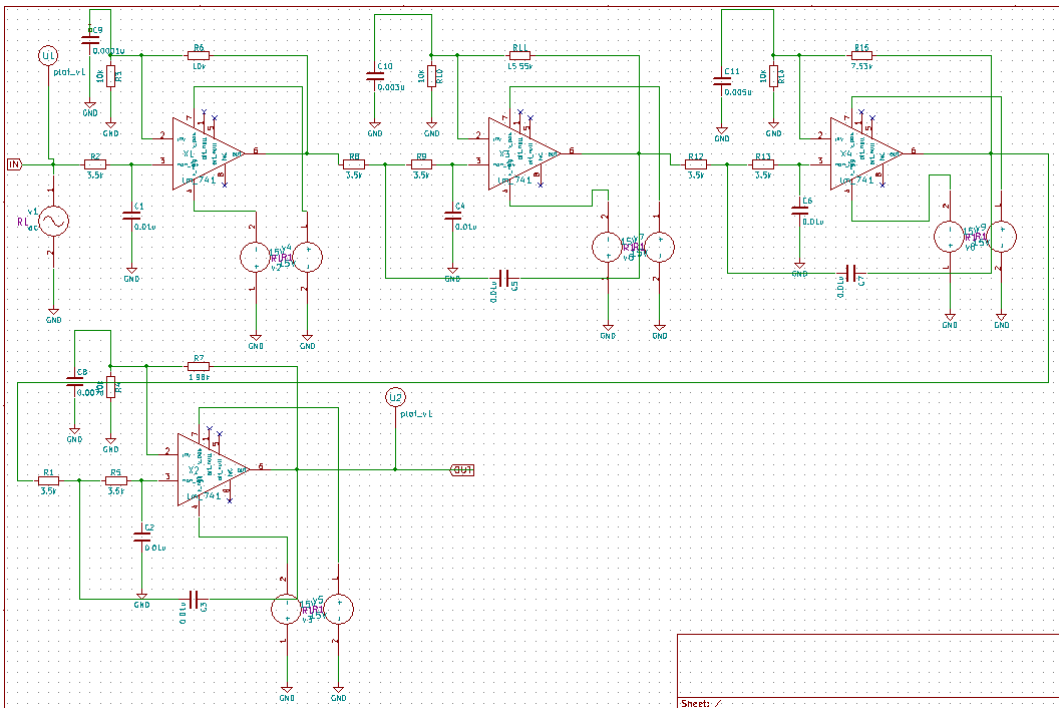

Figure14.7.1 Circuit Diagram

INPUT AND OUTPUT WAVEFORM:

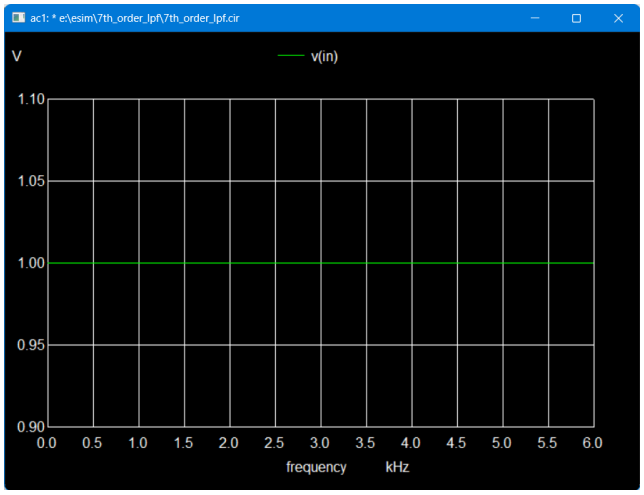

Figure14.7.2 Input waveform

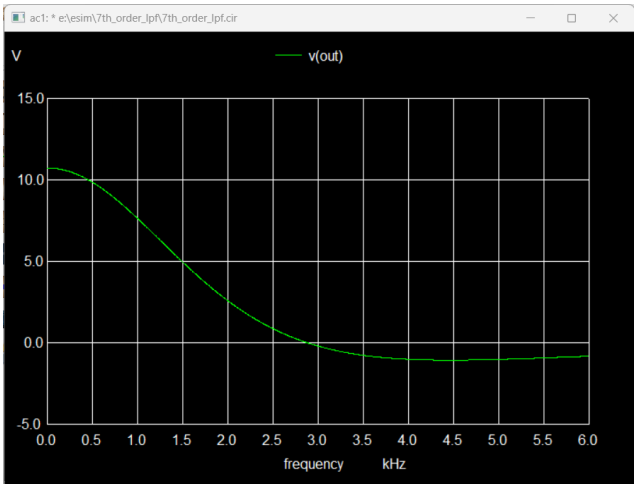

Figure14.7.3 Output waveform

14.8 EIGHTH ORDER BUTTERWORTH LOW PASS FILTER

CIRCUIT DIAGRAM:

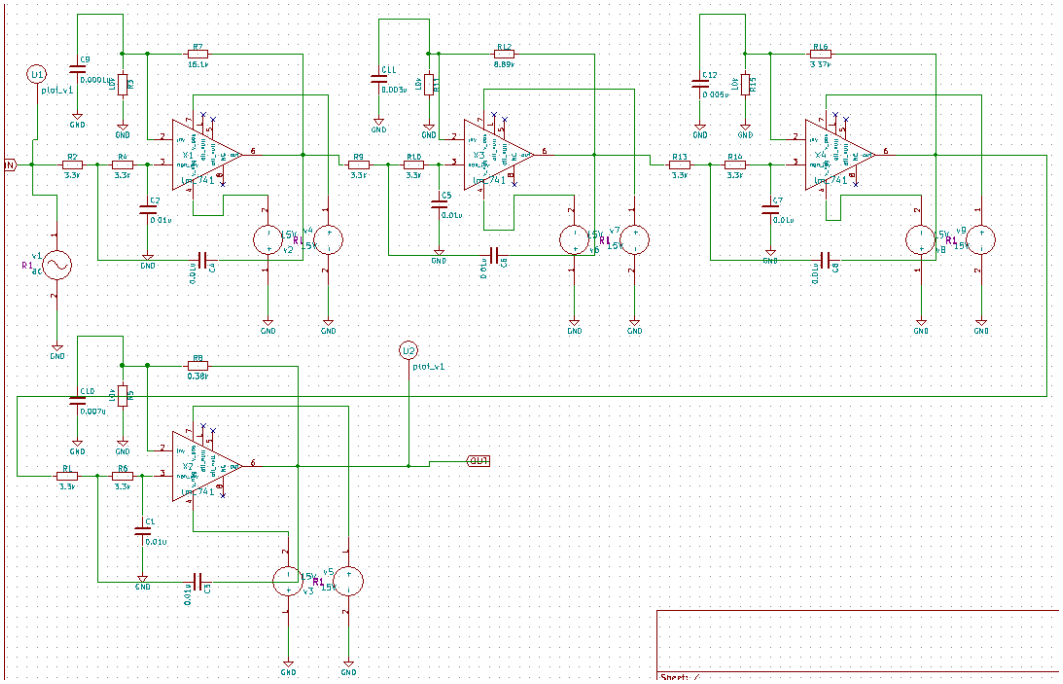

Figure14.8.1 Circuit Diagram

INPUT AND OUTPUT WAVEFORM:

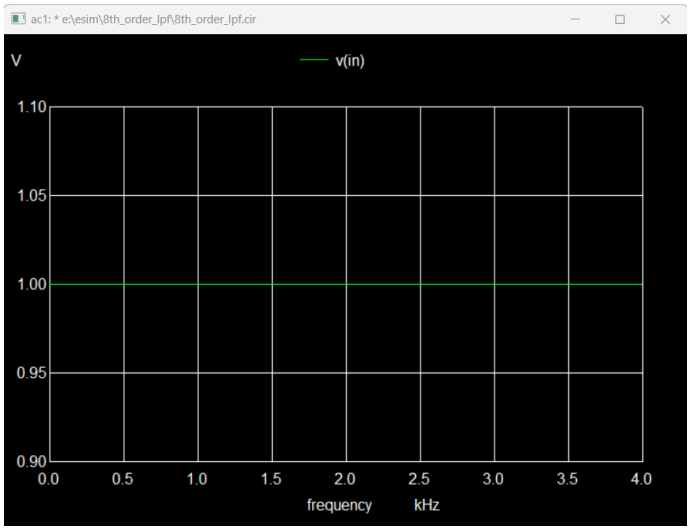

Figure14.8.2 Input waveform

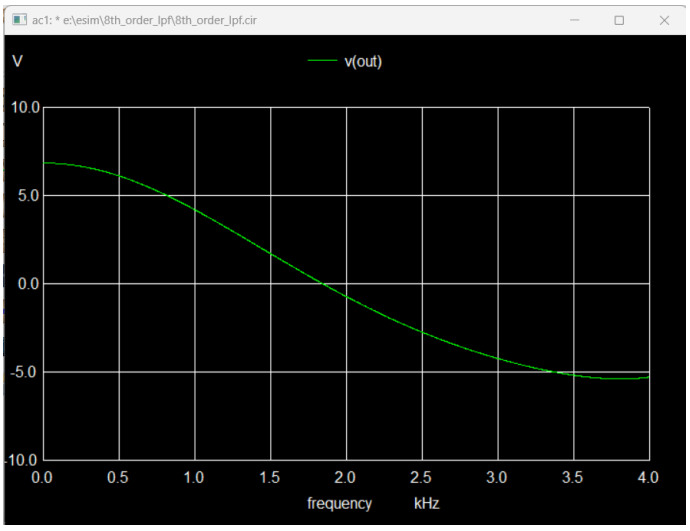

Figure14.8.3 Output waveform

14.9 NINETH ORDER BUTTERWORTH LOW PASS FILTER

CIRCUIT DIAGRAM:

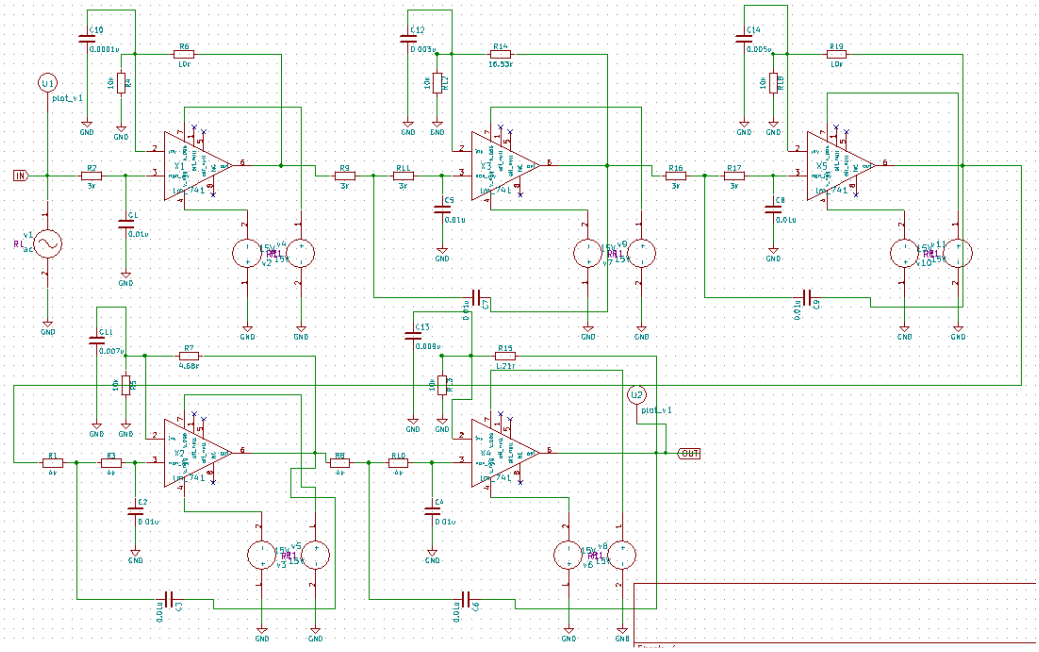

Figure14.9.1 Circuit Diagram

INPUT AND OUTPUT WAVEFORM:

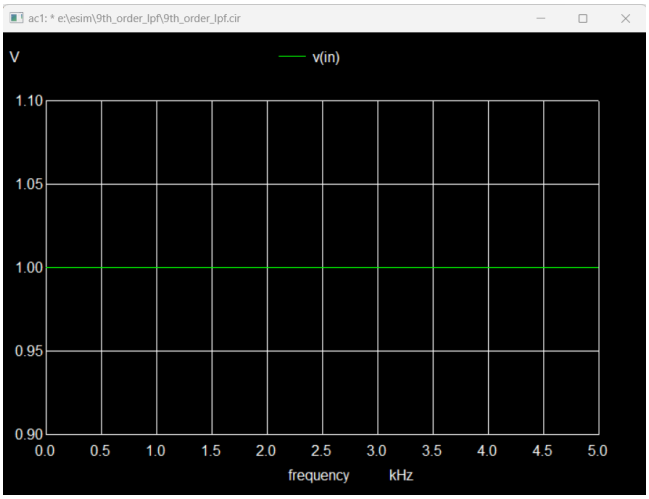

Figure14.9.2 Input waveform

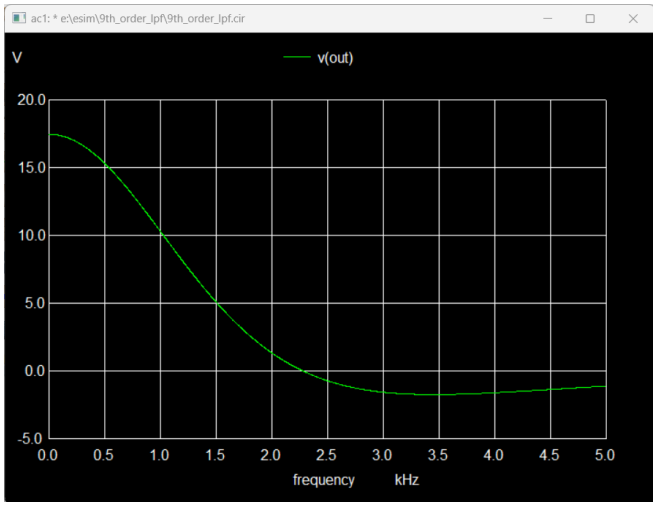

Figure14.9.3 Output waveform

14.10 TENTH ORDER BUTTERWORTH LOW PASS FILTER

CIRCUIT DIAGRAM:

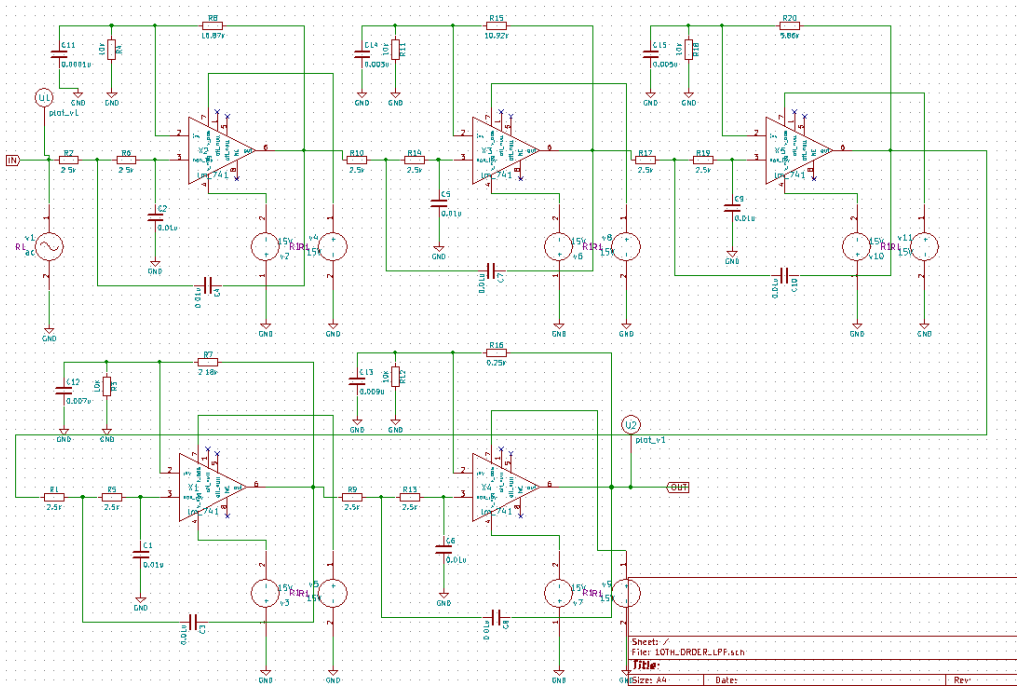

Figure14.10.1 Circuit Diagram

INPUT AND OUTPUT WAVEFORM:

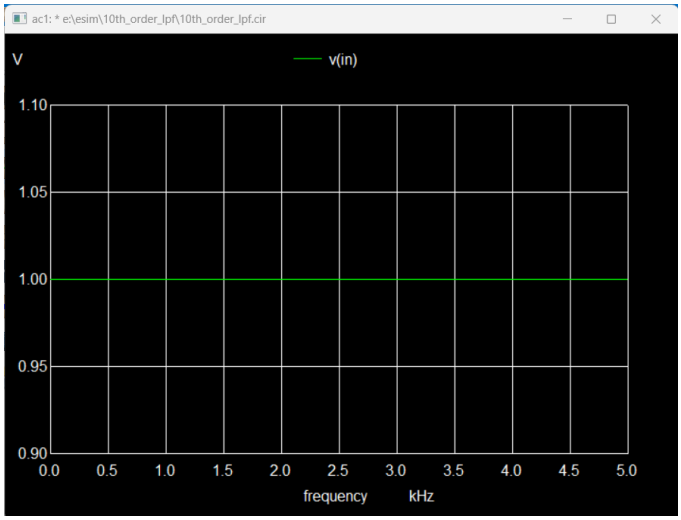

Figure14.10.2 Input waveform

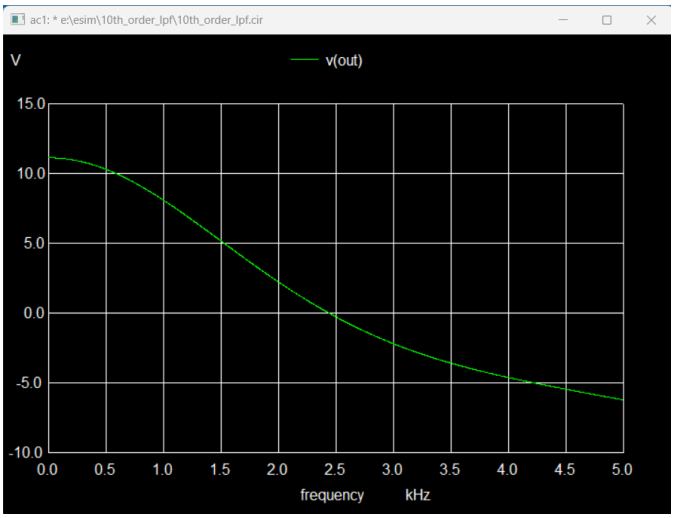

Figure14.10.3 Output waveform

15. DESIGN OF BESSEL LOW PASS FILTERS FROM 1ST ORDER TO 10TH ORDER

BESSEL FILTER TABLE

Order(n)	Normalized Denominator Polynomials in Factored form
1	$1+s$
2	$1+1.414s+s^2$
3	$(1+s)(1+s+s^2)$
4	$(1+0.765s+s^2)(1+1.848s+s^2)$
5	$(1+s)(1+0.618s+s^2)(1+1.618s+s^2)$
6	$(1+0.518s+s^2)(1+1.414s+s^2)(1+1.932s+s^2)$
7	$(1+s)(1+0.445s+s^2)(1+1.247s+s^2)(1+1.802s+s^2)$
8	$(1+0.390s+s^2)(1+1.111s+s^2)(1+1.663s+s^2)(1+1.962s+s^2)$
9	$(1+s)(1+0.347s+s^2)(1+s+s^2)(1+1.532s+s^2)(1+1.879s+s^2)$
10	$(1+0.313s+s^2)(1+0.908s+s^2)(1+1.414s+s^2)(1+1.782s+s^2)(1+1.975s+s^2)$

Table15.1 Bessel Filter Table

ANALYSIS:

Order	Gain at Stage 1 (at the end of OP-AMP 1)	Gain at Stage 2 (at the end of OP-AMP 2)	Gain at Stage 3 (at the end of OP-AMP 3)	Gain at Stage 4 (at the end of OP-AMP 4)	Gain at Stage 5 (at the end of OP-AMP 5)	Total Gain (at the end of all stages)	Minimum Offset of LM741 OP-AMP	Output voltage (Vout) in V if Vin is 1V	Output voltage (Vout) in dB if Vin is 1V	Output voltage (Vout) in log(out) if Vin is 1V
1	2	-	-	-	-	2	0.5	1	6.0205	0.6931
2	1.2678	-	-	-	-	1.2678	0.5	0.6339	2.0610	0.2372
3	2	1.5592	-	-	-	3.1058	0.5	1.5592	9.8434	1.1332
4	1.7586	1.084	-	-	-	1.9063	0.5	0.95315	5.6038	0.6451
5	2	1.9089	1.2254	-	-	4.6783	0.5	2.6819	14.4017	1.5429
6	2.0229	1.3639	1.0404	-	-	2.8704	0.5	1.4352	9.1588	1.0544
7	2	2.1121	1.4867	1.1218	-	7.0450	0.5	3.5225	16.9576	1.9523
8	1.2131	1.5934	2.1843	1.038	-	4.3226	0.5	2.1613	12.7149	1.4638
9	2	2.2436	1.6853	1.3034	1.0759	10.6047	0.5	5.3023	20.5099	2.3613
10	2.2933	1.7655	1.3871	1.1413	1.0159	6.5116	0.5	3.2558	16.2737	1.8735

Table15.2 Bessel Filter Analysis Table

Explanation of the above analysis table:

Column 1: Order

The order of the Low Pass Filter is specified here.

Column 2: Gain at the end of Stage 1 (at the end of OP-AMP 1)

The coefficient of first variable 's' of the first polynomial in the Normalized Denominator Polynomials in Factored form is used to derive the gain (A_f) where the coefficient is equated to 3-A_f and the resulting gain is specified in this column.

Column 3: Gain at the end of Stage 2 (at the end of OP-AMP 2)

The coefficients of second variable 's' of the second polynomial (if present) in the Normalized Denominator Polynomials in Factored form is used to derive the gain (A_f) where the coefficient is equated to 3-A_f and the resulting gain is specified in this column.

Column 4: Gain at the end of Stage 3 (at the end of OP-AMP 3)

The coefficients of third variable 's' of the third polynomial (if present) in the Normalized Denominator Polynomials in Factored form is used to derive the gain (A_f) where the coefficient is equated to 3-A_f and the resulting gain is specified in this column.

Column 5: Gain at the end of Stage 4 (at the end of OP-AMP 4)

The coefficients of fourth variable 's' of the fourth polynomial (if present) in the Normalized Denominator Polynomials in Factored form is used to derive the gain (A_f) where the coefficient is equated to 3-A_f and the resulting gain is specified in this column.

Column 6: Gain at the end of Stage 5 (at the end of OP-AMP 5)

The coefficients of fifth variable 's' of the fifth polynomial (if present) in the Normalized Denominator Polynomials in Factored form is used to derive the gain (A_f) where the coefficient is equated to 3-A_f and the resulting gain is specified in this column.

Column 7: Total Gain (at the end of all stages)

The total gain is the product of all the gains in different stages.

Column 8: Minimum Offset of LM741 OP-AMP

The offset of the opamp used is 0.5 or -6dB of attenuation where the resulting output voltage at the cut off frequency is observed.

Column 9: Output voltage (Vout) in V

The output voltage is calculated as the product of the Total gain (Column 7) and the Minimum offset of LM741 OP-AMP (Column 8). If Vin is 1V, then 1 is multiplied to the product; if Vin is 2V, then 2 is multiplied to the product and so on.

Column 10: Output voltage (Vout) in dB

The output voltage in dB is calculated using the formula $Vout(dB)=20*\log_{10}(Vout(V))$ where the Vout(V) is replaced by the product of Total gain (Column7) and Vin as specified in Column 9.

Column 11: Output voltage (Vout) in log(out)

The output voltage in log is calculated using the formula $Vout=\log_e(Vout(V))$ where the Vout(V) is replaced by the product of Total gain (Column7) and Vin as specified in Column 9.

Use the above analysis table 15.2 to compare the output waveforms of the filters implemented in the following pages.

15.1 FIRST ORDER BESSEL LOW PASS FILTER

CIRCUIT DIAGRAM:

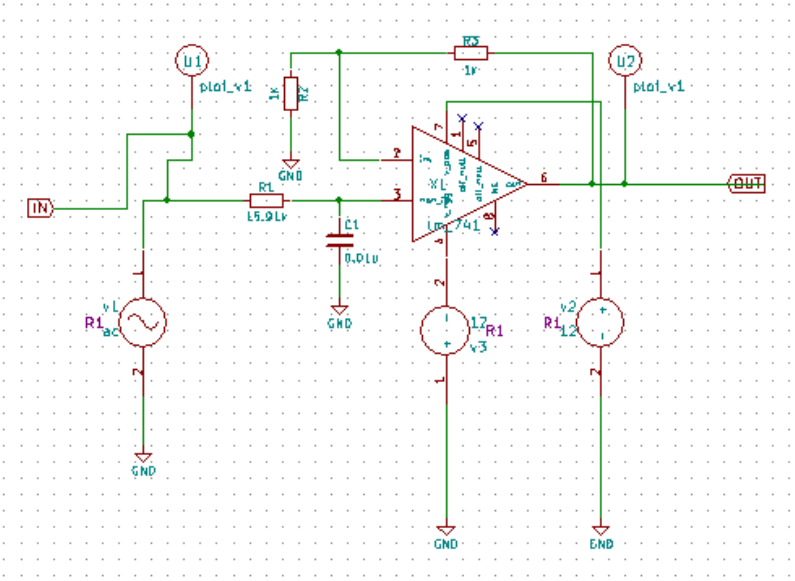

Figure15.1.1 Circuit Diagram

INPUT AND OUTPUT WAVEFORM:

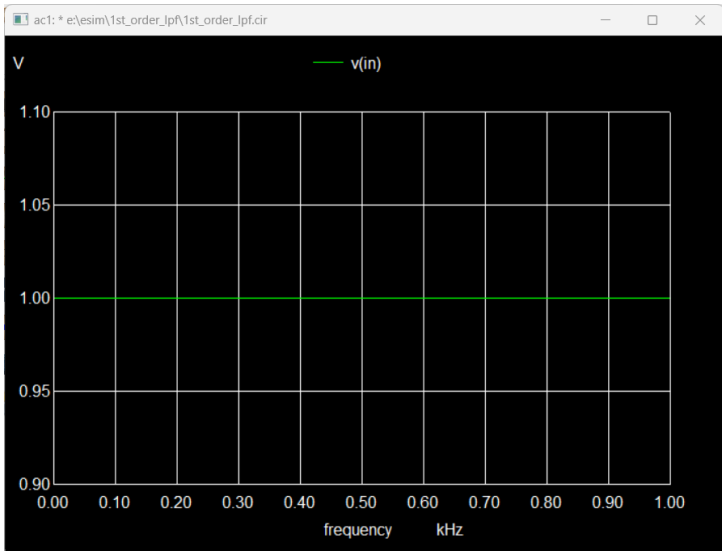

Figure15.1.2 Input waveform

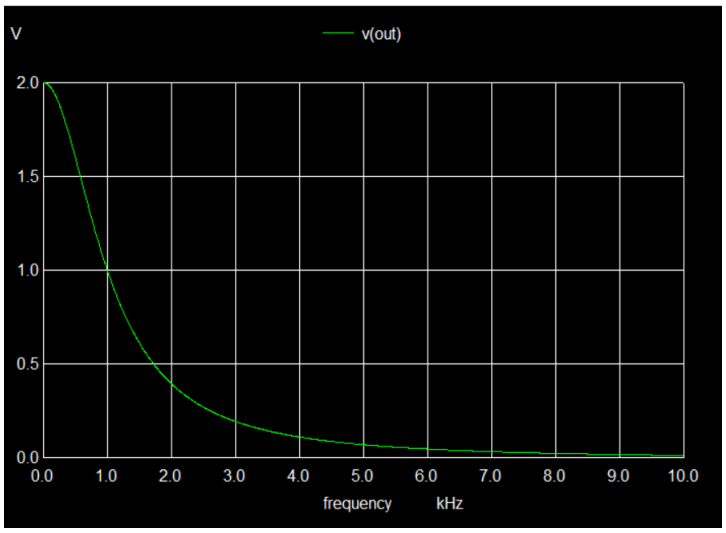

Figure15.1.3 Output waveform

15.2 SECOND ORDER BESSEL LOW PASS FILTER

CIRCUIT DIAGRAM:

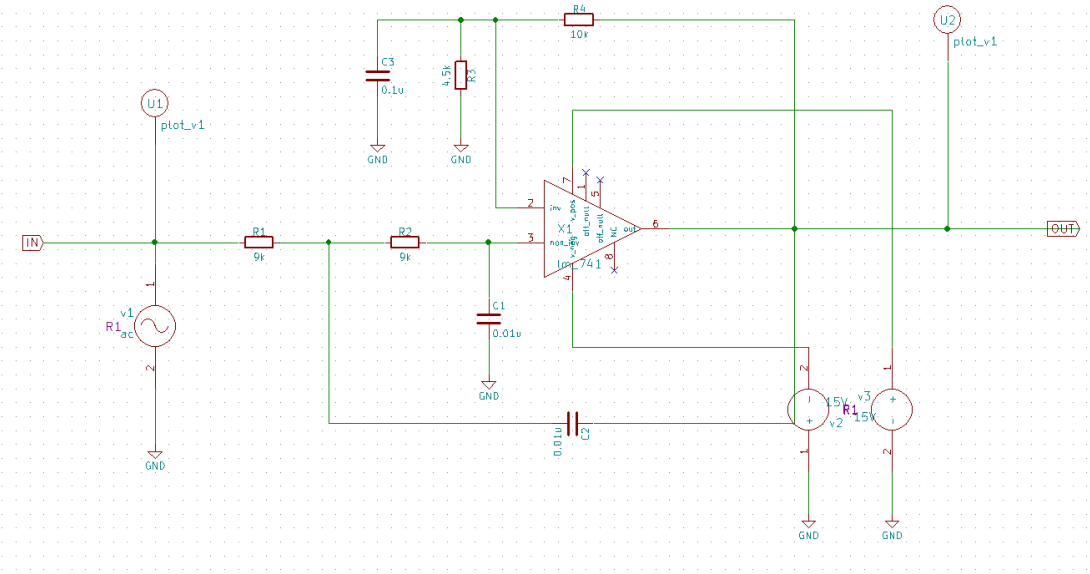

Figure15.2.1 Circuit Diagram

INPUT AND OUTPUT WAVEFORM:

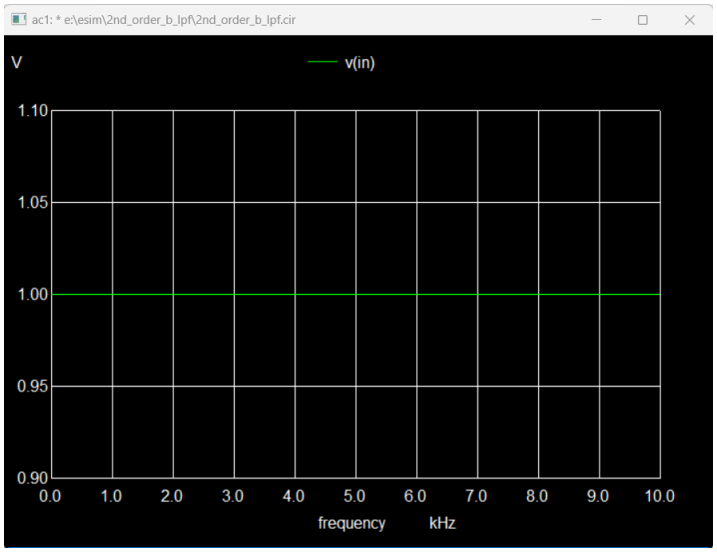

Figure15.2.2 Input waveform

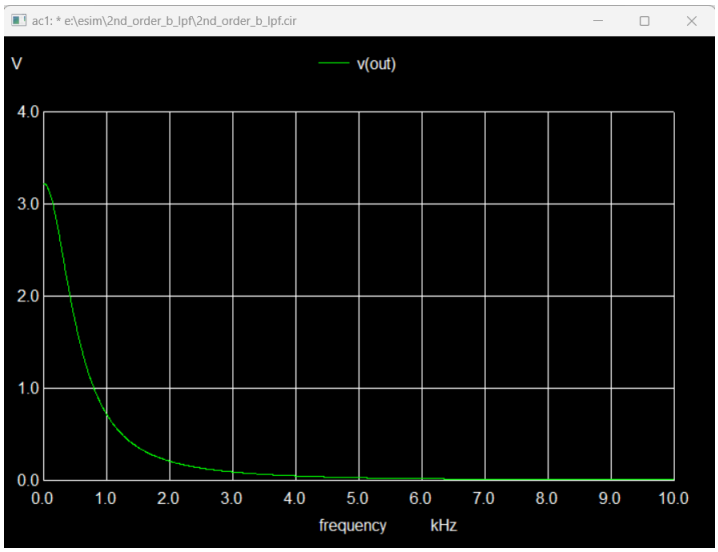

Figure15.2.3 Output waveform

15.3 THIRD ORDER BESSEL LOW PASS FILTER

CIRCUIT DIAGRAM:

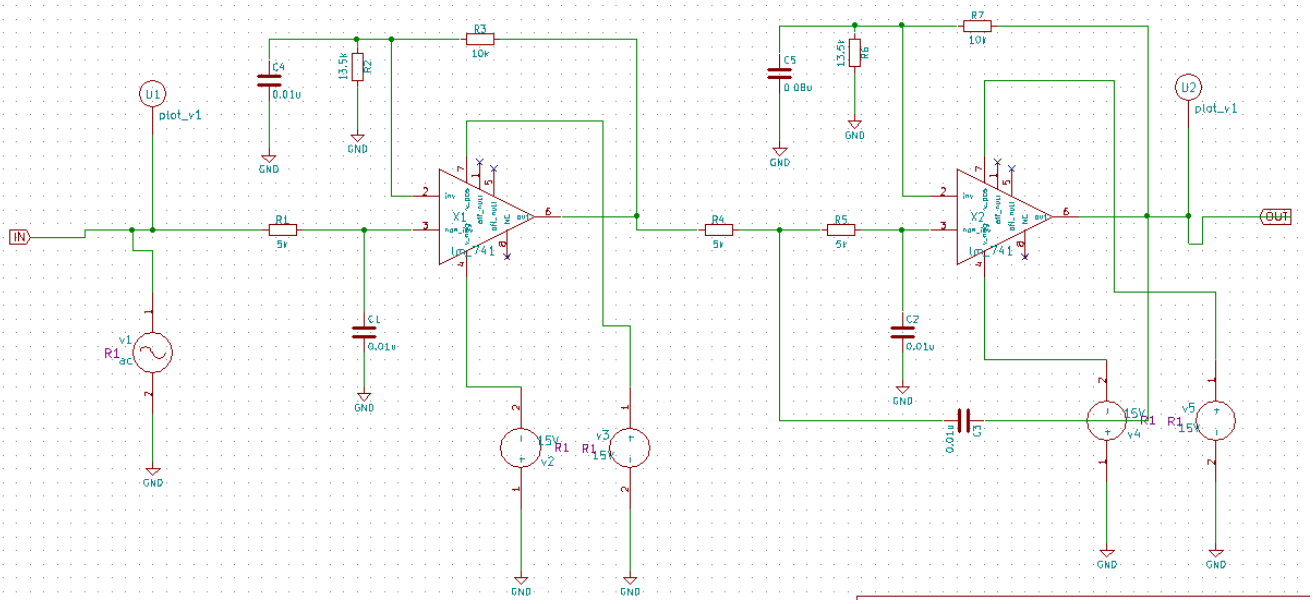

Figure15.3.1 Circuit Diagram

INPUT AND OUTPUT WAVEFORM:

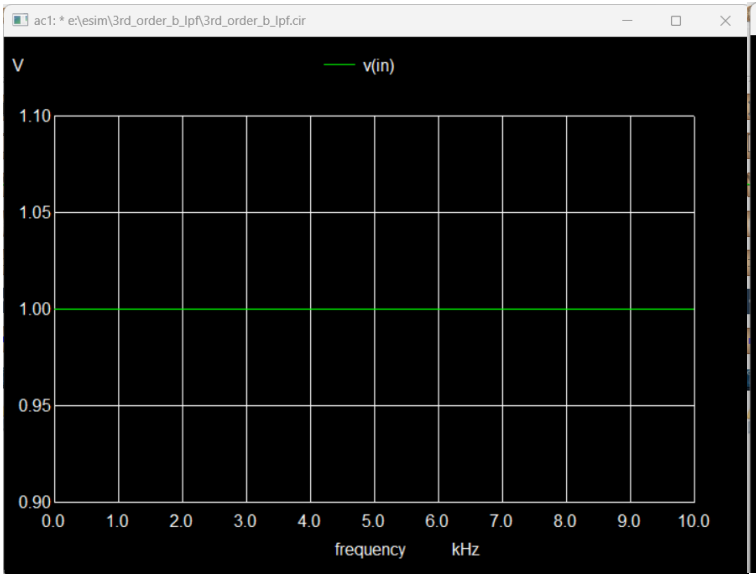

Figure15.3.2 Input waveform

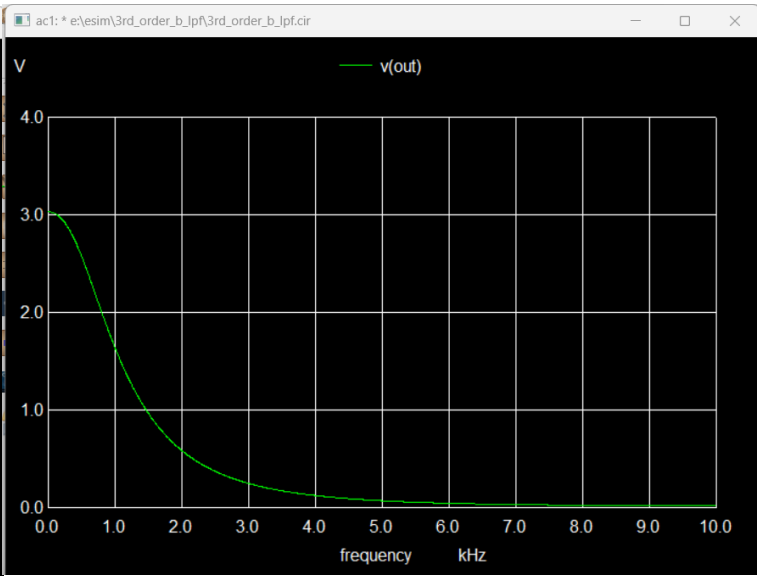

Figure15.3.3 Output waveform

15.4 FOURTH ORDER BESSEL LOW PASS FILTER

CIRCUIT DIAGRAM:

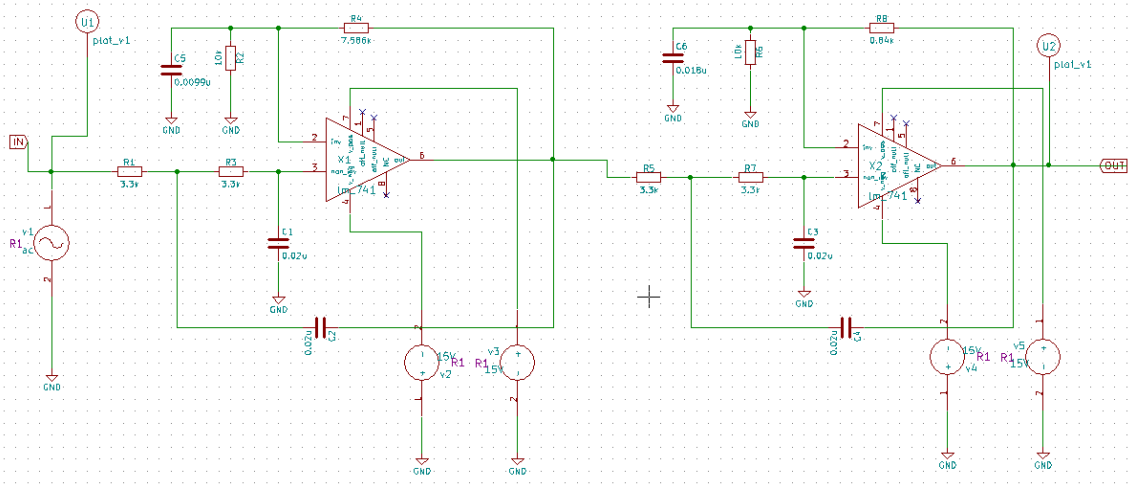

Figure15.4.1 Circuit Diagram

INPUT AND OUTPUT WAVEFORM:

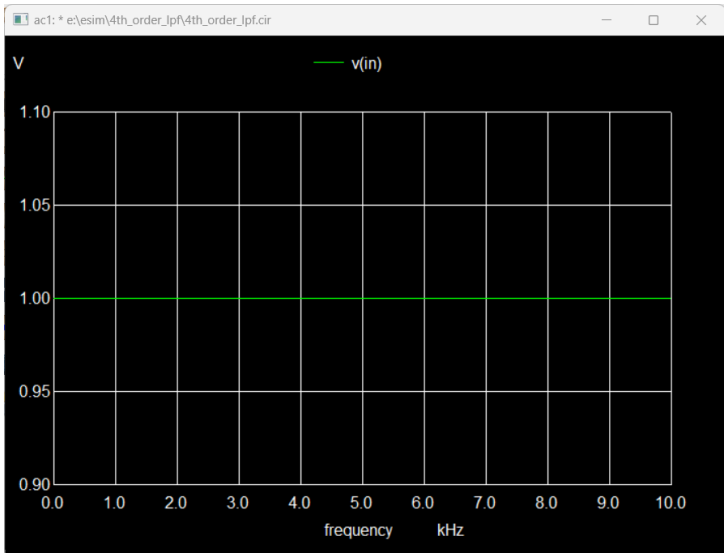

Figure15.4.2 Input waveform

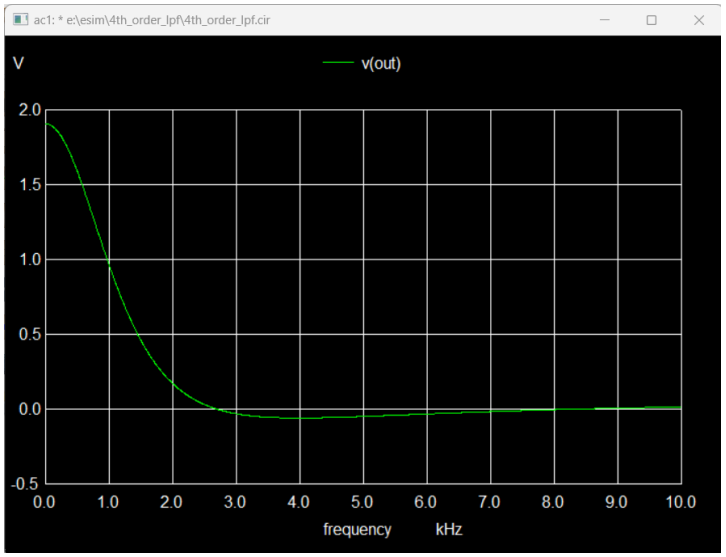

Figure15.4.3 Output waveform

15.5 FIFTH ORDER BESSEL LOW PASS FILTER

CIRCUIT DIAGRAM:

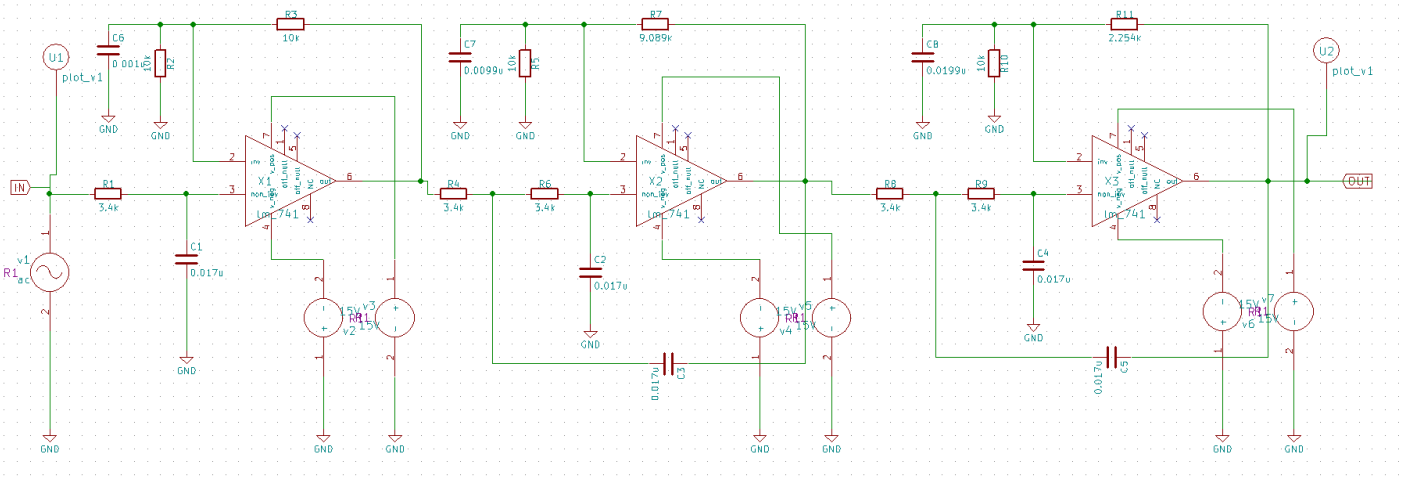

Figure15.5.1 Circuit Diagram

INPUT AND OUTPUT WAVEFORM:

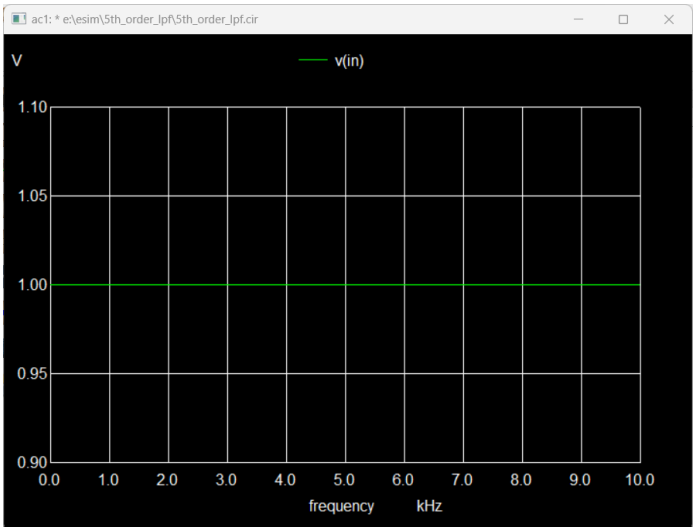

Figure15.5.2 Input waveform

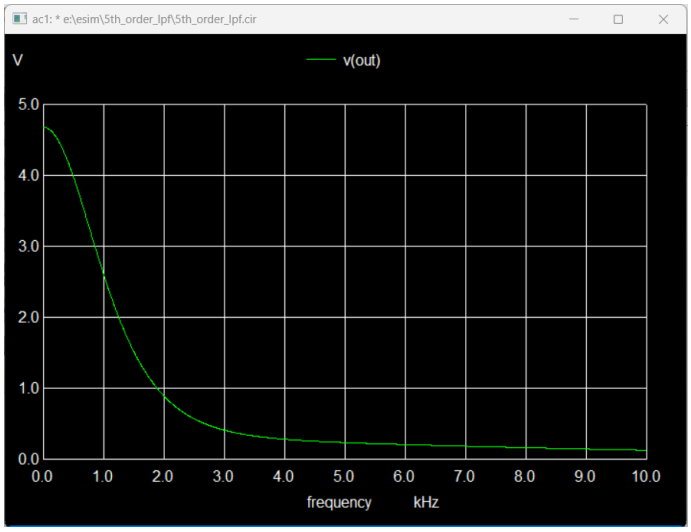

Figure15.5.3 Output waveform

15.6 SIXTH ORDER BESSEL LOW PASS FILTER

CIRCUIT DIAGRAM:

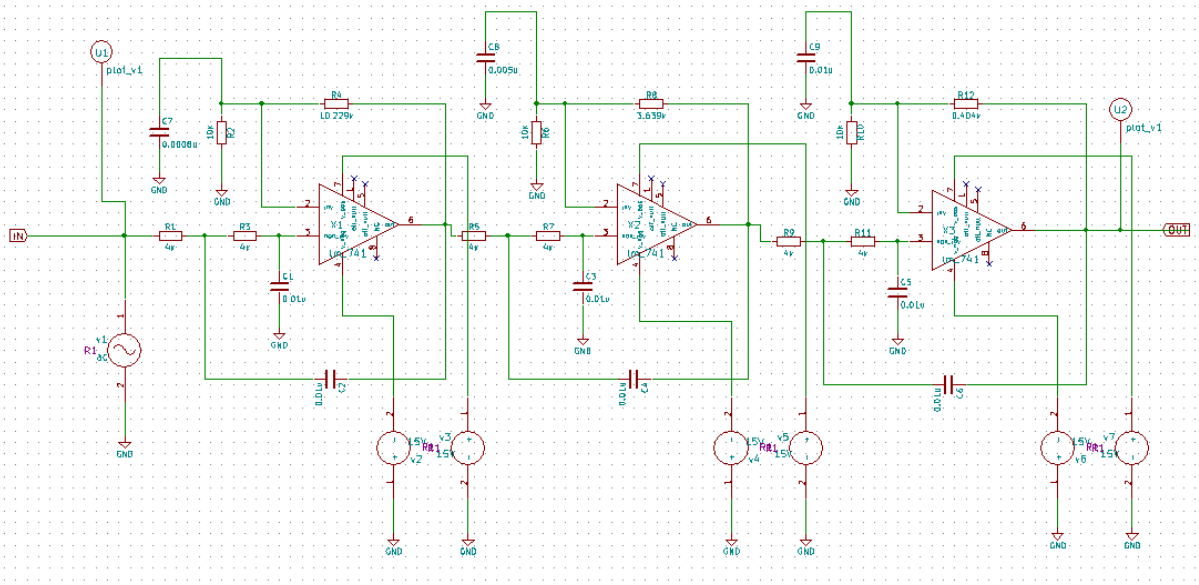

Figure15.6.1 Circuit Diagram

INPUT AND OUTPUT WAVEFORM:

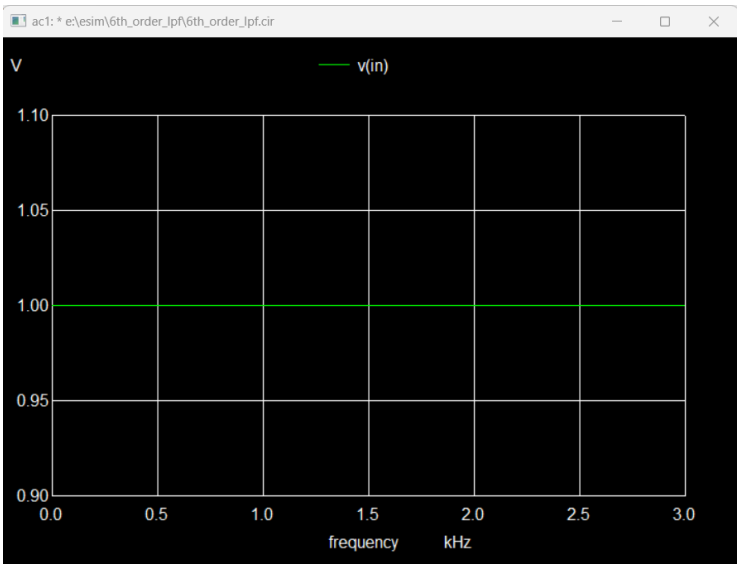

Figure15.6.2 Input waveform

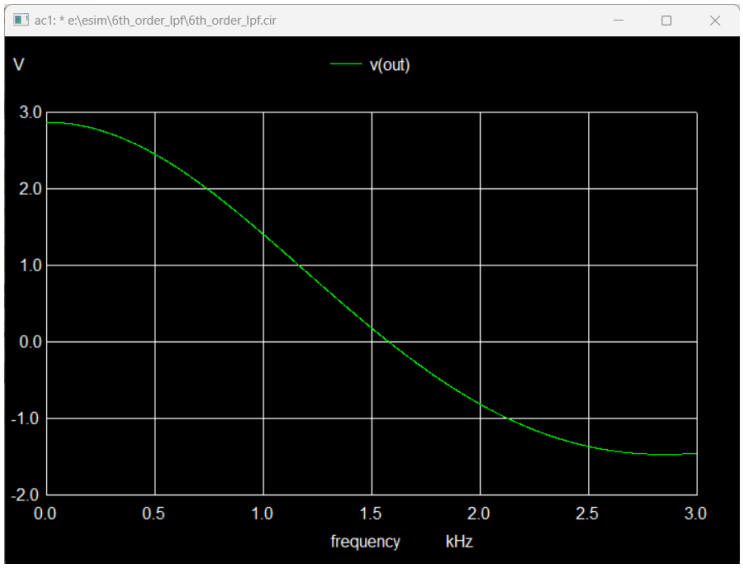

Figure15.6.3 Output waveform

15.7 SEVENTH ORDER BESSEL LOW PASS FILTER

CIRCUIT DIAGRAM:

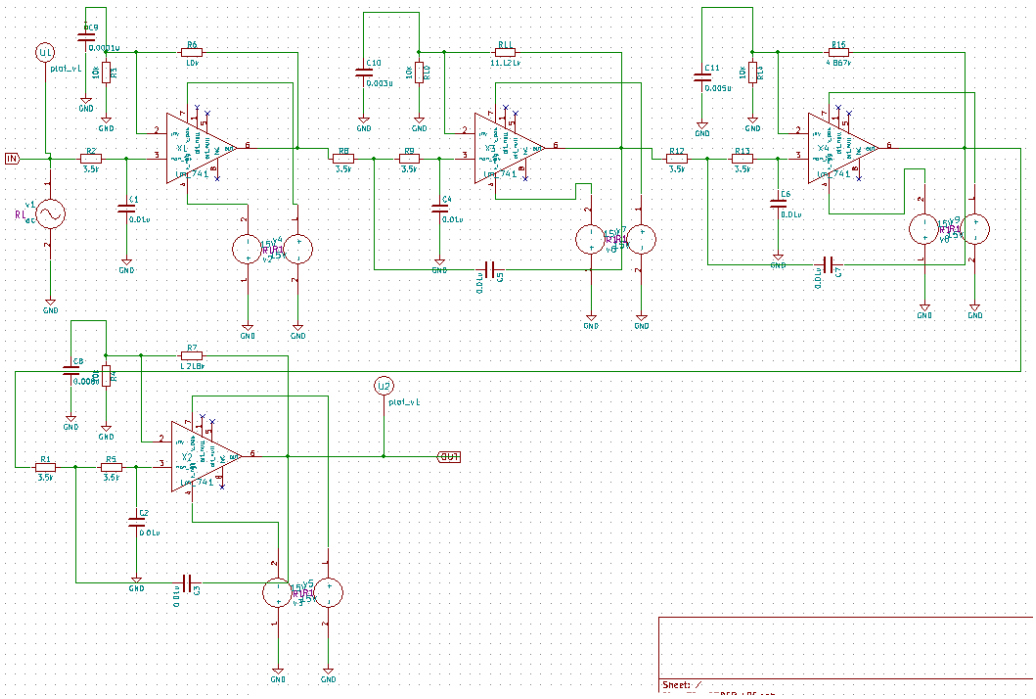

Figure15.7.1 Circuit Diagram

INPUT AND OUTPUT WAVEFORM:

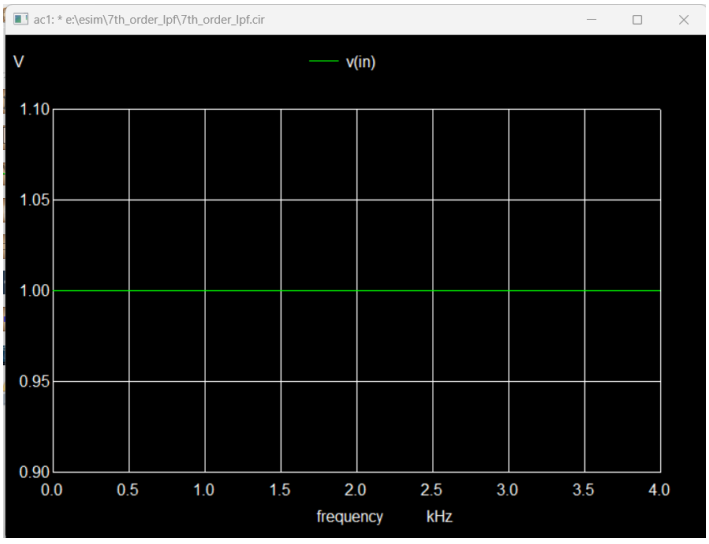

Figure15.7.2 Input waveform

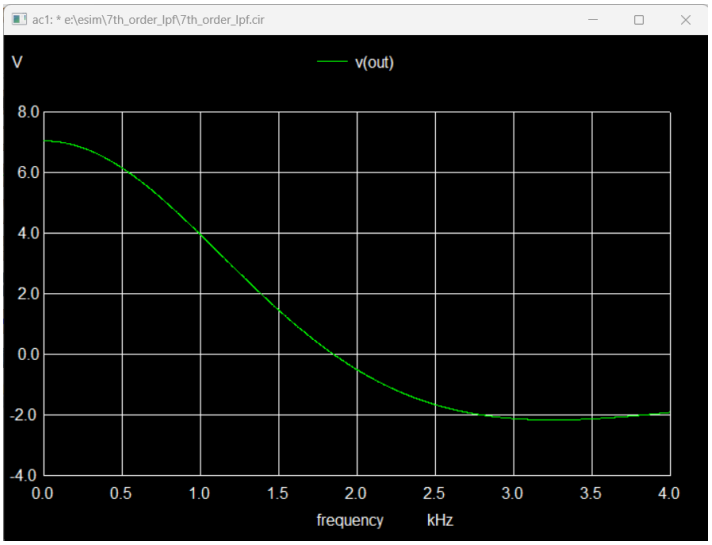

Figure15.7.3 Output waveform

15.8 EIGTH ORDER BESSEL LOW PASS FILTER

CIRCUIT DIAGRAM:

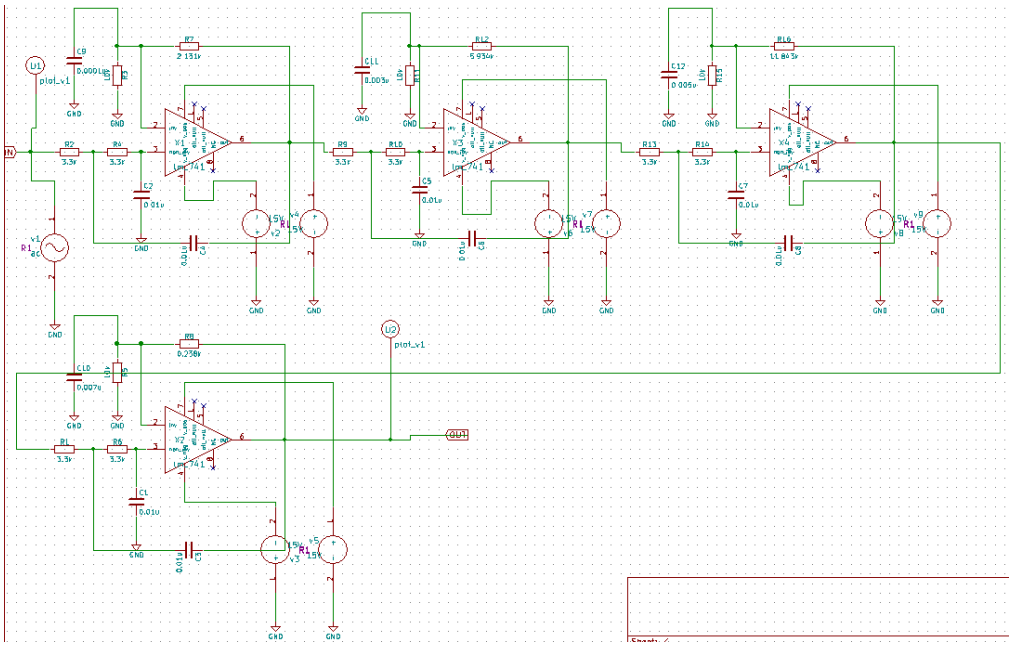

Figure15.8.1 Circuit Diagram

INPUT AND OUTPUT WAVEFORM:

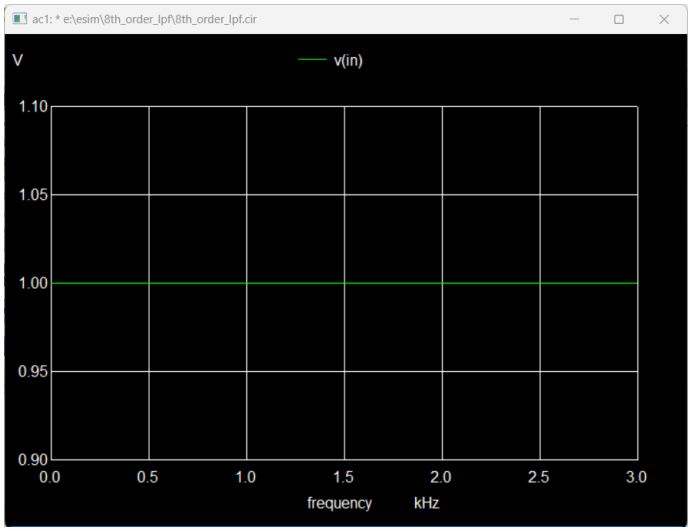

Figure15.8.2 Input waveform

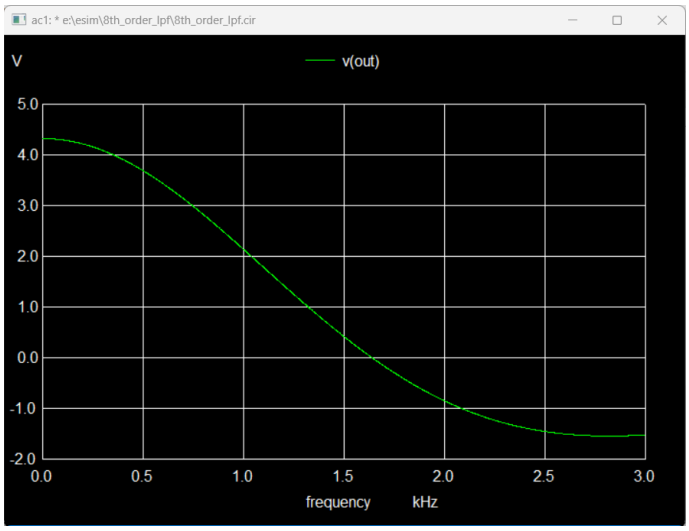

Figure15.8.3 Output waveform

15.9 NINETH ORDER BESSEL LOW PASS FILTER

CIRCUIT DIAGRAM:

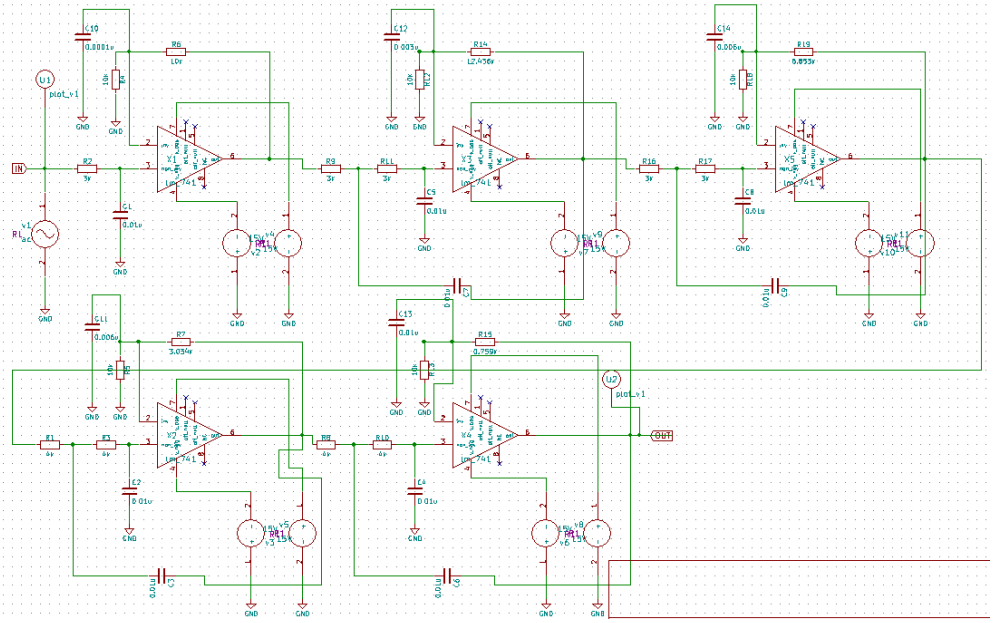

Figure15.9.1 Circuit Diagram

INPUT AND OUTPUT WAVEFORM:

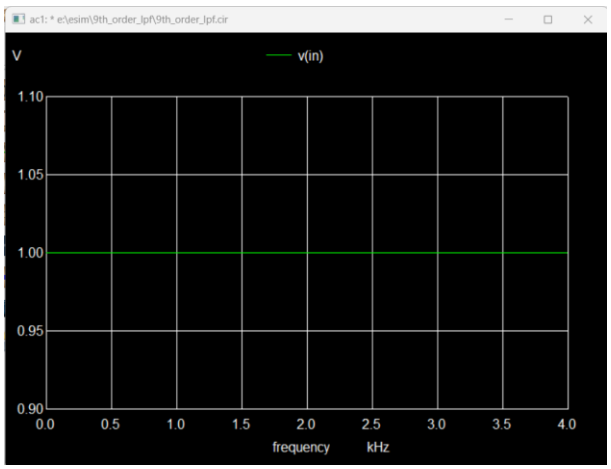

Figure15.9.2 Input waveform

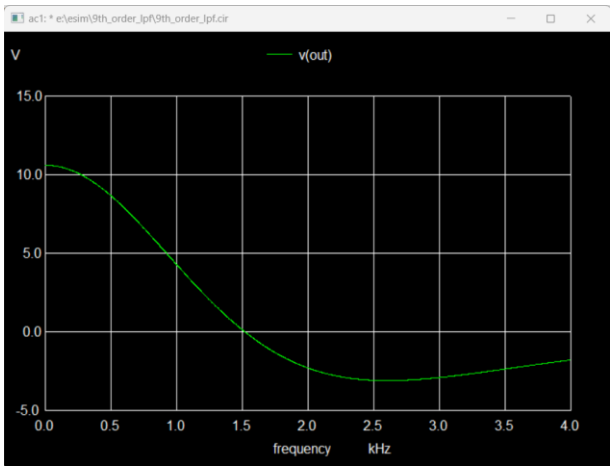

Figure15.9.3 Output waveform

15.10 TENTH ORDER BESSEL LOW PASS FILTER

CIRCUIT DIAGRAM:

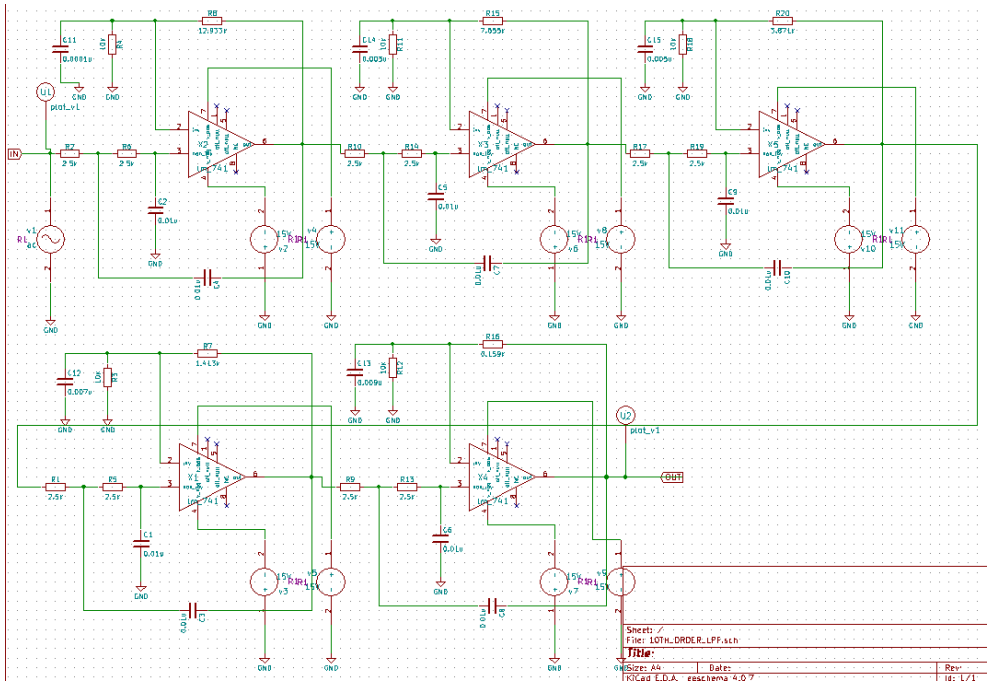

Figure15.10.1 Circuit Diagram

INPUT AND OUTPUT WAVEFORM:

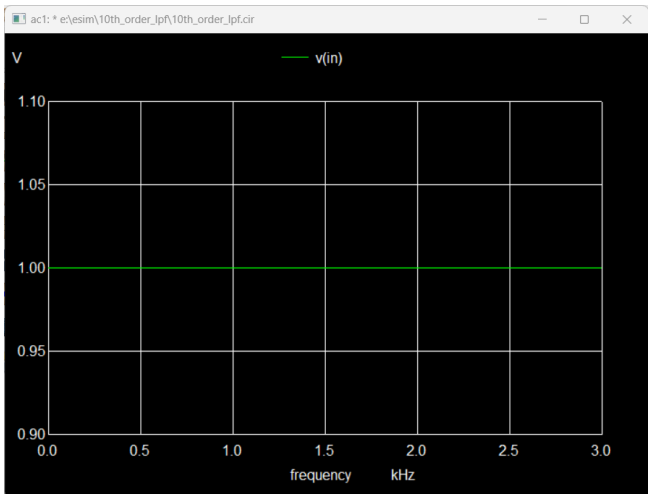

Figure15.10.2 Input waveform

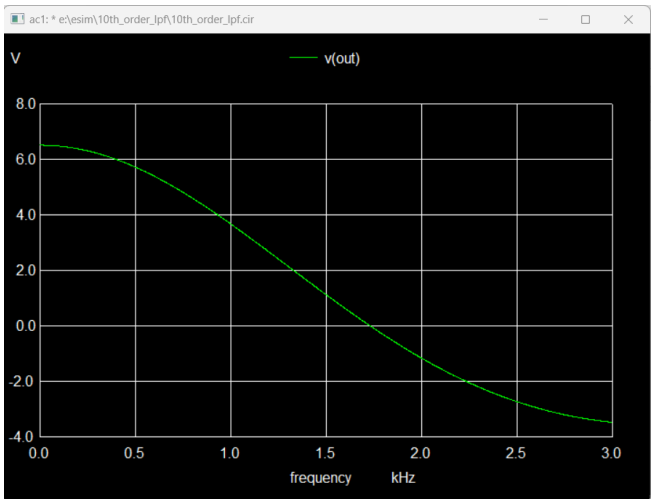

Figure15.10.3 Output waveform

16. CONCLUSION AND FUTURE SCOPE

Integrated Circuits on Filters were designed and used in test circuits to verify their working. These ICs are able to provide the results of the Butterworth and Bessel Low Pass Filter designs. The designed Filter ICs can be used as an application in Radio links & Modems, Antialiasing Filters, Smoothing & Reconstruction Filters, Matched Filter Pairs, Replacement of LC Filters, ADC Anti-aliasing, DAC Postfiltering, Speech processing and Data Communications. Further, these ICs can be used to build higher order filter ICs and dual channel filter ICs.

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