Semester Long Internship Report

On

Designing Integrated Circuit in eSim

Submitted By

Aman Shukla

Under the guidance of

Prof.Kannan M. Moudgalya
Chemical Engineering Department

IIT Bombay

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Acknowledgment

I would like to express my sincerest gratitude to the entire FOSSEE team for providing me this golden opportunity to be part of their Semester Long Internship program. The experience of working with an open-source organization such as FOSSEE has been immensely informative. It has given me the opportunity to learn about the complexities of simulation programs like eSim and develop valuable problem-solving abilities. My sincere gratitude goes out to Prof. Kannan M. Moudgalya for his visionary leadership and commitment to the advancement of this project.

In addition, I want to express my gratitude to Mr. Sumanto Kar and Dr. Shubhankar Majumdar, who served as our mentors. Throughout my internship, their constant support and mentoring have been helpful. They were always there to offer advice and assist me in navigating through complexities so that I could find practical solutions whenever I ran into problems.

Overall, I had a great time interning with FOSSEE. My future will undoubtedly be shaped by the amazing thoughts and information I have learned. This internship is an important turning-point in my career aspirations as a professional in the semiconductor sector.

Contents

Introduction

The FOSSEE project at IIT Bombay, part of the National Mission on Education through ICT, promotes the use of free/libre and open source software (FLOSS) in Indian education to reduce reliance on proprietary software. Through various activities, FOSSEE encourages the adoption of FLOSS tools, develops new ones, and upgrades existing ones for academic and research needs.

eSim, a FLOSS EDA tool developed by FOSSEE, IIT Bombay, facilitates circuit design, simulation, analysis, and PCB design. It integrates open-source tools like KiCad, Ngspice, NGHDL, and GHDL. Ngspice is a versatile circuit simulator for various analyses, supporting a wide range of components and semiconductor devices. Makerchip is a platform providing accessible browser-based and desktop environments for Verilog digital circuit design, compilation, simulation, and debugging, utilizing both open-source and proprietary tools. Verilator converts Verilog files to C++. In eSim's ngveri, Verilog designs are first simulated in Verilator with random inputs to verify their correctness before proceeding with mixed-signal design.

The objective of this internship is to design integrated circuits (ICs) for eSim's subcircuit library, utilizing eSim tools such as the KiCAD to NGSpice converter and the Verilog code to NGSpice converter. This will allow users to simulate and incorporate these ICs into more complex circuit designs.

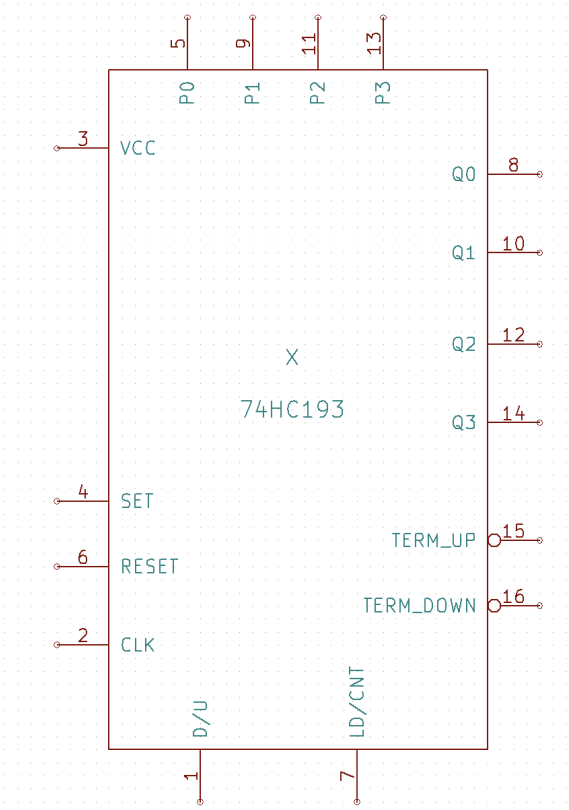
Chapter 2

IC 74HC193

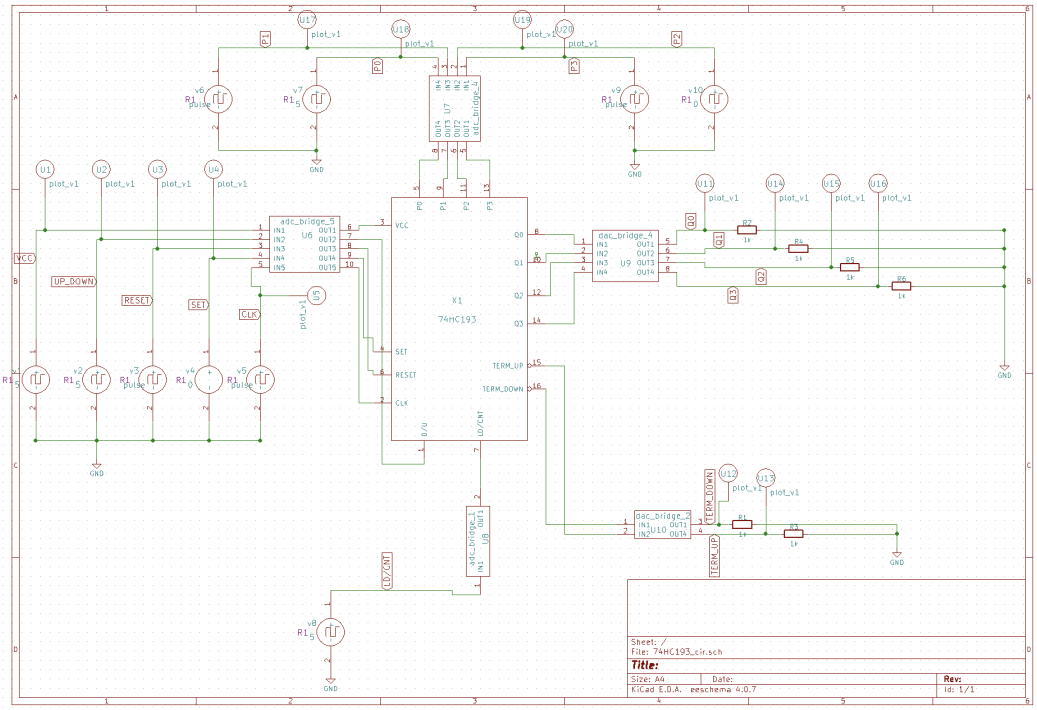
2.1 Circuit Details

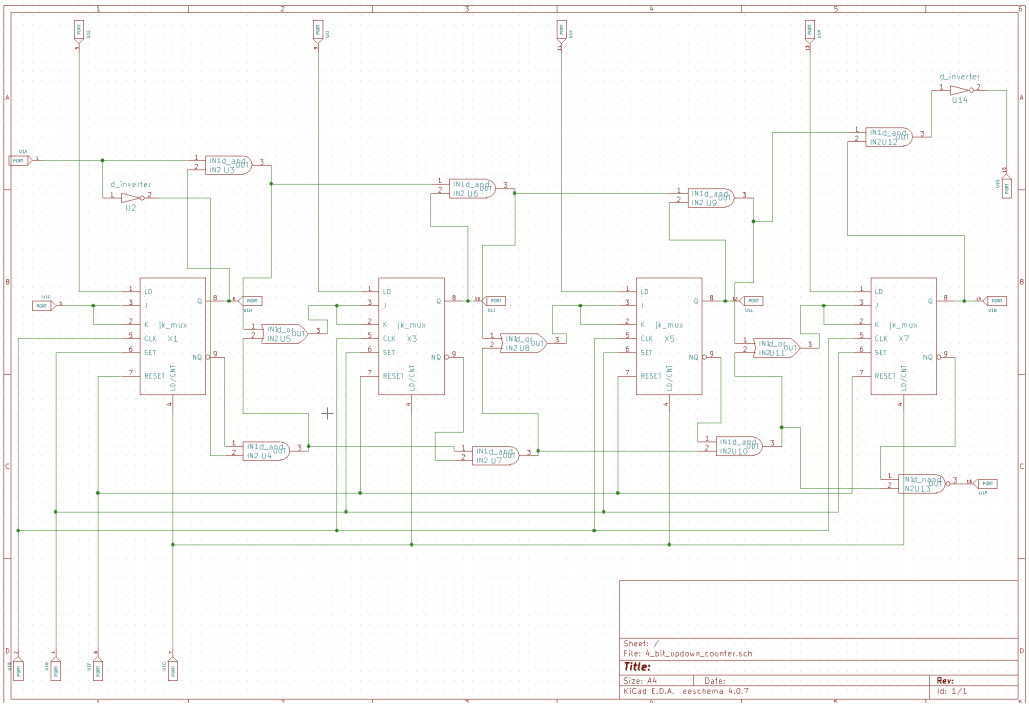
The SN74HC193 is a high-speed CMOS, fully synchronous 4-bit up/down binary counter featuring separate UP and DOWN clock inputs to control incrementing or decrementing on each rising edge. It incorporates an asynchronous, active-HIGH CLR input that immediately resets all Q outputs to zero, regardless of clock activity or load state. A parallel LOAD input (active LOW) allows any 4-bit value present on the A–D inputs to be transferred into the counter on the next clock pulse. Look-ahead carry (CO) and borrow (BO) outputs pulse at terminal counts (all “1”s for carry, all “0”s for borrow) to enable ripple-free cascading of multiple counters. Because all four internal D-flip-flops are clocked simultaneously, the SN74HC193 avoids the count-spiking issues typical of ripple counters and ensures glitch-free operation. It operates over a 2 V to 6 V supply range, draws minimal static ICC current, and offers typical propagation delays in the 15–25 ns range at VCC = 5 V.

2.2 Pin Diagram

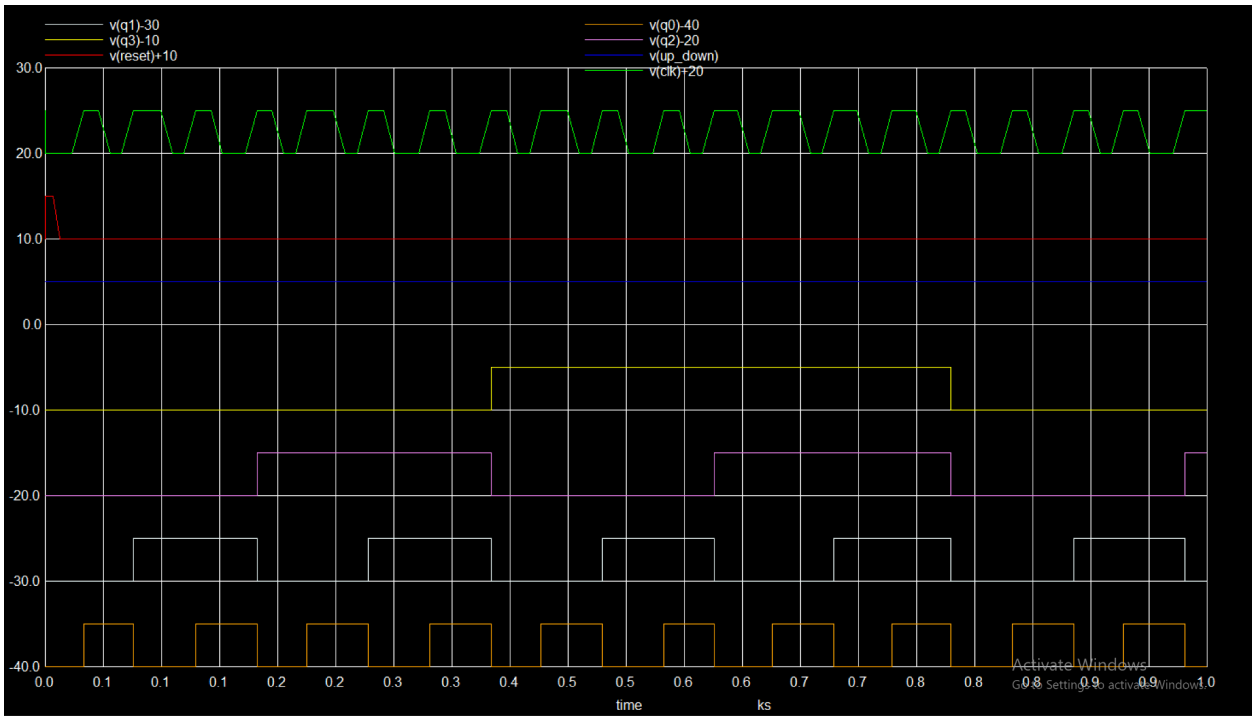


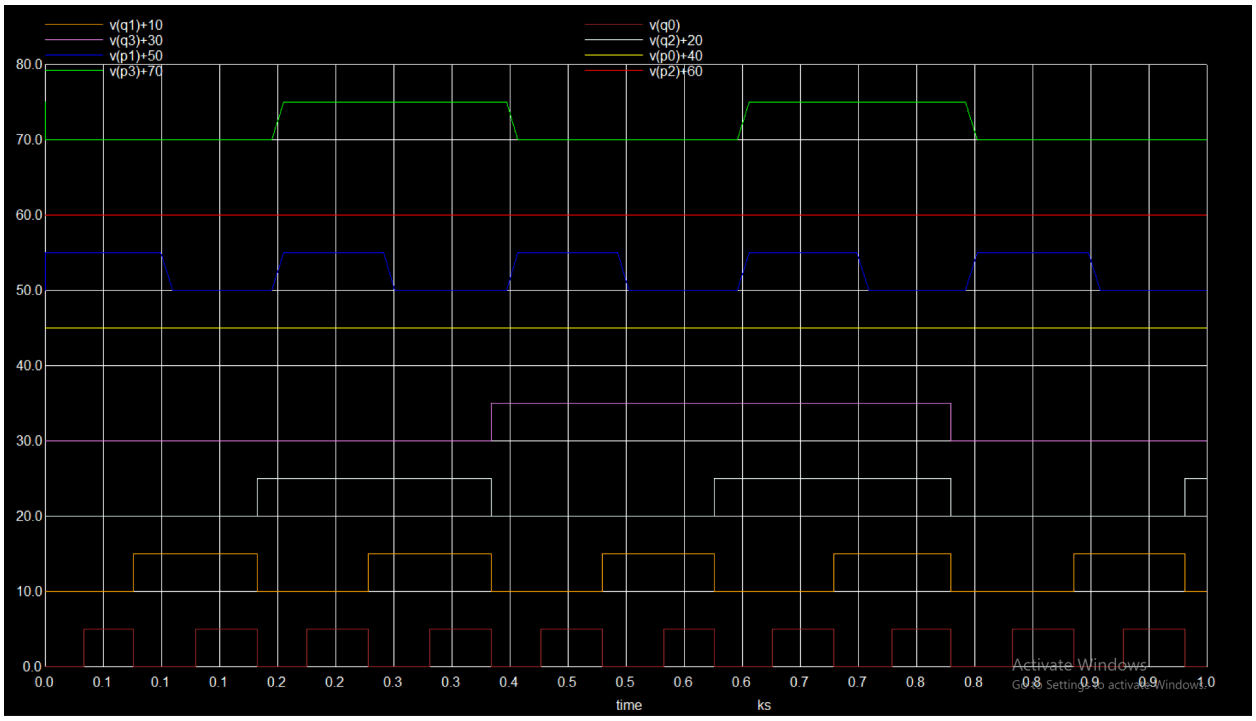
2.3 Schematic diagram





2.4 Simulation Output





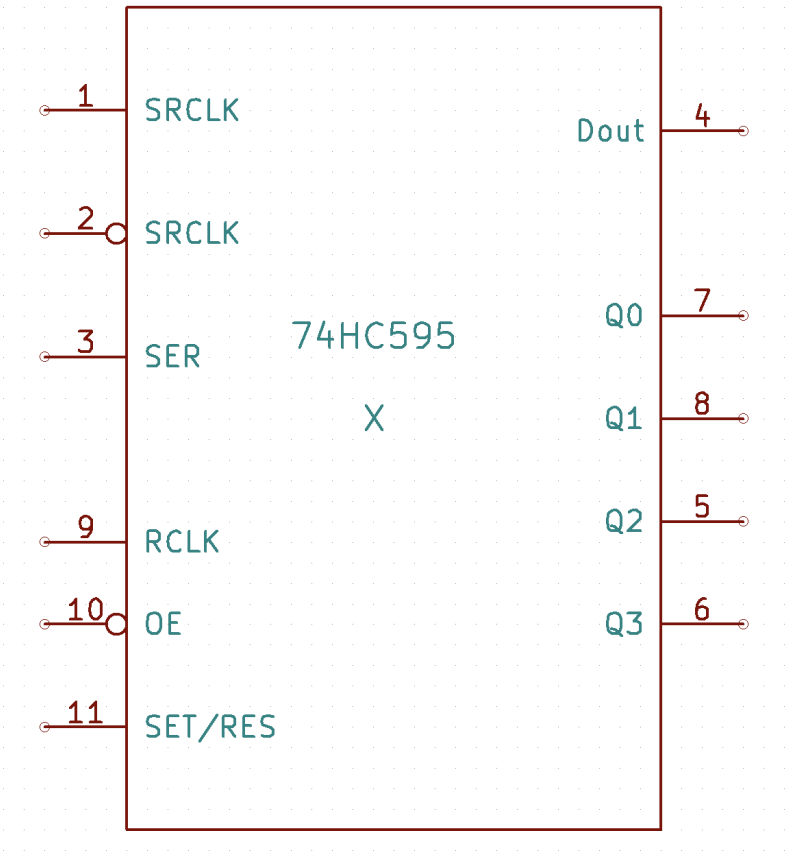
Chapter 3

IC 74HC595

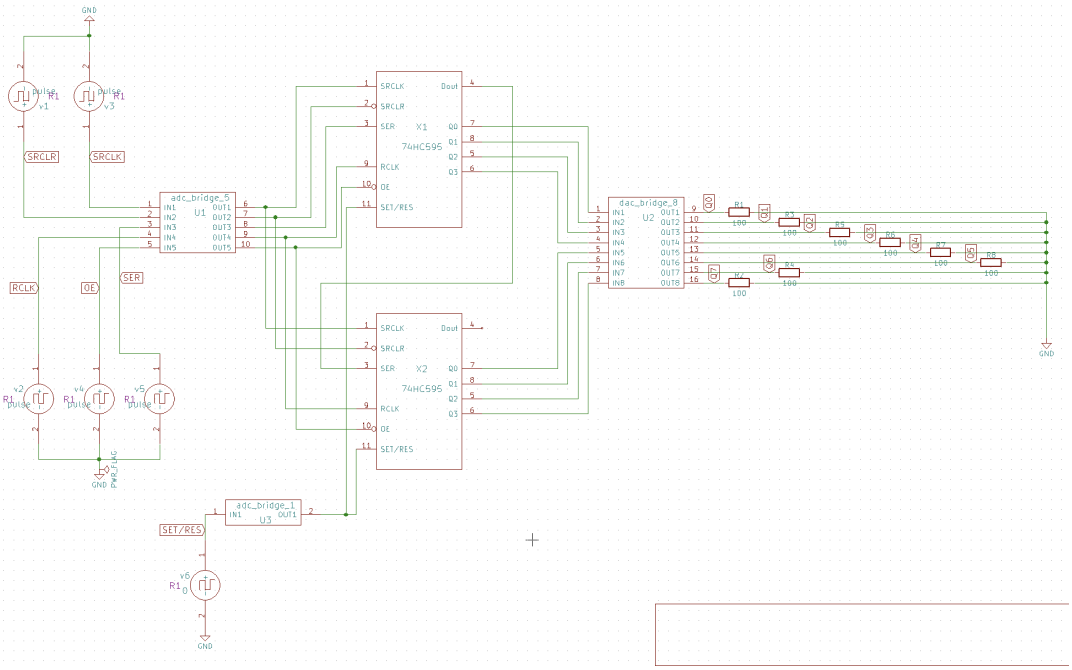
3.1 Circuit Details

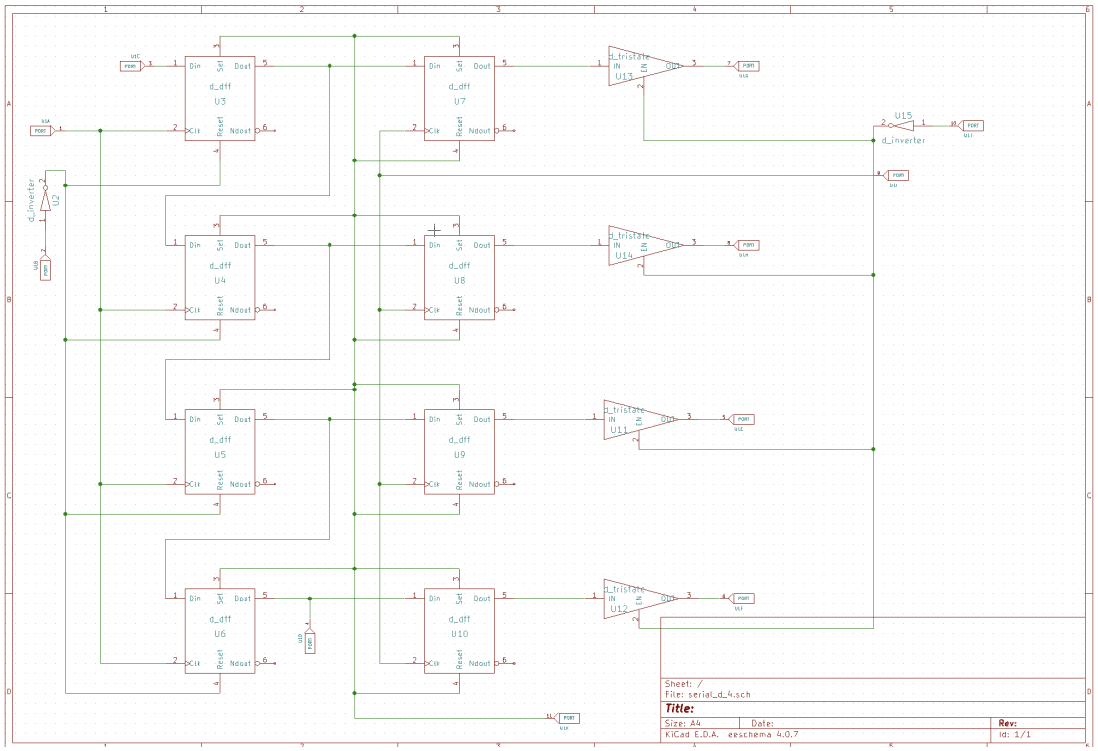
The SN74HC595 comes in a 16-pin package whose key pins are arranged as follows. On one side you have the serial data input (SER, pin 14), the shift-clock input (SRCLK, pin 11), and the latch-clock input (RCLK, pin 12); together these let you clock bits into the internal 8-bit shift register and then transfer them en masse into the output register. The active-LOW shift-register clear (SRCLR, pin 10) asynchronously resets the shift register to all zeros, while the output-enable (OE, pin 13, active LOW) gates the eight outputs into a high-impedance state for bus sharing. The parallel outputs QA through QH appear on pins 15, 1, 2, 3, 4, 5, 6, and 7, respectively, and there's a serial "daisy-chain" output QH' on pin 9 that reflects the last bit shifted in. Finally, VCC is on pin 16 and GND on pin 8. Together, these pins let you cascade multiple 74HC595s to expand microcontroller I/O by shifting data down a chain, latching it, and selectively enabling or clearing outputs—all with just three control lines plus data in.

3.2 Pin Diagram

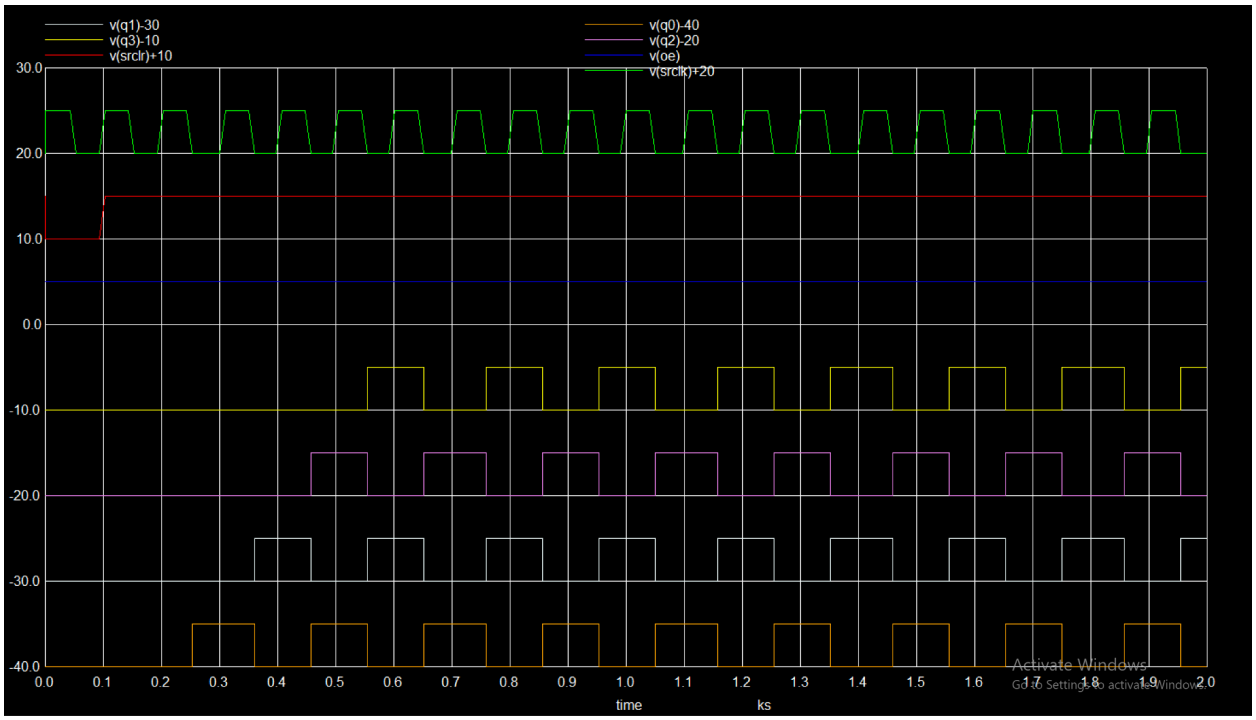


3.3 Schematic diagram





3.4 Simulation Output



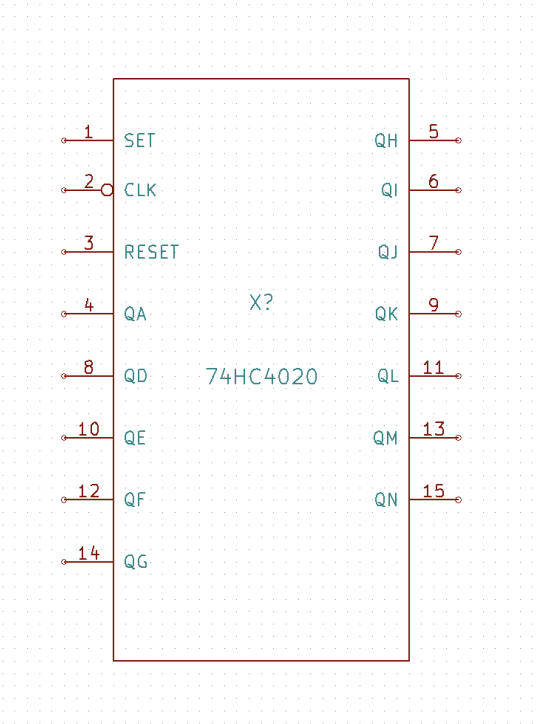
Chapter 4

IC 74HC4020

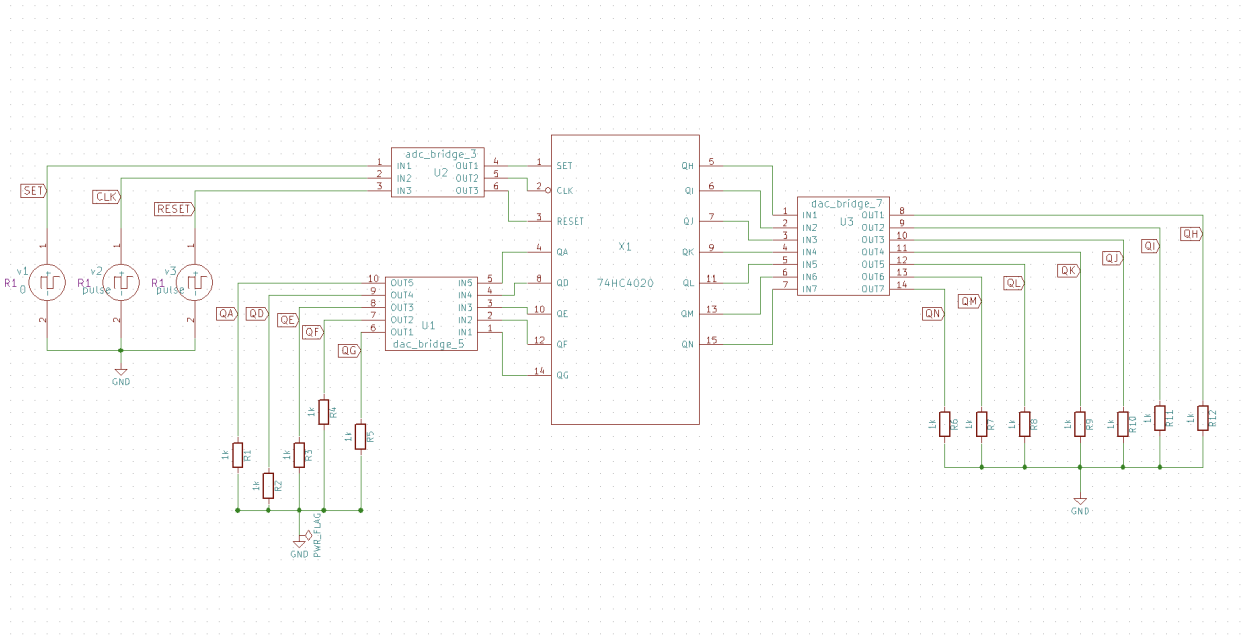
4.1 Circuit Details

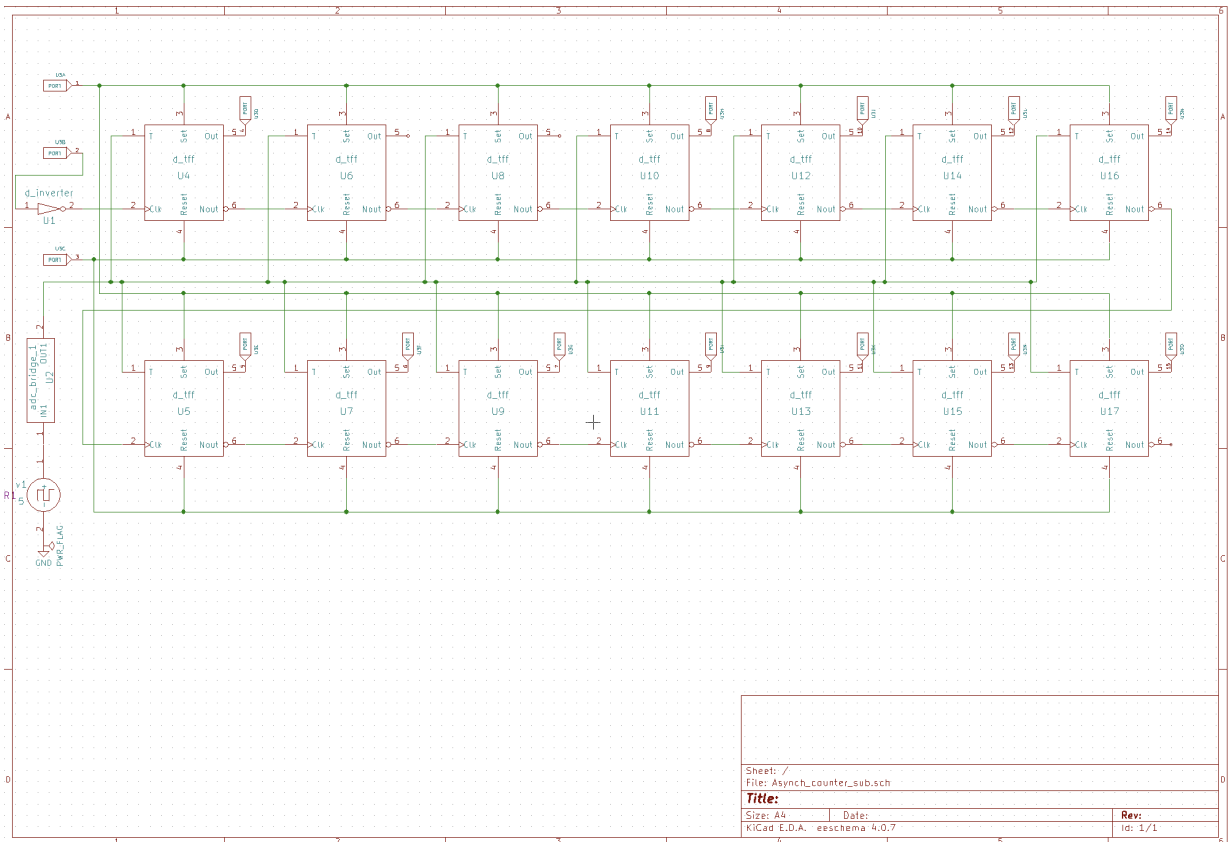
The SN74HC4020 is a 14-stage ripple-carry binary counter in a 16-pin package, with its master reset (MR, pin 11) held LOW to enable counting and taken HIGH to asynchronously clear all output stages. The clock input (CLK, pin 10) advances the count on each rising edge, feeding a chain of 14 flip-flops whose Q1–Q7 outputs appear on pins 9, 7, 6, 5, 4, 3, and 2, and whose Q8–Q14 outputs are on pins 1, 15, 14, 13, 12, 8, and 9 (note Q9/Q1 share pin 9). VCC is on pin 16 and GND on pin 8. Each flip-flop output toggles at half the frequency of its predecessor, so Q1 divides CLK by 2, Q2 by 4, … up to Q14 by 16,384, making the 4020 ideal for large-range frequency division, time-base generation, and event counting with minimal external gating. You can cascade multiple 4020s by feeding the overflow of the highest stage into the CLK of the next device or by OR’ing selected outputs for custom division ratios.

4.2 Pin Diagram



4.3 Schematic diagram




d_inverter
U1
d_tff
U4
U5
U6
U7
U8
U9
U10
U11
U12
U13
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U15
U16
U17
adc_bridge_1
U2
V1
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GND
PWR_FLAG
Sheet: /
File: Asynch_counter_sub.sch
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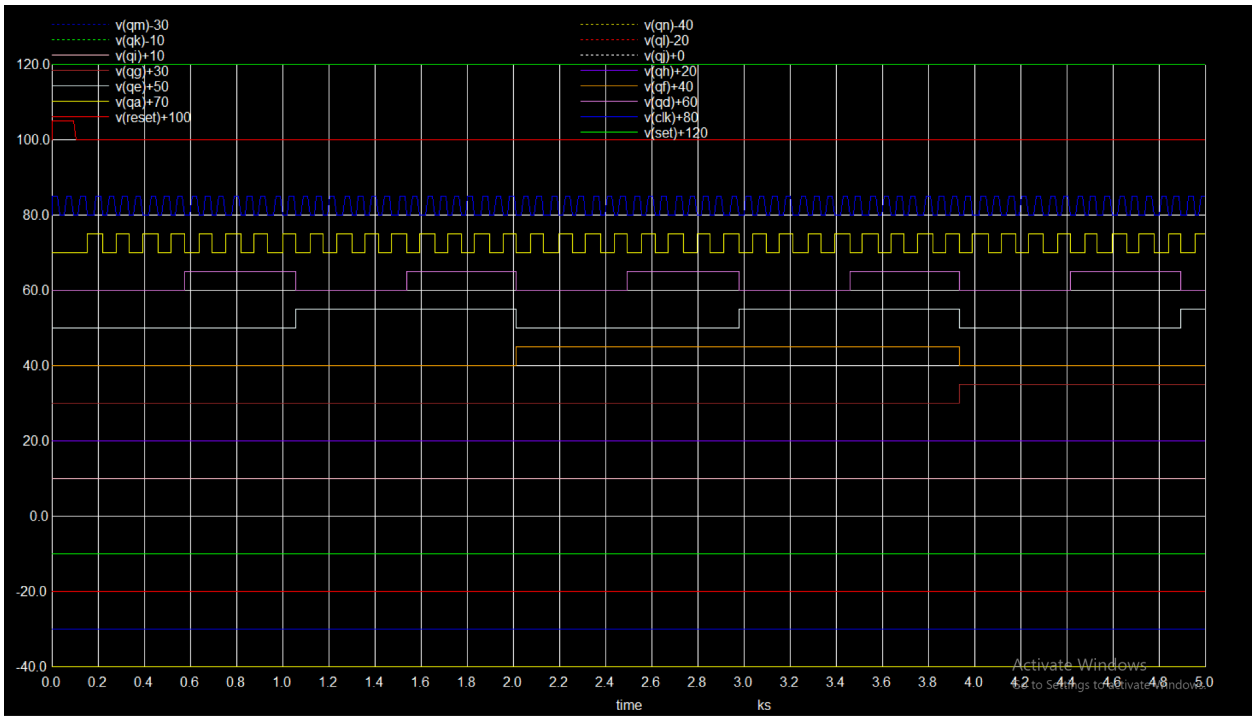
KiCad E.D.A. eeschema 4.0.7
Id: 1/1

4.4 Simulation Output



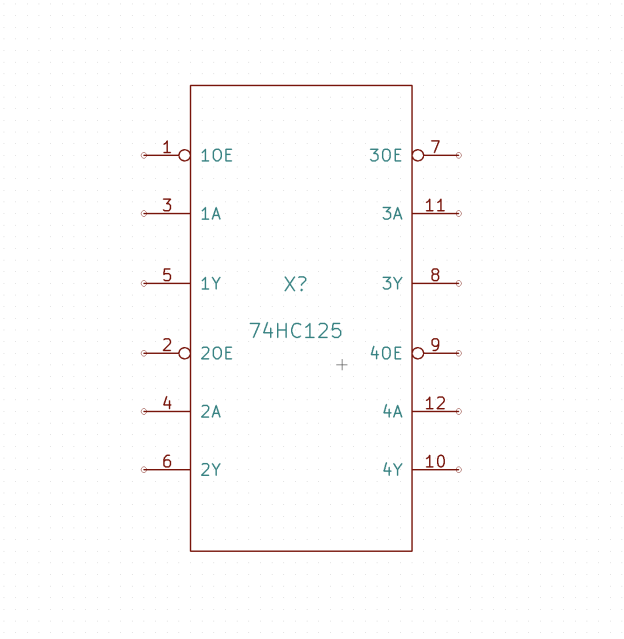
Chapter 5

IC 74HC125

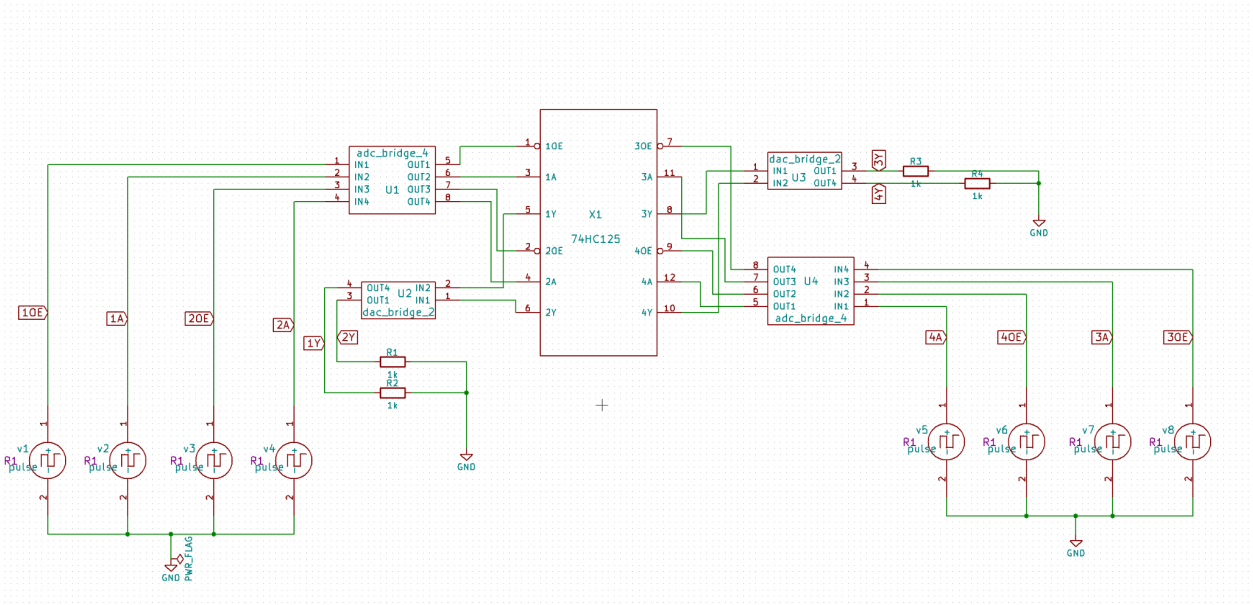
5.1 Circuit Details

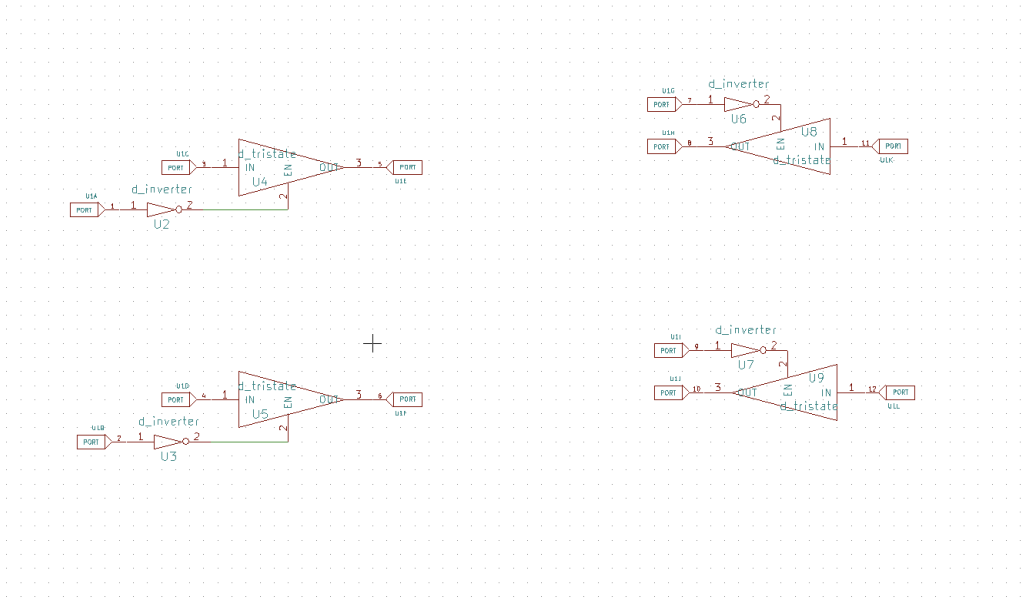
The SN74HC125 is a quad, non‑inverting bus buffer with independent 3-state outputs. Each of the four gates implements the Boolean function Y = A in positive logic, with an output-enable (OE) input that, when HIGH, places the corresponding Y output into a high-impedance state. On a 14-pin package, OE1 (pin 1), A1 (pin 2), and Y1 (pin 3) form gate 1; OE2 (pin 4), A2 (pin 5), and Y2 (pin 6) form gate 2; GND is pin 7; gate 3 is Y3 (pin 8), A3 (pin 9), OE3 (pin 10); gate 4 is Y4 (pin 11), A4 (pin 12), OE4 (pin 13); and VCC is pin 14. The device operates from 2 V to 6 V and is specified for typical propagation delays around 11 ns.

5.2 Pin Diagram

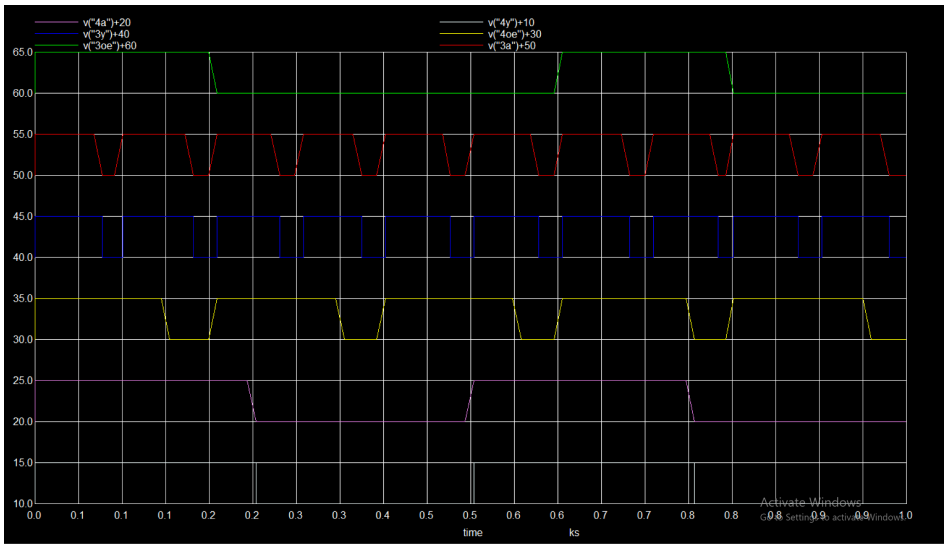


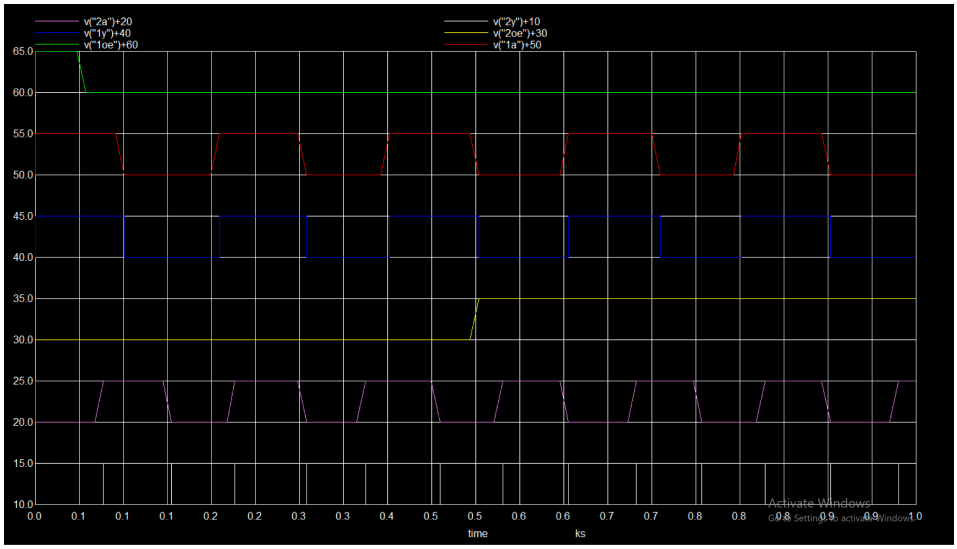
5.3 Schematic diagram





5.4 Simulation Output





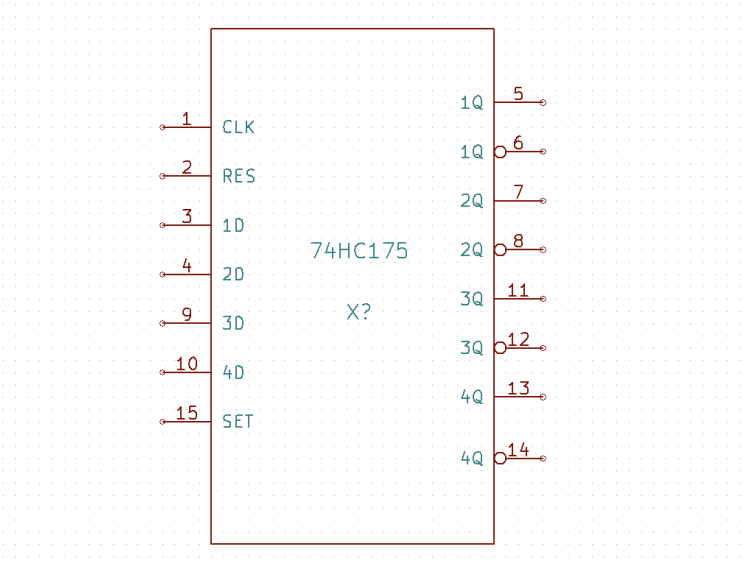
Chapter 6

IC 74HC175

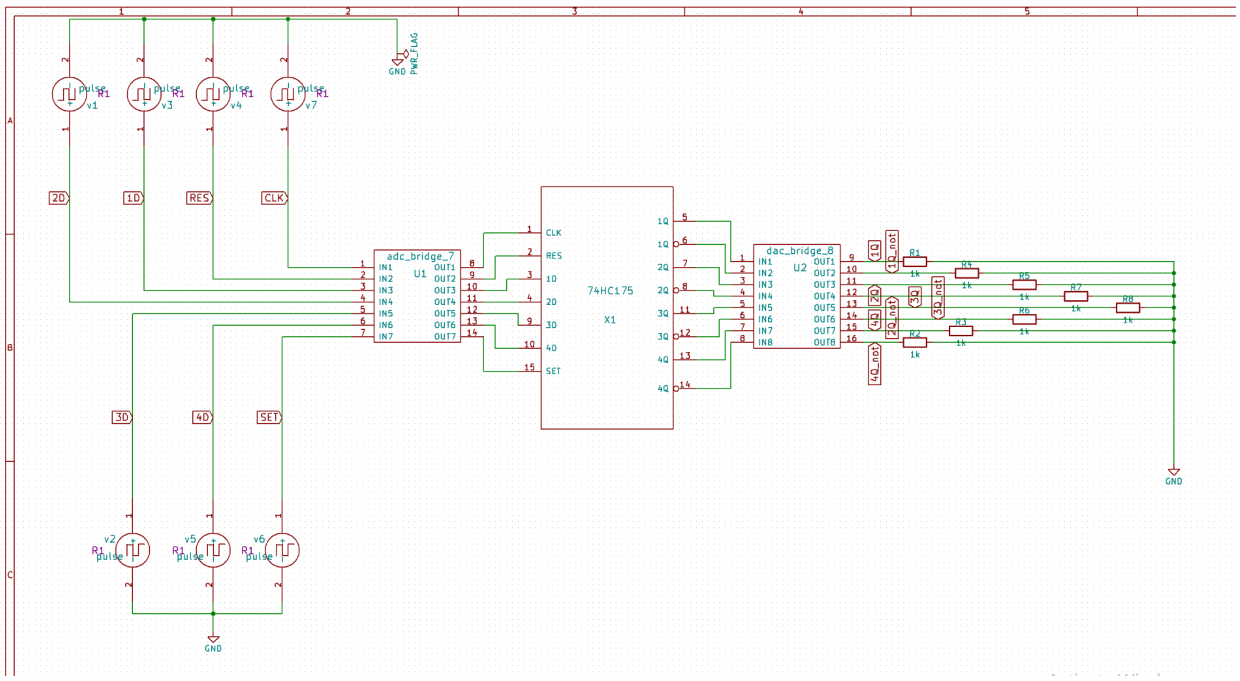
6.1 Circuit Details

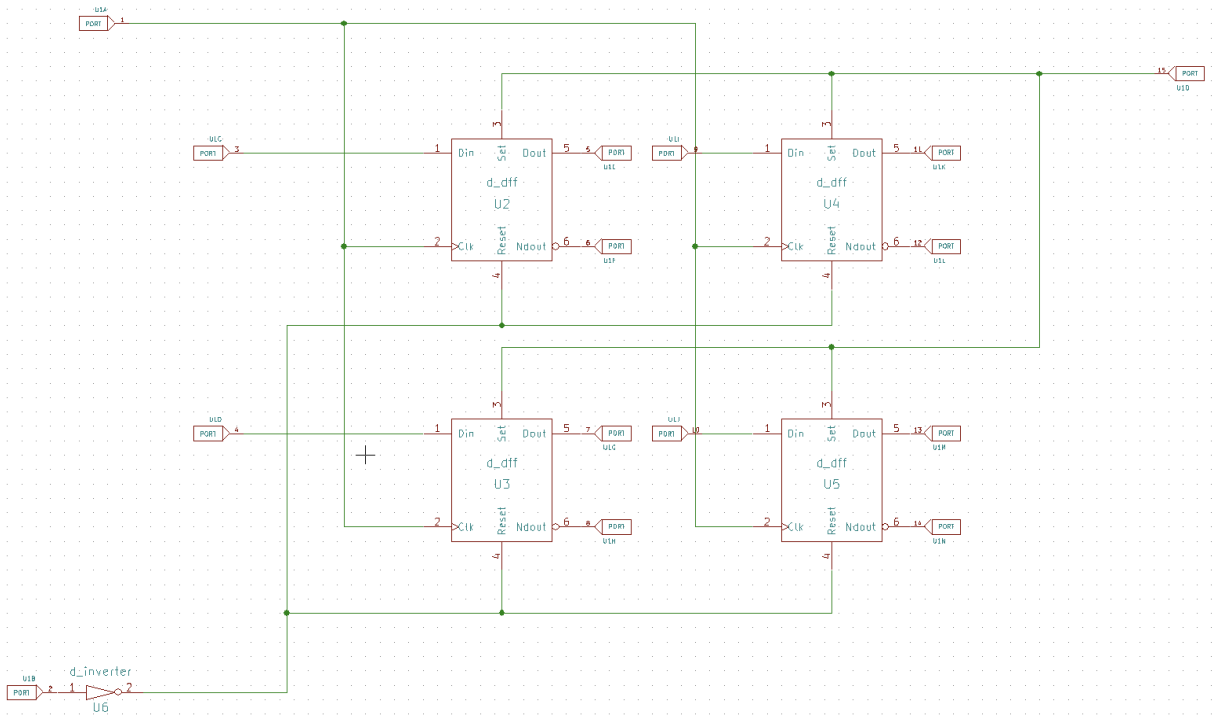
The SN74HC175 is a quad, positive-edge-triggered D-type flip-flop with an asynchronous, active-LOW master reset (MR) that, when asserted (pin 1), clears all four Q outputs to LOW regardless of clock or data. A single clock input (CLK, pin 9) simultaneously latches each of the four data inputs D0–D3 (pins 4, 5, 12, 13) into its corresponding flip-flop on the rising edge, provided MR is held HIGH. Each flip-flop provides both true outputs Q0–Q3 (pins 2, 7, 10, 15) and complementary outputs Q0′–Q3′ (pins 3, 6, 11, 14), enabling easy bus driving or feedback without external inverters. The device operates from 2 V to 6 V (VCC on pin 16, GND on pin 8) and typically exhibits a propagation delay of ≈13 ns at VCC = 5 V, making it suitable for moderate-speed storage and register applications. All unused inputs must be tied to VCC or GND to prevent floating-input issues, and each flip-flop can drive up to 10 LSTTL loads.

6.2 Pin Diagram

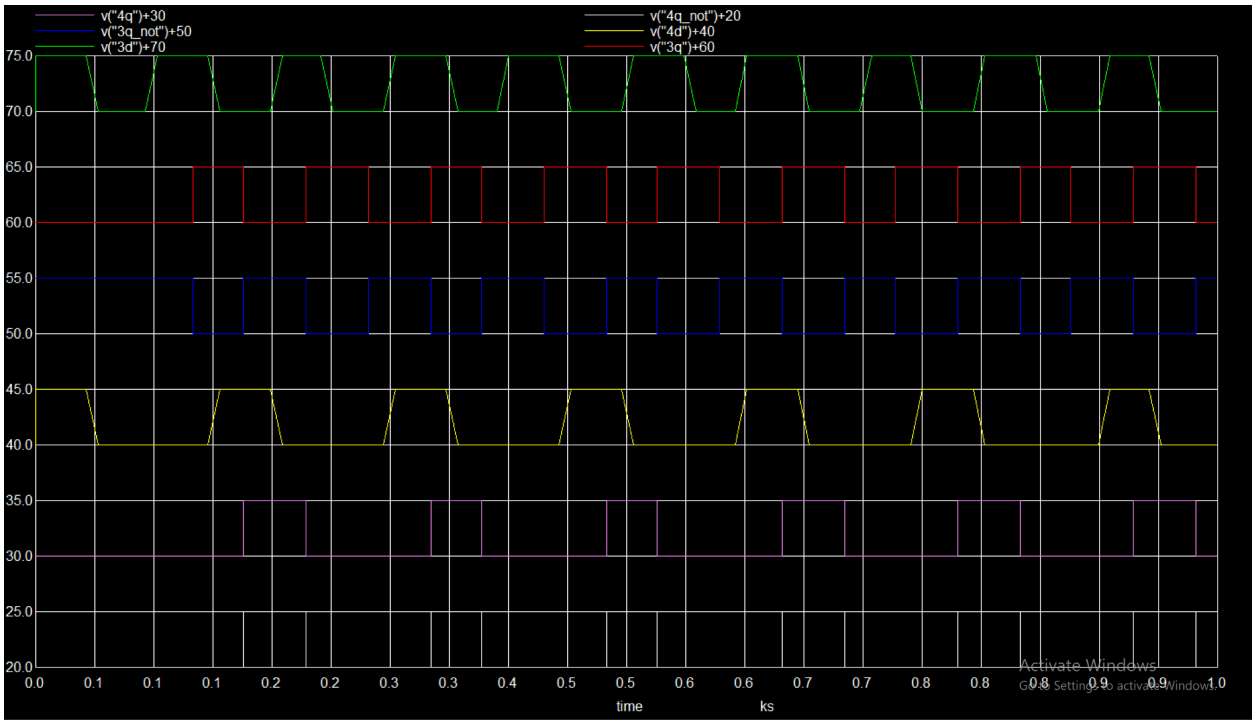


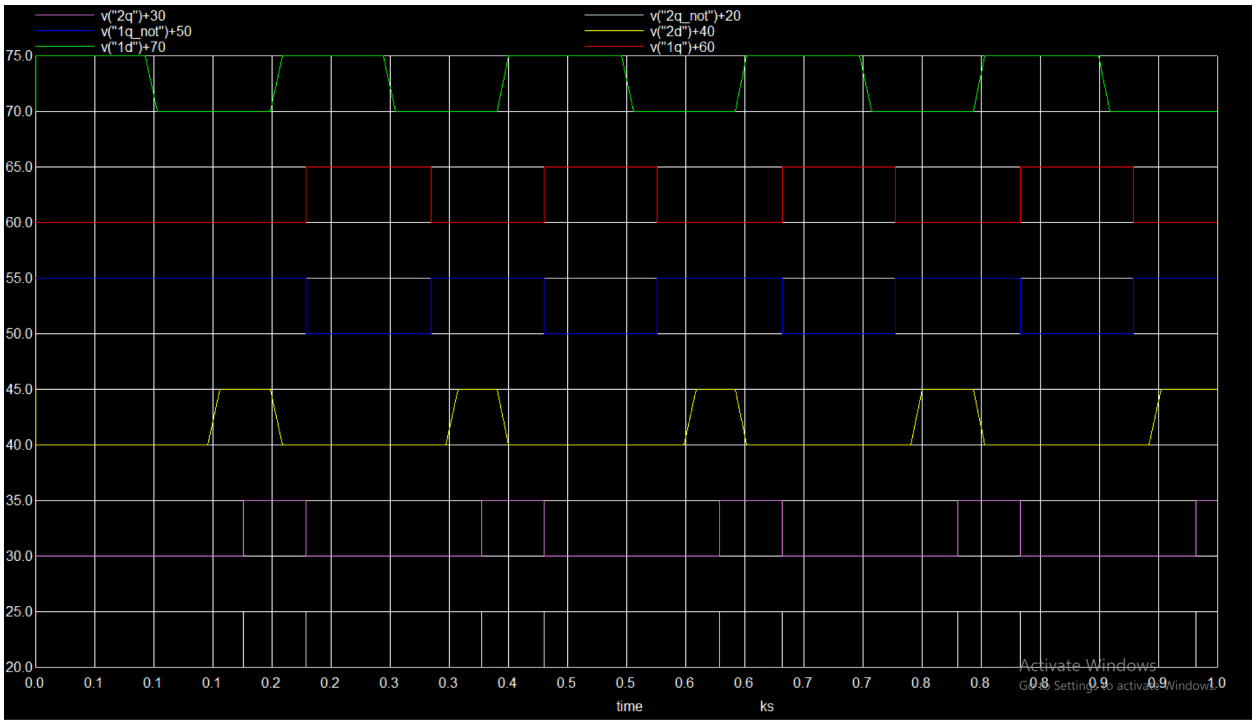
6.3 Schematic diagram





6.4 Simulation Output





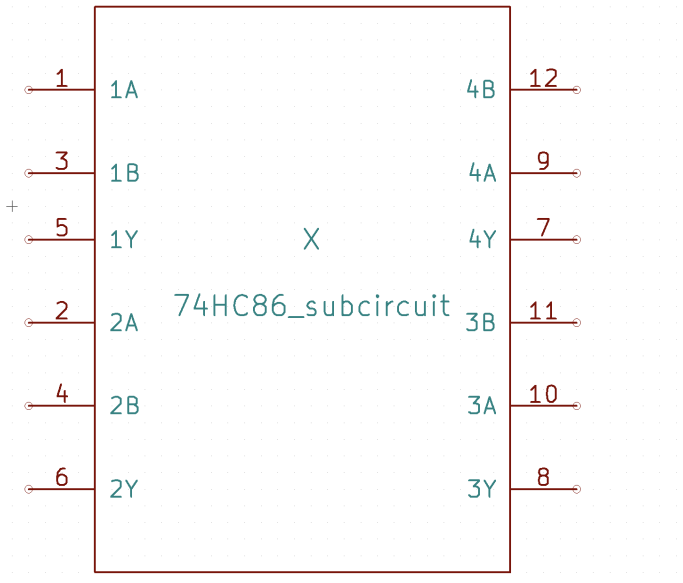
Chapter 7

IC 74HC86

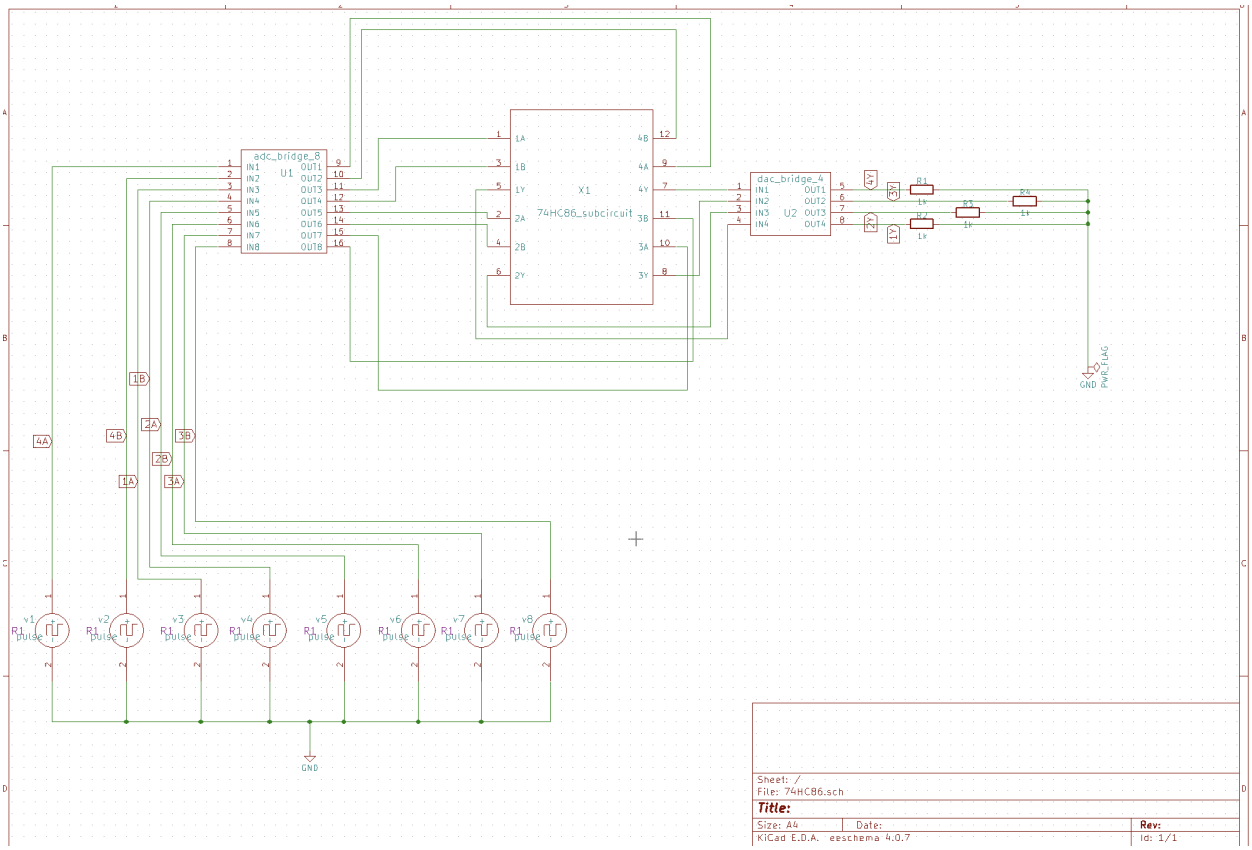
7.1 Circuit Details

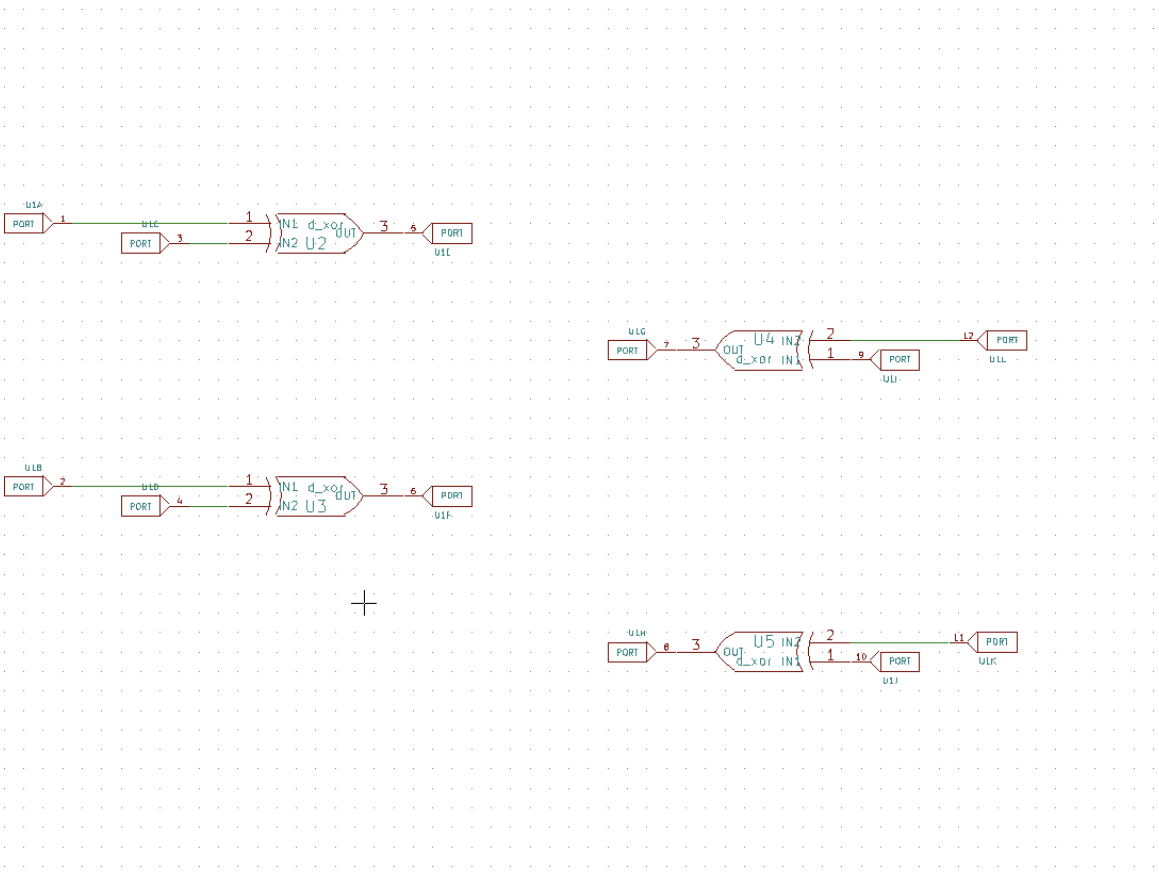
The SN74HC86 is a quad, 2-input exclusive-OR gate in a 14-pin package that performs the Boolean function Y = A ⊕ B in positive logic. Each gate has two buffered inputs (A1/B1 on pins 1/2, A2/B2 on pins 4/5, A3/B3 on pins 9/10, A4/B4 on pins 12/13) and a corresponding output (Y1–Y4 on pins 3, 6, 8, 11). Ground (GND) is on pin 7 and VCC on pin 14. With a wide operating voltage range of 2 V–6 V and typical propagation delays of about 10 ns, it supports fan-out of up to 10 LSTTL loads and is ideal for parity checking, phase-difference detection, and creating inverters/buffers by tying one input HIGH or LOW. Because all four gates are independent, you can cascade or combine their outputs for more complex even- or odd-parity and comparison functions without additional external logic.

7.2 Pin Diagram

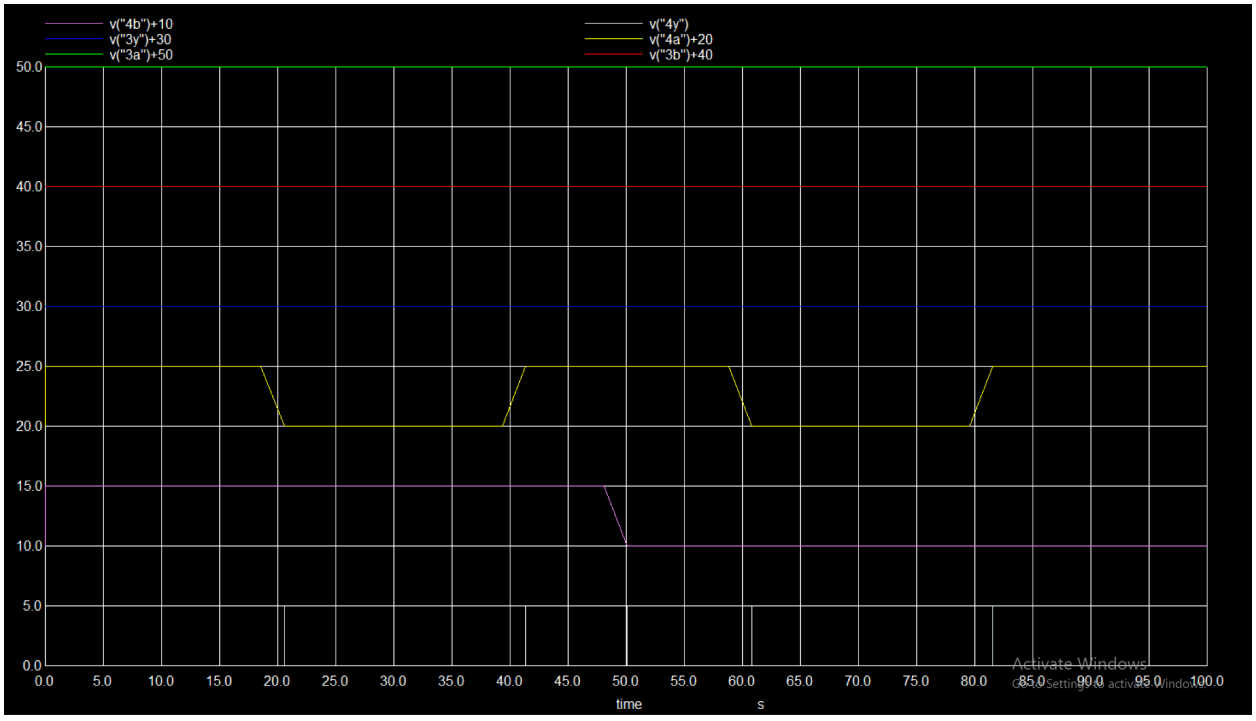


7.3 Schematic diagram





7.4 Simulation Output



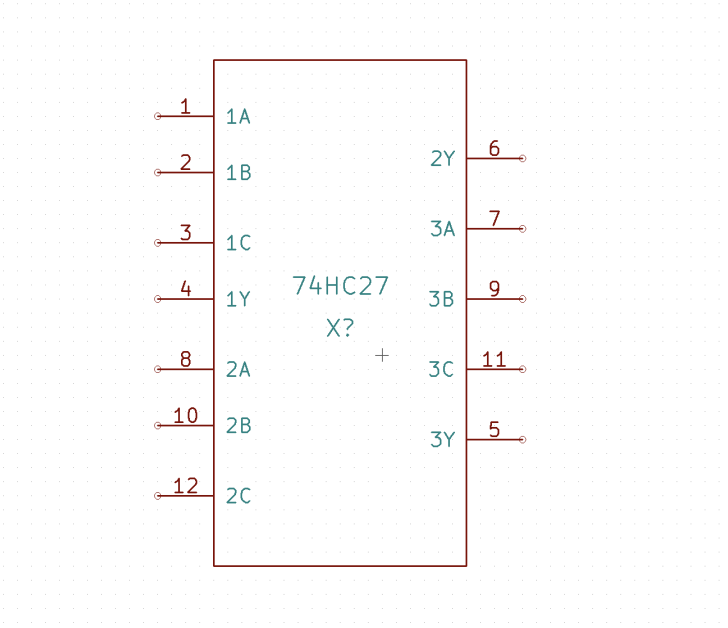
Chapter 8

IC 74HC27

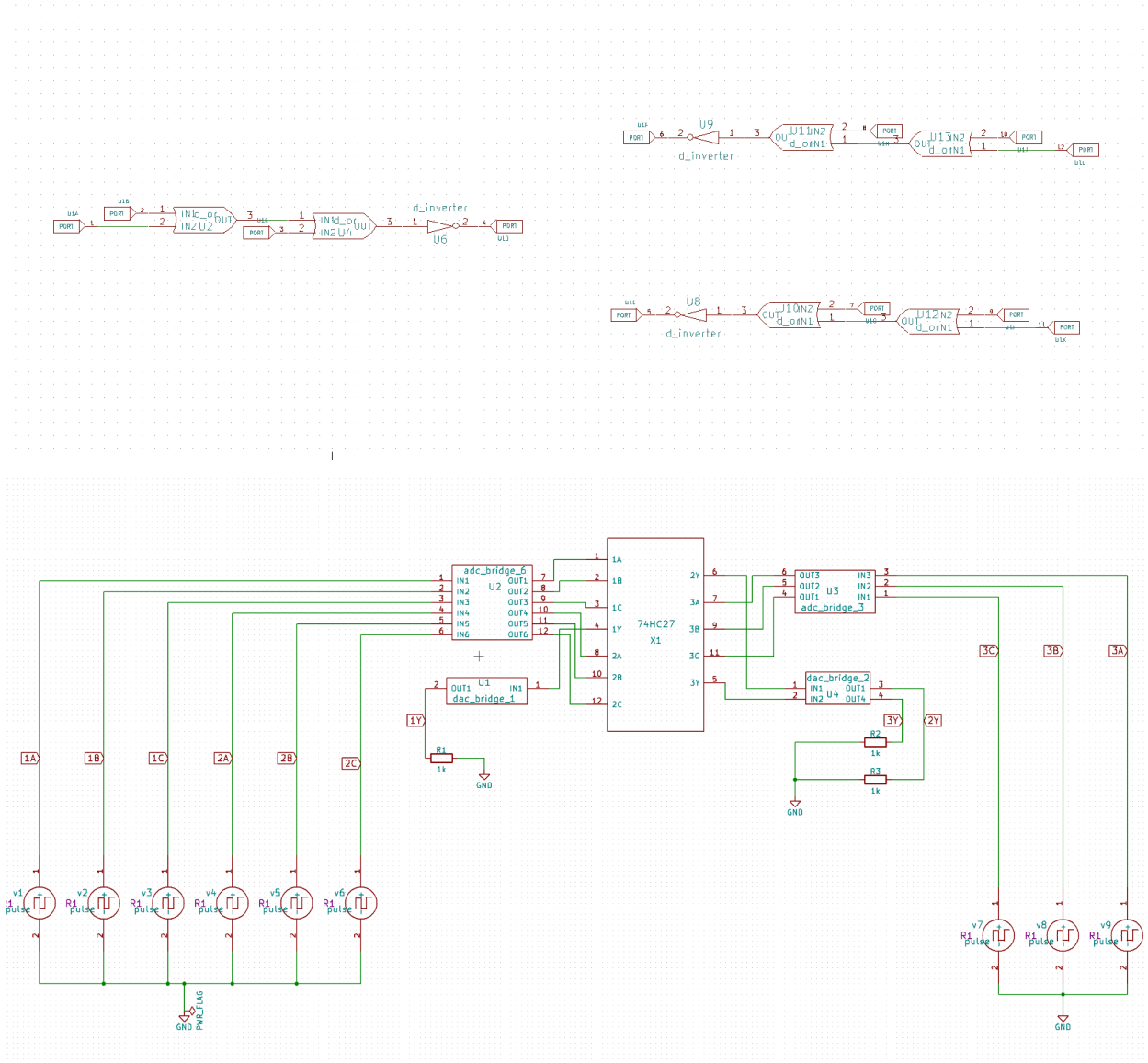
8.1 Circuit Details

The SN74HC27 contains three independent 3-input positive-logic NOR gates, each implementing the Boolean function Y = ¬(A · B · C). All inputs are buffered for low skew: Gate 1's inputs A1/B1/C1 are on pins 1, 2, 3 with output Y1 on pin 4; Gate 2's A2/B2/C2 are on pins 5, 6, 7 with Y2 on pin 8; Gate 3's A3/B3/C3 are on pins 9, 10, 11 with Y3 on pin 12. VCC is on pin 14 and GND on pin 7. The device operates over a 2 V–6 V supply range and typically exhibits propagation delays around 10 ns at VCC = 5 V, making it suitable for high-speed logic applications, wired-NOR functions, and simple combinational logic without external pull-ups. Unused inputs must be tied to VCC or GND to prevent floating conditions and ensure reliable operation.

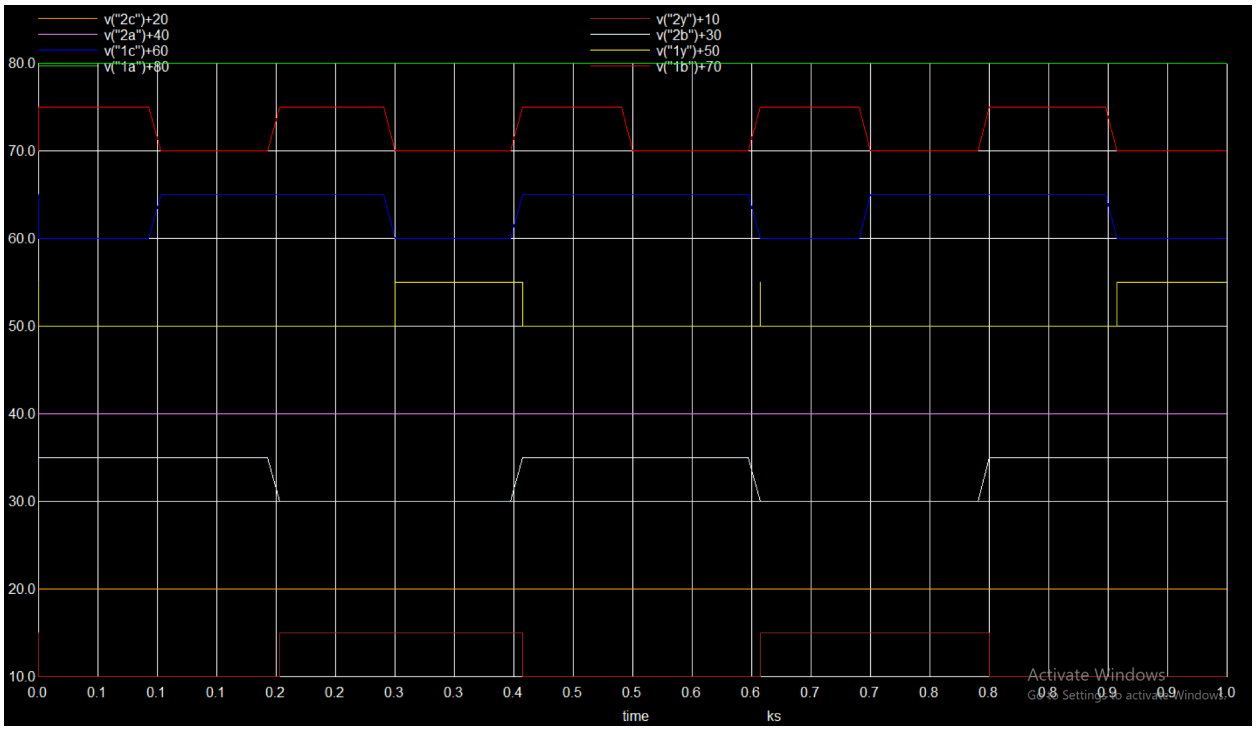
8.2 Pin Diagram



8.3 Schematic diagram



8.4 Simulation Output



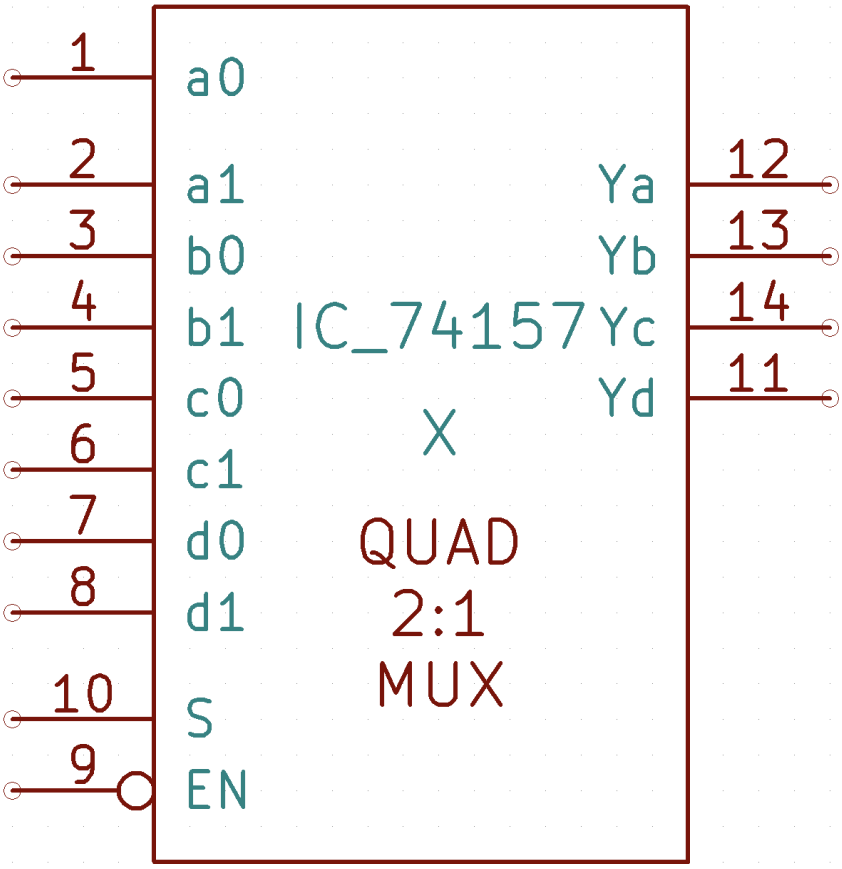
Chapter 9

IC 74HC157

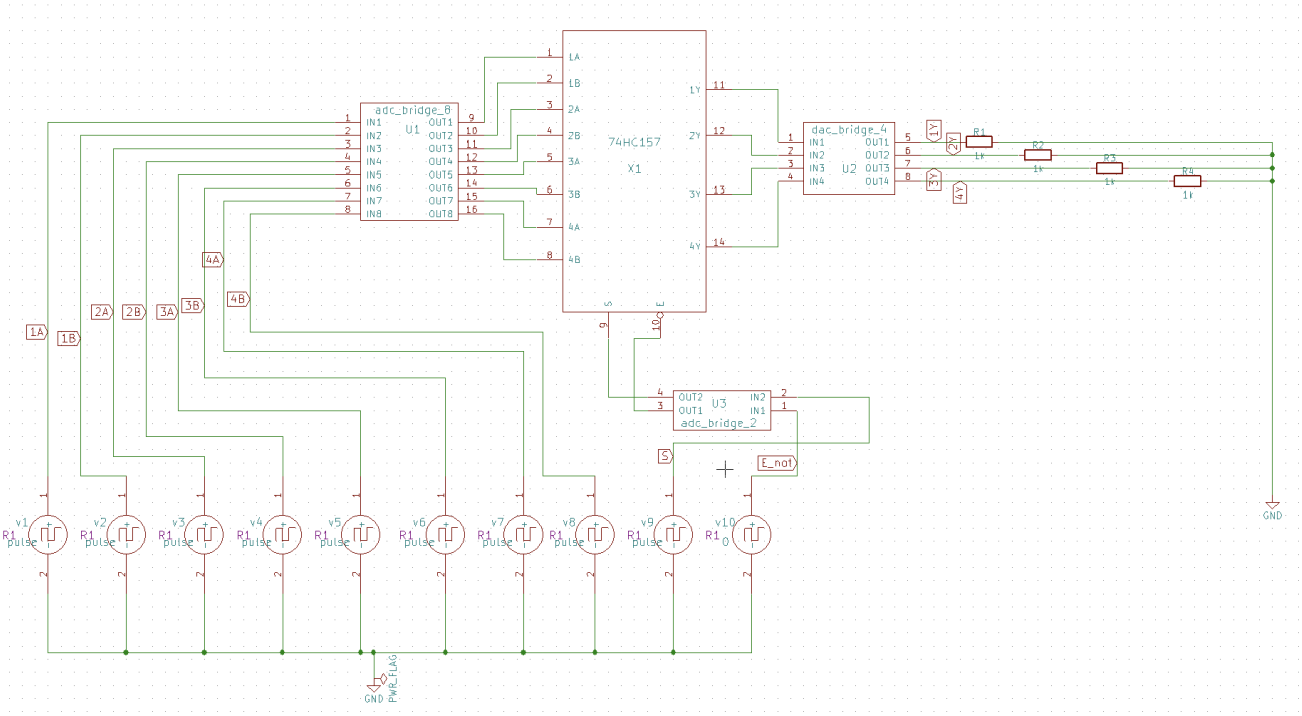
9.1 Circuit Details

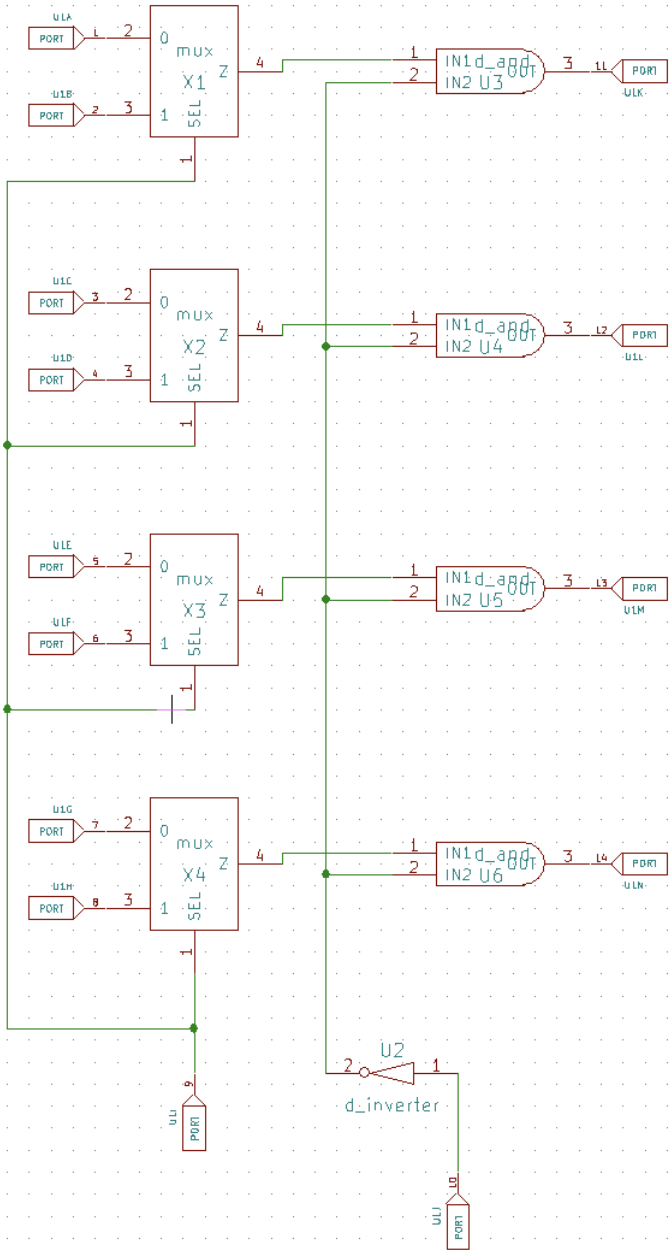
The SN74HC157 is a quad 2-input data selector/multiplexer that routes one of two 4-bit data sources (A0–A3 or B0–B3) onto its four outputs (Y0–Y3) under control of a single common select input (S). An active-LOW enable ($\overline{E}$) input forces all outputs LOW when asserted, allowing easy gating of the entire bus. Internally, each channel consists of a pair of transmission-gate switches that pass the selected input directly to the output, ensuring rail-to-rail logic levels and low propagation delay. The outputs are non-inverting, and because the device is fully static CMOS, it does not require a minimum clock rate or refresh. The SN74HC157 operates from 2 V to 6 V (VCC on pin 16, GND on pin 8) and exhibits typical propagation delays around 10 – 15 ns at VCC = 5 V, making it well suited for high-speed bus-switching and multiplexing in digital systems.

9.2 Pin Diagram



9.3 Schematic diagram

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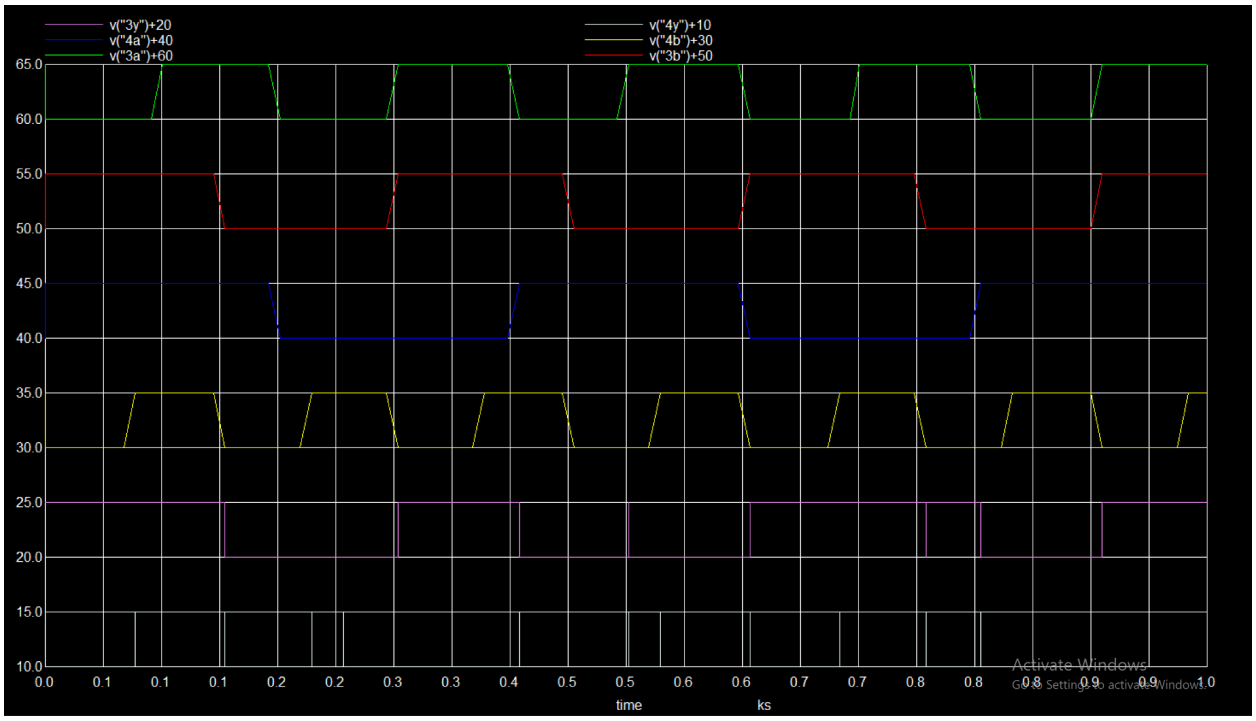
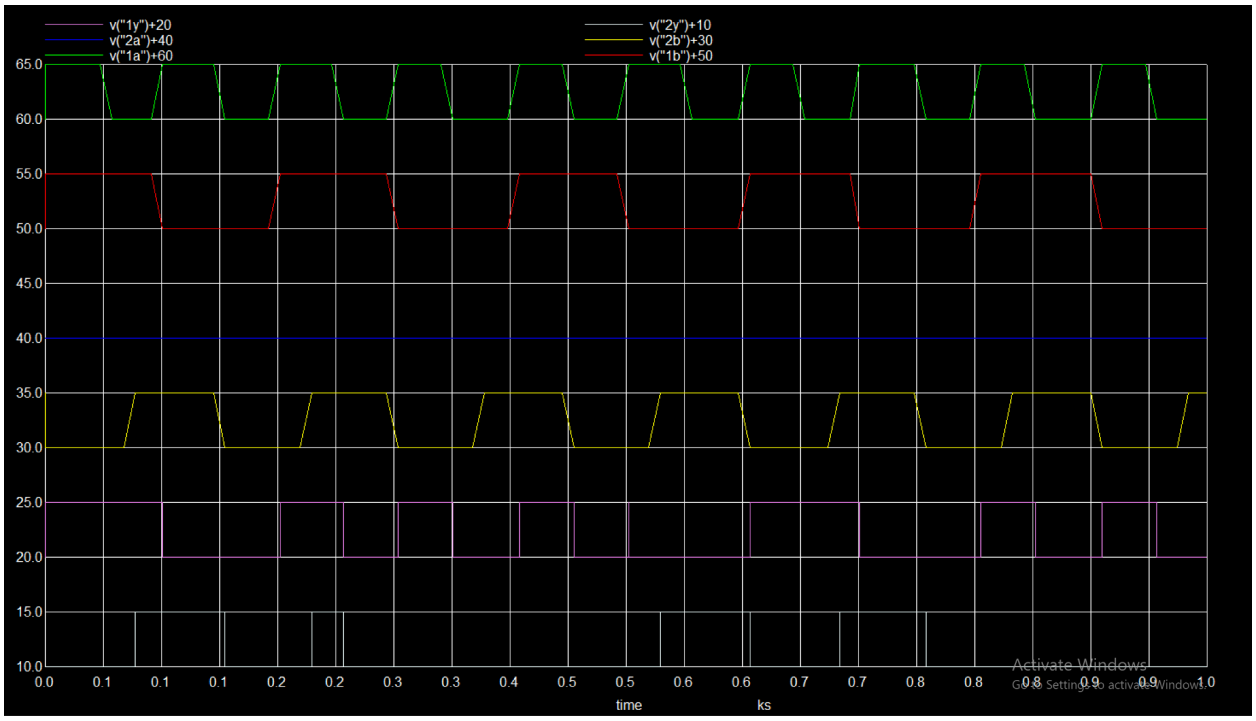
2
U1B
PORT
2
3
0
mux
X1
Z
1
SEL
4
1
IN1 d_and
IN2 U3
OUT
2
3
L1
PORT
U1K
1
U1C
PORT
3
2
U1D
PORT
4
3
0
mux
X2
Z
1
SEL
4
1
IN1 d_and
IN2 U4
OUT
2
3
L2
PORT
U1L
1
U1E
PORT
5
2
U1F
PORT
6
3
0
mux
X3
Z
1
SEL
4
1
IN1 d_and
IN2 U5
OUT
2
3
L3
PORT
U1M
1
U1G
PORT
7
2
U1H
PORT
8
3
0
mux
X4
Z
1
SEL
4
1
IN1 d_and
IN2 U6
OUT
2
3
L4
PORT
U1N
1
U2
2
1
d_inverter
9
U1
PORT
10
U1J
PORT

9.4 Simulation Output





Conclusion

Through this internship, we have successfully leveraged eSim's schematic-capture and waveform-analysis capabilities to design, simulate, and validate eight key 74HC-series integrated circuits: the 4-bit up/down counter (74HC193), 8-bit serial-in/parallel-out shift register (74HC595), 14-stage ripple counter (74HC4020), quad bus buffer (74HC125), quad D-flip-flop register (74HC175), quad XOR gate (74HC86), triple 3-input NOR gate (74HC27), and quad 2-to-1 multiplexer (74HC157). Each device was instantiated, stimulus-driven, and its dynamic behavior observed under realistic timing and loading conditions. By methodically stacking, offsetting, and analyzing their waveforms in a single or multiple plot windows, we confirmed correct logic functionality, timing margins, and cascading capability. The project has not only demonstrated the versatility of eSim for both digital and mixed-signal workflows, but also solidified our understanding of synchronous design principles, bus-expansion techniques, and gate-level logic integration—all without the expense or turnaround time of physical prototyping.

Future Scope

1. **Physical Layout and Parasitics**

   Transition from schematic simulation to PCB- or ASIC-level layout within eSim (or an integrable CAD flow) to study the effects of interconnect capacitance, crosstalk, and power distribution on timing and signal integrity.

2. **Process-Technology Modeling**

   Incorporate technology-specific SPICE models (TSMC, GlobalFoundries) to simulate device variability, leakage currents, and temperature dependence, thereby bridging the gap toward real silicon.

3. **Mixed-Signal Extensions**

   Enhance the testbench by adding analog front-ends—such as phase-locked loops (PLLs) driven by the 74HC4020 divider or voltage-controlled oscillators using LM566 models—to validate system-level interactions.

4. **Automation and Regression Testing**

   Develop Python or Tcl scripts to automate batch simulations, waveform extraction, and pass/fail criteria checks, establishing a regression-ready flow for rapid design iterations.

5. **FPGA Prototyping**

   Map the HDL equivalents of the 74HC-series designs onto an FPGA platform to measure real-world performance, validate timing closure, and explore dynamic reconfiguration for educational demos.

6. **Power-Optimization Studies**

   Perform dynamic and static power analysis under different clock rates and supply voltages to identify low-power operating points, investigate clock-gating strategies, and quantify energy per switching event.

By pursuing these extensions, we can evolve from proof-of-concept simulations to a robust, technology-aware design methodology—paving the way for future VLSI and mixed-signal system development.

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