



Winter Internship Report

On

Integrated Circuit Design using Subcircuit feature of eSim

Submitted by

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I also sincerely appreciate the entire FOSSEE initiative for its efforts in empowering students and researchers by making tools freely accessible, thus removing the barriers imposed by costly commercial software. This mission not only fosters innovation but also strengthens the open-source ecosystem, allowing young learners to actively contribute and grow.

This internship has been a memorable and rewarding phase of my academic journey. The knowledge, skills, and experiences I have gained will undoubtedly serve as a strong foundation as I move forward in my career in the semiconductor and VLSI domain.

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Chapter 1

Introduction

The advancement of Electronic Design Automation (EDA) tools has revolutionized the way electronic circuits are designed, simulated, and verified. Among these, open-source tools play a crucial role in making advanced EDA capabilities accessible to students, educators, and researchers without the burden of expensive licenses. The FOSSEE project at IIT Bombay has taken significant steps to promote such open-source tools globally.

One of the key open-source tools developed and promoted under FOSSEE is **eSim**, which integrates multiple open-source EDA tools to provide a unified platform for circuit design, simulation, and PCB layout. Various tools like NgSpice, Makerchip, and KiCad work together under eSim to offer a complete design environment.

1.1 eSim

eSim is an open-source Electronic Design Automation (EDA) tool developed by FOSSEE, IIT Bombay. The primary objective of eSim is to provide a completely free and open-source alternative to commercial circuit design and simulation software, thereby reducing dependency on expensive proprietary tools in academia and research.

eSim integrates multiple open-source tools to provide a comprehensive design and simulation environment. **KiCad** is used for schematic capture and PCB design, while **NgSpice** performs analog circuit simulation. For digital simulation, **GHDL** is integrated, supporting VHDL based designs, and **Makerchip** enables online Transaction Level Verilog (TL-Verilog) based digital design and verification. Python support is also available in eSim, allowing users to perform customized simulations, generate netlists.

One of the key features of eSim is its **Subcircuit feature**, which allows complex designs to be modularized into reusable blocks, simplifying the design of large systems. Additionally, eSim supports device modeling, enabling users to define and simulate custom semiconductor devices using real-world parameters. As part of its continuous development, eSim also supports **SkyWater SKY130 PDK**, allowing users to perform simulations using an open-source 130nm Process Design Kit, which is widely used for analog, mixed-signal, and digital IC design research.

By supporting a fully open-source toolchain, eSim empowers students, educators, and researchers to gain hands-on experience with industry-relevant EDA tools and contribute actively to the open-source hardware ecosystem.

1.1.1 NgSpice

NgSpice is an open-source circuit simulator integrated into eSim for performing analog and mixed-signal simulations. Based on the SPICE simulation engine, NgSpice supports DC, AC, transient, and parametric analyses, making it suitable for analyzing a wide range of circuits.

It allows users to simulate circuit behavior using industry-standard SPICE models, including support for subcircuits and behavioral modeling. In eSim, NgSpice works as the backend simulator for schematics created using KiCad, providing waveform outputs for voltage, current, and frequency responses. Its flexibility and accuracy make it a powerful tool for verifying designs before hardware implementation.

1.1.2 Makerchip

Makerchip is an integrated platform designed to simplify digital circuit design by offering both browser-based and desktop-based environments for coding, simulating, and debugging digital hardware designs. It supports multiple hardware description languages including Verilog, SystemVerilog, and Transaction-Level Verilog (TL-Verilog), allowing flexibility for users at various levels of expertise.

In eSim, Makerchip is interfaced through a Python-based application called Makerchip-App, which seamlessly launches the Makerchip IDE for digital design and verification. The platform integrates several open-source and proprietary tools to provide a rich set of features such as real-time simulation, waveform viewing, and code linting, thereby improving design accuracy and productivity.

1.1.3 KiCad

KiCad is an open-source PCB design and schematic capture tool integrated within eSim for creating circuit schematics and generating PCB layouts. It allows users to design multi-layer boards, define custom footprints, and perform design rule checks to ensure design correctness before fabrication.

In eSim, KiCad acts as the primary schematic editor, allowing users to graphically build circuits by placing and interconnecting components from extensive open-source libraries. The designed schematics can directly be used for both simulation and PCB layout generation. KiCad also supports features such as 3D visualization of PCBs, Gerber file export for manufacturing, and electrical rule checking to identify design issues early. Its seamless integration within eSim enables a smooth transition from schematic design to simulation and physical realization, offering a complete design-to-fabrication workflow entirely within an open-source environment.

1.1.4 GHDL

GHDL is an open-source simulator for VHDL, a hardware description language widely used in digital circuit design. It supports the complete IEEE VHDL standard, allowing designers to simulate, verify, and debug VHDL-based digital systems effectively.

In eSim, GHDL is integrated to enable digital simulation alongside analog simulation provided by NgSpice. Users can model digital circuits using VHDL, which are then simulated using GHDL to verify logical functionality and timing behavior. This integration allows eSim to handle mixed-signal designs, where the analog components are simulated by NgSpice and the digital components by GHDL, providing a comprehensive platform for complex system design. The combination of these tools allows designers to validate both analog and digital subsystems within a unified simulation environment.

Chapter 2

Features of eSim

eSim offers a comprehensive set of features that make it a powerful open-source alternative for electronic design automation. Some of the key features include:

- **Open-source and Free:** eSim is fully open-source, allowing unrestricted access without licensing costs, making it ideal for academic and research purposes.
- **Integrated Toolchain:** Combines multiple open-source tools such as KiCad for schematic capture and PCB design, NgSpice for analog simulation, GHDL for digital simulation, and Makerchip for advanced digital design.
- **Mixed-Signal Simulation:** Supports both analog and digital simulation, allowing users to design and simulate mixed-signal circuits efficiently.
- **Subcircuit Feature:** Enables hierarchical and modular design by allowing complex circuits to be broken into reusable subcircuits.
- **Device Modeling:** Supports custom device modeling, allowing users to simulate real-world semiconductor devices using user-defined parameters.
- **SkyWater SKY130 PDK Support:** Provides access to open-source 130nm process design kit for IC design and simulation.
- **Python Integration:** Allows automation, scripting, and advanced analysis using Python interfaces.
- **User-Friendly Interface:** Offers an intuitive GUI that simplifies circuit creation, simulation setup, and result analysis, making it suitable for both beginners and advanced users.
- **Cross-Platform Support:** Compatible with major operating systems like Linux and Windows.
- **Active Community and Documentation:** Extensive documentation, tutorials, and community support provided through FOSSEE ensure smooth learning and troubleshooting.

Chapter 3

Problem Statement

To design, develop and test various Analog and Digital Integrated Circuit Models using the sub-circuit feature in eSim and create Device Models using the Model Editor tool. These subcircuits are to be built using the device models already present in the eSim library. After successful testing of these IC models and their integration into the eSim subcircuit library, these models would be useful in the future for circuit designing purposes.

3.1 Subcircuit Design and Integration

Digital ICs are modeled as subcircuits based on datasheet specifications and integrated into eSim's subcircuit library.

3.1.1 Approach

- **Datasheet Analysis:** The primary step is to browse through various analog and digital IC datasheets, and hence find suitable circuits to implement in eSim, that are not previously included into the eSim library. Check for the detailed schematic of the IC's and once the component values and the truth table is ascertained, then finalise the IC to be created.
- **Subcircuit Creation:** After deciding the IC, we start modeling it as a sub-circuit in eSim, using the model files present in the eSim device model library only. The design is strictly according to the information given in the official data-sheets of the ICs. This step also includes building the Symbol/Pin diagram of the IC according to the packaging and pin description given in the data-sheets only
- **Symbol Creation:** Custom IC symbols are created according to package type and pin configuration for correct circuit integration.
- **Test Circuit Design:** Once the component of the IC is ready, now we can build the test circuits, according to the data-sheets. In this step we build the test cases and test circuits using the component IC
- **Simulation and Validation:** Once the test circuits are ready, now it's time to simulate the test circuits so that the output can be obtained in the form

of wave-forms and plots. Here we take help of KiCad to NgSpice conversion and Simulation feature in eSim. If the output of the test circuit is not as per expectation, this implies that the test case has failed, and there is some error in the schematic. In such cases we go back to the design phase of the IC or the test circuits, to look for possible errors and then repeat the testing process again after making required changes. Once the expected output of the test cases are correct and satisfy the expected results, then in such a case the IC is declared successfully working. The test case has been verified and the designing process is complete.

Chapter 4

Digital IC's

The Subcircuit feature of eSim allows hierarchical modeling of complex Integrated Circuits by combining multiple basic components into a single reusable block. By utilizing datasheets and internal schematics of various ICs, accurate subcircuit models are created using eSim's schematic editor.

4.1 74HCT165 - 8-bit parallel-in/serial-out shift register

Description: The 74HC/HCT165 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A. The 74HC/HCT165 are 8-bit parallel-load or serial-in shift registers with complementary serial outputs (Q_7 and \bar{Q}_7) available from the last stage. When the parallel load (PL) input is LOW, parallel data from the D0 to D7 inputs are loaded into the register asynchronously

When PL is HIGH, data enters the register serially at the Ds input and shifts one place to the right ($Q_0 \rightarrow Q_1 \rightarrow Q_2, \text{etc.}$) with each positive-going clock transition. This feature allows parallel-to-serial converter expansion by tying the Q_7 output to the DS input of the succeeding stage.

4.1.1 IC Layout

This figure represents the Pin Package Diagram of 74HCT165 ic

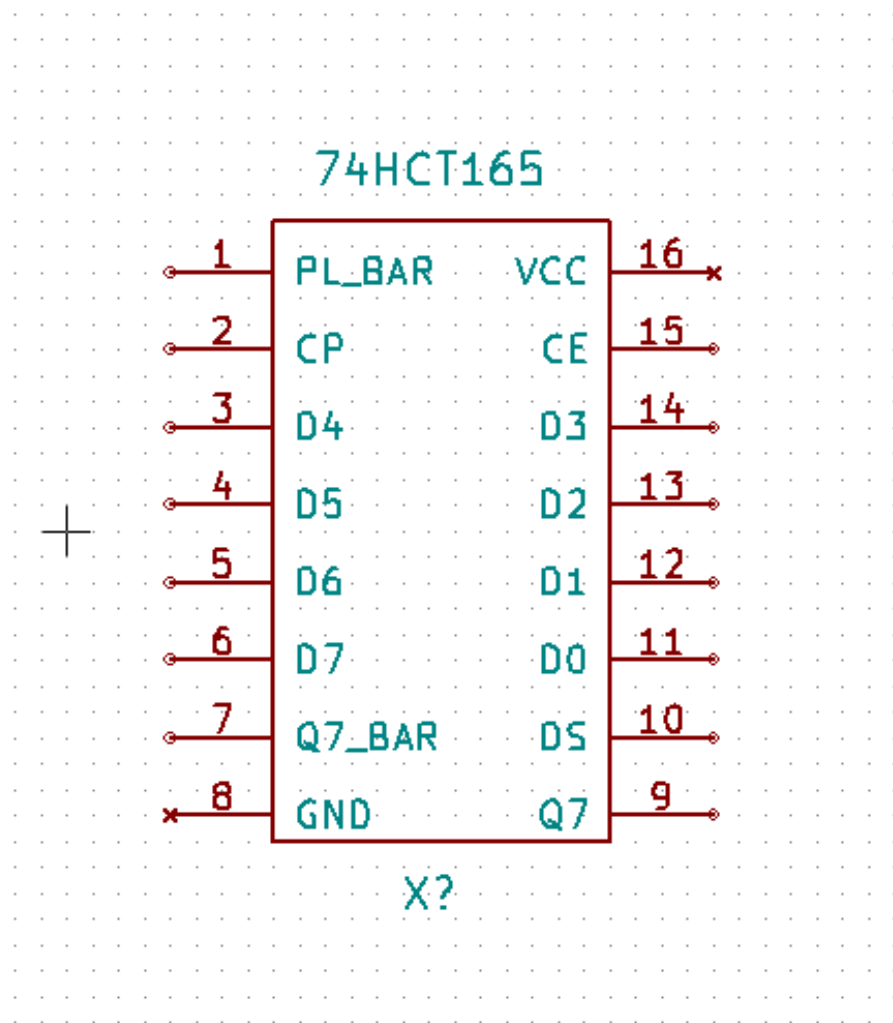


Figure 4.1: Pin diagram of 74HCT165

4.1.2 Subcircuit Schematic Diagram 74HCT165

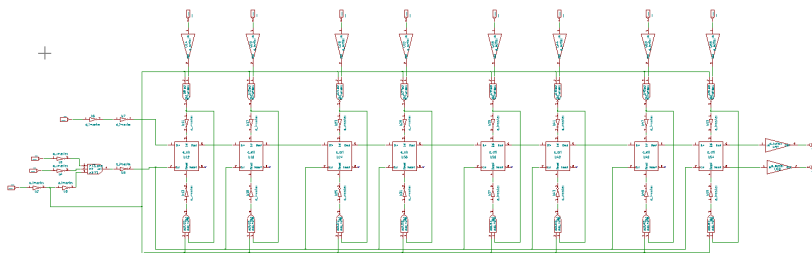


Figure 4.2: Subcircuit Schematic Diagram of 74HCT165

4.1.3 Test Circuit

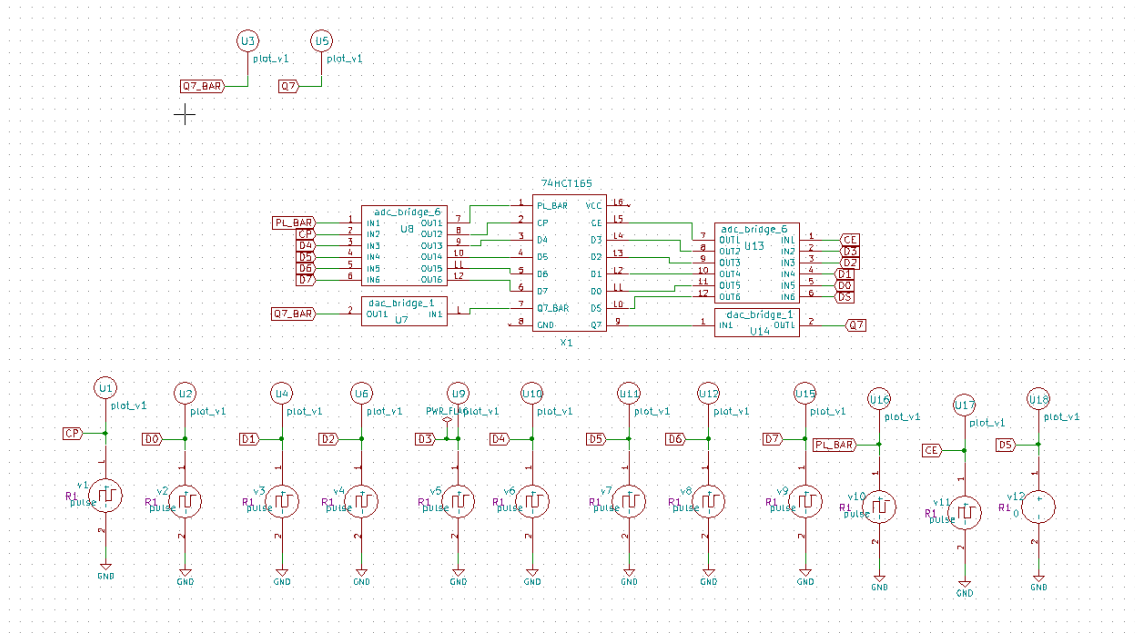


Figure 4.3: Test Circuit of 74HCT165

4.1.4 Input Plots

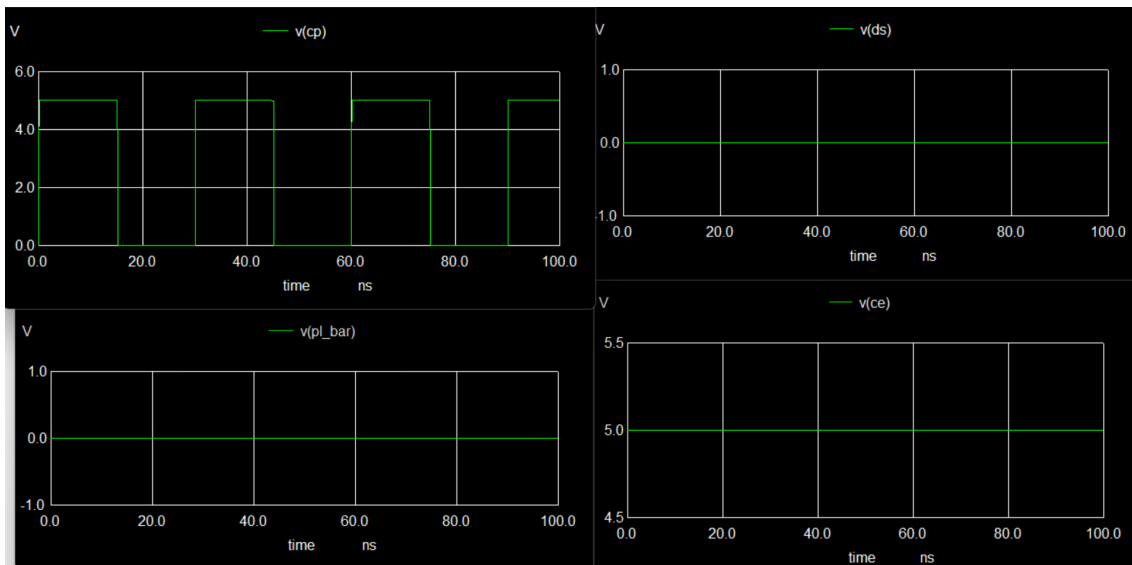


Figure 4.4: Input Plots Waveform of 74HCT165

4.1.5 Output Plots

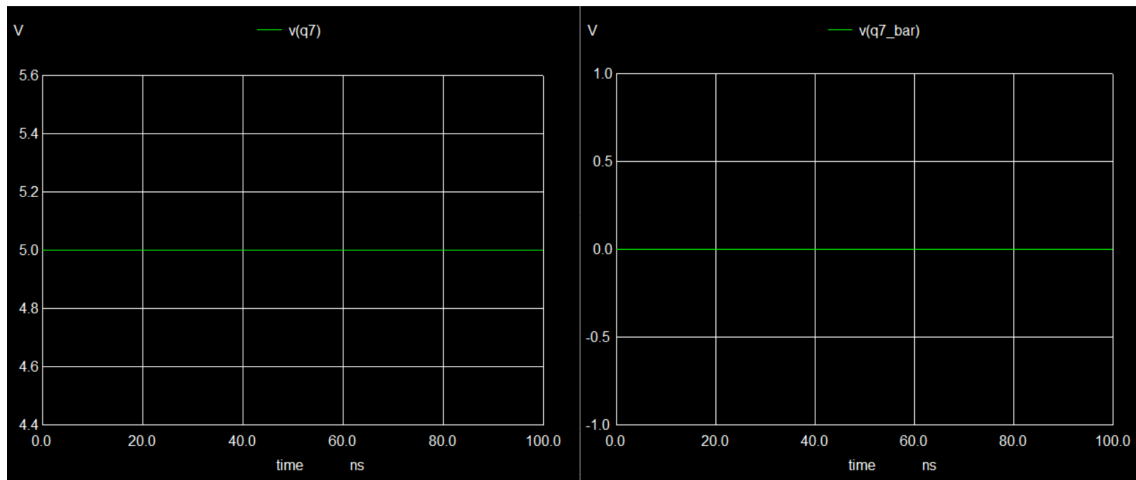


Figure 4.5: Output Voltage Waveform of 74HCT165

4.2 74141 - 1-of-10 Decoder/Driver (Nixie) with open-collector output

Description: The 74141 is a 1-of-10 BCD-to-decimal decoder/driver with open-collector outputs that accepts 4-bit BCD inputs from all TTL circuits. It is specifically designed to produce the correct output selection to directly drive gas-filled cold-cathode indicator tubes that require 7.0 mA or less of cathode current. To ensure a stable display, the IC incorporates design improvements that minimize switching transients. The device features ten high-performance, npn output transistors with a maximum reverse current of 50 μ A at 55 V, and it operates with a typical power dissipation of 55 mW. Additionally, for binary inputs 10 through 15, the outputs remain OFF, allowing these invalid codes to be utilized for blanking leading or trailing-edge zeros in visual displays.

4.2.1 IC Layout

This figure represents the Pin Package Diagram of 74141 ic

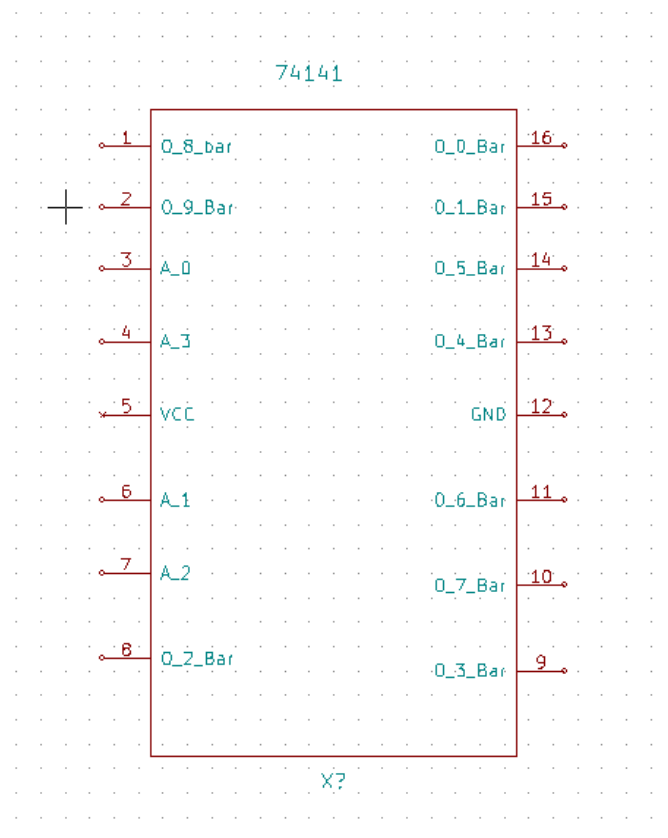


Figure 4.6: Pin diagram of 74141

4.2.2 Subcircuit Schematic Diagram 74141

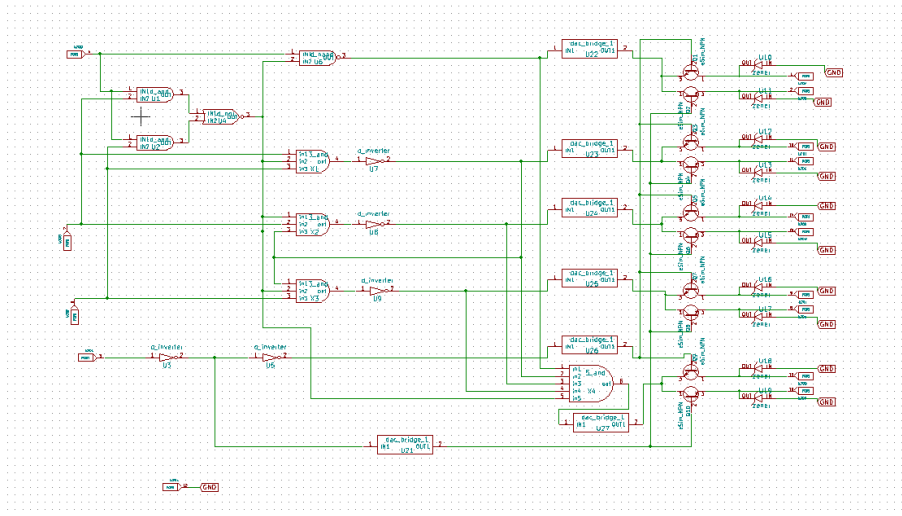


Figure 4.7: Subcircuit Schematic Diagram of 74141

4.2.3 Test Circuit

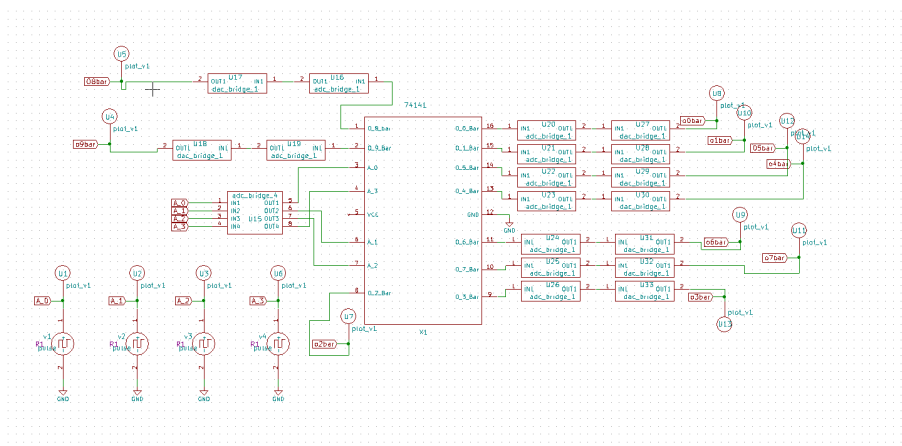


Figure 4.8: Test Circuit of 74141

4.2.4 Input Plots

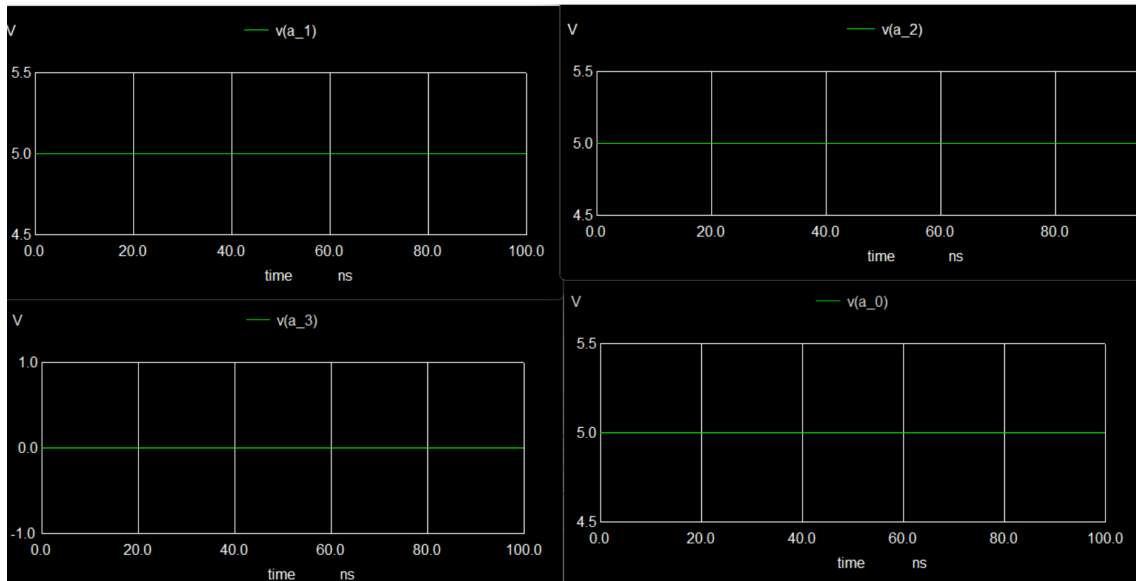


Figure 4.9: Input Plots Waveform of 74141

4.2.5 Output Plots

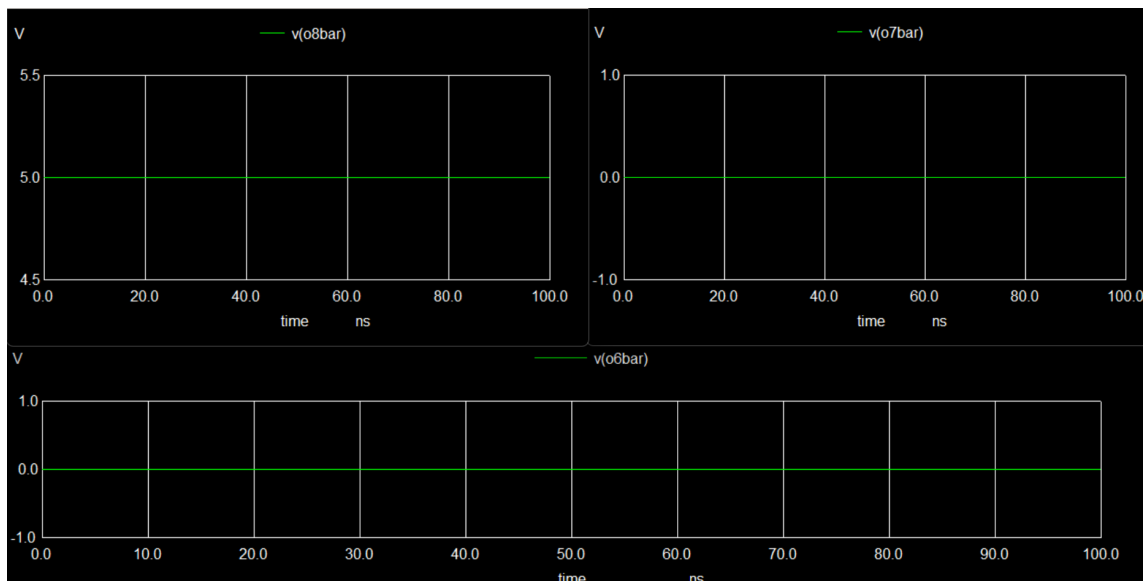


Figure 4.10: Output Voltage Waveform of 74141

4.3 74F280B - 9-bit odd/even parity generator/checker

Description: The 74F280B is a 9-bit Parity Generator or Checker commonly used to detect errors in high speed data transmission or data retrieval systems. Both Even (E) and Odd (O) parity outputs are available for generating or checking even or odd parity on up to 9 bits. The Even (E) parity output is High when an even number of Data inputs (I0 - I8) are High. The Odd (O) parity output is High when an odd number of Data inputs are High. Expansion to larger word sizes is accomplished by tying the Even (E) outputs of up to nine parallel devices to the data inputs of the final stage. This expansion scheme allows an 81-bit data word to be checked in less than 20ns.

4.3.1 IC Layout

This figure represents the Pin Package Diagram of 74F280B ic

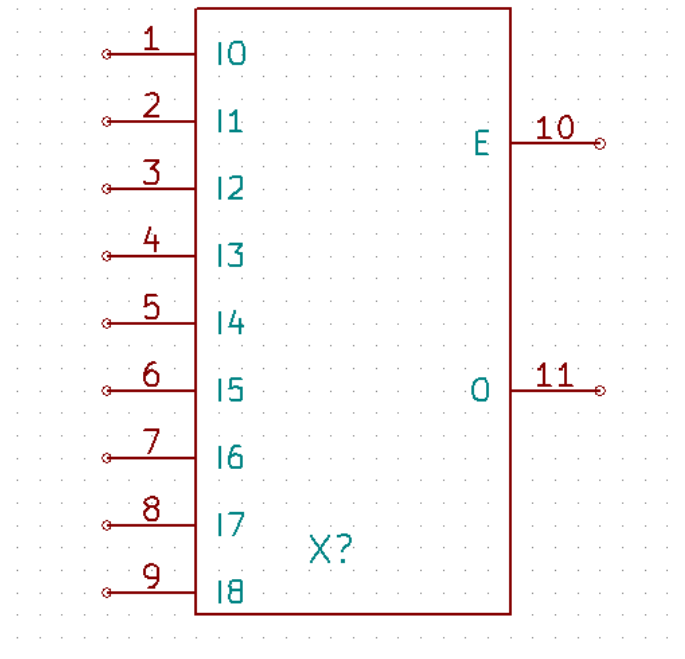


Figure 4.11: Pin diagram of 74F280B

4.3.2 Pin Diagram Schematic Diagram 74F280B

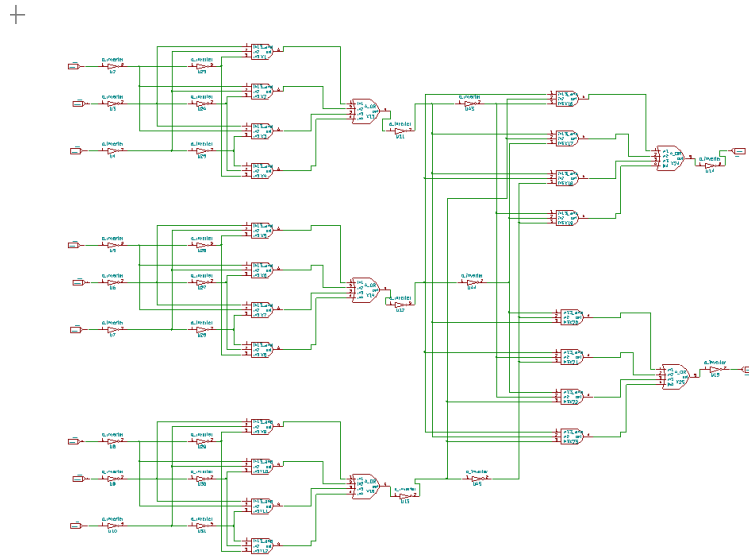


Figure 4.12: Subcircuit Schematic Diagram of 74F280B

4.3.3 Test Circuit

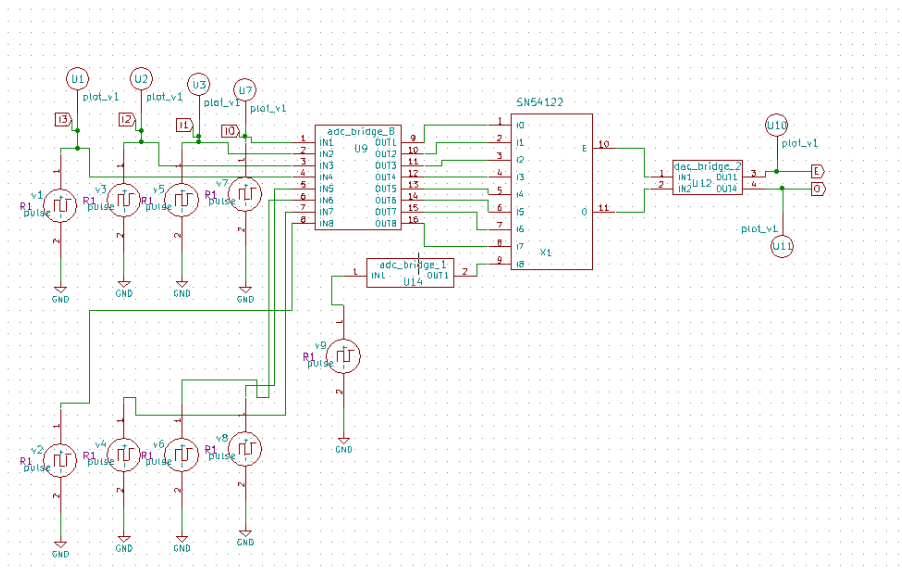


Figure 4.13: Test Circuit of 74F280B

4.3.4 Input Plots

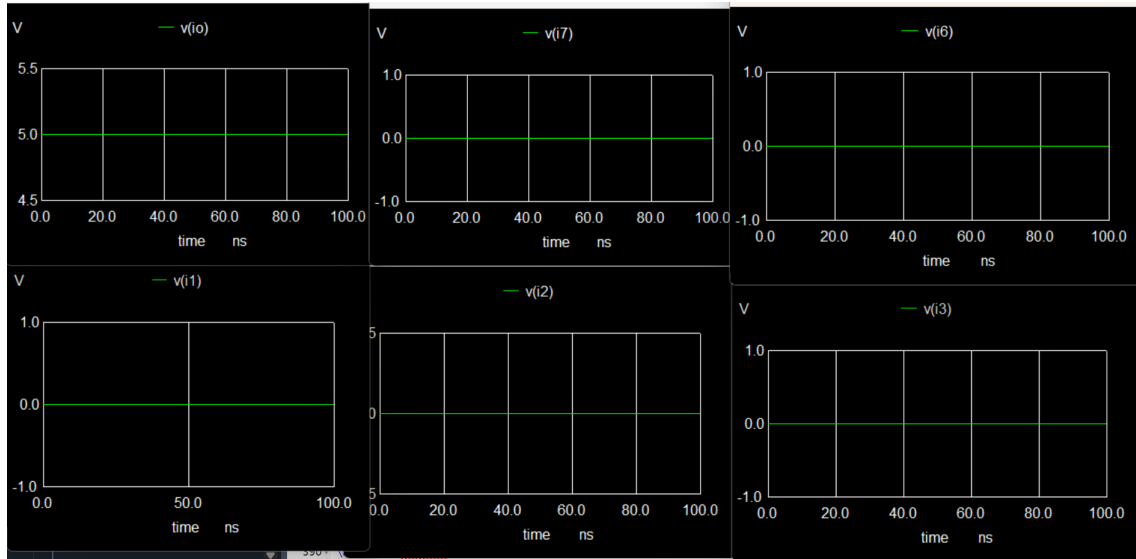


Figure 4.14: Input Plots Waveform of 74F280B

4.3.5 Output Plots

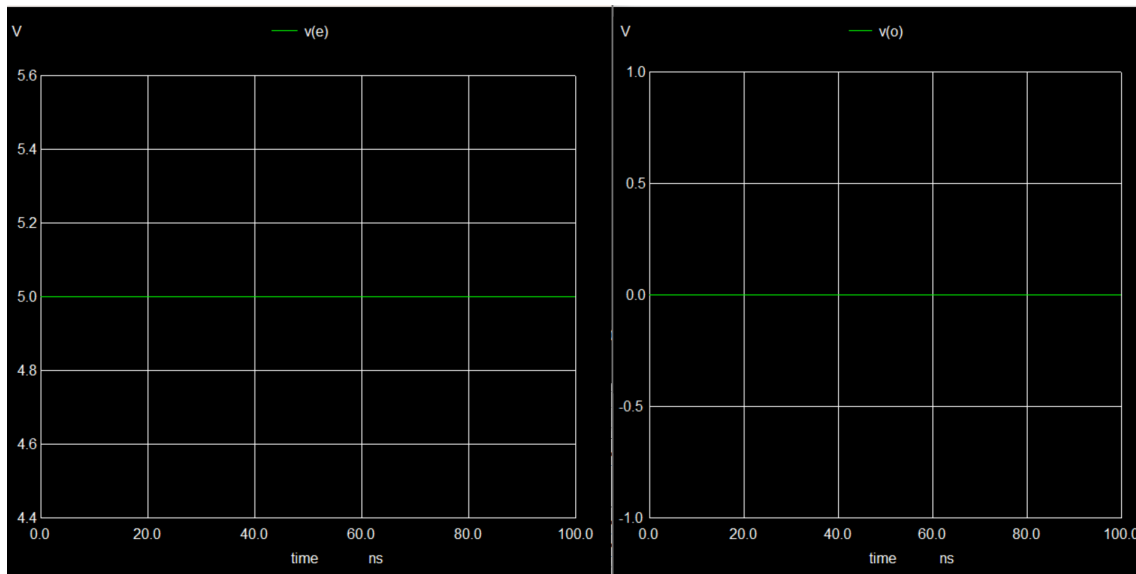


Figure 4.15: Output Voltage Waveform of 74F280B

4.4 SN54190 - SYNCHRONOUS UP/DOWN COUNTERS WITH DOWN/UP MODE CONTROL

Description: The SN54190/191 and SN74LS190/191 are synchronous up/down counters designed for reliable counting in BCD or binary formats. They operate with all flip-flops clocked simultaneously, eliminating timing errors common in ripple counters and ensuring stable synchronous performance. The counting direction is controlled by the up/down input, while the enable input allows counting only when active. These counters are fully programmable, letting users preset values through parallel data inputs using the load control. They also provide ripple clock and maximum/minimum outputs to support easy cascading of multiple counters for larger counting applications. With buffered control inputs and efficient design, they reduce drive requirements and are suitable for high-speed digital systems.

4.4.1 IC Layout

This figure represents the Pin Package Diagram of SN54190 ic

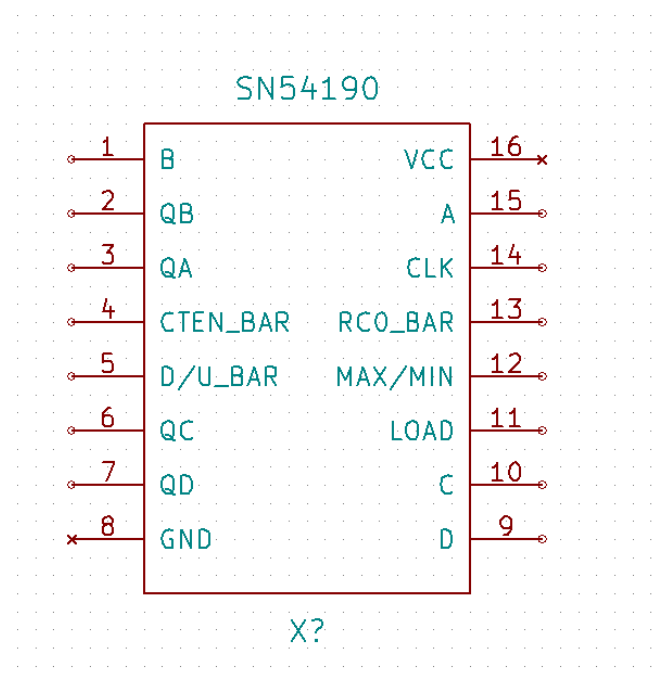


Figure 4.16: Pin diagram of SN54190

4.4.2 Subcircuit Schematic Diagram SN54190

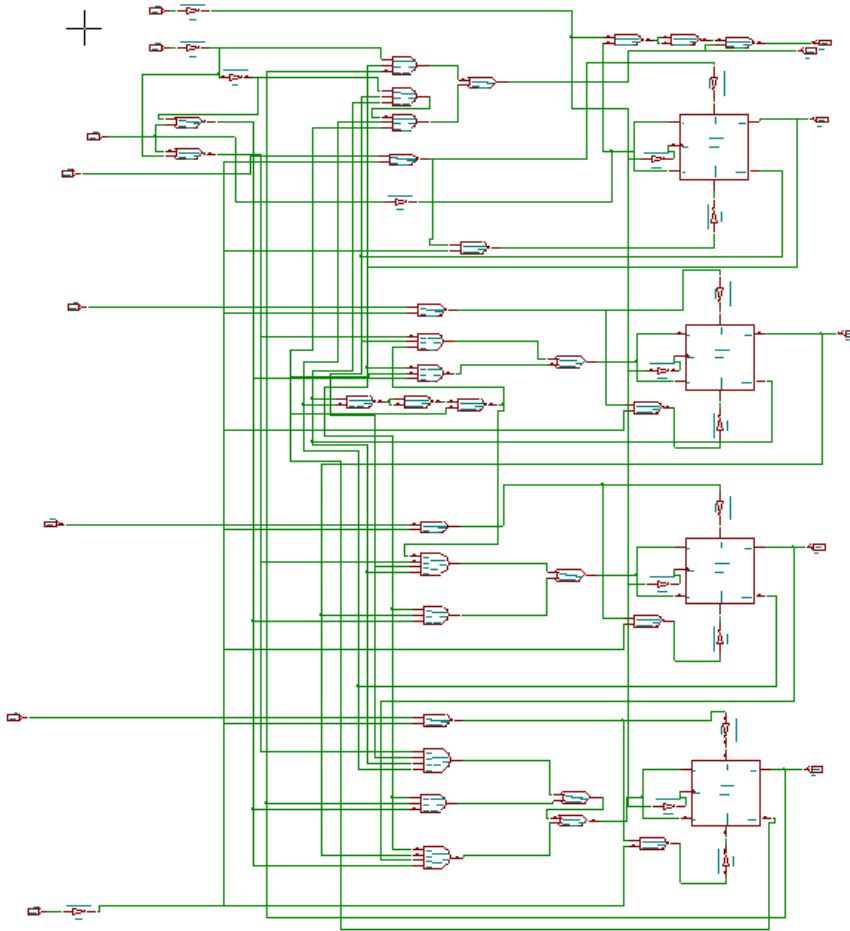


Figure 4.17: Subcircuit Schematic Diagram of SN54190

4.4.3 Test Circuit

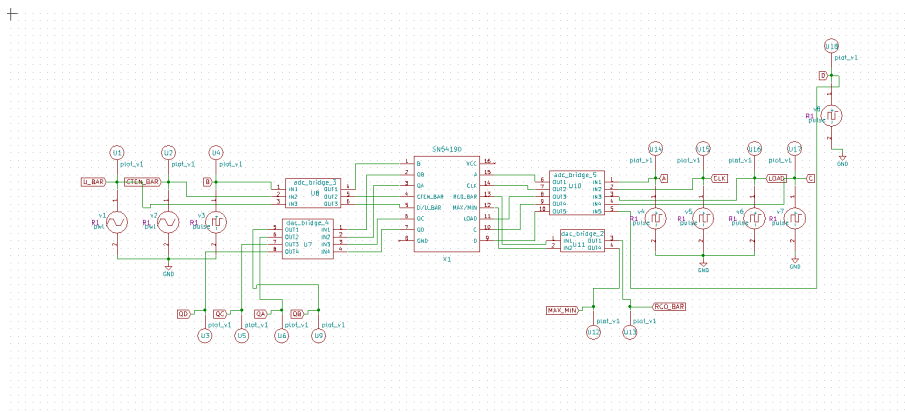


Figure 4.18: Test Circuit of SN54190

4.4.4 Input Plots

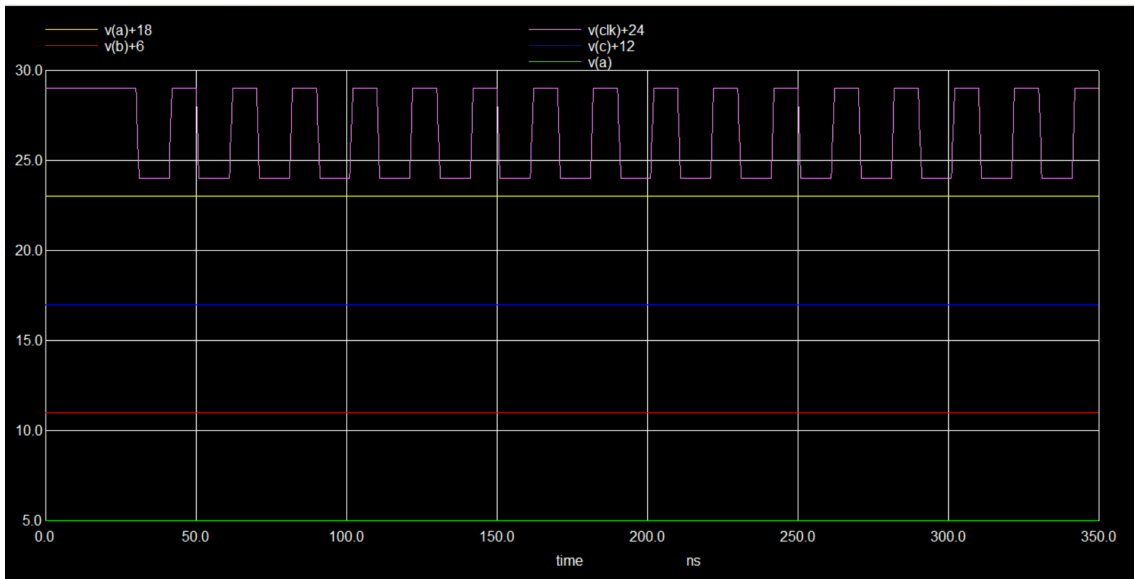


Figure 4.19: Input Plots Waveform of SN54190

4.4.5 Output Plots

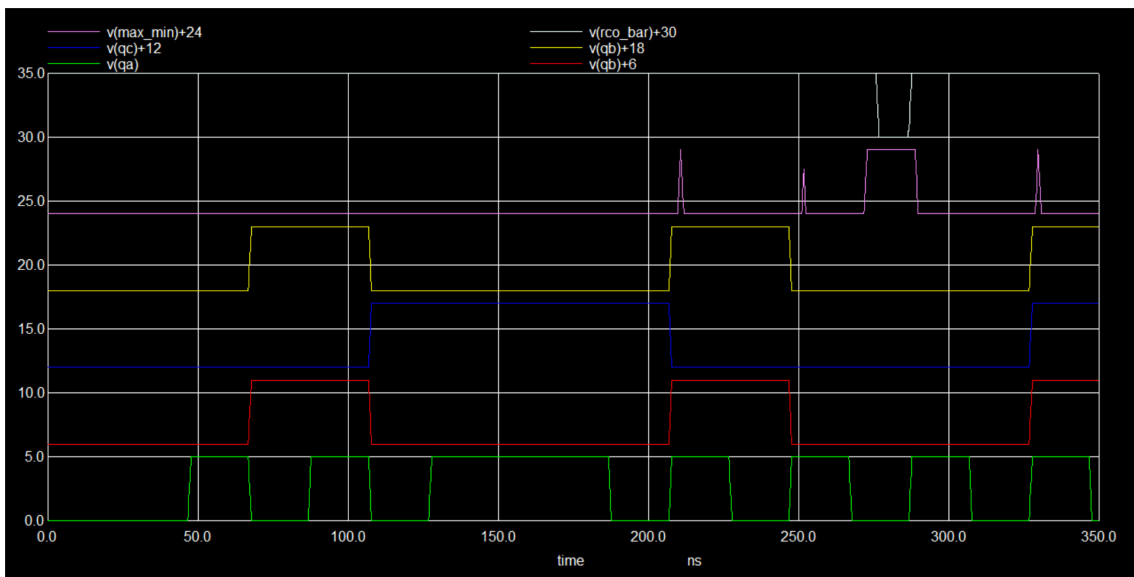


Figure 4.20: Output Voltage Waveform of SN54190

Chapter 5

Analog IC's

5.1 ULN2804 - EIGHT HIGH VOLTAGE, HIGH CURRENT DARLINGTON ARRAYS

Description: The ULN2804 is a high voltage, high current Darlington array comprised of eight NPN Darlington pairs. The device features open-collector outputs with suppression diodes for inductive loads and is ideally suited for interfacing between low-level logic circuitry and high power loads. Typical loads including relays DC motors, filament lamps, LED displays, printer hammers and high power buffers.

5.1.1 IC Layout

This figure represents the Pin Package Diagram of ULN2804 ic

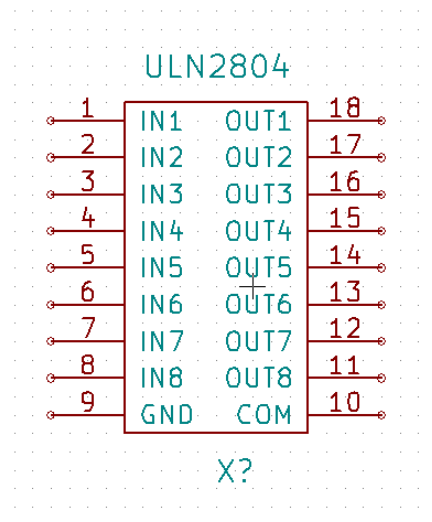


Figure 5.1: Pin diagram of ULN2804

5.1.2 Subcircuit Schematic Diagram ULN2804

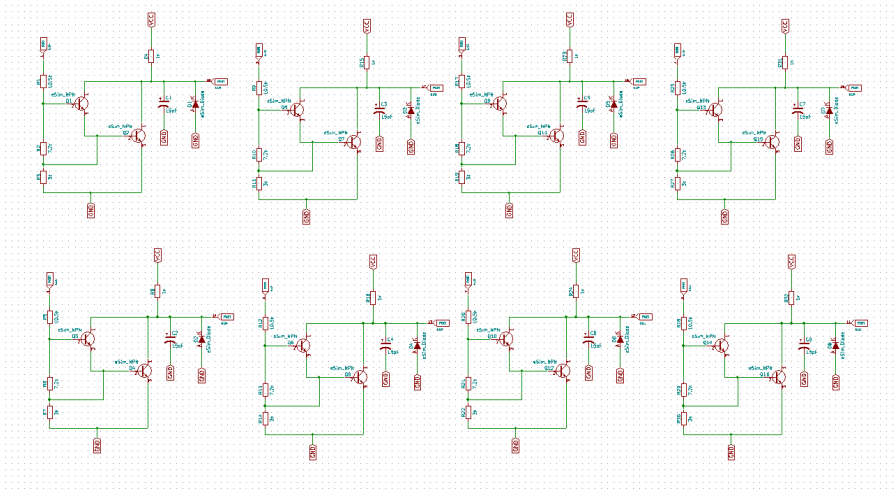


Figure 5.2: Subcircuit Schematic Diagram of ULN2804

5.1.3 Test Circuit

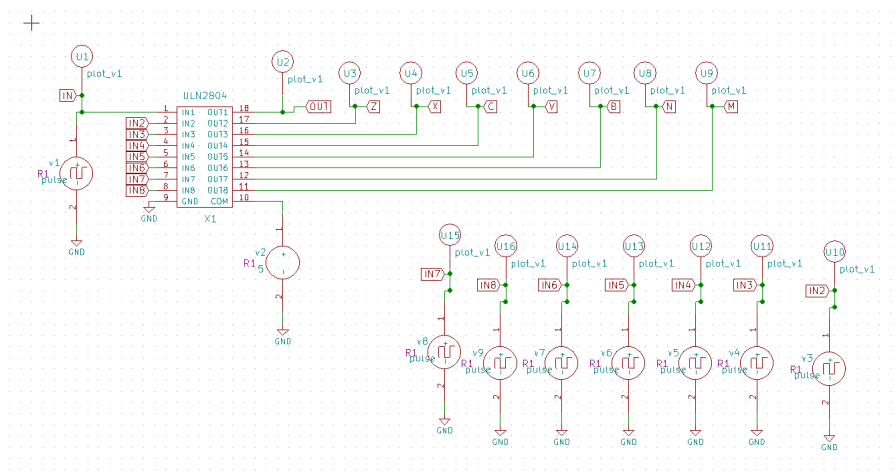


Figure 5.3: Test Circuit of ULN2804

5.1.4 Input Plots

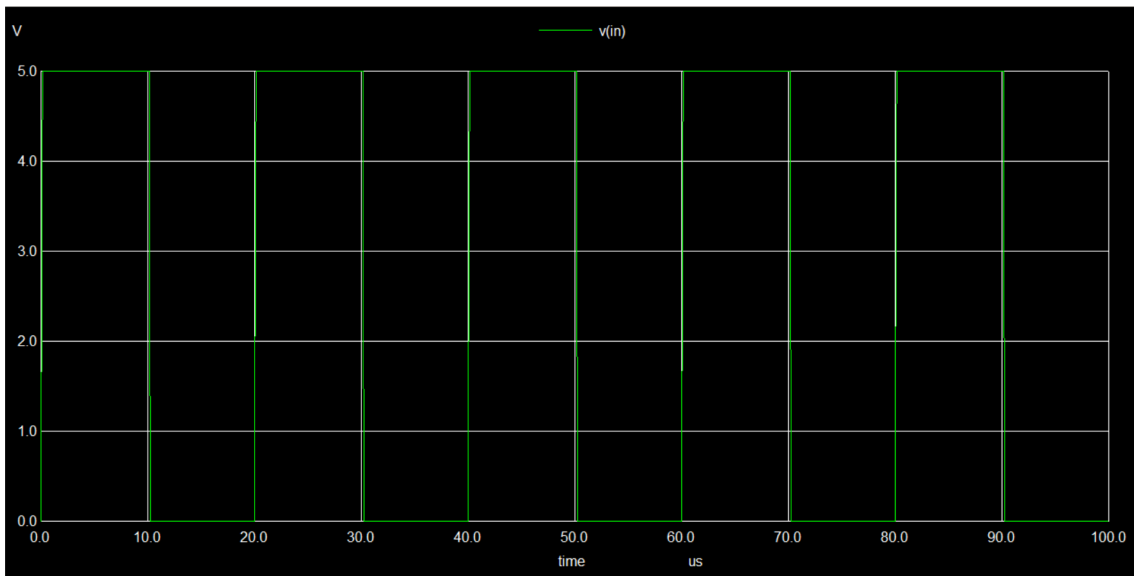


Figure 5.4: Input Plots Waveform of ULN2804

5.1.5 Output Plots

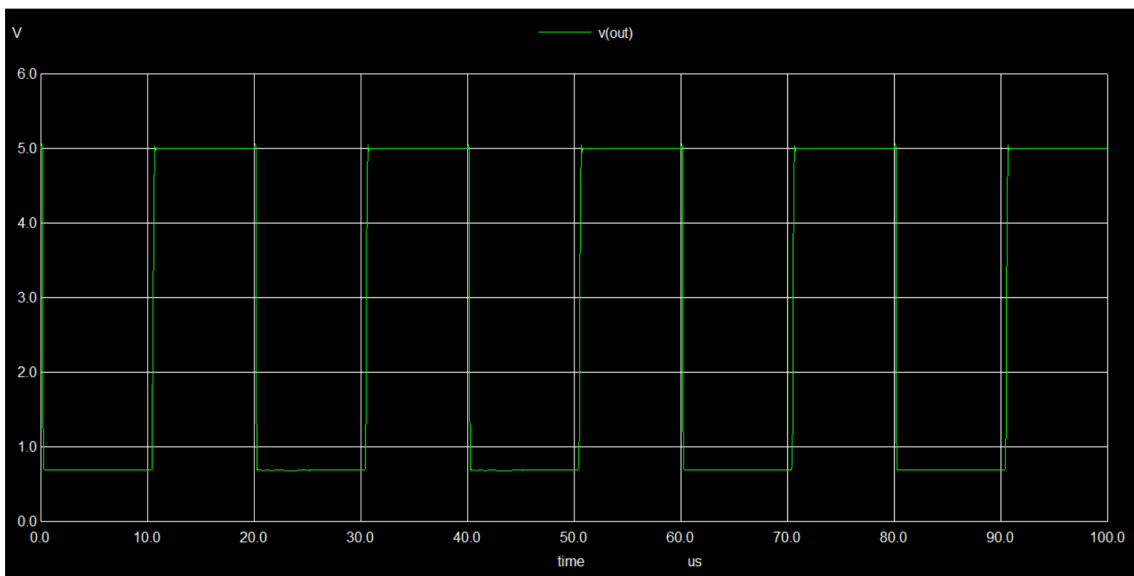


Figure 5.5: Output Voltage Waveform of ULN2804

5.2 SN55189 - QUADRUPLE LINE RECEIVERS

Description: These devices are monolithic low-power Schottky quadruple line receivers designed to satisfy the requirements of the standard interface between data-terminal equipment and data-communication equipment as defined by TIA/EIA-232-F. A separate response-control (CONT) terminal is provided for each receiver. A resistor or a resistor and bias-voltage source can be connected between this terminal and ground to shift the input threshold levels. An external capacitor can be connected between this terminal and ground to provide input noise filtering. The SN55189 and SN55189A are characterized for operation over the full military temperature range of -55°C to 125°C . The MC1489, MC1489A, SN75189, and SN75189A are characterized for operation from 0°C to 70°C

5.2.1 IC Layout

This figure represents the Pin Package Diagram of SN55189 ic

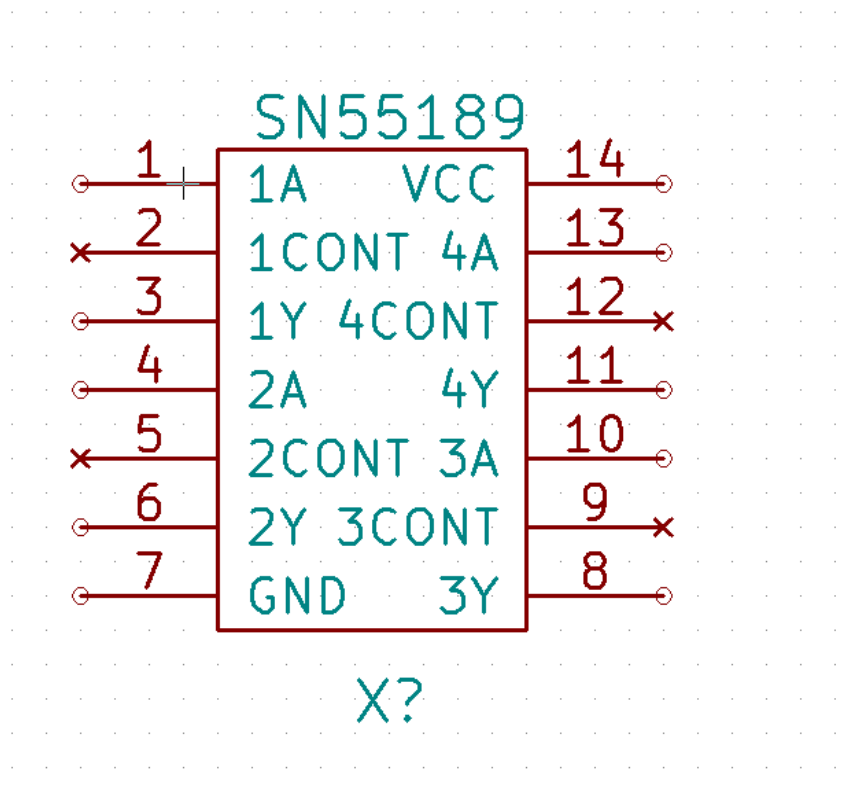


Figure 5.6: Pin diagram of SN55189

5.2.2 Subcircuit Schematic Diagram SN55189

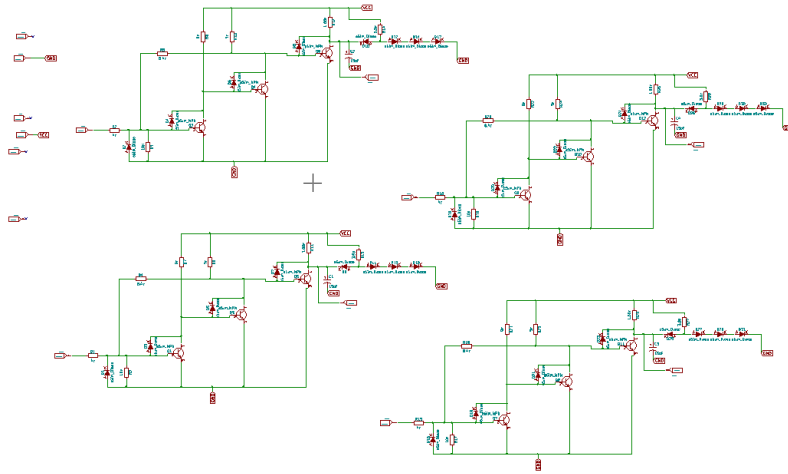


Figure 5.7: Subcircuit Schematic Diagram of SN55189

5.2.3 Test Circuit

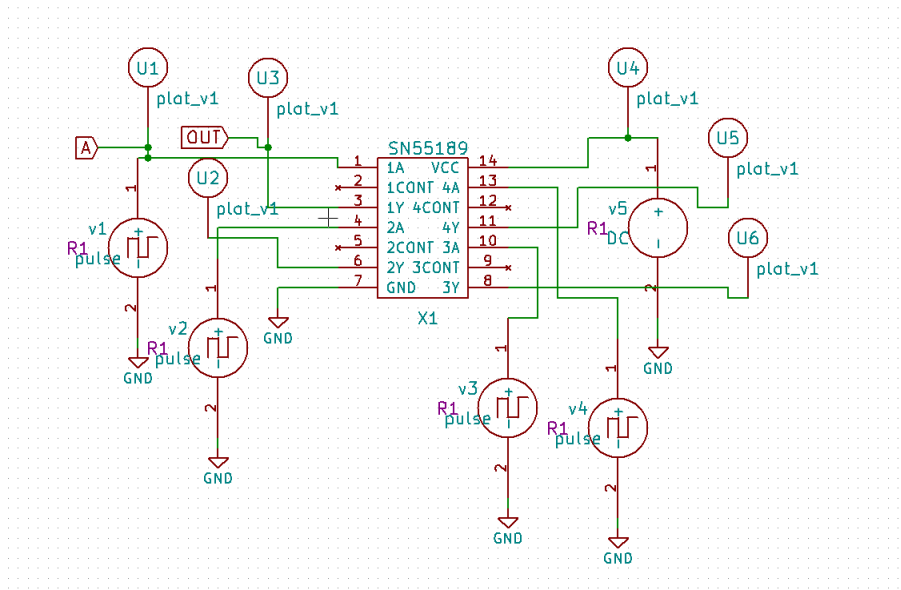


Figure 5.8: Test Circuit of SN55189

5.2.4 Input Plots

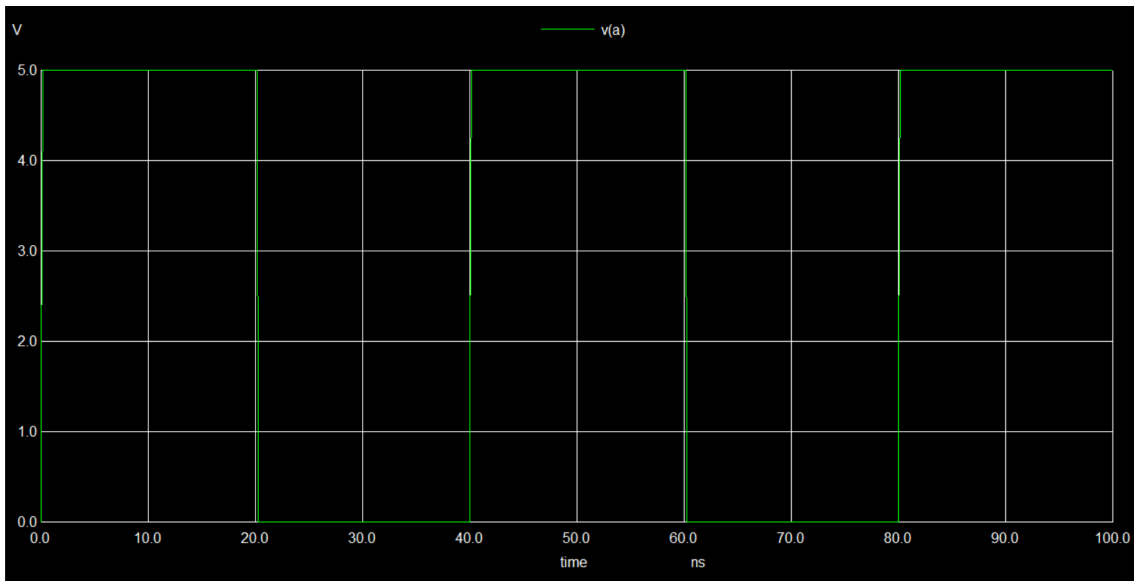


Figure 5.9: Input Plots Waveform of SN55189

5.2.5 Output Plots

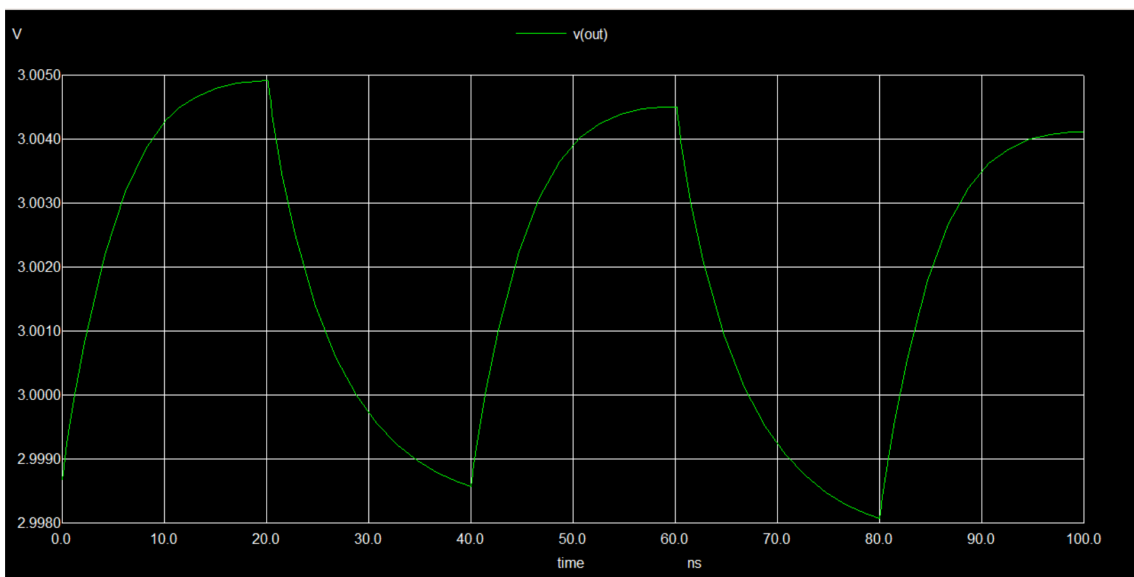


Figure 5.10: Output Voltage Waveform of SN55189

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