Winter Internship Report

on

Design and Simulation of a PLL using eSim

submitted by

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Acknowledgement

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I would also like to acknowledge Prof. Kannan M. Moudgalya for his foundational role in establishing and nurturing the FOSSEE initiative. His contributions toward open-source education and the creation of the FOSSEE fellowship framework have directly shaped the platform through which this internship was undertaken.

My sincere appreciation extends to my mentor, Mr.Sumanto Kar, for his continual support, technical guidance, and encouragement throughout the duration of this project. His insights and feedback played a key role in refining ideas, overcoming challenges, and ensuring the timely completion of the tasks assigned to me.

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This internship has been an enriching learning experience, allowing me to work closely with open-source EDA tools, designing circuits in eSim, and gain exposure to real-world circuit design and simulation workflows. The knowledge acquired during this period will undoubtedly support my future academic and professional pursuits.

I would also like to thank the entire FOSSEE team for their coordination, assistance, and timely interactions at various stages of this work. Their collective efforts ensured smooth workflow, resource accessibility, and effective project execution.

Contents

Chapter 1

Introduction

The Free/Libre and Open Source Software for Education (FOSSEE) project is an initiative by IIT Bombay under the National Mission on Education through Information and Communication Technology (ICT), funded by the Ministry of Education,Government of India. The project aims to reduce dependency on proprietary software in academic and research institutions by promoting the adoption of Free and Open Source Software (FOSS) alternatives.

It provides comprehensive documentation, tutorials, workshops, and hands-on train ing sessions, for empowering students, educators, and professionals to leverage open source software for their projects and coursework. The organization's commitment to fostering a collaborative and inclusive environment has significantly contributed to the democratization of technology and has opened up new avenues for innovation and learning. FOSSEE which stands for Free/Libre and Open Source Software for Education is an organization, based at IIT Bombay, as a remarkable initiative aimed at promoting the use of open-source software in education and research

1.1 eSim

One of FOSSEE's most significant contributions to the open-source ecosystem is eSim, a free and open-source Electronic Design Automation (EDA) tool for circuit design, simulation, analysis, and PCB design. Developed by IIT Bombay, eSim integrates multiple FLOSS tools to provide a complete design and simulation environment for electrical and electronics engineers. [1]

1.2 ngspice

NgSpice is the open-source spice simulator for electric and electronic circuits. Such a circuit may comprise JFETs, bipolar and MOS transistors, passive elements like R, L,or C, diodes, transmission lines and other devices, all interconnected in a netlist. Digital circuits are simulated as well, event-driven and fast, from single gates to complex circuits and the combination of both analog and digital as well as a mixed signal circuits. NgSpice offers a wealth of device models for active, passive, analog, and digital elements.[2]

Chapter 2

Features of eSim

The objective behind the development of eSim is to provide an open source EDA solution for electronics and electrical engineers. The software should be capable of performing schematic creation, PCB design and circuit simulation (analog, digital and mixed-signal). It should provide facilities to create new models and components. Thus,eSim offers the following features

1. Schematic Creation: eSim provides an easy-to-use graphical interface for drawing circuit schematics, making it accessible for users of all levels. Users can drag and drop components from the library onto the schematic, simplifying the design process. Comprehensive editing tools allow for easy modification of schematics, includingmoving, rotating, and labeling components.

2. Circuit Simulation: eSim supports SPICE (Simulation Program with Inte grated Circuit Emphasis), a standard for simulating analog and digital circuits. Users can perform various types of analysis such as transient, AC, and DC, providing insights into circuit behavior over time and frequency.An integrated waveform viewer helps visualize simulation results, aiding in the analysis and debugging of circuit designs.[2]

3. PCB Design: The PCB layout editor allows users to place components and route traces with precision. eSim includes DRC capabilities to ensure that the PCB design adheres to manufacturing constraints and electrical rules. Users can generate Gerber files, which are standard for PCB fabrication, directly from their designs.

4. Subcircuit Feature: This feature enables users to create complex circuits by integrating smaller, simpler subcircuits, promoting modular and hierarchical design approaches. Subcircuits can be reused in different projects, saving time and effort in redesigning common circuit elements.

5. Open Source Integration: eSim integrates several open-source tools like KiCad, Ngspice, and GHDL, providing a comprehensive suite for EDA. Being open-source, eSim is free to use, making advanced circuit design tools accessible without the need for expensive licenses.

Chapter 3

Design Statement

A fully integrated, 1.2V mixed-signal Phase-Locked Loop designed in IHP 130nm technology. The system utilizes a unified thin-oxide architecture to synchronize a highly sensitive 400 MHz current-starved ring oscillator to a 50 MHz reference clock, achieving sub-2µs lock times with an 18 µA charge pump and a 50 pF loop filter.

3.1 Approach

Initially, we designed the analog blocks (VCO, charge pump, and loop filter) using thick-oxide transistors for a 3.3V Vdd supply. After characterizing these blocks, we moved to the digital components. A roadblock emerged: in the IHP PDK, digital standard cells are characterized only for thin-oxide transistors at Vdd = 1.2V. While level shifters were one solution, we pivoted the entire design—including analog blocks—to use thin-oxide transistors exclusively.

The design methodology centered on a unified 1.2V voltage domain using the IHP 130nm PDK [3] to optimize switching speed and eliminate the area and power overhead of thick-oxide level shifters. Digital components, including the Phase Frequency Detector and Divide-by-8 feedback counter, were implemented using high-speed standard cells. The analog engine—comprising a current-starved ring oscillator and balanced charge pump—was custom-designed at the transistor level. Transistor sizing was strictly partitioned: minimum channel lengths (0.13 µm) were used for high-frequency switching paths, while longer lengths (0.5 µm) were employed in current mirrors to ensure precise 18 µA delivery to the 50 pF loop filter. Finally, physical closed-loop functionality was verified via NGspice transient simulations, successfully extracting real-world silicon parameters such as startup dead-zone and VCO gain ($K_{\mathrm{VCO}} = 6.4$ GHz/V).

Chapter 4

Voltage Controlled Oscillator

The initial Voltage Controlled Oscillator (VCO) architecture was implemented utilizing 3.3V thick-oxide transistors (sg13-hv) from the IHP 130nm PDK. These high-voltage devices feature a thicker gate dielectric layer. The design employs a classic current-starved ring oscillator configuration.
At its core, the architecture consists of an odd number of inverter stages connected in a continuous feedback loop to naturally sustain oscillation. To achieve frequency control, tail transistors (current mirrors) are placed between these inverters and the power rails. The analog control voltage (Vctrl) drives the gates of the bottom NMOS devices, acting as a tunable valve that restricts (or "starves") the amount of current available to charge and discharge the internal parasitic capacitances of the inverter nodes. Translating an input voltage into a current-limited propagation delay—remains the immutable foundation of the VCO's operation.

4.1 Schematic

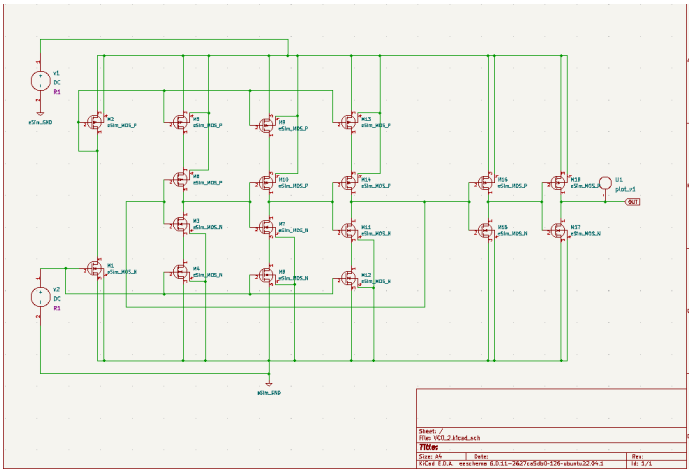


Figure 1: Voltage Controlled Oscillator Schematic in eSim.

4.2 Spice netlist

Listing 1: SPICE netlist for VCO in Fig. 1

```
.title kicad schematic

.lib /home/fossee/ihp/IHP-Open-PDK/ihp-sg13g2/libs.tech/ngspice/models/cornerMOShv.lib mos_tt

.control
pre_osdi /home/fossee/ihp/IHP-Open-PDK/ihp-sg13g2/libs.tech/ngspice/osdi/psp103.osdi
pre_osdi /home/fossee/ihp/IHP-Open-PDK/ihp-sg13g2/libs.tech/ngspice/osdi/psp103_nqs.osdi
.endc

.param VCTRL=2

xm18 out net-_m15-pad1_ net-_m10-pad4_ net-_m10-pad4_ sg13_hv_pmos W=3.7u L=0.35u
xm17 out net-_m15-pad1_ gnd gnd sg13_hv_nmos W=1u L=0.35u
xm15 net-_m15-pad1_ net-_m11-pad1_ gnd gnd sg13_hv_nmos W=1u L=0.35u
xm16 net-_m15-pad1_ net-_m11-pad1_ net-_m10-pad4_ net-_m10-pad4_ sg13_hv_pmos W=3.7u L=0.35u
v2 net-_m1-pad2_ gnd  dc {VCTRL}
xm1 net-_m1-pad1_ net-_m1-pad2_ gnd gnd sg13_hv_nmos W=1u L=0.35u
xm4 net-_m3-pad3_ net-_m1-pad2_ gnd gnd sg13_hv_nmos W=0.7u L=0.7u
xm6 net-_m10-pad2_ net-_m11-pad1_ net-_m5-pad1_ net-_m10-pad4_ sg13_hv_pmos W=3.7u L=0.35u
xm3 net-_m10-pad2_ net-_m11-pad1_ net-_m3-pad3_ gnd sg13_hv_nmos W=1u L=0.35u
xm11 net-_m11-pad1_ net-_m10-pad1_ net-_m11-pad3_ gnd sg13_hv_nmos W=1u L=0.35u
xm12 net-_m11-pad3_ net-_m1-pad2_ gnd gnd sg13_hv_nmos W=0.7u L=0.7u
xm14 net-_m11-pad1_ net-_m10-pad1_ net-_m13-pad1_ net-_m10-pad4_ sg13_hv_pmos W=3.7u L=0.35u
xm13 net-_m13-pad1_ net-_m1-pad1_ net-_m10-pad4_ net-_m10-pad4_ sg13_hv_pmos W=1.85u L=0.7u
v1 net-_m10-pad4_ gnd  dc 3.3
xm5 net-_m5-pad1_ net-_m1-pad1_ net-_m10-pad4_ net-_m10-pad4_ sg13_hv_pmos W=1.85u L=0.7u
```

```
xm2 net-_m1-pad1_ net-_m1-pad1_ net-_m10-pad4_ net-_m10-pad4_
    sg13_hv_pmos W=3.7u L=0.35u
xm10 net-_m10-pad1_ net-_m10-pad2_ net-_m10-pad3_ net-_m10-pad4_
    sg13_hv_pmos W=3.7u L=0.35u
xm9 net-_m10-pad3_ net-_m1-pad1_ net-_m10-pad4_ net-_m10-pad4_
    sg13_hv_pmos W=1.85u L=0.7u
xm7 net-_m10-pad1_ net-_m10-pad2_ net-_m7-pad3_ gnd sg13_hv_nmos W=1u L
    =0.35u
xm8 net-_m7-pad3_ net-_m1-pad2_ gnd gnd sg13_hv_nmos W=0.7u L=0.7u


*Gear (2nd-order) integration for stable transient behavior and to
    suppress numerical ringing.
.options method=gear maxord=2
.save V(out) I(v1)
.ic V(out)=0.01
*use initial conditions by-passing DC operating point analysis with min
    time step of 20ps and max internal time step of 10ps.
.tran 20p 100n 0 10p uic

.measure tran Iavg AVG I(v1) FROM=0n TO=100n
.measure tran Pavg PARAM='-Iavg*3.3'

.measure tran tper10 TRIG V(out) VAL=1.65 RISE=3 TARG V(out) VAL=1.65
    RISE=13
.measure tran period param='tper10/10'
.measure tran freq   param='1/period'

.control
run
print allv > plot_data_v.txt
print alli > plot_data_i.txt
plot v(out)
.endc
.end
```

4.3 Simulation waveforms

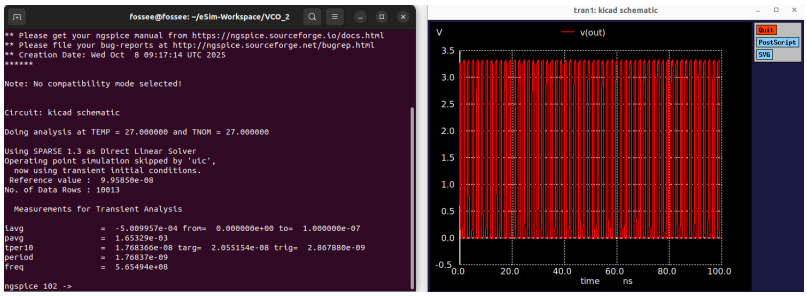


Figure 2: VCO generating output waveforms.

4.4 Specifications table

Parameter	Symbol	Value	Remarks
Technology		130-nm CMOS	IHP SG13G2
Supply Voltage	VDD	3.3V	HV(High Voltage, Thick oxide CMOS
Operating Temperaure Range	T	27C	Characterized at room temperature (-40C to +125C
Control Voltage	Vctrl	1.2V-3	Maximum linearity observed in this range
Output VCO Frequency	Vout	120MHz-1GHz	Maximum frequency of 1.03GHz
Centre frequency	fo	550MHz	@Vctrl = 2V
Frequenct Range	Δf	1GHz	Wide tuning range
VCO gain	KVCO	472MHz/V	Linear in 1.2-3V range
Power consumption	Pavg	1.65mW	At VDD=3.3V, Vctrl=2.0V

Figure 3: Specification table of VCO using Vdd=3.3V.

Chapter 5

Charge Pump and Loop filter

The Charge Pump and Loop Filter act as the critical bridge between the digital and analog domains of the Phase-Locked Loop. The Charge Pump is driven directly by the digital UP and DOWN error pulses generated by the Phase Frequency Detector (PFD). It consists of precision-matched PMOS and NMOS current mirrors that function as steered current sources. When an UP pulse is received, the PMOS network turns on to source a constant, stable current—designed to be approximately 18 µA in this system—into the loop filter. Conversely, a DOWN pulse activates the NMOS network to sink an identical amount of current out of the filter. Strict transistor sizing (such as using longer 0.5 µm channel lengths for the mirrors) is utilized to ensure the UP and DOWN currents are perfectly matched, which prevents steady-state phase offsets.
Beyond simply converting current to voltage, the loop filter suppresses the high-frequency switching noise generated by the PFD and dictates the dominant pole of the closed-loop system, ultimately governing the PLL's damping factor, stability, and sub-2µs lock time.

5.1 Schematic

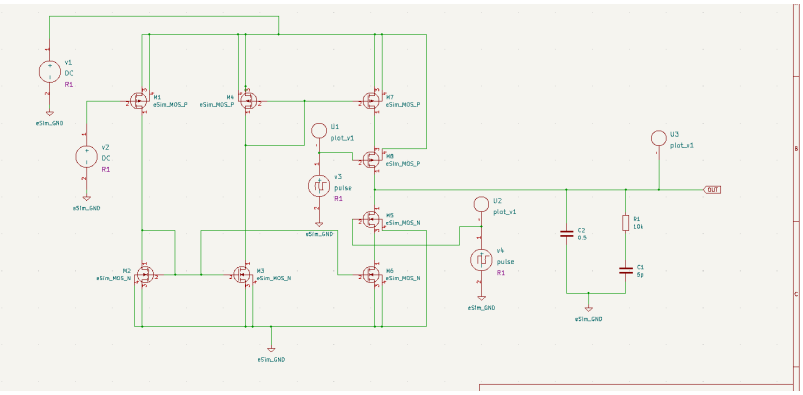


Figure 4: chargepump and loopfilter schematic in eSim.

5.2 Spice netlist

Listing 2: SPICE netlist for chargepump and loopfilter in Fig. **??**

```
  .title kicad schematic


.lib /home/fossee/ihp/IHP-Open-PDK/ihp-sg13g2/libs.tech/ngspice/models/
    cornerMOShv.lib mos_tt

.control
pre_osdi /home/fossee/ihp/IHP-Open-PDK/ihp-sg13g2/libs.tech/ngspice/osdi/
    psp103.osdi
pre_osdi /home/fossee/ihp/IHP-Open-PDK/ihp-sg13g2/libs.tech/ngspice/osdi/
    psp103_nqs.osdi
.endc



xm6 net-_m5-pad3_ net-_m1-pad1_ gnd gnd sg13_hv_nmos W=10u L=1u M=1
v3 net-_u1-pad~_ gnd pulse(3.3 0 10ns 100p 100p 10ns 40ns)
xm5 out net-_u2-pad~_ net-_m5-pad3_ gnd sg13_hv_nmos W=10u L=0.5u M=1
xm8 out net-_u1-pad~_ net-_m7-pad1_ net-_v1-pad1_ sg13_hv_pmos W=20u L=0.5u
     M=1
xm7 net-_m7-pad1_ net-_m3-pad1_ net-_v1-pad1_ net-_v1-pad1_ sg13_hv_pmos W
    =20u L=1u M=1
xm3 net-_m3-pad1_ net-_m1-pad1_ gnd gnd sg13_hv_nmos W=10u L=1u M=1
xm2 net-_m1-pad1_ net-_m1-pad1_ gnd gnd sg13_hv_nmos W=10u L=1u M=1
v1 net-_v1-pad1_ gnd  dc 3.3v
xm1 net-_m1-pad1_ net-_v2-pad1_ net-_v1-pad1_ net-_v1-pad1_ sg13_hv_pmos W
    =20u L=1u M=1
xm4 net-_m3-pad1_ net-_m3-pad1_ net-_v1-pad1_ net-_v1-pad1_ sg13_hv_pmos W
    =20u L=1u M=1
v2 net-_v2-pad1_ gnd  dc 2.7v
c2 out gnd 5p
r1 net-_c1-pad1_ out 1k
* u3 out plot_v1
c1 net-_c1-pad1_ gnd 50p
.ic v(out)=1.5
v4 net-_u2-pad~_ gnd pulse(0 3.3v 22ns 100p 100p 10n 40n)
* u2 net-_u2-pad~_ plot_v1
```

```
* u1 net-_u1-pad~_ plot_v1
.tran 2e-09 0.1e-06 0e-00

* Control Statements
.control
run
print allv > plot_data_v.txt
print alli > plot_data_i.txt
plot v(net-_u1-pad~_)
plot v(out)
plot v(net-_u2-pad~_)
plot v(net-_c1-pad1_)
.endc
.end
```

5.3 Simulation waveforms

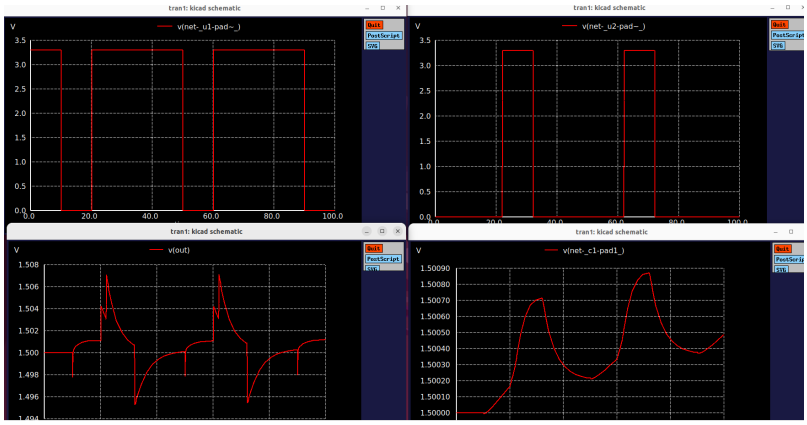


Figure 5: output of loop filter at capacitor c1 and Vout.

Chapter 6

Frequency Divider

The Frequency Divider serves as the critical digital link that closes the negative feedback loop of the Phase-Locked Loop . Its primary function is to step down the high-speed output of the Voltage Controlled Oscillator (400 MHz) so that it can be continuously compared against the highly stable Reference Clock (50 MHz). To achieve the required frequency multiplication factor of $N = 8$, the architecture is implemented as a Divide-by-8 counter, constructed by cascading three edge-triggered D-Flip-Flop standard cells.

6.1 Schematic

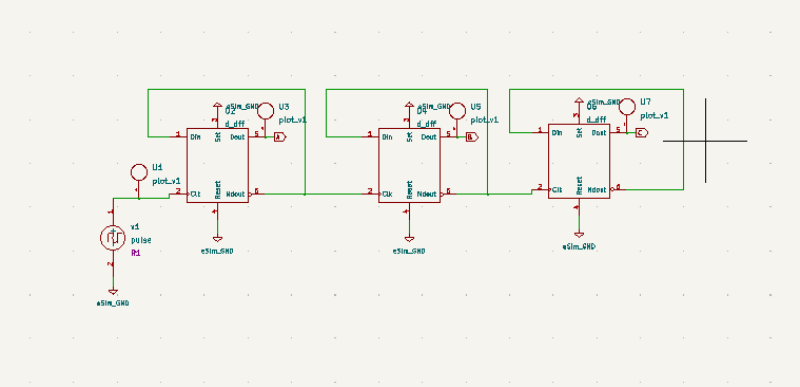


Figure 6: frequency divider schematic in eSim.

6.2 Spice netlist

Listing 3: SPICE netlist for frequency divier in Fig. 6

```
1   .title kicad schematic
2
3 .lib /home/fossee/ihp/IHP-Open-PDK/ihp-sg13g2/libs.tech/ngspice/models/
    cornerMOSlv.lib mos_tt
```

```
4
5  .include /home/fossee/ihp/IHP-Open-PDK/ihp-sg13g2/libs.ref/sg13g2_stdcell/
       spice/sg13g2_stdcell.spice
6
7  .control
8  pre_osdi /home/fossee/ihp/IHP-Open-PDK/ihp-sg13g2/libs.tech/ngspice/osdi/
       psp103.osdi
9  pre_osdi /home/fossee/ihp/IHP-Open-PDK/ihp-sg13g2/libs.tech/ngspice/osdi/
       psp103_nqs.osdi
10 .endc
11
12 * u5 b plot_v1
13 * u4 net-_u4-pad1_ net-_u2-pad1_ gnd gnd b net-_u4-pad1_ d_dff
14 * u6 net-_u6-pad1_ net-_u4-pad1_ gnd gnd c net-_u6-pad1_ d_dff
15 * u7 c plot_v1
16 * u3 a plot_v1
17 * u1 net-_u1-pad~_ plot_v1
18 v1 net-_u1-pad~_ gnd pulse(0 1.2 0 100p 100p 0.9n 2n)
19 * u2 net-_u2-pad1_ net-_u1-pad~_ gnd gnd a net-_u2-pad1_ d_dff
20
21
22 *a1 net-_u4-pad1_ net-_u2-pad1_ gnd gnd b net-_u4-pad1_ u4
23 *a2 net-_u6-pad1_ net-_u4-pad1_ gnd gnd c net-_u6-pad1_ u6
24 *a3 net-_u2-pad1_ net-_u1-pad~_ gnd gnd a net-_u2-pad1_ u2
25 * Schematic Name:                              d_dff, Ngspice Name: d_dff
26 *.model u4 d_dff(clk_delay=1.0e-9 set_delay=1.0e-9 reset_delay=1.0 ic=0
       data_load=1.0e-12 clk_load=1.0e-12 set_load=1.0e-12 reset_load=1.0e-12
       rise_delay=1.0e-9 fall_delay=1.0e-9 )
27 * Schematic Name:                              d_dff, Ngspice Name: d_dff
28 *.model u6 d_dff(clk_delay=1.0e-9 set_delay=1.0e-9 reset_delay=1.0 ic=0
       data_load=1.0e-12 clk_load=1.0e-12 set_load=1.0e-12 reset_load=1.0e-12
       rise_delay=1.0e-9 fall_delay=1.0e-9 )
29 * Schematic Name:                              d_dff, Ngspice Name: d_dff
30 *.model u2 d_dff(clk_delay=1.0e-9 set_delay=1.0e-9 reset_delay=1.0 ic=0
       data_load=1.0e-12 clk_load=1.0e-12 set_load=1.0e-12 reset_load=1.0e-12
       rise_delay=1.0e-9 fall_delay=1.0e-9 )
31
32 v_logic VDD gnd dc 1.2
33
34 X_FF1 a a_n net-_u1-pad~_ a_n VDD VDD gnd sg13g2_dfrbp_1
```

```
35
36 X_FF2 b b_n a b_n VDD VDD gnd sg13g2_dfrbp_1
37
38 X_FF3 c c_n b c_n VDD VDD gnd sg13g2_dfrbp_1
39
40
41 .tran 100e-12 100e-09 0e-00
42
43 * Control Statements
44 .control
45 run
46 print allv > plot_data_v.txt
47 print alli > plot_data_i.txt
48 plot v(b)
49 plot v(c)
50 plot v(a)
51 plot v(net-_u1-pad~_)
52 .endc
53 .end
```

6.3 Simulation waveforms

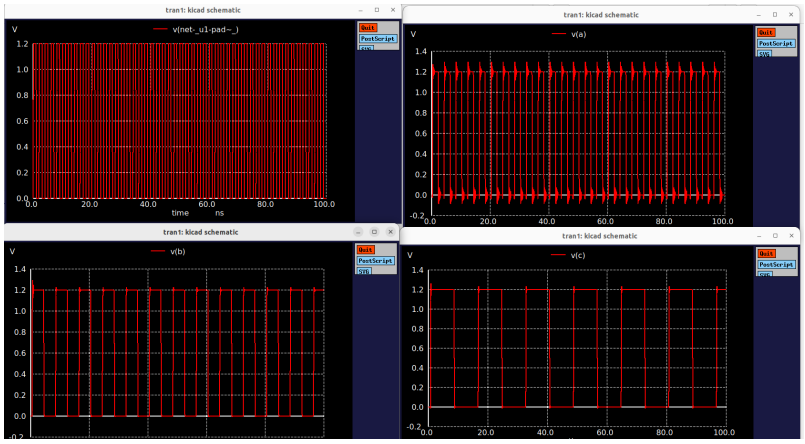


Figure 7: Frequency decreases as the signal moves from a to c

Chapter 7

Phase Frequency Detector

Architecturally, the PFD is constructed using two edge-triggered D-Flip-Flops and an asynchronous reset path (typically a NAND gate) sourced directly from the 1.2V thin-oxide digital standard cell library of the IHP 130nm PDK. If the Reference Clock arrives early, the PFD asserts an UP logic pulse, signaling the Charge Pump to increase the control voltage and speed up the VCO. Conversely, if the feedback clock arrives early, a DOWN pulse is asserted to drain charge and slow the VCO. A critical feature of this specific digital architecture is its built-in "dead-zone avoidance".

7.1 Schematic

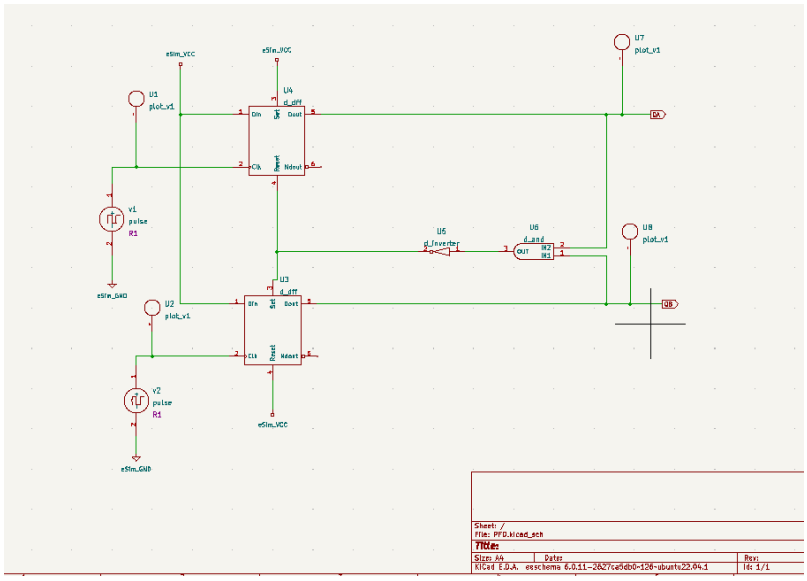


Figure 8: Phase frequency detector schematic in eSim.

7.2 Spice netlist

Listing 4: SPICE netlist for PFD in Fig. 8

```
  .title kicad schematic

.lib /home/fossee/ihp/IHP-Open-PDK/ihp-sg13g2/libs.tech/ngspice/models/
    cornerMOSlv.lib mos_tt
.include /home/fossee/ihp/IHP-Open-PDK/ihp-sg13g2/libs.ref/sg13g2_stdcell/
    spice/sg13g2_stdcell.spice

.control
pre_osdi /home/fossee/ihp/IHP-Open-PDK/ihp-sg13g2/libs.tech/ngspice/osdi/
    psp103.osdi
pre_osdi /home/fossee/ihp/IHP-Open-PDK/ihp-sg13g2/libs.tech/ngspice/osdi/
    psp103_nqs.osdi
.endc


v_logic VDD gnd dc 1.2

* u5 net-_u5-pad1_ net-_u3-pad3_ d_inverter
* u6 qa qa net-_u5-pad1_ d_and
* u7 qa plot_v1
* u8 qa plot_v1
* u3 vcc net-_u2-pad~_ net-_u3-pad3_ vcc qa net-_u3-pad6_ d_dff
* u2 net-_u2-pad~_ plot_v1
* u1 net-_u1-pad~_ plot_v1
* u4 vcc net-_u1-pad~_ vcc net-_u3-pad3_ qa net-_u4-pad6_ d_dff


v1 net-_u1-pad~_ gnd pulse(0 1.2 4n 100p 100p 7.9n 16n)
v2 net-_u2-pad~_ gnd pulse(0 1.2 0n 100p 100p 7.9n 16n)


* Top D-Flip-Flop (Generates QA / "UP" pulse)
* Pin Order: Q  Q_N  CLK  D  RESET_B  VDD  VSS
X_FF_UP QA qa_n net-_u1-pad~_ VDD reset_b VDD gnd sg13g2_dfrbp_1

X_FF_DN QB qb_n net-_u2-pad~_ VDD reset_b VDD gnd sg13g2_dfrbp_1

```

```
* Reset Logic (NAND gate replacing AND + INVERTER)
X_NAND reset_b QA QB VDD gnd sg13g2_nand2_1


.tran 10e-12 100e-09 0e-00

* Control Statements
.control
run
print allv > plot_data_v.txt
print alli > plot_data_i.txt
plot v(qa)
plot v(qb)
plot v(net-_u2-pad~_)
plot v(net-_u1-pad~_)
.endc
.end
```

7.3 Simulation waveforms

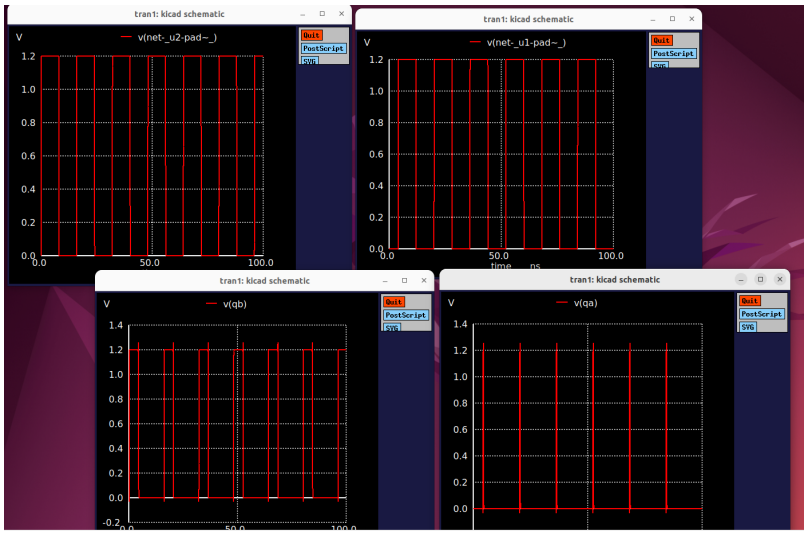


Figure 9: Qa and Qb outputs

Chapter 8

Phase Locked Loop

Phase-Locked Loop (PLL) is a highly precise, mixed-signal negative feedback control system designed to synchronize a locally generated oscillator with a stable external reference.This closed-loop negative feedback mechanism ensures that any momentary deviation in the output frequency automatically generates a counteracting control voltage. The system continuously pushes and pulls this voltage, forcing the loop to dynamically look for and lock onto the exact operating point where phase and frequency errors are driven to absolute zero [4].

8.1 Schematic

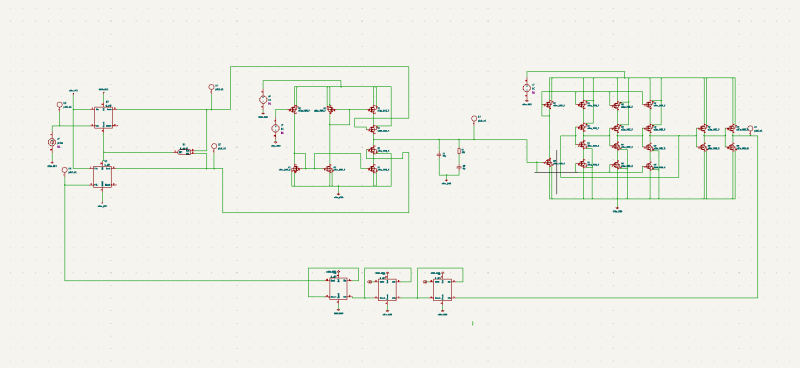


Figure 10: Phase Locked Loop schematic in eSim.

8.2 Spice netlist

Listing 5: SPICE netlist for PLL in Fig. 10

```
.title kicad schematic


.lib /home/fossee/ihp/IHP-Open-PDK/ihp-sg13g2/libs.tech/ngspice/models/
    cornerMOSlv.lib mos_tt
.include /home/fossee/ihp/IHP-Open-PDK/ihp-sg13g2/libs.ref/sg13g2_stdcell/
    spice/sg13g2_stdcell.spice

.control
pre_osdi /home/fossee/ihp/IHP-Open-PDK/ihp-sg13g2/libs.tech/ngspice/osdi/
    psp103.osdi
pre_osdi /home/fossee/ihp/IHP-Open-PDK/ihp-sg13g2/libs.tech/ngspice/osdi/
    psp103_nqs.osdi
.endc

v_logic VDD gnd dc 1.2


v1 net-_u1-pad~_ gnd pulse(0 1.2 0 100p 100p 9.9n 20n)

* --------Digital Domain Standard cells-------------

* --Frequency Divider---
* Driven by VCO Output: net-_m25-pad1_
X_DIV1 div_a div_a_n net-_m25-pad1_ div_a_n VDD VDD gnd sg13g2_dfrbp_1
X_DIV2 div_b div_b_n div_a          div_b_n VDD VDD gnd sg13g2_dfrbp_1
X_DIV3 net-_u2-pad~_ div_c_n div_b  div_c_n VDD VDD gnd sg13g2_dfrbp_1

* ----Phase Frequency Detector---
* --UP Flip-Flop
X_PFD_UP QA net-_m8-pad2_ net-_u1-pad~_ VDD reset_b VDD gnd sg13g2_dfrbp_1

*---Down Flip-Flop
X_PFD_DN net-_m5-pad2_ qb_n net-_u2-pad~_ VDD reset_b VDD gnd
    sg13g2_dfrbp_1

X_NAND reset_b QA net-_m5-pad2_ VDD gnd sg13g2_nand2_1
```

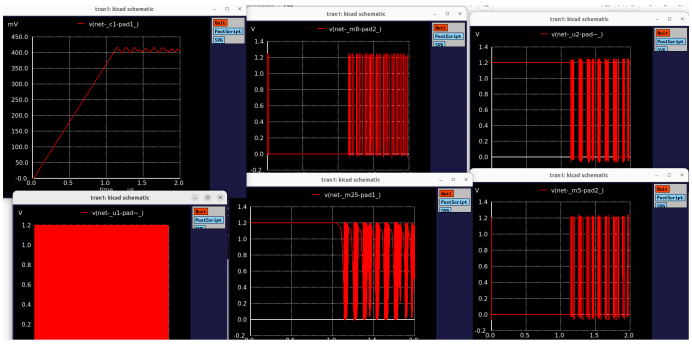
```
33
34 * ----------Analog Domain---------------
35
36 * ---Charge Pump -------------
37
38 * Charge bias to M1
39
40 v3 net-_m1-pad2_ gnd dc 0.6
41
42 * PMOS Mirror & Switches
43 xm4 net-_m3-pad1_ net-_m3-pad1_ net-_m1-pad3_ net-_m1-pad3_ sg13_lv_pmos w
       =4u l=0.5u
44 xm1 net-_m1-pad1_ net-_m1-pad2_ net-_m1-pad3_ net-_m1-pad3_ sg13_lv_pmos w
       =4u l=0.5u
45 *v3 net-_m1-pad2_ gnd  dc 0.7
46 xm8 net-_c1-pad1_ net-_m8-pad2_ net-_m7-pad1_ net-_m1-pad3_ sg13_lv_pmos w
       =4u l=0.13u
47 xm7 net-_m7-pad1_ net-_m3-pad1_ net-_m1-pad3_ net-_m1-pad3_ sg13_lv_pmos w
       =4u l=0.5u
48
49
50 *NMOS Mirror & Switches
51
52 xm2 net-_m1-pad1_ net-_m1-pad1_ gnd gnd sg13_lv_nmos w=2u l=0.5u
53 xm3 net-_m3-pad1_ net-_m1-pad1_ gnd gnd sg13_lv_nmos w=2u l=0.5u
54 xm5 net-_c1-pad1_ net-_m5-pad2_ net-_m5-pad3_ gnd sg13_lv_nmos w=2u l=0.13u
55 xm6 net-_m5-pad3_ net-_m1-pad1_ gnd gnd sg13_lv_nmos w=2u l=0.5u
56
57 * Loop filter
58
59 r1 net-_c2-pad1_ net-_c1-pad1_ 10k
60 c2 net-_c2-pad1_ gnd 5p
61 c1 net-_c1-pad1_ gnd 50p
62
63 *Pre-charge filter to speed up locking time
64 *.ic v(net-_c1-pad1_)=0.6
65 * for VCO signal to lag behind reference signal keep the initial voltage to
       0v.
66 .ic v(net-_c1-pad1_)=0.0
67
```

```
* -- Voltage Controlled Oscillator-----

* Current Limiters

xm10 net-_m10-pad1_ net-_m10-pad1_ net-_m10-pad3_ net-_m10-pad3_
    sg13_lv_pmos w=4u l=0.5u
xm17 net-_m17-pad1_ net-_m10-pad1_ net-_m10-pad3_ net-_m10-pad3_
    sg13_lv_pmos w=4u l=0.5u
xm13 net-_m13-pad1_ net-_m10-pad1_ net-_m10-pad3_ net-_m10-pad3_
    sg13_lv_pmos w=4u l=0.5u
xm21 net-_m21-pad1_ net-_m10-pad1_ net-_m10-pad3_ net-_m10-pad3_
    sg13_lv_pmos w=4u l=0.5u

xm9 net-_m10-pad1_ net-_c1-pad1_ gnd gnd sg13_lv_nmos w=2u l=0.5u
xm12 net-_m11-pad3_ net-_c1-pad1_ gnd gnd sg13_lv_nmos w=2u l=0.5u
xm20 net-_m19-pad3_ net-_c1-pad1_ gnd gnd sg13_lv_nmos w=2u l=0.5u
xm16 net-_m15-pad3_ net-_c1-pad1_ gnd gnd sg13_lv_nmos w=2u l=0.5u

* High Speed Inverter Stages

xm22 net-_m11-pad2_ net-_m15-pad1_ net-_m21-pad1_ net-_m10-pad3_
    sg13_lv_pmos w=2u l=0.13u
xm19 net-_m11-pad2_ net-_m15-pad1_ net-_m19-pad3_ gnd sg13_lv_nmos w=1u l
    =0.13u

xm18 net-_m15-pad1_ net-_m11-pad1_ net-_m17-pad1_ net-_m10-pad3_
    sg13_lv_pmos w=2u l=0.13u
xm15 net-_m15-pad1_ net-_m11-pad1_ net-_m15-pad3_ gnd sg13_lv_nmos w=1u l
    =0.13u

xm14 net-_m11-pad1_ net-_m11-pad2_ net-_m13-pad1_ net-_m10-pad3_
    sg13_lv_pmos w=2u l=0.13u
xm11 net-_m11-pad1_ net-_m11-pad2_ net-_m11-pad3_ gnd sg13_lv_nmos w=1u l
    =0.13u

* Output Buffer

xm24 net-_m23-pad1_ net-_m11-pad2_ net-_m10-pad3_ net-_m10-pad3_
    sg13_lv_pmos w=2u l=0.13u
xm23 net-_m23-pad1_ net-_m11-pad2_ gnd gnd sg13_lv_nmos w=1u l=0.13u
```

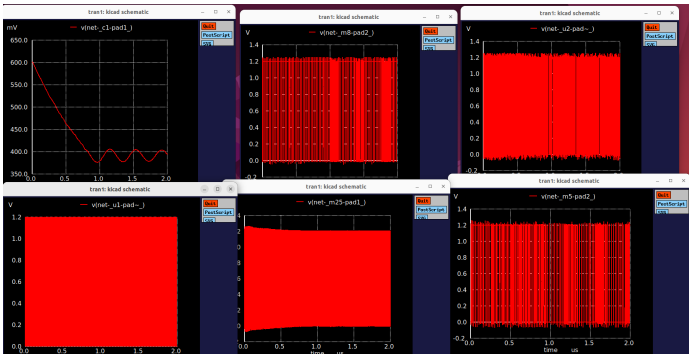
```
xm26 net-_m25-pad1_ net-_m23-pad1_ net-_m10-pad3_ net-_m10-pad3_
    sg13_lv_pmos w=2u l=0.13u
xm25 net-_m25-pad1_ net-_m23-pad1_ gnd gnd sg13_lv_nmos w=1u l=0.13u

.tran 50p 2u 0

* u11 net-_c1-pad1_ plot_v1
v4 net-_m10-pad3_ gnd  dc 1.2


* u12 net-_m25-pad1_ plot_v1

v2 net-_m1-pad3_ gnd  dc 1.2


* u8 net-_u8-pad1_ net-_u8-pad2_ gnd gnd net-_u2-pad~_ net-_u8-pad1_ d_dff
* u10 net-_u10-pad1_ net-_m25-pad1_ gnd gnd a net-_u10-pad1_ d_dff
* u9 net-_u8-pad2_ net-_u10-pad1_ gnd gnd b net-_u8-pad2_ d_dff
* u1 net-_u1-pad~_ plot_v1
* u4 vcc net-_u1-pad~_ vcc net-_u3-pad3_ net-_m8-pad2_ net-_u4-pad6_ d_dff
* u5 net-_m5-pad2_ net-_m8-pad2_ net-_u3-pad3_ d_nand
* u6 net-_m8-pad2_ plot_v1
*v1 net-_u1-pad~_ gnd pulse(1.2 0 0 100p 100p 5n 10n)


* u7 net-_m5-pad2_ plot_v1
* u3 vcc net-_u2-pad~_ net-_u3-pad3_ vcc net-_m5-pad2_ net-_u3-pad6_ d_dff
* u2 net-_u2-pad~_ plot_v1

*.tran 10e-12 100e-09 oe-00

* Control Statements
.control
run
print allv > plot_data_v.txt
print alli > plot_data_i.txt
plot v(net-_c1-pad1_)
plot v(net-_m25-pad1_)
plot v(net-_u1-pad~_)
plot v(net-_m8-pad2_)
```

```
plot v(net-_m5-pad2_)
plot v(net-_u2-pad~_)
.endc
.end
```

8.3 Simulation waveforms



(a) When feedback signal lags and starts from zero.



(b) When feedback signal dominates.

Figure 11: Control voltage at different instances

Chapter 9

Conclusion and Future Scope

9.1 Conclusion

In this project, a fully integrated 400 MHz mixed-signal Phase-Locked Loop (PLL) was successfully architected, designed, and verified at the transistor level using the open-source IHP 130nm (sg13g2) CMOS process. A major architectural achievement of this design was the implementation of a unified 1.2V voltage domain. By strategically utilizing thin-oxide (sg13-lv) transistors for both the analog components (Charge Pump,VCO) and the digital standard cells (Phase Frequency Detector, Frequency Divider), the system achieved high-speed operation while completely eliminating the area, power, and delay overhead associated with cross-domain level shifters.Rigorous transient simulations validated the closed-loop negative feedback physics of the system. The PLL successfully multiplied a 50 MHz reference clock by a factor of 8 to achieve a stable 400 MHz output. Key silicon parameters were successfully extracted from the simulation data, demonstrating a stable charge pump current (Icp) of 18µA and a highly sensitive VCO gain (Kvco) of 6.4 GHz/V. Furthermore, both "cold-start" (0.0V initial condition) and pre-charged (0.6V initial condition) transient analyses proved the system's robust capability to overcome the NMOS dead-zone (less than 0.38V) and achieve precise phase and frequency lock in under sub-2µs.

9.2 Future Scope

While the current design successfully demonstrates core PLL functionality and fast lock times, several enhancements can be implemented to prepare the architecture for commercial ASIC tapeout: VCO Coarse/Fine Tuning to Reduce Phase Noise: The current thin-oxide current-starved ring oscillator exhibits a highly sensitive gain (Kvco) of 6.4 GHz/V. While this allows for rapid locking, it makes the oscillator highly susceptible to supply noise and jitter. Future iterations should implement a hybrid tuning architecture: a digitally switched capacitor bank for "coarse" frequency tuning, paired with a reduced-gain analog control path (approx 100 MHz/V) for "fine" phase tracking to drastically improve phase noise performance.
Physical Layout and Parasitic Extraction (PEX): The next critical step in the ASIC design flow is translating the SPICE netlist into a physical GDSII layout. Following Design Rule Checking

(DRC) and Layout Versus Schematic (LVS) verification, Post-Layout Extraction (PEX) must be performed. Simulating the extracted netlist will reveal how physical wire resistance and parasitic routing capacitance impact the 400 MHz maximum frequency and the loop's damping factor.

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