



eSim Semester Long Internship Autumn 2025

On

Integrated Circuit Design using Subcircuit Feature of eSim

Submitted by

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Chapter 1

Introduction

FOSSEE (Free/Libre and Open Source Software for Education) is an initiative based at the Indian Institute of Technology Bombay, aimed at promoting the use of open-source software in education and research. The primary objective of FOSSEE is to reduce dependency on proprietary software and to encourage the adoption of high-quality, free, and open-source alternatives across academic institutions and industries.

FOSSEE supports the development, documentation, and dissemination of several open-source tools across multiple domains, including electronics, mathematics, computer science, and science education. It provides comprehensive documentation, tutorials, workshops, and hands-on training sessions to empower students, educators, and professionals to effectively use open-source software for academic projects, research work, and industrial applications.

The organization actively fosters a collaborative and inclusive ecosystem where users can contribute to tool development, report issues, and share improvements. This approach has significantly contributed to the democratization of technology by making advanced software tools accessible to a wider audience. Through its initiatives, FOSSEE has opened new avenues for innovation, learning, and skill development, particularly in resource-constrained educational environments.

1.1 eSim

eSim is a powerful open-source electronic design automation (EDA) tool developed under the FOSSEE project at IIT Bombay. It is designed to provide an integrated environment for schematic capture, circuit simulation, and printed circuit board (PCB) design. By combining multiple open-source software packages into a single cohesive platform, eSim simplifies the workflow involved in electronic circuit design and analysis.

eSim integrates tools such as KiCad for schematic and PCB design, NgSpice for circuit simulation, and Makerchip for digital and mixed-signal design. This integration allows users to seamlessly transition from schematic creation to simulation and layout, eliminating the need to rely on multiple disconnected tools. eSim is particularly beneficial for students, educators, and researchers who require an affordable and accessible alternative to commercial EDA software.

One of the most significant features of eSim is its Subcircuit capability. This feature enables users to design complex circuits by hierarchically integrating smaller, reusable subcircuits. The subcircuit approach improves modularity, reduces design complexity, and enhances maintainability of large-scale circuit designs. Through eSim, FOSSEE promotes open-source solutions in electronics education and professional practice, encouraging innovation, collaboration, and reproducibility.

1.2 NgSpice

NgSpice is an open-source SPICE-based simulator used for the analysis of electrical and electronic circuits. It supports simulation of a wide range of circuit components, including resistors, capacitors, inductors, diodes, BJTs, MOSFETs, JFETs, and various other semiconductor devices. Circuit descriptions are provided in the form of netlists, which define component connections and parameters.

NgSpice is capable of performing different types of analyses such as DC operating point analysis, AC small-signal analysis, transient analysis, and noise analysis. In addition to analog circuits, NgSpice also supports digital and mixed-signal circuit simulation, allowing users to simulate simple logic gates as well as complex hybrid systems that combine analog and digital components.

The simulator provides extensive device models for active and passive components, making it suitable for both educational and research-oriented applications. Simulation results are typically displayed as graphical plots of voltages, currents, and other electrical quantities, or stored in output data files for further analysis. Within eSim, NgSpice serves as the core simulation engine, enabling accurate and efficient circuit verification.

1.3 Makerchip

Makerchip is an online and desktop-based platform designed to simplify digital circuit design and verification. It provides an intuitive environment for writing, compiling, simulating, and debugging Verilog, SystemVerilog, and Transaction-Level Verilog (TLV) code. Makerchip supports both open-source and proprietary simulation tools, ensuring a flexible and comprehensive digital design workflow.

In the eSim ecosystem, Makerchip is interfaced through a Python-based application known as Makerchip-App. This interface allows users to launch the Makerchip Integrated Development Environment (IDE) directly from eSim, enabling seamless digital and mixed-signal design integration. Users can simulate digital logic, validate design functionality, and visualize waveforms within the Makerchip environment.

Makerchip emphasizes ease of use and accessibility, making it suitable for users of all skill levels. Its user-friendly interface, guided workflows, and educational features help reduce the learning curve associated with digital circuit design. While individual open-source tools often focus on specific aspects such as simulation or PCB design, Makerchip complements eSim by addressing digital design requirements.

Despite their advantages, many open-source EDA tools are not comprehensive on their own. Some tools specialize in PCB design, while others focus solely on

simulation. To the best of our knowledge, there is no single open-source platform that independently combines schematic design, simulation, digital design, and PCB layout. eSim bridges this gap by integrating multiple tools into a unified platform, making it a complete solution for electronic system design.

Chapter 2

Features of eSim

The primary objective behind the development of eSim is to provide a comprehensive open-source Electronic Design Automation (EDA) solution for electronics and electrical engineering applications. eSim is capable of performing schematic creation, printed circuit board (PCB) design, and circuit simulation, including analog, digital, and mixed-signal circuits. In addition, it provides facilities for creating new device models and custom components, thereby extending its usability for research and educational purposes.

By integrating multiple open-source tools into a unified platform, eSim addresses the limitations of individual tools that focus on isolated aspects of circuit design. The key features of eSim are described below.

2.1 Schematic Creation

eSim provides a user-friendly graphical interface for creating circuit schematics. Users can easily design circuits by dragging and dropping components from an extensive library onto the schematic workspace. The intuitive interface makes eSim accessible to users with varying levels of expertise, from beginners to experienced designers.

Comprehensive editing tools are available to modify schematics efficiently, including options to move, rotate, mirror, and label components. Electrical connections can be drawn and edited with ease, enabling quick iteration during the design process.

2.2 Circuit Simulation

eSim supports circuit simulation using SPICE (Simulation Program with Integrated Circuit Emphasis), which is a widely accepted standard for analog and digital circuit analysis. Users can perform various types of simulations, including DC operating point, AC small-signal, and transient analyses, to study circuit behavior under different conditions.

The integrated waveform viewer allows users to visualize voltages, currents, and other electrical parameters over time or frequency. This feature aids in debugging

circuit designs, validating functionality, and understanding system-level behavior.

2.3 PCB Design

The PCB design module in eSim enables users to translate schematics into physical layouts suitable for fabrication. The layout editor provides tools for precise component placement and trace routing, ensuring reliable electrical connectivity and optimal board performance.

eSim includes Design Rule Check (DRC) capabilities that help verify compliance with manufacturing and electrical constraints, thereby reducing the likelihood of errors during fabrication. Users can generate industry-standard Gerber files directly from the PCB layouts, facilitating seamless integration with PCB manufacturing processes.

2.4 Subcircuit Feature

The Subcircuit feature is one of the most significant capabilities of eSim, allowing users to implement hierarchical and modular circuit designs. Complex circuits can be constructed by integrating smaller, well-defined subcircuits, improving design readability and manageability.

Subcircuits can be reused across multiple projects, reducing redundancy and saving development time. This approach is particularly beneficial for designing large-scale systems and integrated circuits, where modular design principles enhance scalability and maintenance.

2.5 Open-Source Integration

eSim integrates several open-source tools such as KiCad for schematic and PCB design, NgSpice for circuit simulation, and GHDL for digital and mixed-signal modeling. This integration provides a complete and flexible EDA workflow within a single platform.

As an open-source software, eSim is freely available, eliminating the need for expensive commercial licenses. This makes advanced electronic design tools accessible to a wider community, promoting learning, experimentation, and innovation in both academic and professional environments.

Chapter 3

Problem Statement

The objective of this project is to design and develop various analog and digital Integrated Circuit (IC) models in the form of subcircuits using the device model files already available in the eSim library. These IC subcircuit models are intended to be integrated into the eSim subcircuit library, making them accessible for future circuit design and simulation purposes.

Once successfully implemented and validated, these IC models will assist developers, students, and researchers in designing complex electronic systems efficiently without the need to recreate commonly used IC functionalities from scratch.

3.1 Approach

The approach adopted to achieve the stated objective follows a systematic and iterative design methodology. The complete IC design workflow followed in this project is illustrated in Figure 3.1.

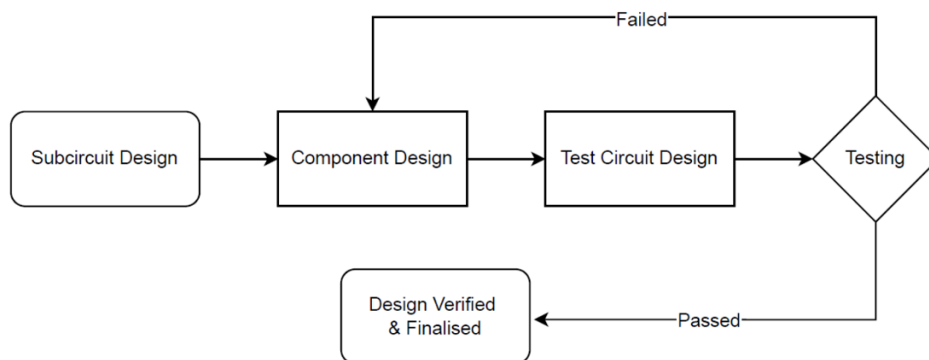


Figure 3.1: Flowchart of IC Design Approach Followed

The methodology involved extensive reference to datasheets from leading Integrated Circuit manufacturers such as Texas Instruments, Analog Devices, and NXP Semiconductors. ICs with diverse functionalities, including precision amplifiers, comparators, encoders, and audio amplifiers, were selected for implementation.

The complete process was carried out in the following steps.

3.1.1 Analyzing Datasheets

The first step involved a detailed analysis of datasheets corresponding to various analog and digital ICs. The objective was to identify ICs that were not already available in the existing eSim subcircuit library.

This process included examining internal circuit schematics, understanding truth tables for digital ICs, evaluating component values, and studying electrical characteristics. ICs offering unique functionality or enhanced performance were prioritized for implementation.

3.1.2 Subcircuit Creation

After selecting suitable ICs, the next step involved modeling them as subcircuits within the eSim environment. The device model files available in the eSim library were utilized to construct accurate subcircuit representations.

Special attention was given to ensure strict compliance with the specifications provided in the official datasheets. Symbol creation and pin configuration were performed according to the IC package details and pin descriptions. This step was critical in maintaining the functional accuracy and usability of the developed subcircuit models.

3.1.3 Test Circuit Design

Once the subcircuits were created, test circuits were designed to verify the correctness of the implemented IC models. These test circuits were constructed based on reference application circuits provided in the datasheets.

Multiple test cases were developed to evaluate the performance of the ICs under different operating conditions. This step ensured that the subcircuits behaved consistently with their real-world counterparts.

3.1.4 Schematic Testing and Validation

The designed test circuits were simulated to analyze the outputs and overall circuit behavior. Waveforms and plots were generated to assess performance parameters. KiCad was used to convert schematic designs into NgSpice netlists, and simulations were carried out using eSim's integrated simulation tools.

If the simulated results deviated from the expected outputs specified in the datasheets, the schematic designs were revisited to identify and correct errors. This iterative process of debugging and re-simulation continued until satisfactory results were achieved.

Once the IC subcircuits met the desired functional and performance criteria, they were considered successfully validated, thereby completing the IC design process.

Chapter 4

Completed Integrated Circuits

4.1 74LVC1G17 – Single Schmitt-Trigger Buffer

4.1.1 General Description

The 74LVC1G17 is a single non-inverting Schmitt-trigger buffer designed for high-speed digital signal conditioning. It is a part of the 74LVC logic family and operates over a wide supply voltage range, making it suitable for low-voltage and high-performance digital applications.

The device incorporates a Schmitt-trigger input, which provides hysteresis and enhanced noise immunity. This feature ensures clean and stable output transitions even when the input signal has slow rise and fall times or is affected by noise. The 74LVC1G17 is especially useful for interfacing between noisy environments and sensitive digital logic circuits.

With its low power consumption, compact package, and reliable switching characteristics, the 74LVC1G17 is widely used in modern digital systems requiring robust signal buffering and conditioning.

4.1.2 Key Features

The key features of the 74LVC1G17 Schmitt-trigger buffer include the following:

- **Schmitt-Trigger Input:** Provides hysteresis to improve noise immunity and ensure clean digital transitions for slow or noisy input signals.
- **Wide Supply Voltage Range:** Operates over a broad voltage range, making it compatible with low-voltage and mixed-voltage digital systems.
- **High-Speed Operation:** Supports fast signal propagation, making it suitable for high-frequency digital applications.
- **Low Power Consumption:** Designed for low static and dynamic power dissipation, ideal for battery-powered and portable devices.
- **CMOS Technology:** Fabricated using advanced CMOS technology, ensuring high reliability and long-term stability.

- **Small Package Size:** Available in compact packages, enabling space-efficient PCB designs.

4.1.3 Applications

The 74LVC1G17 Schmitt-trigger buffer is used in a wide range of digital and mixed-signal applications, including:

- **Signal Conditioning:** Cleans noisy or distorted digital signals before they are processed by downstream logic.
- **Debouncing Circuits:** Used in switch and button debounce applications to eliminate unwanted signal fluctuations.
- **Waveform Shaping:** Converts slow-rising or analog-like signals into well-defined digital waveforms.
- **Clock Signal Buffering:** Improves clock signal integrity by providing sharp transitions.
- **Interfacing Logic Levels:** Acts as a buffer between different digital subsystems to ensure reliable communication.

4.1.4 Pin Configuration

Figure 4.1 shows the pin configuration of the 74LVC1G17 Schmitt-trigger buffer.

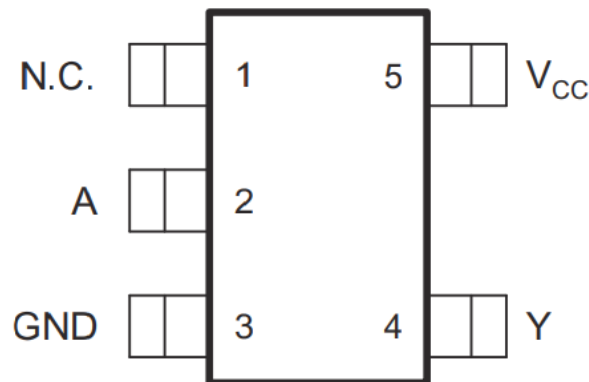


Figure 4.1: Pin Configuration of the 74LVC1G17

4.1.5 IC Layout

The internal IC layout of the 74LVC1G17 is shown in Figure 4.3. The layout illustrates the arrangement of internal transistors and logic elements used to implement the Schmitt-trigger buffer functionality.

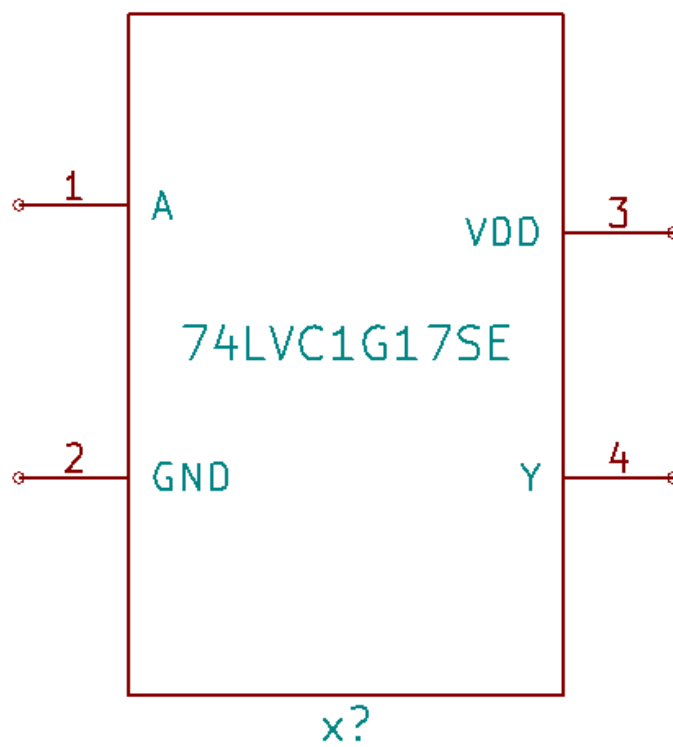


Figure 4.2: Subcircuit Schematic Diagram of the 74LVC1G17

4.1.6 Subcircuit Schematic Diagram

Figure 4.2 shows the subcircuit schematic diagram of the 74LVC1G17 Schmitt-trigger buffer implemented in eSim using available device model files.

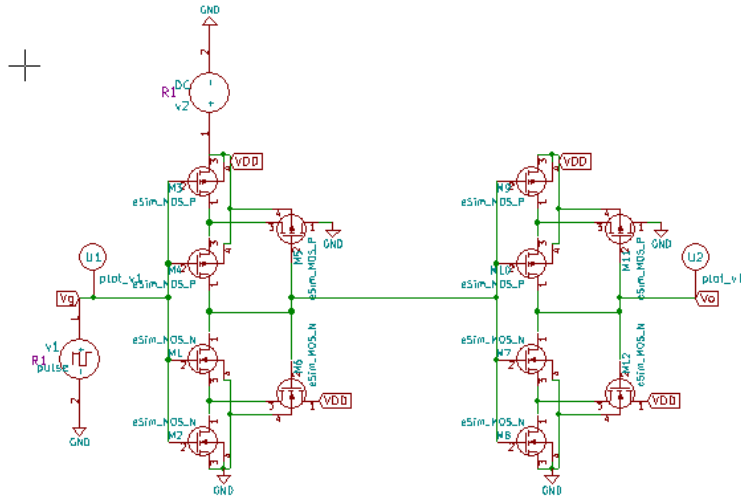


Figure 4.3: IC Layout of the 74LVC1G17

4.1.7 Input Plot

Figure 4.4 shows the input waveform applied to the IC in the test circuit.

4.1.8 Output Plot

Figure 4.4 shows the output waveform obtained from the IC in the test circuit.

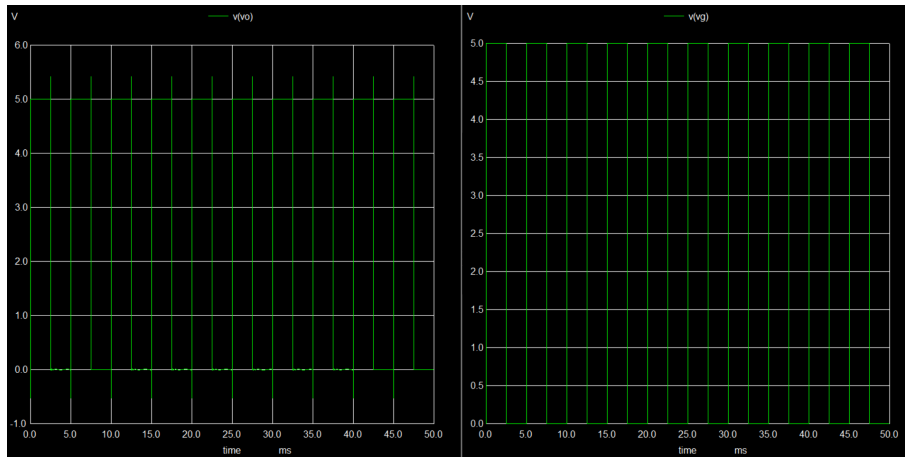


Figure 4.4: Input and Output Plot for 74lvc1g17 Test Circuit

4.2 CD40106BC / CD40106B – CMOS Hex Schmitt-Trigger Inverters

4.2.1 General Description

The CD40106BC / CD40106B device contains six independent inverters with Schmitt-trigger inputs. Each inverter performs the Boolean function $Y = \overline{A}$ in positive logic. The Schmitt-trigger inputs provide hysteresis, which ensures a minimum separation between positive and negative switching thresholds. This feature allows the device to handle noisy or slow input signals without causing oscillation or excessive current consumption.

4.2.2 Key Features

- Six independent Schmitt-trigger inverters in a single IC
- Wide operating voltage range: 3 V to 18 V
- Low quiescent current: 20 μ A (tested at 20 V)
- Operating temperature range: -55°C to $+125^{\circ}\text{C}$
- High noise immunity due to Schmitt-trigger inputs
- Standardized symmetrical output characteristics

4.2.3 Applications

- Signal conditioning and waveform shaping
- Debouncing switches or push-buttons
- Noise filtering for digital logic signals
- Level detection for sensors or slow input signals
- Interfacing between different logic voltage levels

4.2.4 Pin Configuration

Figure 4.5 shows the pin configuration of the CD40106B.

4.2.5 IC Layout

Figure 4.6 shows the internal IC layout of the CD40106B device.

4.2.6 Subcircuit Schematic Diagram

Figure 4.7 illustrates the subcircuit schematic diagram of the CD40106B as implemented in eSim.

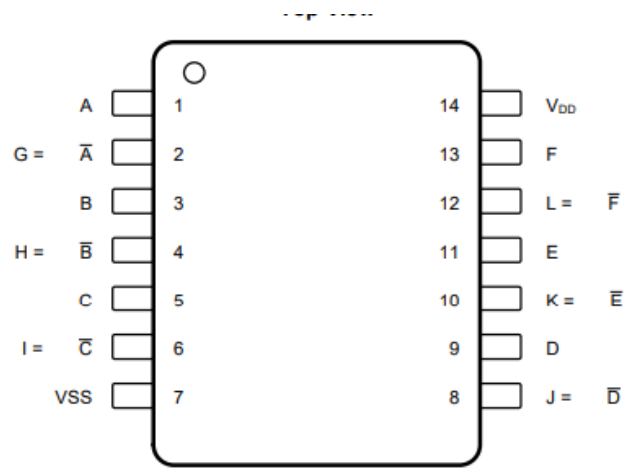


Figure 4.5: Pin Configuration of CD40106B

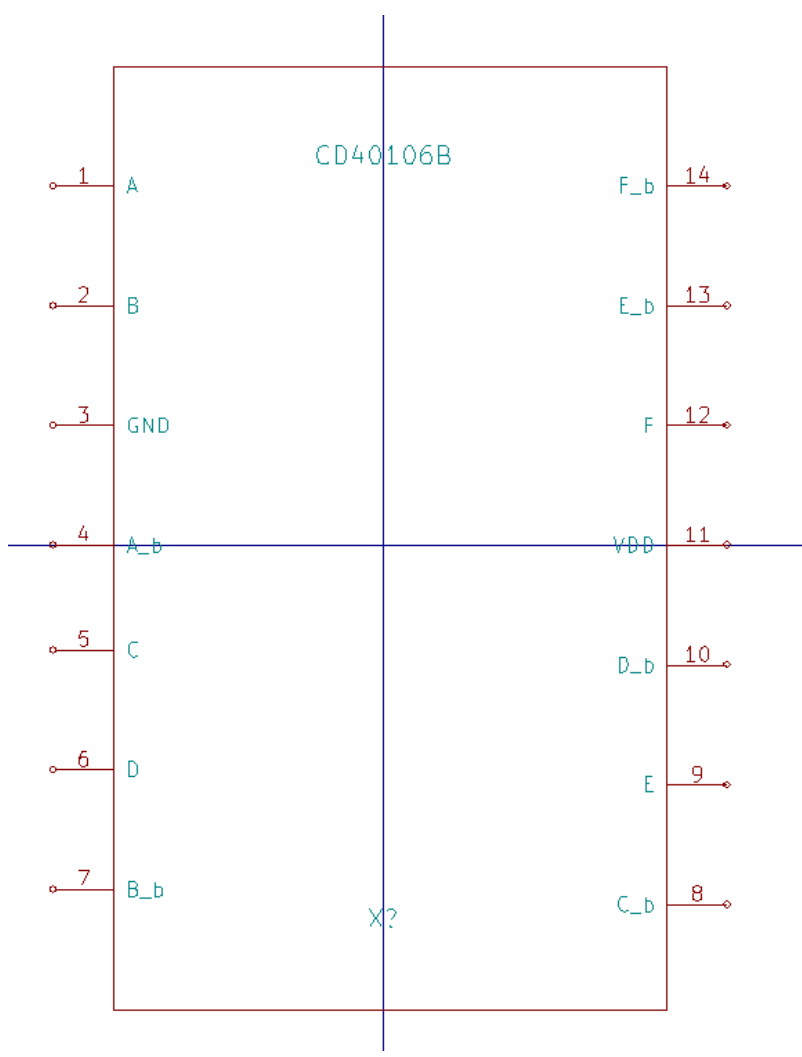


Figure 4.6: IC Layout of CD40106B

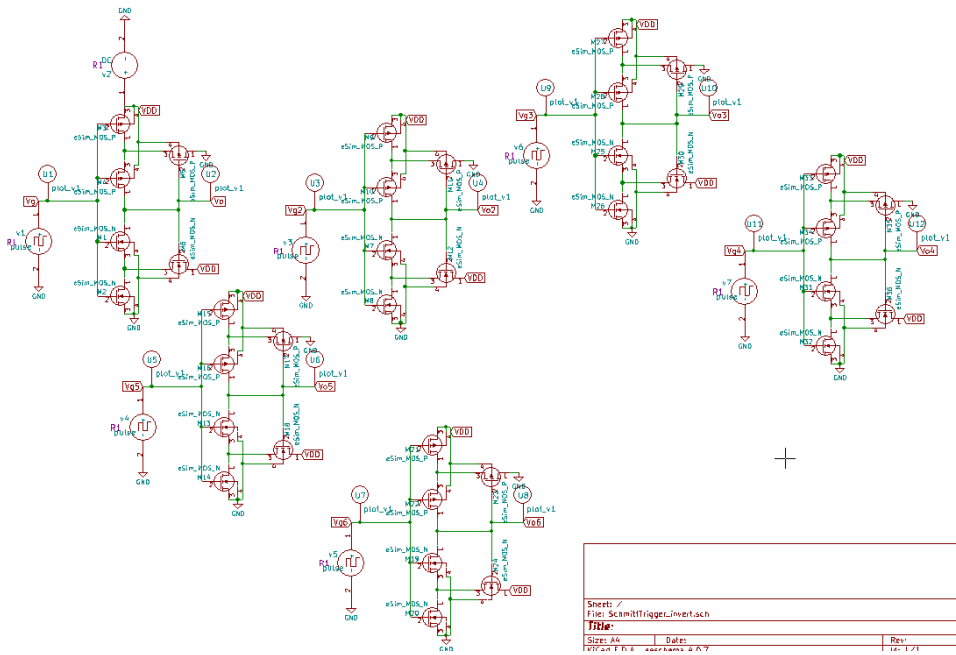


Figure 4.7: Subcircuit Schematic Diagram of CD40106B

4.2.7 Input Plot

Figure 4.8 shows the input waveform applied to the IC in the test circuit.

4.2.8 Output Plot

Figure 4.8 shows the output waveform obtained from the IC in the test circuit.

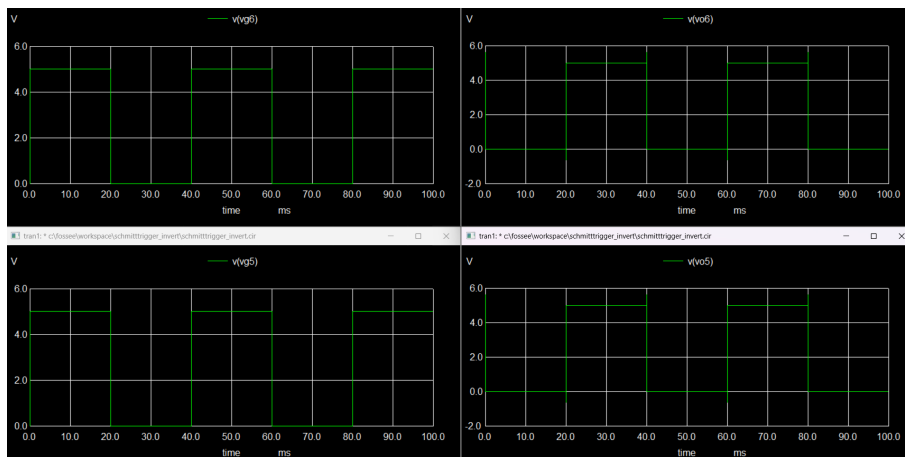


Figure 4.8: Output and Input Plot for CD40106B Test Circuit

4.3 74LVC2G00 – Dual 2-Input NAND Gate / SN74LVC2G00 Dual 2-Input Positive-NAND Gate

4.3.1 General Description

The SN74LVC2G00 is a dual 2-input positive-NAND gate designed for low-voltage CMOS logic applications. It operates over a wide supply voltage range from 1.65 V to 5.5 V, making it suitable for both low-power and high-performance digital systems. The device performs the Boolean function

$$Y = \overline{A \cdot B}$$

for each gate in positive logic.

The device incorporates NanoFree™ package technology and supports partial power-down operation using the *Ioff* feature, preventing damaging current backflow during power-off conditions.

4.3.2 Key Features

- Wide operating voltage range: 1.65 V to 5.5 V
- Inputs accept voltages up to 5.5 V
- Maximum propagation delay of 4.3 ns at 3.3 V
- Low power consumption (10 μ A max ICC)
- ± 24 mA output drive capability at 3.3 V
- NanoFree™ compact package technology
- *Ioff* support for live insertion and partial power-down

4.3.3 Applications

- Optical networking and communication systems
- IP phones and telecom equipment
- DC/DC power modules
- Digital signal processing systems
- Logic level translation circuits

4.3.4 Pin Configuration

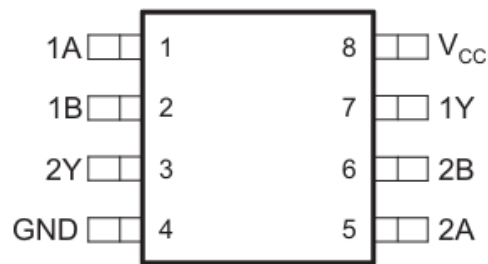


Figure 4.9: Pin Configuration of the SN74LVC2G00 Dual NAND Gate

4.3.5 IC Layout

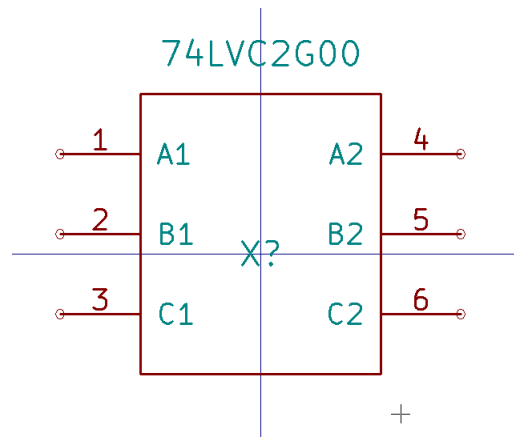


Figure 4.10: IC Layout of the SN74LVC2G00 Dual NAND Gate

4.3.6 Subcircuit Schematic Diagram

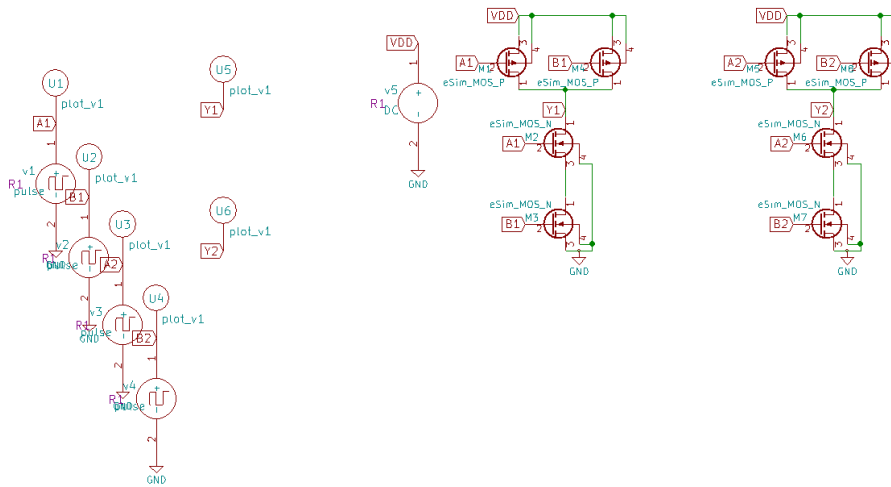


Figure 4.11: Subcircuit Schematic Diagram of the SN74LVC2G00

4.3.7 Input and output Waveform

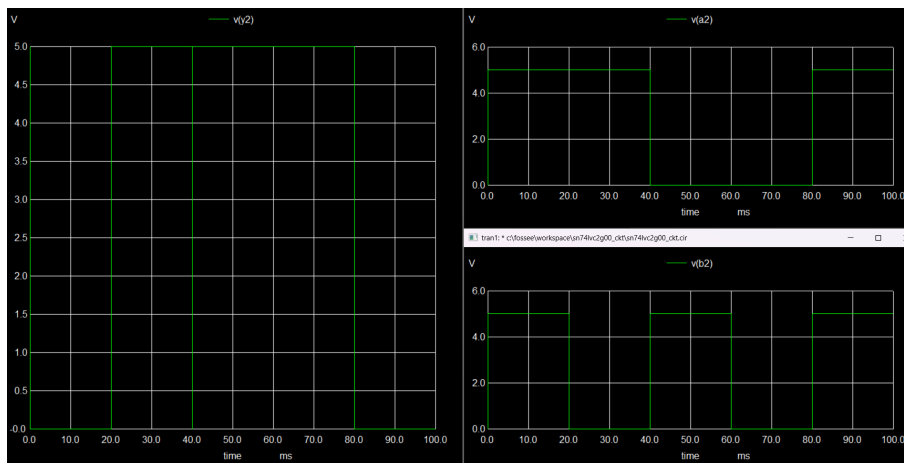


Figure 4.12: Input Waveforms Applied to the SN74LVC2G00 NAND Gate to get Output

4.4 74ALS10A – Triple 3-Input NAND Gate / SN74ALS10A

4.4.1 General Description

The SN74ALS10A is a triple 3-input positive-NAND gate designed using advanced bipolar technology for high-speed digital logic applications. Each device contains three independent 3-input NAND gates that perform the Boolean function

$$Y = \overline{A \cdot B \cdot C}$$

in positive logic.

The SN74ALS10A operates over a supply voltage range of 4.5 V to 5.5 V and is characterized for operation over the commercial temperature range of 0°C to 70°C. Its fast switching characteristics make it suitable for timing-critical applications in digital systems.

4.4.2 Key Features

- Contains three independent 3-input NAND gates
- Operates from 4.5 V to 5.5 V
- High-speed bipolar logic technology
- Low power dissipation compared to standard TTL
- TTL-compatible input and output levels
- Reliable operation over commercial temperature range

4.4.3 Applications

- Digital control systems
- Timing and sequencing circuits
- Address decoding logic
- Arithmetic and logic units (ALUs)
- Industrial and communication systems

4.4.4 Pin Configuration

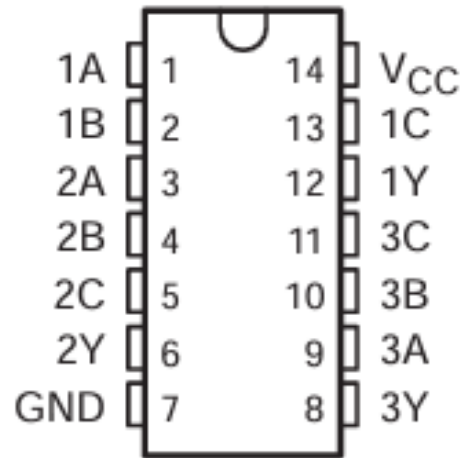


Figure 4.13: Pin Configuration of the SN74ALS10A Triple 3-Input NAND Gate

4.4.5 Input Waveform

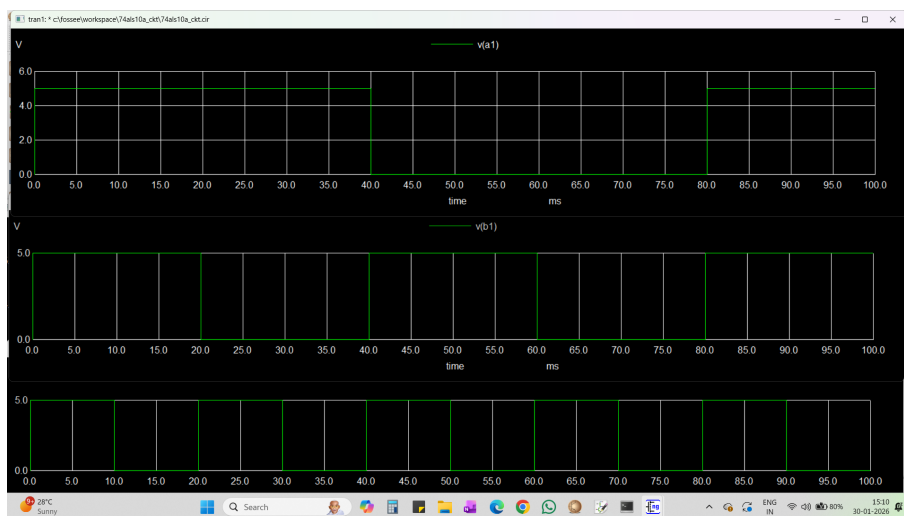


Figure 4.14: Input Waveforms Applied to the SN74ALS10A NAND Gate

4.4.6 Output Waveform

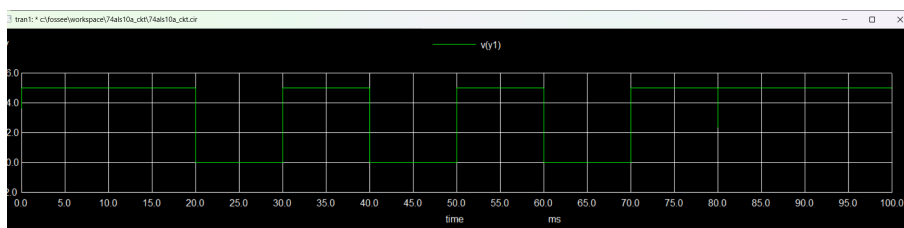


Figure 4.15: Output Waveform of the SN74ALS10A NAND Gate

4.5 SN74LVC3G17 – Triple Schmitt-Trigger Buffer

4.5.1 General Description

The SN74LVC3G17 is a triple non-inverting Schmitt-trigger buffer designed for high-speed digital signal conditioning. The device contains three independent buffers, each performing the Boolean function $Y = A$.

Schmitt-trigger inputs provide hysteresis with different positive-going (V_{T+}) and negative-going (V_{T-}) threshold voltages, enabling reliable operation with slow-rising, noisy, or distorted input signals. This makes the device particularly suitable for signal conditioning and waveform shaping applications.

The SN74LVC3G17 operates over a wide supply voltage range from 1.65 V to 5.5 V and supports inputs up to 5.5 V regardless of the supply voltage. The device is fully specified for partial-power-down applications using the I_{off} feature, which disables the outputs when $V_{CC} = 0$ V, preventing current backflow through the device.

Fabricated using NanoFree™ package technology, the SN74LVC3G17 offers reduced power consumption, high output drive capability, and excellent ESD and latch-up protection, making it suitable for modern low-power digital systems.

4.5.2 Key Features

- Triple independent non-inverting Schmitt-trigger buffers
- Wide operating voltage range: 1.65 V to 5.5 V
- Inputs accept voltages up to 5.5 V
- Maximum propagation delay of 5.4 ns at 3.3 V
- Low power consumption: 10 μ A maximum ICC
- ± 24 mA output drive capability at 3.3 V
- I_{off} supports live insertion and partial power-down
- High ESD protection and latch-up immunity
- Available in NanoFree™ packages

4.5.3 Applications

- Signal conditioning and noise filtering
- Waveform shaping for digital signals
- Audio and video equipment
- Portable consumer electronics
- Solid-state drives and data storage systems

- Telecommunications and server power supplies
- Wireless peripherals such as keyboards and mice

4.5.4 Pin Configuration

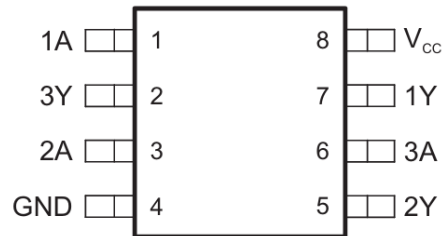


Figure 4.16: Pin Configuration of the SN74LVC3G17

4.5.5 IC Layout

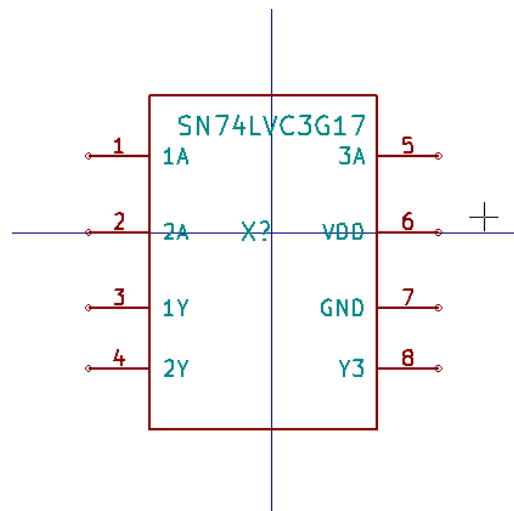


Figure 4.17: IC Layout of the SN74LVC3G17

4.5.6 Subcircuit Schematic Diagram

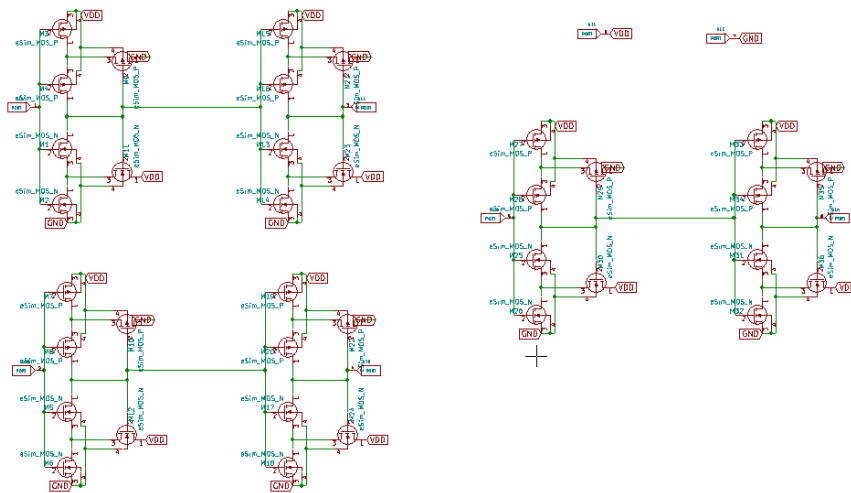


Figure 4.18: Subcircuit Schematic Diagram of the SN74LVC3G17

4.5.7 Input and Output Waveform

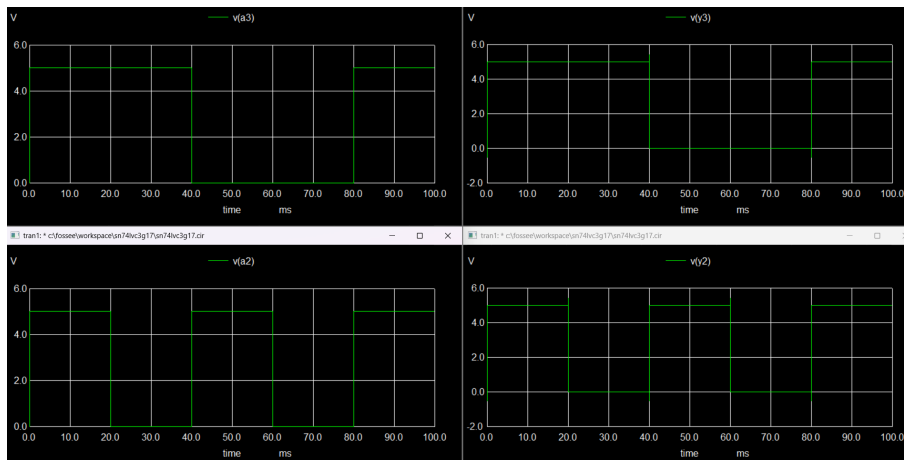


Figure 4.19: Input Waveform Applied to the SN74LVC3G17 to get Output

4.6 PI3B16244 – 16-Bit 4-Port Bus Switch

4.6.1 General Description

The PI3B16244 is a 16-bit, 4-port bus switch manufactured by Pericom Semiconductor. It is pin-compatible with the 74-series 16244 16-bit bus driver and provides near-zero propagation delay by using low on-resistance CMOS switches.

Four active-low bus enable (*nBE*) signals control the data paths, allowing inputs to be connected directly to outputs when enabled. The device introduces no additional ground bounce noise, making it suitable for high-speed data switching applications.

4.6.2 Key Features

- Near-zero propagation delay
- 5 Ω low on-resistance switches
- Fast switching speed: 4 ns (maximum)
- Pin compatible with 74-series 16244
- Operating voltage range: 3.0 V to 3.6 V
- Industrial temperature range: -40°C to $+85^{\circ}\text{C}$

4.6.3 Applications

- High-speed bus switching
- Data routing in digital systems
- Memory interfacing
- Notebook and portable electronics

4.6.4 Pin Configuration

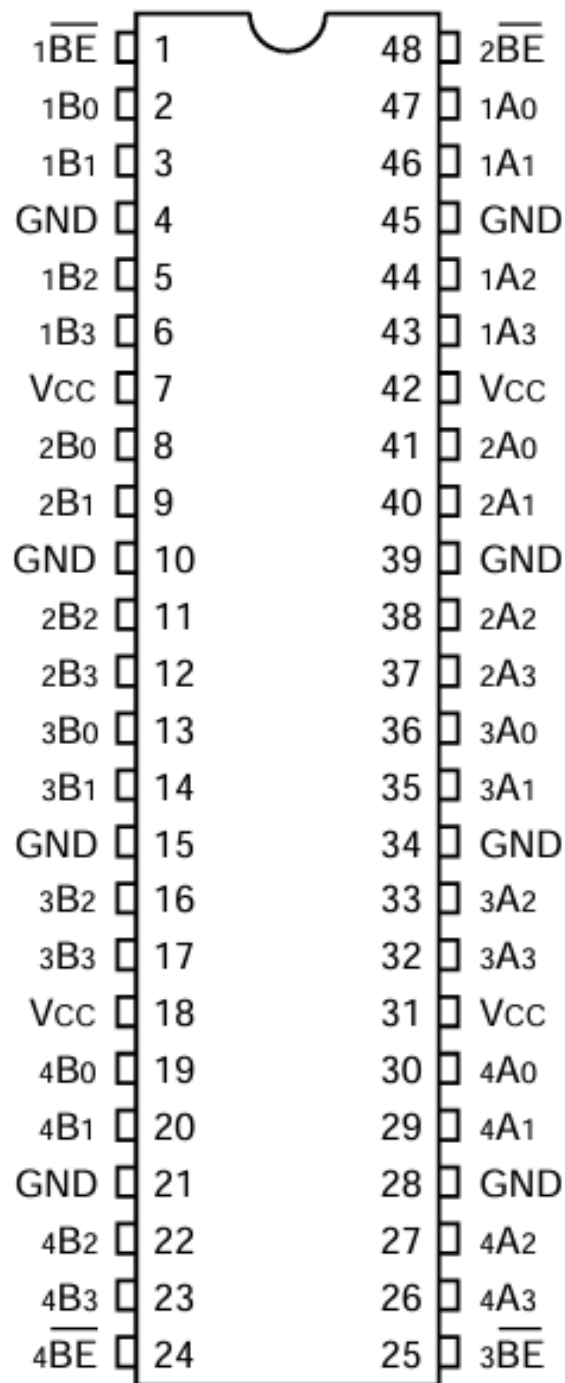


Figure 4.20: Pin Configuration of PI3B16244

4.6.5 IC Layout

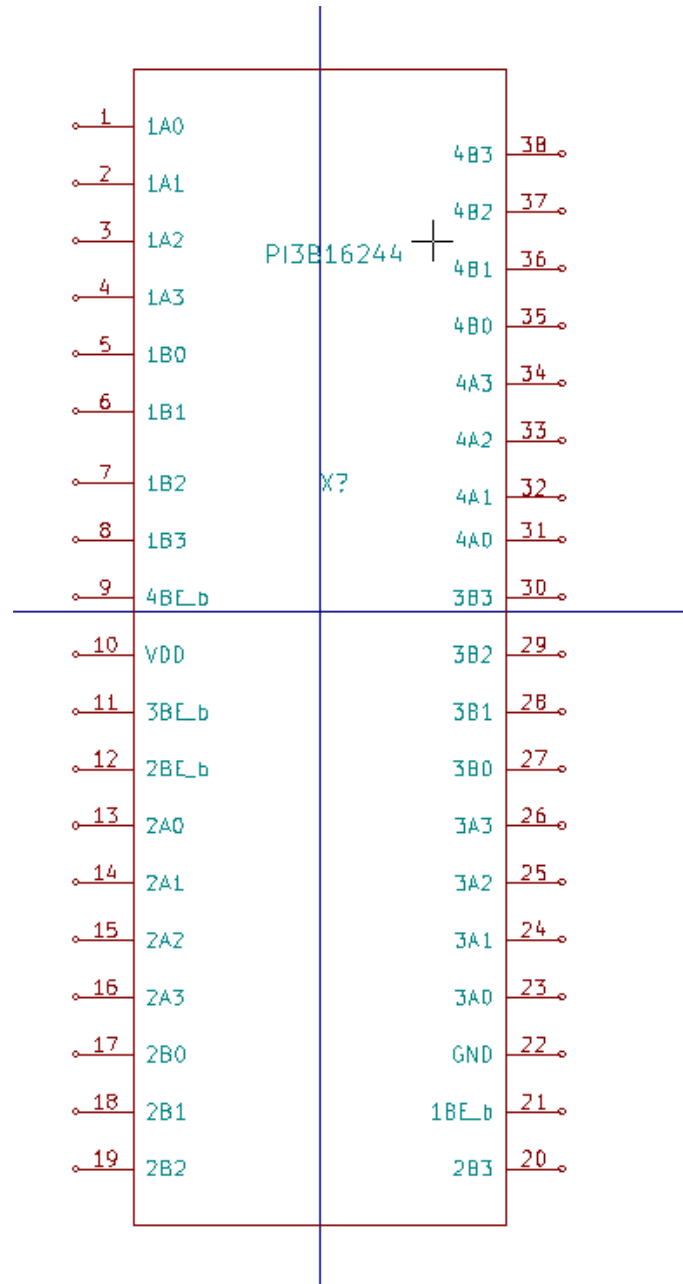


Figure 4.21: IC Layout of PI3B16244

4.6.6 Subcircuit Schematic Diagram

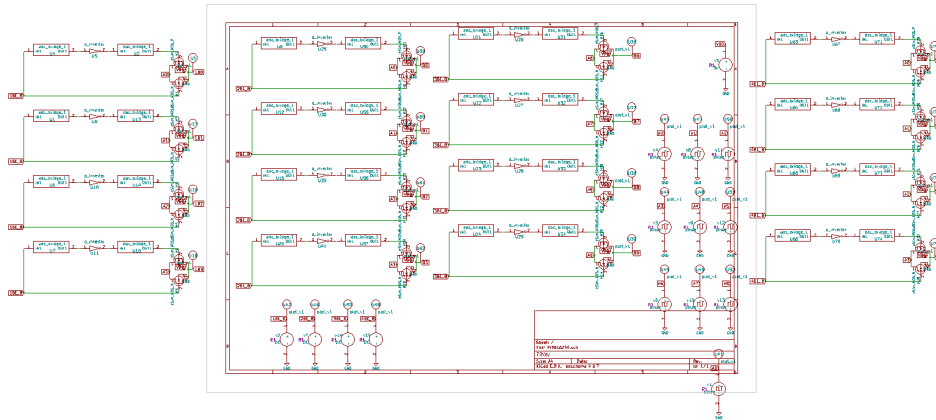


Figure 4.22: Subcircuit Diagram of PI3B16244

4.6.7 Input Waveform

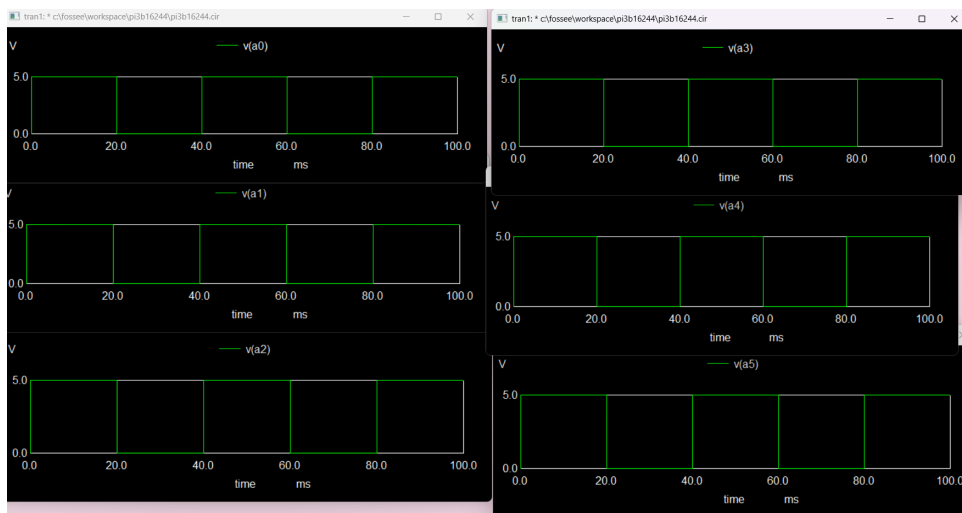


Figure 4.23: Input Waveform of PI3B16244

4.6.8 Output Waveform

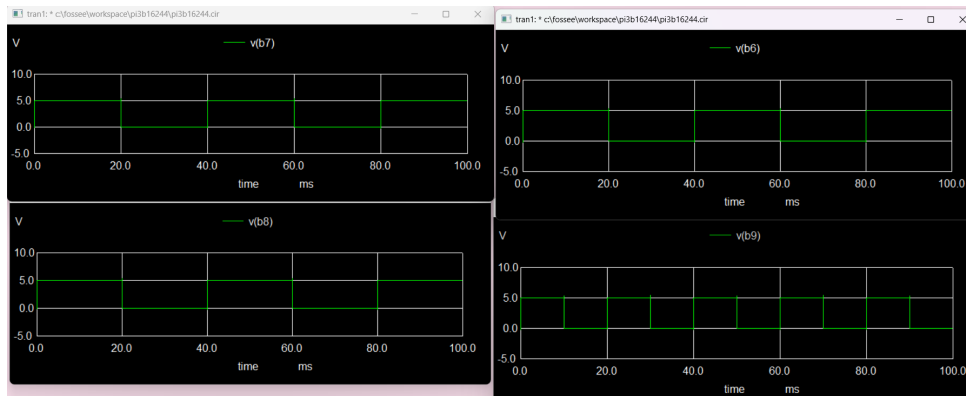


Figure 4.24: Output Waveform of PI3B16244

4.7 PI3B3384 – High-Speed Bus Switch

4.7.1 General Description

The PI3B3384 is a high-speed bus switch designed for low propagation delay and minimal signal distortion. It uses low on-resistance CMOS switches to directly connect inputs to outputs when enabled.

The device is optimized for high-frequency digital signal routing and introduces negligible propagation delay and ground bounce noise.

4.7.2 Key Features

- Near-zero propagation delay
- 5 Ω low on-resistance switches
- Fast switching speed: 4 ns (maximum)
- Operating voltage range: 3.0 V to 3.6 V
- Industrial temperature range: -40°C to $+85^{\circ}\text{C}$

4.7.3 Applications

- High-speed data buses
- Digital signal multiplexing
- Communication systems
- Portable electronic devices

4.7.4 Pin Configuration

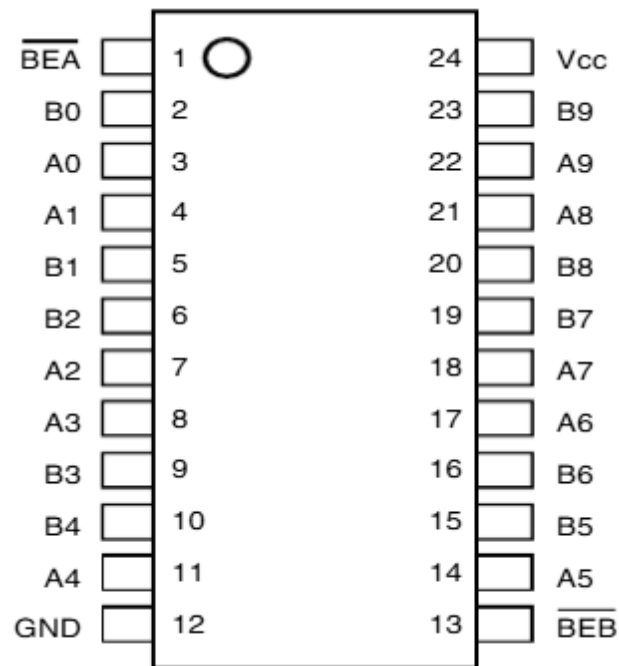


Figure 4.25: Pin Configuration of PI3B3384

4.7.5 IC Layout

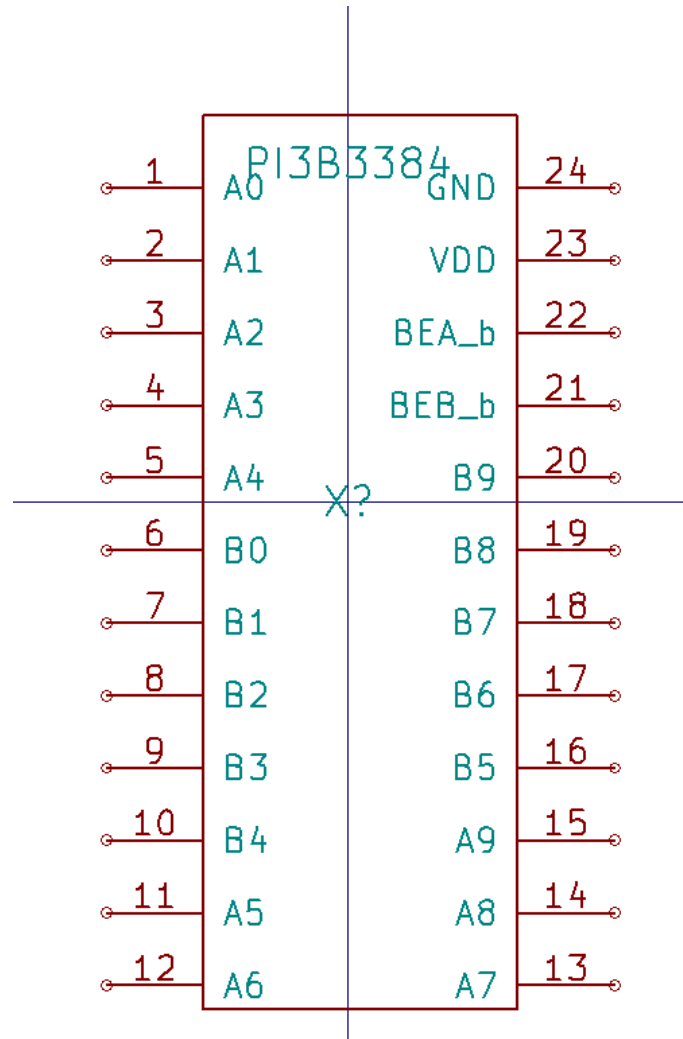


Figure 4.26: IC Layout of PI3B3384

4.7.6 Subcircuit Schematic Diagram

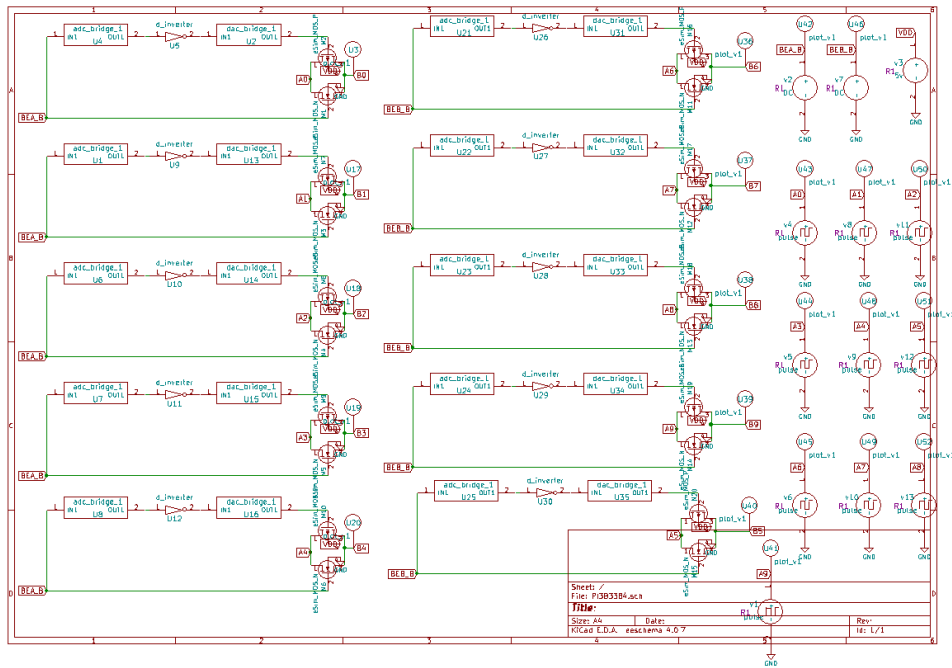


Figure 4.27: Subcircuit Diagram of PI3B3384

4.7.7 Input Waveform



Figure 4.28: Input Waveform of PI3B3384

4.7.8 Output Waveform

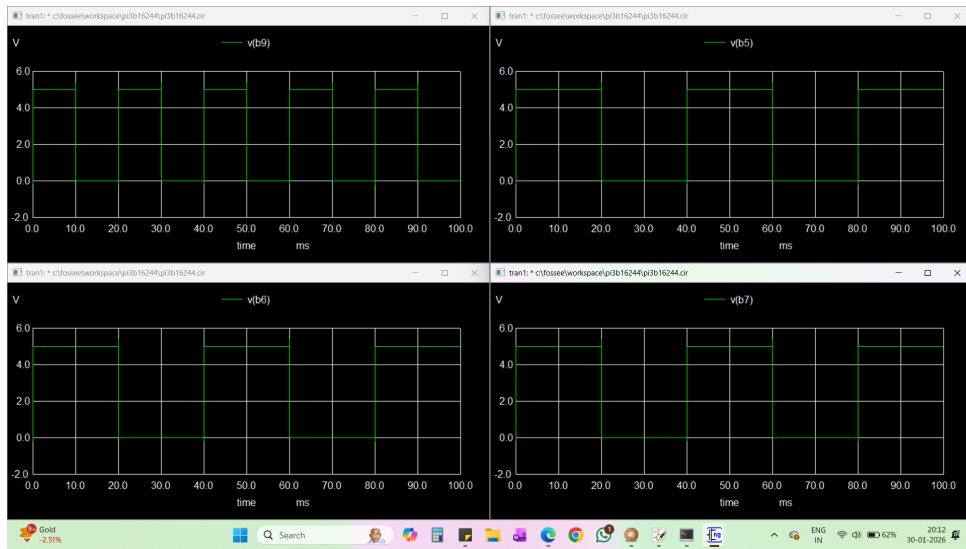


Figure 4.29: Output Waveform of PI3B3384

4.8 PI3B3861 – 10-Bit 2-Port Bus Switch

4.8.1 General Description

The PI3B3861 is a 10-bit, 2-port bus switch operating at 3.3 V. It is designed with low on-resistance CMOS switches that allow direct connection between inputs and outputs.

The device introduces no additional propagation delay or ground bounce noise and is enabled through a Bus Enable (BE) control signal.

4.8.2 Key Features

- Near-zero propagation delay
- 5 Ω low on-resistance switches
- Fast switching speed: 4.5 ns (maximum)
- Ultra-low quiescent power: 0.1 μA (typical)
- Optimized for notebook applications

4.8.3 Applications

- Notebook and portable systems
- High-speed data routing
- Signal multiplexing

4.8.4 Pin Configuration

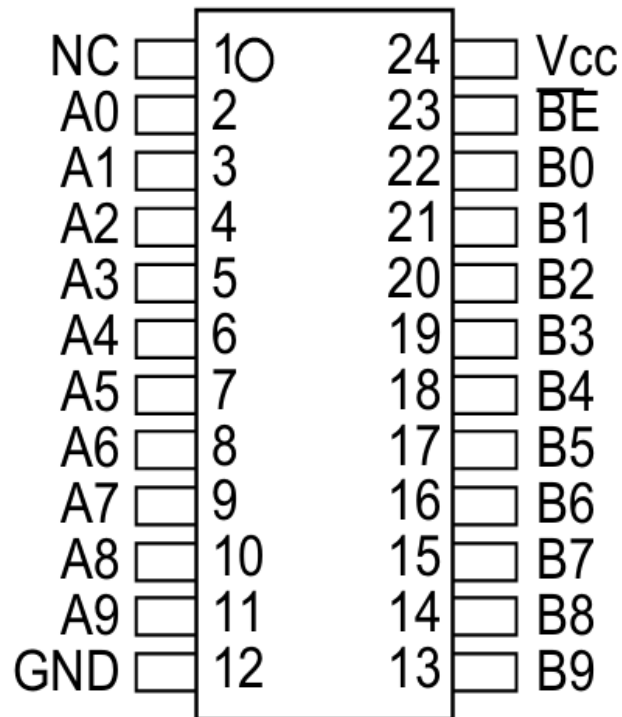


Figure 4.30: Pin Configuration of PI3B3861

4.8.5 Subcircuit Schematic Diagram

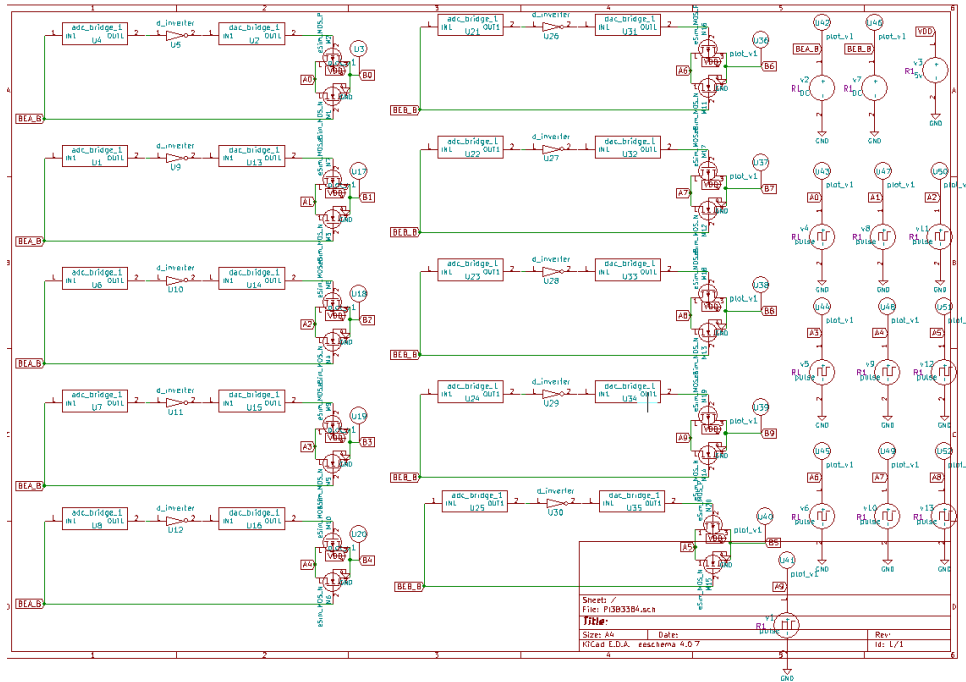


Figure 4.31: Subcircuit Diagram of PI3B3861

4.8.6 Input and Output Waveform



Figure 4.32: Input and output Waveform of PI3B3861

4.9 ICS83840 – DDR SDRAM MUX

4.9.1 General Description

The ICS83840 is a DDR SDRAM multiplexer belonging to the HiPerClockS™ family of high-performance clock solutions. The device consists of 10 host lines, each capable of driving four data ports.

It supports SSTL-2 compatible signaling and operates from a 2.5 V supply. Low output skew and precise timing characteristics make the ICS83840 suitable for demanding DDR memory applications.

4.9.2 Key Features

- 40 low-skew single-ended DIMM ports
- SSTL-2 compatible inputs and outputs
- Maximum switching speed: 3 ns
- Output skew: 120 ps (maximum)
- Bank skew: 45 ps (maximum)
- Typical on-resistance: 8 Ω
- 2.5 V operation

4.9.3 Applications

- DDR SDRAM interfaces
- Memory multiplexing
- High-performance computing systems
- Server and embedded memory subsystems

4.9.4 Pin Configuration

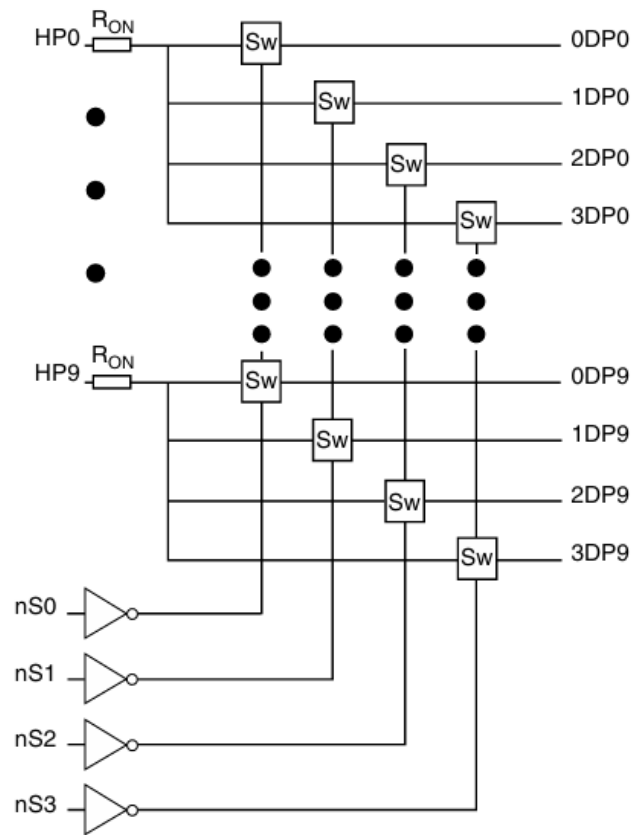


Figure 4.33: Pin Configuration of ICS83840

4.9.5 IC Layout

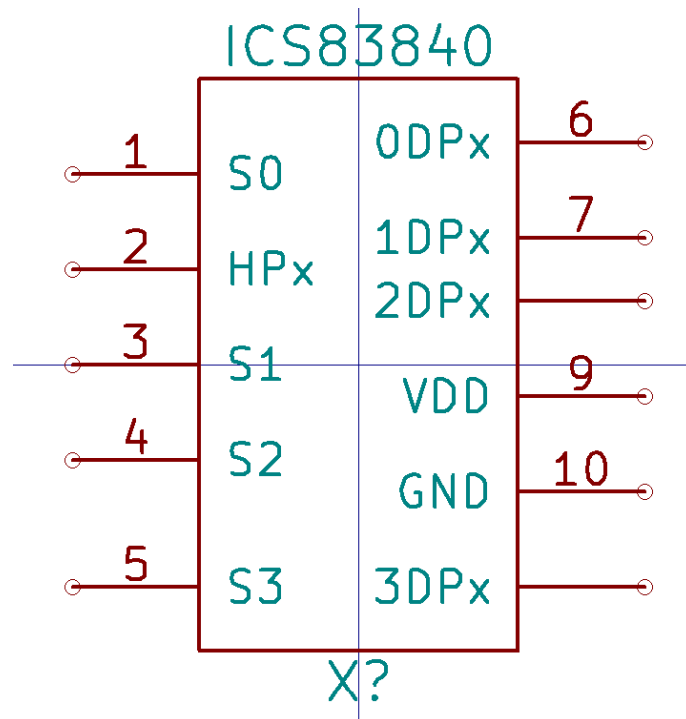


Figure 4.34: IC Layout of ICS83840

4.9.6 Subcircuit Schematic Diagram

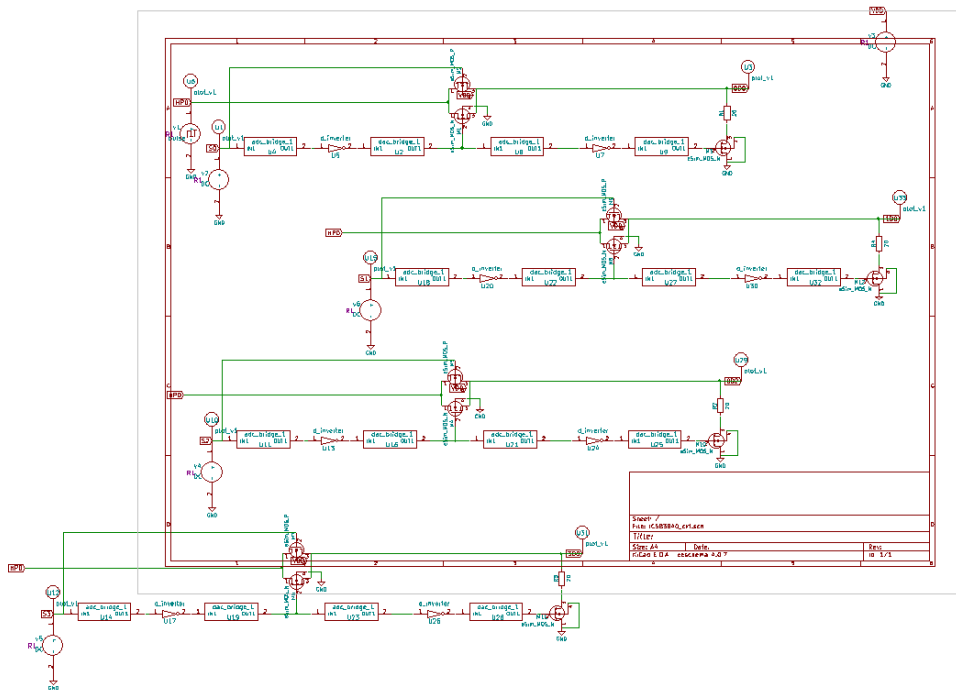


Figure 4.35: Subcircuit Diagram of ICS83840

4.9.7 Input Waveform

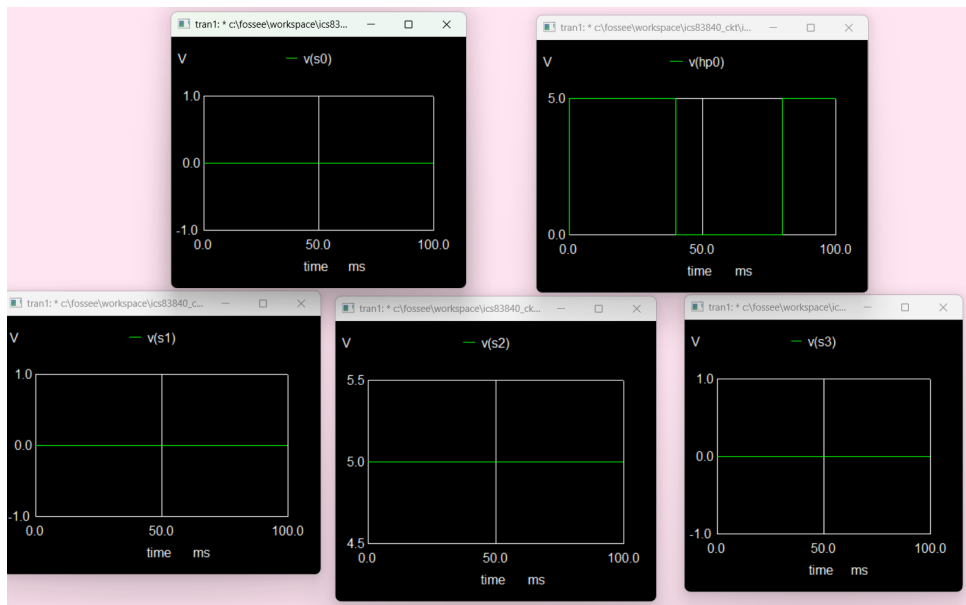


Figure 4.36: Input Waveform of ICS83840

4.9.8 Output Waveform

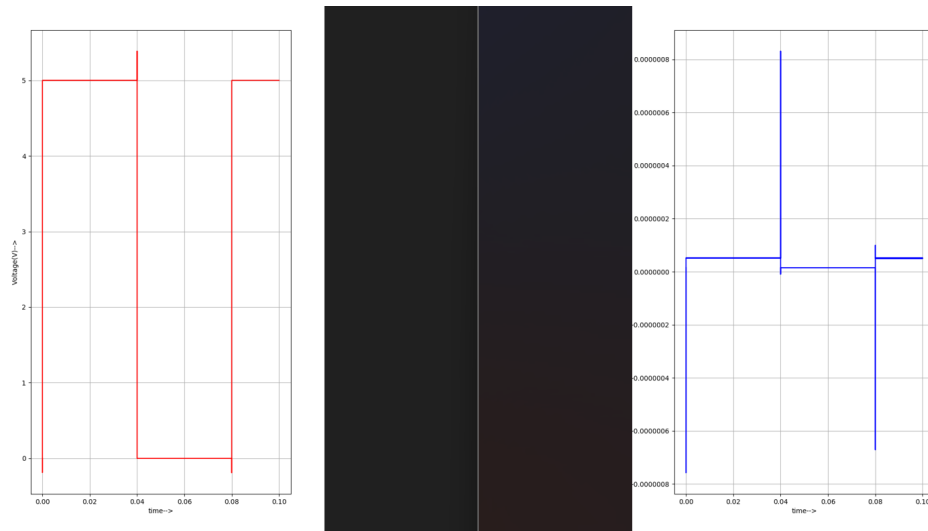


Figure 4.37: Output Waveform of ICS83840

4.10 SNx4HC574 – Octal edge-triggered D-type flip-flop

4.10.1 General Description

The SNx4HC574 is an octal edge-triggered D-type flip-flop with 3-state outputs. It is designed for bus-oriented storage applications and operates on the positive edge of the clock. The device provides non-inverting outputs and features an output enable control to place the outputs in a high-impedance state when required.

4.10.2 Key Features

- Octal D-type edge-triggered flip-flop
- Positive edge-triggered clock operation
- 3-state outputs for bus interfacing
- Non-inverting data outputs
- High-speed CMOS technology
- Low power consumption

4.10.3 Applications

- Bus-oriented registers
- Data storage buffers
- I/O port latching
- Microprocessor-based systems
- Memory address/data buffering

4.10.4 Pin Configuration

Figure 4.38 shows the pin configuration of the SNx4HC574 IC.

Figure 4.38: Pin Configuration of SNx4HC574

Chapter 5

Failed Integrated Circuits

5.0.1 Overview

This section documents the integrated circuits that could not be successfully implemented or verified in eSim. The failures were primarily due to missing internal subcircuit definitions, incorrect behavioral modeling, and mismatches between digital logic operation and analog signal behavior. Each failed IC is analyzed with respect to its intended functionality, observed issue, and limitations encountered during simulation.

5.0.2 Failed Circuit 1: CD4511 / HEF4511B

Circuit Description

The CD4511 (HEF4511B) is a BCD to 7-segment latch, decoder, and driver IC. It accepts a 4-bit BCD input and drives seven output lines corresponding to a 7-segment display. The device includes latch enable, ripple blanking, and lamp test control inputs for flexible display control.

Circuit Diagram

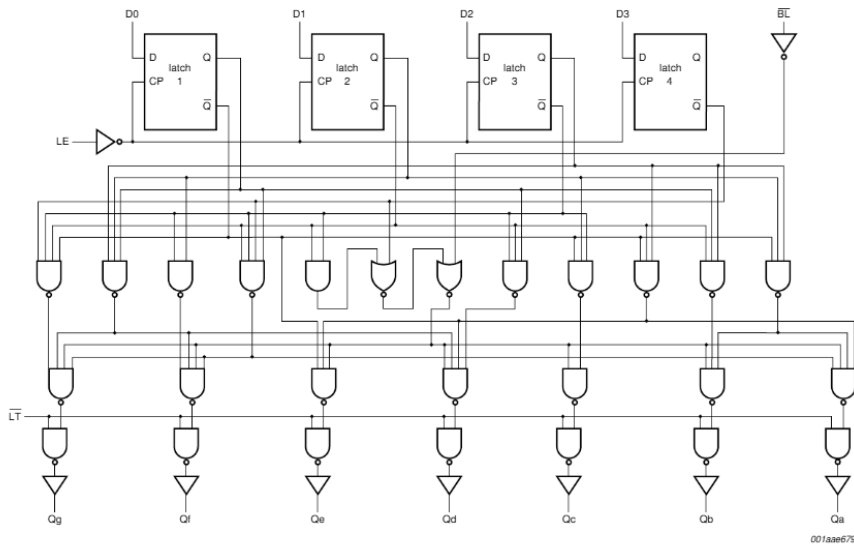


Figure 5.1: CD4511 Internal Circuit Diagram

eSim Circuit Diagram

Issue Description

Although the CD4511 symbol was available in eSim, the internal subcircuit required for simulation was already pre-existing but not functionally complete. The latch and decoder logic did not respond correctly to BCD inputs, resulting in incorrect or static segment outputs. Due to this limitation, proper verification of the IC behavior was not possible.

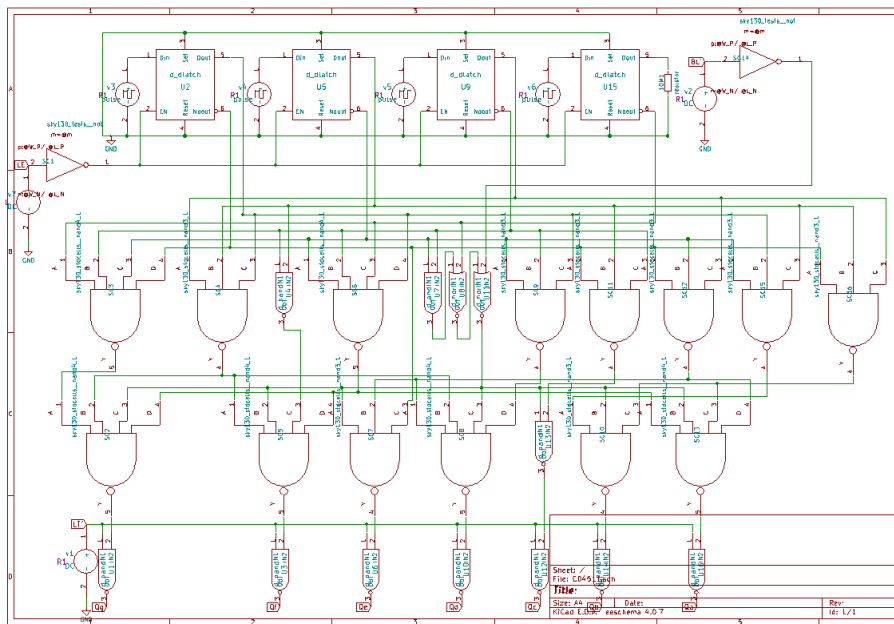


Figure 5.2: CD4511 eSim Implementation Showing Simulation Error

5.0.3 Failed Circuit 2: CDx4HC241 and CD74HC240 Variant

Circuit Description

The CD74HC241 is a non-inverting three-state buffer with mixed active-high and active-low output enable inputs. It is widely used for bus isolation and data buffering applications.

Circuit Diagram

eSim Circuit Diagram

Issue Description

The datasheet does not provide internal buffer subcircuits, and the eSim model lacked proper internal implementation. As a result, the output enable functionality did not behave correctly, leading to constant high-impedance or undefined output states during simulation.

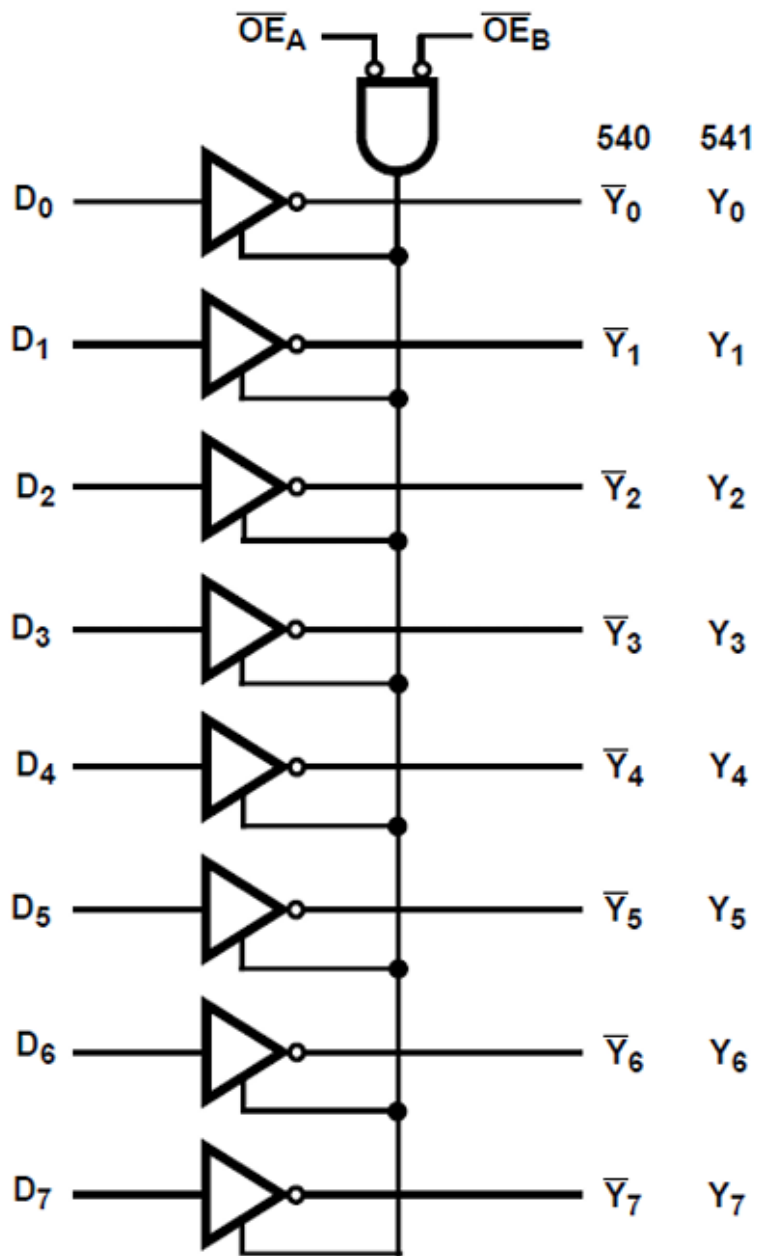


Figure 5.3: CD74HC241 Logic Diagram

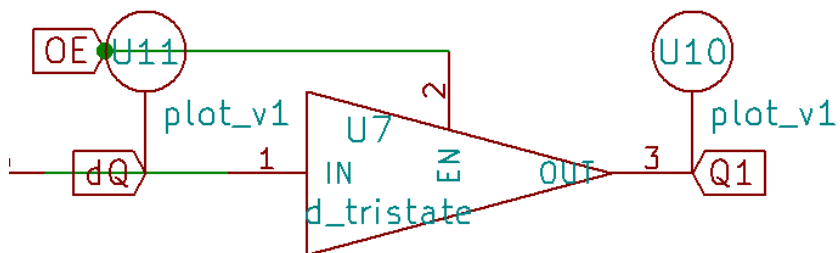


Figure 5.4: CD74HC241 eSim Circuit with Simulation Error

Chapter 6

Conclusion and Future Scope

6.1 Conclusion

In conclusion, the integrated circuits studied in this project play a vital role as fundamental building blocks in digital and electronic systems. They provide reliable, efficient, and predictable operation across a wide range of operating conditions. Their functional characteristics—such as stable logic behavior, low power consumption, compatibility with standard logic levels, and dependable switching performance—enable seamless integration into complex electronic systems.

Throughout this work, the functional behavior, pin configurations, applications, and limitations of various digital ICs were analyzed and implemented using eSim. Successful simulations demonstrated the importance of proper subcircuit modeling and accurate logic representation, while failed implementations highlighted practical challenges such as missing internal architectures, digital–analog mismatches, and incomplete behavioral descriptions in simulation environments.

Overall, the studied devices proved to be robust and versatile components suitable for educational experiments, prototyping, and industrial-level electronic designs. Their well-defined electrical specifications and architectural simplicity simplify system design and enhance reliability in data processing, control, timing, and interfacing applications.

6.2 Future Scope

The scope of this work can be extended in several directions to enhance functionality, accuracy, and real-world applicability:

- Integration of the studied ICs with microcontrollers or programmable logic devices (PLDs) to develop intelligent and automated control systems.
- Expansion of simulations to include real-time sensor interfacing for applications in embedded systems and Internet of Things (IoT) platforms.
- Development of custom subcircuit models for failed ICs to improve simulation accuracy in eSim.
- Cascading multiple ICs to implement higher-order logic functions, counters, registers, and complex data-path architectures.
- Optimization of power consumption for battery-operated and low-power embedded applications.
- Inclusion of protection, filtering, and signal-conditioning circuits to improve noise immunity and operational robustness.
- Hardware validation by implementing the simulated circuits on breadboards or PCBs for real-world performance comparison.
- Exploration of advanced simulation tools and mixed-signal modeling techniques to overcome digital–analog mismatch issues.

With continuous advancements in embedded technology, automation, and smart systems, these integrated circuits will remain relevant as reliable elements in timing, control, interfacing, and signal-processing applications.

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