eSim Semester Long Internship-Autumn 2025

On

IC Design Using Subcircuit in eSim

Submitted by

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Acknowledgment

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Chapter 1

Introduction

FOSSEE, abbreviated as Free/Libre and Open Source Software for Education, is an initiative based at IIT Bombay that focuses on promoting the use of open-source software in academic and research domains. The primary objective of FOSSEE is to reduce reliance on proprietary software by providing high-quality open-source alternatives. Through its efforts, FOSSEE supports students, educators, and researchers by offering a variety of software tools that address diverse technical and educational requirements.

The organization provides detailed documentation, tutorials, workshops, and practical training programs to enable effective adoption of open-source technologies. By encouraging collaboration and knowledge sharing, FOSSEE has played a significant role in making advanced technological resources accessible to a wider audience. This approach has helped create an inclusive learning environment while fostering innovation and skill development.

FOSSEE operates under the National Mission on Education through Information and Communication Technology (NME-ICT), an initiative of the Ministry of Education, Government of India. As part of this mission, FOSSEE has successfully developed and maintained multiple open-source software platforms that enhance the quality of education. These tools are freely available and are continuously updated to ensure they remain robust, reliable, and comparable to commercial software solutions.

1.1 eSim

eSim, developed under the FOSSEE initiative at IIT Bombay, is a powerful opensource software tool used for electronic circuit design and simulation. It integrates multiple open-source applications into a single unified environment, enabling users to efficiently design, simulate, and analyze electronic circuits. The software serves as a cost-effective and accessible alternative to proprietary Electronic Design Automation (EDA) tools, making it especially beneficial for students, educators, and practicing engineers.

The platform supports schematic capture, circuit simulation, and PCB design, and provides a comprehensive library of electronic components. One of the key

features of eSim is the Subcircuit Builder, which allows users to create complex circuit designs by combining smaller functional blocks. This modular approach simplifies design reuse and enhances productivity. By offering such capabilities, eSim encourages the adoption of open-source tools in both academic learning and professional applications.

eSim functions as a Computer-Aided Design (CAD) tool that assists electronic system designers in developing, testing, and validating their circuit designs. Being open source, it allows users to customize and extend the software according to their specific requirements. Built using several free and open-source software components, eSim provides a flexible and extensible framework for experimenting with and understanding electronic systems.

1.1.1 KiCad

KiCad is an open-source software suite used for electronic design automation, primarily for schematic capture and printed circuit board (PCB) layout. It provides a user-friendly environment that enables designers to create and modify electronic schematics with ease. KiCad is widely used in both academic and industrial settings due to its reliability, flexibility, and free availability.

The software supports multi-layer PCB design and offers a comprehensive library of electronic components. KiCad also allows users to create custom symbols and footprints, making it adaptable to a wide range of design requirements. As an open-source tool, KiCad encourages community-driven development and continuous improvement, making it a valuable resource for electronics education and research.

1.1.2 Ngspice

Ngspice is an open-source mixed-level circuit simulation software derived from SPICE. It is used to perform various types of circuit analyses, including DC, AC, and transient simulations. Ngspice plays a crucial role in verifying circuit functionality and performance before hardware implementation.

The simulator supports analog, digital, and mixed-signal circuits, providing accurate and efficient simulation results. Its compatibility with multiple design tools makes it highly versatile. Being free and open source, Ngspice enables users to study, modify, and extend its capabilities, which is particularly beneficial for learning and experimentation in electronics.

1.1.3 KiCad to Ngspice Converter

The KiCad to Ngspice Converter is a utility that enables seamless integration between KiCad schematics and the Ngspice simulation engine. It converts schematic designs created in KiCad into Ngspice-compatible netlists, allowing users to simulate their circuits without manual intervention.

This conversion process ensures accuracy and consistency between the schematic and simulation stages. By automating the translation of circuit information, the converter simplifies the design workflow and reduces errors. This feature enhances productivity and makes the overall design and simulation process more efficient within the eSim environment..

Chapter 2

Abstract

The objective of this internship was to design and develop various integrated circuits using the Subcircuit Builder Method in eSim. This involved modeling the ICs with eSim library files and subsequently simulating them with different circuits. The goal was to expand the eSim Subcircuit Library for future use, enhancing its utility and application in educational and practical scenarios.

2.1 Approach

- Identify and research an integrated circuit (IC) that is not currently available in the eSim library.
- Obtain and study the datasheet of the selected IC thoroughly
- Carefully examine the schematic provided in the datasheet.
- Accurately recreate the schematic in eSim using the Subcircuit Builder Method.
- Model the IC in eSim, ensuring all parameters and configurations match those in the datasheet. • Simulate the integrated circuit within eSim, testing it with various circuits to verify its functionality.
- Document the process and results to contribute to the future use and expansion of the eSim Subcircuit Library.

2.2 Execution

The following information outline the method for creating a subcircuit in eSim 2.5 for the Windows version.

When eSim is launched, the main application window opens, and by default, all project files are stored in the eSim workspace. A new project is created within this workspace to begin the design process. After creating the project, the Subcircuit Builder environment is opened to start developing the required integrated circuit. A new subcircuit schematic is then created by providing an appropriate schematic

name. This opens the Eeschema window, where the internal circuit of the IC is recreated based on the corresponding datasheet. After completing the schematic and properly connecting all input and output ports, the schematic symbols are annotated to uniquely identify each component.

Once annotation is completed, a netlist is generated from the schematic. This netlist serves as an essential input for simulation and further processing within eSim. After generating the netlist, the design is converted into an NgSpicecompatible format using the KiCad to NgSpice conversion process.

During the conversion stage, suitable device models are added from the available model library based on the components used in the circuit. After successful modeling, a custom symbol for the designed subcircuit is created using the Symbol Editor. The device details are entered, and the pin diagram is drawn according to the datasheet specifications.

After completing the symbol creation, the subcircuit is used to build a test circuit for simulation. The schematic is then converted to NgSpice format, and simulation is performed. The output waveforms obtained from the simulation are analyzed and verified against the expected results provided in the datasheet to confirm correct functionality.

Chapter 3

Integrated Circuit Design

3.1 74HC00

3.1.1 Description

The 74HC00 is a high-speed CMOS integrated circuit consisting of four independent 2-input NAND gates. NAND gates are fundamental building blocks in digital electronics, as any Boolean logic function can be implemented using only NAND gates. This IC is designed using CMOS technology, which ensures low power consumption and high noise immunity compared to TTL-based logic families. The 74HC00 operates over a wide range of supply voltages, making it suitable for both low-voltage and standard digital systems. Due to its fast switching speed and reliable performance, it is commonly used in combinational logic circuits, control logic, clock generation circuits, and digital signal processing applications. In this work, the internal logic of the 74HC00 was modeled using basic logic elements and verified through simulation in eSim.

3.1.2 Pin Diagram

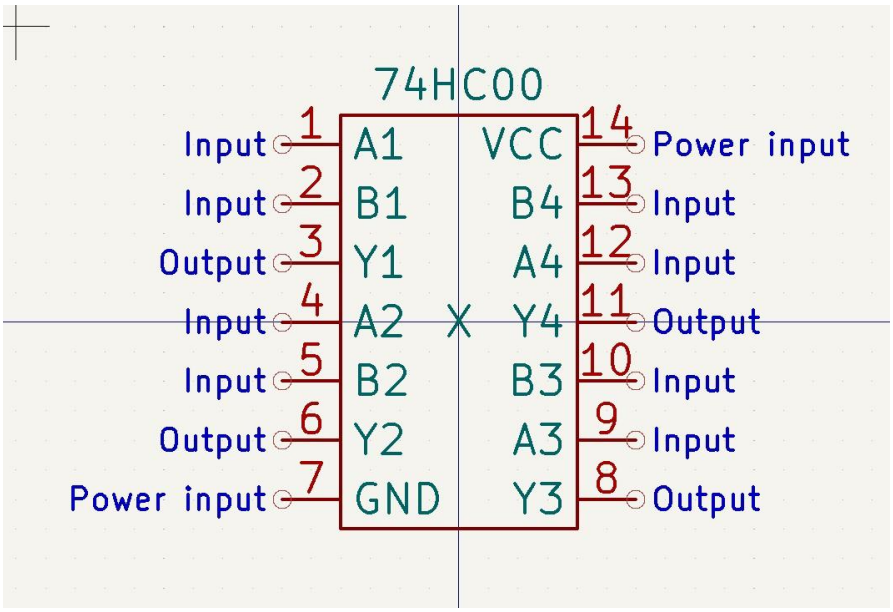

Figure 3.1: Pin Diagram of 74HC00

3.1.3 Schematic Diagram

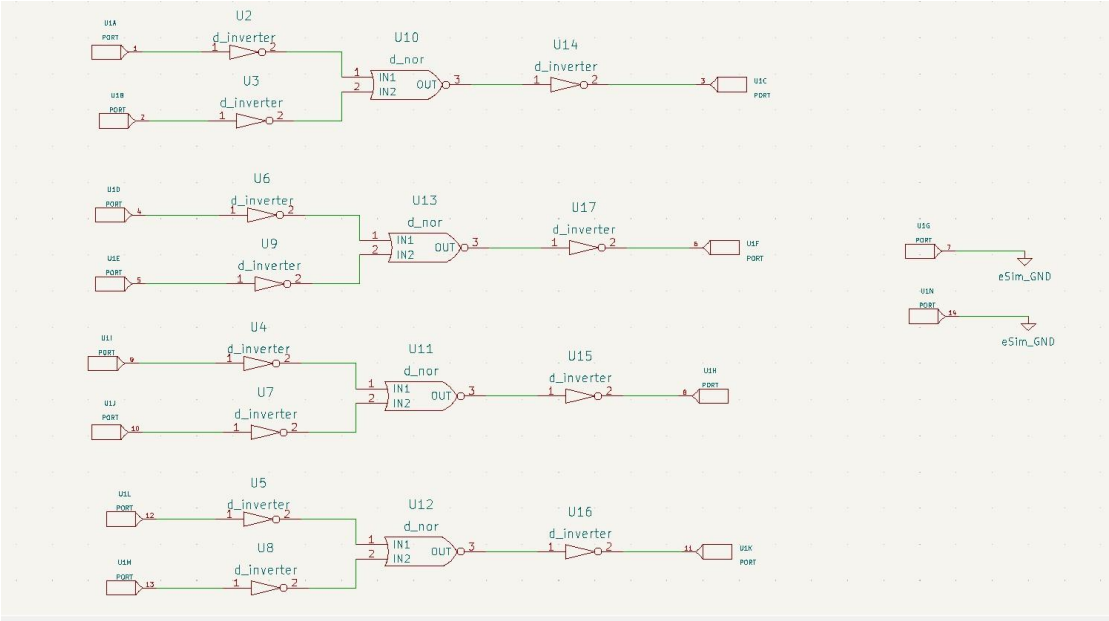

Figure 3.2: Schematic Diagram of 74HC00

3.1.4 Simulation Circuit

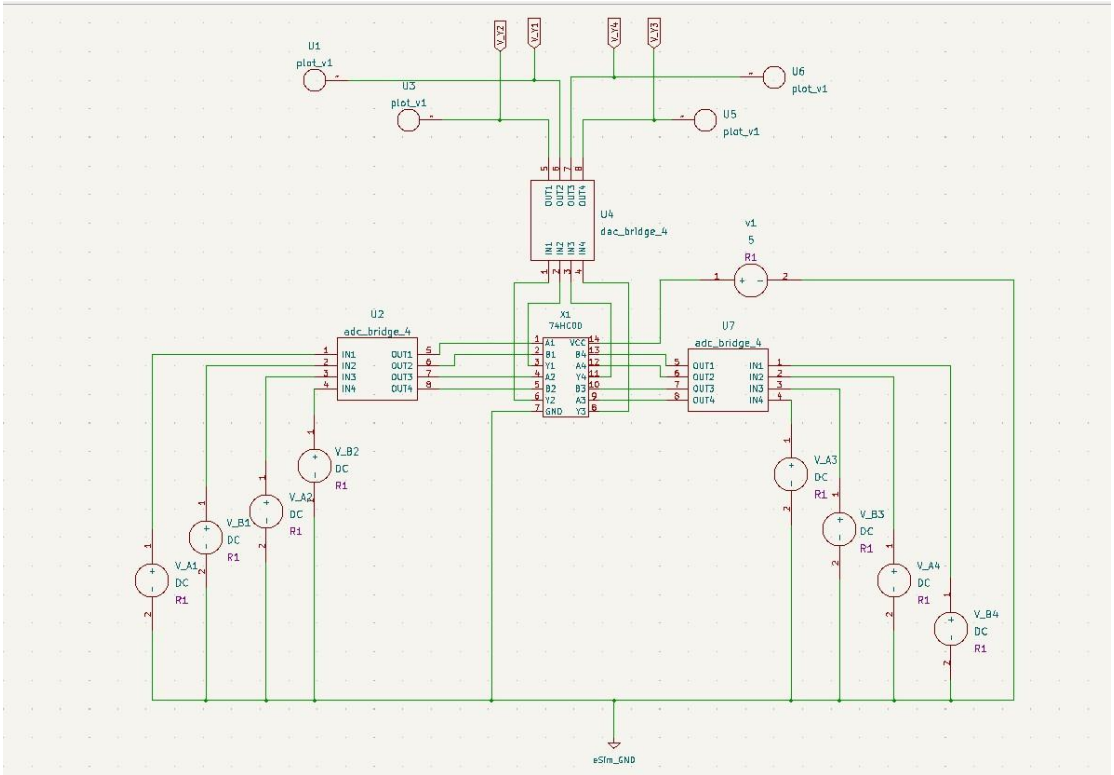

Figure 3.3: Simulation Circuit of 74HC00

3.1.5 Inputs

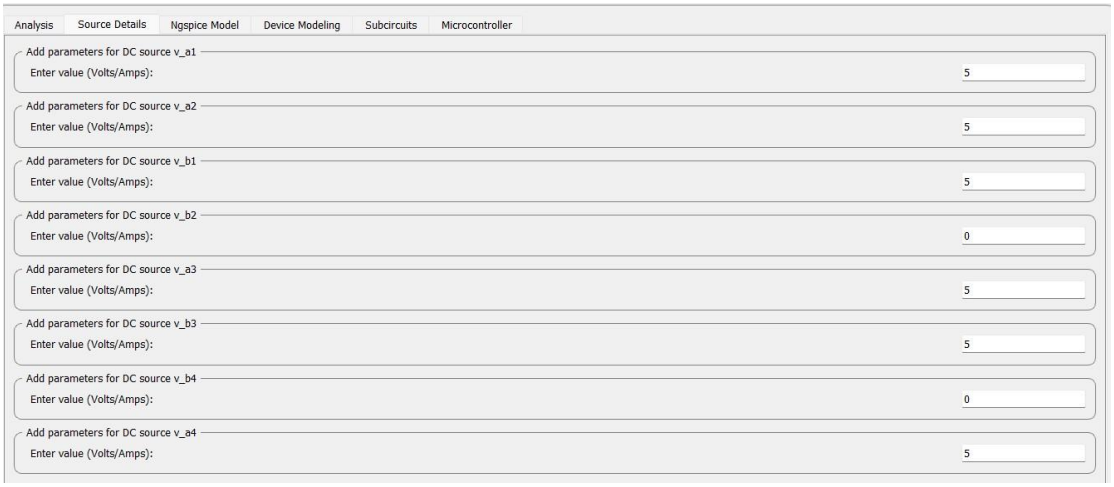

Figure 3.4: Inputs given to the Simulation Circuit

3.1.6 Output Plot

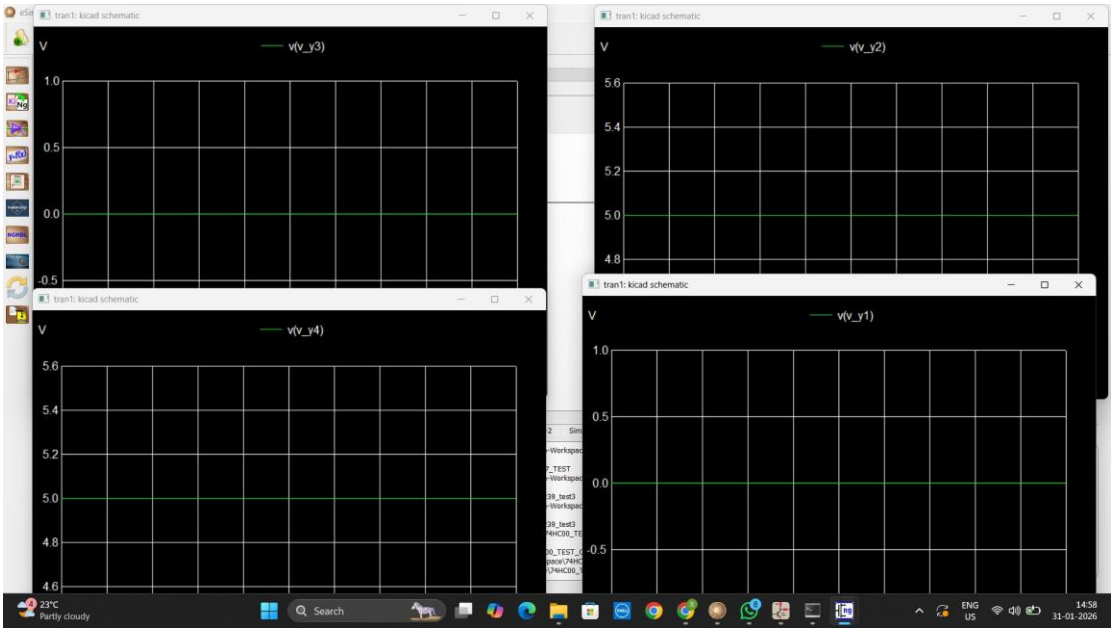

Figure 3.5: Output waveform of 74HC00

3.1.7 Functional Table

FUNCTION TABLE
See note 1.

INPUT		OUTPUT
nA	nB	nY
L	L	H
L	H	H
H	L	H
H	H	L

Note

1. H = HIGH voltage level;
   L = LOW voltage level.

Figure 3.6: truth table of 74HC00

3.2 74HC02

3.2.1 Description

The 74HC02 is a high-speed CMOS integrated circuit that contains four independent 2-input NOR gates. NOR gates play a crucial role in digital system design, as they are universal logic gates capable of implementing any logical function. The CMOS architecture provides low static power dissipation and improved noise margins. This IC is widely used in logic control circuits, signal inversion, and digital decision-making systems. The wide operating voltage range allows the device to be interfacedwith various digital components. In this project, the 74HC02 was implemented as asubcircuit in eSim, and its logical behavior was verified using appropriate testinputs and simulation results.

3.2.2 Pin Diagram

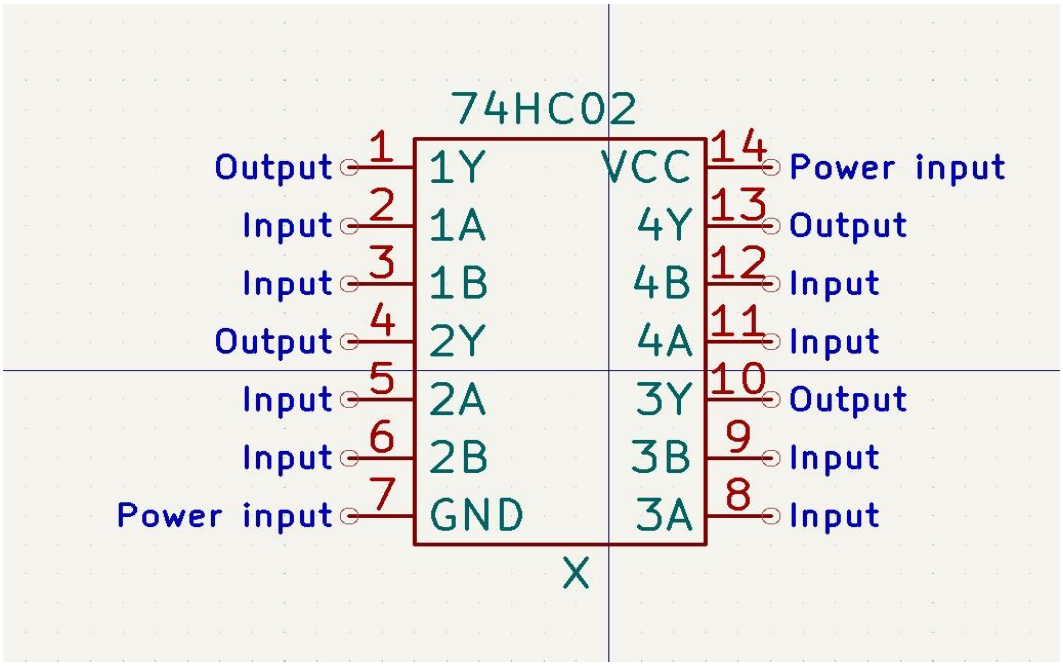

Figure 3.7: Pin Diagram of 74HC02

3.2.3 Schematic Diagram

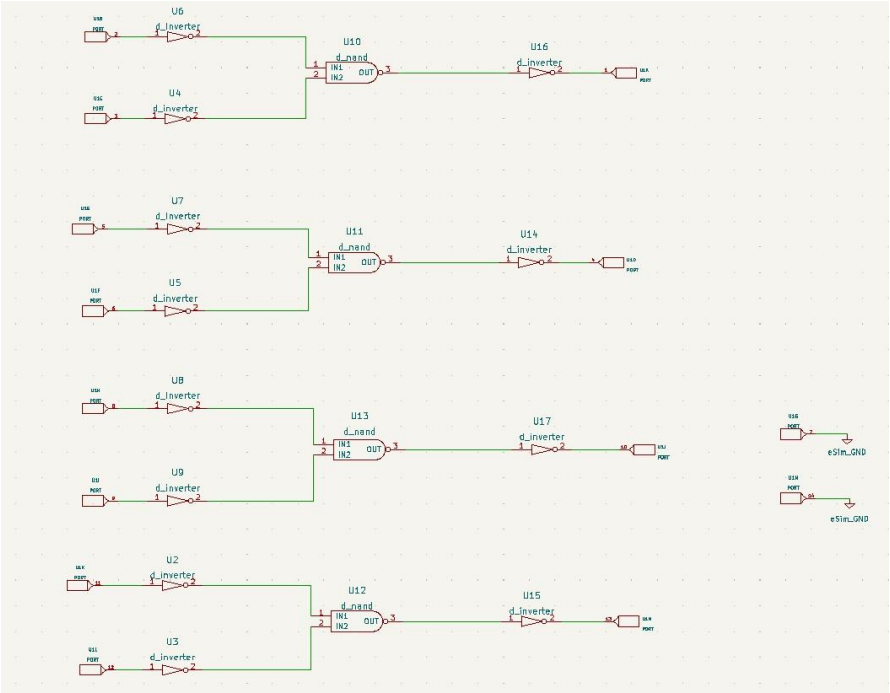

Figure 3.8: Schematic Diagram of 74HC02

3.2.4 Simulation Circuit

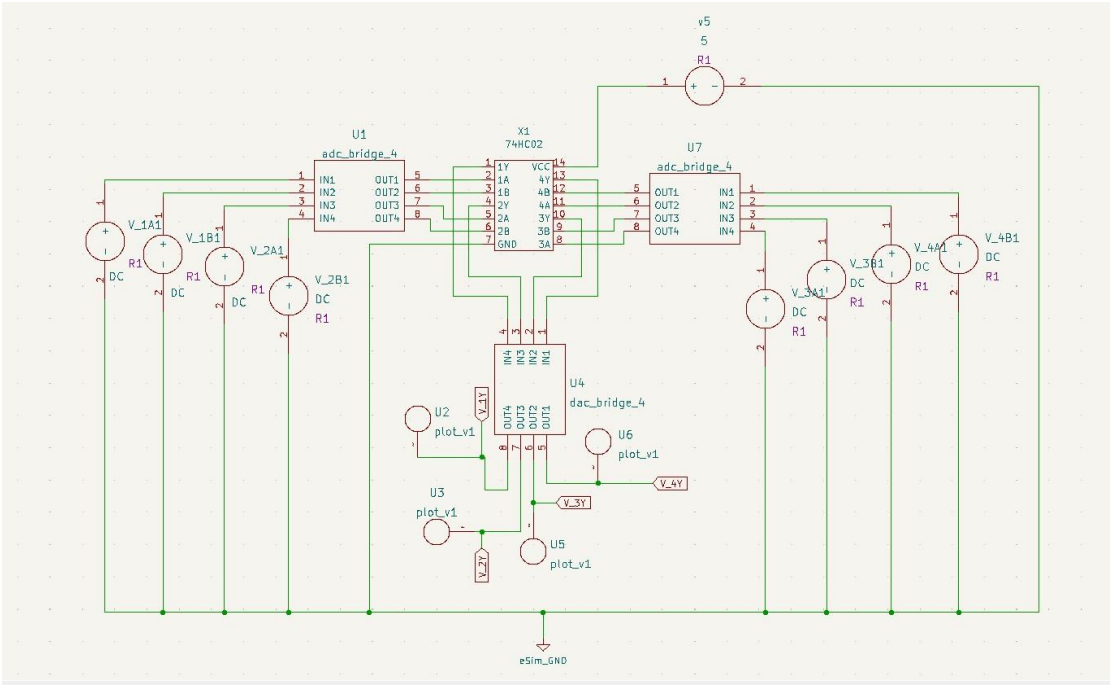

Figure 3.9: Simulation Circuit of 74HC02

3.2.5 Inputs

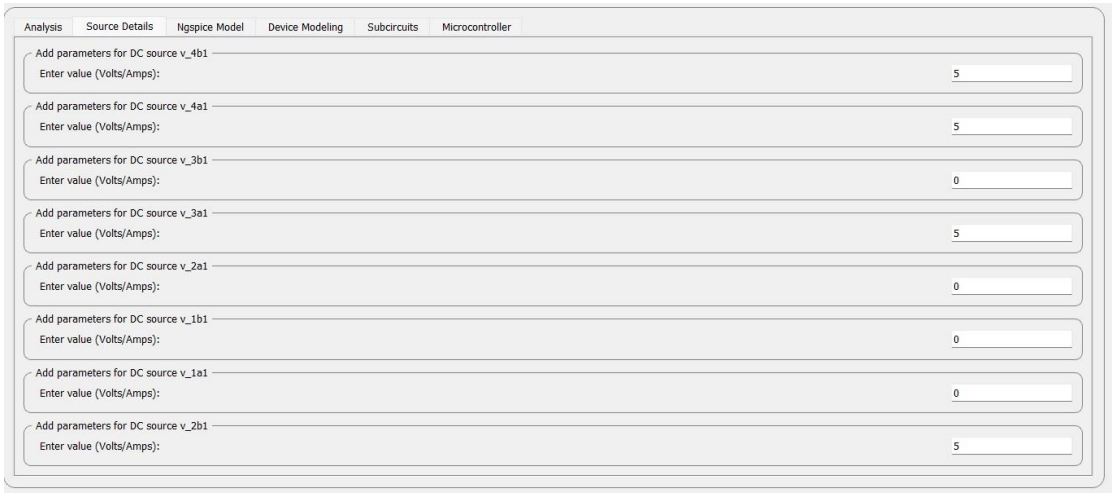

Figure 3.10: Inputs given to the Simulation circuit

3.2.6 Output Plot

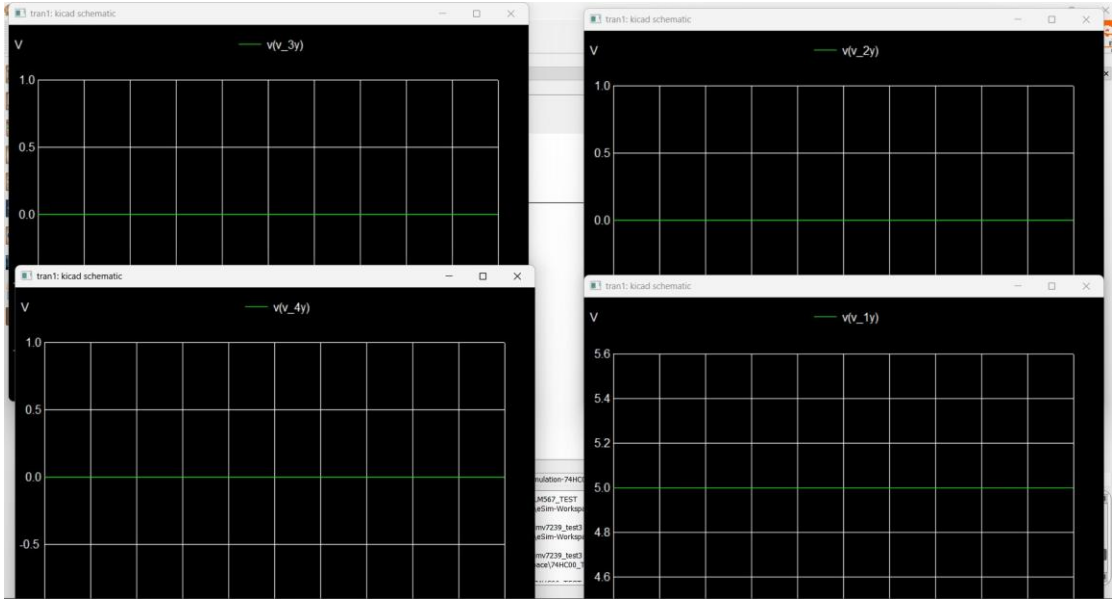

Figure 3.11: Output waveform of 74HC02

3.2.7 Functional Table

FUNCTION TABLE

INPUTS		OUTPUT
nA	nB	nY
L	L	H
L	H	L
H	L	L
H	H	L

Notes

1. H = HIGH voltage level
   L = LOW voltage level

Figure 3.12: Truth table for 74HC02

3.3 74HC86

3.3.1 Description

The 74HC86 is a CMOS-based integrated circuit containing four independent 2input Exclusive-OR (XOR) gates. XOR gates are extensively used in arithmetic circuits, parity checking, error detection, and digital comparators. The output of the XOR gate is high only when the inputs are different, making it suitable for comparison operations.

The CMOS design of the 74HC86 ensures low power consumption and high-speed operation. This IC is commonly employed in adders, subtractors, and digital communication systems. In this work, the XOR logic was modeled using the eSim Subcircuit Builder, and its functionality was verified through simulation waveforms.

3.3.2 Pin Diagram

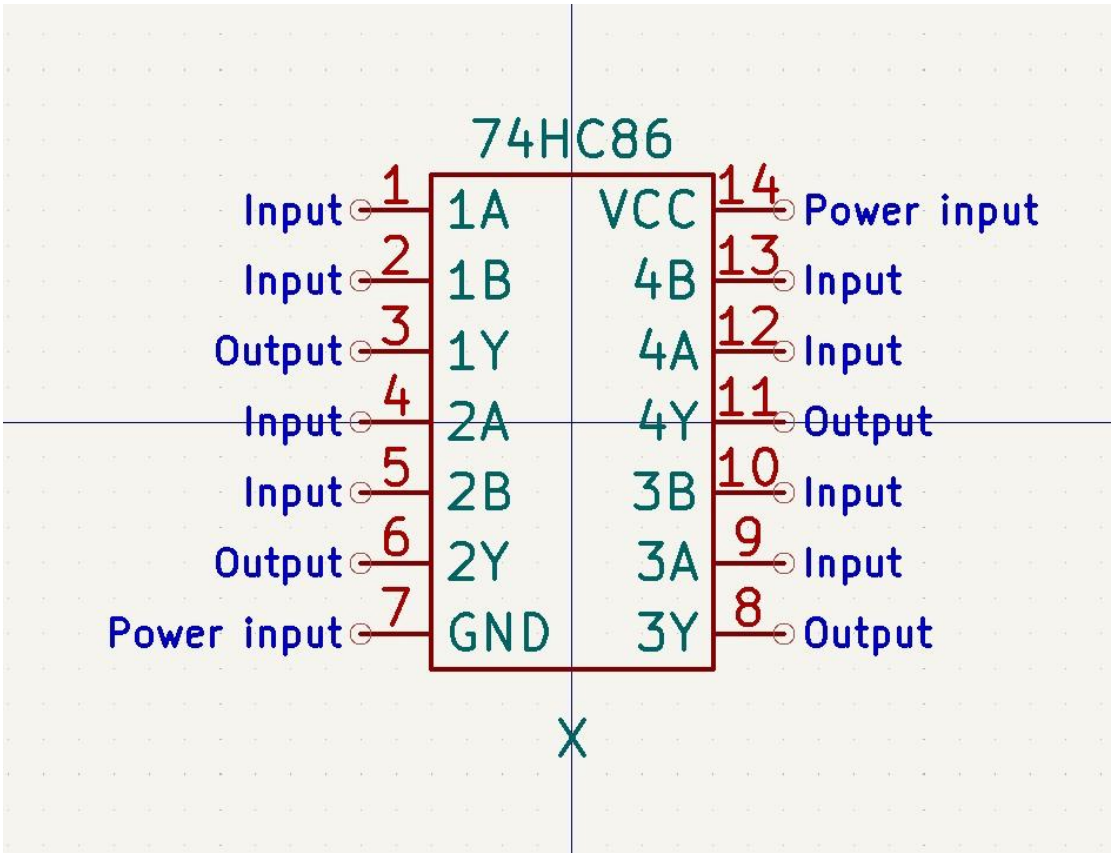

Figure 3.13: Pin Diagram of 74HC86

3.3.3 Schematic Diagram

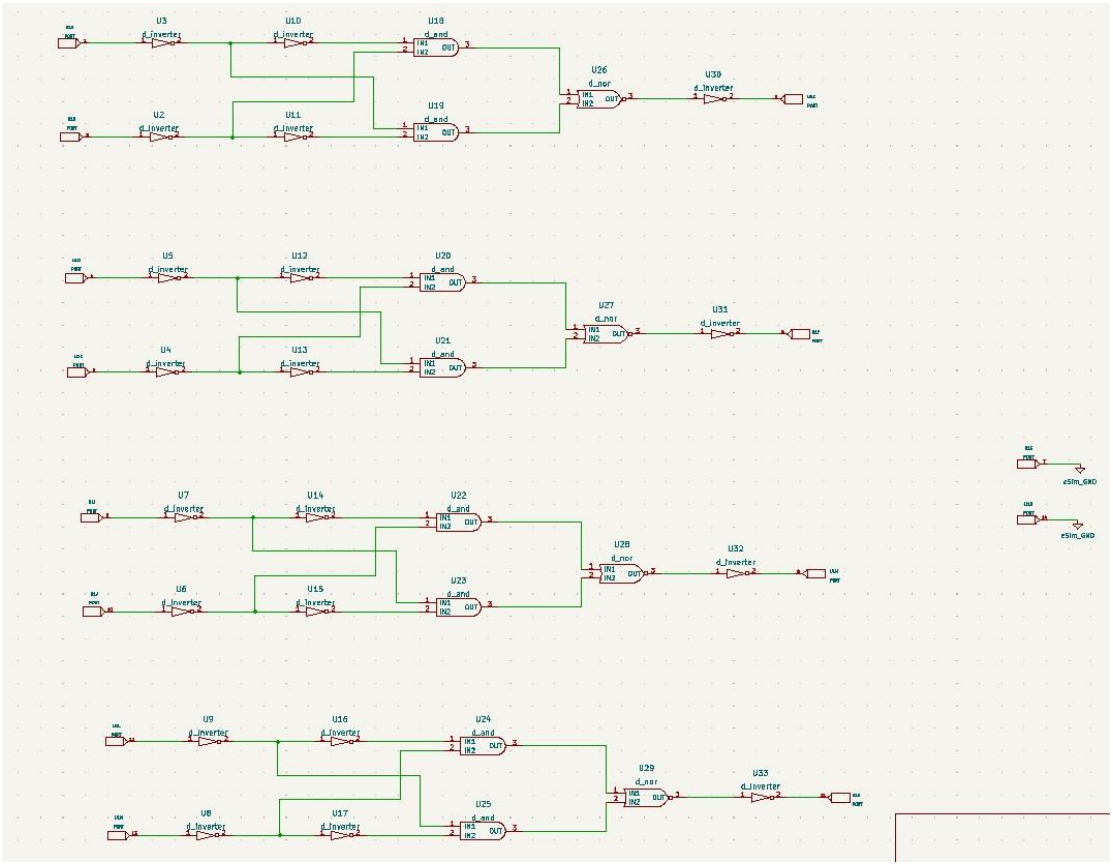

Figure 3.14: Schematic Diagram of 74HC86

3.3.4 Simulation Circuit

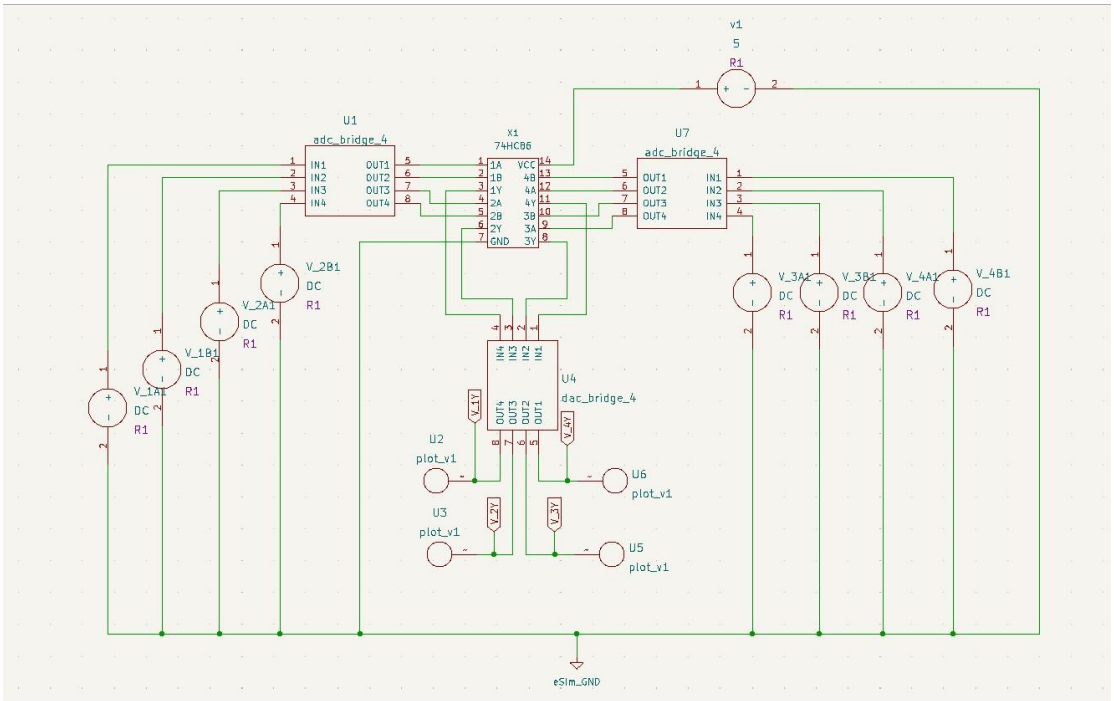

Figure 3.15: Simulation Circuit of 74HC86

3.3.5 Inputs

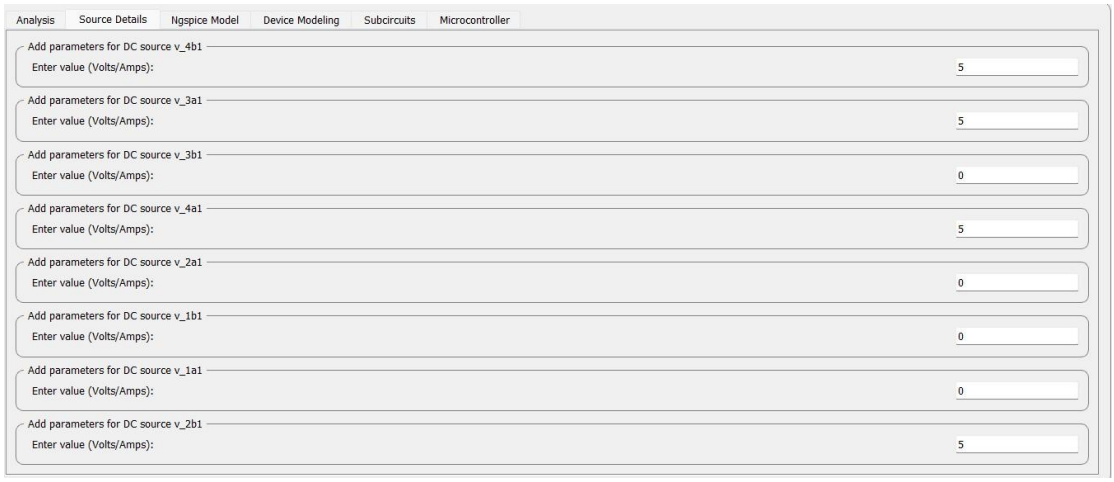

Figure 3.16: Inputs given to the Simulation Circuit of 74HC86

3.3.6 Output Plot

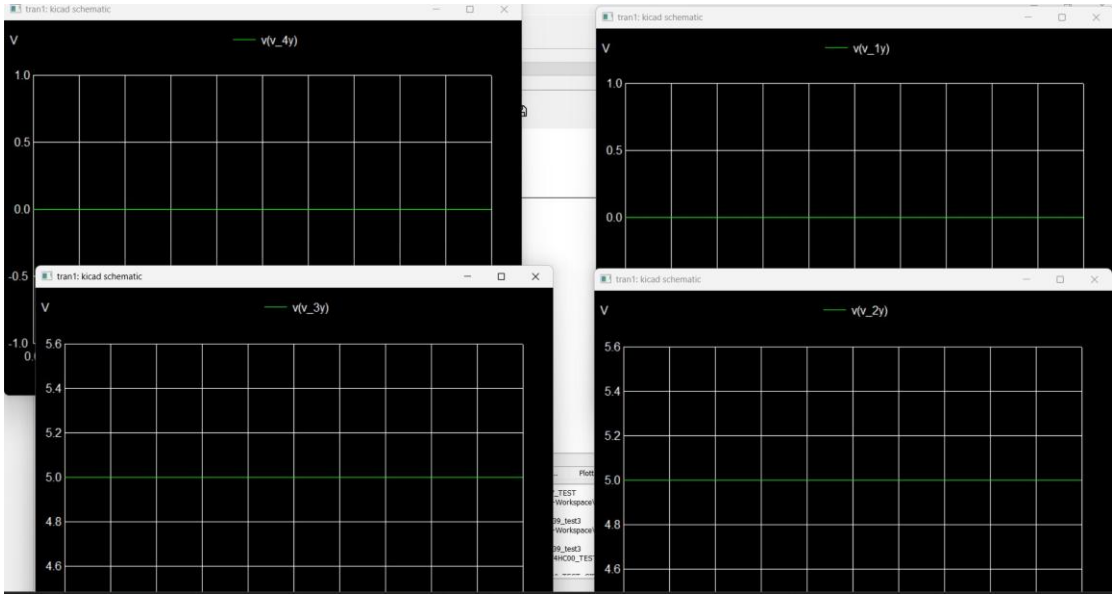

Figure 3.17: Output waveform of 74HC86

3.3.7 Functional Table

FUNCTION TABLE

INPUTS		OUTPUTS
nA	nB	nY
L	L	L
L	H	H
H	L	H
H	H	L

Notes

1. H = HIGH voltage level
   L = LOW voltage level

Figure 3.18: Truth Table for 74HC86

3.4 74HC74A

3.4.1 Description

The 74HC74A is a dual D-type positive-edge-triggered flip-flop with asynchronous preset and clear inputs. Flip-flops are fundamental sequential elements used for data storage and synchronization in digital systems. The device captures the data present at the D input on the rising edge of the clock signal.

The asynchronous preset and clear inputs allow immediate setting or resetting of the output, independent of the clock. Due to its reliable operation and low power consumption, the 74HC74A is widely used in registers, counters, and memory circuits. In this project, the internal structure of the flip-flop was modeled and tested using clock and data input signals in eSim.

3.4.2 Pin Diagram

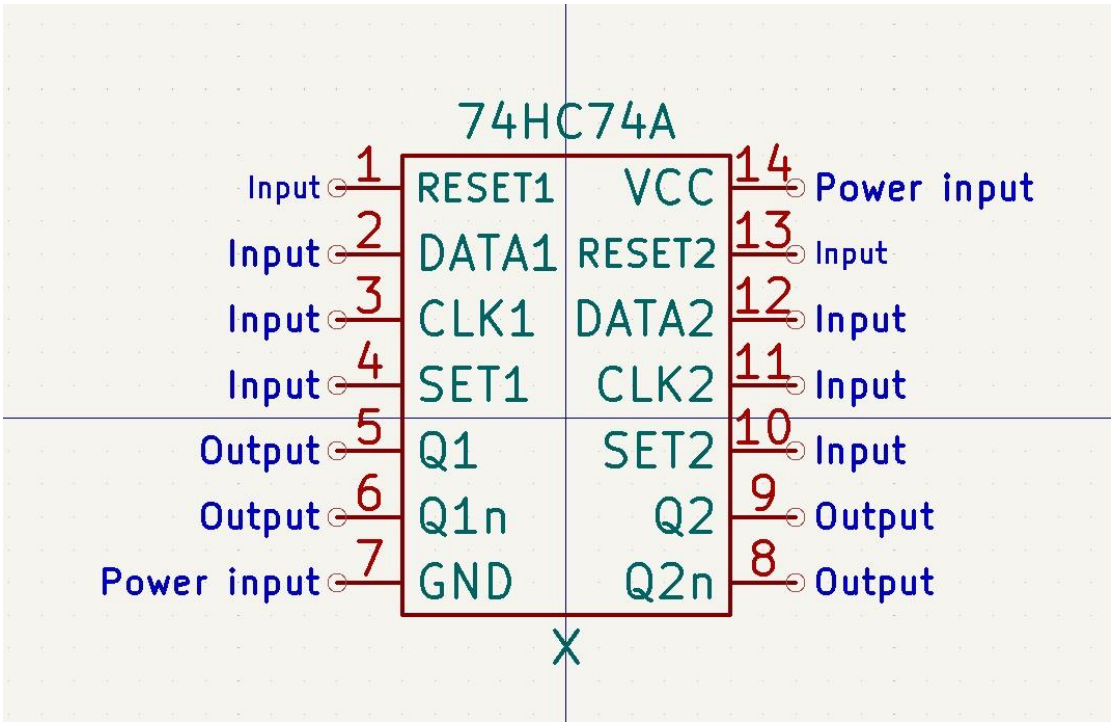

Figure 3.19: Pin Diagram of 74HC74A

3.4.3 Schematic Diagram

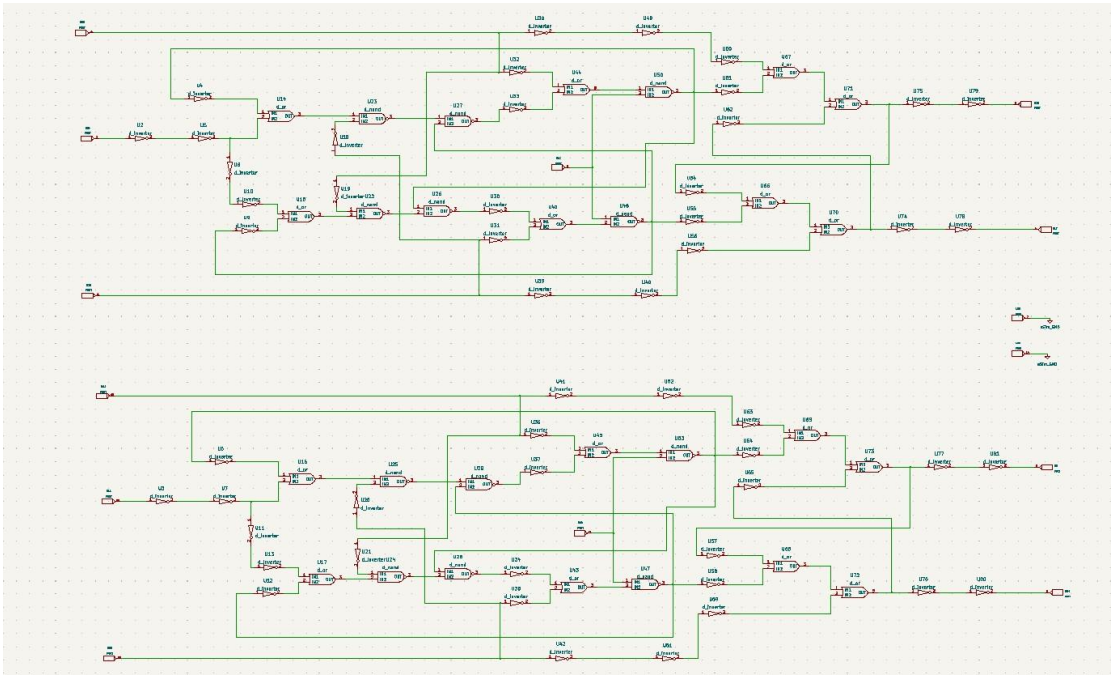

Figure 3.20: Schematic Diagram of 74HC74A

3.4.4 Simulation Circuit

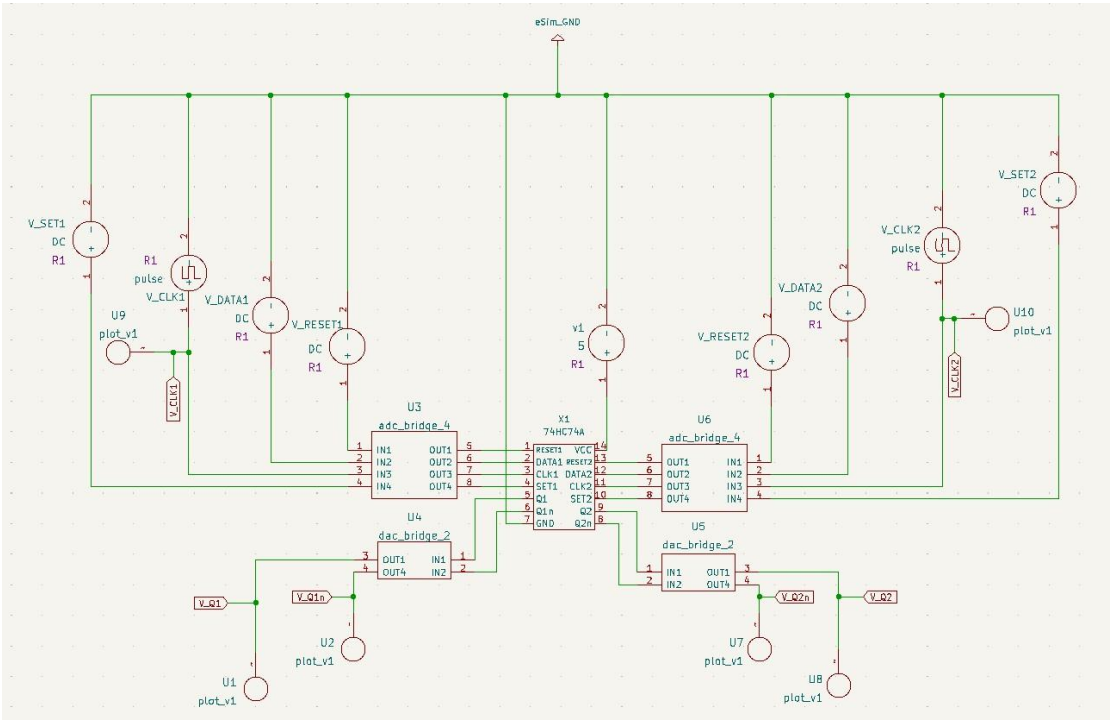

Figure 3.21: Simulation Circuit of 74HC74A

3.4.5 Inputs

Figure 3.22: Inputs given to Simulation Circuit of 74HC74A

3.4.6 Output

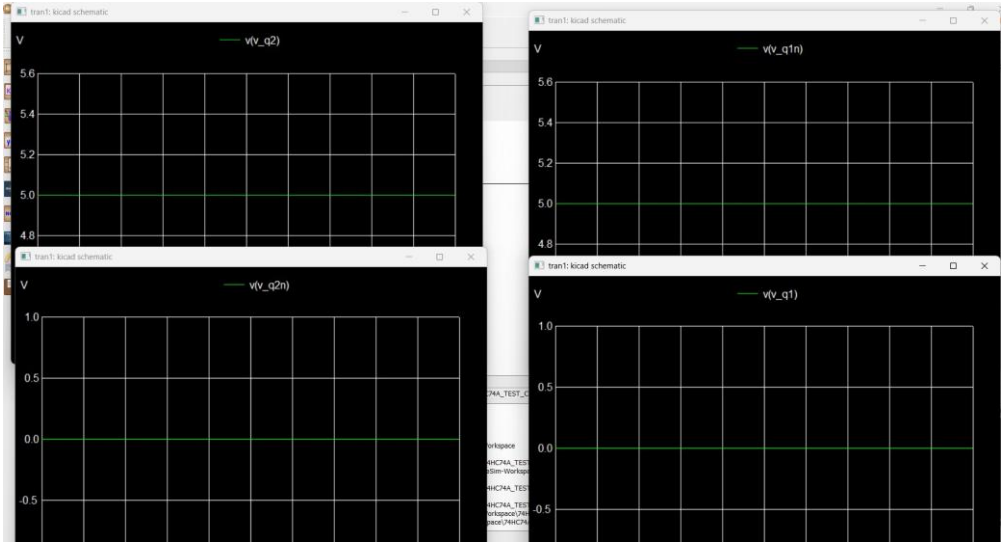

Figure 3.23: Output for Simulation Circuit of 74HC74A

3.4.7 Functional Table

FUNCTION TABLE

Inputs				Outputs	
Set	Reset	Clock	Data	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H*	H*
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	No Change	
H	H	H	X	No Change	
H	H	↓	X	No Change	

*Both outputs will remain high as long as Set and Reset are low, but the output states are unpredictable if Set and Reset go high simultaneously.

Figure 3.24: Truth Table for 74HC74A

3.5 74HC125

3.5.1 Description

The 74HC125 is a quad buffer integrated circuit with tri-state outputs. Tri-state buffers are used to isolate or connect signals to a shared data bus without causing contention. Each buffer has an independent enable input that controls the output state.

The CMOS design ensures low power consumption and fast switching speeds. The 74HC125 is commonly used in bus interfacing, signal isolation, and digital system designs. In this project, the buffering and high-impedance behavior of the IC was verified through simulation using enable control signals in eSim.

3.5.2 Pin Diagram

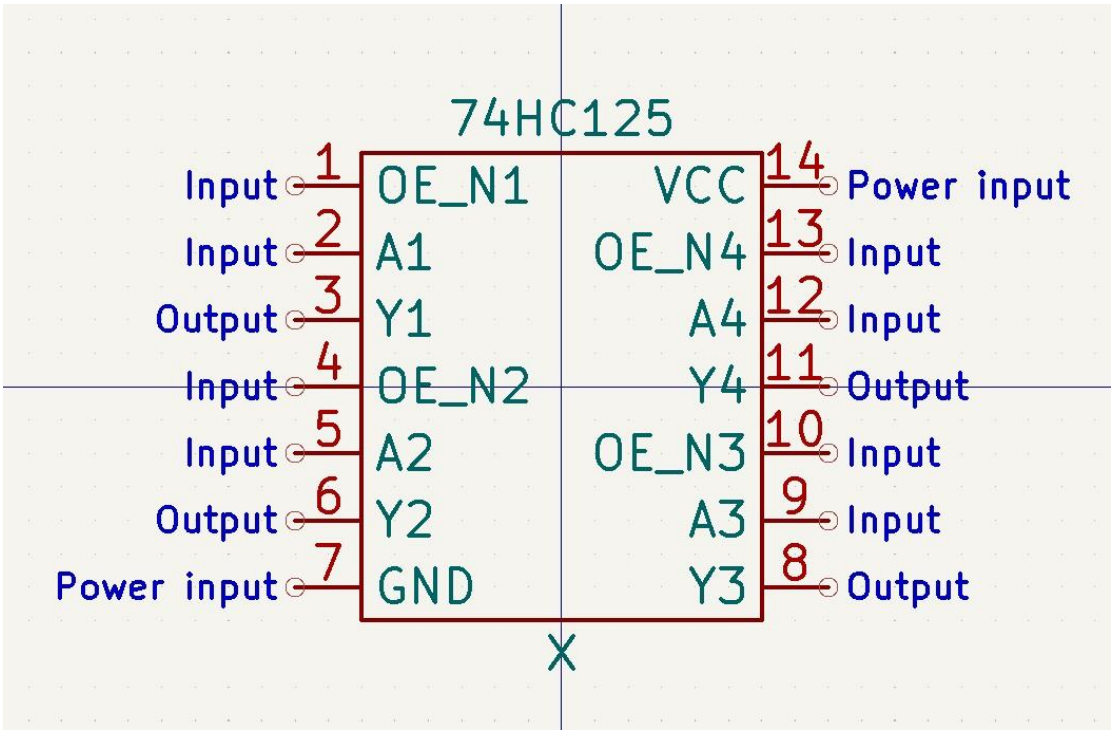

Figure 3.25: Pin Diagram of 74HC125

3.5.3 Schematic Diagram

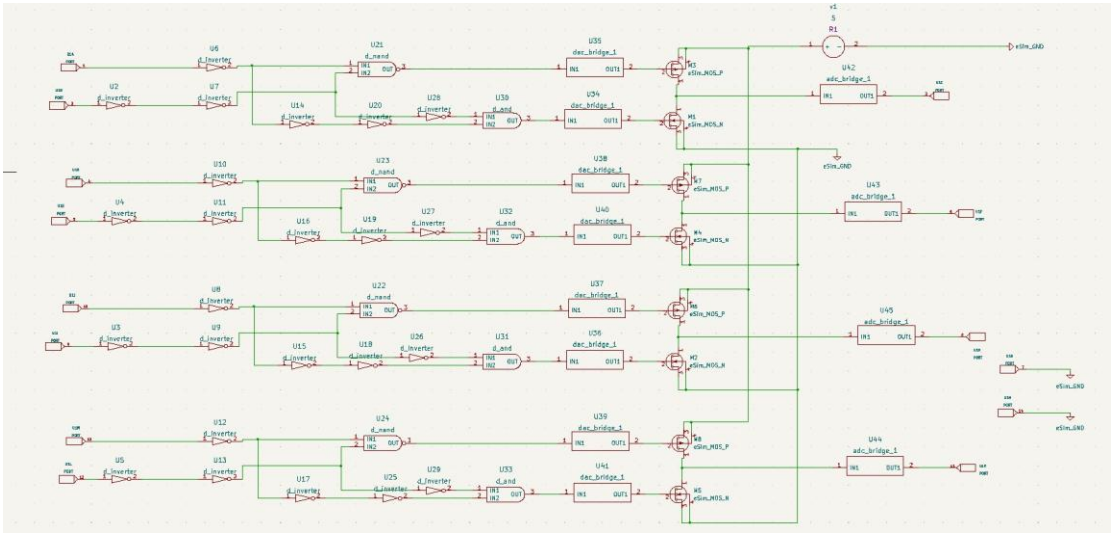

Figure 3.26: Schematic Diagram of 74HC125

3.5.4 Simulation Circuit

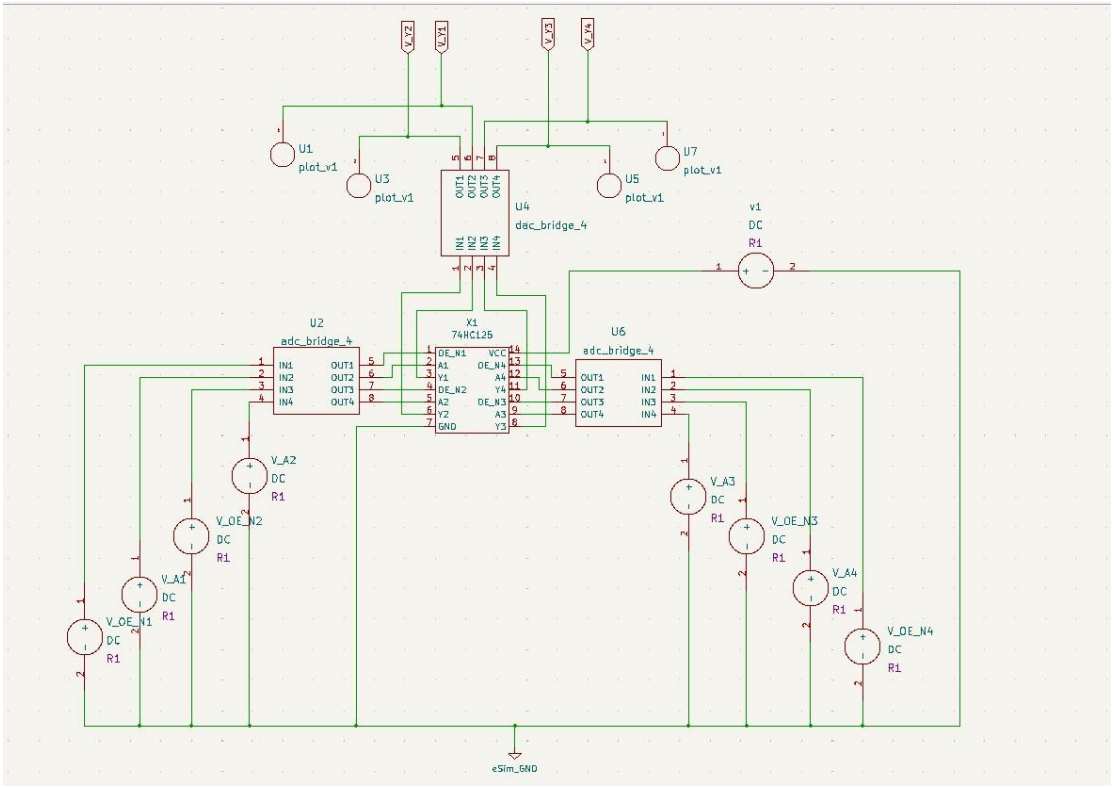

Figure 3.27: Simulation Circuit of 74HC125

3.5.5 Inputs

Figure 3.28: Inputs given to Simulation Circuit of 74HC125

3.5.6 Output Plot

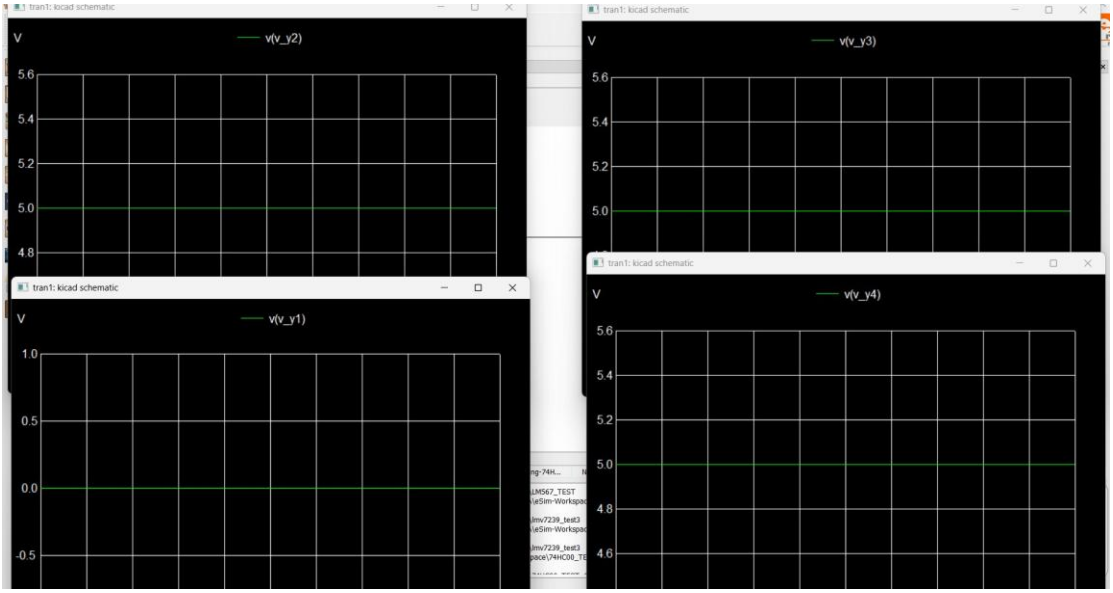

Figure 3.29: Output waveform of 74HC125

3.5.7 Functional Table

FUNCTION TABLE

HC125		
Inputs		Output
A	OE	Y
H	L	H
L	L	L
X	H	Z

Figure 3.30: Truth Table for 74HC125

3.6 74HC151

3.6.1 Description

The 74HC151 is an 8-to-1 data selector or multiplexer that selects one of eight input lines and connects it to a single output based on the select inputs. Multiplexers are essential components in digital systems for data routing and resource sharing.

This IC includes an enable input that allows the device to be activated or disabled as required. The CMOS-based design provides high-speed operation with low power dissipation. The 74HC151 is widely used in communication systems, data acquisition, and control logic. In this work, the multiplexer operation was modeled and verified by applying different select line combinations in eSim.

3.6.2 Pin Diagram

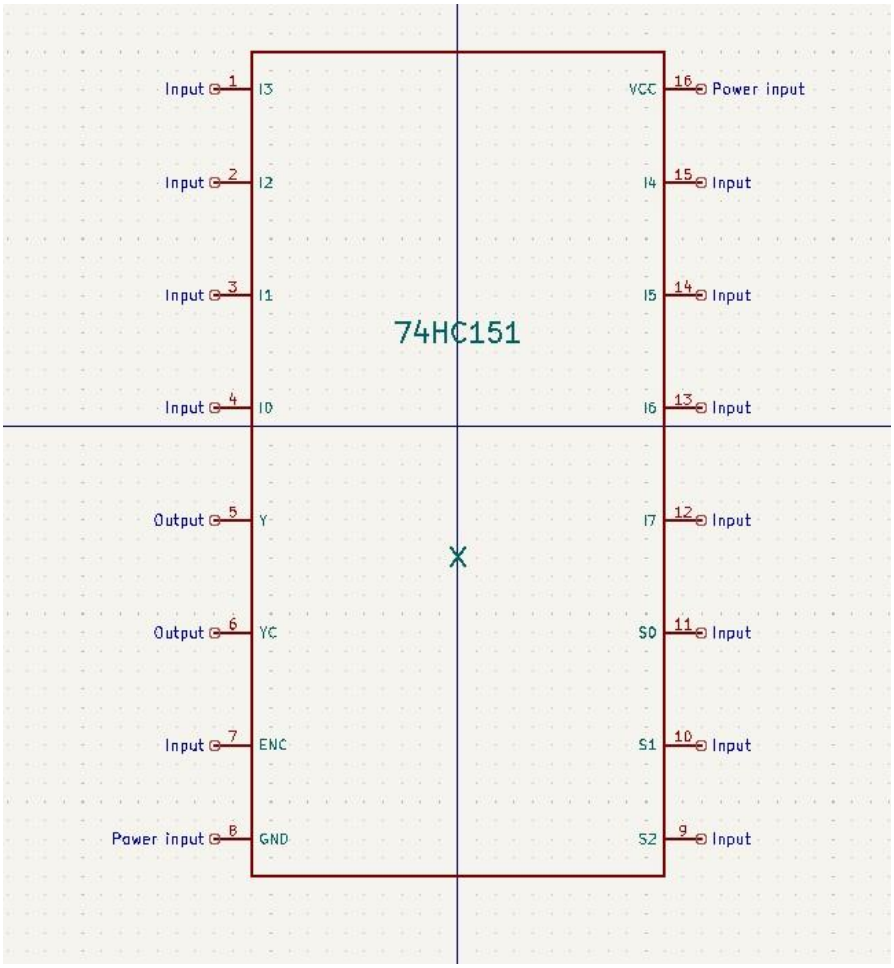

Figure 3.31: Pin Diagram of 74HC151

3.6.3 Schematic Diagram

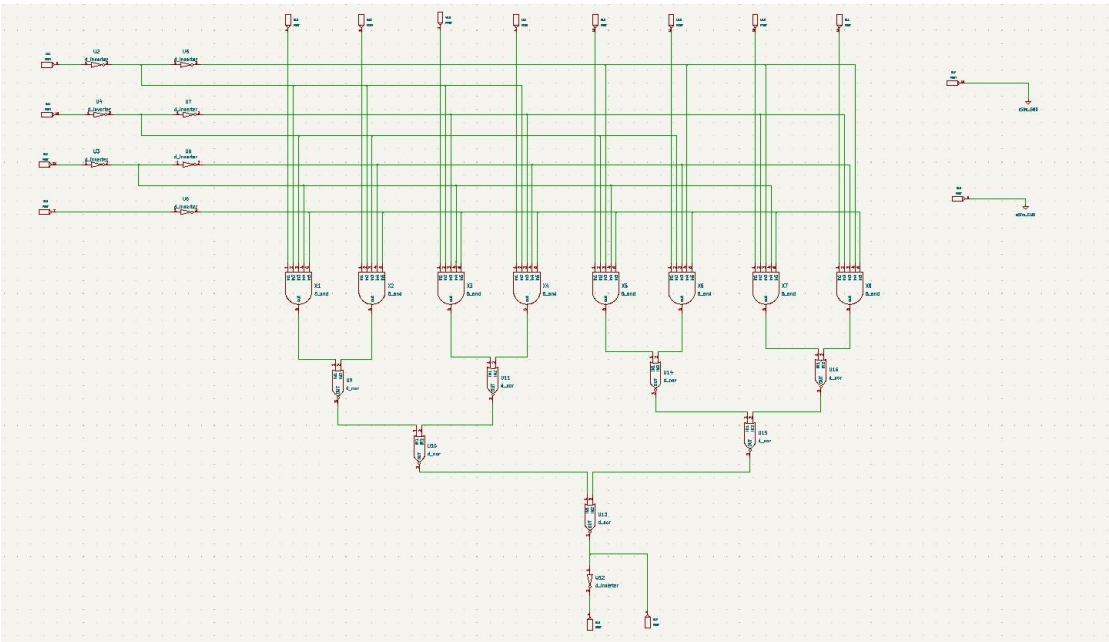

Figure 3.32: Schematic Diagram of 74HC151

3.6.4 Simulation Circuit

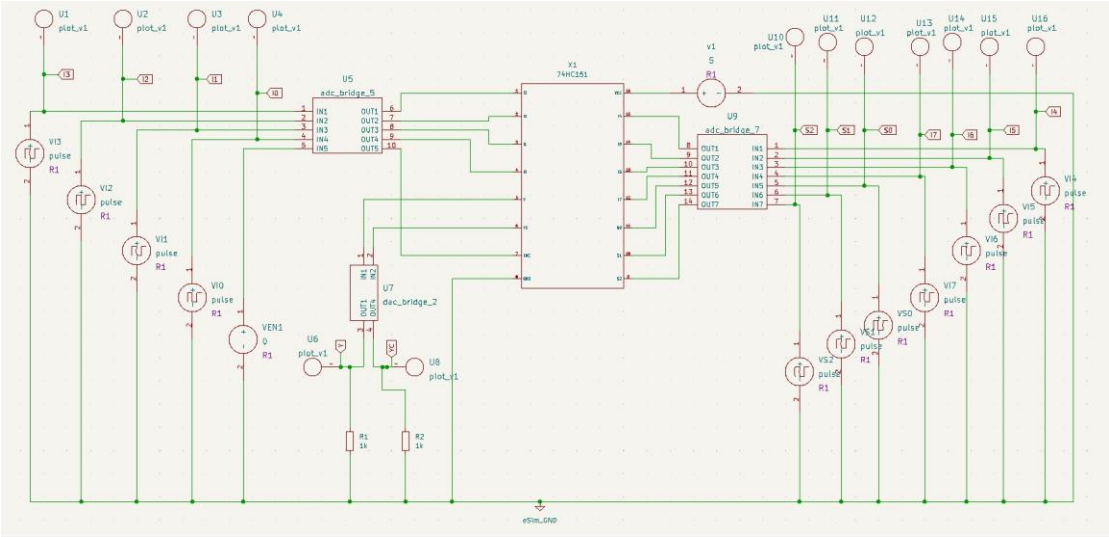

Figure 3.33: Simulation Circuit of 74HC151

3.6.5 Output Plot

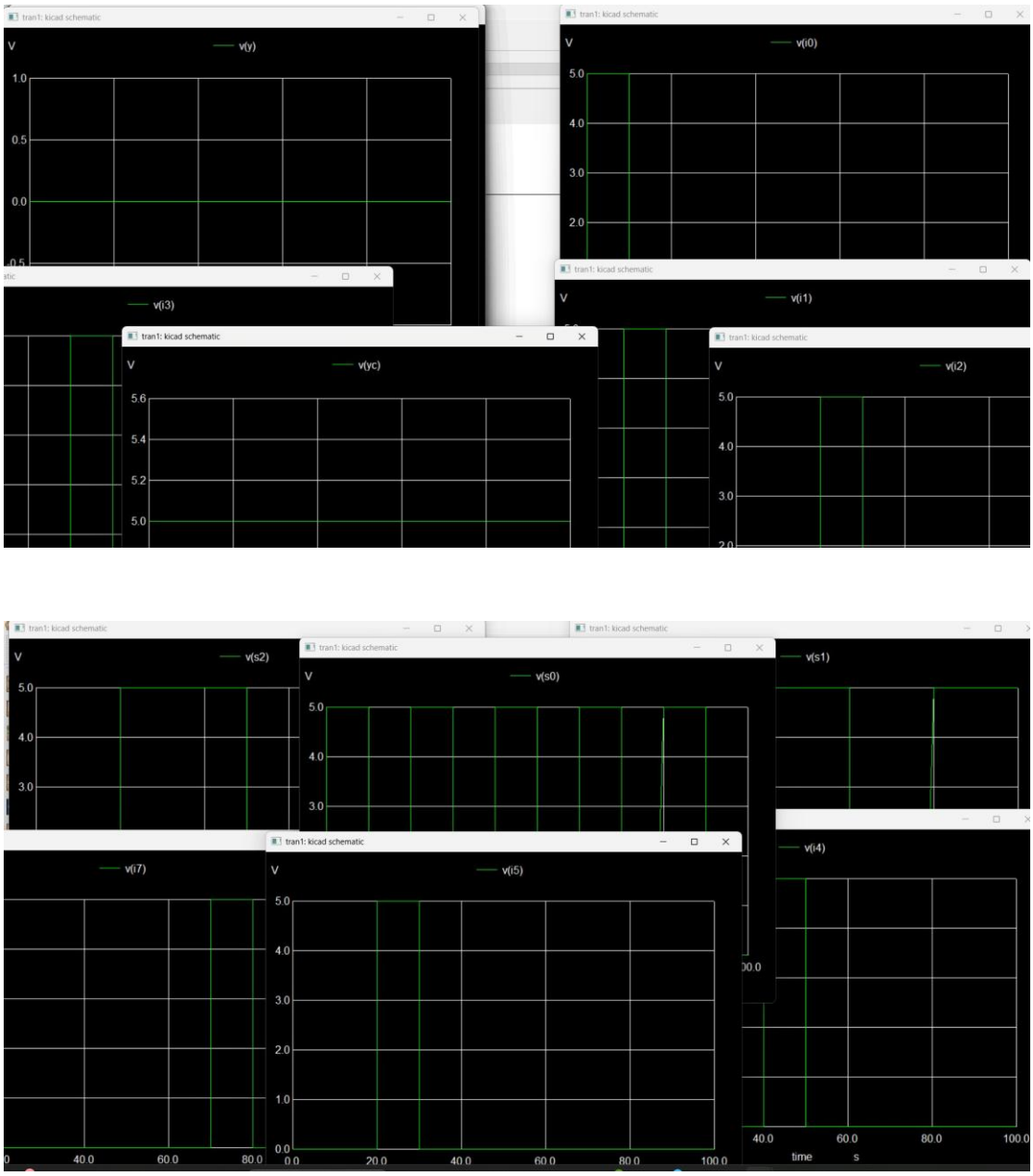

Figure 3.34: Output waveforms of 74HC151

3.7 74HC154

3.7.1 Description

The 74HC154 is a 4-to-16 line decoder/demultiplexer with active-low outputs. It decodes a 4-bit binary input into one of sixteen mutually exclusive outputs. Decoders are primarily used in memory addressing, instruction decoding, and control signal generation.

The IC includes enable inputs that control the activation of the device. The CMOS implementation ensures low power consumption and reliable operation. In this project, the 74HC154 was modeled as a subcircuit in eSim, and its decoding functionality was verified using different binary input combinations.

3.7.2 Pin Diagram

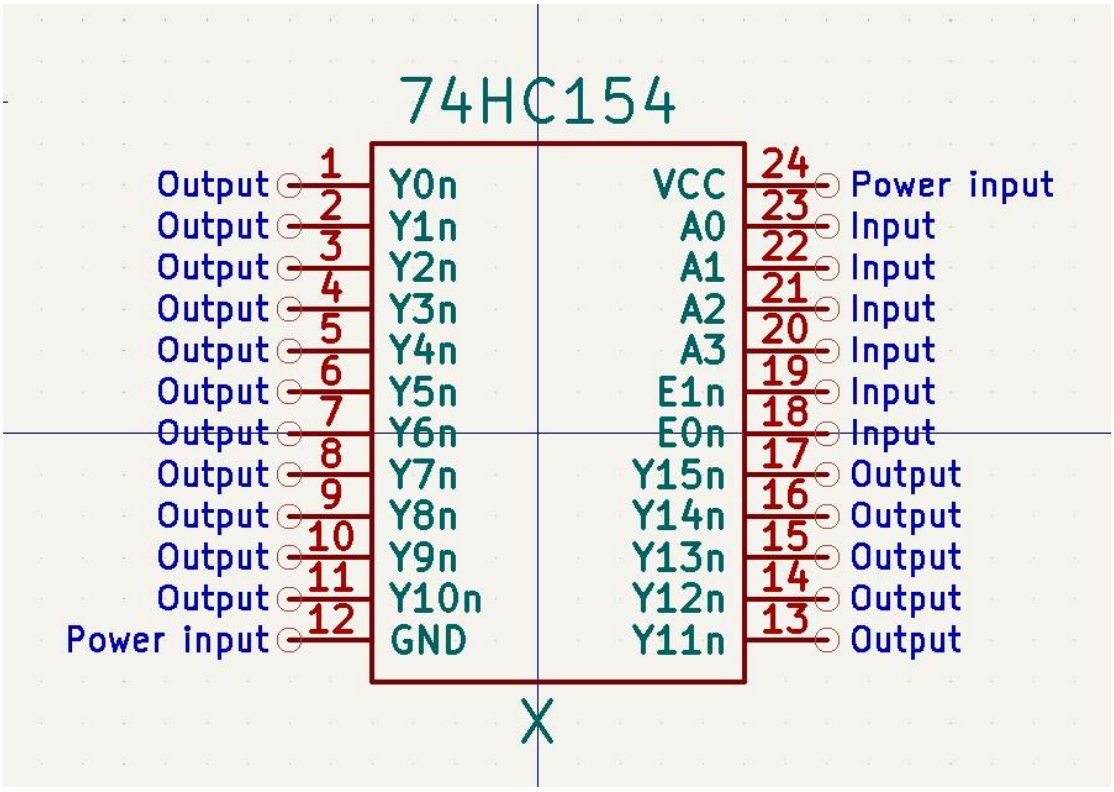

Figure 3.35: Pin Diagram of 74HC154

3.7.3 Schematic Diagram

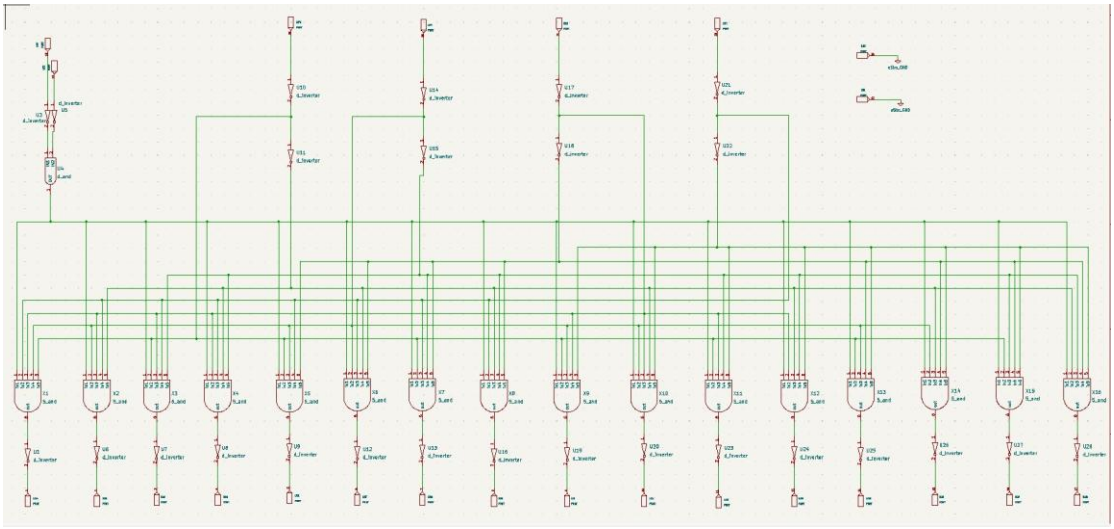

Figure 3.36: Schematic Diagram of 74HC154

3.7.4 Simulation Circuit

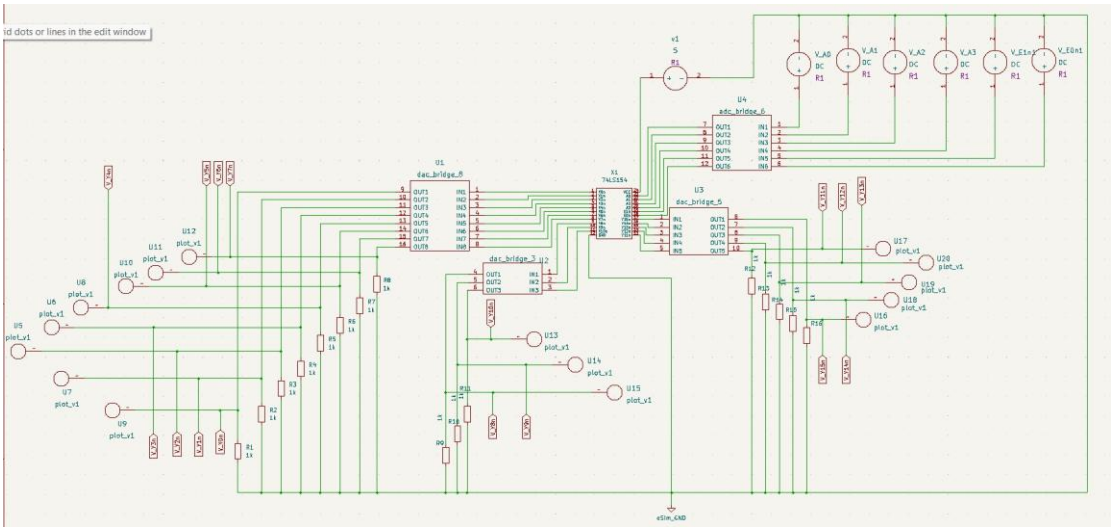

Figure 3.37: Simulation Circuit of 74HC154

3.7.5 Inputs

Figure 3.38: Inputs given to Simulation Circuit of 74HC154

3.7.6 Output Plot

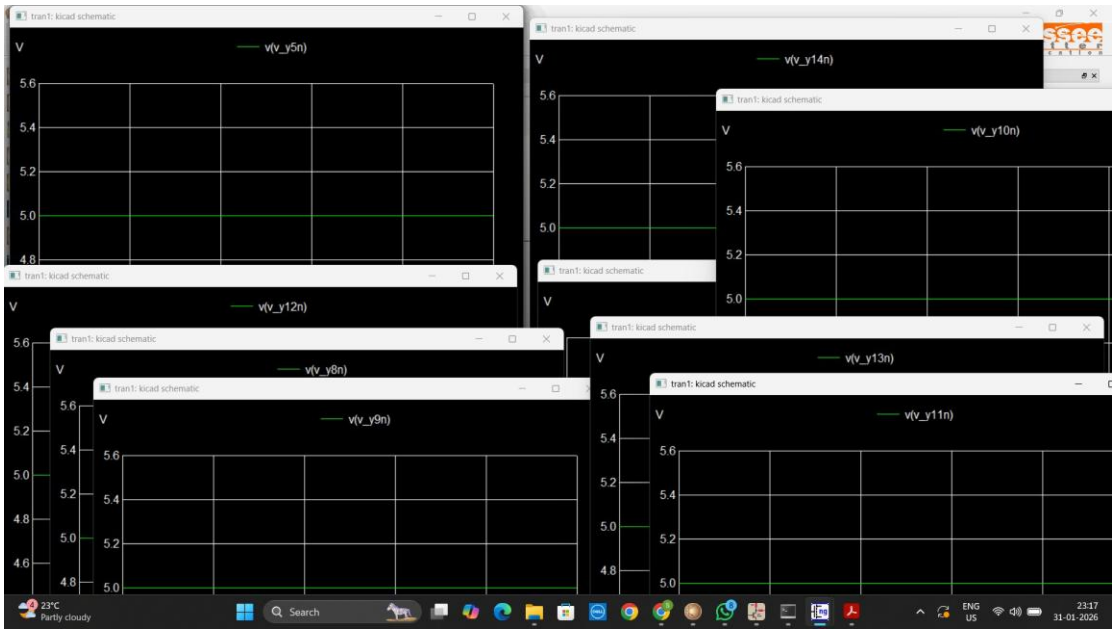

Figure 3.39: Output waveforms of 74HC154

3.7.7 Functional Table

FUNCTION TABLE

		INPUTS				OUTPUTS														
$\overline{E}_0$	$\overline{E}_1$	A_0	A_1	A_2	A_3	$\overline{Y}_0$	$\overline{Y}_1$	$\overline{Y}_2$	$\overline{Y}_3$	$\overline{Y}_4$	$\overline{Y}_5$	$\overline{Y}_6$	$\overline{Y}_7$	$\overline{Y}_8$	$\overline{Y}_9$	$\overline{Y}_{10}$	$\overline{Y}_{11}$	$\overline{Y}_{12}$	$\overline{Y}_{13}$	$\overline{Y}_{14}$	$\overline{Y}_{15}$
H	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	L	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	H	L	L	L	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	H	H	L	L	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	L	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H
L	L	H	L	H	L	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H
L	L	L	H	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H
L	L	H	H	H	L	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H
L	L	H	L	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H
L	L	L	H	L	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H
L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H
L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H
L	L	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H
L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L

Note

1. H = HIGH voltage level
   L = LOW voltage level
   X = don't care

Figure 3.40: Truth Table for 74HC154

3.8 74HC175

3.8.1 Description

The 74HC175 is a quad D-type flip-flop with a common clock input and an asynchronous reset. It is designed for storing and transferring 4-bit data in synchronous digital systems. On the rising edge of the clock, the data present at the D inputs is transferred to the corresponding outputs.

The asynchronous reset allows all outputs to be cleared simultaneously, making the device suitable for initialization operations. The 74HC175 is widely used in registers, counters, and data buffering applications. In this work, the flip-flop operation was implemented and verified using clock-controlled simulations in eSim.

3.8.2 Pin Diagram

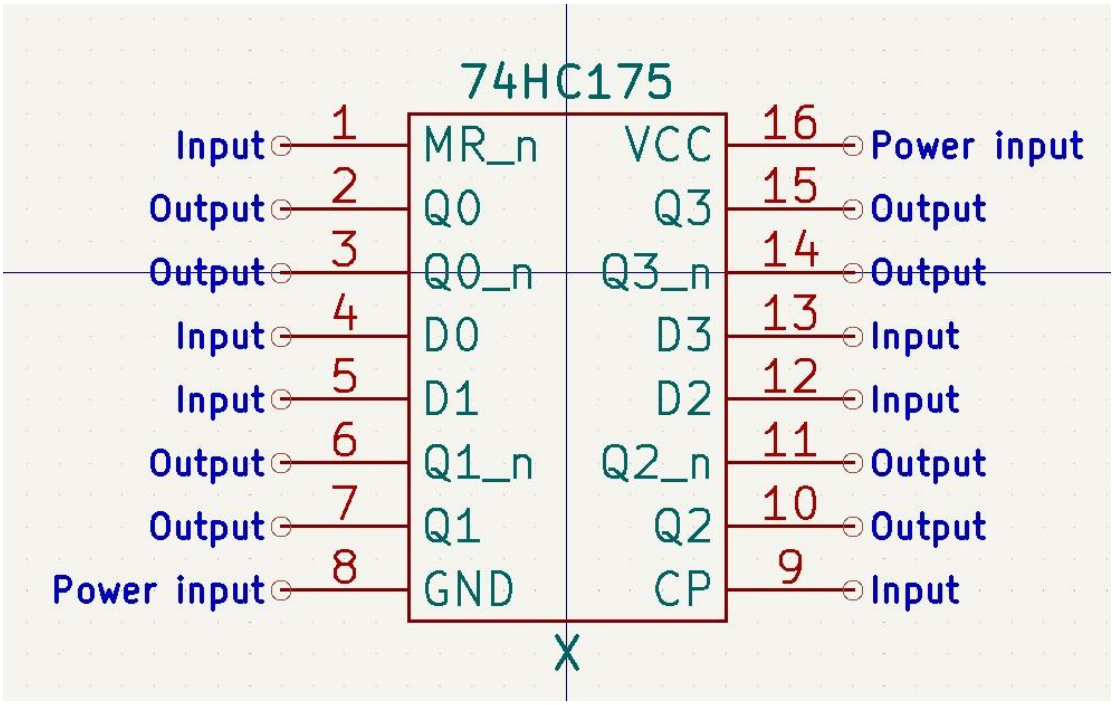

Figure 3.41: Pin Diagram of 74HC175

3.8.3 Schematic Diagram

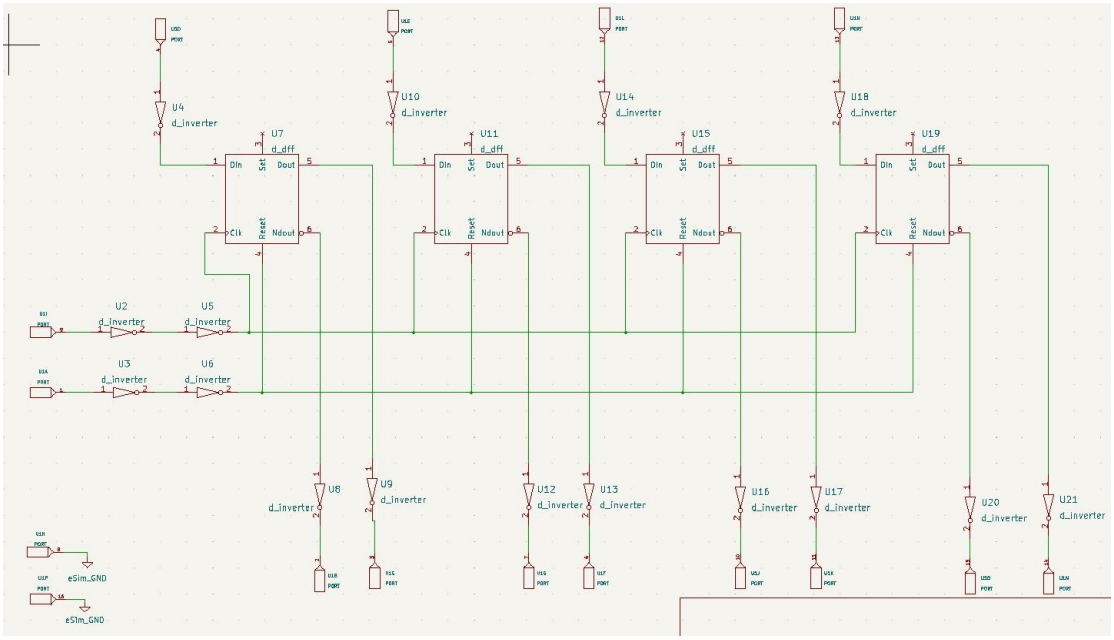

Figure 3.42: Schematic Diagram of 74HC175

3.8.4 Simulation Circuit

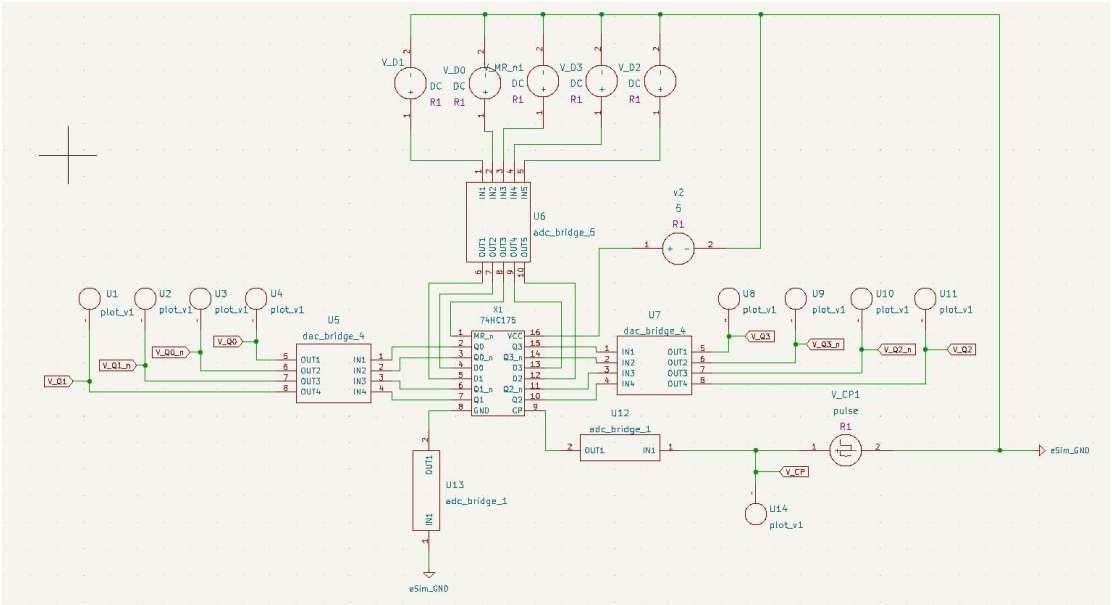

Figure 3.43: Simulation Circuit of 74HC175

3.8.5 Inputs

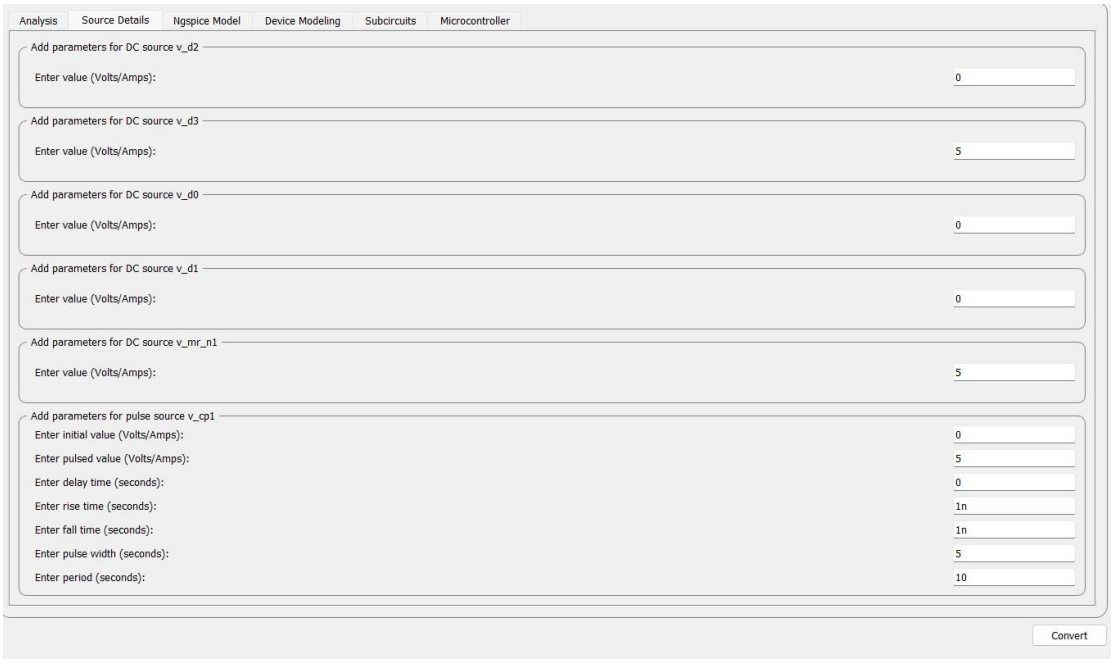

Figure 3.44: Inputs given to Simulation Circuit of 74HC175

3.8.6 Output Plot

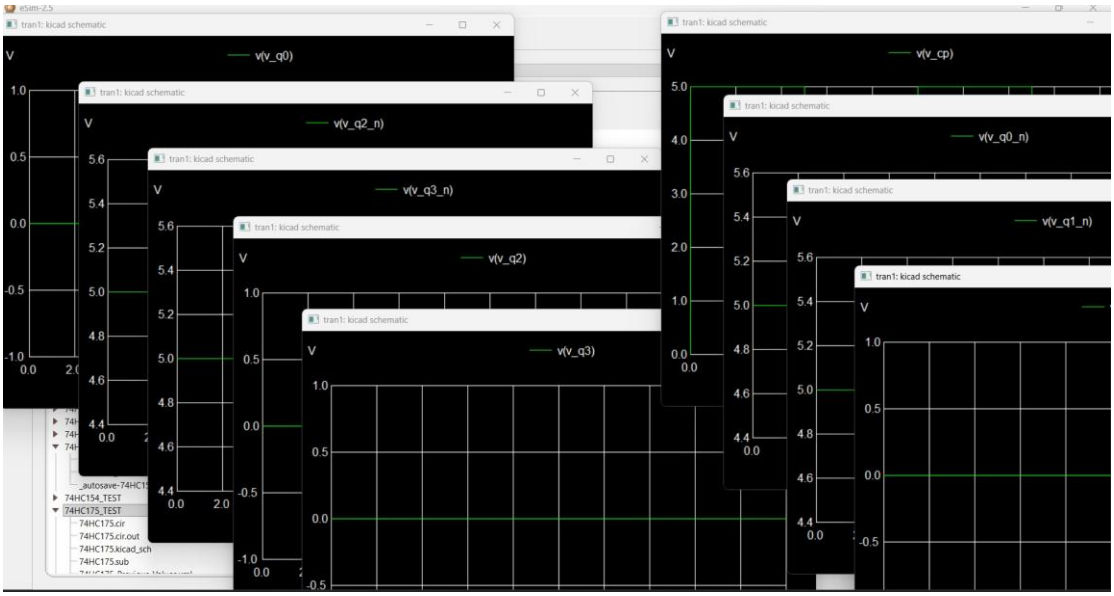

Figure 3.45: Output waveform of 74HC175

3.8.7 Functional Table

FUNCTION TABLE

OPERATING MODES	INPUTS			OUTPUTS	
	$\overline{MR}$	CP	D_n	Q_n	$\overline{Q}_n$
reset (clear)	L	X	X	L	H
load "1"	H	↑	h	H	L
load "0"	H	↑	l	L	H

Note

1. H = HIGH voltage level
   h = HIGH voltage level one set-up time prior to the LOW-to-HIGH CP transition
   L = LOW voltage level
   l = LOW voltage level one set-up time prior to the LOW-to-HIGH CP transition
   ↑ = LOW-to-HIGH CP transition
   X = don't care

Figure 3.46: Truth Table for 74HC175

3.9 74HC245

3.9.1 Description

The 74HC245 is an octal bidirectional bus transceiver designed for data transfer between two buses. It allows data to flow in either direction depending on the direction control input. The device also features tri-state outputs to prevent bus conflicts.

This IC is widely used in microprocessor-based systems, data buses, and memory interfacing applications. The CMOS technology provides high-speed operation with low power consumption. In this work, bidirectional data transfer was modeled and verified using controlled simulation inputs in eSim.

3.9.2 Pin Diagram

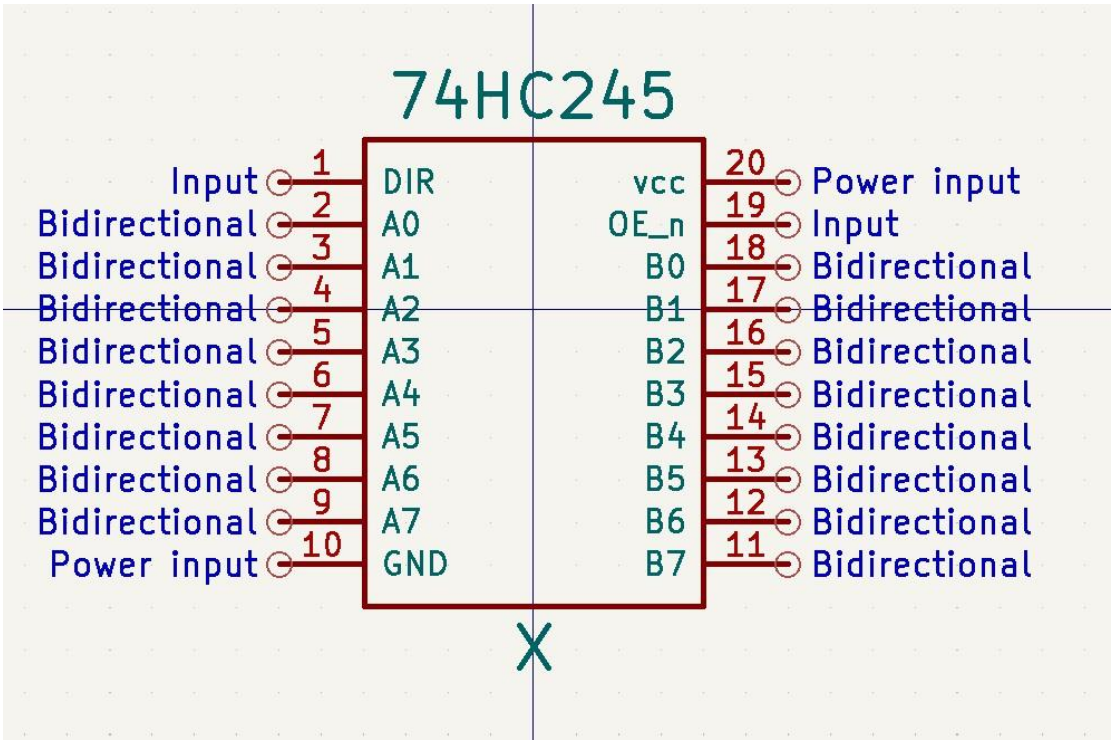

Figure 3.47: Pin Diagram of 74HC245

3.9.3 Schematic Diagram

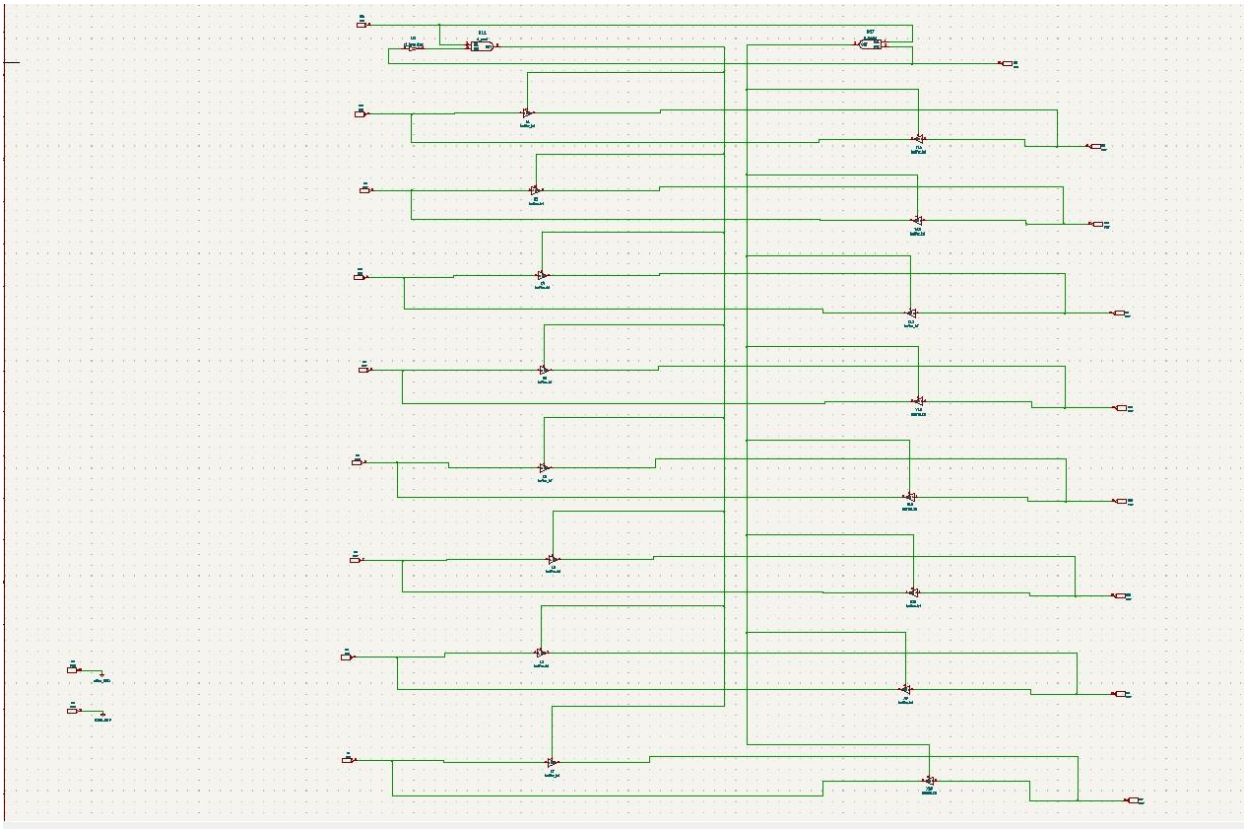

Figure 3.48: Schematic Diagram of 74HC245

3.9.4 Simulation Circuit

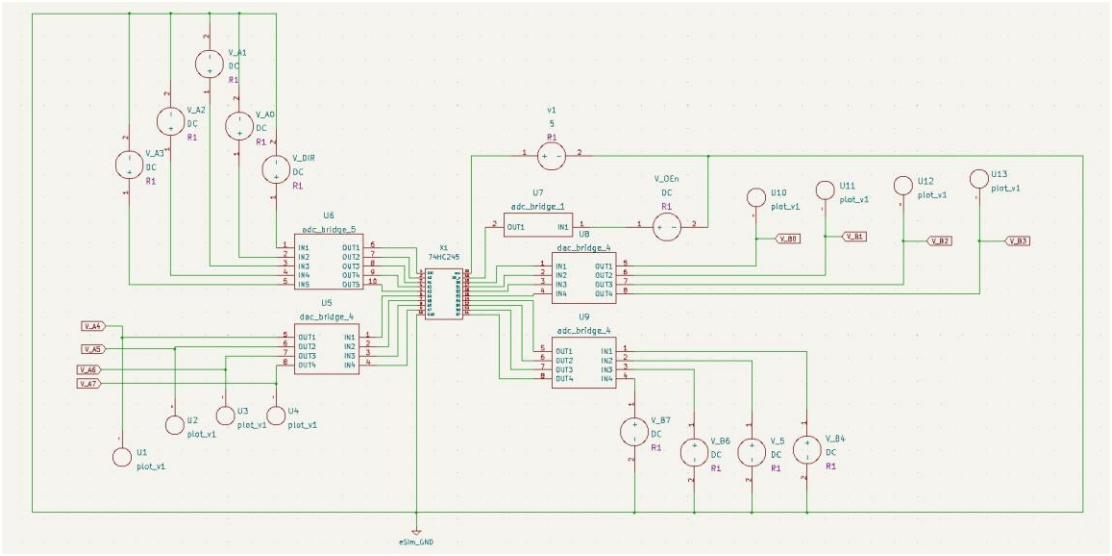

Figure 3.49: Simulation Circuit of 74HC245

3.9.5 Inputs

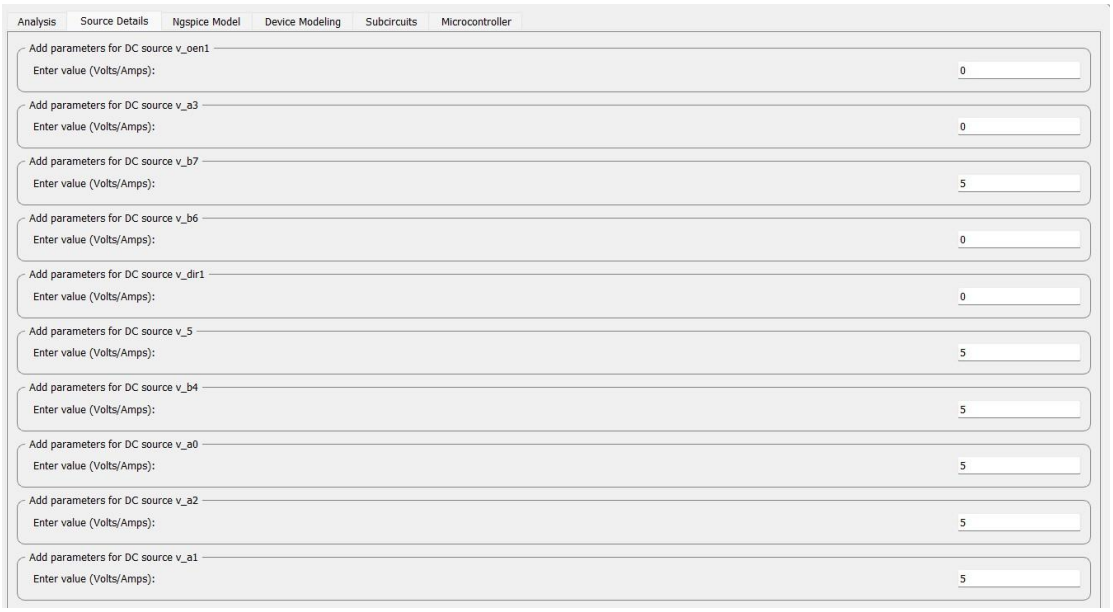

Figure 3.50: Inputs given to Simulation Circuit of 74HC245

3.9.6 Output Plot

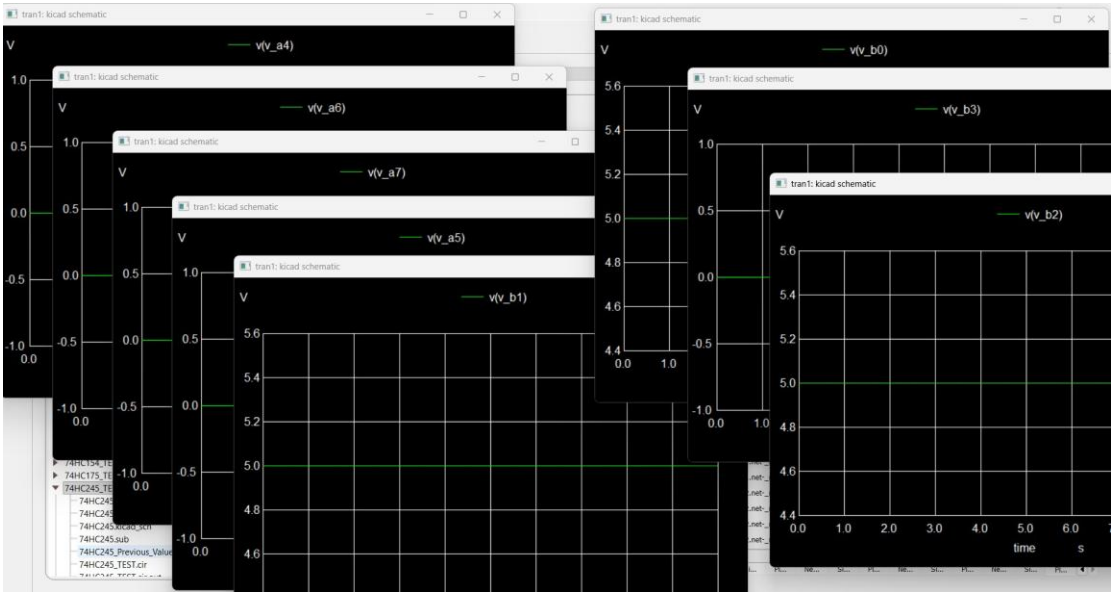

Figure 3.51: Output waveform of 74HC245

3.9.7 Functional Table

Table 4: Function table [1]

Input		Input/output	
$\overline{OE}$	DIR	An	Bn
L	L	A = B	input
L	H	input	B = A
H	X	Z	Z

[1] H = HIGH voltage level;
L = LOW voltage level;
X = don't care;
Z = high-impedance OFF-state.

Figure 3.52: Truth Table for 74HC245

3.10 74LS83

3.10.1 Description

The 74LS83 is a 4-bit binary full adder capable of performing arithmetic addition of two 4-bit binary numbers along with a carry input. It generates a 4-bit sum and a carry output. Binary adders are fundamental components in arithmetic logic units (ALUs) and digital processors.

The IC belongs to the LS-TTL logic family and is known for its reliable arithmetic performance. The 74LS83 is commonly used in calculators, processors, and digital computation circuits. In this project, the adder functionality was implemented and verified using binary input combinations in eSim.

3.10.2 Pin Diagram

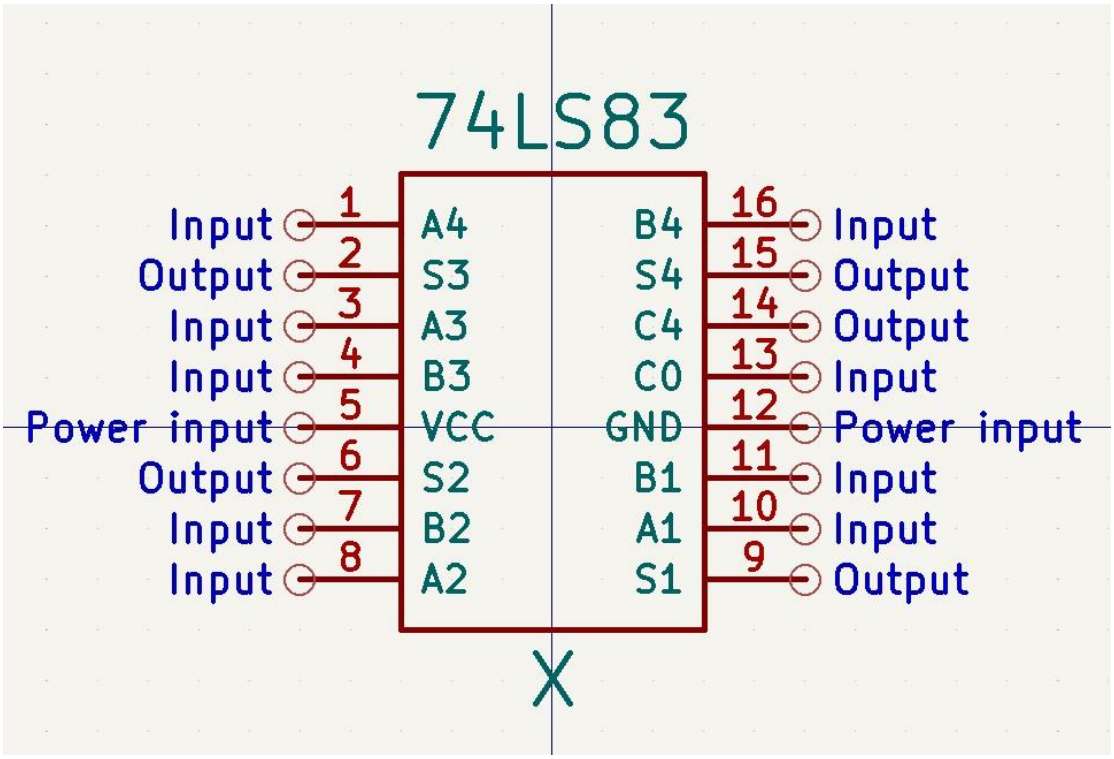

Figure 3.53: Pin Diagram of 74LS83

3.10.3 Schematic Diagram

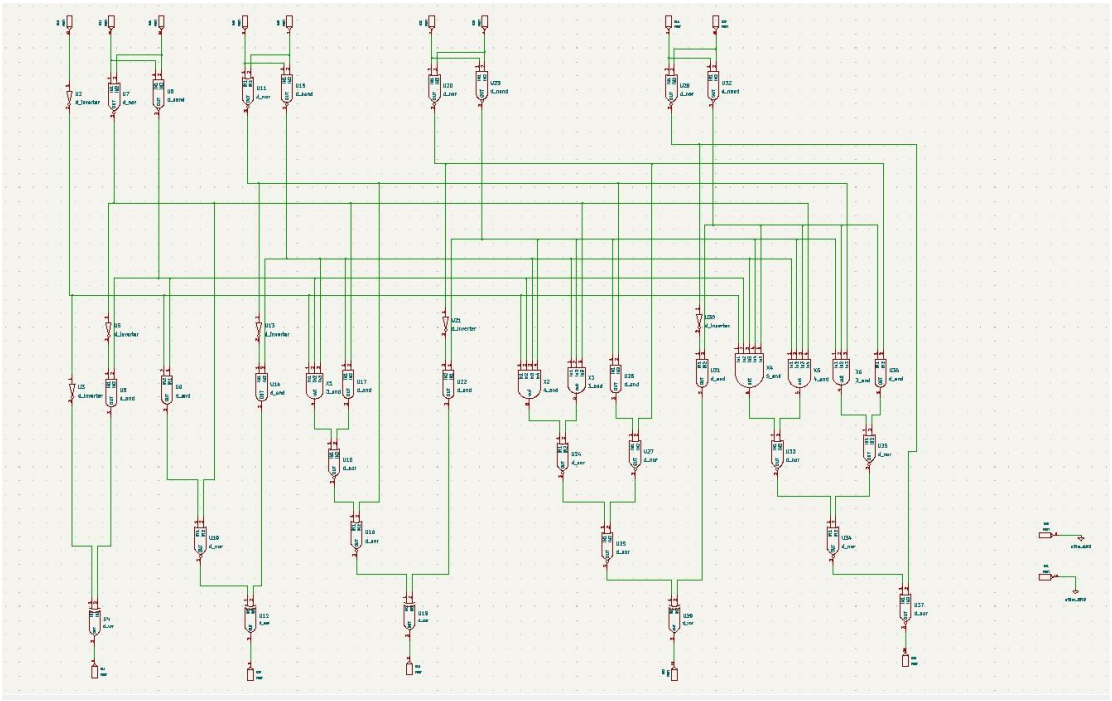

Figure 3.54: Schematic Diagram of 74LS83

3.10.4 Simulation Circuit

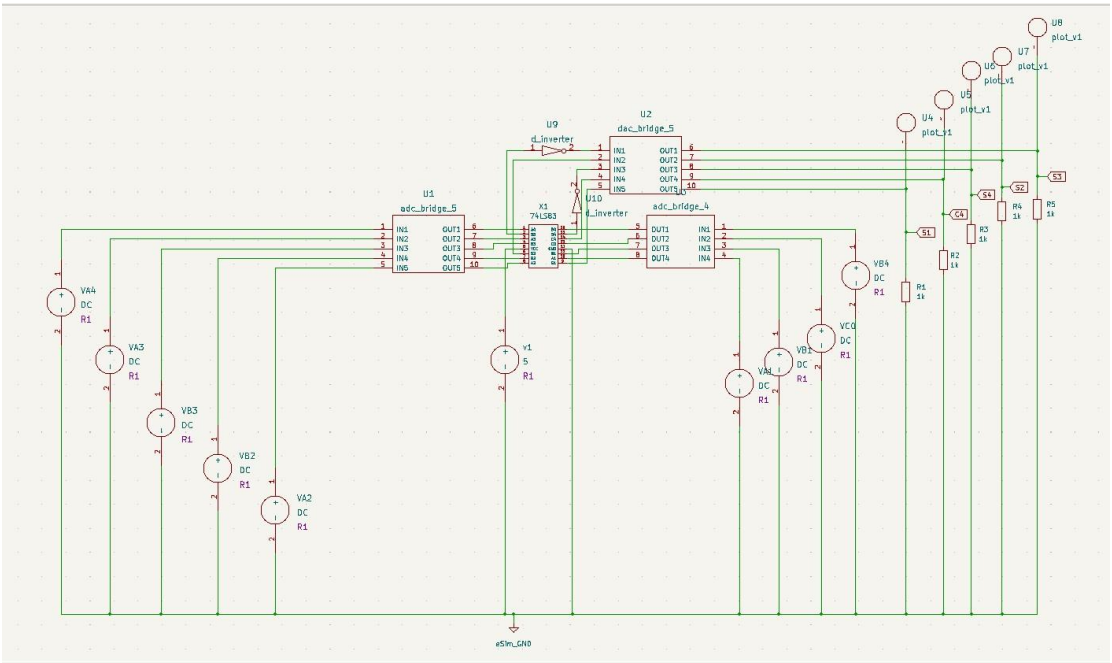

Figure 3.55: Simulation Circuit of 74LS83

3.10.5 Inputs

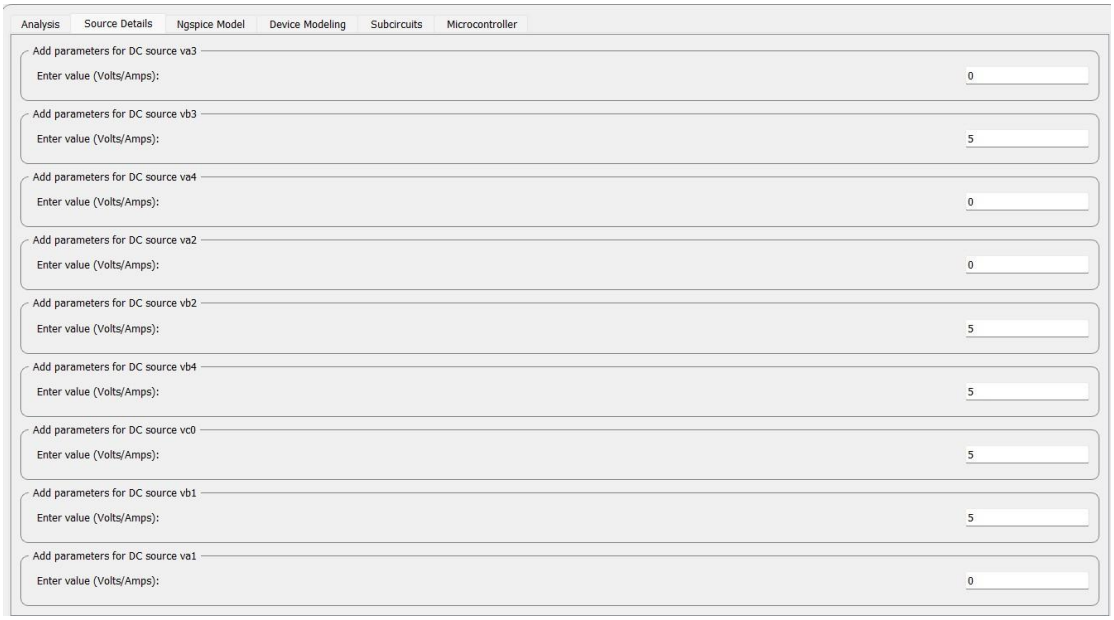

Figure 3.56: Inputs given to Simulation Circuit of 74LS83

3.10.6 Output Plot

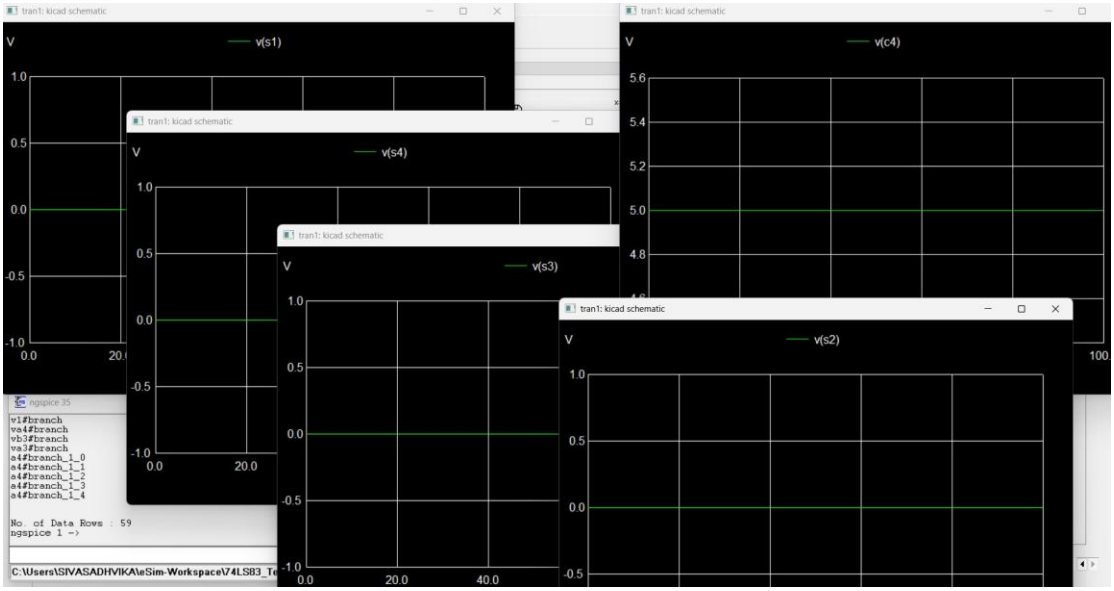

Figure 3.57: Output waveform of 74LS83

3.10.7 Functional Table

FUNCTIONAL TRUTH TABLE

C (n–1)	A_n	B_n	Σ_n	C_n
L	L	L	L	L
L	L	H	H	L
L	H	L	H	L
L	H	H	L	H
H	L	L	H	L
H	L	H	L	H
H	H	L	L	H
H	H	H	H	H

C_1 — C_3 are generated internally
C_0 — is an external input
C_4 — is an output generated internally

Figure 3.58: Truth Table for 74LS83

3.11 LM567

3.11.1 Description

The LM567 is a tone decoder integrated circuit based on a phase-locked loop (PLL). It is designed to detect the presence of a specific input frequency and provide a logic-level output when the detected frequency matches the preset center frequency. The center frequency can be adjusted using external resistor and capacitor values.

This IC is widely used in communication systems, remote control applications, and frequency-based control circuits. Due to its high noise immunity, the LM567 performs reliably even in noisy environments. In this project, the PLL-based operation of the LM567 was modeled and verified using frequency-based input signals in eSim.

3.11.2 Pin Diagram

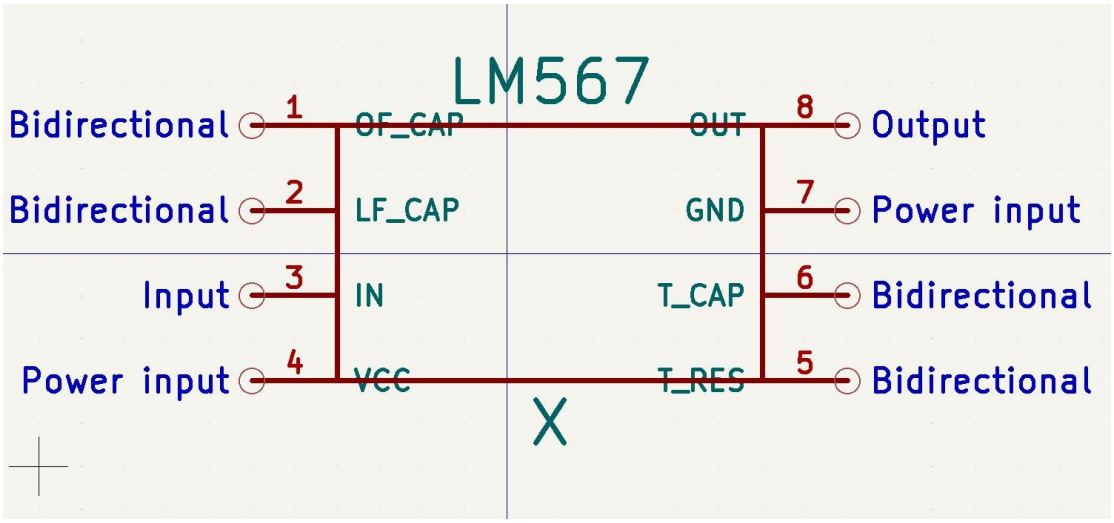

Figure 3.59: Pin Diagram of LM567

3.11.3 Schematic Diagram

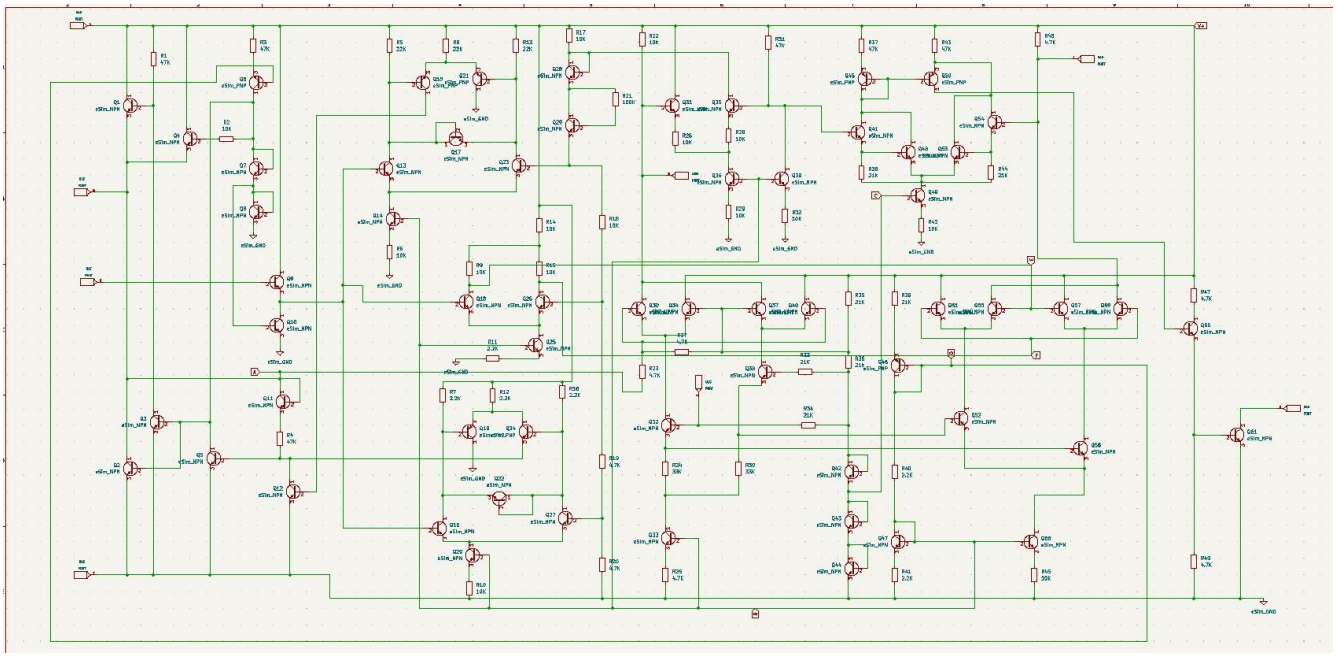

Figure 3.60: Schematic Diagram of LM567

3.11.4 Simulation Circuit

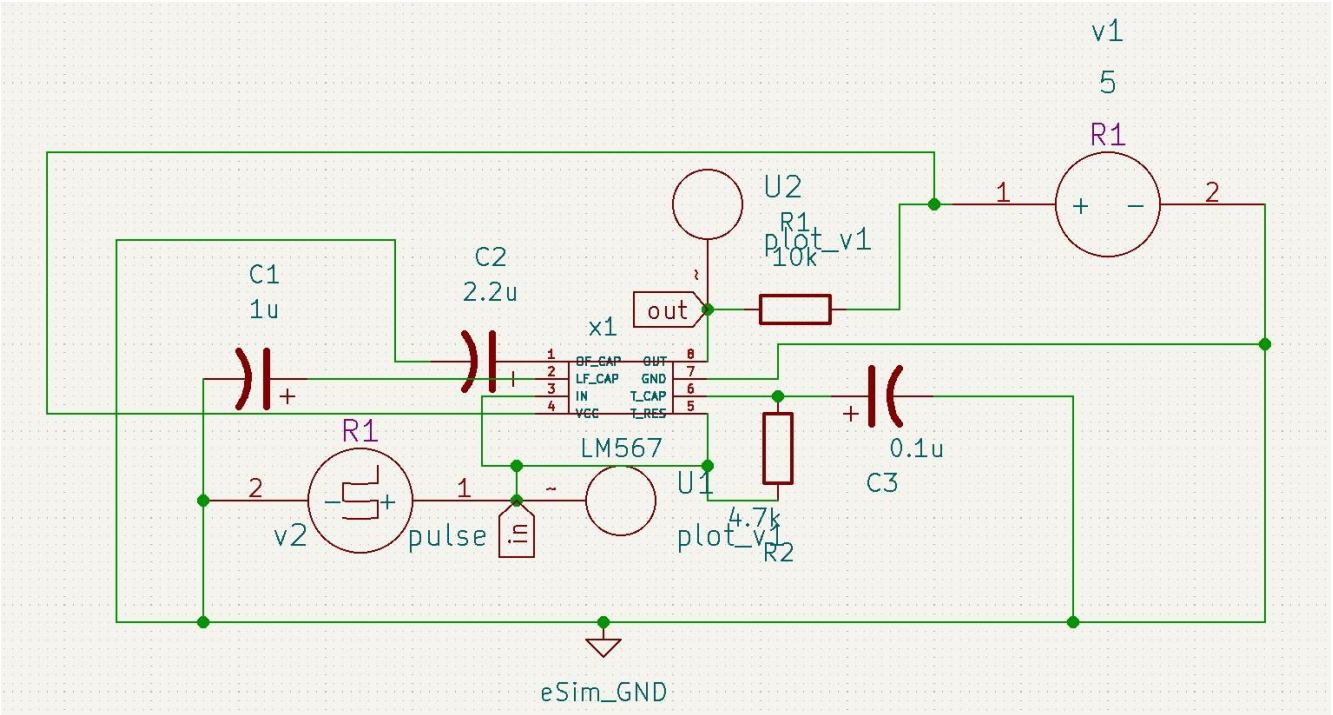

Figure 3.61: Simulation Circuit of LM567

3.11.5 Inputs

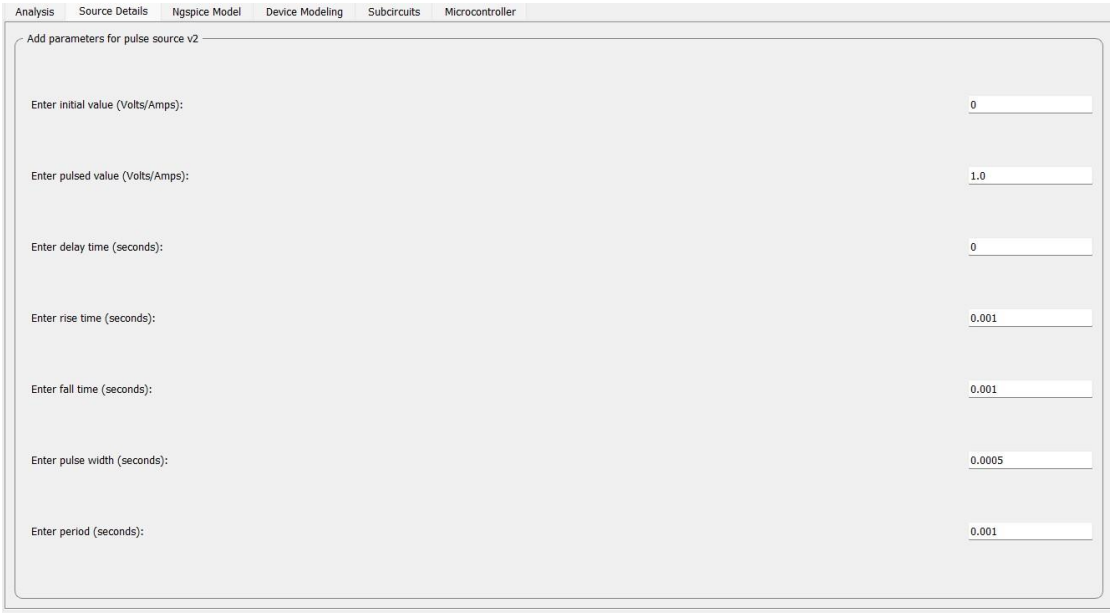

Figure 3.62: Inputs given to Simulation Circuit of LM567

3.11.6 Output Plot

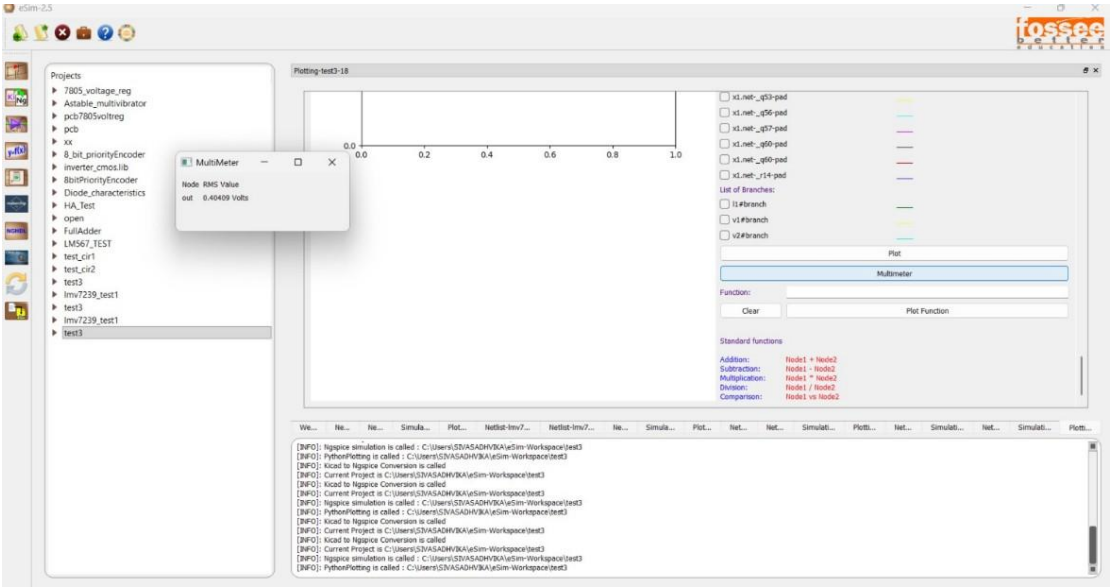

Figure 3.63: Output of LM567

3.12 LMV7239

3.12.1 Description

The LMV7239 is a high-speed, low-power voltage comparator designed for fast and accurate comparison of analog input signals. It operates over a wide supply voltage range and is optimized for low-voltage applications, making it suitable for portable and battery-powered systems. The comparator provides a rapid response to input voltage changes, enabling precise detection of signal transitions. The device features a push-pull output stage that ensures fast switching and reliable logic-level outputs. Due to its low propagation delay and reduced power consumption, the LMV7239 is commonly used in signal conditioning, zero-crossing detection, threshold detection, and mixed-signal processing applications. In this work, the LMV7239 was modeled using the Subcircuit Builder in eSim and verified through simulation to confirm its functional behavior in accordance with the datasheet

.3.12.2 Pin Diagram

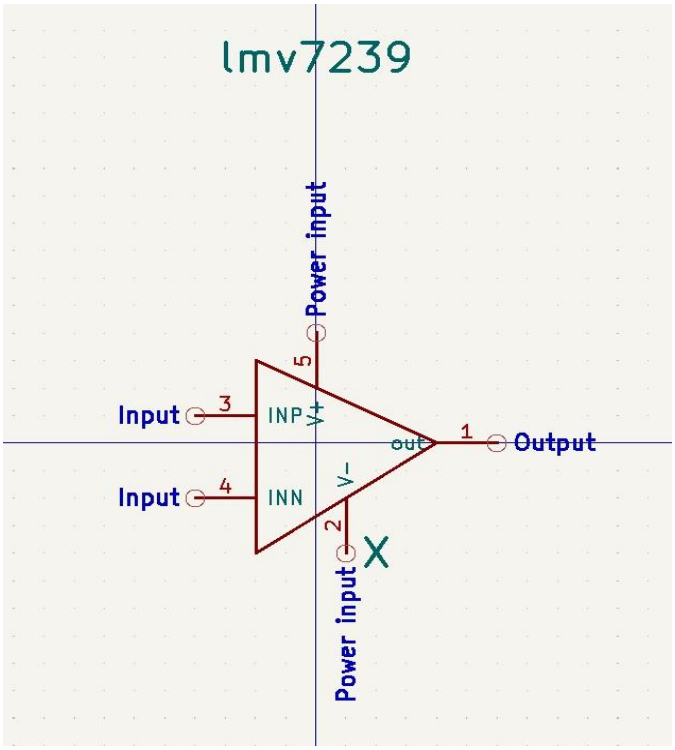

Figure 3.64: Pin Diagram of LMV7239

3.12.3 Schematic Diagram

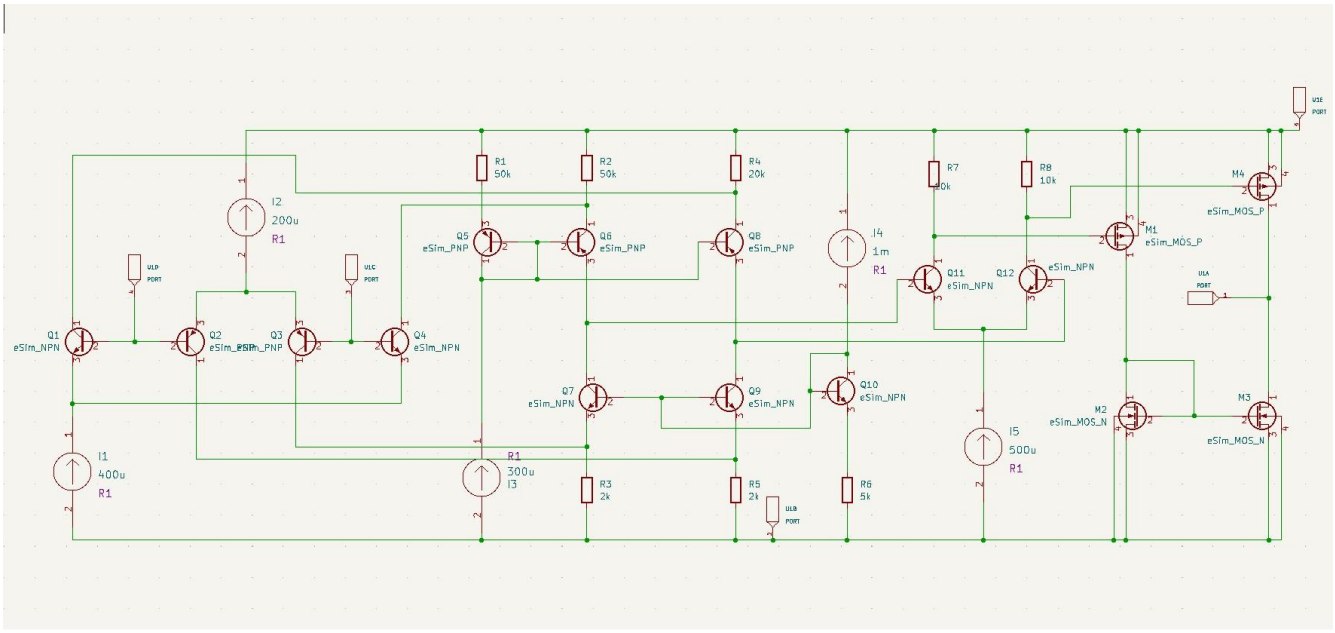

Figure 3.65: Schematic Diagram of LMV7239

3.12.4 Simulation Circuit

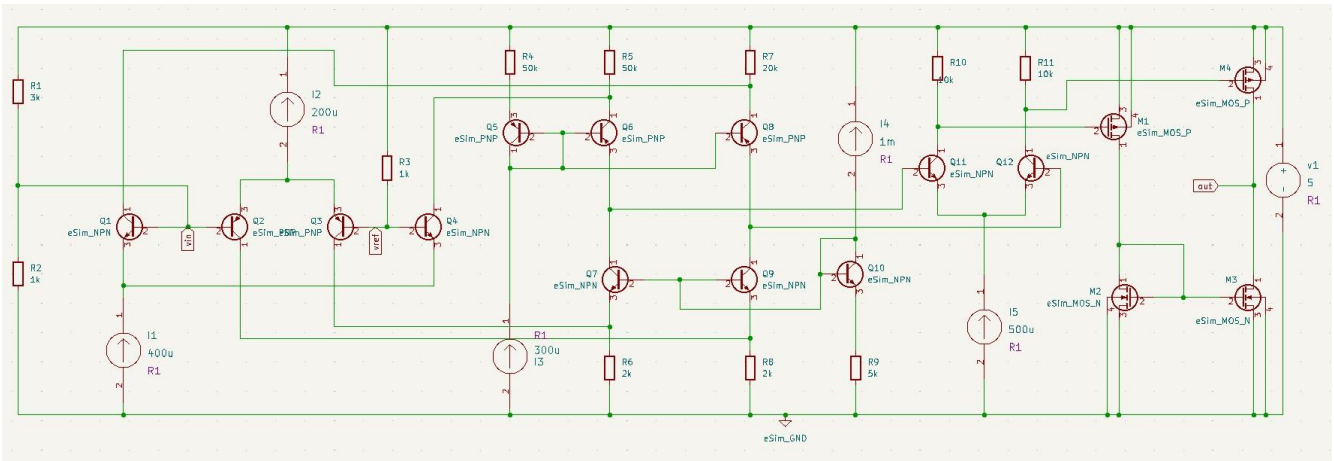

Figure 3.66: Simulation Circuit of LMV7239

3.12.5 Output Plot

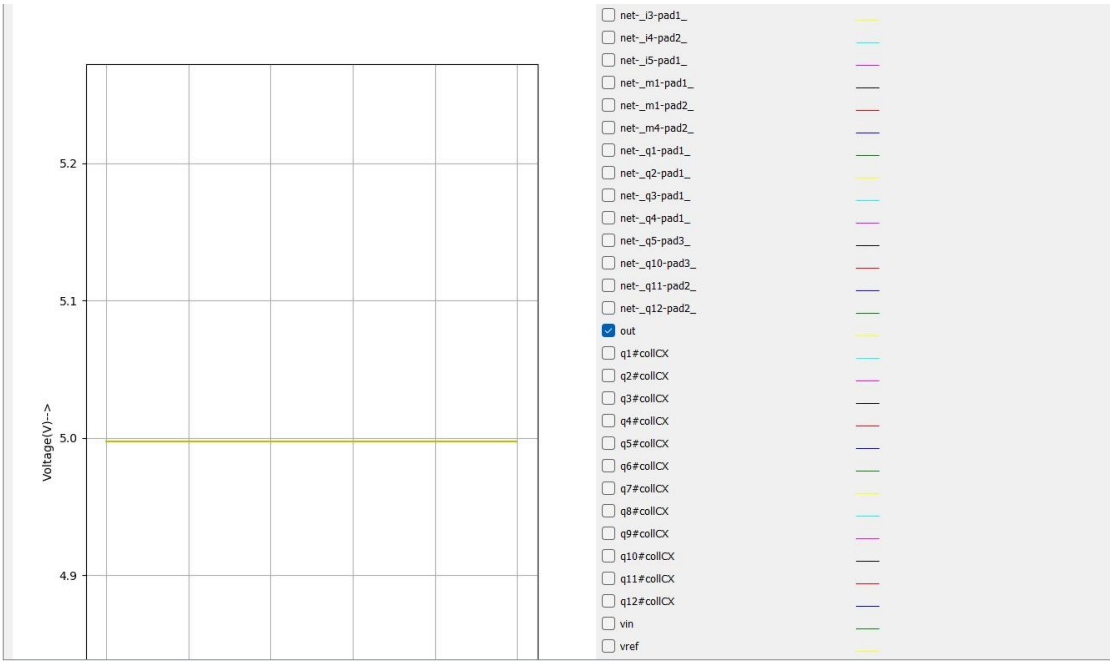

Figure 3.67: Output waveform of LMV7239

Chapter 4

Conclusion and Future Scope

The project successfully achieved its objective of contributing a comprehensive set of accurately modeled integrated circuits to the eSim subcircuit library. Each IC was implemented by carefully analyzing its respective datasheet and was validated through appropriate simulation test circuits to ensure correct functionality and reliability. The contributions include a combination of widely used digital logic ICs and essential analog components, such as logic gates, multiplexers, decoders, flip-flops, buffers, bus transceivers, adders, comparators, and frequency detection circuits.

These IC models serve as fundamental building blocks for designing and simulating complex electronic systems within the eSim environment. By integrating these verified subcircuits into the eSim library, the project enhances the platform's usability for students, educators, and researchers engaged in digital and mixedsignal circuit design. The availability of these models supports practical learning, experimentation, and rapid prototyping of real-world applications.

This initiative highlights the significance of open-source Electronic Design Automation tools in academic and research domains. As the eSim device library continues to expand, it is expected to attract wider adoption within the engineering community and enable the development of more advanced and integrated circuit designs. The outcomes of this work represent a valuable contribution toward strengthening the open-source ecosystem for circuit design and simulation.

Chapter 5

Circuits Contribution

This chapter presents the list of Integrated Circuits (ICs contributed during the internship. Each IC has been carefully modeled, verified through simulation, and successfully added to the eSim subcircuit library. The contributions include both digital and analog ICs covering a broad range of functionalities commonly used in electronic system design. List of ICs Contributed

- 74HC00 – Quad 2-Input NAND Gate
- 74HC02 – Quad 2-Input NOR Gate
- 74HC86 – Quad 2-Input Exclusive-OR Gate
- 74HC74A – Dual D-Type Flip-Flop with Preset and Clear
- 74HC151 – 8-to-1 Data Selector / Multiplexer
- 74HC154 – 4-to-16 Line Decoder / Demultiplexer
- 74HC175 – Quad D-Type Flip-Flop
- 74HC125 – Quad Tri-State Buffer
- 74HC245 – Octal Bidirectional Bus Transceiver
- 74LS83 – 4-Bit Binary Full Adder
- LMV7238 – High-Speed Voltage Comparator
- LM567 – Phase-Locked Loop (PLL) Based Tone Decoder

Chapter 6

Bibliography

- FOSSEE Official Website, [Online]. Available: https://fossee.in.
- eSim Official Website,[Online].Available:https://esim.fossee.in/.
- https://www.alldatasheet.com/datasheet-pdf/pdf/15520/PHILIPS/74HC00.html
- https://www.alldatasheet.com/datasheet-pdf/pdf/15521/PHILIPS/74HC02.html
- https://www.alldatasheet.com/datasheet-pdf/pdf/15668/PHILIPS/74HC86.html
- https://www.alldatasheet.com/datasheet-pdf/pdf/885530/ONSEMI/74HC74A.html
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