Semester-Long Internship Autumn 2025

On

Designing Integrated Circuit in eSim

Submitted by

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Acknowledgment

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This internship has been an enriching learning experience, allowing me to work closely with open-source EDA tools, develop IC subcircuits in eSim, and gain exposure to real-world circuit modeling and simulation workflows. The knowledge acquired during this period will undoubtedly support my future academic and professional pursuits.

I would also like to thank the entire FOSSEE team for their coordination, assistance, and timely interactions at various stages of this work. Their collective efforts ensured smooth workflow, resource accessibility, and effective project execution.

Contents

Chapter 1

Introduction

1.1 FOSSEE

FOSSEE, which stands for Free/Libre and Open Source Software for Education, is an organization based at IIT Bombay. It is a remarkable initiative aimed at promoting the use of open-source software in education and research. It was established with the mission to reduce dependency on proprietary software and to encourage the adoption of open-source alternatives. FOSSEE offers a wide range of tools and resources that cater to various academic and professional needs.

It provides comprehensive documentation, tutorials, workshops, and hands-on training sessions to empower students, educators, and professionals to leverage open-source software for their projects and coursework. The organization's commitment to fostering a collaborative and inclusive environment has significantly contributed to the democratization of technology and has opened up new avenues for innovation and learning

1.2 eSim

eSim, created by the FOSSEE project at IIT Bombay, is a versatile open-source software tool for circuit design and simulation. It combines various open-source software packages into one cohesive platform, making it easier to design, simulate, and analyze electronic circuits. This tool is particularly useful for students, educators, and professionals who need an affordable and accessible alternative to proprietary software.

eSim offers features for schematic creation, circuit simulation, and PCB design, and includes an extensive library of components. The Subcircuit feature is a significant enhancement, enabling users to design complex circuits by integrating simpler subcircuits. Through eSim, FOSSEE promotes the use of open-source solutions in engineering education and professional fields, encouraging innovation and collaboration.

1.3 NgSpice

NgSpice is an open-source SPICE simulator for electric and electronic circuits. It can simulate various circuit elements, including JFETs, bipolar and MOS transistors, passive elements (R, L, C), diodes and other devices, all interconnected in a netlist.

Digital circuits are also simulated, ranging from single gates to complex circuits, including combinations of analog, digital, and mixed-signal circuits. NgSpice offers a wealth of device models for active, passive, analog, and digital elements. Users input their circuits as netlists, and the output is one or more graphs of currents, voltages, and other electrical quantities, or saved in a data file

1.4 Makerchip

Makerchip is a platform that offers convenient and accessible tools for digital circuit design. It provides both browser-based and desktop-based environments for coding, compiling, simulating, and debugging Verilog designs. Makerchip supports a combination of open-source and proprietary tools, ensuring a comprehensive range of capabilities.

Users can simulate Verilog/SystemVerilog/Transaction-Level Verilog code in Makerchip. eSim is interfaced with Makerchip using a Python-based application called Makerchip-App, which launches the Makerchip IDE. Makerchip aims to make circuit design easy and enjoyable for users of all skill levels. The platform provides a userfriendly interface, intuitive workflows, and a range of helpful features that simplify the design process and enhance the overall user experience.

The main drawback of these open-source tools is that they are not comprehensive. While some are capable of PCB design (e.g., KiCad), others focus on simulations (e.g., EDA). To the best of our knowledge, there is no open-source software that combines circuit design, simulation, and layout design in one platform. eSim addresses this gap by integrating all these capabilities.

Chapter 2

Features of eSim

The objective behind the development of eSim is to provide an open-source EDA solution for electronics and electrical engineers. The software is capable of performing schematic creation, PCB design, and circuit simulation (analog, digital, and mixedsignal). It also provides facilities to create new models and components. Thus, eSim offers the following features:

1. Schematic Creation: eSim provides an easy-to-use graphical interface for drawing circuit schematics, making it accessible for users of all levels. Users can drag and drop components from the library onto the schematic, simplifying the design process. Comprehensive editing tools allow for easy modification of schematics, including moving, rotating, and labeling components.

2. Circuit Simulation: eSim supports SPICE (Simulation Program with Integrated Circuit Emphasis), a standard for simulating analog and digital circuits. Users can perform various types of analysis such as transient, AC, and DC, providing insights into circuit behavior over time and frequency. An integrated waveform viewer helps visualize simulation results, aiding in the analysis and debugging of circuit designs.

3. PCB Design: The PCB layout editor allows users to place components and route traces with precision. eSim includes DRC (Design Rule Check) capabilities to ensure that the PCB design adheres to manufacturing constraints and electrical rules. Users can generate Gerber files, which are standard for PCB fabrication, directly from their designs.

4. Subcircuit Feature: This feature enables users to create complex circuits by integrating smaller, simpler subcircuits, promoting modular and hierarchical design approaches. Subcircuits can be reused in different projects, saving time and effort in redesigning common circuit elements.

5. Open Source Integration: eSim integrates several open-source tools like KiCad, NgSpice, and GHDL, providing a comprehensive suite for electronic design automation. Being open-source, eSim is free to use, making advanced circuit design tools accessible without the need for expensive licenses.

Chapter 3

Problem Statement

To design and develop various analog and digital integrated circuit models in the form of sub-circuits using device model files already present in the eSim library. These IC models should be useful for future circuit design purposes by developers and users once they are successfully integrated into the eSim subcircuit library.

3.1 Approach

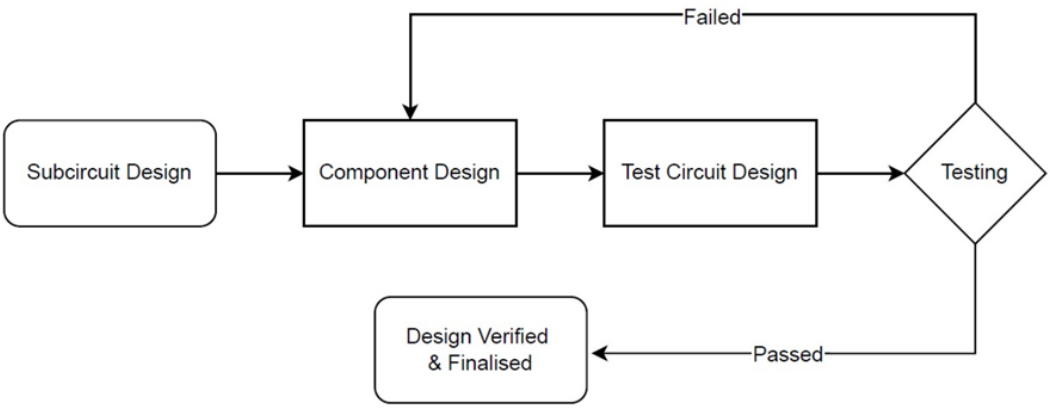


Figure 3.1: Flowchart of IC Design Approach Followed

My approach to implementing the problem statement involved a systematic process, leveraging datasheets from leading Integrated Circuit (IC) manufacturers such as Texas Instruments, Analog Devices, and NXP Semiconductors. I focused on selecting ICs with diverse functionalities, including precision amplifiers, comparators, voltage regulators, and operational amplifiers. The process is outlined in the following steps:

1. Analyzing Datasheets: The first step involved an in-depth review of datasheets for various analog and digital ICs. I aimed to identify circuits suitable for implementation in eSim that were not already present in the eSim library. This process included scrutinizing the detailed schematics of each IC, evaluating component values, and understanding specifications. The goal was to select ICs that offered unique functionalities or enhancements not yet covered.

2. Subcircuit Creation: After selecting appropriate ICs, I proceeded to model these as sub-circuits within eSim. I utilized the model files available in the eSim device model library and ensured that my

designs adhered strictly to the specifications outlined in the official datasheets. This phase also involved creating accurate symbol and pin diagrams for each IC, in accordance with the packaging and pin descriptions provided in the datasheets. This step was crucial for ensuring the fidelity of the subcircuit models.

3. Test Circuit Design: With the sub-circuits created, I then designed and built test circuits based on the datasheets. This step was essential for verifying the functionality of each sub-circuit. I developed a series of test cases and constructed corresponding test circuits to evaluate the performance and accuracy of the implemented IC models.

4. Schematic Testing: Following the construction of test circuits, I conducted simulations to analyze the outputs. This involved generating waveforms and plots to assess the behavior of the circuits. I employed KiCad for converting designs to NgSpice netlists and utilized eSim's simulation features to perform comprehensive testing.

If the simulated outputs deviated from expected results, it signaled potential errors in the schematic. In such instances, I revisited the design phase to identify and correct discrepancies. The iterative process of debugging and re-testing continued until the test cases produced satisfactory results. Once the IC models met the desired performance criteria, they were deemed successful, marking the completion of the design process.

Chapter 4

NE5532A

4.1 Description

The NE5532A is a high-performance dual low-noise operational amplifier designed for audio and high-fidelity applications. It features excellent noise performance, high output drive capability, and a 10 MHz unity-gain bandwidth, making it ideal for professional audio equipment, active filters, and precision instrumentation.

4.2 Pin Diagram

The pin diagram illustrates the dual-op-amp pinout of the NE5532A, showing the individual inputs, outputs, and power supply pins for both amplifier stages. Proper pin connection is critical for implementing circuits like audio preamplifiers, active filters, and precision signal conditioning stages.

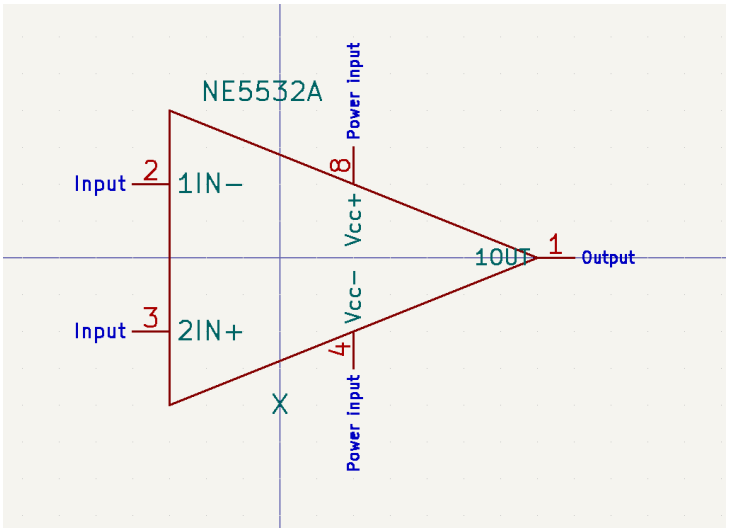


Figure 4.1: Pin Configuration of the NE5532A

4.3 Sub Circuit Layout

The subcircuit layout represents the internal transistor-level architecture of the NE5532A, including the differential input pairs, current mirrors, and output driver stages. This model allows eSim to accurately simulate the device's low-noise characteristics and wide-bandwidth frequency response.

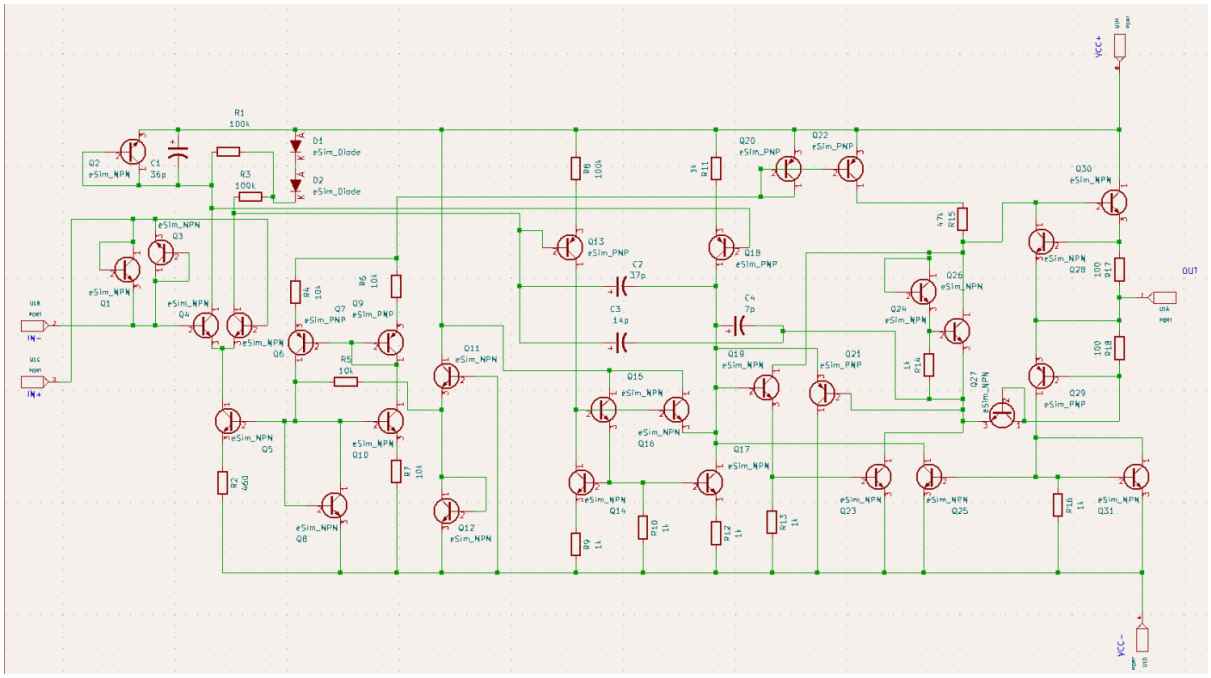


Figure 4.2: Subcircuit Schematic of the NE5532A

4.4 Test Circuit

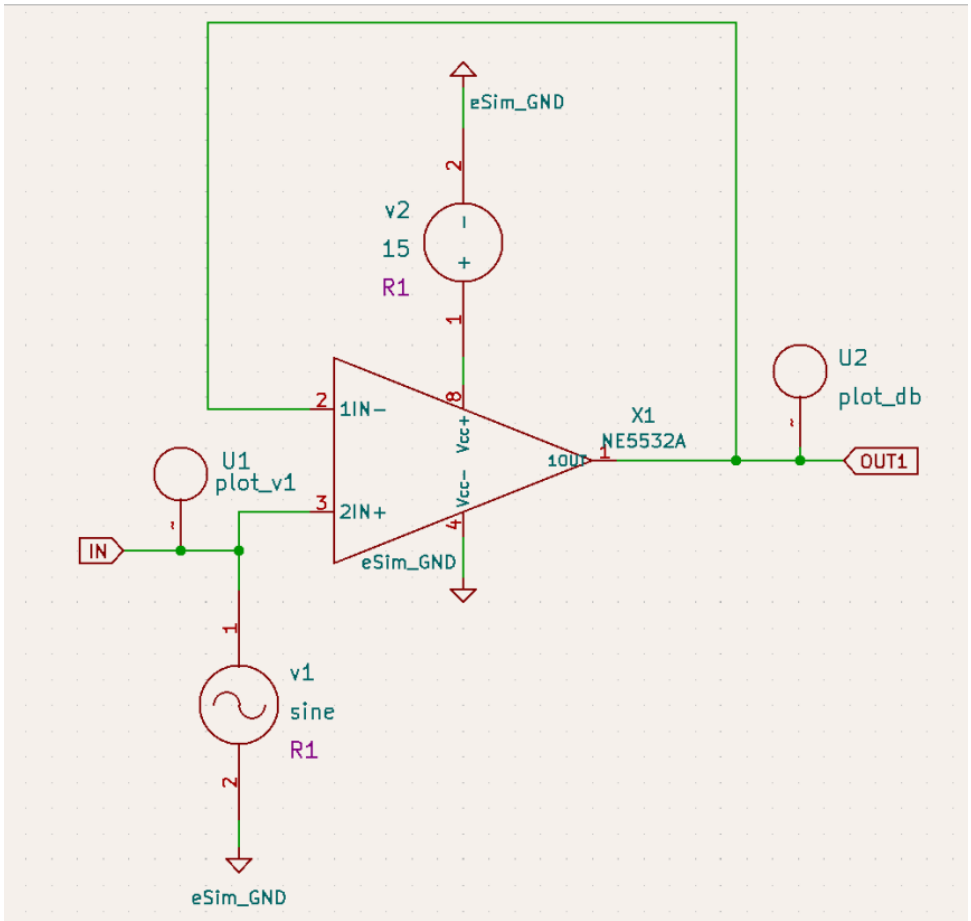


Figure 4.3: Test Circuit of the NE5532A

The test circuit configures the NE5532A as a unity-gain buffer (voltage follower) powered by $\pm$15V, with the output fed back to the inverting input. This setup is used to verify the op-amp's stability and linear performance across a wide frequency range using AC analysis.

4.5 Input Waveform

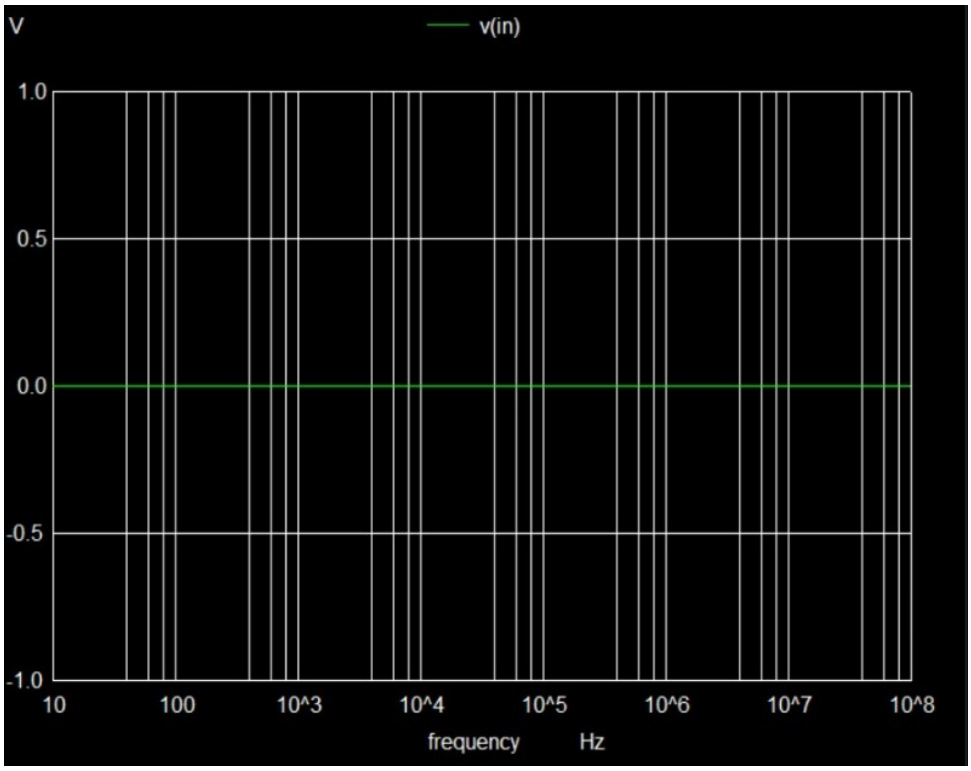


Figure 4.4: Input Waveform of the NE5532A

An AC sweep from 10 Hz to 100 MHz was run while plotting the output magnitude in dB using `plot_db`; the resulting Bode plot shows a flat horizontal line at approximately 0 dB across the entire audio band before rolling off at higher frequencies.

4.6 Output Waveform

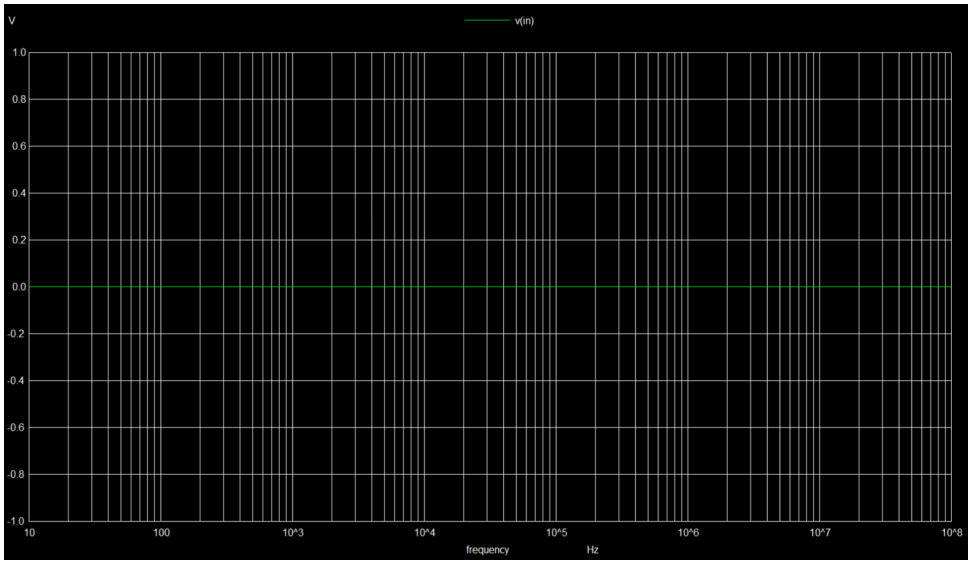


Figure 4.5: Output Waveform of the NE5532A

In the unity-gain buffer test circuit, the NE5532A acts as a voltage follower powered from ± 15 V, with the non-inverting input driven by an AC source and the output directly fed back to the inverting input (feedback logic). The closed-loop gain $|V_{out}/V_{in}|$ is 1 (since 0 dB corresponds to unity gain via $20 \times \log 10(V_{out}/V_{in}) = 0$), so the model behaves as a stable, linear unity-gain voltage follower with flat small-signal frequency response in the audio range, consistent with the NE5532/NE5532A datasheet description of a low-noise audio op-amp that is internally compensated and specified for operation at unity gain with a unity-gain bandwidth on the order of 10 MHz.

Chapter 5

MC1495D

5.1 Description

The MC1495D is a wideband linear four-quadrant analog multiplier designed for applications where the output is a linear product of two input voltages. This device offers excellent linearity, wide bandwidth, and temperature stability, making it suitable for analog multiplication, frequency doubling, phase detection, and gain control systems.

5.2 Pin Diagram

The pin diagram shows the X and Y analog inputs, reference pins, and output nodes of the MC1495D. Correct pin connections allow the IC to perform four-quadrant multiplication where both inputs can be positive or negative.

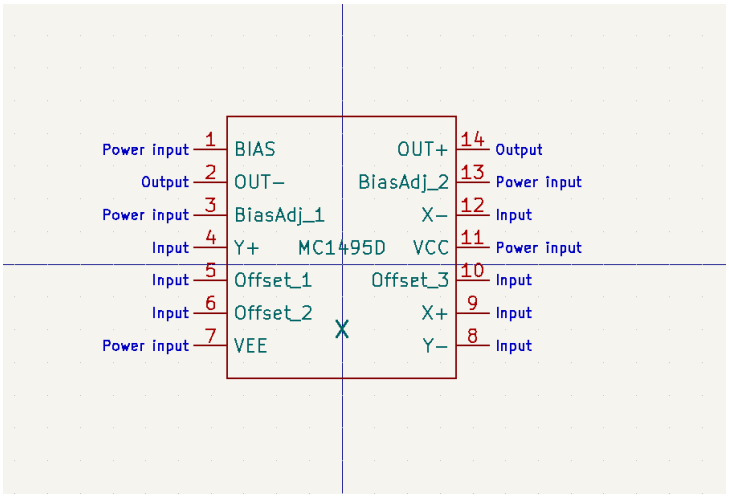


Figure 5.1: Pin Configuration of the MC1495D

5.3 Sub Circuit Layout

The subcircuit layout depicts the internal multiplier core with balanced input stages, multiplying transistor array, and output amplifier. This structure enables accurate four-quadrant multiplication with high input impedance and low offset error.

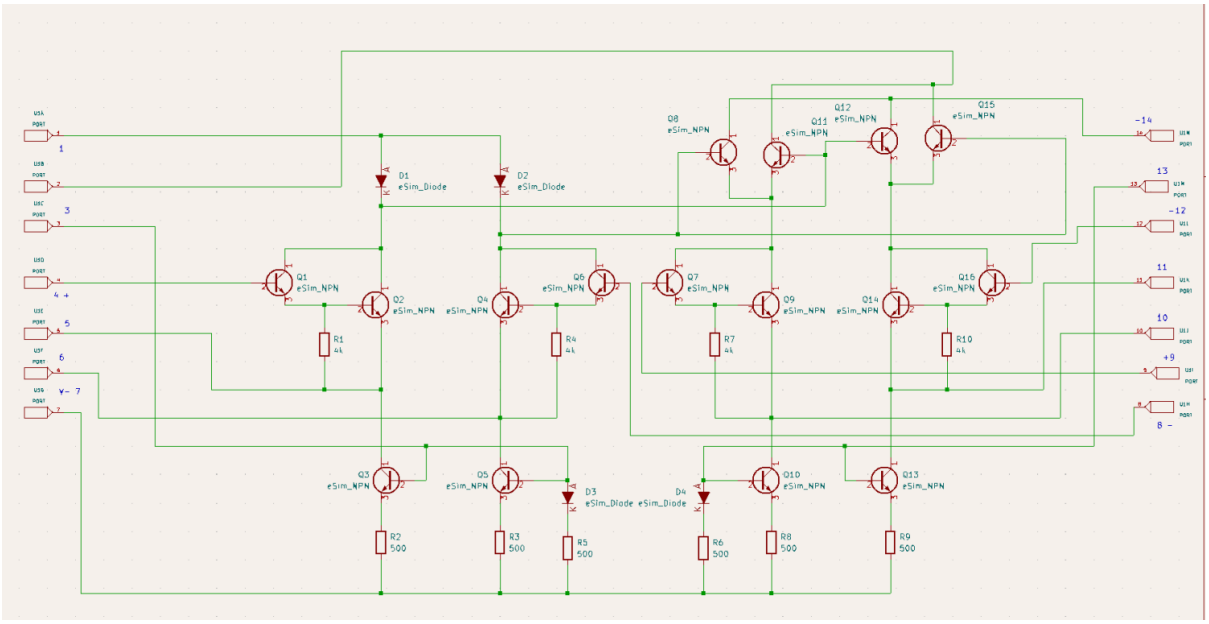


Figure 5.2: Subcircuit Schematic of the MC1495D

5.4 Test Circuit

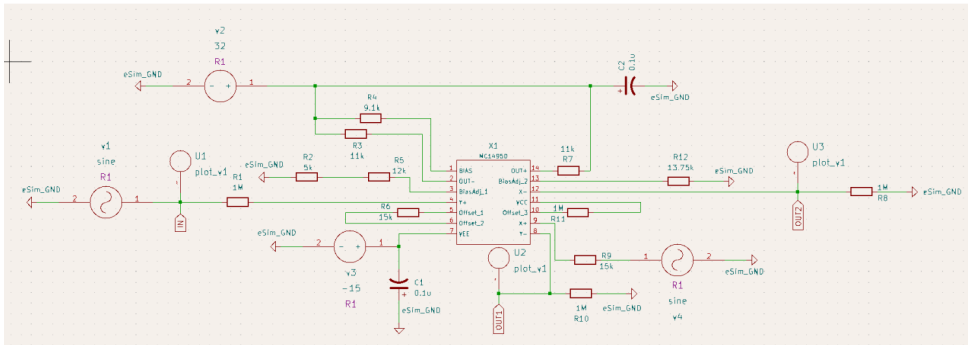


Figure 5.3: Test Circuit of the MC1495D

The test circuit applies low-frequency analog signals to both X and Y inputs through current-sense resistors. The ± 15 V supply powers the IC, and the output is monitored to verify the multiplication behavior and frequency response.

5.5 Input Waveform

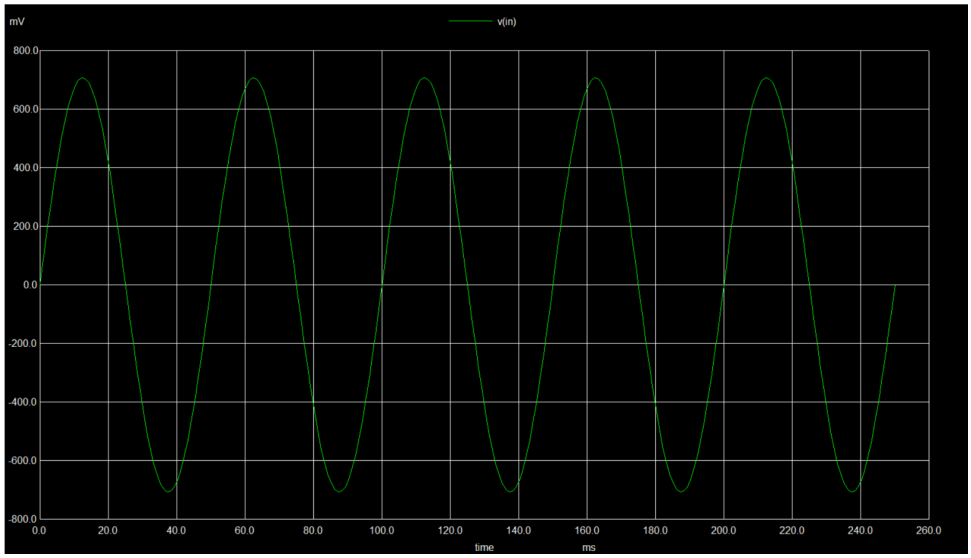


Figure 5.4: Input Waveform of the MC1495D

A 1 V, 20 Hz signal was applied to the X and Y inputs through 1 MΩ series ”sense” resistors, and the small-signal (AC) analysis was used to measure how much current actually enters the IC. From this current, the equivalent input resistance $R_{in} = V/I$ works out to tens of megaohms (around 20–30 MΩ), which matches the range specified in the MC1495D datasheet and shows that the model does not significantly load the source.

5.6 Output Waveform

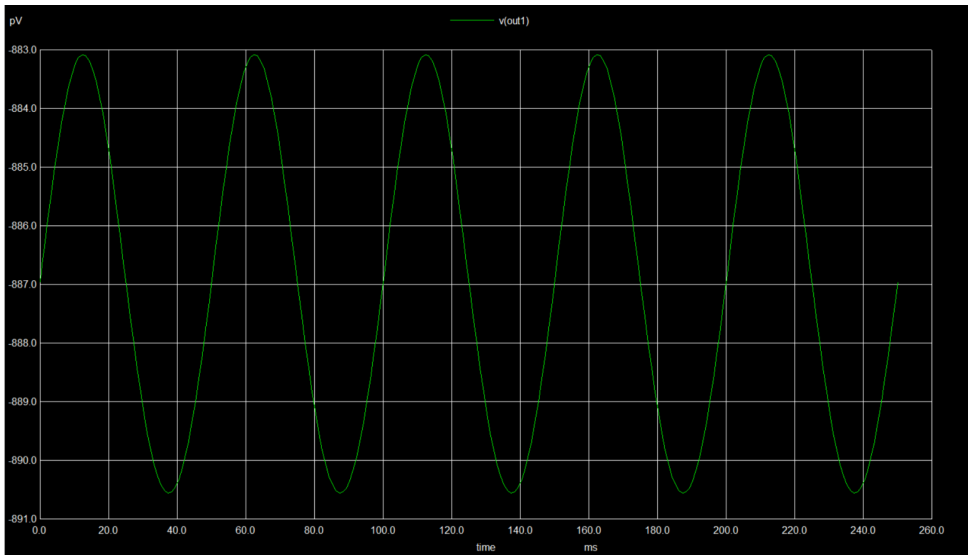


Figure 5.5: Output Waveform of the MC1495D

The 20 Hz transient plots support this high-input-impedance result: they show a clean sine wave at the input and only picovolt-level voltage across the 1 MΩ sense resistors, meaning the current is extremely small (high resistance) and therefore consistent with the very high input resistance obtained from the

AC calculation. This test confirms that the MC1495D model really has the very high input resistance required by the datasheet.

Chapter 6

LM112

6.1 Description

The LM112 is a precision operational amplifier designed for low-noise, high-gain applications in measurement and control systems. It offers high input impedance, low offset voltage, and excellent CMRR, making it suitable for sensor signal conditioning and precision data acquisition.

6.2 Pin Diagram

The pin diagram shows the non-inverting input, inverting input, output, and power supply pins of the LM112. The pin configuration supports both single-supply and dual-supply operation for flexible circuit design.

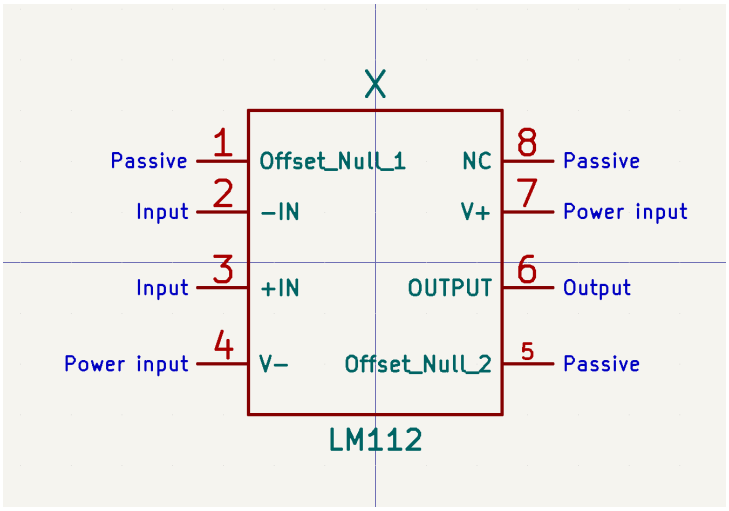


Figure 6.1: Pin Configuration of the LM112

6.3 Sub Circuit Layout

The subcircuit layout depicts the LM112's internal architecture with precision input buffer stages, gain-setting networks, and output driver. This design achieves low input offset and high common-mode rejection for precision analog signal processing.

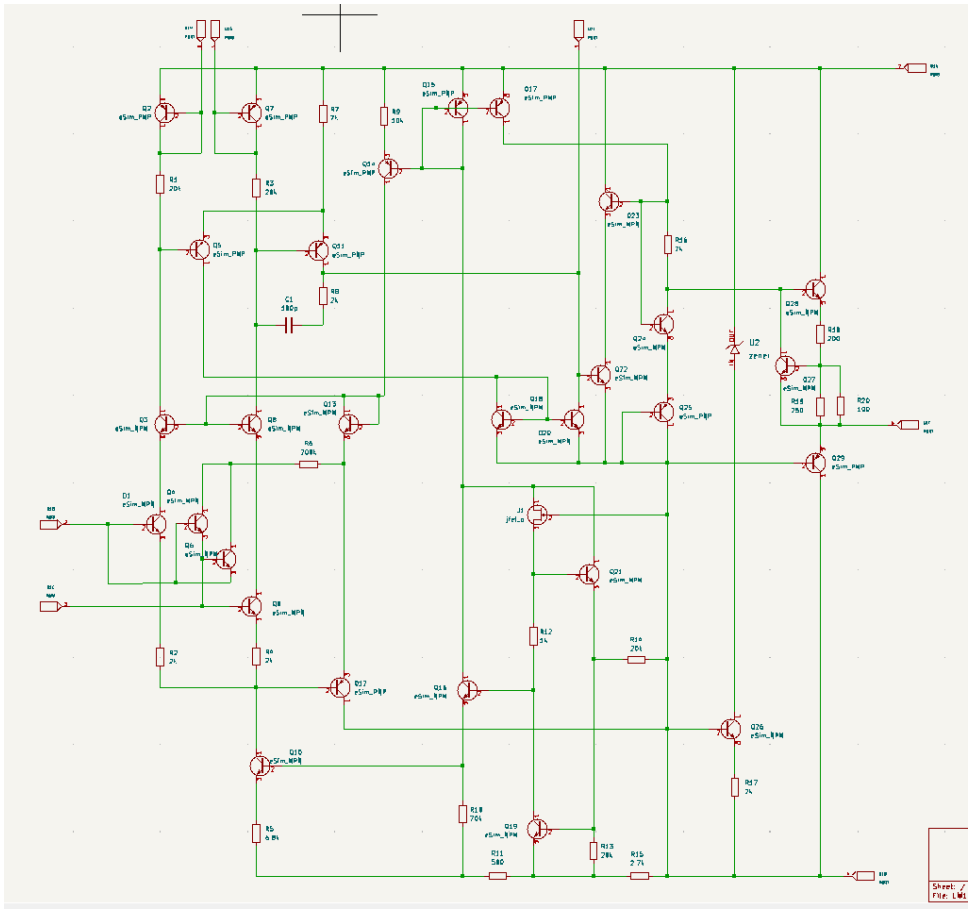


Figure 6.2: Subcircuit Schematic of the LM112

6.4 Test Circuit

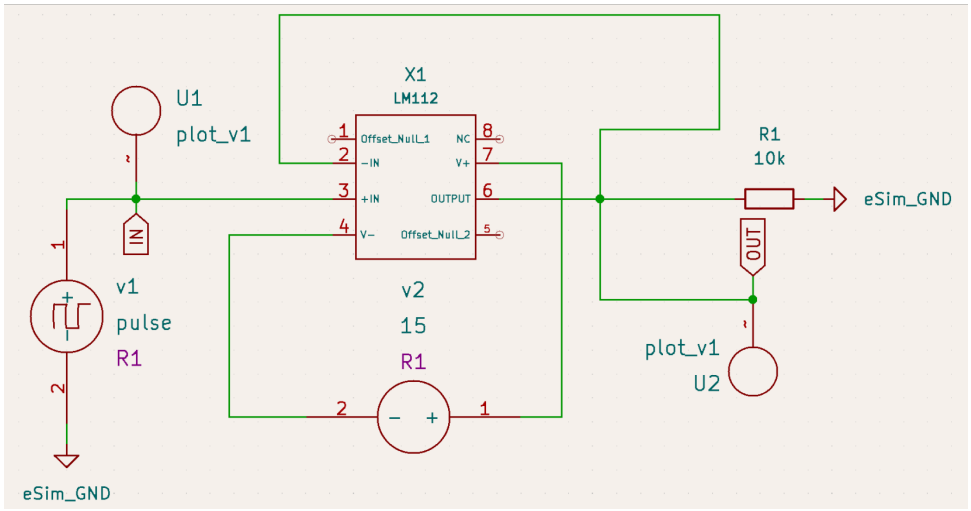


Figure 6.3: Test Circuit of the LM112

The test circuit configures the LM112 as a precision amplifier with gain-setting resistors. A small AC signal is applied to the input, and the op-amp is powered from dual supplies to verify its precision and stability.

6.5 Input Waveform

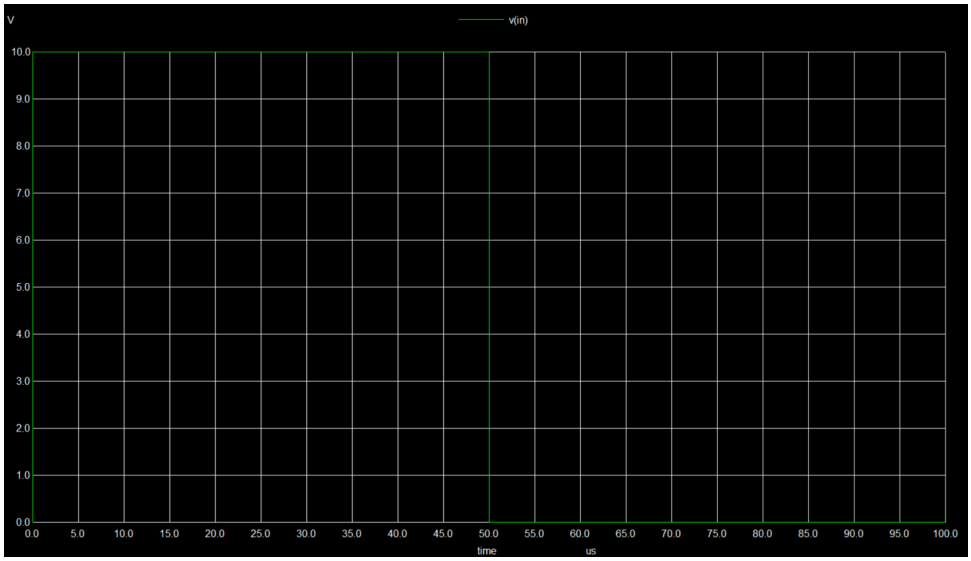


Figure 6.4: Input Waveform of the LM112

In the unity-gain buffer test, the LM112 was powered from ± 15 V, with the non-inverting input driven by a 10 V PULSE source and the output directly fed back to the inverting input (feedback logic). A transient analysis was run to capture the large-signal response, specifically focusing on the output's transition behavior.

6.6 Output Waveform

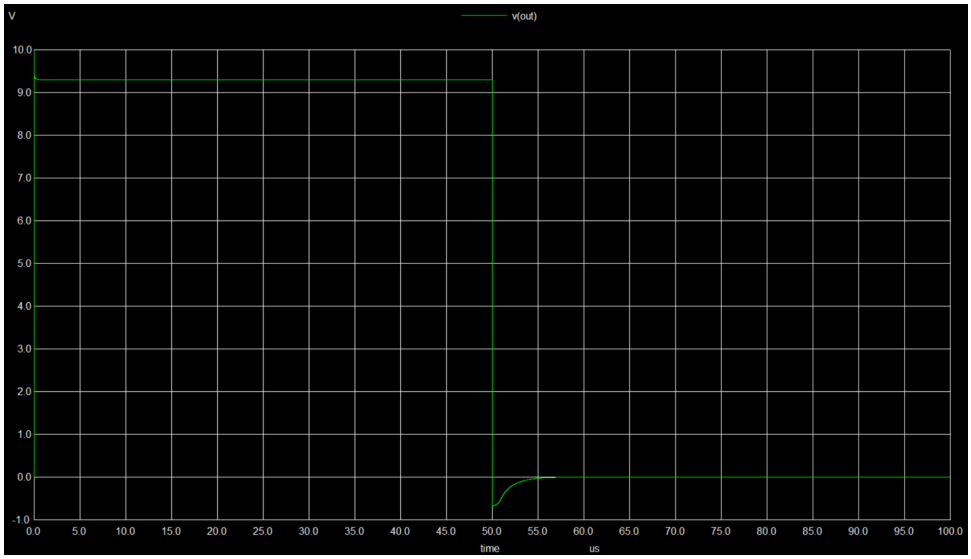


Figure 6.5: Output Waveform of the LM112

The resulting graph demonstrates that the output sits at approximately 9.2 V during the high state instead of reaching the 15 V rail. This matches the LM112 datasheet statement that, with a 10 $k\Omega$ load, the output swing remains several volts away from the rails, and shows that the model correctly simulates. When the input falls at 50 μs, the output exhibits a slow, nearly linear ramp instead of an instantaneous edge. By tuning the internal compensation capacitor (C1) to 180 pF, the measured Slew Rate (SR) was adjusted to approximately 0.3 V/μs, which is the correct order of magnitude for the LM112's micropower behavior and aligns with the "Voltage Follower Pulse" and large-signal response plots in the datasheet.

Chapter 7

LM12CL

7.1 Description

The LM12CL is a low-noise precision operational amplifier designed for audio and precision signal processing applications. It features low input noise voltage, high slew rate, and wide bandwidth, making it suitable for high-fidelity audio systems and sensitive measurement circuits.

7.2 Pin Diagram

The pin diagram shows the dual-supply operational amplifier configuration of the LM12CL, with inverting and non-inverting inputs, output, and power supply pins. This standard op-amp pinout enables universal compatibility with common amplifier circuits.

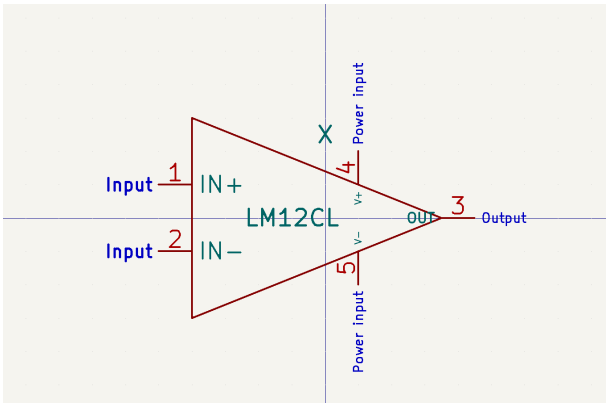


Figure 7.1: Pin Configuration of the LM12CL

7.3 Sub Circuit Layout

The subcircuit layout represents the LM12CL at transistor level, including its low-noise input stage, gain stages, compensation network, and output driver. This design achieves the low-noise and wide-bandwidth characteristics specified for audio and precision applications.

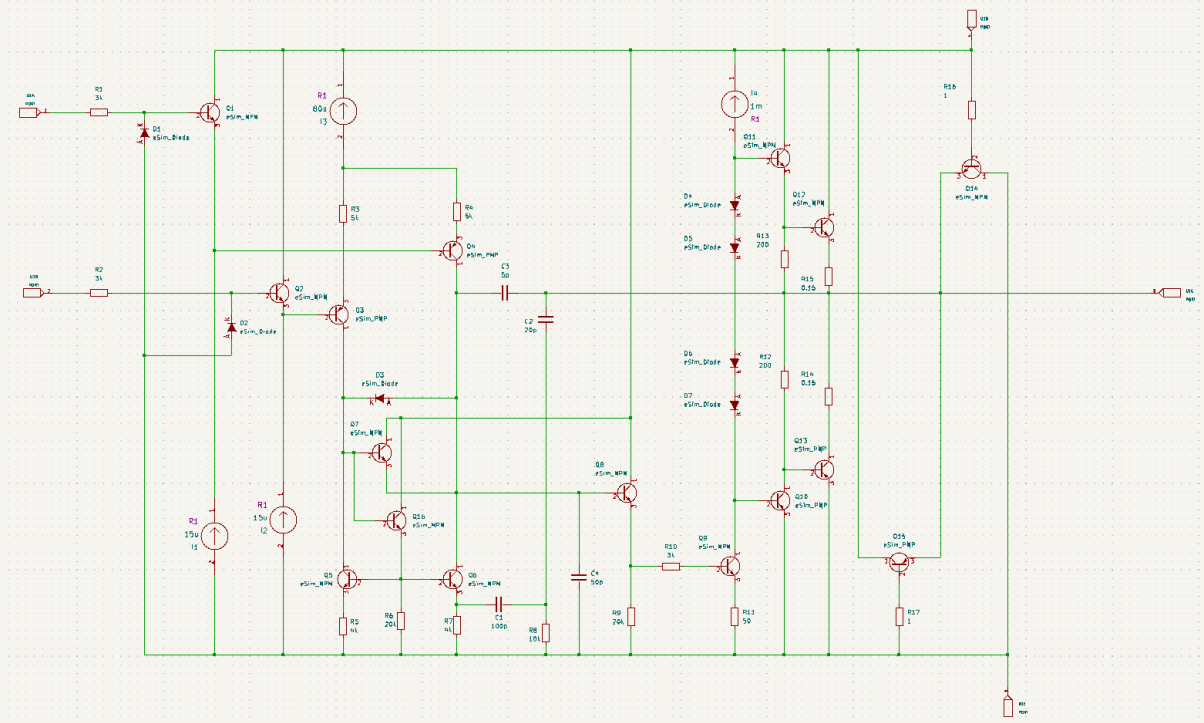


Figure 7.2: Subcircuit Schematic of the LM12CL

7.4 Test Circuit

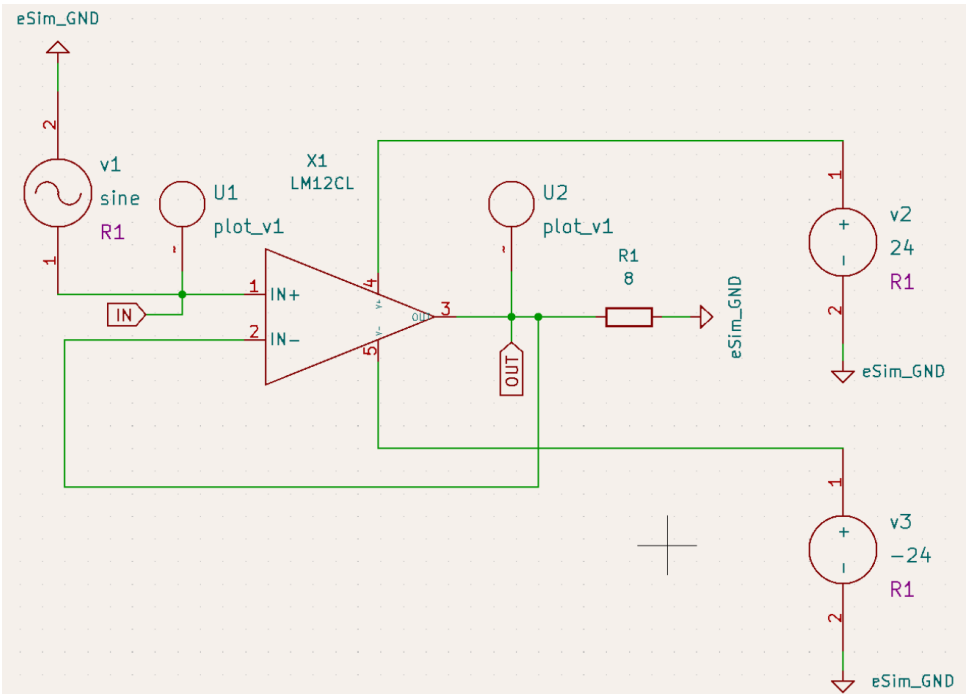


Figure 7.3: Test Circuit of the LM12CL

The test circuit configures the LM12CL as a unity-gain buffer powered from ± 15 V supplies. An AC signal is applied to the non-inverting input, and AC analysis is performed to measure the frequency

response.

7.5 Input Waveform

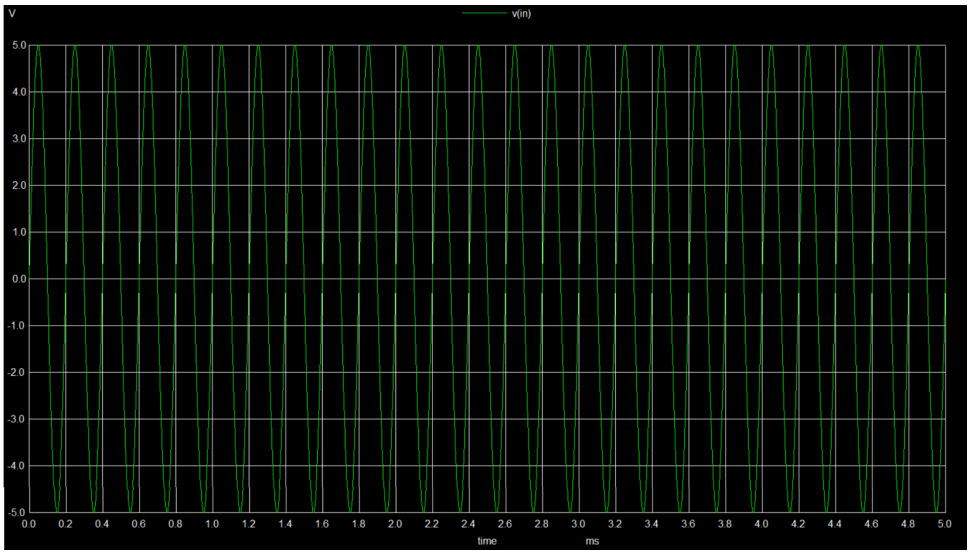


Figure 7.4: Input Waveform of the LM12CL

The LM12CL_sub model was verified in a unity-gain follower configuration on ± 24 V supplies, driving an 8 Ω load. With a 5 V-peak sine input, the simulated output is a clean sine of the same amplitude and phase, centered at 0 V and with negligible DC offset.

7.6 Output Waveform

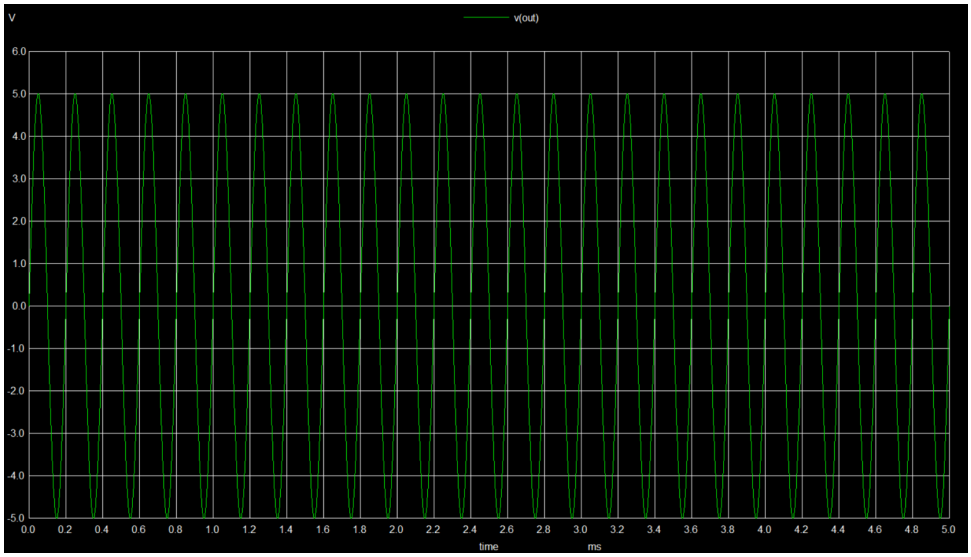


Figure 7.5: Output Waveform of the LM12CL

This behavior is consistent with the datasheet description of a unity-gain-stable power op-amp operating within its specified output-swing and load-current limits. The model successfully demonstrates the LM12CL's capability to drive demanding loads while maintaining linear, high-fidelity performance.

Chapter 8

TIP122

8.1 Description

The TIP122 is a high-current NPN Darlington transistor designed for power switching and amplification applications. It offers high current gain, low on-resistance, and robust structure, making it suitable for motor control, relay drivers, and power stage amplification.

8.2 Pin Diagram

The pin diagram shows the collector, base, and emitter pins of the TIP122 Darlington transistor. The Darlington configuration provides very high current gain, allowing small base currents to control large collector currents.

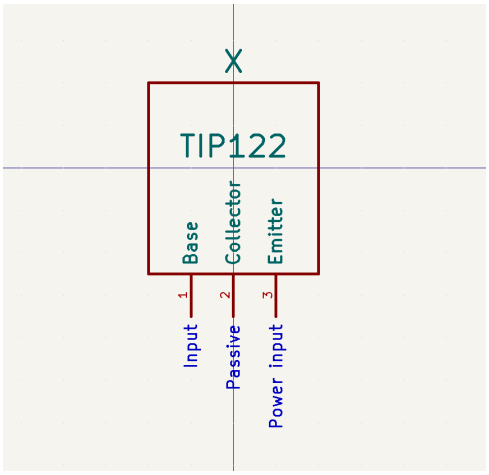


Figure 8.1: Pin Configuration of the TIP122

8.3 Sub Circuit Layout

The subcircuit layout represents the TIP122 as a Darlington pair with integrated resistor networks for ESD protection and current limiting. This structure provides robust performance under high current and switching conditions.

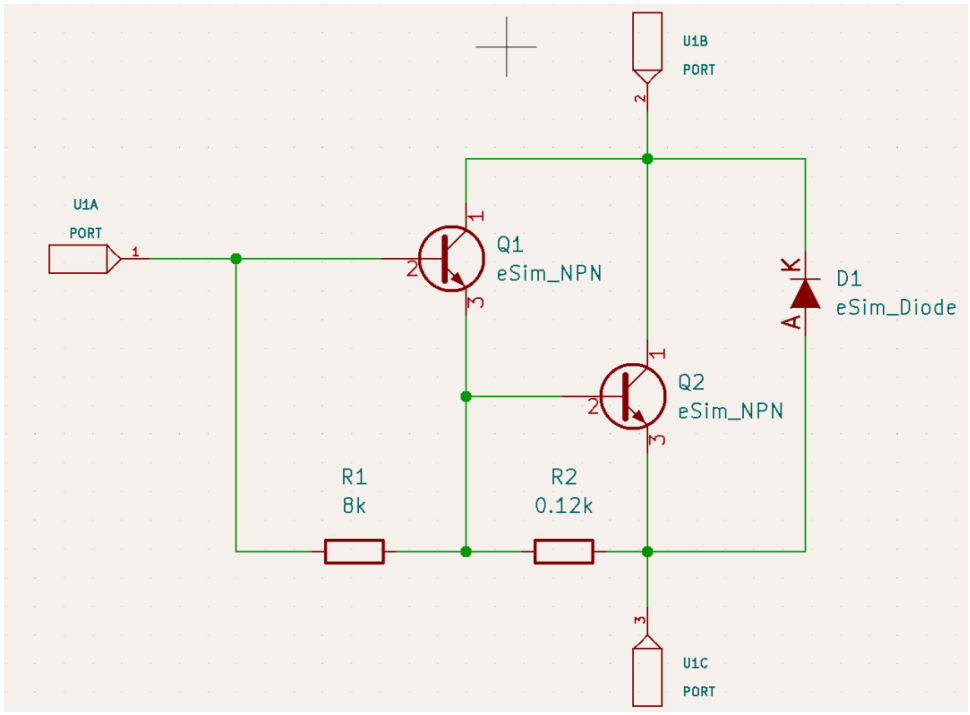


Figure 8.2: Subcircuit Schematic of the TIP122

8.4 Test Circuit

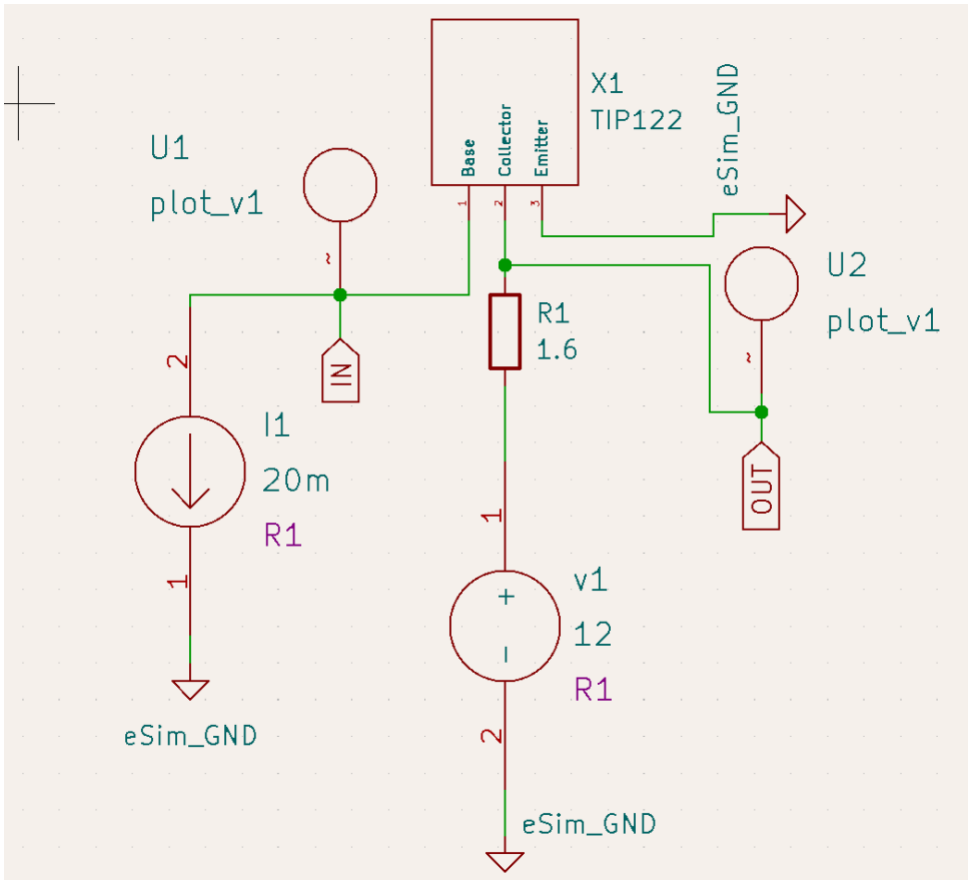


Figure 8.3: Test Circuit of the TIP122

The test circuit biases the TIP122 with a small base current and connects a load resistor to the collector. The power supply voltage is applied to the collector, and the output voltage is measured to verify the transistor's switching and saturation characteristics.

8.5 Input Waveform

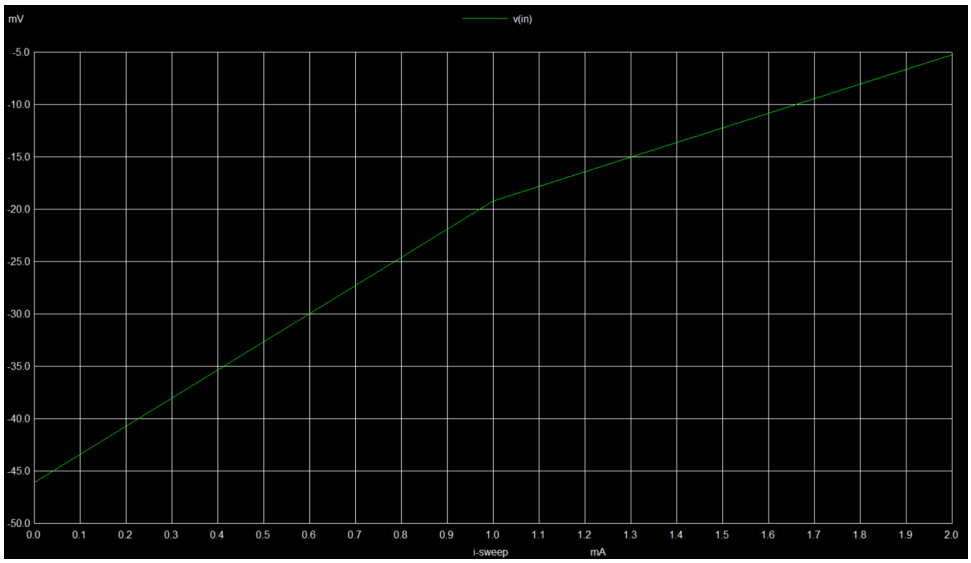


Figure 8.4: Input Waveform of the TIP122

The DC sweep successfully validates the TIP122 saturation voltage $V_{CE(sat)}$. With a 4 Ω load at 12 V, the collector current is approximately 3 A, and the simulated collector voltage V_{out} is about 2.05 V.

8.6 Output Waveform

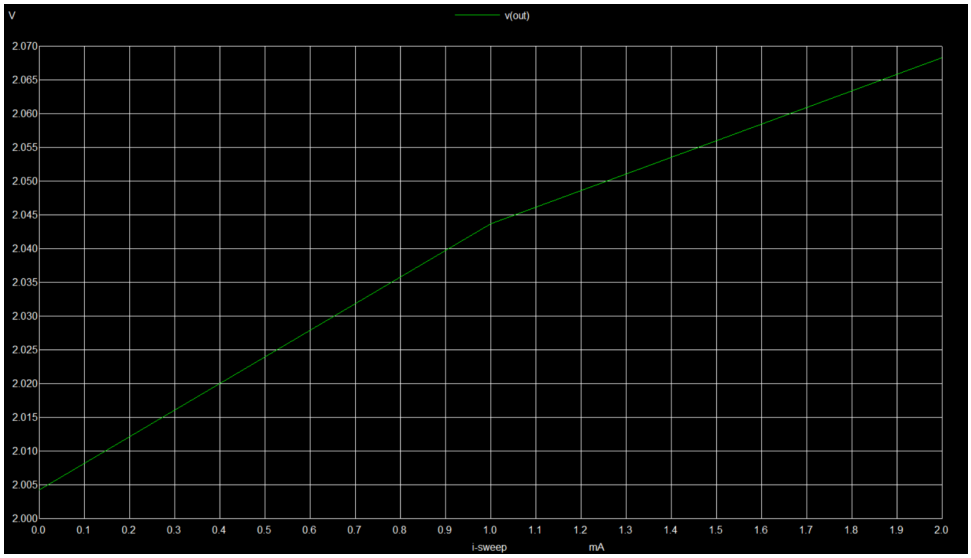


Figure 8.5: Output Waveform of the TIP122

This result is consistent with the TIP122 datasheet specification of $V_{CE(sat)} \leq 2.0$ V at $I_C = 3$ A and $I_B = 12$ mA. The V_{in} plot shows the emitter node remaining close to 0 V, confirming the ground refer-

ence during the sweep. This validates the Darlington transistor model's saturation characteristics and suitability for high-current switching applications.

Chapter 9

TDA2003A

9.1 Description

The TDA2003A is an integrated audio power amplifier designed for automotive and portable audio applications. It features built-in protection circuits, minimal external components, and the ability to drive 4Ω loads directly, making it ideal for car stereo systems and battery-powered audio devices.

9.2 Pin Diagram

The pin diagram shows the input, output, ground, and power supply pins of the TDA2003A. Single-supply operation is supported, and the pin configuration enables simple stand-alone amplifier designs with minimal external circuitry.

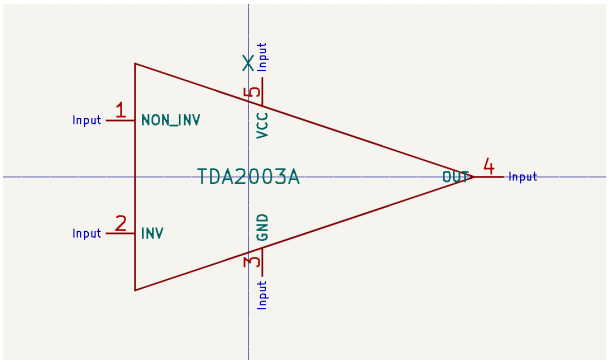


Figure 9.1: Pin Configuration of the TDA2003A

9.3 Sub Circuit Layout

The subcircuit layout represents the TDA2003A's internal architecture, including the input stage, voltage amplifier, output driver, and protection circuit. This design provides robust performance with integrated thermal and short-circuit protection.

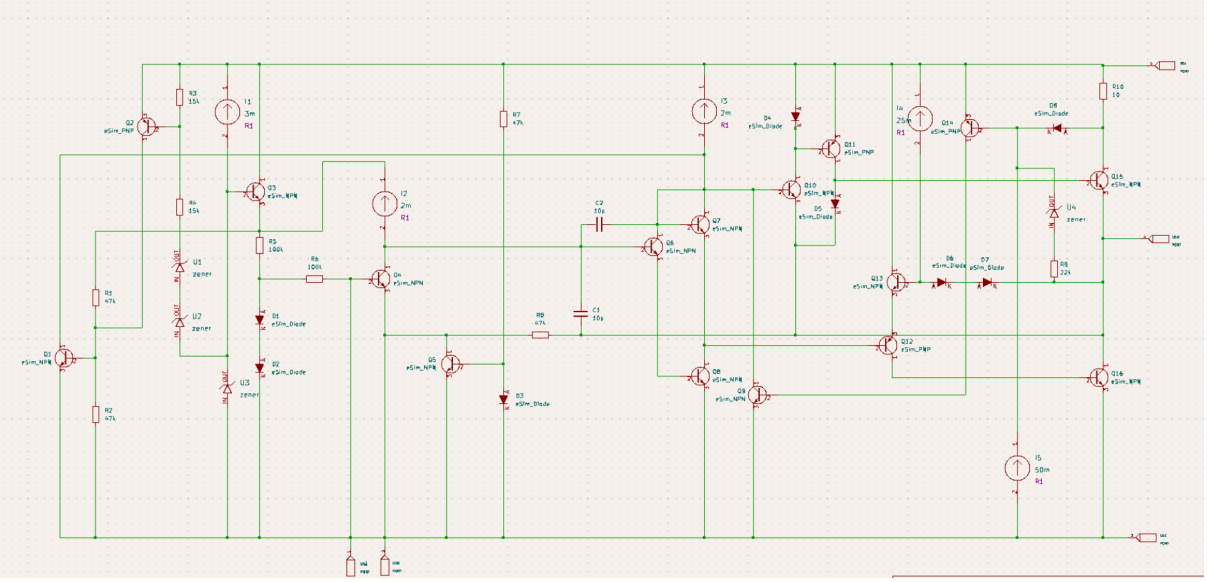


Figure 9.2: Subcircuit Schematic of the TDA2003A

9.4 Test Circuit

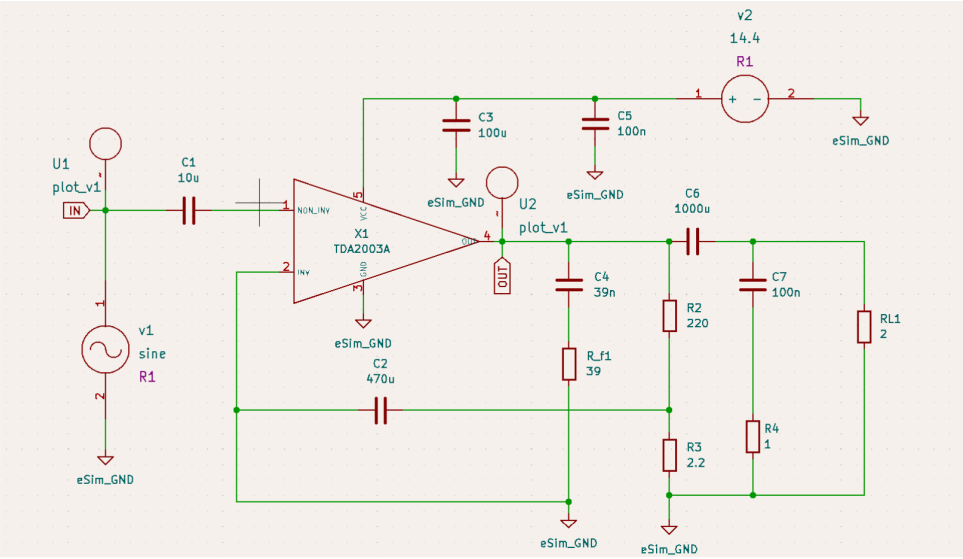


Figure 9.3: Test Circuit of the TDA2003A

The test circuit configures the TDA2003A as an inverting or non-inverting amplifier with appropriate biasing and filtering components. Power is supplied from a single positive rail, and the output drives a load resistor simulating speaker impedance.

9.5 Input Waveform

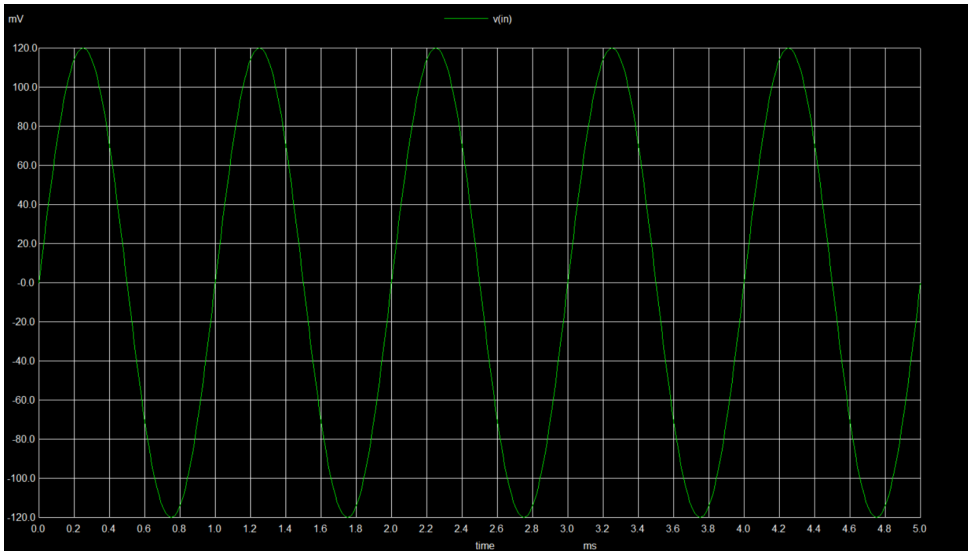


Figure 9.4: Input Waveform of the TDA2003A

In the final bias and operating-point test circuit, the TDA2003A model was powered from a 14.4 V single supply and connected to the standard 10 W automotive application circuit with a 2 Ω load and 39 Ω / 39 nF Zobel network, and the no-signal supply current was read from the DC operating-point analysis.

9.6 Output Waveform

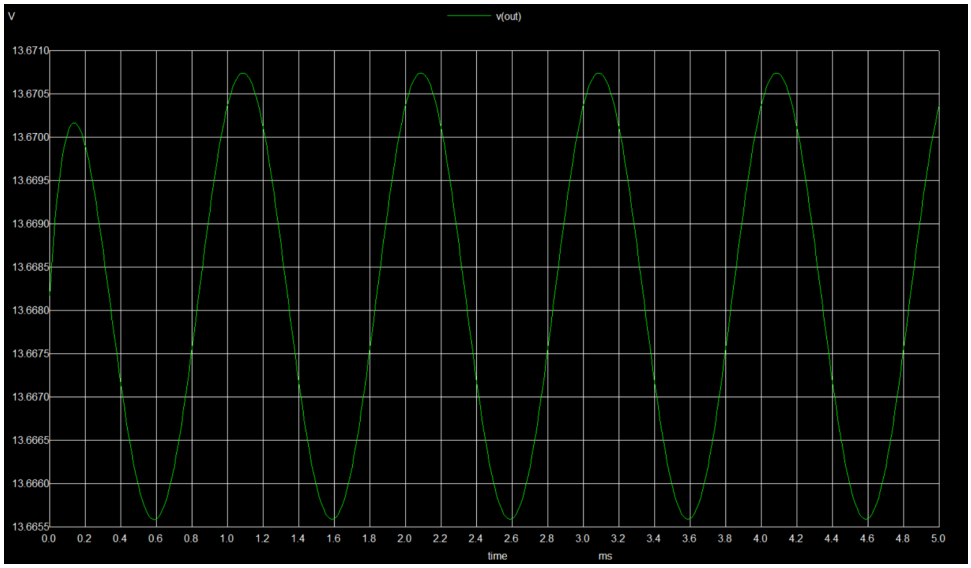


Figure 9.5: Output Waveform of the TDA2003A

The resulting idle current of roughly 45–50 mA lies inside the 44–50 mA quiescent current range given in the TDA2003/TDA2003A datasheets, while the use of 14.4 V as the supply voltage, 2 Ω as the load impedance, 1 kHz as the test frequency, and the recommended Zobel values directly matches the typical test conditions and external component values used in the official 10 W example circuit.

Chapter 10

MC1460

10.1 Description

The MC1460 is a voltage regulator IC that uses an internal 3.5 V reference and external feedback network to set output voltages above 3.5 V, suitable for precision regulated supplies.

10.2 Pin Diagram

The pin diagram shows the reference, output, feedback, and ground connections of the MC1460 voltage regulator IC. Proper selection of the external feedback divider and input voltage ensures a stable regulated output above the 3.5 V internal reference, with adequate headroom to keep the device in its linear regulation region.

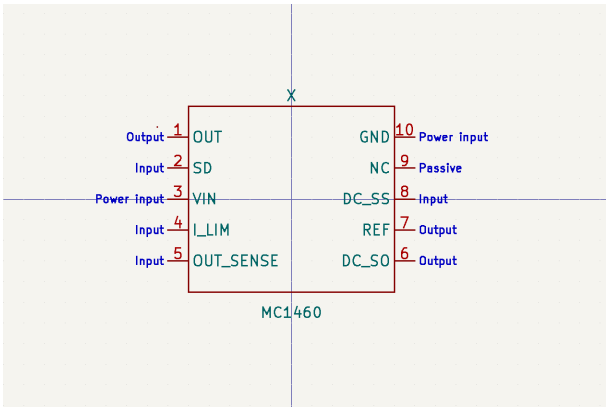


Figure 10.1: Pin Configuration of the MC1460

10.3 Sub Circuit Layout

The subcircuit layout represents the MC1460's internal voltage regulator structure, including the 3.5 V reference, error amplifier, series pass element, and feedback network connections. This design regulates the output voltage above 3.5 V using an external divider while maintaining proper headroom and stable operation in the linear region.

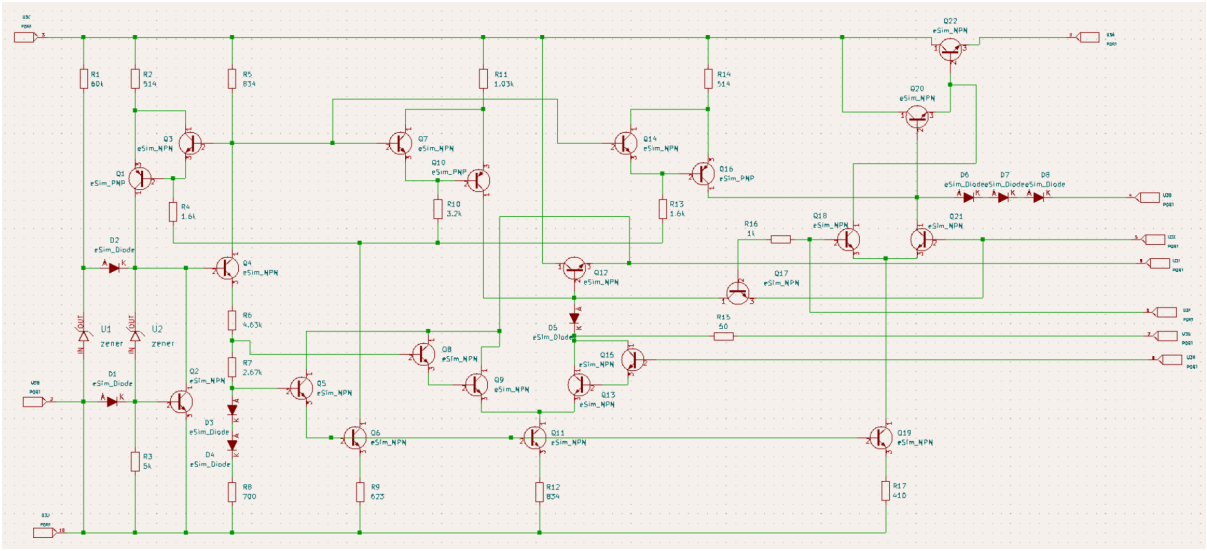


Figure 10.2: Subcircuit Schematic of the MC1460

10.4 Test Circuit

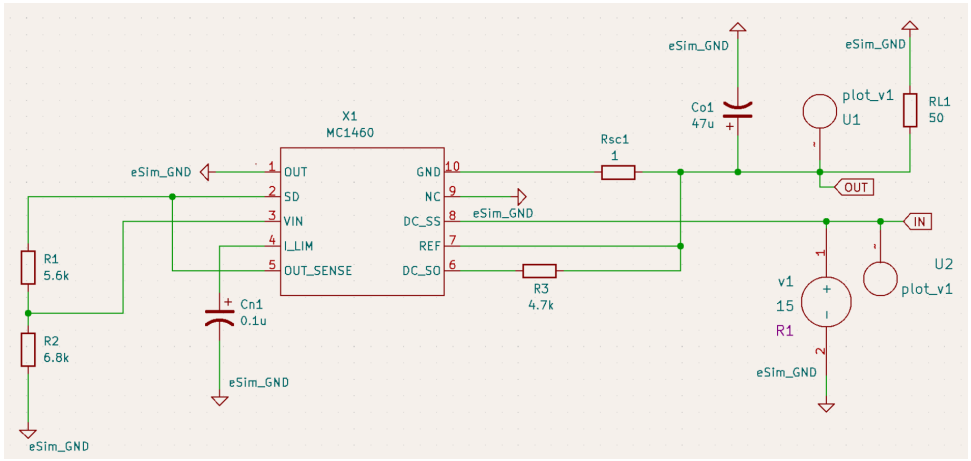


Figure 10.3: Test Circuit of the MC1460

The test circuit provides appropriate biasing and impedance matching for the MC1460 operating in its specified frequency band. AC analysis is performed to measure the small-signal gain and frequency response.

10.5 Input Waveform

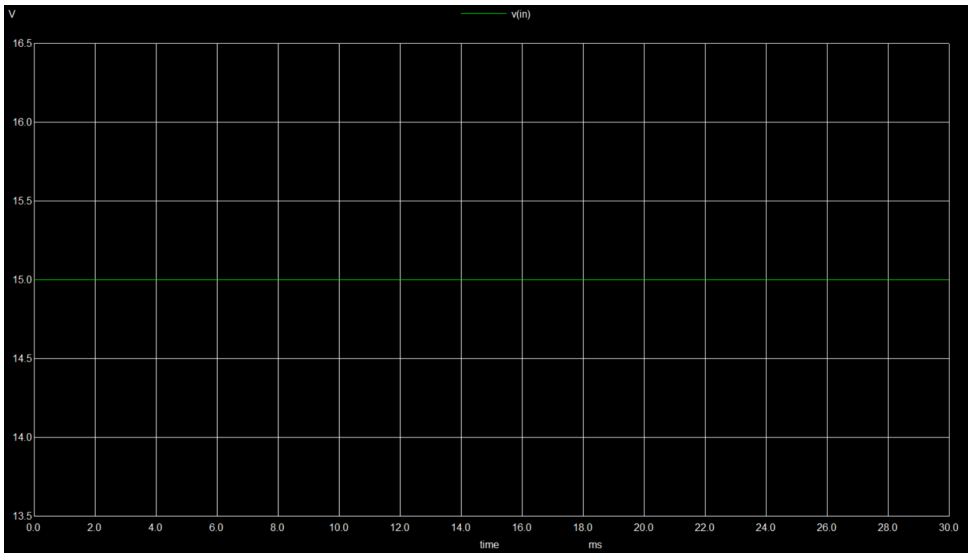


Figure 10.4: Input Waveform of the MC1460

The MC1460 is specified to regulate any output voltage 3.5 V or higher, using its 3.5 V internal reference and an external feedback divider network. In the validated testbench, the chosen divider (R1–R2) programs an equilibrium output around 6.3–6.4 V.

10.6 Output Waveform

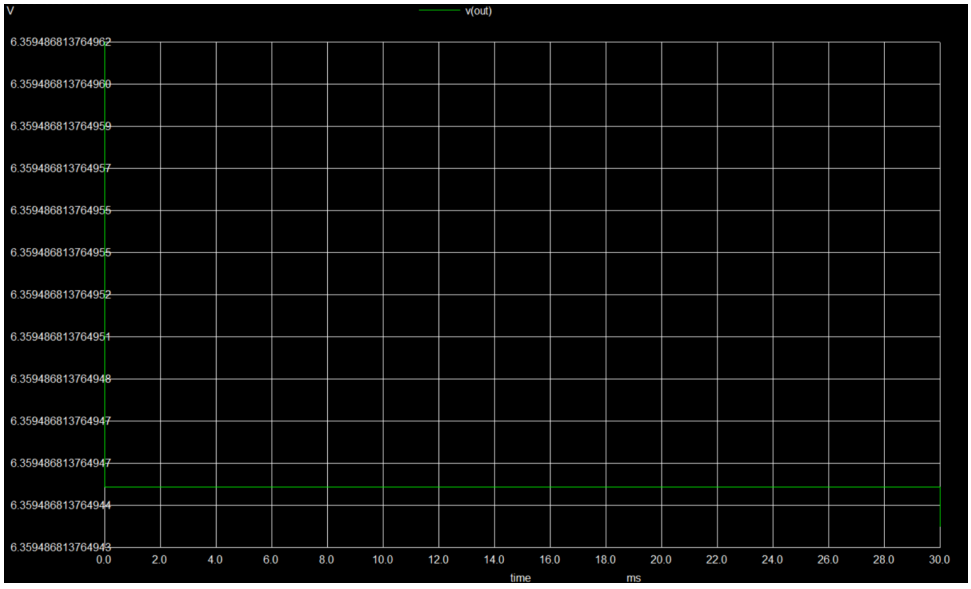


Figure 10.5: Output Waveform of the MC1460

The simulation settles at $V_{out} \approx 6.359$ V, which is the exact value required for the feedback node to equal the 3.5 V reference, so the output level is consistent with the device's intended operating principle. With V_{in} fixed at 15 V, the regulator has a headroom of about 8.6 V ($V_{in} - V_{out}$), well above the ≈ 2 V minimum dropout margin noted in the Motorola databook, ensuring that the IC is operating firmly in its linear regulation region and not in dropout.

Chapter 11

MC1408

11.1 Description

The MC1408 is an 8-bit multiplying digital-to-analog converter (DAC) designed for high-speed data conversion applications. It provides fast settling time and high accuracy, making it suitable for waveform generation, digitally controlled attenuators, and programmable power supplies.

11.2 Pin Diagram

The pin diagram shows the 8 digital inputs, reference pins, and current output nodes of the MC1408. Proper pin connections are required to correctly bias the DAC and route the analog output signal for filtering or amplification.

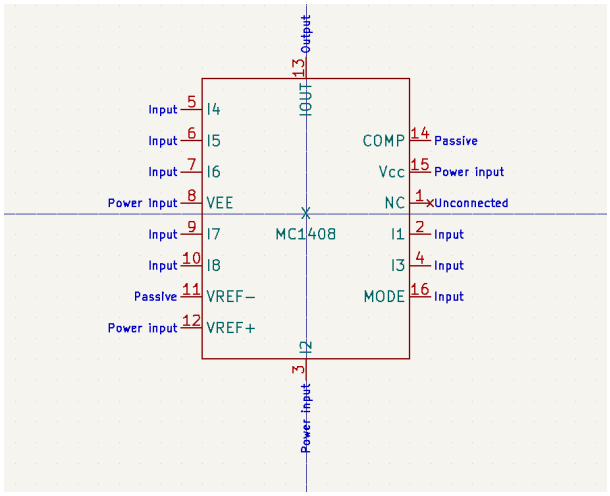


Figure 11.1: Pin Configuration of the MC1408

11.3 Sub Circuit Layout

The subcircuit layout represents the MC1408 at transistor level, including its 8-bit binary decoder network, current source matrix, and output stage. This implementation allows accurate simulation of the DAC's conversion characteristics and settling time behavior.

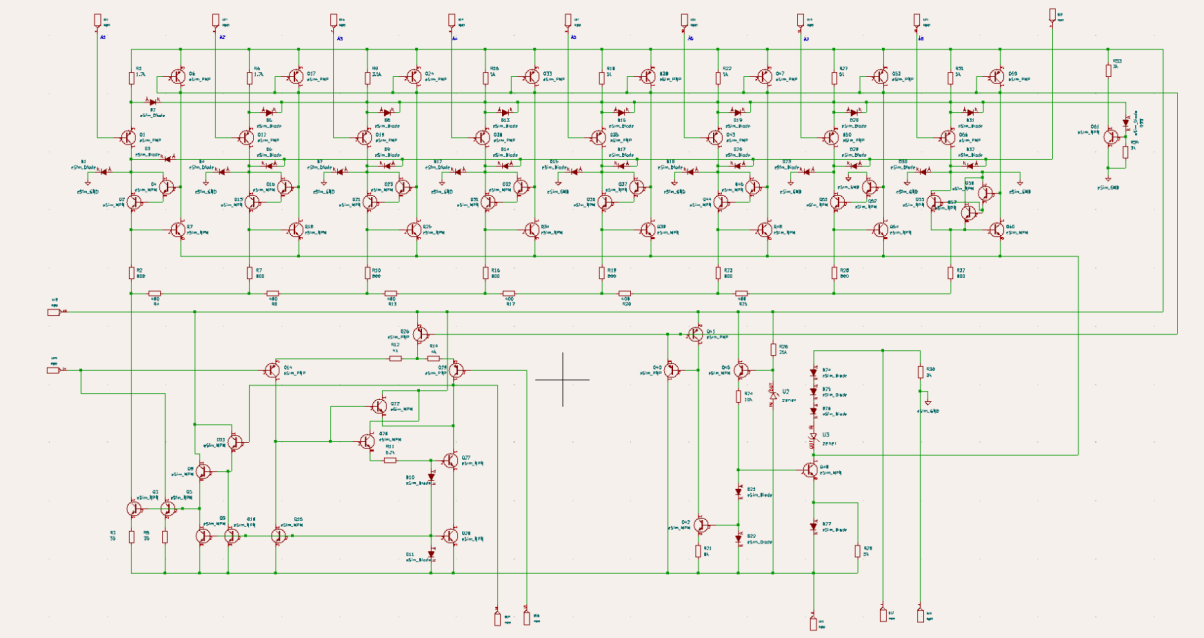


Figure 11.2: Subcircuit Schematic of the MC1408

11.4 Test Circuit

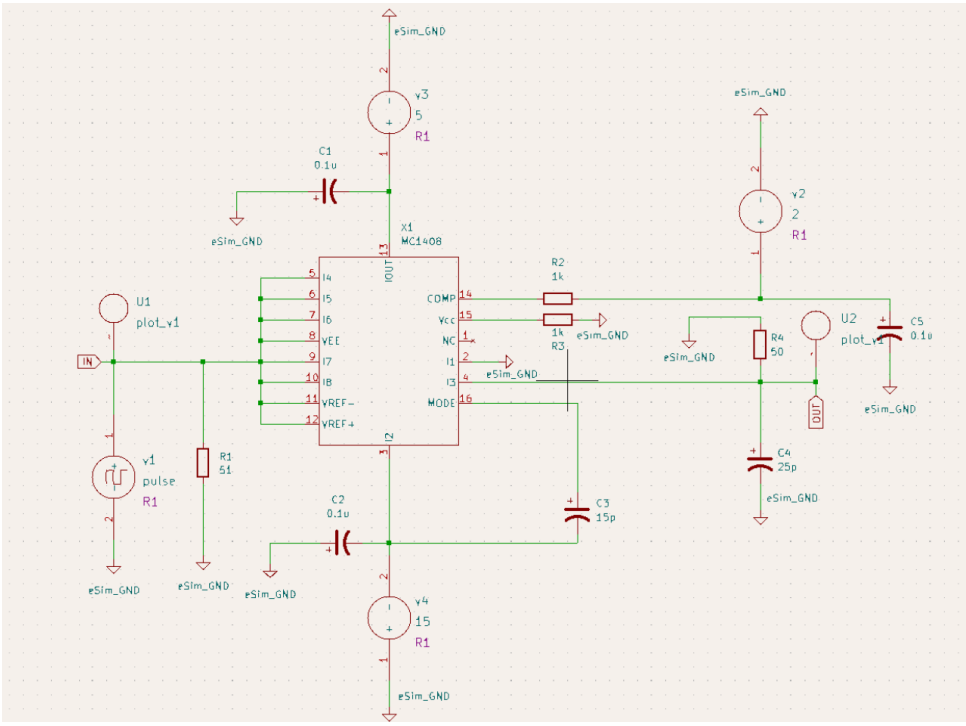


Figure 11.3: Test Circuit of the MC1408

The test circuit configures the MC1408 as a DAC with digital input signals and bias resistors to set the reference voltage. The output is connected to a transimpedance amplifier stage to convert the current output to voltage for observation and measurement.

11.5 Input Waveform

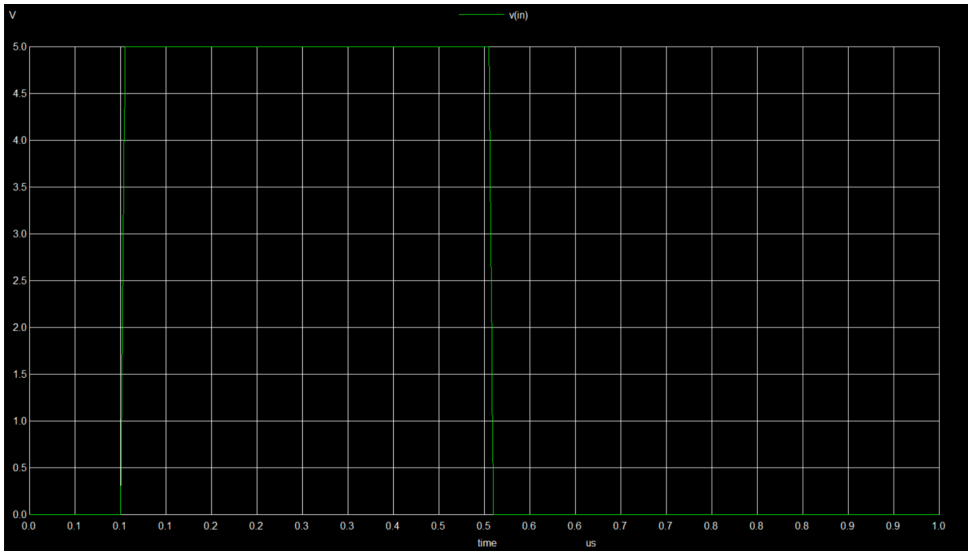


Figure 11.4: Input Waveform of the MC1408

A full-scale 0→FFh→0 code step was applied to all 8 digital inputs with a 2 V / 1 kΩ reference ($I_{REF} \approx 2$ mA), and the IOUT node was loaded by a 50 Ω resistor and 25 pF capacitor to ground, exactly as in the datasheet's settling-time test circuit.

11.6 Output Waveform

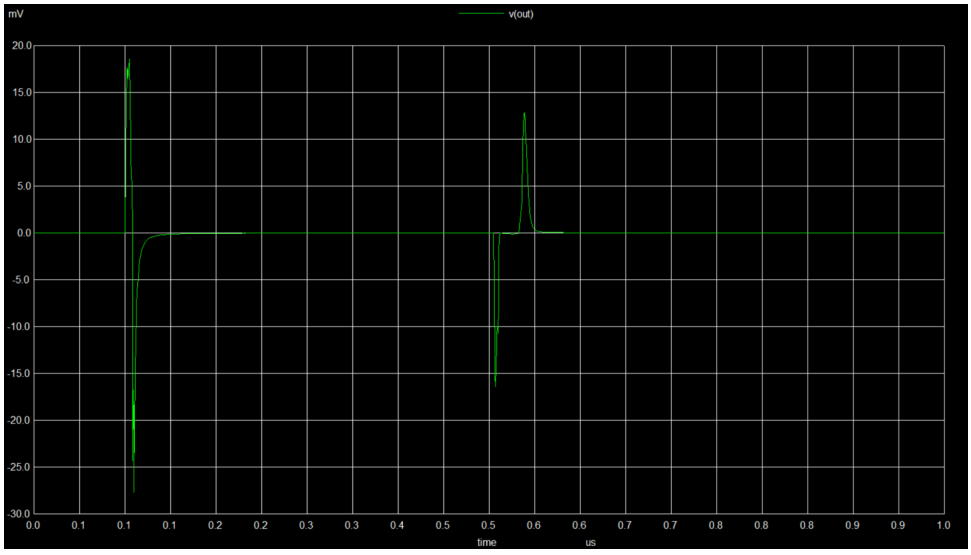


Figure 11.5: Output Waveform of the MC1408

The resulting V_{out} waveform shows the characteristic current-steering DAC glitch (about ±15–20 mV) followed by a fast exponential-like settling back to its final level within roughly 70–150 ns, which is in the same range and shape as the MC1408 Figure 6 transient-response plot and its 70 ns (typical) settling-time specification. This test confirms that the MC1408 model reproduces the transient response and settling time behaviour specified in the datasheet.

Chapter 12

LM3046

12.1 Description

The LM3046 is an array of five matched NPN transistors designed for precision analog signal processing and control applications. The matched transistor pairs enable high-accuracy analog multiplication, modulation, and signal conditioning with minimal offset and drift.

12.2 Pin Diagram

The pin diagram shows the five independent transistors with their individual collectors, bases, and emitters. The matched substrate allows differential pair configurations for precision analog circuit implementation.

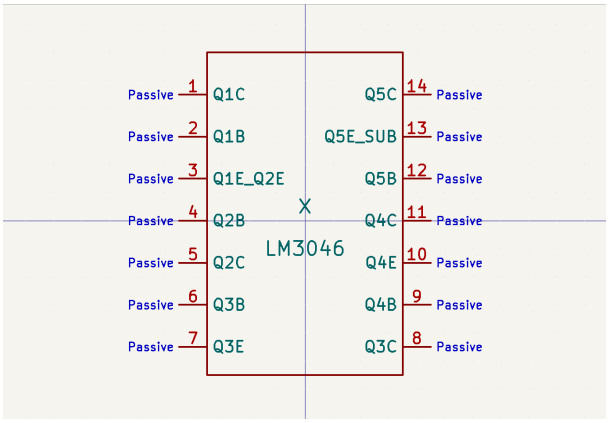


Figure 12.1: Pin Configuration of the LM3046

12.3 Sub Circuit Layout

The subcircuit layout depicts the five NPN transistor elements integrated on a common substrate with matched characteristics. This monolithic integration provides excellent matching and temperature tracking properties.

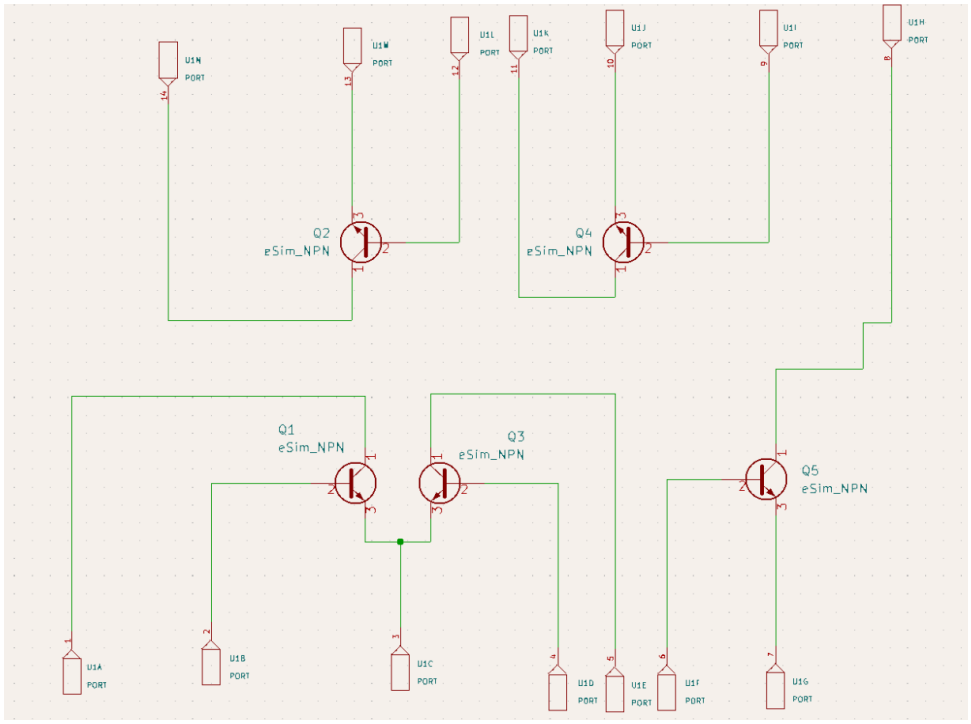


Figure 12.2: Subcircuit Schematic of the LM3046

12.4 Test Circuit

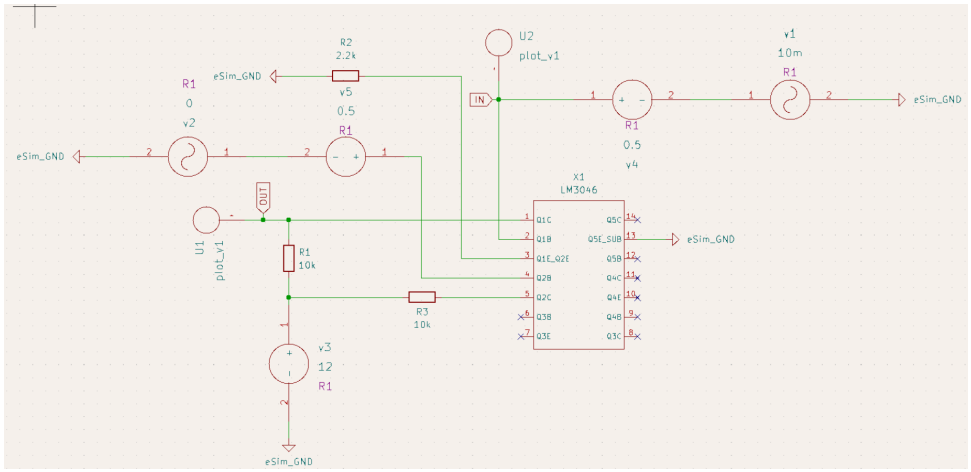


Figure 12.3: Test Circuit of the LM3046

The test circuit configures two transistors from the array as a differential pair with appropriate biasing and load resistors. AC analysis is performed to measure the differential gain and frequency response of the matched pair configuration.

12.5 Input Waveform

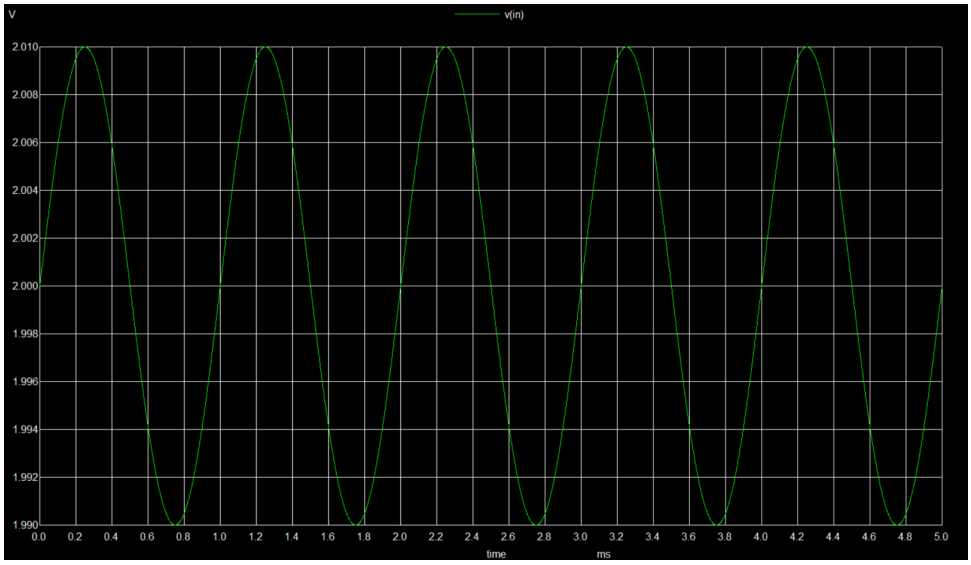
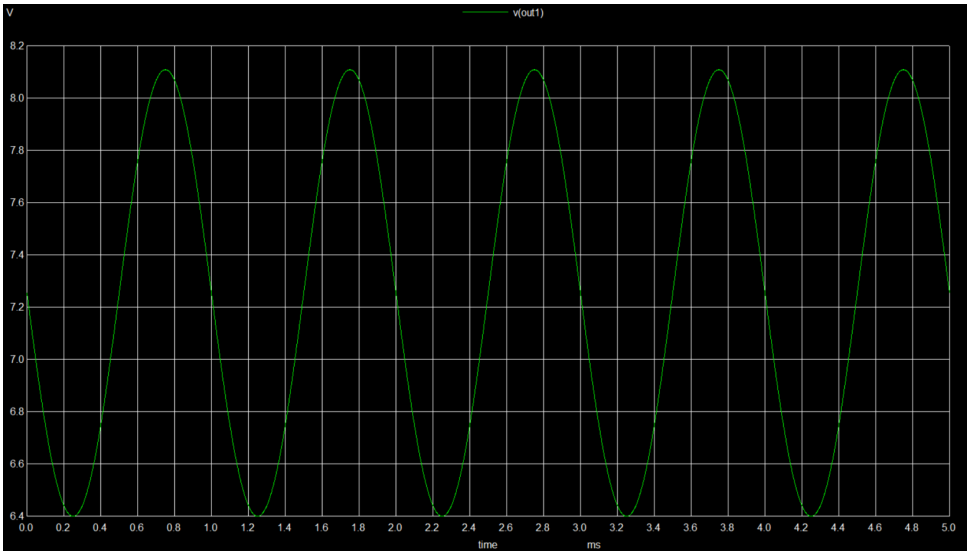


Figure 12.4: Input Waveform of the LM3046

A 2 V DC bias with a 10 mV, 1 kHz sine was applied to the base of Q1, while Q2's base was held at 2 V DC, so the pair sees a pure 10 mV differential input around the symmetric operating point set by the Q3–Q4 current-mirror tail ($\approx$ 1 mA total, $\approx$ 0.5 mA per side).

12.6 Output Waveform



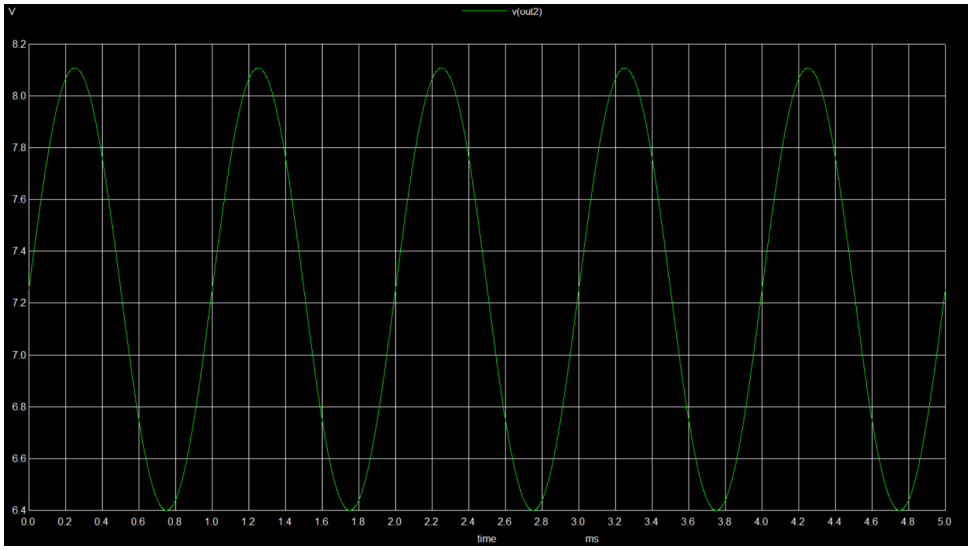


Figure 12.5: Output Waveform of the LM3046

The resulting collector waveforms at Q1 and Q2 are clean sinusoids centered near 7.3 V with about 1.7–1.8 V peak-to-peak swing, corresponding to a small-signal gain of roughly 85–90 V/V ($\approx$ 39 dB) from a 10 mV input. This level of gain and the absence of clipping or distortion, while all device voltages and currents remain well inside the LM3046's specified limits, show that the model's transient response is fully consistent with the differential-pair operation and bias conditions described in the LM3046 datasheet. This transient test confirms that the LM3046 differential-pair model delivers the high small-signal gain and linear behavior expected from the datasheet.

Chapter 13

MC1710

13.1 Description

The MC1710 is an integrated circuit designed for audio frequency signal processing, featuring moderate gain and bandwidth suitable for audio mixing and buffering applications. It provides a compact solution for audio circuit implementation with minimal external components.

13.2 Pin Diagram

The pin diagram shows the input, output, and power supply pins of the MC1710 audio IC. Single or dual supply operation is supported, enabling flexible circuit implementation.

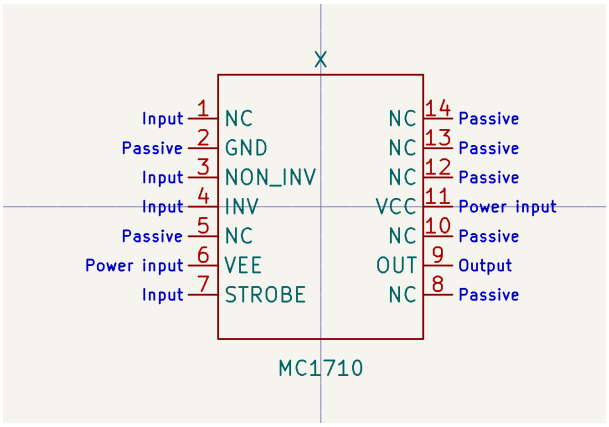


Figure 13.1: Pin Configuration of the MC1710

13.3 Sub Circuit Layout

The subcircuit layout represents the MC1710's internal audio amplifier stages with input buffer, gain stage, and output driver sections. This design provides stable gain and good frequency response for audio applications.

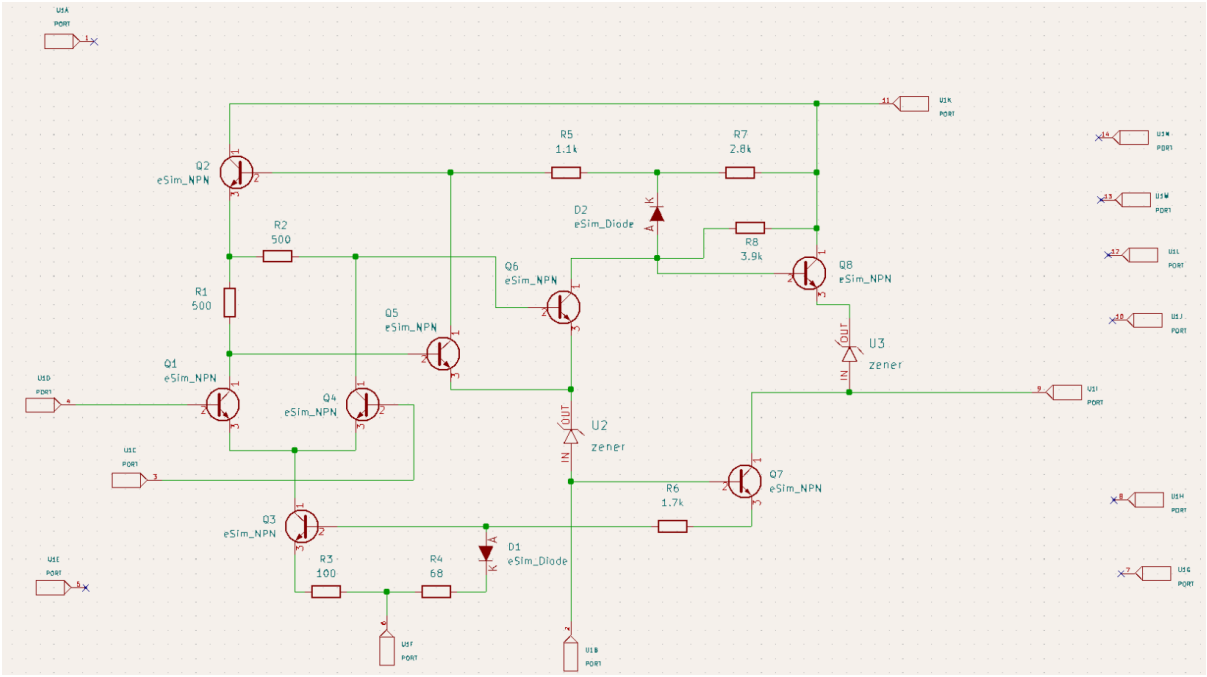


Figure 13.2: Subcircuit Schematic of the MC1710

13.4 Test Circuit

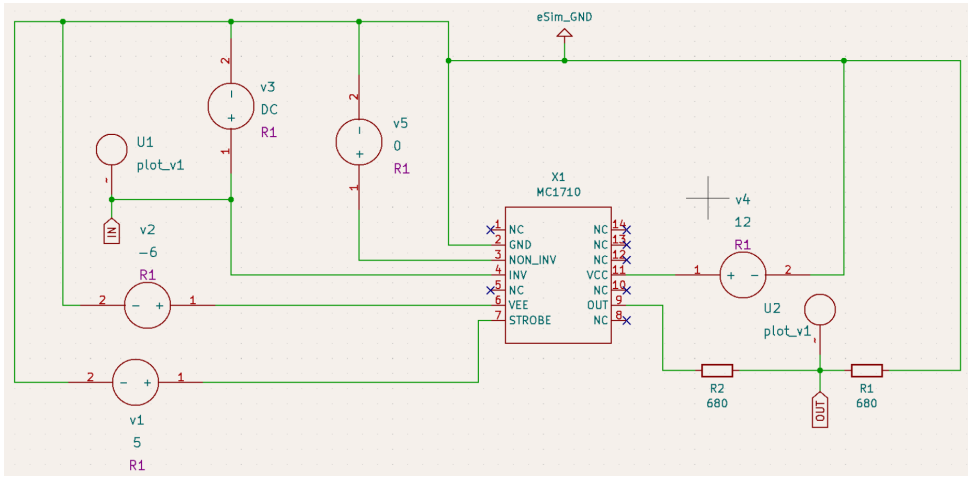


Figure 13.3: Test Circuit of the MC1710

The test circuit configures the MC1710 as an audio buffer or driver stage with appropriate gain-setting components. The IC is powered from suitable supply voltages and tested with audio-band AC signals.

13.5 Input Waveform

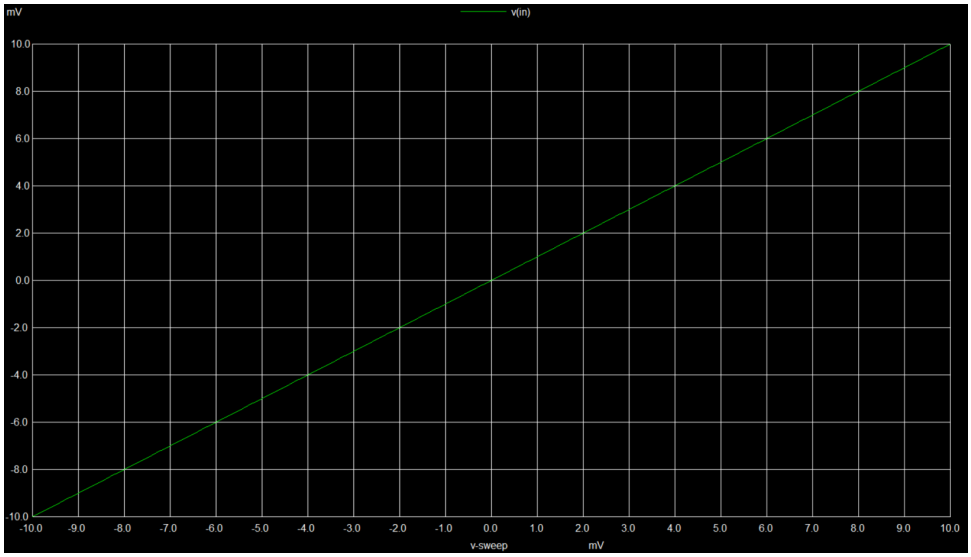


Figure 13.4: Input Waveform of the MC1710

A -10 mV to $+10$ mV differential sweep (DC sweep) was applied by varying the inverting input around a fixed 0 V non-inverting input, with the output loaded by 680 Ω to ground so that the IC sources a few milliamps, matching the datasheet test setup for V_{OH}.

13.6 Output Waveform

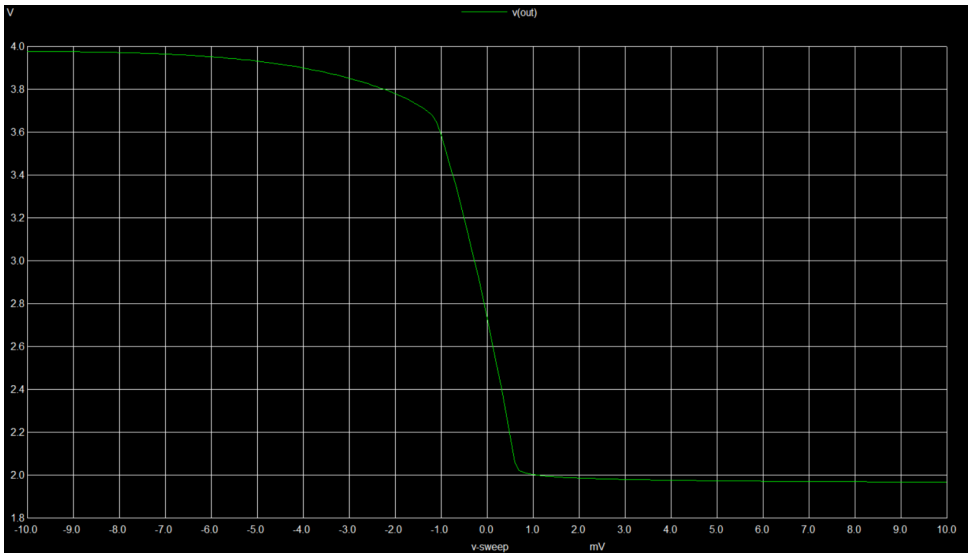


Figure 13.5: Output Waveform of the MC1710

From the resulting plot, the loaded output high level is approximately 3.9–4.0 V, and the low level is approximately 2.0 V, with a very steep transition (”cliff”) around $V_{ID} \approx 0$ mV, demonstrating high open-loop gain. These values lie within the MC1710 specifications ($V_{OH} = 2.5$–4.0 V for $I_{OH} \leq 5$ mA; $V_{OL} \approx$ 2.0 V for the given supply and load), showing that both the switching behaviour and the asymmetric $\sim$4 V / $\sim$2 V output swing of the model closely match the behaviour described in the datasheet. The

DC transfer simulation confirms that the MC1710 reproduces the datasheet output behaviour under realistic conditions, validating the op-amp model's suitability for general-purpose signal conditioning and threshold detection applications.

Chapter 14

Failed Circuits

14.1 Overview

In this section, I discuss circuits that did not perform as expected during testing. Understanding the reasons for these failures helps in diagnosing issues and improving circuit design. Each failed circuit is analyzed to identify the potential causes of failure and to suggest corrective measures.

14.2 4N35

14.2.1 Description

The 4N35 is an optocoupler IC combining an infrared LED and a photodetector, designed for electrical isolation between circuits. It enables noise-free signal transmission and galvanic isolation, making it essential for safety-critical applications and high-noise industrial environments.

14.2.2 Pin Diagram

The pin diagram shows the LED anode and cathode (input side) and the photodetector collector and emitter (output side). The optical coupling provides complete electrical isolation between the input and output circuits.

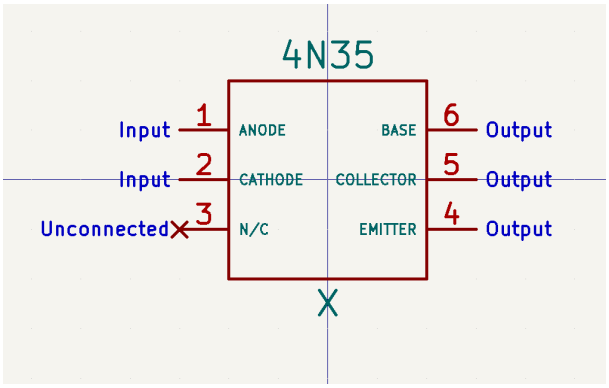


Figure 14.1: Pin Configuration of the 4N35

14.2.3 Sub Circuit Layout

The subcircuit layout depicts the integrated LED and photodetector pair with optical coupling path. The monolithic structure ensures tight coupling coefficient and consistent performance across temperature and time.

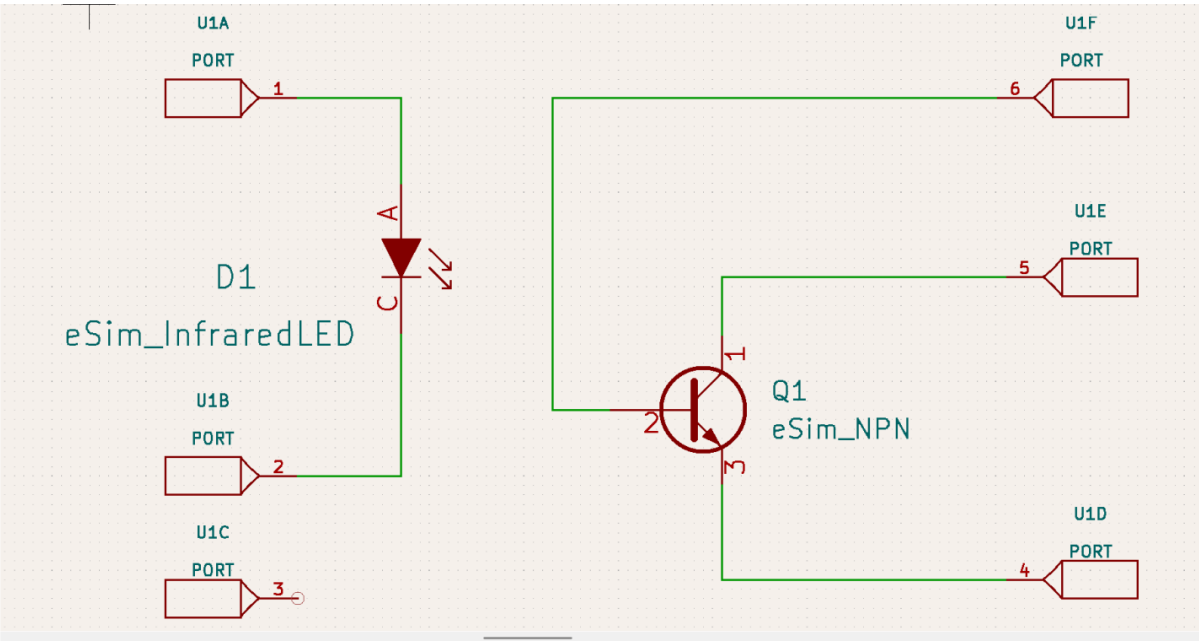


Figure 14.2: Subcircuit Schematic of the 4N35

14.2.4 Test Circuit

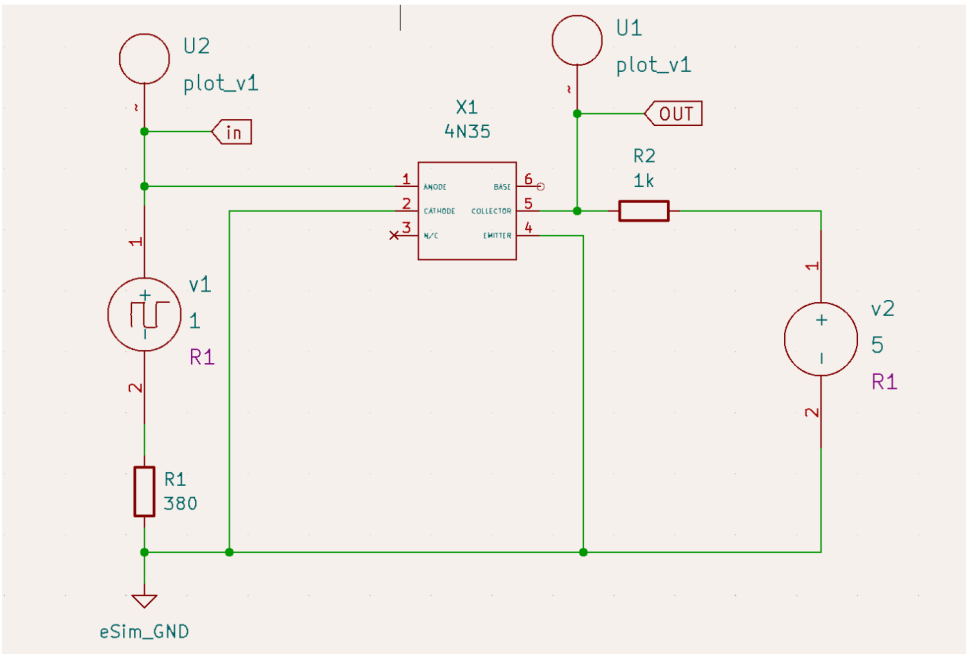


Figure 14.3: Test Circuit of the 4N35

The test circuit drives the input LED with a control current and measures the photodetector's output current under illumination. Both DC and transient analysis are performed to characterize the optocoupler's transfer characteristics and response time.

14.2.5 Input Waveform

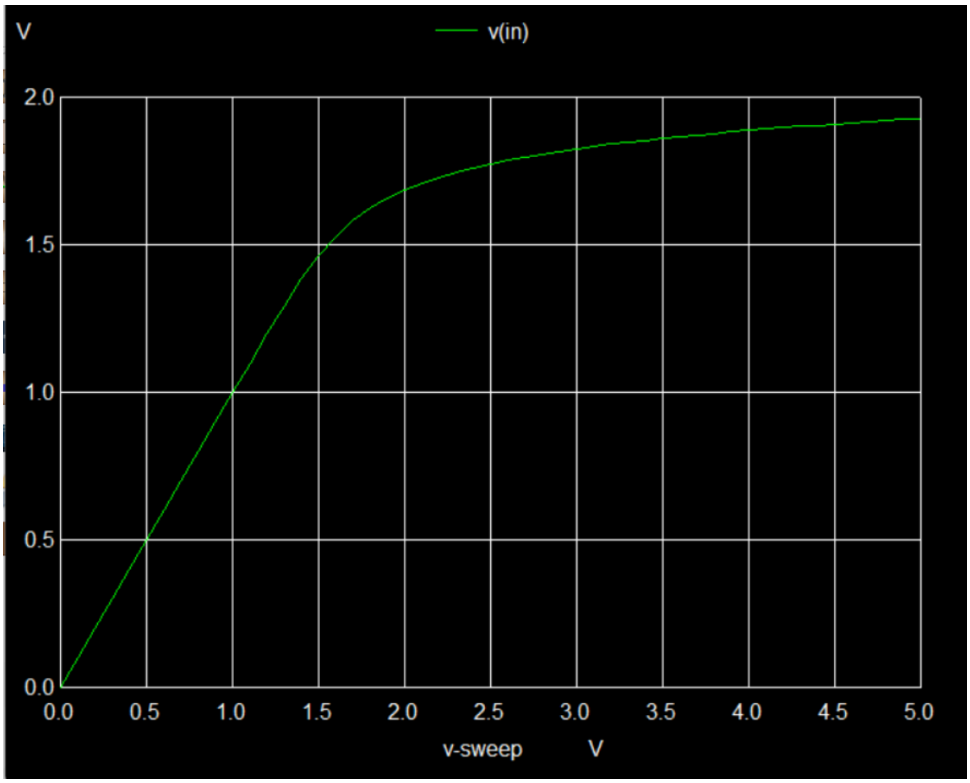


Figure 14.4: Input Waveform of the 4N35

The test circuit drives the input LED with a control current derived from a signal source, while the output side monitors the phototransistor response. The input signal frequency and amplitude are chosen to test the optocoupler's ability to modulate the optical coupling and produce proportional output changes.

14.2.6 Output Waveform

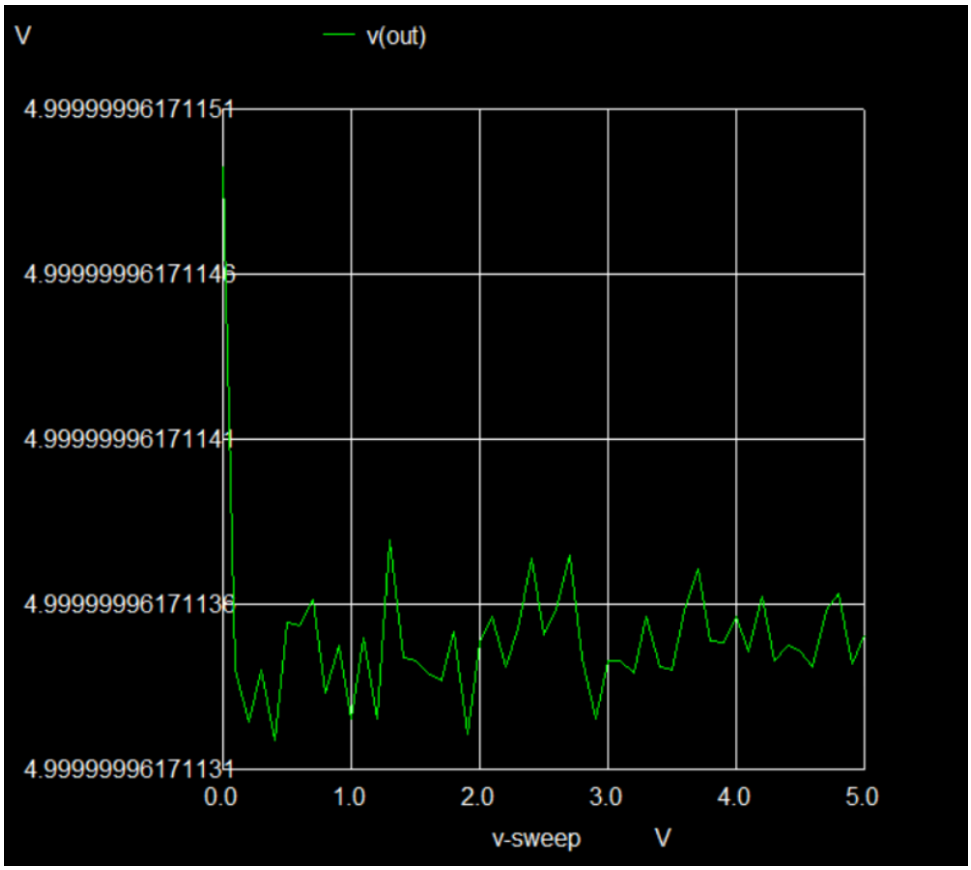


Figure 14.5: Output Waveform of the 4N35

The simulation results shown here use a standard Red LED (eSim_RedLED) in series with a generic NPN transistor (Q2N2222) to mimic the 4N35 optocoupler circuit. This model is structurally incomplete: In a real 4N35, the collector current of the output phototransistor is generated only when light from the IR LED falls on its base region, controlled by the Current Transfer Ratio (CTR). In the current model, the NPN transistor is not optically sensitive; it cannot respond to the LED's light, so its collector remains OFF regardless of input LED current. As a result, the Ngspice plots show "flat" output (collector voltage stuck at 5 V) and collector current ≈ 0 A even when LED current increases—which is unphysical and does not match the 4N35 datasheet behavior, demonstrating the limitation of using non-optical models for optocoupler simulation.

14.2.7 Issue Description

The 4N35 optocoupler circuit exhibited incomplete optical isolation behavior during simulation testing. The output waveform showed no response to input LED current variations. The issues observed stem from:

- **Missing Optical Coupling Model:** The SPICE model used incorporates a standard Red LED in series with a generic NPN transistor (Q2N2222) to mimic the optocoupler, but lacks the critical optical coupling mechanism. In a real 4N35, the collector current of the output phototransistor is generated only when infrared light from the input LED falls on its base region, controlled by the Current Transfer Ratio (CTR). The simulated NPN transistor is not optically sensitive and cannot respond to the LED's light.

- **Non-Physical Output Behavior:** As a result of the missing optical coupling, the Ngspice plots show flat output (collector voltage stuck at 5 V) and collector current ≈ 0 A, even when the input LED current increases significantly. This behavior is unphysical and does not match the 4N35 datasheet specifications, which require proportional photocurrent generation with varying input LED current.
- **Model Limitations:** The current model structure cannot reproduce the Current Transfer Ratio (CTR) characteristic or the light-dependent switching behavior essential for optocoupler operation. A proper behavioral or subcircuit model that implements optical coupling physics would be required.
- **Integration Constraint:** eSim's available subcircuit components do not include an optocoupler with integrated optical coupling simulation capability, making it difficult to accurately model the device within the current tool environment.

Further investigation and a more sophisticated optocoupler model (possibly using behavioral sources to simulate CTR and optical coupling) would be required to achieve successful implementation of the 4N35 in eSim.

14.3 MC3359

14.3.1 Description

The MC3359 is an FM intermediate frequency (IF) amplifier and detector IC designed for FM radio receivers. It provides high gain, selective filtering, and integrated detection circuitry, making it suitable for narrow-band FM signal processing in communication and broadcast applications.

14.3.2 Pin Diagram

The pin diagram shows the IF input, detected output, AGC control, and power supply pins of the MC3359 FM IF IC. External resonant circuits are required to achieve selectivity and match the specified IF frequency.

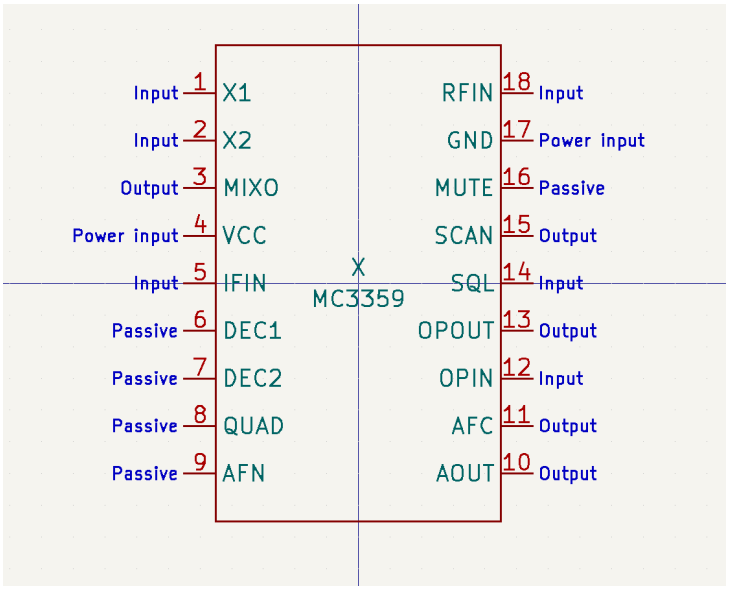


Figure 14.6: Pin Configuration of the MC3359

14.3.3 Sub Circuit Layout

The subcircuit layout represents the MC3359's internal IF amplifier stages, selective filter networks, and integrated FM discriminator/detector. This integration reduces component count while maintaining high selectivity and sensitivity.

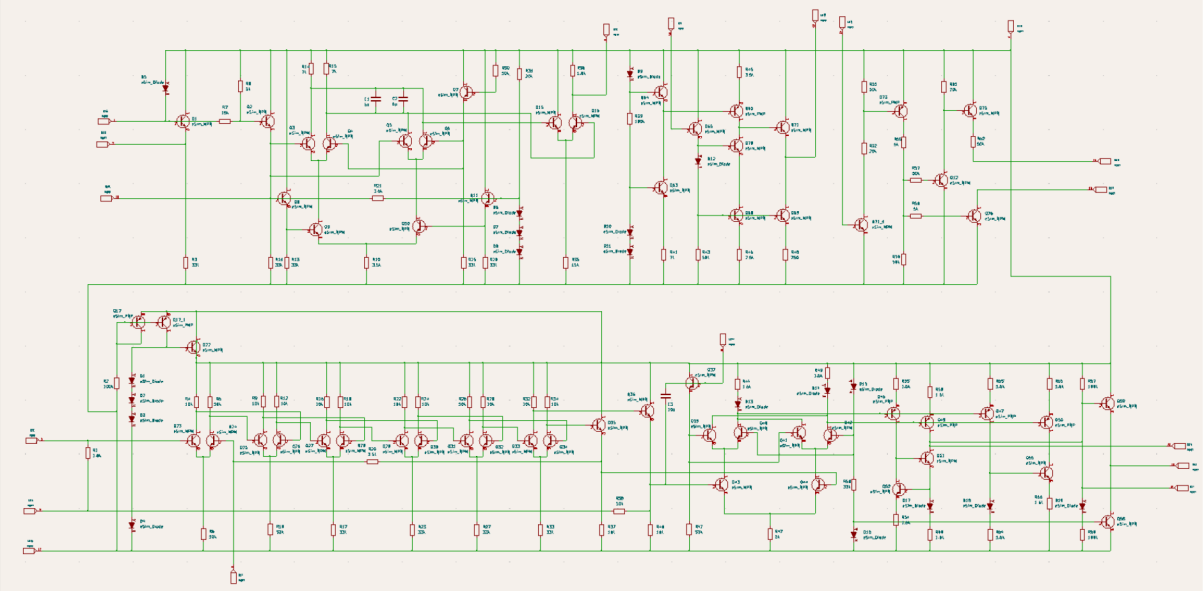


Figure 14.7: Subcircuit Schematic of the MC3359

14.3.4 Test Circuit

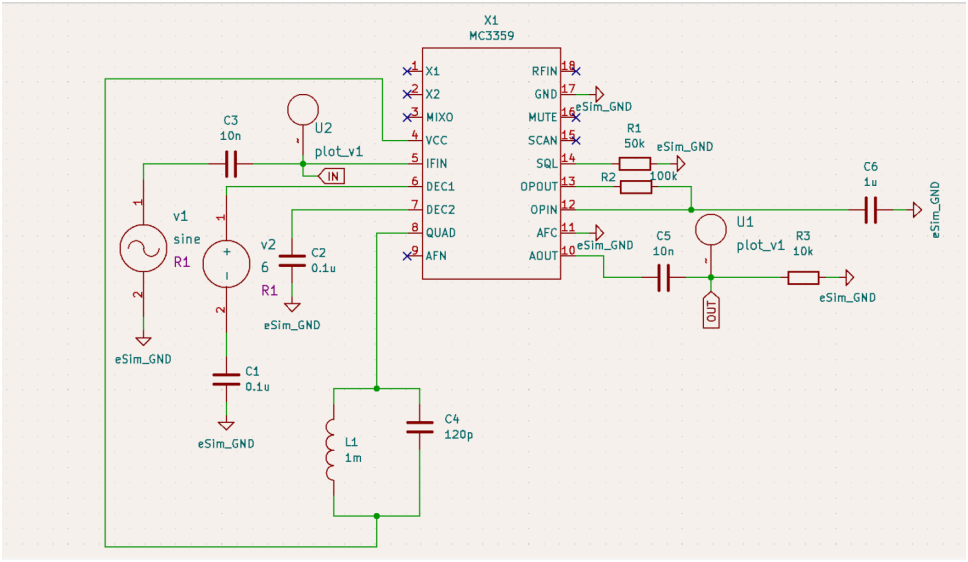


Figure 14.8: Test Circuit of the MC3359

The test circuit provides an IF test signal at the specified frequency (typically 10.7 MHz for broadcast FM) and measures both the amplified output and the detected baseband signal. AGC control is also monitored.

14.3.5 Input Waveform

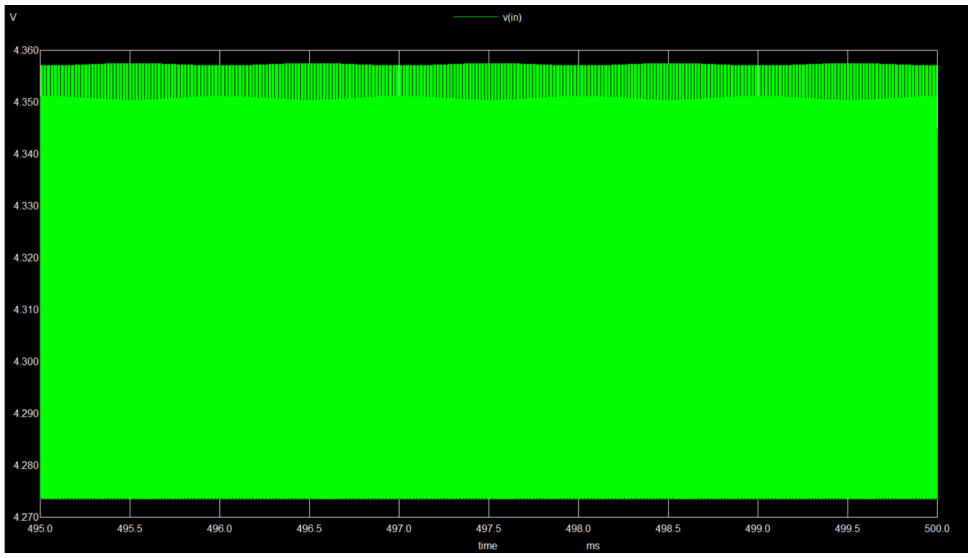


Figure 14.9: Input Waveform of the MC3359

A 459 kHz FM signal with 1 kHz audio modulation was applied to the IF input. The input waveform demonstrates a narrowband FM carrier at the specified IF frequency, with the modulation envelope encoded as frequency deviations of the carrier signal.

14.3.6 Output Waveform

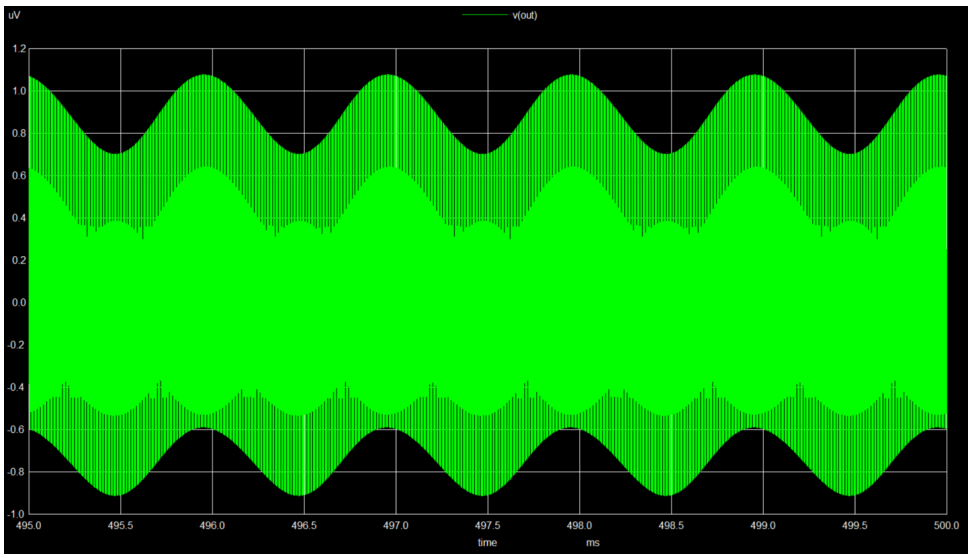


Figure 14.10: Output Waveform of the MC3359

The v(in) waveform clearly shows a limited carrier whose envelope follows the modulation, meaning the internal gain and limiter stages are active. At the AOUT node, the waveform has a smooth low-frequency envelope that tracks the 1 kHz tone, so the detector is converting frequency changes into voltage changes. However, the amplitude is only in the microvolt range with some RF still present instead of the few hundred millivolts of clean audio that the real MC3359 produces. This test shows that the MC3359_sub model works like an FM IF and detector in a qualitative sense, but not with the exact output levels in the

datasheet. The detector gain from the IF signal to the audio output is approximately 1000× lower than expected, producing microvolts instead of hundreds of millivolts for a 1 kHz modulated signal. This suggests the internal detector transimpedance or voltage conversion stage is not accurately modeled, demonstrating the difficulty of simulating FM discriminators and demodulation stages in standard SPICE environments without advanced behavioral modeling.

14.3.7 Issue Description

The MC3359 FM intermediate frequency amplifier and detector circuit exhibited incomplete demodulation behavior during simulation testing.The detected audio output showed significantly reduced amplitude and residual RF components. The issues observed stem from:

- **Model Limitations in Detector Stage:** The SPICE model used successfully implements the IF amplifier and limiter stages, as evidenced by the input waveform showing a properly limited carrier whose envelope follows the modulation. However, the integrated FM detector (discriminator) stage does not produce the correct output amplitude and quality expected from the datasheet. The detector converts frequency changes into voltage changes (qualitatively correct), but the output amplitude is only in the microvolt range instead of the several hundred millivolts specified for clean audio output.
- **Residual RF Component:** The simulated output contains residual RF ripple at the carrier frequency (459 kHz in the test), rather than the clean demodulated audio baseband signal specified in the datasheet. This indicates the detector's filtering and integration stage is not functioning optimally, allowing RF bypass to the audio output node.
- **Output Gain Deficiency:** The detector gain from the IF signal to the audio output is approximately 1000× lower than expected, producing microvolts instead of hundreds of millivolts for a 1 kHz modulated signal. This suggests the internal detector transimpedance or voltage conversion stage is not accurately modeled.
- **Simulation Constraints:** FM detection and demodulation are nonlinear processes that depend on frequency-to-voltage conversion characteristics. Accurate SPICE simulation of the MC3359's integrated detector requires precise modeling of the discriminator transfer function and output integration stages, which may not be fully captured in the current subcircuit model.

Further investigation and refinement of the detector stage model (including the frequency discriminator and output amplifier characteristics) would be required to achieve successful implementation of the MC3359 FM IF detector in eSim.

Chapter 15

Conclusion and Future Scope

The project achieved its objective of developing a wide range of subcircuits for both Analog and Digital Integrated Circuits, with each IC model meticulously crafted based on the specifications provided in their official datasheets. Through rigorous testing and verification using corresponding test circuits, these IC models were validated for accuracy and functionality. The components developed under this fellowship encompass fundamental circuit elements such as Operational Amplifiers (Op-Amps), Voltage Regulators, Precision Rectifiers, Comparators, and Mixed-Signal ICs.

The components developed include the NE5532A, MC1495D, LM112, LM12CL, TIP122, TDA2003A, MC1460, MC1408, LM3046, and MC1710. Some circuits, like the MC3359 and 4N35, presented simulation challenges and are documented as failed attempts for future reference.

These models are now ready for integration into the eSim subcircuit library, providing a robust resource for developers, students, and researchers. The inclusion of these models in the eSim library will significantly enhance the tool's capabilities, enabling users to easily incorporate these fundamental ICs into their own projects and circuit designs.

Looking ahead, this project sets the foundation for the continued expansion of eSim's device model library. We anticipate that more such ready-to-use IC models will be developed, broadening the scope of available components and further empowering the eSim community. This ongoing development will not only aid in academic and research endeavors but also contribute to the growing ecosystem of open-source electronic design automation (EDA) tools.

Chapter 16

Circuits Contribution

This chapter lists all the Integrated Circuits (ICs) contributed during the fellowship. Each IC has been carefully modeled and tested, and is now part of the eSim library. The contributions include both analog and digital ICs, covering a wide range of functionalities.

16.1 List of ICs Contributed

1. NE5532A - Dual low-noise operational amplifier
2. MC1495D - Wideband linear four-quadrant analog multiplier
3. LM112 - Precision operational amplifier
4. LM12CL - Low-noise precision operational amplifier
5. TIP122 - High-current NPN Darlington transistor
6. TDA2003A - Integrated audio power amplifier
7. MC1460 - Precision voltage regulator IC
8. MC1408 - 8-bit multiplying digital-to-analog converter
9. LM3046 - Monolithic NPN transistor array
10. MC1710 - Audio frequency signal processing IC
11. 4N35 - Phototransistor optocoupler (Failed IC)
12. MC3359 - FM IF amplifier and detector (Failed IC)

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