eSim Semester Long Internship Autumn 2025

On

Designing Integrated Circuit (IC) in eSim

Submitted by

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Acknowledgment

I would like to express my deepest gratitude to **Prof. Prabhu Ramachandran** for providing me the opportunity to be a part of the FOSSEE internship program and for supporting open-source engineering tool development at IIT Bombay. His guidance and vision have encouraged students and researchers to actively contribute to the open-source ecosystem.

I would also like to acknowledge **Prof. Kannan M. Mondgalya** for his foundational role in establishing and nurturing the FOSSEE initiative. His contributions toward open-source education and the creation of the FOSSEE fellowship framework have directly shaped the platform through which this internship was undertaken.

My sincere appreciation extends to my mentor, Sumanto Kar, for his continual support, technical guidance, and encouragement throughout the duration of this project. lis insights and feedback played a key role in refining ideas, overcoming challenges, and ensuring timely completion of the tasks assigned to me.

I would also like to thank my internal mentors, Mr. Varad Patil, Ms. Shanthi Priya K, and Mr. Aditya M, for their valuable guidance, coordination, and technical inputs during the internship. Their mentorship contributed significantly to the clarity, progress, and successful execution of the work.

This internship has been an enriching learning experience, allowing me to work closely with open-source EDA tools, develop IC subcircuits in eSim, and gain exposure to real-world circuit modeling and simulation workflows. The knowledge acquired during this period will undoubtedly support my future academic and professional pursuits.

I would also like to thank the entire FOSSEE team for their coordination, assistance, and timely interactions at various stages of this work. Their collective efforts ensured smooth workflow, resource accessibility, and effective project execution.

I extend my heartfelt thanks to **Mr. Sumanto Kar** for his constant support, leadership, and motivation.

This fellowship has been a defining chapter in my academic journey, and I leave it with not only new skills and knowledge, but also with clarity and excitement for the path that lies ahead in the VLSI domain.

Contents

Chapter 1

Introduction

The FOSSEE (Free/Libre and Open-Source Software for Education) project at IIT Bombay, an initiative of the Ministry of Education, Government of India, is committed to promoting the widespread adoption of open-source software in academic and research institutions. By reducing dependence on expensive proprietary tools, FOSSEE empowers individuals and institutions to explore free/libre alternatives that are equally capable and accessible.

1.1 FOSSEE Semestrer Long Internship

As part of its mission, FOSSEE conducts the Semestrer Long Internship Program, which provides students an opportunity to contribute to active open-source projects. The program aims to develop students' technical skills, encourage collaborative development practices, and inspire long-term involvement in the open-source community.

1.2 eSim

eSim is an open-source Electronic Design Automation (EDA) tool developed by FOSSEE for circuit design, simulation, and PCB layout. Built on top of KiCad and Ngspice, eSim is designed to provide a complete and intuitive workflow for analog, digital, and mixed-signal circuit simulation.

1.3 KiCad

In the eSim environment, KiCad is used to create the circuit schematics and define component connections. Its graphical interface simplifies the process of drawing and organizing complex circuit design.

1.4 Ngspice

Integrated within eSim, Ngspice is responsible for performing time-domain, frequency-domain, and other simulations based on the circuit designs created in KiCad. It helps in visualizing voltage, current, and other waveform outputs through simulation.

1.5 Key Features of eSim

eSim is designed to be a comprehensive, open-source EDA tool that enables users to design, simulate, and validate electronic circuits efficiently. Its features make it suitable not only for academic learning but also for real-world circuit development and prototyping. Some of its key features include:

- **Integrated Circuit Design and Simulation :** Combines KiCad for schematic capture and Ngspice for simulation, enabling users to design and test analog, digital, and mixed-signal circuits in a unified environment.
- **Subcircuit Modeling and Reuse:** Users can create custom IC models using subcircuits, which can then be saved and reused from the esim subckt library, ideal for modular design and rapid prototyping.
- **PCB Design and Layout Support :**Leveraging KiCad's PCB design suite, eSim allows users to not only simulate circuits but also transition directly to PCB layout and fabrication, making it practical for real-time product development and hardware prototyping.
- **Waveform Analysis and Debugging :** Provides interactive waveform plotting for voltage and current through simulation outputs, which helps in verifying and debugging circuits before implementation.

Chapter 2

Subcircuit Modeling of Analog and Digital ICs in eSim

2.1 Problem Statement

To design and implement subcircuit models of various analog and digital Integrated Circuits (ICs) in eSim by utilizing existing device models from the eSim library. The subcircuits are to be developed based on standard IC datasheets and integrated into the esim subckt library. Each IC model must be verified for correct functionality through suitable test circuits. This work aims to expand the reusable IC model base in eSim for future circuit design and simulation purposes.

2.2 Approach

1. **IC Selection and Datasheet Analysis :** Begin by selecting commonly used analog and digital ICs. Carefully study their datasheets to extract internal schematic diagrams, pin configurations, electrical characteristics, and application circuits.

2. **Subcircuit Schematic Development :** Using the extracted internal circuit from the datasheet, replicate the schematic in eSim. This is done using only the standard device models already available in the eSim library. The circuit is designed with strict adherence to the original datasheet specifications to ensure accurate modeling.

3. **Component Symbol and Pin Configuration Design :** Once the subcircuit is created, the corresponding symbol (component) is designed in eSim. The pin configuration and labeling are matched exactly as per the datasheet to ensure easy usability in any circuit design. This new component is saved into the esim subckt library.

4. **Application-Based Test Circuit Design :** Typical application circuits provided in the datasheet are recreated to serve as test environments. These circuits help in validating whether the behavior of the modeled IC aligns with its real-world application.

5. **Simulation and Functional Testing :** The test circuits are simulated using eSim's KiCad-to-Ngspice interface. Expected output waveforms or behaviors are compared against the datasheet's specifications. Multiple test cases are formulated and evaluated to ensure full coverage of the IC's operating conditions.

6. **Verification and Debugging Loop :** If the test results match expectations, the IC model is considered verified and finalized for library inclusion. If discrepancies arise, the model undergoes debugging—either the subcircuit or the test circuit is reviewed, modified, and re-tested until satisfactory performance is achieved.

7. **Library Integration and Reusability :** Successfully verified ICs are added to the esim subckt library with complete symbol, pin mapping, and validated functionality. These components are now available for future use in any circuit simulation within eSim.

This structured approach ensures that each subcircuit model is not only accurate but also practical and reusable for educational and design purposes.

Chapter 3

IC Design and Simulation

3.1 74HC123 Dual Retriggerable Monostable Multivibrator

74HC123 is a dual retriggerable monostable multivibrator IC used to generate a single output pulse of controlled width. The pulse duration is set using an external resistor and capacitor. The output pulse can be retriggered, allowing extension of the pulse width if another trigger occurs before timeout. It operates with low power consumption in CMOS logic systems.

Applications: Timing circuits, pulse shaping, switch debouncing, delay generation.

3.1.1 IC Schematic Diagram

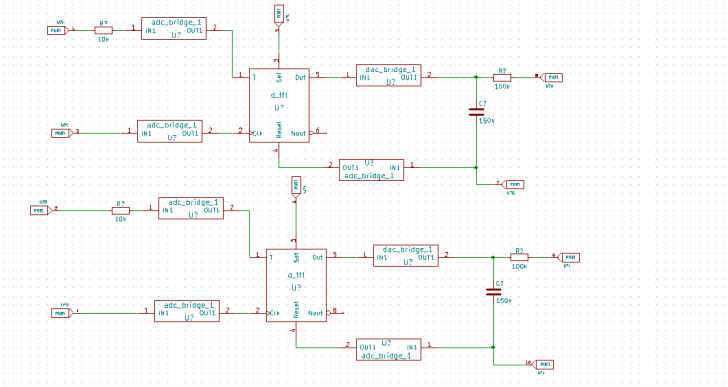

Figure 3.1: Schematic Diagram of 74HC123 IC

3.1.2 Pin Diagram

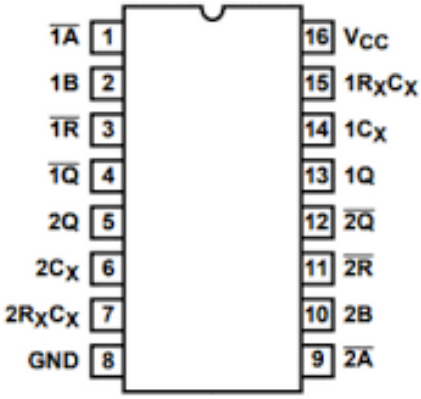

Figure 3.2: Pin diagram of 74HC123 IC

3.1.3 Test Circuit

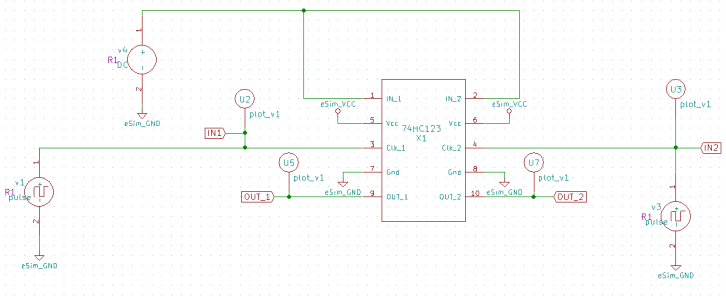

Figure 3.3: Test Circuit of 74HC123 IC

3.1.4 Output Waveforms

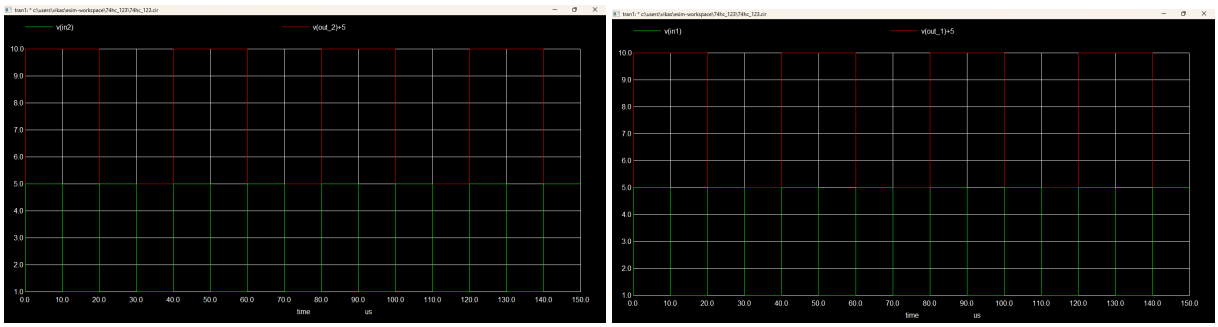

Figure 3.4: output waveforms

3.2 74HC164 8-Bit Serial-In Parallel-Out Shift Register

74HC164 is an 8-bit serial-in, parallel-out shift register that converts serial data into parallel outputs. Data is shifted on the rising edge of the clock signal. It includes an asynchronous clear input to reset all outputs. The IC is commonly used for data storage and expansion of output lines.

Applications: Serial-to-parallel data conversion, LED display driving, digital control circuits.

3.2.1 IC Schematic Diagram

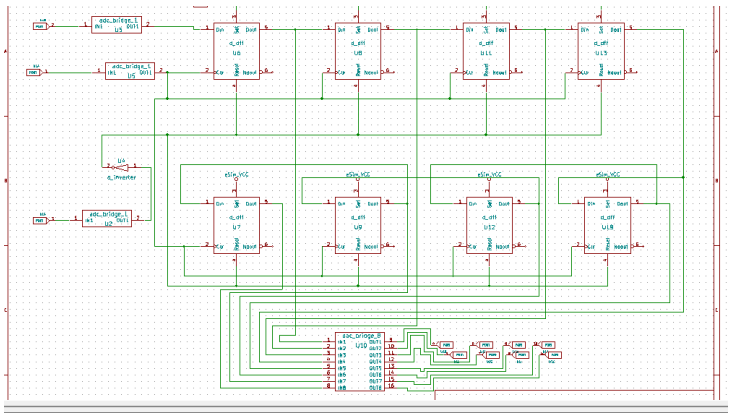

Figure 3.5: Schematic Diagram of 74HC164 IC

3.2.2 Pin Diagram

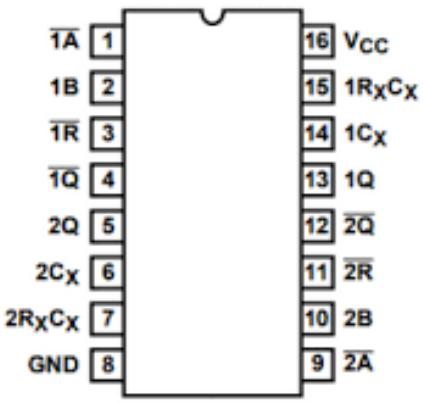

Figure 3.6: Pin diagram of 74HC164 IC

3.2.3 Test Circuit

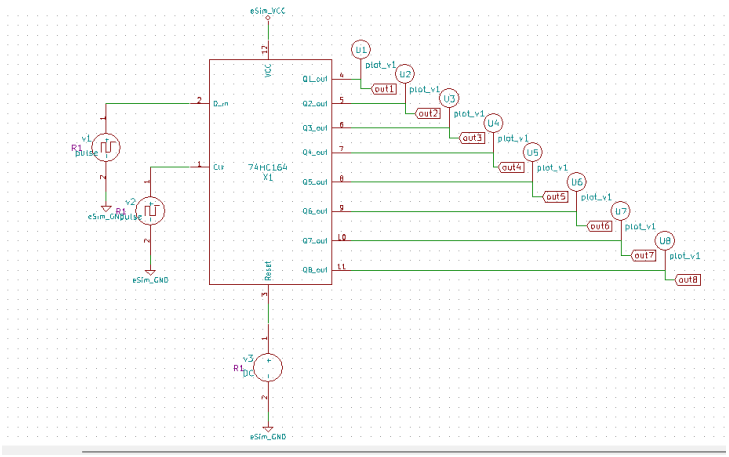

Figure 3.7: Test Circuit of 74HC164 IC

3.2.4 Output Waveforms

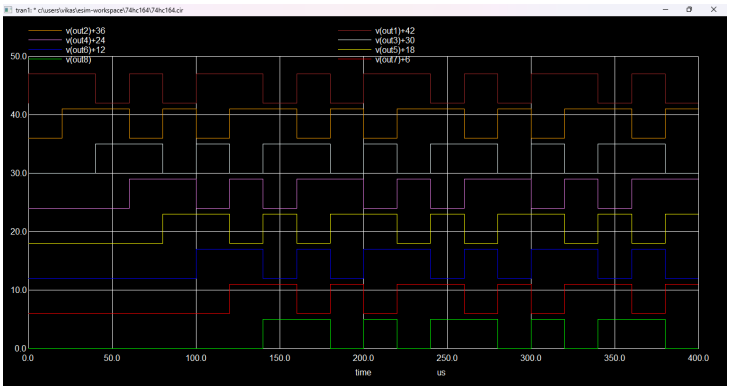

Figure 3.8: output waveforms

3.3 CD4520 Dual Binary Up Counter

CD4520 is a dual 4-bit binary up counter IC based on CMOS technology. Each counter section operates independently with its own clock input. It increments the binary count on each clock pulse. The IC provides reliable counting with low power consumption.

Applications: Event counters, frequency division, digital clocks, counting applications.

3.3.1 IC Schematic Diagram

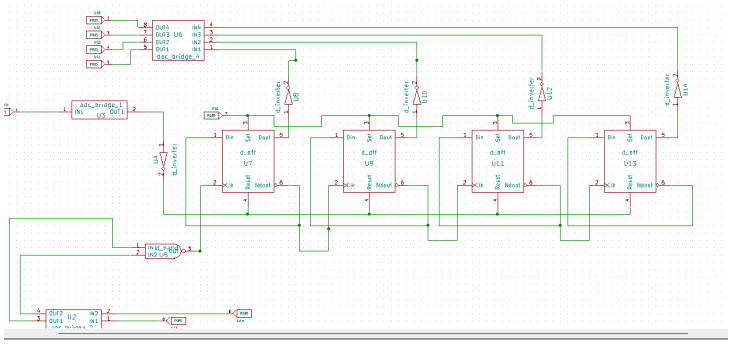

Figure 3.9: Schematic Diagram of CD4520 IC

3.3.2 Pin Diagram

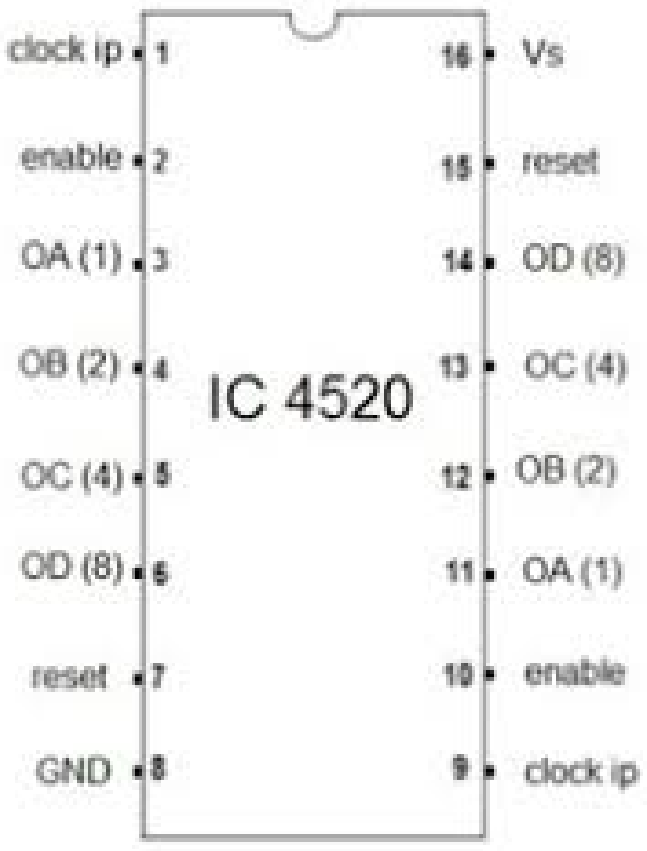

Figure 3.10: Pin diagram of CD4520 IC

3.3.3 Test Circuit

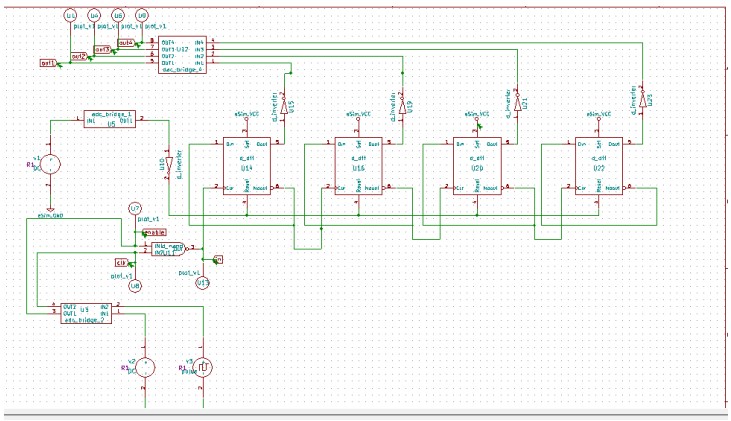

Figure 3.11: Test Circuit of CD4520 IC

3.3.4 Output Waveforms

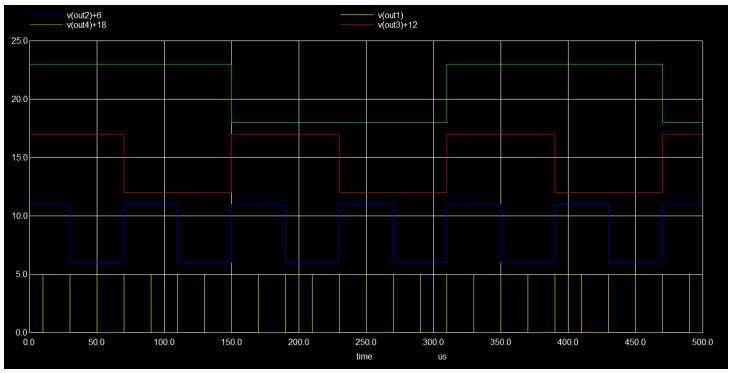

Figure 3.12: output waveforms

3.4 74LS90 Decade Counter (BCD Counter)

74LS90 is a decade (MOD-10) ripple counter from the TTL logic family. It consists of divide-by-2 and divide-by-5 counters internally. The IC can be configured for different counting modes using external connections. It operates at relatively high speed compared to CMOS counters.

Applications: Digital clocks, frequency counters, timers, divide-by-10 circuits.

3.4.1 IC Schematic Diagram

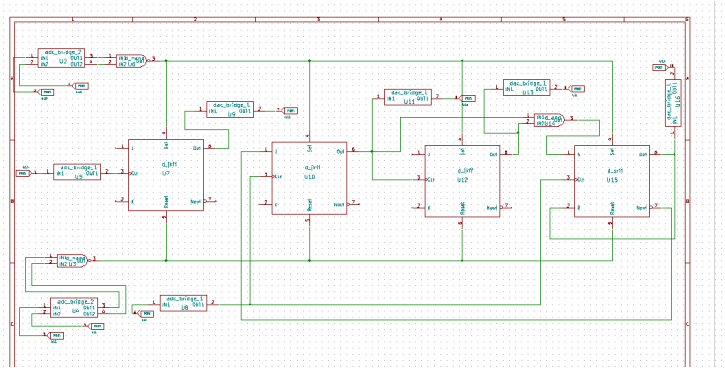

Figure 3.13: Schematic Diagram of 74LS90 IC

3.4.2 Pin Diagram

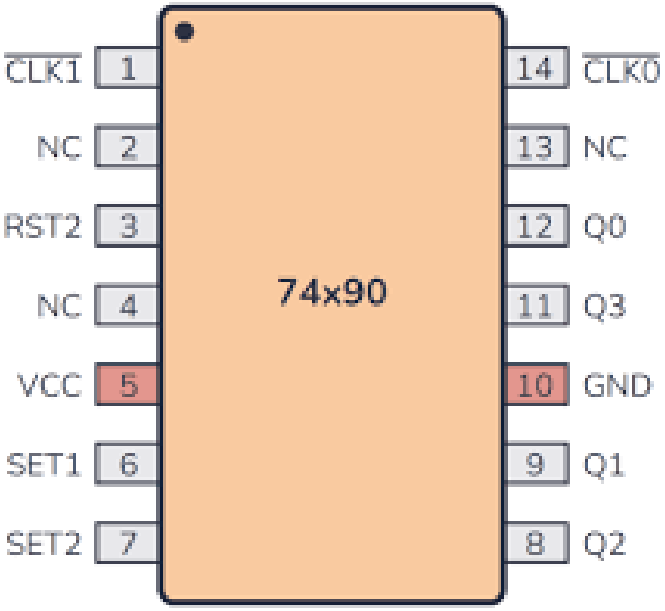

Figure 3.14: Pin diagram of 74LS90 IC

3.4.3 Test Circuit

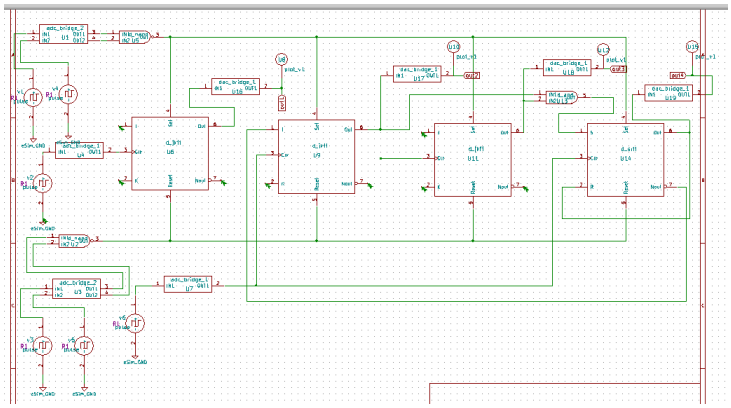

Figure 3.15: Test Circuit of 74LS90 IC

3.4.4 Output Waveforms

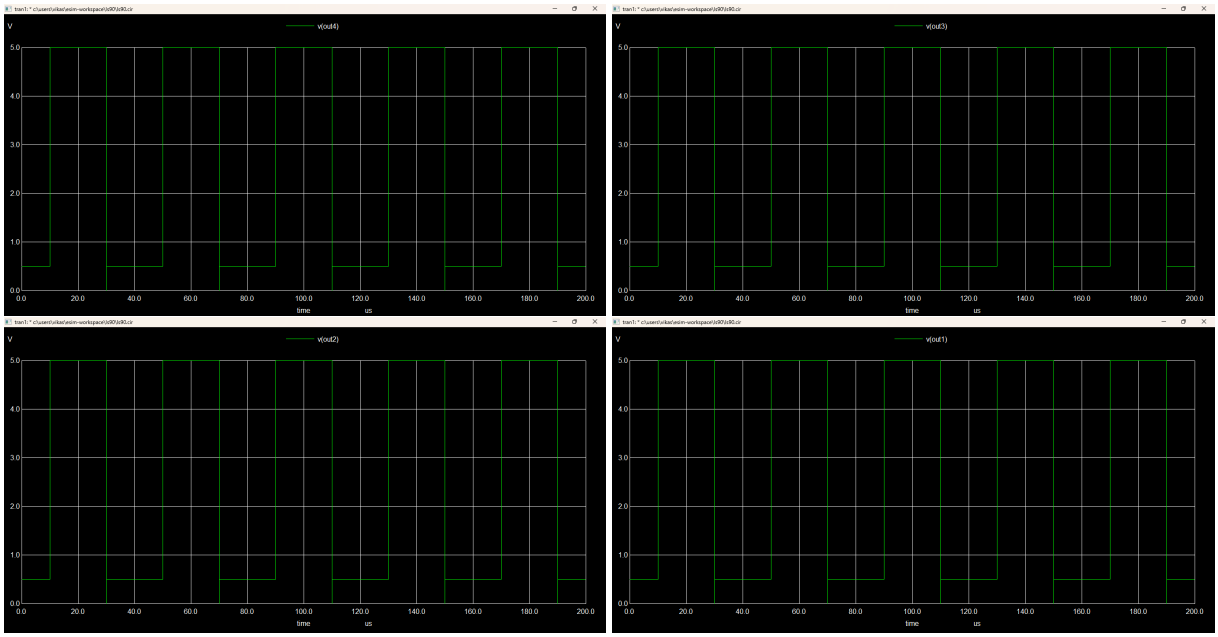

Figure 3.16: Output Waveforms

3.5 74HC107 Dual JK Flip-Flop with Clear

74HC107 is a dual JK flip-flop with asynchronous clear inputs. It toggles its output based on the J and K input conditions at the clock edge. The IC is designed using high-speed CMOS technology with low power consumption. It is suitable for synchronous logic designs.

Applications: Counters, toggle circuits, frequency dividers, control logic.

3.5.1 IC Schematic Diagram

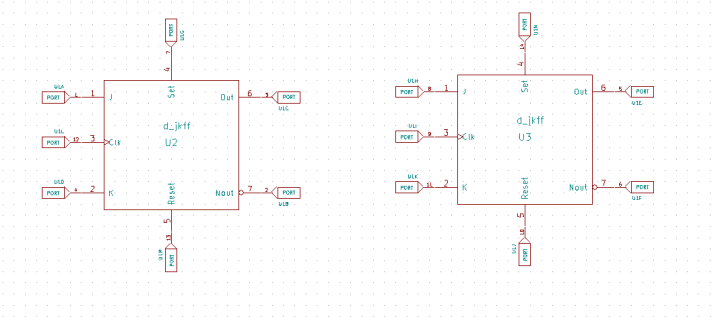

Figure 3.17: Schematic Diagram of 74HC107 IC

3.5.2 Pin Diagram

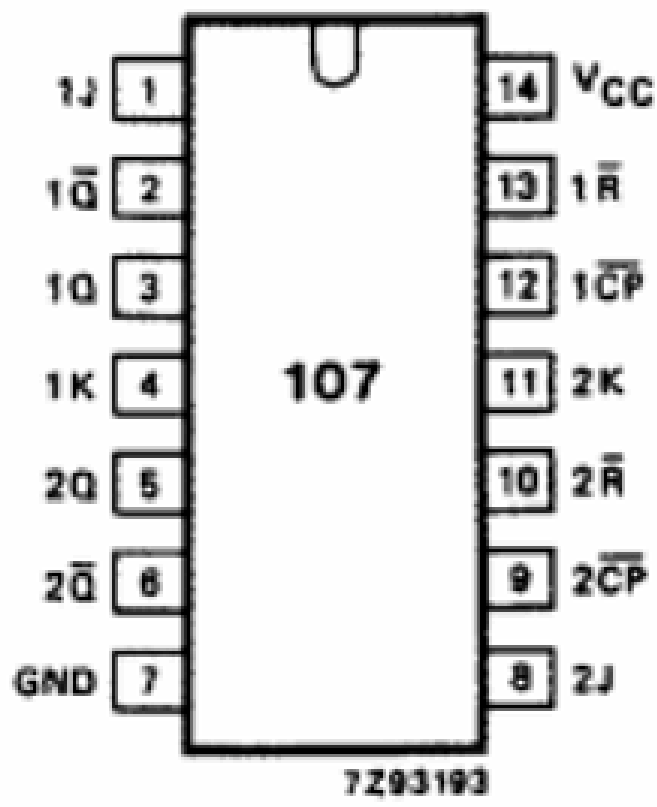

Figure 3.18: Pin diagram of 74HC107 IC

3.5.3 Test Circuit

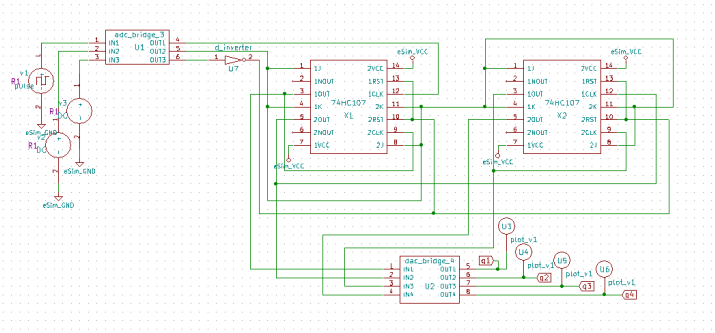

Figure 3.19: Test Circuit of 74HC107 IC

3.5.4 Output Waveforms

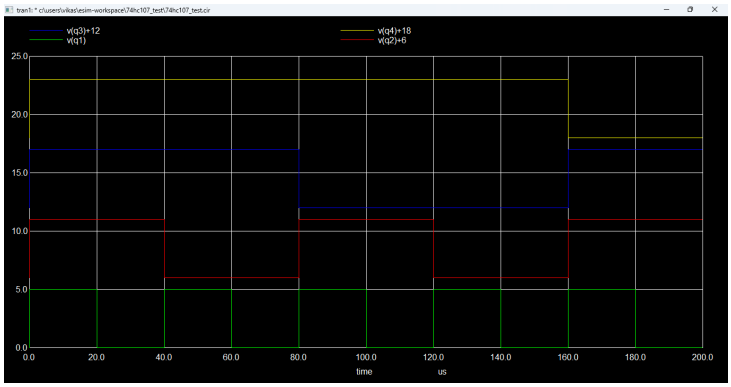

Figure 3.20: output waveforms

3.6 74HC273 Octal D-Type Flip-Flop with Clear

74HC273 is an octal D-type flip-flop with a common clock and asynchronous clear. It stores 8 bits of data simultaneously on a clock edge. All outputs are reset to zero when the clear input is activated. The IC ensures stable and synchronized data storage.

Applications: Data registers, memory buffering, digital data storage.

3.6.1 IC Schematic Diagram

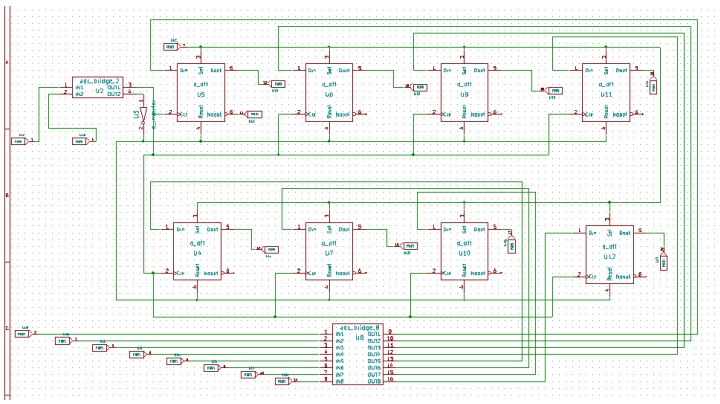

Figure 3.21: Schematic Diagram of 74HC273 IC

3.6.2 Pin Diagram

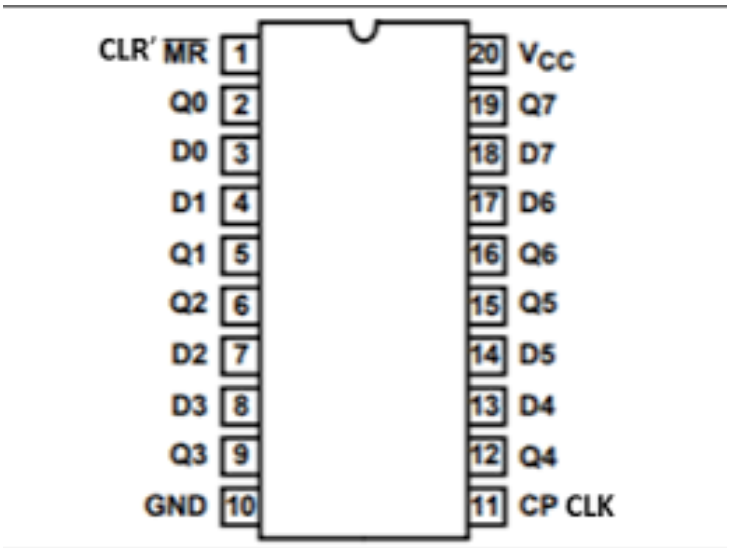

Figure 3.22: Pin diagram of 74HC273 IC

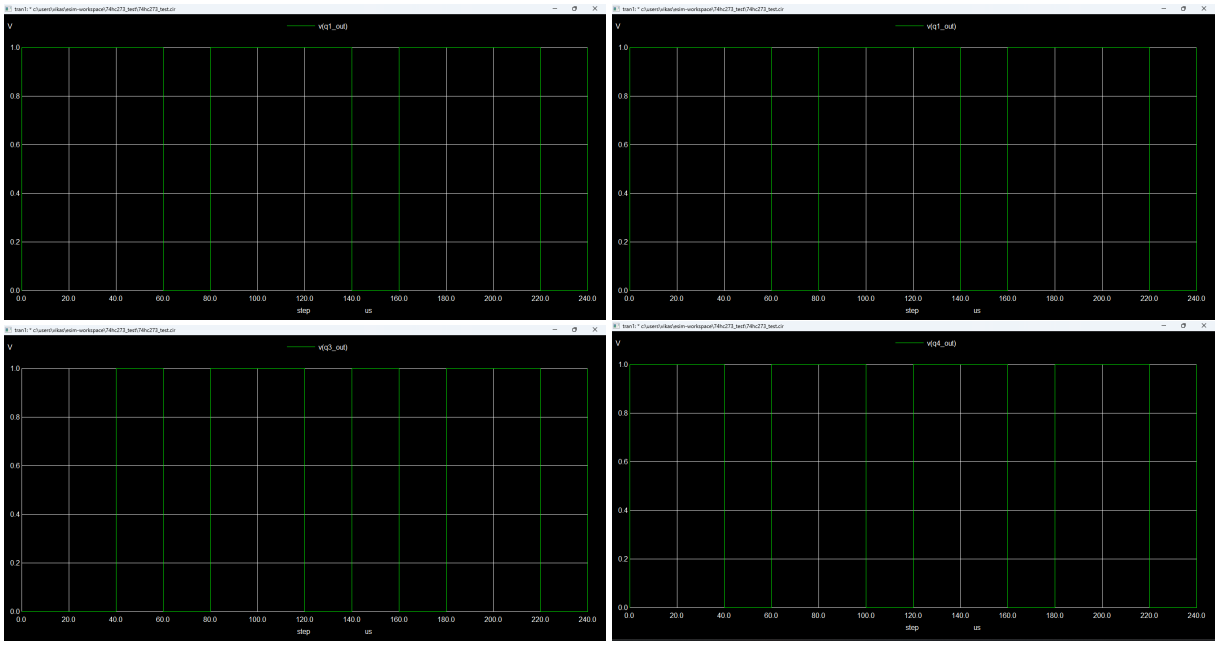

Figure 3.24: Output Waveforms

3.6.3 Test Circuit

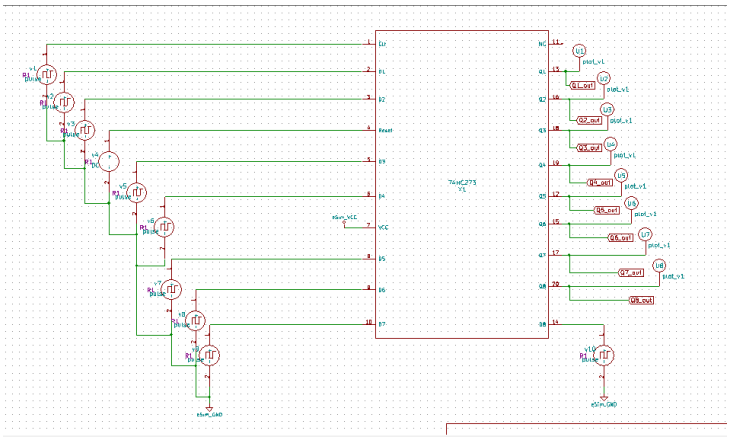

Figure 3.23: Test Circuit of 74HC273 IC

3.6.4 Output Waveforms

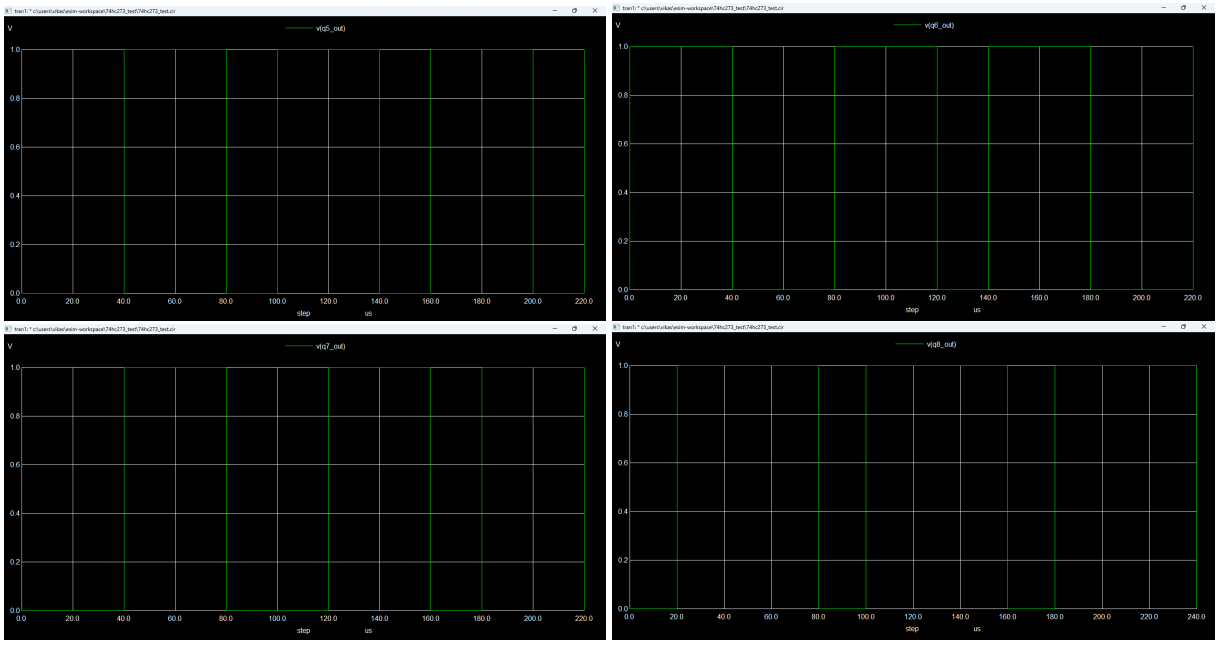

Figure 3.25: output waveforms

3.7 74HC4049 Hex Inverting Buffer

74HC4049 is a hex inverting buffer (hex inverter) IC from the High-Speed CMOS logic family. It contains six independent NOT gates that provide logic inversion and signal buffering. The IC can operate over a wide supply voltage range and offers low power consumption. It is commonly used for level shifting, waveform shaping, and driving higher load circuits.

Applications: Logic level inversion, signal buffering, waveform shaping, level conversion, interfacing between digital circuits.

3.7.1 IC Schematic Diagram

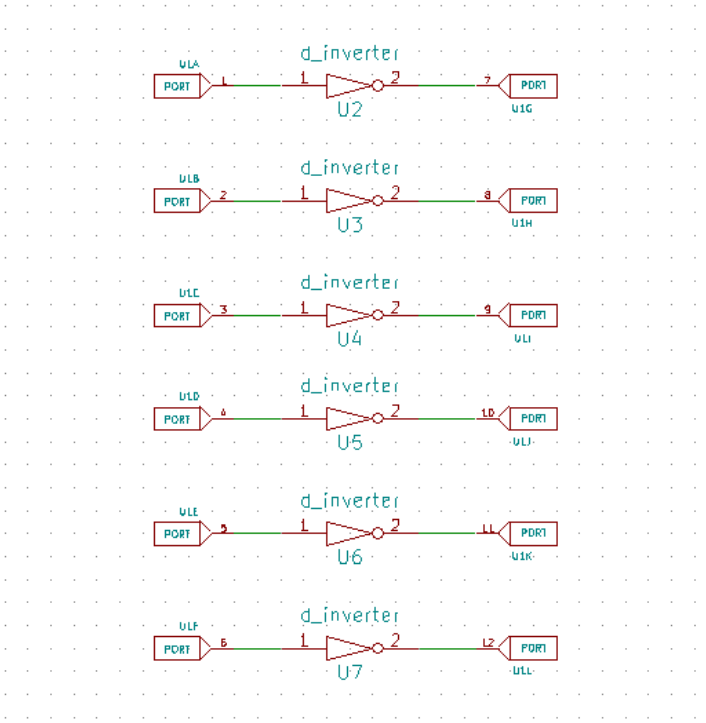

Figure 3.26: Pin diagram of 74HC4049

3.7.2 Pin Diagram

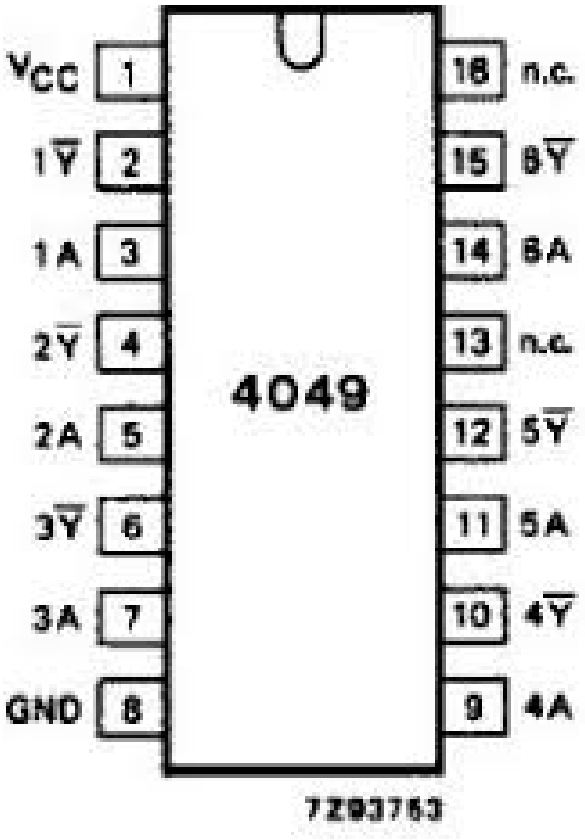

Figure 3.27: Pin diagram of 74HC4049

3.7.3 Test Circuit

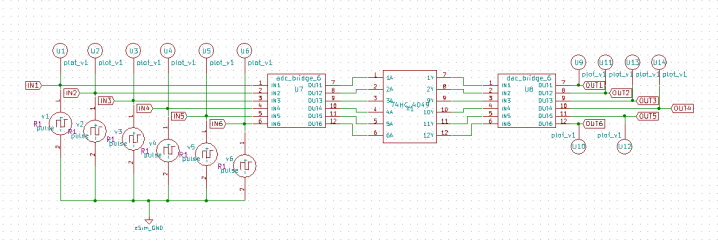

Figure 3.28: Pin diagram of 74HC4049

3.7.4 Output Waveforms

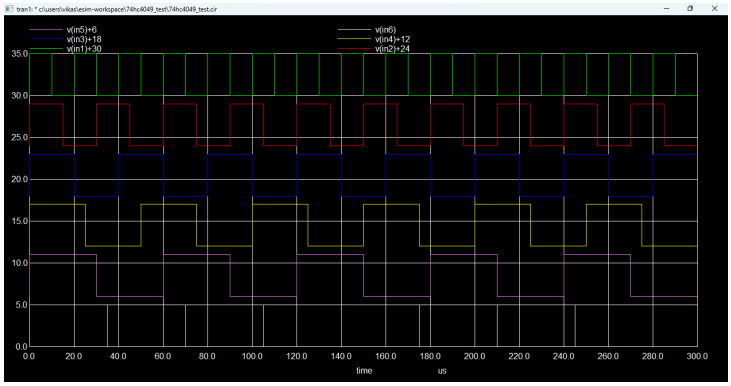

Figure 3.29: Input Waveforms

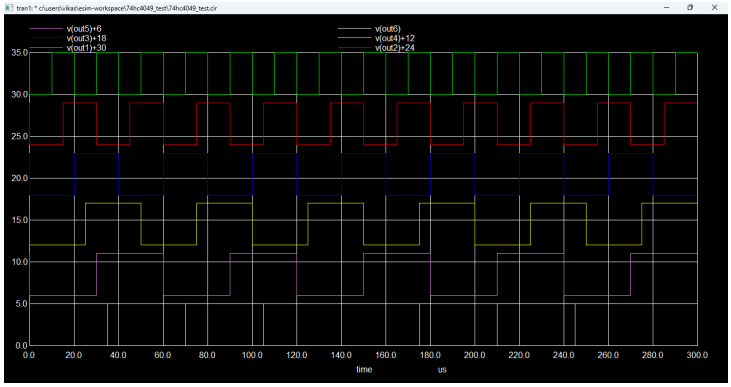

Figure 3.30: Output Waveforms

3.8 74HC393 Dual 4-Bit Binary Counter

74HC393 is a dual 4-bit binary ripple counter with asynchronous clear inputs. Each counter operates independently and increments on clock pulses. The ripple architecture makes it simple and reliable for counting tasks. It uses CMOS technology for low power operation.

Applications: Frequency division, event counting, timer circuits.

3.8.1 IC Schematic Diagram

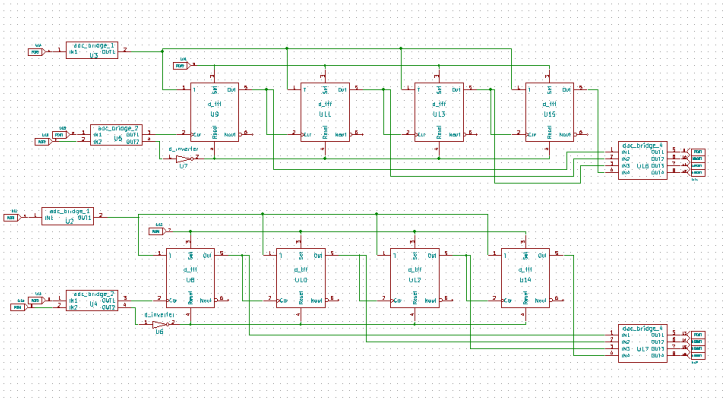

Figure 3.31: Schematic Diagram of 74HC393 IC

3.8.2 Pin Diagram

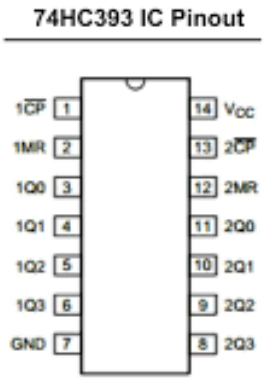

Figure 3.32: Pin diagram of 74HC393 IC

3.8.3 Test Circuit

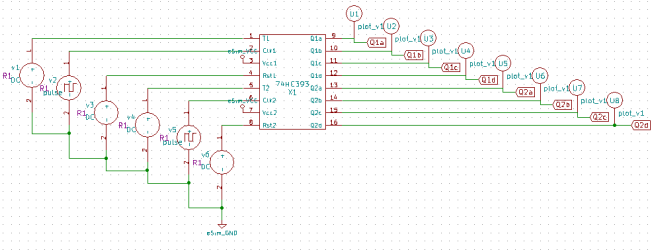

Figure 3.33: Test Circuit of 74HC393 IC

3.8.4 Output Waveforms

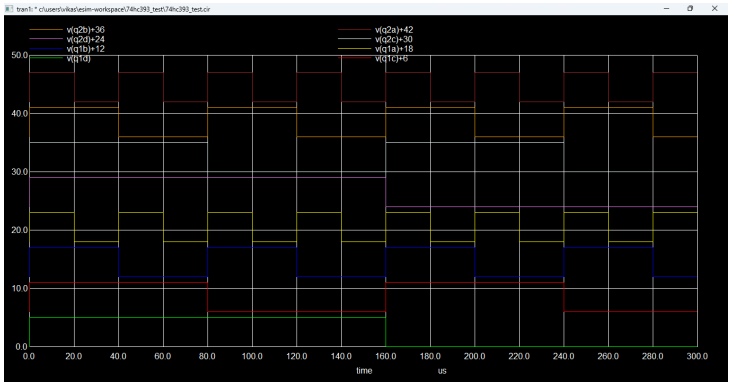

Figure 3.34: output waveforms

3.9 74HC174 Hex D-Type Flip-Flop with Clear

74HC174 is a hex D-type flip-flop with a common clock and asynchronous clear. It stores six bits of data simultaneously. The clear input resets all outputs to zero instantly. This IC is suitable for synchronous data storage applications.

Applications: Registers, data buffering, digital storage circuits.

3.9.1 IC Schematic Diagram

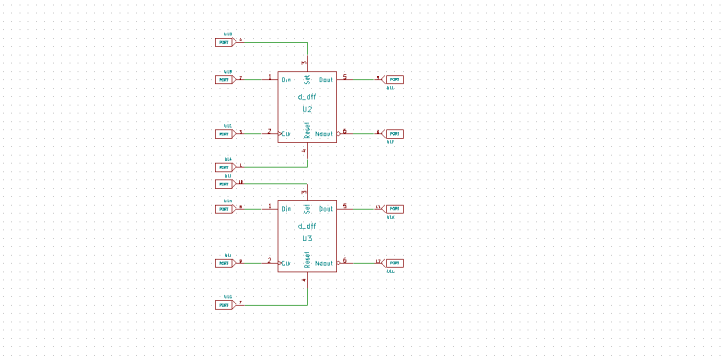

Figure 3.35: Schematic Diagram of 74HC174 IC

3.9.2 Pin Diagram

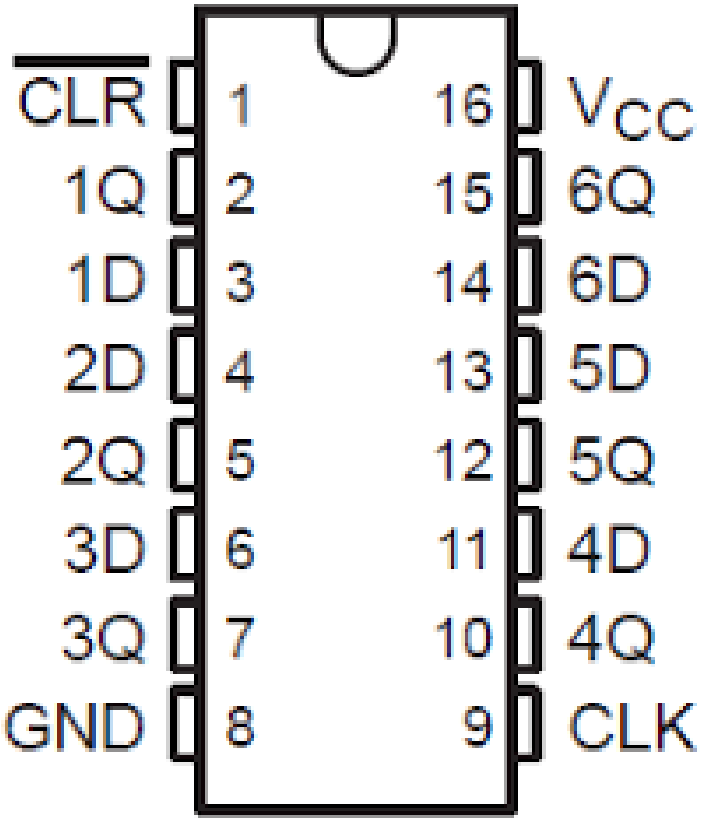

Figure 3.36: Pin diagram of 74HC174 IC

3.9.3 Test Circuit

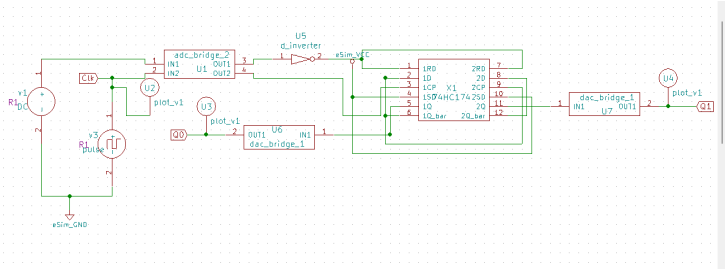

Figure 3.37: Test Circuit of 74HC174 IC

3.9.4 Output Waveforms

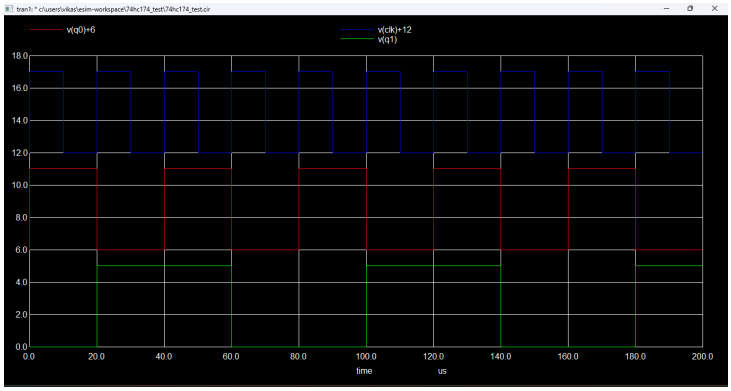

Figure 3.38: output waveforms

3.10 74HC85 4-Bit Magnitude Comparator

74HC85 is an IC 4-bit magnitude comparator. It compares two 4-bit binary numbers and indicates whether one number is greater than, equal to, or less than the other. The IC supports cascading to compare larger bit-width numbers. It operates with high-speed CMOS logic.

Applications: Digital comparison circuits, arithmetic logic units, decision-making systems.

3.10.1 IC Schematic Diagram

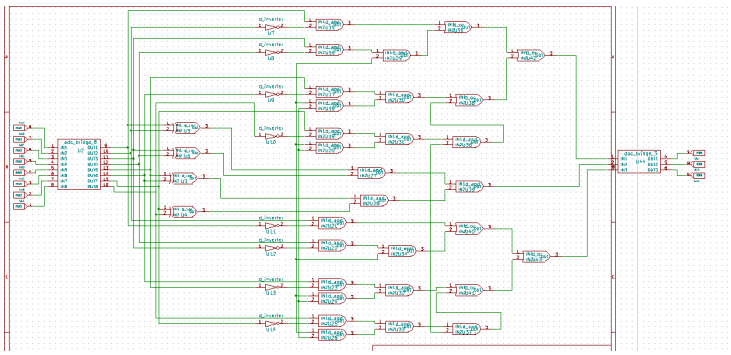

Figure 3.39: Schematic Diagram of 74HC85 IC

3.10.2 Pin Diagram

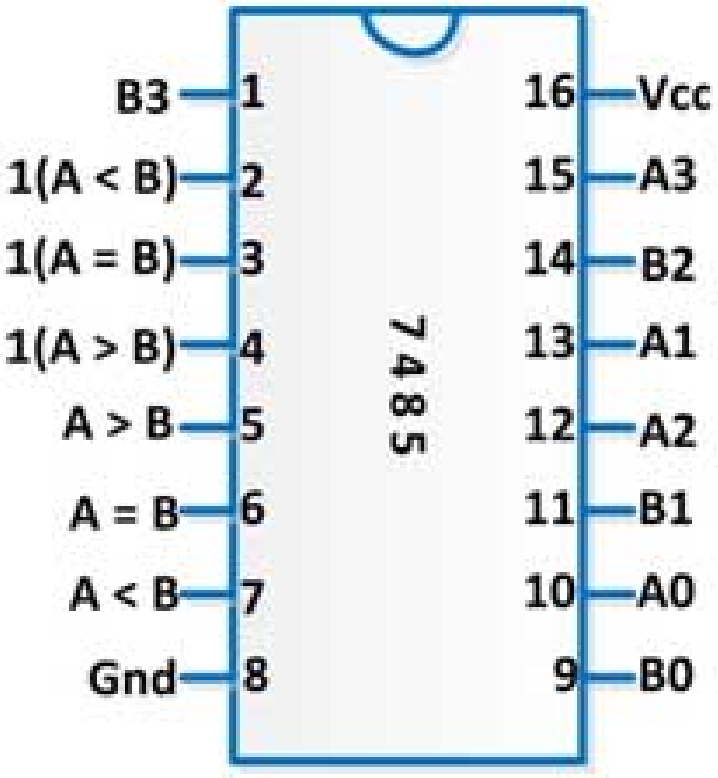

Figure 3.40: Pin diagram of 74HC85 IC

3.10.3 Test Circuit

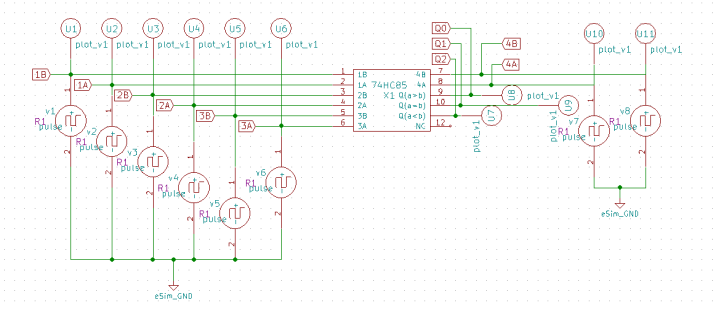

Figure 3.41: Test Circuit of 74HC85 IC

3.10.4 Output Waveforms

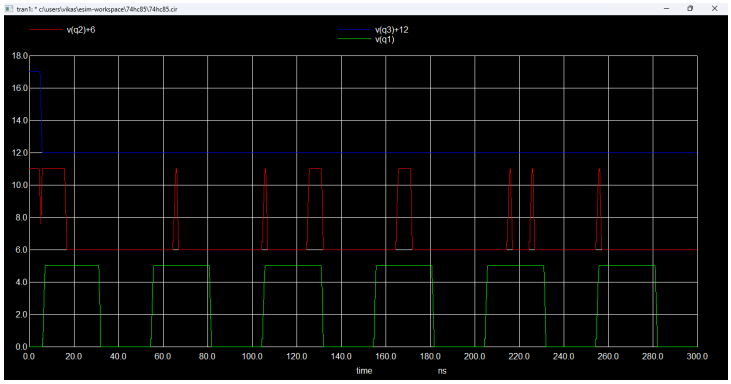

Figure 3.42: output waveforms

Chapter 4

Conclusion and Future Scope

This semester long internship provided practical exposure to the concepts of integrated circuit design and simulation using the open-source eSim platform. The work primarily involved modeling, implementing, and verifying various digital integrated circuits through the use of subcircuit design techniques. By carefully studying IC datasheets and reproducing their internal logic using standard device models available in eSim, functional and reusable subcircuits were successfully developed.

Each designed IC was validated using appropriate test circuits and waveform analysis, ensuring correct logical behavior and reliable operation.The internship also strengthened familiarity with CMOS and TTL logic families, counters, flip-flops, latches, comparators, and inverters, while emphasizing structured documentation and systematic testing practices.

The experience gained during this internship can be further extended by modeling more complex digital and mixed-signal integrated circuits such as arithmetic logic units, encoders, decoders, memory elements, and programmable logic blocks. Future work may also include performance evaluation in terms of propagation delay, power consumption, and noise margins. Additionally, the developed subcircuits can be expanded into a standardized reusable library for educational and research purposes, and the simulated designs can be validated through PCB implementation and hardware testing. These extensions would enhance the effectiveness of eSim as a comprehensive platform for learning, experimentation, and practical VLSI system design.

Bibliography

[1] FOSSEE Project, IIT Bombay, India. [Online]. Available: https://fossee.in/

[2] eSim – Open Source EDA Tool, FOSSEE, IIT Bombay. [Online]. Available: https://esim.fossee.in/

[3] KiCad EDA Suite. [Online]. Available: https://www.kicad.org/

[4] Ngspice – Mixed-Level/Mixed-Signal Circuit Simulator. [Online]. Available: http://ngspice.sourceforge.net/

[5] Datasheet Catalog – Electronic Component Datasheets. [Online]. Available: https://www.datasheetcatalog.com/

[6] AllDatasheet – IC Datasheets. [Online]. Available: https://www.alldatasheet.com/

[7] Texas Instruments Incorporated. IC Datasheets. [Online]. Available: https://www.ti.com/