Semester-Long Internship Autumn 2025

On

Designing Integrated Circuit in eSim

Submitted by

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Acknowledgment

I would like to express my deepest gratitude to Prof. Prabhu Ramachandran for providing me the opportunity to be a part of the FOSSEE internship program and for supporting open-source engineering tool development at IIT Bombay. His guidance and vision have encouraged students and researchers to actively contribute to the open-source ecosystem.

I would also like to acknowledge Prof. Kannan M. Moudgalya for his foundational role in establishing and nurturing the FOSSEE initiative. His contributions toward open-source education and the creation of the FOSSEE fellowship framework have directly shaped the platform through which this internship was undertaken.

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This internship has been an enriching learning experience, allowing me to work closely with open-source EDA tools, develop IC subcircuits in eSim, and gain exposure to real-world circuit modeling and simulation workflows. The knowledge acquired during this period will undoubtedly support my future academic and professional pursuits.

I would also like to thank the entire FOSSEE team for their coordination, assistance, and timely interactions at various stages of this work. Their collective efforts ensured smooth workflow, resource accessibility, and effective project execution.

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Chapter 1

Introduction

1.1 FOSSEE

FOSSEE, which stands for Free/Libre and Open Source Software for Education, is an organization based at IIT Bombay. It is a remarkable initiative aimed at promoting the use of open-source software in education and research. It was established with the mission to reduce dependency on proprietary software and to encourage the adoption of open-source alternatives. FOSSEE offers a wide range of tools and resources that cater to various academic and professional needs.

It provides comprehensive documentation, tutorials, workshops, and hands-on training sessions to empower students, educators, and professionals to leverage open-source software for their projects and coursework. The organization's commitment to fostering a collaborative and inclusive environment has significantly contributed to the democratization of technology and has opened up new avenues for innovation and learning.

1.2 eSim

eSim, created by the FOSSEE project at IIT Bombay, is a versatile open-source software tool for circuit design and simulation. It combines various open-source software packages into one cohesive platform, making it easier to design, simulate, and analyze electronic circuits. This tool is particularly useful for students, educators, and professionals who need an affordable and accessible alternative to proprietary software.

eSim offers features for schematic creation, circuit simulation, and PCB design, and includes an extensive library of components. The Subcircuit feature is a significant enhancement, enabling users to design complex circuits by integrating simpler subcircuits. Through eSim, FOSSEE promotes the use of open-source solutions in engineering education and professional fields, encouraging innovation and collaboration.

1.3 NgSpice

NgSpice is an open-source SPICE simulator for electric and electronic circuits. It can simulate various circuit elements, including JFETs, bipolar and MOS transistors, passive elements (R, L, C), diodes and other devices, all interconnected in a netlist.

Digital circuits are also simulated, ranging from single gates to complex circuits, including combinations of analog, digital, and mixed-signal circuits. NgSpice offers a wealth of device models for active, passive, analog, and digital elements. Users input their circuits as netlists, and the output is one or more graphs of currents, voltages, and other electrical quantities, or saved in a data file.

1.4 Makerchip

Makerchip is a platform that offers convenient and accessible tools for digital circuit design. It provides both browser-based and desktop-based environments for coding, compiling, simulating, and debugging Verilog designs. Makerchip supports a combination of open-source and proprietary tools, ensuring a comprehensive range of capabilities.

Users can simulate Verilog/SystemVerilog/Transaction-Level Verilog code in Makerchip. eSim is interfaced with Makerchip using a Python-based application called Makerchip-App, which launches the Makerchip IDE. Makerchip aims to make circuit design easy and enjoyable for users of all skill levels. The platform provides a userfriendly interface, intuitive workflows, and a range of helpful features that simplify the design process and enhance the overall user experience.

The main drawback of these open-source tools is that they are not comprehensive. While some are capable of PCB design (e.g., KiCad), others focus on simulations (e.g., EDA). To the best of our knowledge, there is no open-source software that combines circuit design, simulation, and layout design in one platform. eSim addresses this gap by integrating all these capabilities.

Chapter 2

Features of eSim

The objective behind the development of eSim is to provide an open-source EDA solution for electronics and electrical engineers. The software is capable of performing schematic creation, PCB design, and circuit simulation (analog, digital, and mixedsignal). It also provides facilities to create new models and components. Thus, eSim offers the following features:

1. Schematic Creation: eSim provides an easy-to-use graphical interface for drawing circuit schematics, making it accessible for users of all levels. Users can drag and drop components from the library onto the schematic, simplifying the design process. Comprehensive editing tools allow for easy modification of schematics, including moving, rotating, and labeling components.

2. Circuit Simulation: eSim supports SPICE (Simulation Program with Integrated Circuit Emphasis), a standard for simulating analog and digital circuits. Users can perform various types of analysis such as transient, AC, and DC, providing insights into circuit behavior over time and frequency. An integrated waveform viewer helps visualize simulation results, aiding in the analysis and debugging of circuit designs.

3. PCB Design: The PCB layout editor allows users to place components and route traces with precision. eSim includes DRC (Design Rule Check) capabilities to ensure that the PCB design adheres to manufacturing constraints and electrical rules. Users can generate Gerber files, which are standard for PCB fabrication, directly from their designs.

4. Subcircuit Feature: This feature enables users to create complex circuits by integrating smaller, simpler subcircuits, promoting modular and hierarchical design approaches. Subcircuits can be reused in different projects, saving time and effort in redesigning common circuit elements.

5. Open Source Integration: eSim integrates several open-source tools like KiCad, NgSpice, and GHDL, providing a comprehensive suite for electronic design automation. Being open-source, eSim is free to use, making advanced circuit design tools accessible without the need for expensive licenses.

Chapter 3

Problem Statement

To design and develop various analog and digital integrated circuit models in the form of sub-circuits using device model files already present in the eSim library. These IC models should be useful for future circuit design purposes by developers and users once they are successfully integrated into the eSim subcircuit library.

3.1 Approach

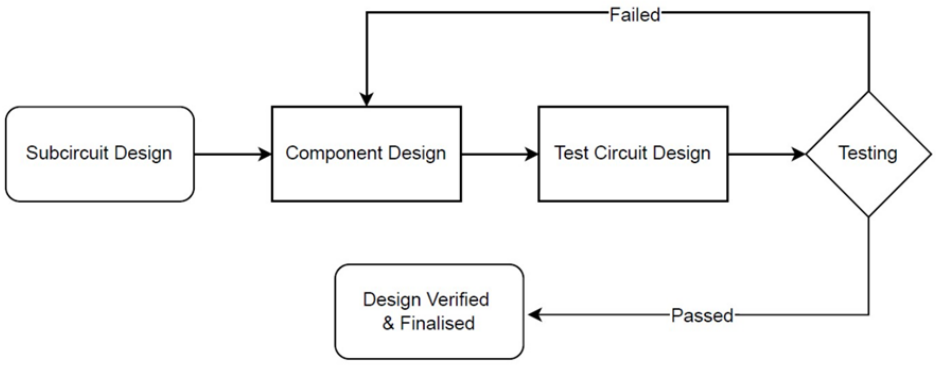


Figure 3.1: Flowchart of IC Design Approach Followed

My approach to implementing the problem statement involved a systematic process, leveraging datasheets from leading Integrated Circuit (IC) manufacturers such as Texas Instruments, Fairchild Semiconductor, and National Semiconductor. I focused on selecting ICs with diverse functionalities, including arithmetic logic units, data selectors, comparators, and specialized logic gates. The process is outlined in the following steps:

1. Analyzing Datasheets: The first step involved an in-depth review of datasheets for various analog and digital ICs. I aimed to identify circuits suitable for implementation in eSim that were not already present in the eSim library. This process included scrutinizing the detailed schematics of each IC, evaluating component values, and understanding specifications. The goal was to select ICs that offered unique functionalities or enhancements not yet covered.

2. Subcircuit Creation: After selecting appropriate ICs, I proceeded to model these as sub-circuits within eSim. I utilized the model files available in the eSim device model library and ensured that my designs adhered strictly to the specifications outlined in the official datasheets. This phase also involved

creating accurate symbol and pin diagrams for each IC, in accordance with the packaging and pin descriptions provided in the datasheets. This step was crucial for ensuring the fidelity of the subcircuit models.

3. Test Circuit Design: With the sub-circuits created, I then designed and built test circuits based on the datasheets. This step was essential for verifying the functionality of each sub-circuit. I developed a series of test cases and constructed corresponding test circuits to evaluate the performance and accuracy of the implemented IC models.

4. Schematic Testing: Following the construction of test circuits, I conducted simulations to analyze the outputs. This involved generating waveforms and plots to assess the behavior of the circuits. I employed KiCad for converting designs to NgSpice netlists and utilized eSim's simulation features to perform comprehensive testing.

If the simulated outputs deviated from expected results, it signaled potential errors in the schematic. In such instances, I revisited the design phase to identify and correct discrepancies. The iterative process of debugging and re-testing continued until the test cases produced satisfactory results. Once the IC models met the desired performance criteria, they were deemed successful, marking the completion of the design process.

Chapter 4

74HC283

4.1 Description

The 74HC283 is a high-speed CMOS 4-bit binary full adder with fast carry that performs the addition of two 4-bit binary numbers. It features look-ahead carry design for high-speed arithmetic operations, making it ideal for use in arithmetic logic units (ALUs), processors, and high-speed computing systems. The device accepts two 4-bit words (A0, A1, A2, A3 and B0, B1, B2, B3) and a carry input (Cin), produCing a 4-bit sum (S0, S1, S2, S3) and a carry output (Cout).

4.2 Pin Diagram

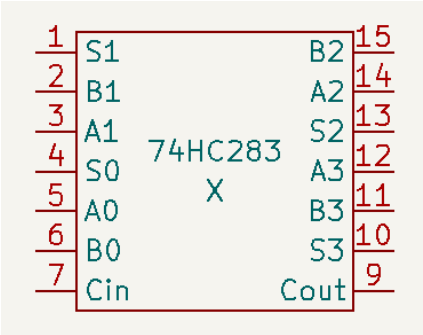


Figure 4.1: Pin Configuration of the 74HC283

4.3 Sub Circuit Layout

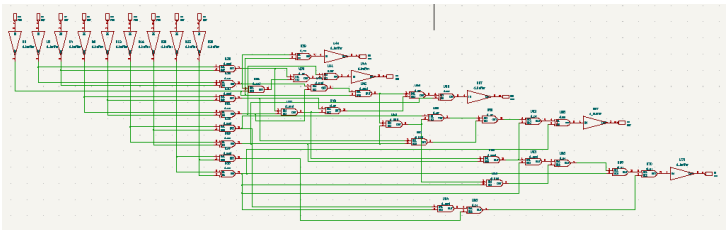


Figure 4.2: Subcircuit Schematic of the 74HC283

4.4 Test Circuit

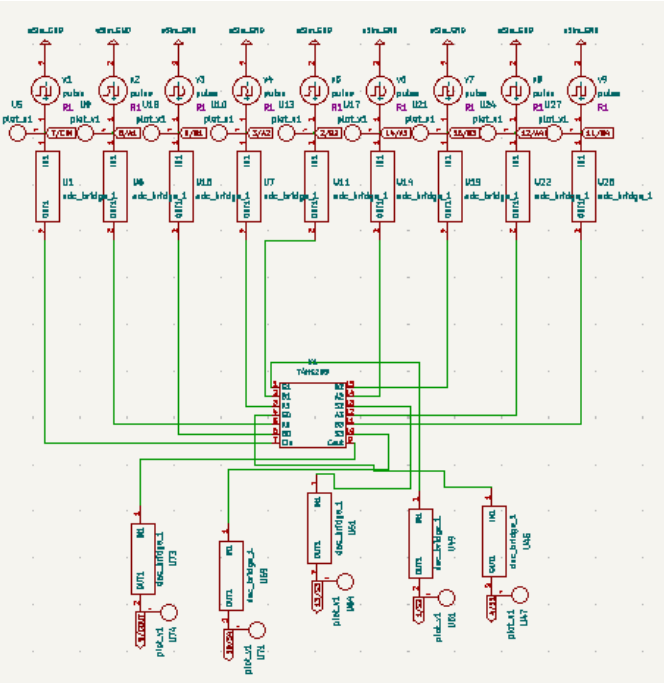
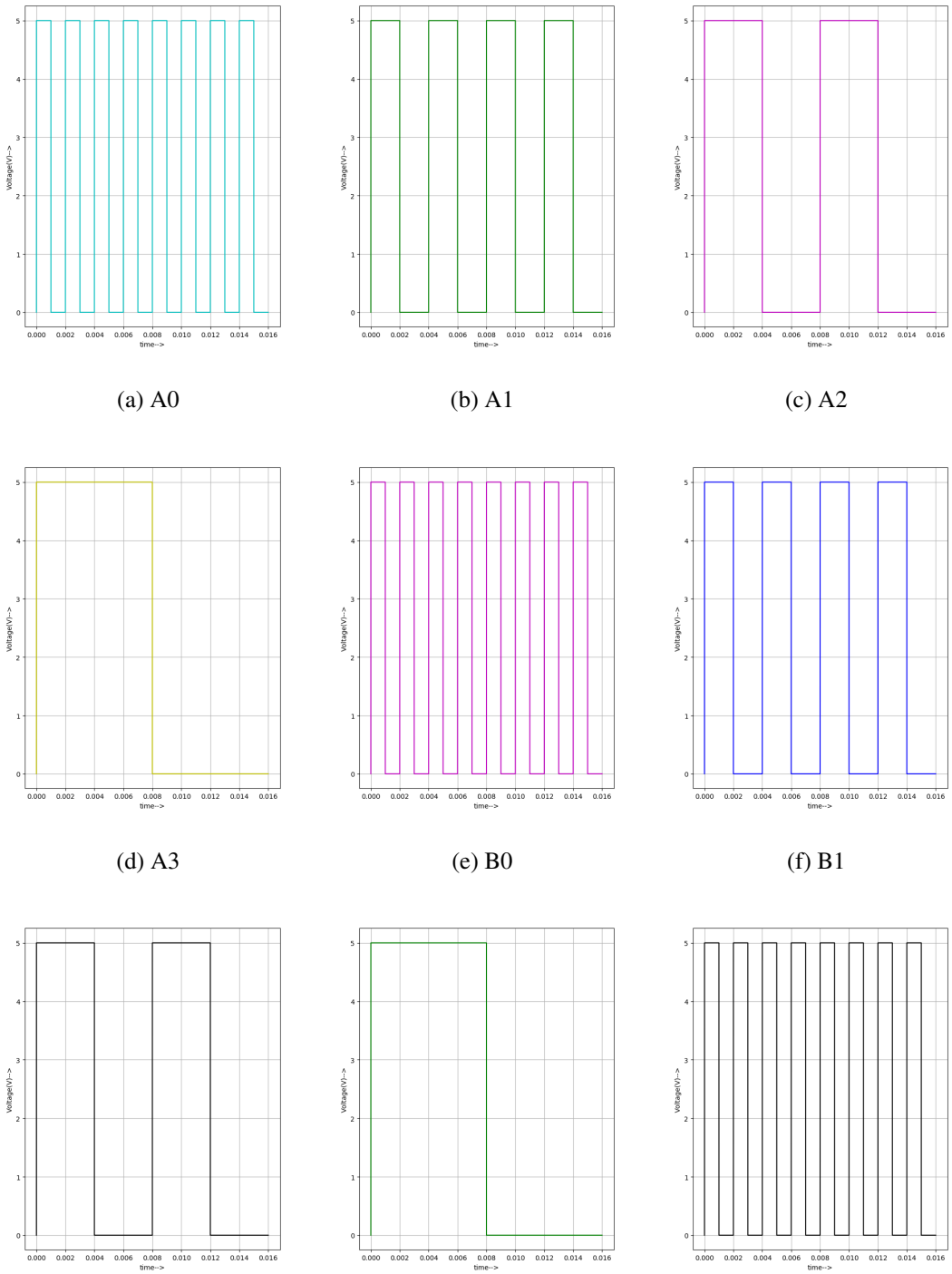


Figure 4.3: Test Circuit of the 74HC283

4.5 Input Waveforms



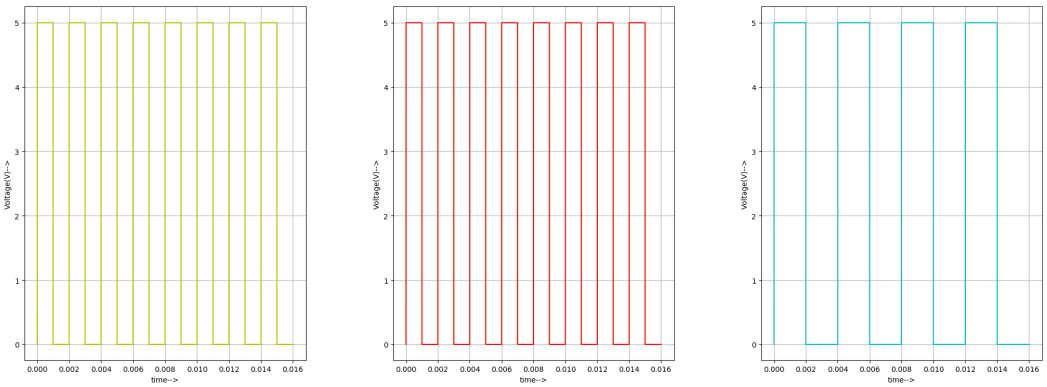
(a) A0 (b) A1 (c) A2

(d) A3 (e) B0 (f) B1

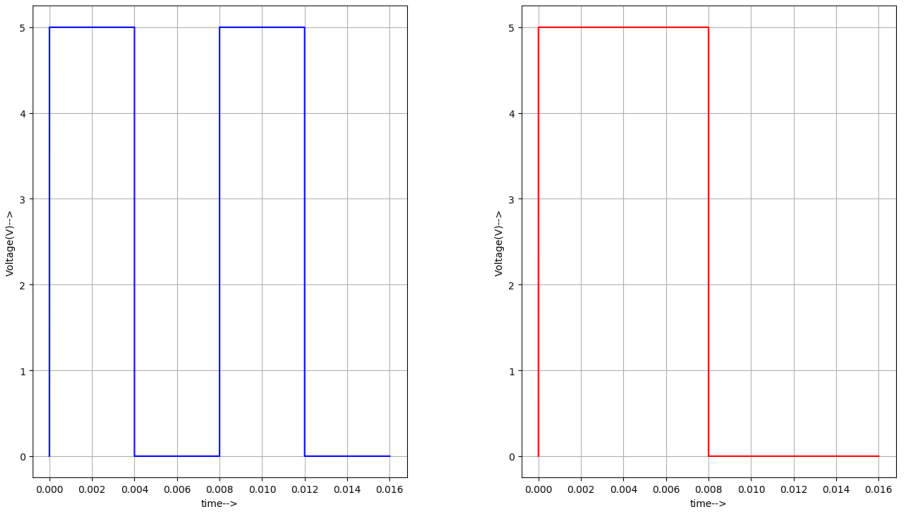
(g) B2 (h) B3 (i) Cin

Figure 4.4: Input Waveforms of the 74HC283

4.6 Output Waveforms



(a) S0 (b) S1 (c) S2



(d) S3 (e) Cout

Figure 4.5: Output Waveforms of the 74HC283

Chapter 5

74LS352

5.1 Description

The 74LS352 is a dual 4-line to 1-line data selector/multiplexer with common select lines and independent enable inputs. Each multiplexer selects one of four data sources (1C0,1C1,1C2,1C3 for the first multiplexer; 2C0,2C1,2C2,2C3 for the second) based on the state of the common select lines (A, B) and routes it to the output (Y1, Y2). The independent enable inputs (G1, G2) allow each multiplexer to be disabled, forCing the output to a high-impedance or low state depending on the logic family.

5.2 Pin Diagram

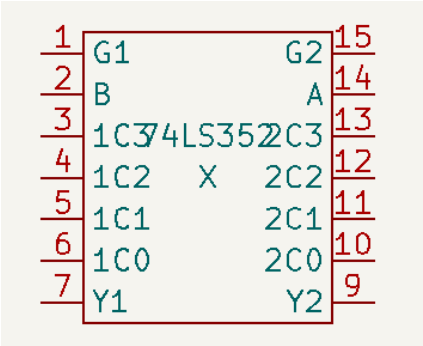


Figure 5.1: Pin Configuration of the 74LS352

5.3 Sub Circuit Layout

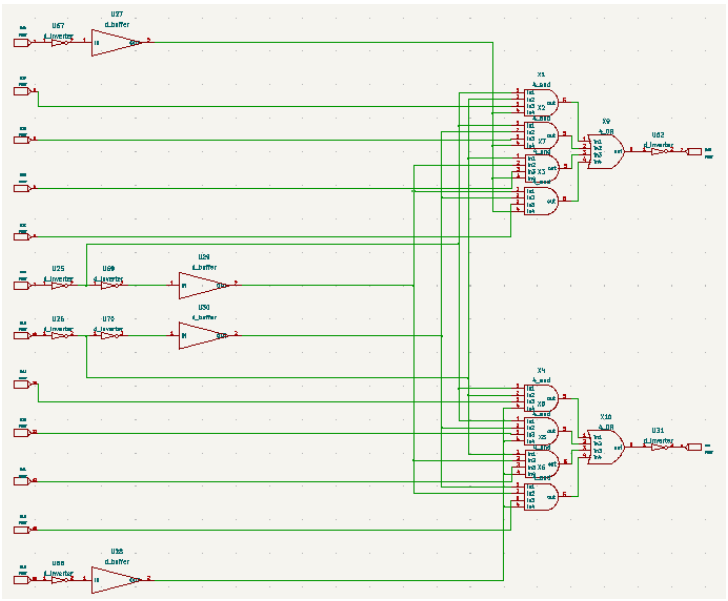


Figure 5.2: Subcircuit Schematic of the 74LS352

5.4 Test Circuit

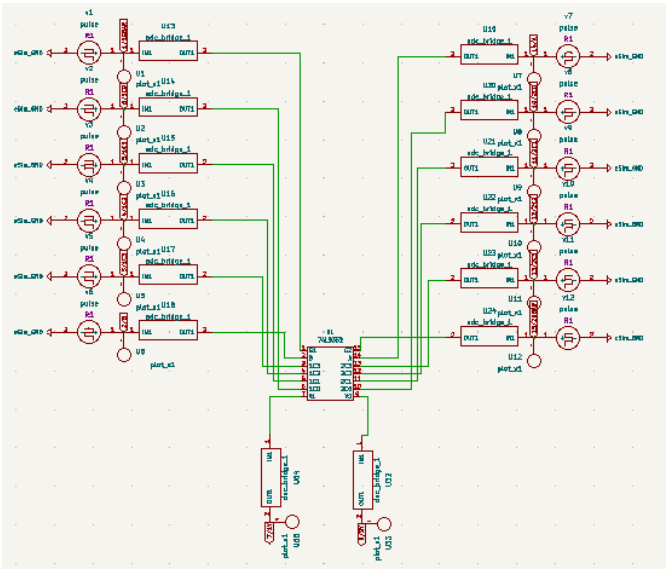
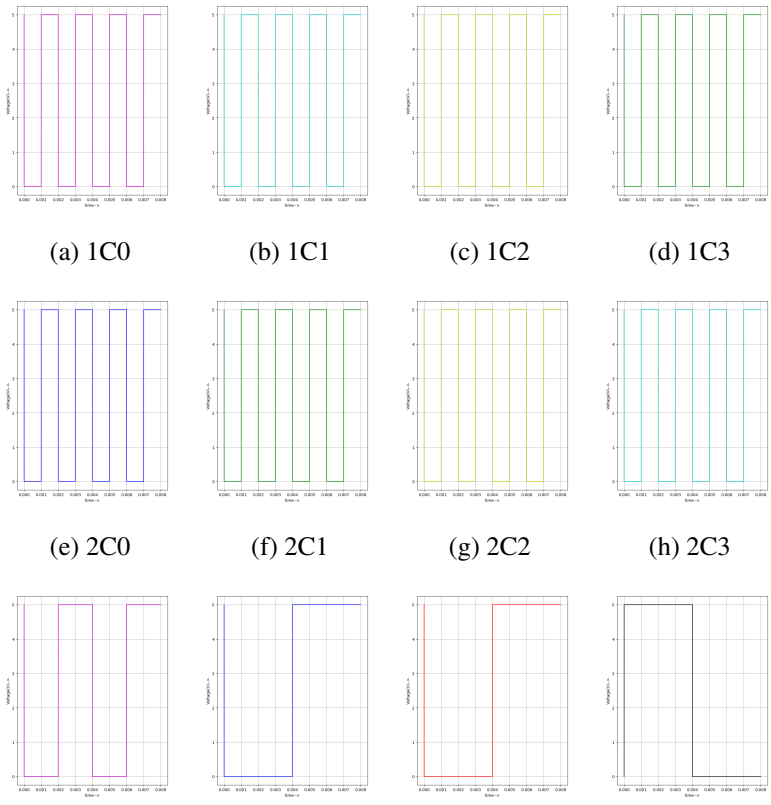


Figure 5.3: Test Circuit of the 74LS352

5.5 Input Waveforms



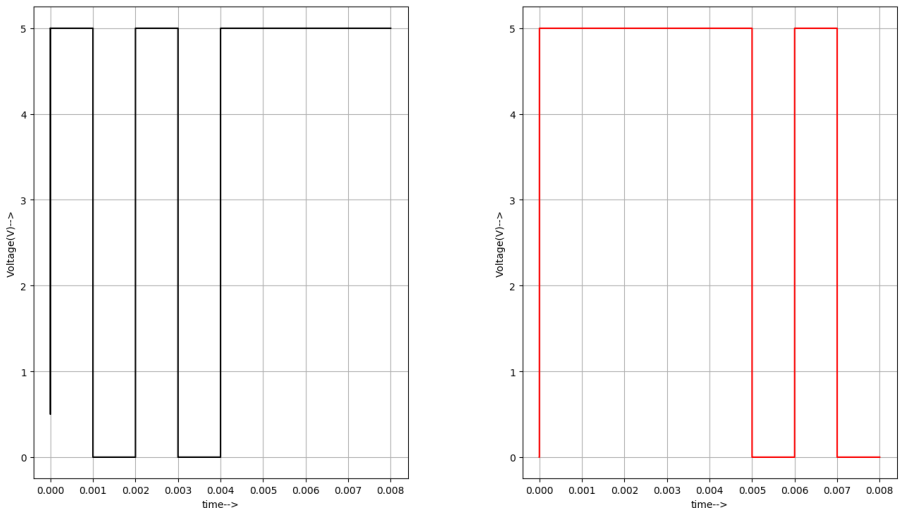
(a) 1C0 (b) 1C1 (c) 1C2 (d) 1C3

(e) 2C0 (f) 2C1 (g) 2C2 (h) 2C3

(i) A (j) B (k) G1 (l) G2

Figure 5.4: Input Waveforms of the 74LS352

5.6 Output Waveforms



(a) Y1 (b) Y2

Figure 5.5: Output Waveforms of the 74LS352

Chapter 6

74F521

6.1 Description

The 74F521 is an 8-bit identity comparator designed for high-speed comparison of two 8-bit words. It features fast propagation delays and provides a single output that indicates whether the two input words are equal. The device compares corresponding bits of the A and B inputs: A0 with B0, A1 with B1, A2 with B2, A3 with B3, A4 with B4, A5 with B5, A6 with B6, and A7 with B7. The output $\bar{O}$ A=B goes low when all corresponding bits are equal, subject to the enable input $\bar{I}$ A=B.

6.2 Pin Diagram

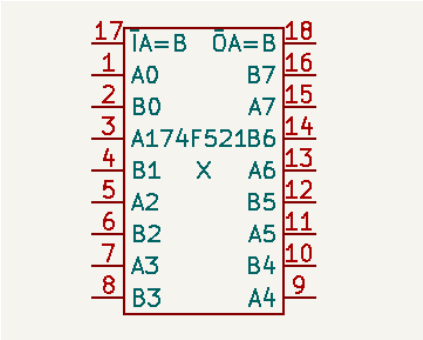


Figure 6.1: Pin Configuration of the 74F521

6.3 Sub Circuit Layout

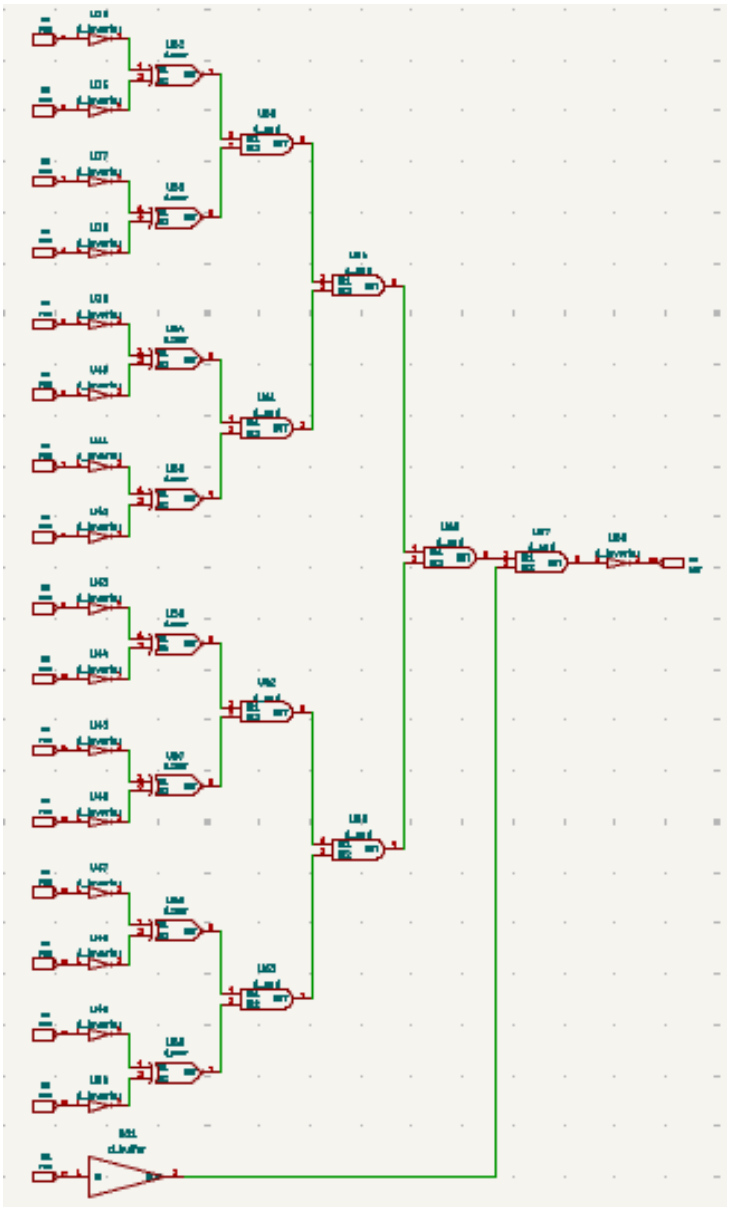


Figure 6.2: Subcircuit Schematic of the 74F521

6.4 Test Circuit

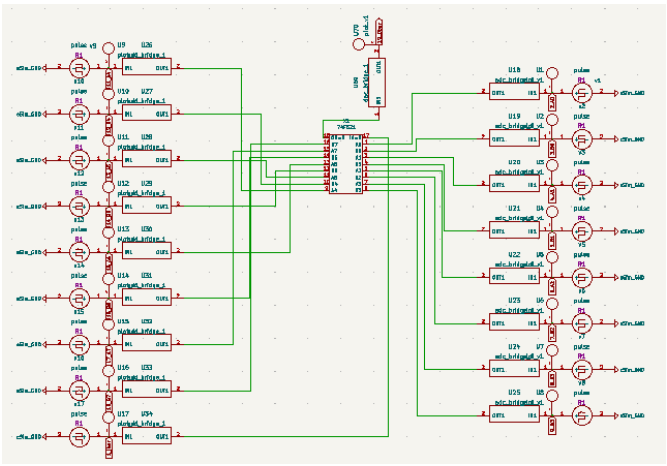
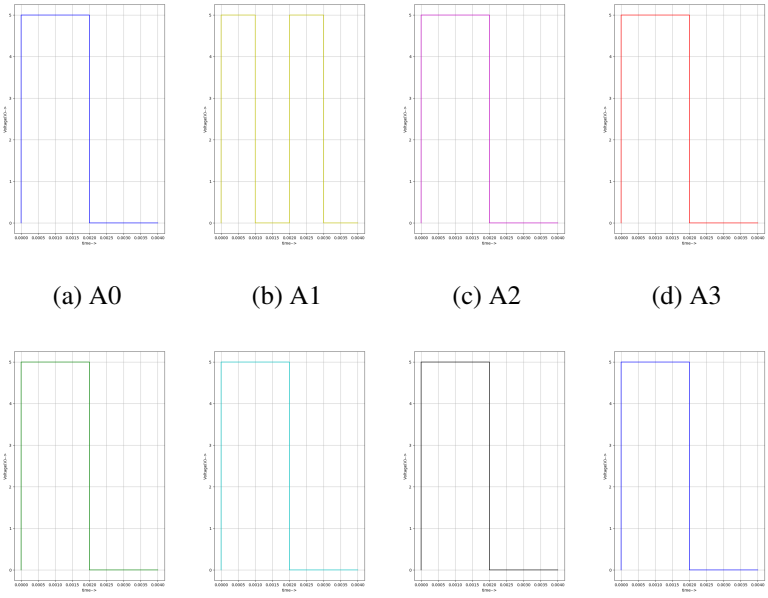


Figure 6.3: Test Circuit of the 74F521

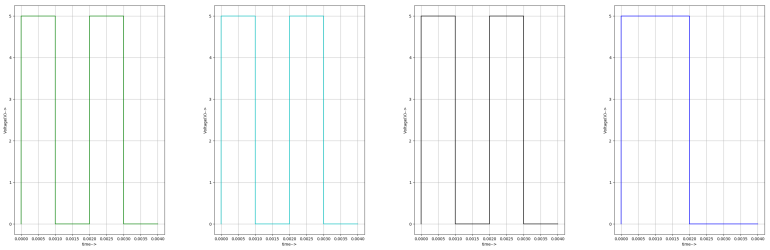
6.5 Input Waveforms



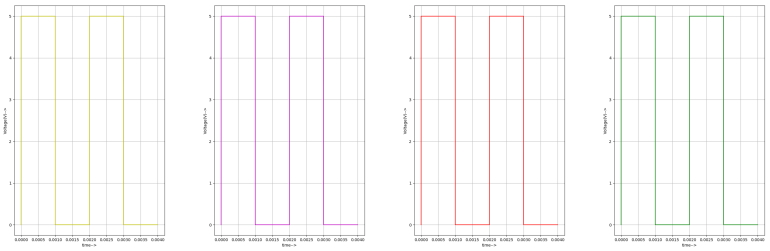
(a) A0 (b) A1 (c) A2 (d) A3

(e) A4 (f) A5 (g) A6 (h) A7

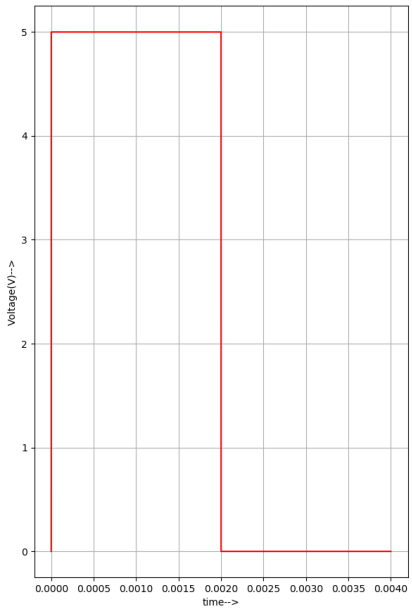
Figure 6.4: Input Waveforms of 74F521 (Inputs A0-A7)



(a) B0 (b) B1 (c) B2 (d) B3



(e) B4 (f) B5 (g) B6 (h) B7



(i) I BAR A=B

Figure 6.5: Input Waveforms of 74F521 (Inputs B0-B7 and Control)

6.6 Output Waveforms

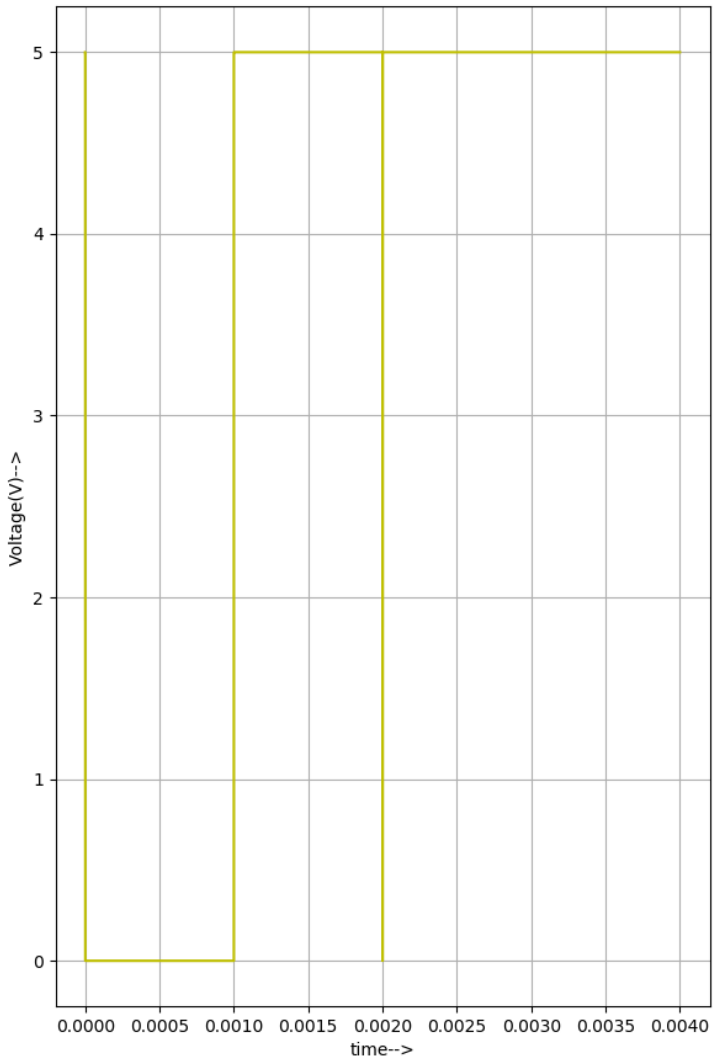


Figure 6.6: Output Waveform of the 74F521 (Active Low Equality Output)

Chapter 7

CD4519BM

7.1 Description

The CD4519BM is a CMOS 4-bit AND/OR selector that performs logical operations on two 4-bit input words. It can be configured to select either the AND or OR function between corresponding bits of the two input words (X and Y), or to pass one of the inputs directly to the output based on the select lines A and B. This versatility makes it useful for arithmetic logic units, data manipulation, and conditional logic operations in digital systems.

7.2 Pin Diagram

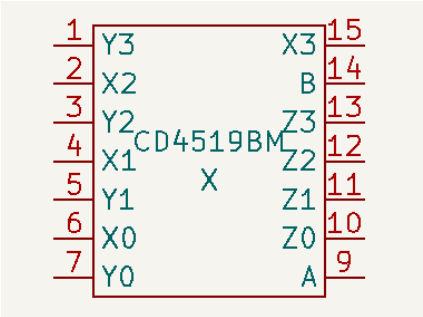


Figure 7.1: Pin Configuration of the CD4519BM

7.3 Sub Circuit Layout

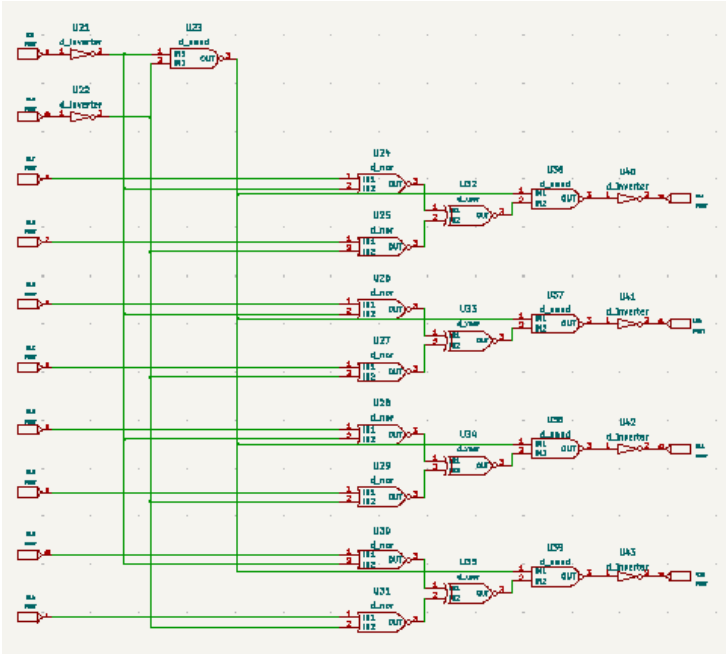


Figure 7.2: Subcircuit Schematic of the CD4519BM

7.4 Test Circuit

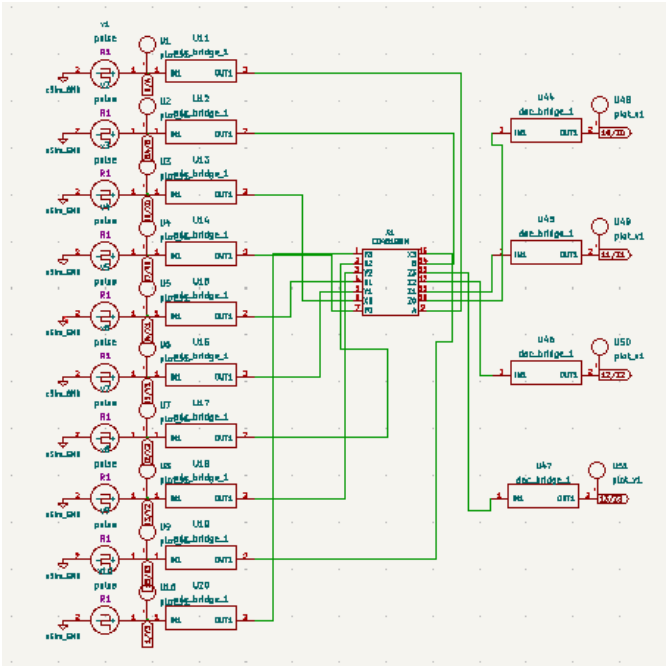
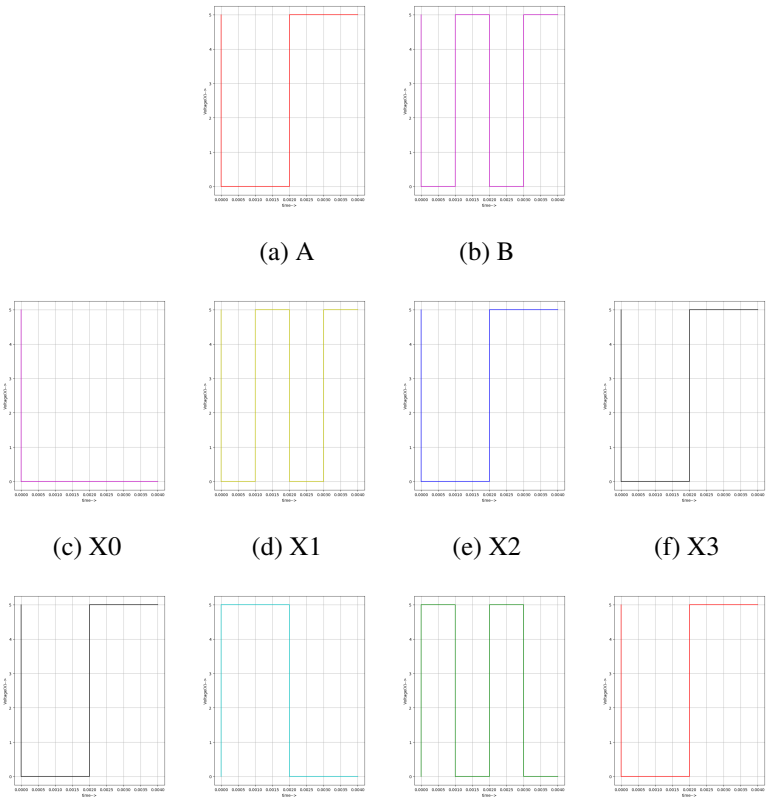


Figure 7.3: Test Circuit of the CD4519BM

7.5 Input Waveforms



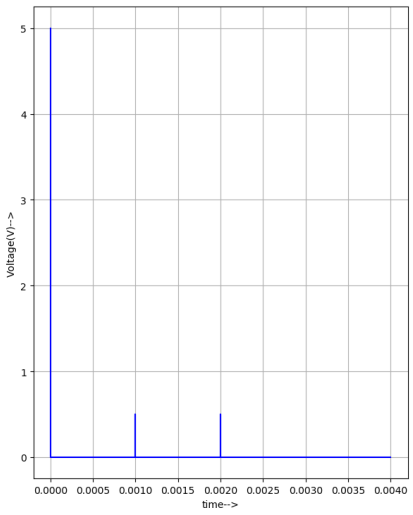
(a) A (b) B

(c) X0 (d) X1 (e) X2 (f) X3

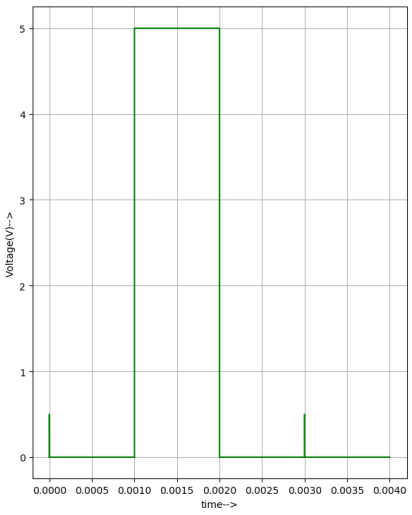
(g) Y0 (h) Y1 (i) Y2 (j) Y3

Figure 7.4: Input Waveforms of CD4519BM

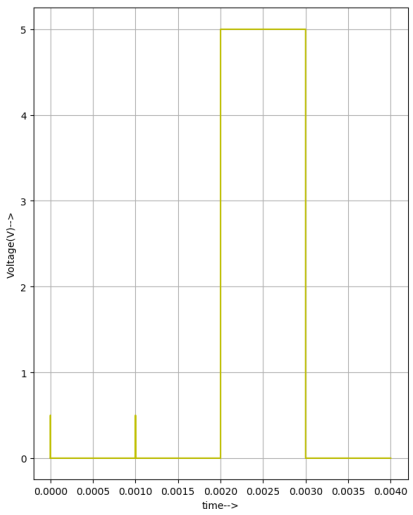
7.6 Output Waveforms



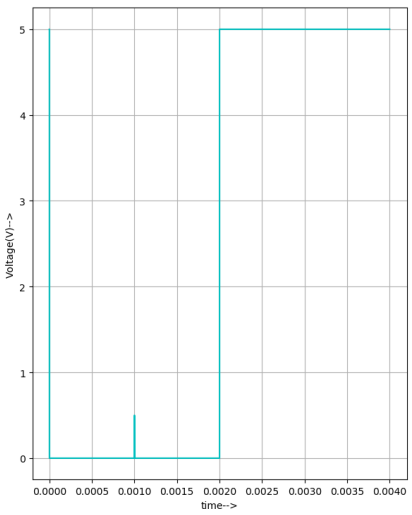
(a) Z0



(b) Z1



(c) Z2



(d) Z3

Figure 7.5: Output Waveforms of the CD4519BM

Chapter 8

74S140

8.1 Description

The 74S140 is a dual 4-input NAND gate with Schottky-clamped transistors for high-speed operation. Each gate performs the logical NAND function on four inputs: first gate with inputs 1A, 1B, 1C, 1D produCing output 1Y; second gate with inputs 2A, 2B, 2C, 2D produCing output 2Y. The output is low only when all four inputs are high. The Schottky clamp diodes prevent transistor saturation, enabling faster switching speeds compared to standard TTL.

8.2 Pin Diagram

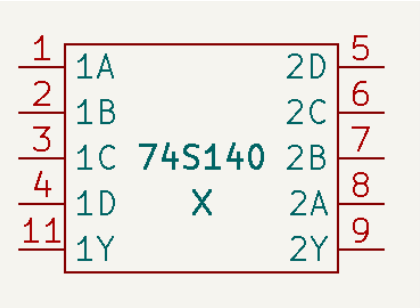


Figure 8.1: Pin Configuration of the 74S140

8.3 Sub Circuit Layout

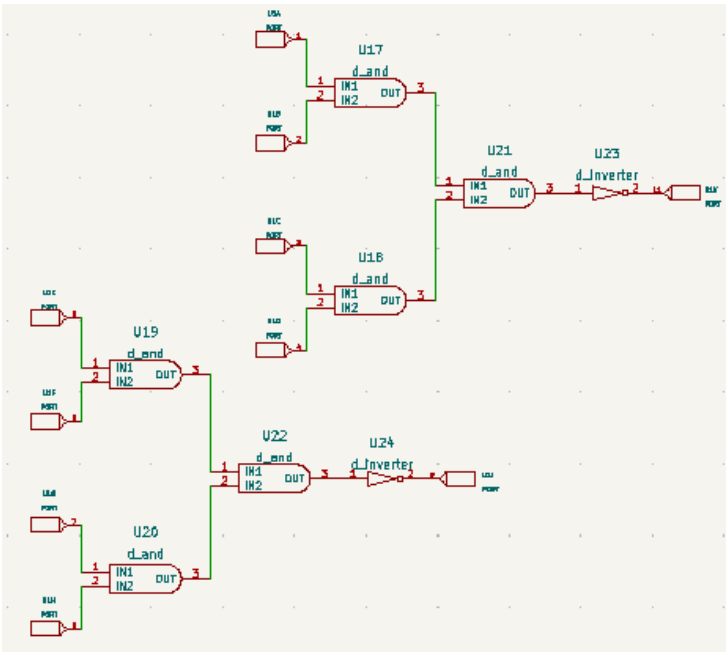


Figure 8.2: Subcircuit Schematic of the 74S140

8.4 Test Circuit

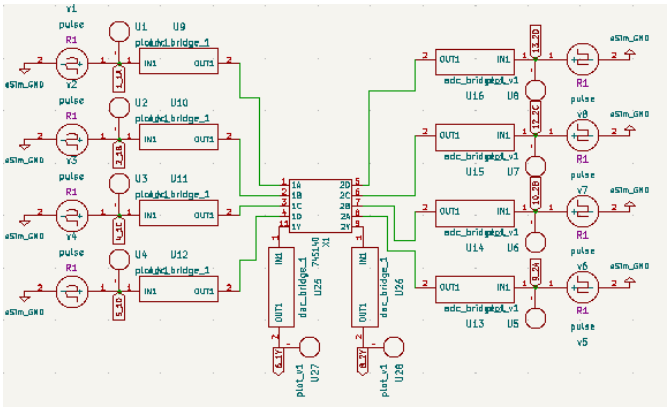
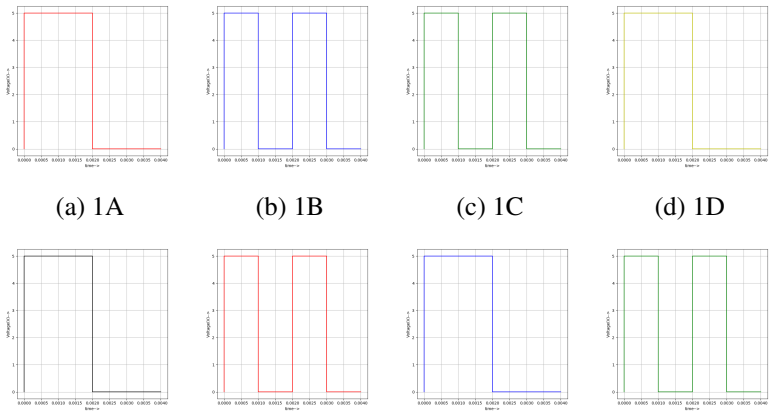


Figure 8.3: Test Circuit of the 74S140

8.5 Input Waveforms

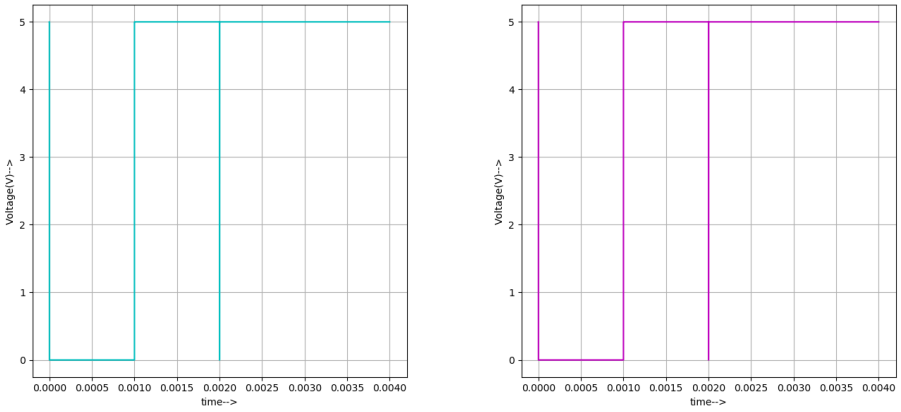


(a) 1A (b) 1B (c) 1C (d) 1D

(e) 2A (f) 2B (g) 2C (h) 2D

Figure 8.4: Input Waveforms of 74S140

8.6 Output Waveforms



(a) 1Y (b) 2Y

Figure 8.5: Output Waveforms of the 74S140

Chapter 9

SN7444A

9.1 Description

The SN7444A is a Gray-to-Decimal decoder that converts a 4-bit Gray code input (A, B, C, D) into a 1-of-10 decimal output. Gray code is a binary numeral system where two successive values differ in only one bit, making it useful for error correction, shaft encoders, and communication systems. This decoder accepts a 4-bit Gray code word and activates the corresponding decimal output line (0 through 9), with all outputs high for invalid Gray code inputs.

9.2 Pin Diagram

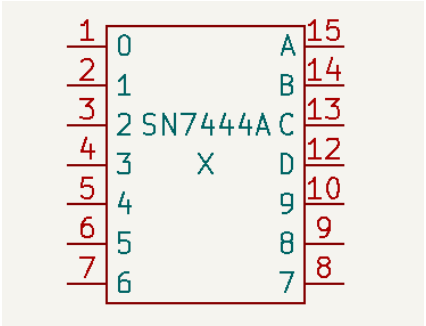


Figure 9.1: Pin Configuration of the SN7444A

9.3 Sub Circuit Layout

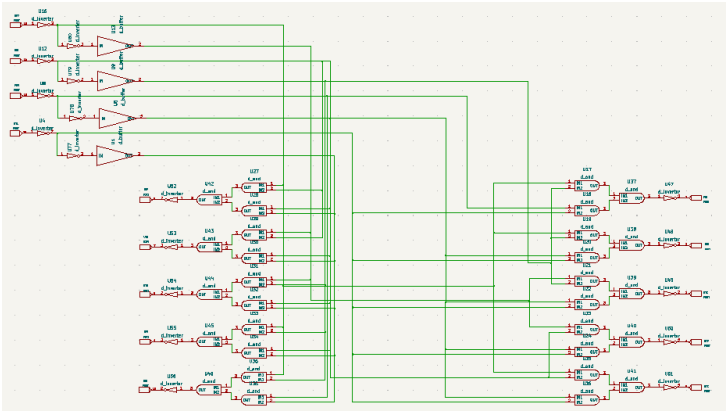


Figure 9.2: Subcircuit Schematic of the SN7444A

9.4 Test Circuit

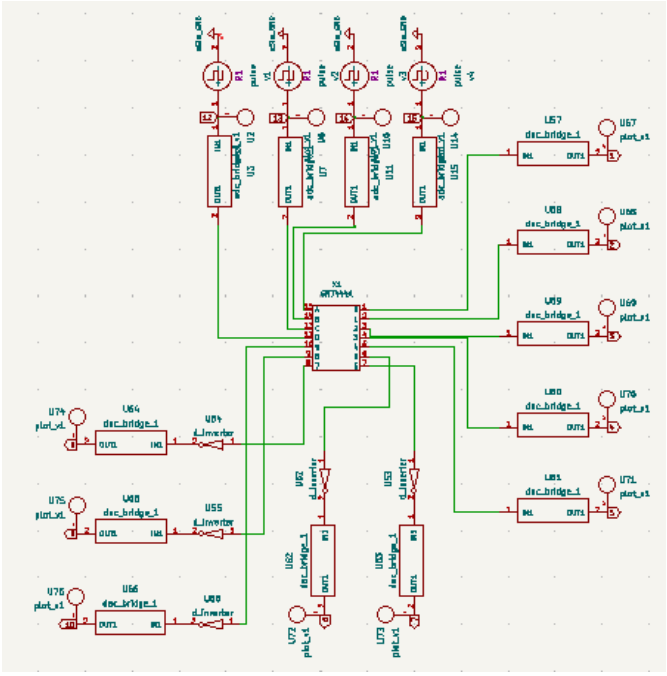
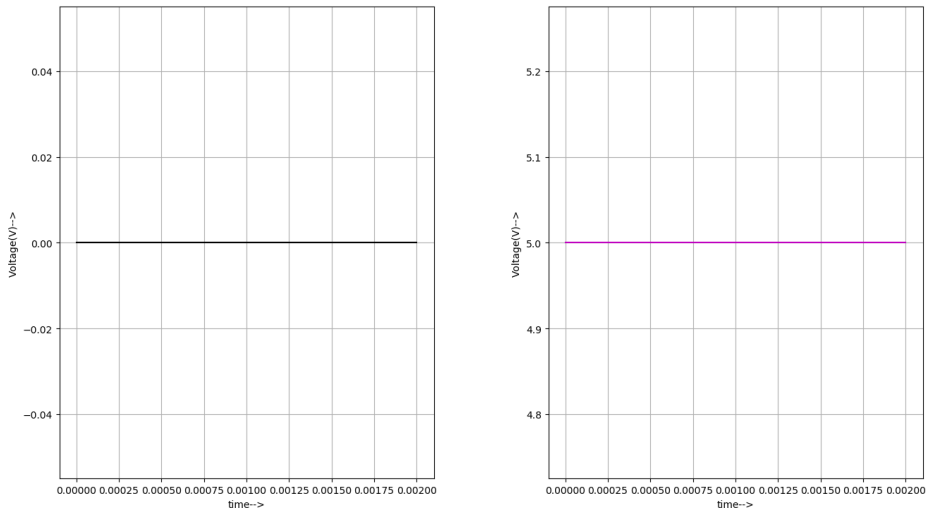


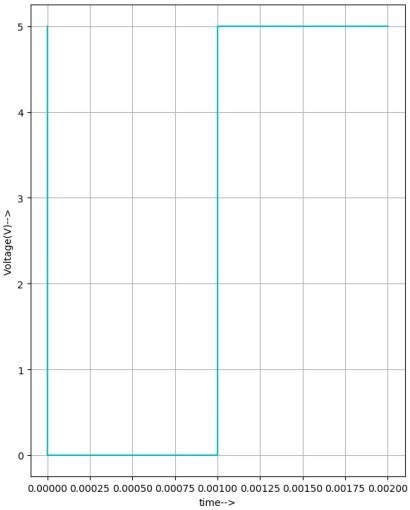
Figure 9.3: Test Circuit of the SN7444A

9.5 Input Waveforms

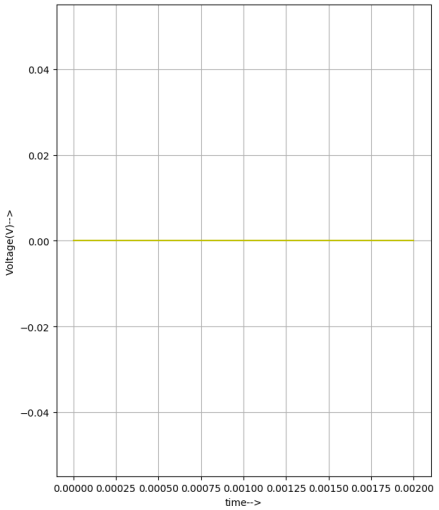


(a) A

(b) B



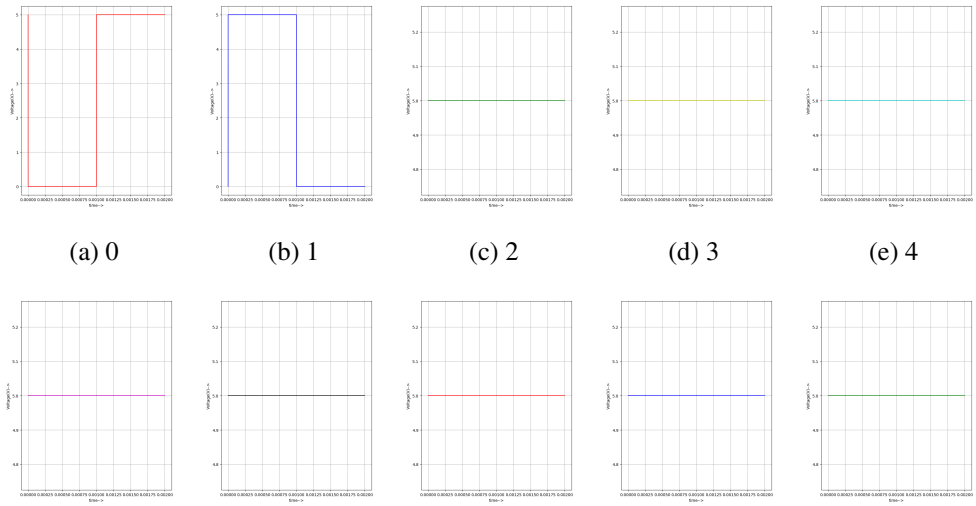
(c) C



(d) D

Figure 9.4: Input Waveforms of SN7444A

9.6 Output Waveforms



(a) 0 (b) 1 (c) 2 (d) 3 (e) 4

(f) 5 (g) 6 (h) 7 (i) 8 (j) 9

Figure 9.5: Output Waveforms for SN7444A

Chapter 10

SN7443A

10.1 Description

The SN7443A is an Excess-3-to-Decimal decoder. It converts a 4-bit Excess-3 binary code input into a 1-of-10 decimal output. Excess-3 code is a self-complementing binary code used in some arithmetic systems. The decoder activates one of the ten decimal outputs (0-9) corresponding to the valid Excess-3 input, providing a direct interface between Excess-3 logic and decimal displays or controls.

10.2 Pin Diagram

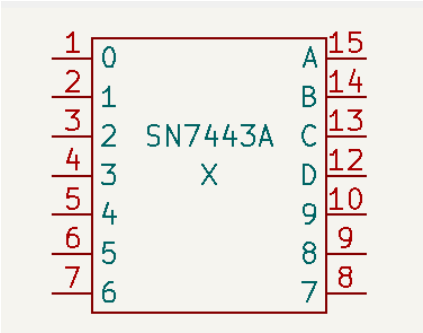


Figure 10.1: Pin Configuration of the SN7443A

10.3 Sub Circuit Layout

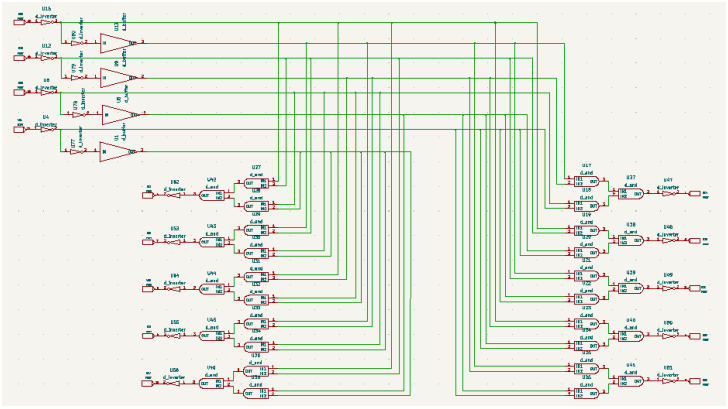


Figure 10.2: Subcircuit Schematic of the SN7443A

10.4 Test Circuit

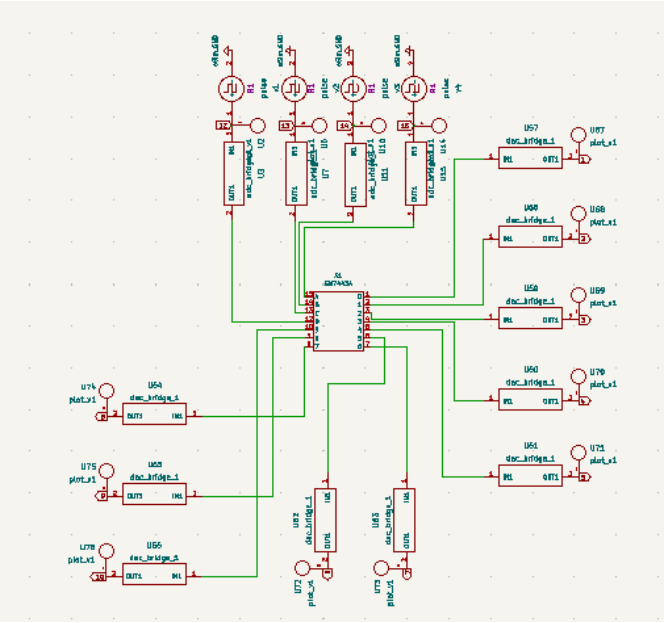
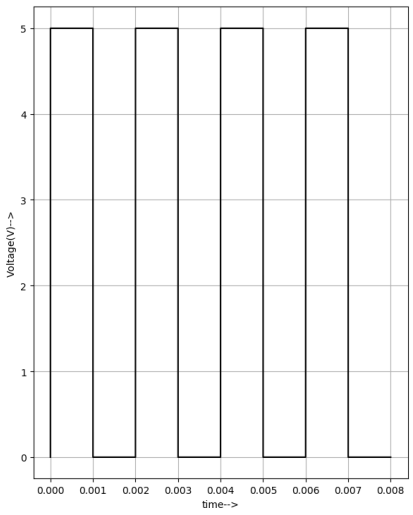
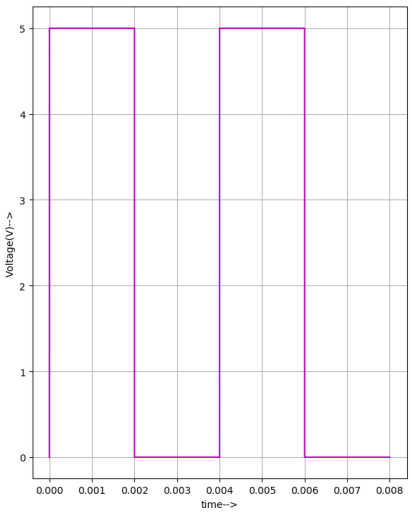


Figure 10.3: Test Circuit of the SN7443A

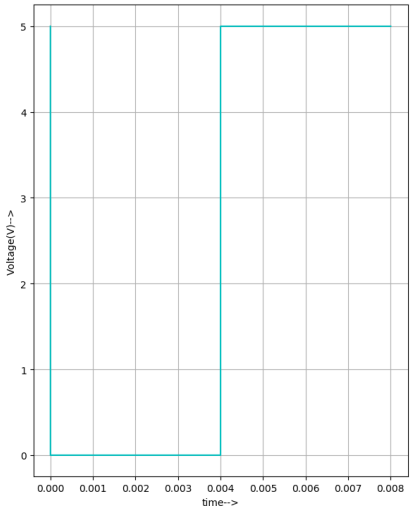
10.5 Input Waveforms



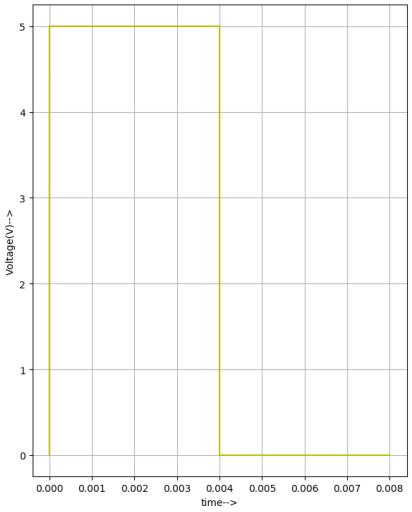
(a) A



(b) B



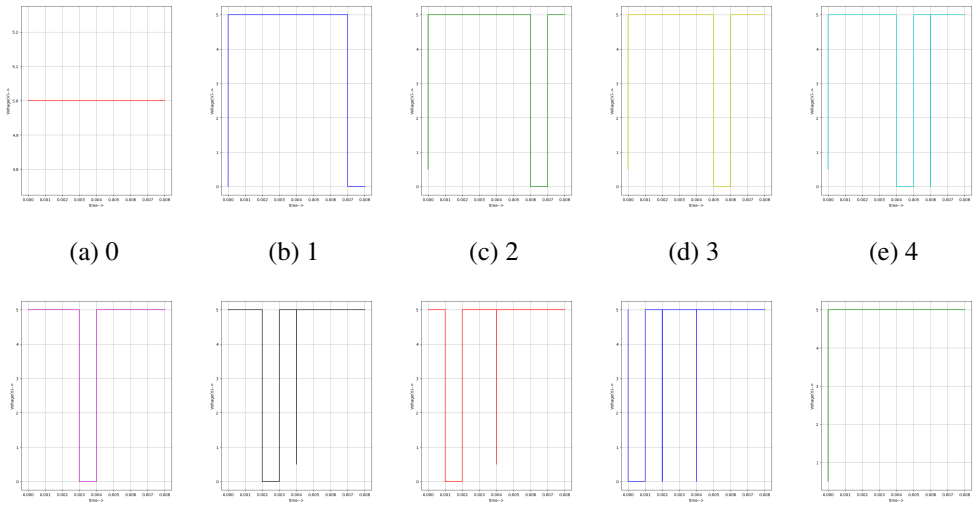
(c) C



(d) D

Figure 10.4: Input Waveforms of SN7443A

10.6 Output Waveforms



(a) 0 (b) 1 (c) 2 (d) 3 (e) 4

(f) 5 (g) 6 (h) 7 (i) 8 (j) 9

Figure 10.5: Output Waveforms for SN7443A

Chapter 11

74F64

11.1 Description

The 74F64 is a 4-2-3-2-input AND-OR-INVERT gate. It performs the logical operation Y = invert ((A0.A1.A2.A3) + (B0.B1) + (C0.C1.C2) + (D0.D1)). This complex logic function allows for efficient implementation of sum-of-products logic with an inverted output, reducing the chip count in complex combinatorial circuits.

11.2 Pin Diagram

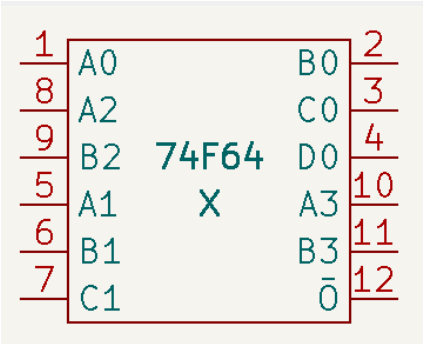


Figure 11.1: Pin Configuration of the 74F64

11.3 Sub Circuit Layout

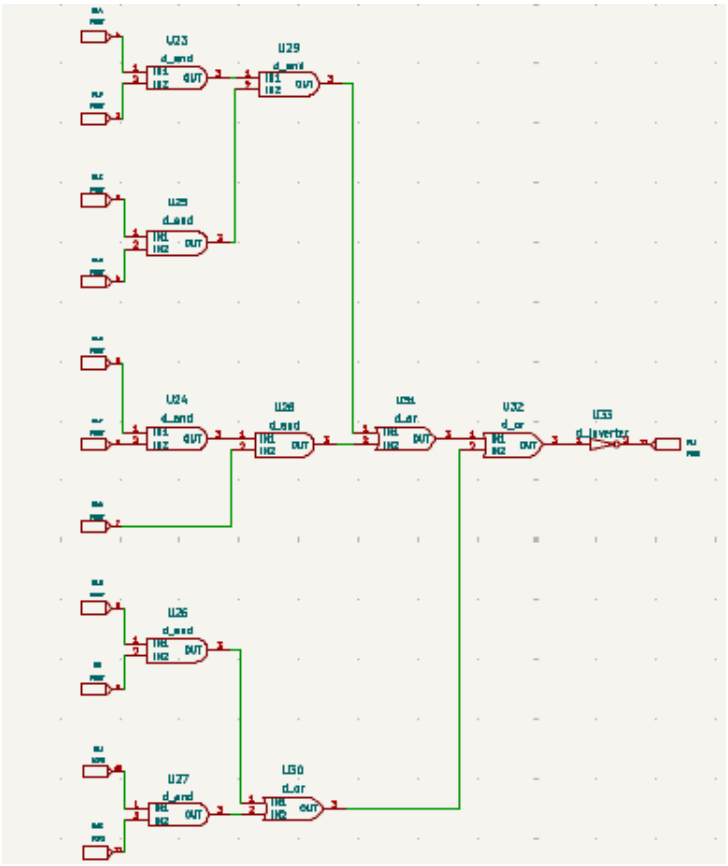


Figure 11.2: Subcircuit Schematic of the 74F64

11.4 Test Circuit

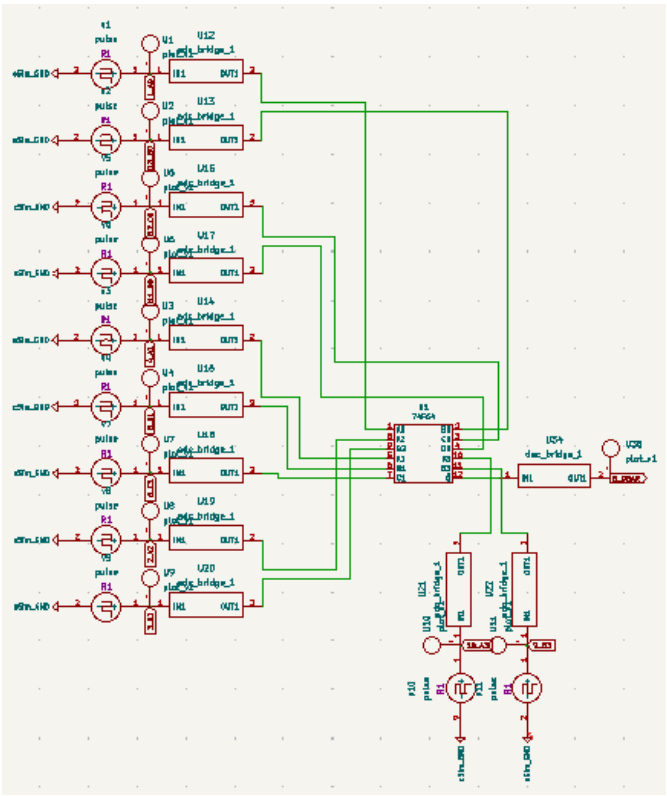
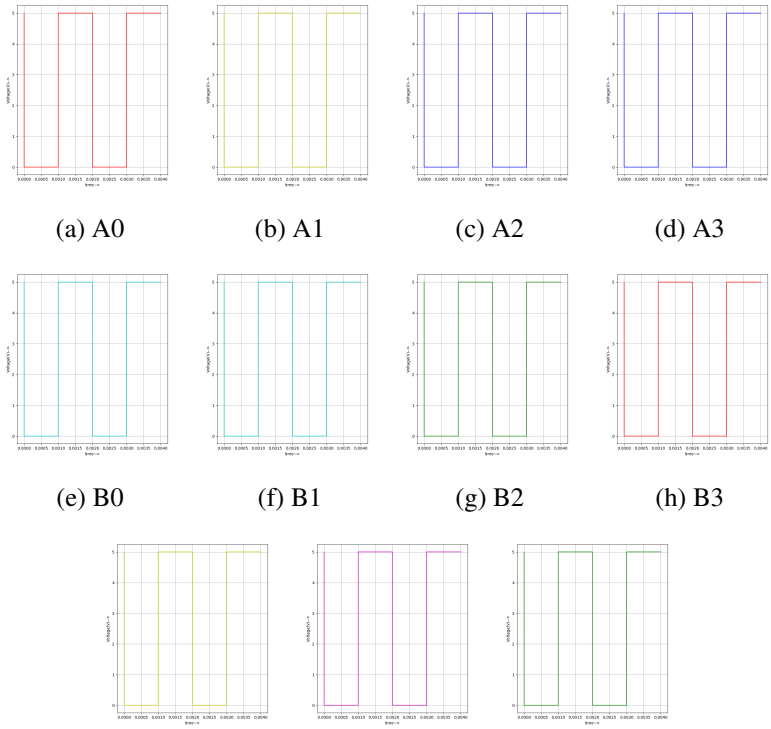


Figure 11.3: Test Circuit of the 74F64

11.5 Input Waveforms



(a) A0 (b) A1 (c) A2 (d) A3

(e) B0 (f) B1 (g) B2 (h) B3

(i) C0 (j) C1 (k) D0

Figure 11.4: Input Waveforms of 74F64

11.6 Output Waveform

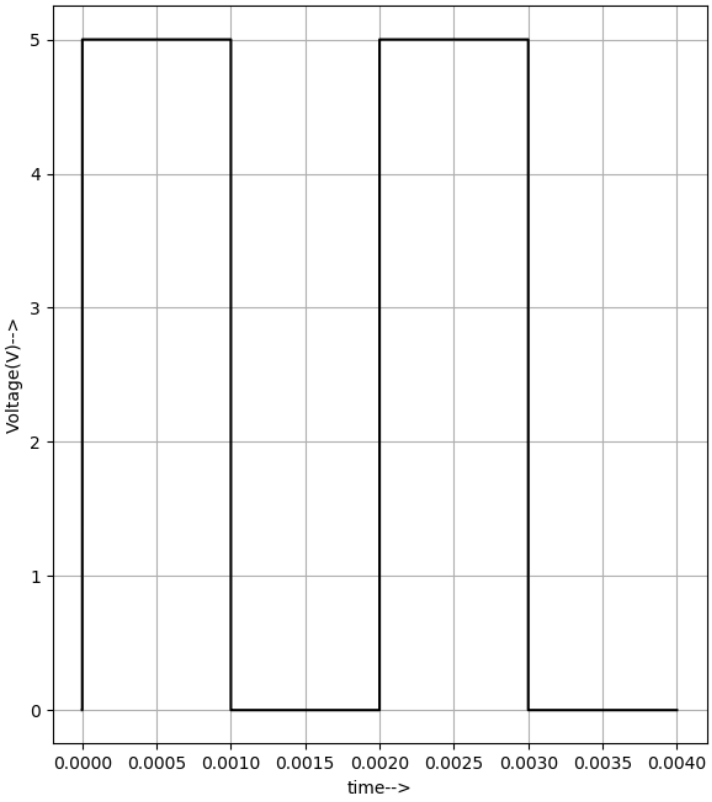


Figure 11.5: Output Waveform of the 74F64

Chapter 12

74133

12.1 Description

The 74133 is a 13-input NAND gate. It produces a logic low output only when all thirteen inputs are at a logic high level. If any single input is low, the output remains high. This device is useful for detecting the simultaneous presence of multiple status signals or decoding large address ranges.

12.2 Pin Diagram

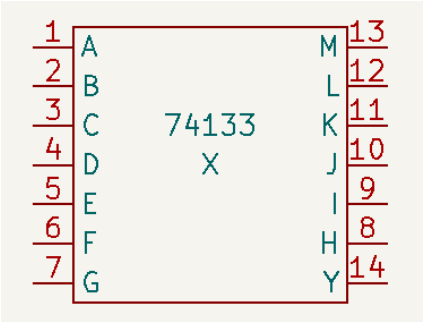


Figure 12.1: Pin Configuration of the 74133

12.3 Sub Circuit Layout

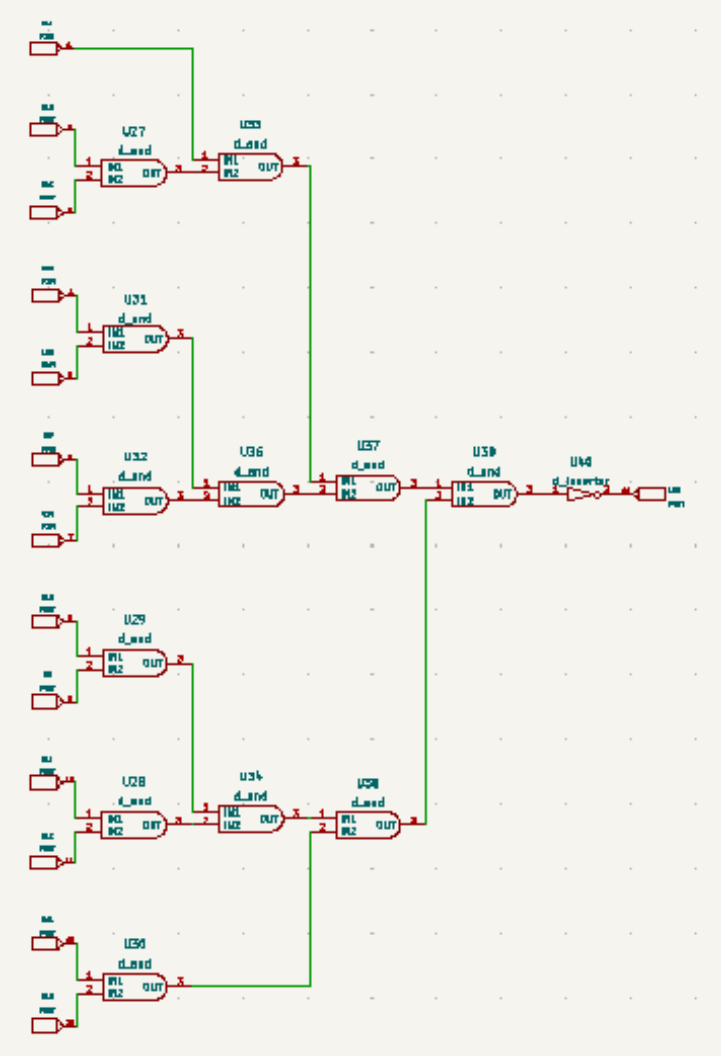


Figure 12.2: Subcircuit Schematic of the 74133

12.4 Test Circuit

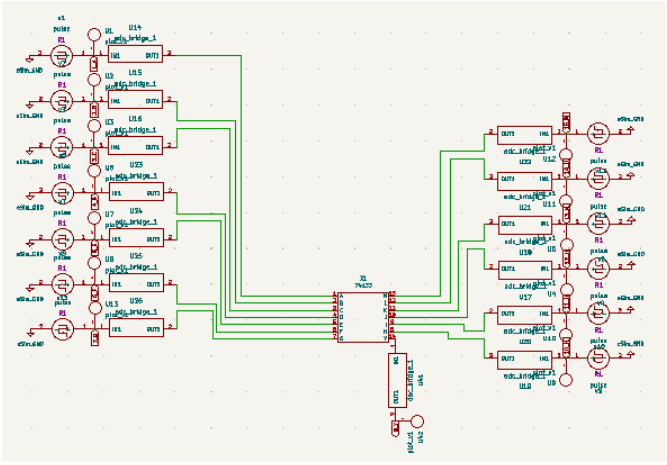
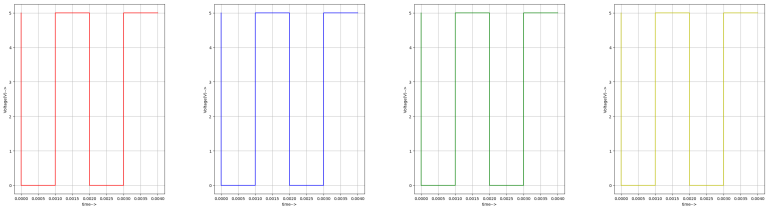
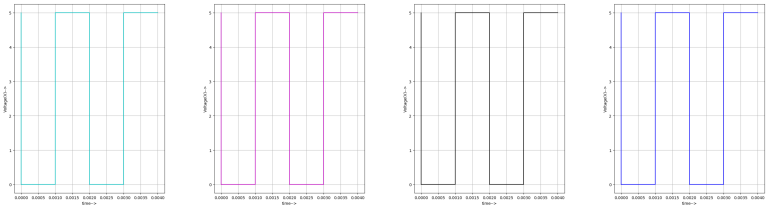


Figure 12.3: Test Circuit of the 74133

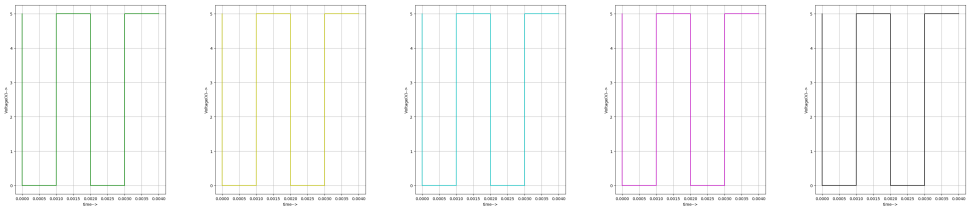
12.5 Input Waveforms



(a) A (b) B (c) C (d) D



(e) E (f) F (g) G (h) H



(i) I (j) J (k) K (l) L (m) M

Figure 12.4: Input Waveforms of 74133

12.6 Output Waveform

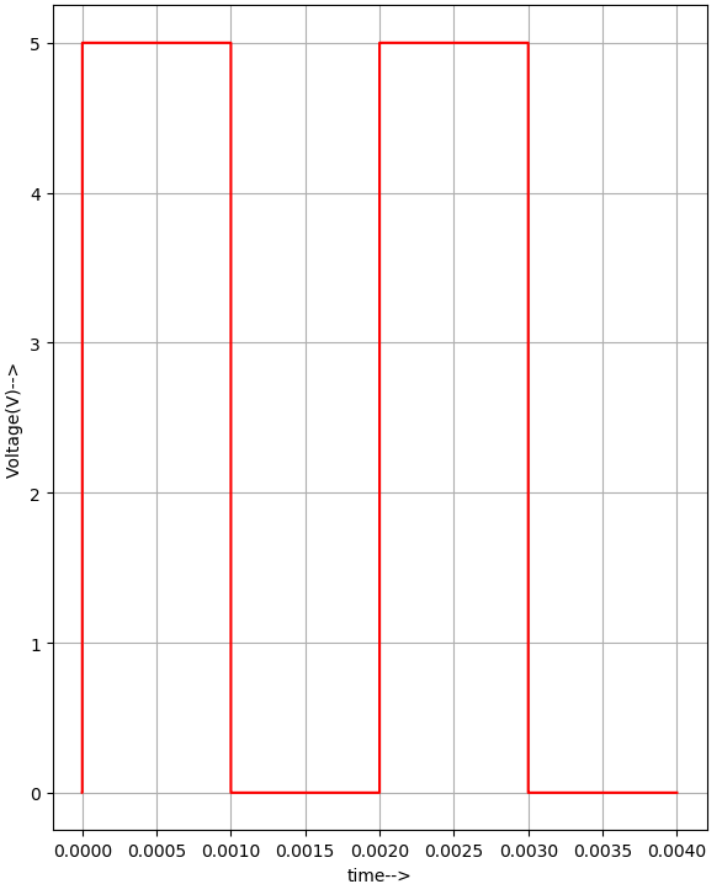


Figure 12.5: Output Waveform of the 74133

Chapter 13

74S51

13.1 Description

The 74S51 is a dual 2-wide 2-input AND-OR-INVERT gate. Each gate consists of two 2-input AND gates feeding into a NOR structure. The output Y is low if (A.B) OR (C.D) is true. It features Schottky-clamped transistors for high-speed switching.

13.2 Pin Diagram

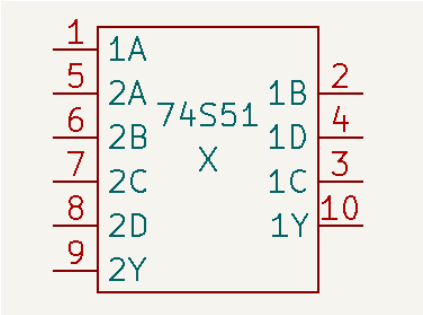


Figure 13.1: Pin Configuration of the 74S51

13.3 Sub Circuit Layout

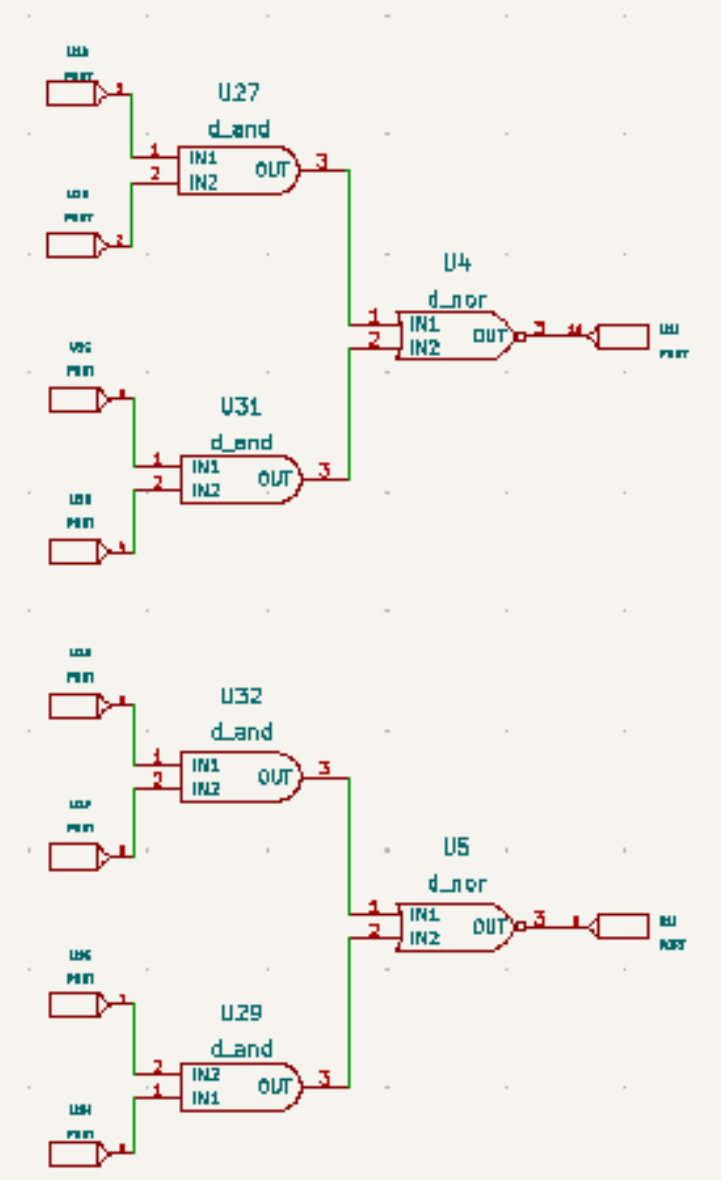


Figure 13.2: Subcircuit Schematic of the 74S51

13.4 Test Circuit

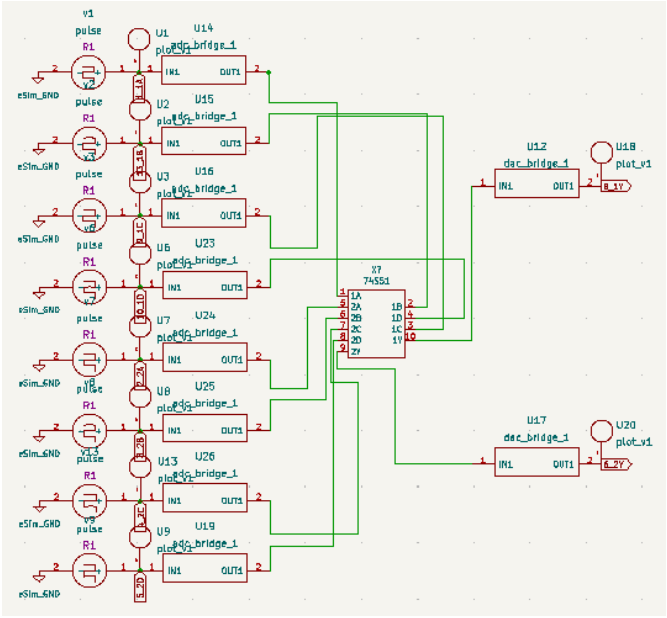
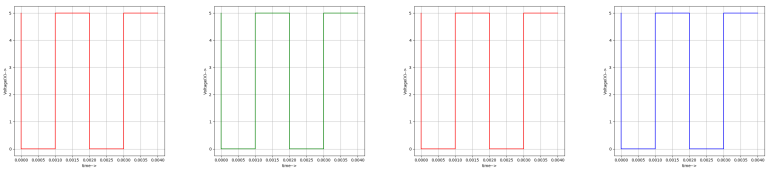
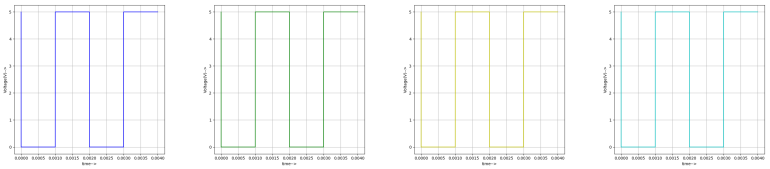


Figure 13.3: Test Circuit of the 74S51

13.5 Input Waveforms



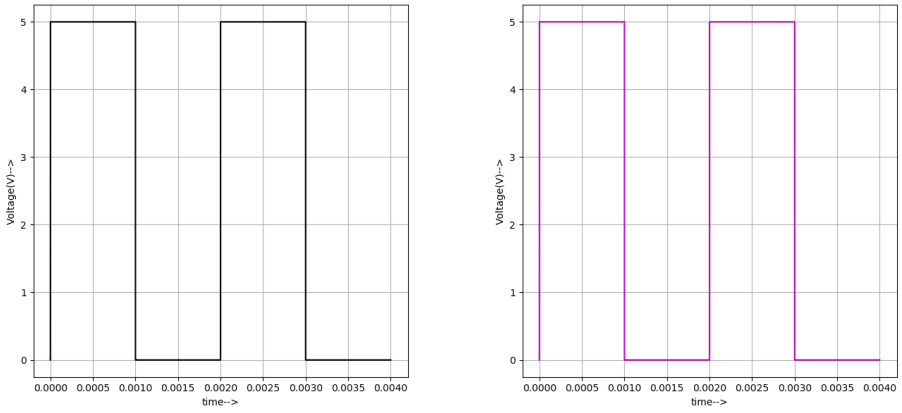
(a) 1A (b) 1B (c) 1C (d) 1D



(e) 2A (f) 2B (g) 2C (h) 2D

Figure 13.4: Input Waveforms of 74S51

13.6 Output Waveforms



(a) 1Y (b) 2Y

Figure 13.5: Output Waveforms of the 74S51

Chapter 14

Conclusion and Future Scope

The project achieved its objective of developing a wide range of subcircuits for Digital Integrated Circuits, with each IC model meticulously crafted based on the specifications provided in their official datasheets. Through rigorous testing and verification using corresponding test circuits, these IC models were validated for accuracy and functionality. The components developed under this fellowship encompass fundamental digital circuit elements such as Arithmetic Logic Units (ALUs), Data Selectors/Multiplexers, Comparators, Logic Selectors, Gates, Decoders, and Complex Logic Functions.

The components developed include the 74HC283, 74LS352, 74F521, CD4519BM, 74S140, SN7444A, SN7443A, 74F64, 74133, and 74S51.

Each IC model was thoroughly tested with appropriate input stimulus, and the output waveforms were captured and verified against datasheet specifications. The input and output plots for each IC demonstrate correct logical functionality, proper timing characteristics, and accurate propagation delays.

These models are now ready for integration into the eSim subcircuit library, providing a robust resource for developers, students, and researchers. The inclusion of these models in the eSim library will significantly enhance the tool's capabilities, enabling users to easily incorporate these fundamental ICs into their own projects and circuit designs.

Looking ahead, this project sets the foundation for the continued expansion of eSim's device model library. We anticipate that more such ready-to-use IC models will be developed, broadening the scope of available components and further empowering the eSim community. This ongoing development will not only aid in academic and research endeavors but also contribute to the growing ecosystem of open-source electronic design automation (EDA) tools.

Chapter 15

Circuits Contribution

This chapter lists all the Integrated Circuits (ICs) contributed during the fellowship.

15.1 List of ICs Contributed

1. **74HC283** - 4-Bit Binary Full Adder with Fast Carry
    - Inputs: A0, A1, A2, A3, B0, B1, B2, B3, Cin
    - Outputs: S0, S1, S2, S3, Cout
2. **74LS352** - Dual 4-Line to 1-Line Data Selectors/Multiplexers
    - Inputs: 1C0-1C3, 2C0-2C3, A, B, G1, G2
    - Outputs: 1Y, 2Y
3. **74F521** - 8-Bit Identity Comparator
    - Inputs: A0-A7, B0-B7, I BAR A=B
    - Outputs: O BAR A=B
4. **CD4519BM** - 4-Bit AND/OR Selector
    - Inputs: A, B, X0-X3, Y0-Y3
    - Outputs: Z0, Z1, Z2, Z3
5. **74S140** - Dual 4-input NAND Gate
    - Inputs: 1A-1D, 2A-2D
    - Outputs: 1Y, 2Y
6. **SN7444A** - Gray-to-Decimal Decoder
    - Inputs: A, B, C, D
    - Outputs: 0-9
7. **SN7443A** - Excess-3-to-Decimal Decoder
    - Inputs: A, B, C, D
    - Outputs: 0-9
8. **74F64** - 4-2-3-2-Input AND-OR-INVERT Gate
    - Inputs: A, B, C, D groups

- Outputs: Y

9. **74133** - 13-input NAND Gate
    - Inputs: A-M
    - Outputs: Y
10. **74S51** - 2-wide 2-input AND-OR-INVERT Gate
    - Inputs: 1A-1D, 2A-2D
    - Outputs: 1Y, 2Y

Bibliography

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[6] Texas Instruments, CD4519BM Datasheet https://www.ti.com/lit/ds/symlink/cd4519b.pdf

[7] Texas Instruments, 74S140 Datasheet https://www.ti.com/lit/ds/symlink/sn74s140.pdf

[8] Texas Instruments, SN7444A Datasheet https://www.ti.com/lit/ds/symlink/sn7444a.pdf

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[11] Texas Instruments, 74133 Datasheet https://www.ti.com/lit/ds/symlink/sn74133.pdf

[12] Texas Instruments, 74S51 Datasheet https://www.ti.com/lit/ds/symlink/sn74s51.pdf