eSim Semester Long Internship Autumn 2025

On

Adding ICs as Subcircuits in eSim Library

Submitted by

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Acknowledgment

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This internship has been an enriching learning experience, allowing me to work closely with open-source EDA tools, develop IC subcircuits in eSim, and gain exposure to real-world circuit modeling and simulation workflows. The knowledge acquired during this period will undoubtedly support my future academic and professional pursuits.

I would also like to thank the entire FOSSEE team for their coordination, assistance, and timely interactions at various stages of this work. Their collective efforts ensured smooth workflow, resource accessibility, and effective project execution.

Contents

Chapter 1

Introduction

1.1 FOSSEE

FOSSEE, which stands for Free/Libre and Open Source Software for Education, is an organization based at IIT Bombay [1]. It is a remarkable initiative aimed at promoting the use of open-source software in education and research. It was established with the mission to reduce dependency on proprietary software and to encourage the adoption of open-source alternatives. FOSSEE offers a wide range of tools and resources that cater to various academic and professional needs.

It provides comprehensive documentation, tutorials, workshops, and hands-on training sessions to empower students, educators, and professionals to leverage open-source software for their projects and coursework. The organization's commitment to fostering a collaborative and inclusive environment has significantly contributed to the democratization of technology and has opened up new avenues for innovation and learning.

1.2 eSim

eSim, created by the FOSSEE project at IIT Bombay [2], is a versatile open-source software tool for circuit design and simulation. It combines various open-source software packages into one cohesive platform, making it easier to design, simulate, and analyze electronic circuits. This tool is particularly useful for students, educators, and professionals who need an affordable and accessible alternative to proprietary software.

eSim offers features for schematic creation, circuit simulation, and PCB design, and includes an extensive library of components. The Subcircuit feature is a significant enhancement, enabling users to design complex circuits by integrating simpler subcircuits. Through eSim, FOSSEE promotes the use of open-source solutions in engineering education and professional fields, encouraging innovation and collaboration.

1.3 NgSpice

NgSpice is an open-source SPICE simulator for electric and electronic circuits. It can simulate various circuit elements, including JFETs, bipolar and MOS transistors, passive elements (R, L, C), diodes and other devices, all interconnected in a netlist.

Digital circuits are also simulated, ranging from single gates to complex circuits, including combinations of analog, digital, and mixed-signal circuits. NgSpice offers a wealth of device models for active, passive, analog, and digital elements. Users input their circuits as netlists, and the output is one or more graphs of currents, voltages, and other electrical quantities, or saved in a data file.

1.4 Makechip

Makechip is a platform that offers convenient and accessible tools for digital circuit design. It provides both browser-based and desktop-based environments for coding, compiling, simulating, and debugging Verilog designs. Makechip supports a combination of open-source and proprietary tools, ensuring a comprehensive range of capabilities.

Users can simulate Verilog/SystemVerilog/Transaction-Level Verilog code in Makechip. eSim is interfaced with Makechip using a Python-based application called Makechip-App, which launches the Makechip IDE. Makechip aims to make circuit design easy and enjoyable for users of all skill levels. The platform provides a userfriendly interface, intuitive workflows, and a range of helpful features that simplify the design process and enhance the overall user experience.

The main drawback of these open-source tools is that they are not comprehensive. While some are capable of PCB design (e.g., KiCad), others focus on simulations (e.g., gEDA). To the best of our knowledge, there is no open-source software that combines circuit design, simulation, and layout design in one platform. eSim addresses this gap by integrating all these capabilities.

Chapter 2

Features of eSim

The objective behind the development of eSim is to provide an open-source EDA solution for electronics and electrical engineers. The software is capable of performing schematic creation, PCB design, and circuit simulation (analog, digital, and mixedsignal). It also provides facilities to create new models and components. Thus, eSim offers the following features:

1. Schematic Creation: eSim provides an easy-to-use graphical interface for drawing circuit schematics, making it accessible for users of all levels. Users can drag and drop components from the library onto the schematic, simplifying the design process. Comprehensive editing tools allow for easy modification of schematics, including moving, rotating, and labeling components.

2. Circuit Simulation: eSim supports SPICE (Simulation Program with Integrated Circuit Emphasis), a standard for simulating analog and digital circuits. Users can perform various types of analysis such as transient, AC, and DC, providing insights into circuit behavior over time and frequency. An integrated waveform viewer helps visualize simulation results, aiding in the analysis and debugging of circuit designs.

3. PCB Design: The PCB layout editor allows users to place components and route traces with precision. eSim includes DRC (Design Rule Check) capabilities to ensure that the PCB design adheres to manufacturing constraints and electrical rules. Users can generate Gerber files, which are standard for PCB fabrication, directly from their designs.

4. Subcircuit Feature: This feature enables users to create complex circuits by integrating smaller, simpler subcircuits, promoting modular and hierarchical design approaches. Subcircuits can be reused in different projects, saving time and effort in redesigning common circuit elements.

5. Open Source Integration: eSim integrates several open-source tools like KiCad, NgSpice, and GHDL, providing a comprehensive suite for electronic design automation. Being open-source, eSim is free to use, making advanced circuit design tools accessible without the need for expensive licenses.

Chapter 3

Problem Statement

To design and develop various analog and digital integrated circuit models in the form of sub-circuits using device model files already present in the eSim library. These IC models should be useful for future circuit design purposes by developers and users once they are successfully integrated into the eSim sub-circuit library.

3.1 Approach

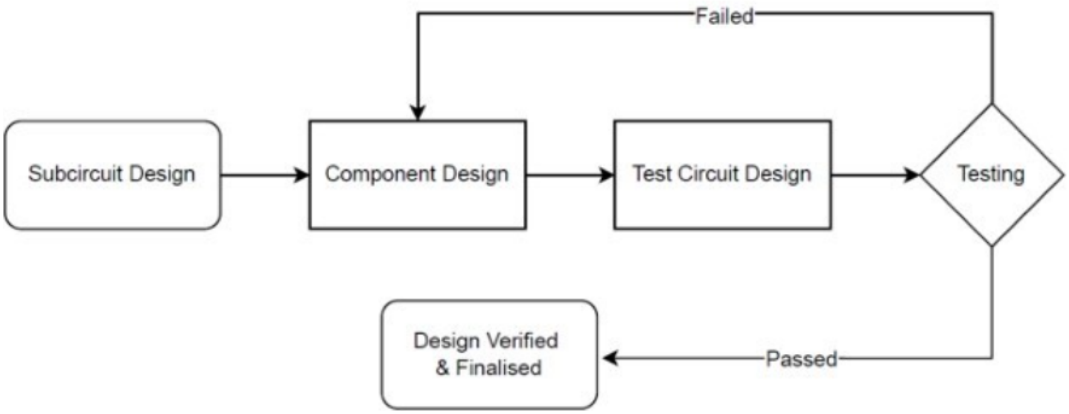

Figure 3.1: Flowchart of IC Design Approach Followed

Our approach to implementing the problem statement involved a systematic process, leveraging datasheets from leading Integrated Circuit (IC) manufacturers such as Texas Instruments, Analog Devices, and NXP Semiconductors. We focused on selecting ICs with diverse functionalities, including precision amplifiers, comparators, encoders, and audio amplifiers. The process is outlined in the following steps:

1. Analyzing Datasheets: The first step involved an in-depth review of datasheets for various analog and digital ICs. We aimed to identify circuits suitable for implementation in eSim that were not already present in the eSim library. This process included scrutinizing the detailed schematics of each IC, evaluating component values, and under-

standing truth tables. The goal was to select ICs that offered unique functionalities or enhancements not yet covered.

2. Subcircuit Creation: After selecting appropriate ICs, we proceeded to model these as sub-circuits within eSim. We utilized the model files available in the eSim device model library and ensured that our designs adhered strictly to the specifications outlined in the official datasheets. This phase also involved creating accurate symbol and pin diagrams for each IC, in accordance with the packaging and pin descriptions provided in the datasheets. This step was crucial for ensuring the fidelity of the subcircuit models.

3. Test Circuit Design: With the sub-circuits created, we then designed and built test circuits based on the datasheets. This step was essential for verifying the functionality of each sub-circuit. We developed a series of test cases and constructed corresponding test circuits to evaluate the performance and accuracy of the implemented IC models.

4. Schematic Testing: Following the construction of test circuits, we conducted simulations to analyze the outputs. This involved generating waveforms and plots to assess the behavior of the circuits. We employed KiCad for converting designs to NgSpice netlists and utilized eSim's simulation features to perform comprehensive testing.

If the simulated outputs deviated from expected results, it signaled potential errors in the schematic. In such instances, we revisited the design phase to identify and correct discrepancies. The iterative process of debugging and re-testing continued until the test cases produced satisfactory results. Once the IC models met the desired performance criteria, they were deemed successful, marking the completion of the design process.

Chapter 4

74HC157

4.1 General Description

The 74HC157 is a quad 2-to-1 line multiplexer/selector from the HC (High-speed CMOS) logic family [3]. It selects one of two 4-bit data inputs and routes it to the output based on a select input. Built using advanced CMOS technology, it provides low power consumption and high-speed operation with TTL-compatible inputs and outputs.

4.2 Key Features

- Quad 2-to-1 line multiplexer
- TTL-compatible logic levels
- High-speed CMOS performance
- Low power consumption
- Common select input for all four multiplexers

4.3 Applications

- Data routing in digital systems
- Input selection in microcontroller circuits
- Signal multiplexing in communication systems
- Logic switching and control applications

4.4 Subcircuit

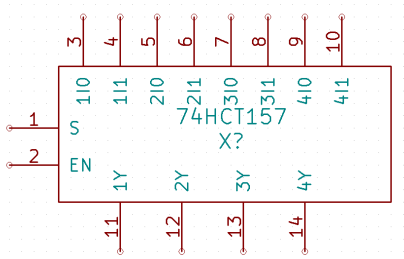

Figure 4.1: Subcircuit of 74HC157

4.5 Subcircuit Schematic Diagram

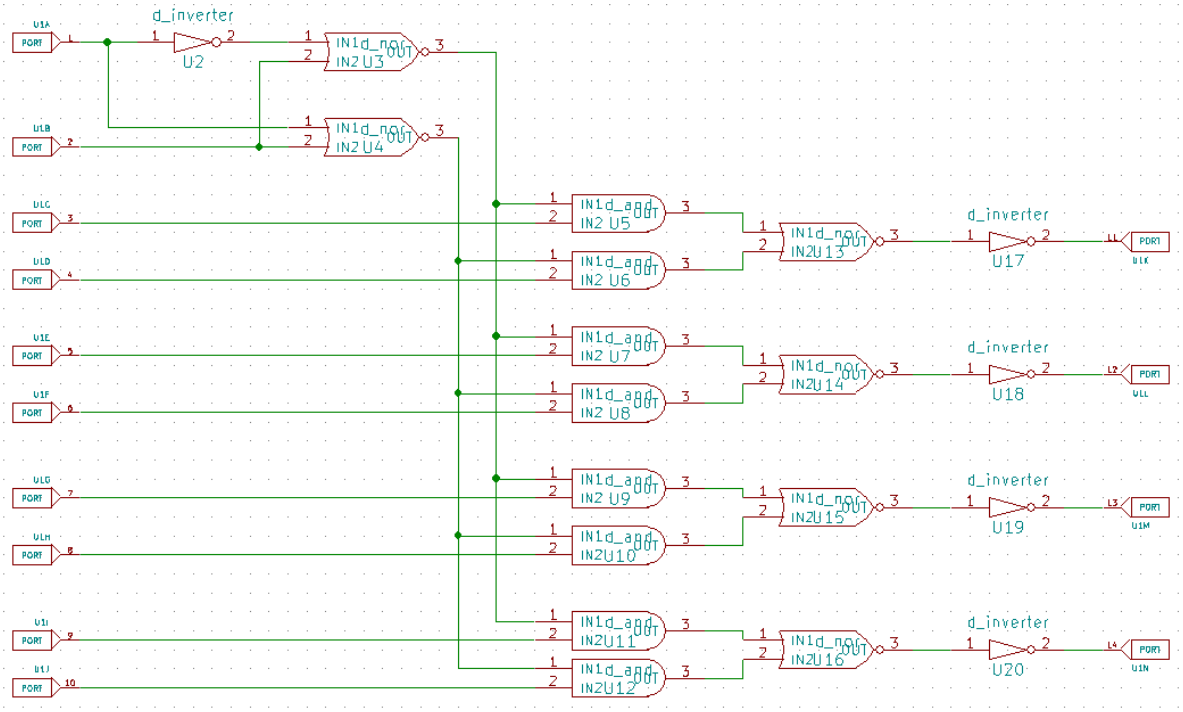

Figure 4.2: Subcircuit Schematic of the 74HC157

4.6 Test Circuit

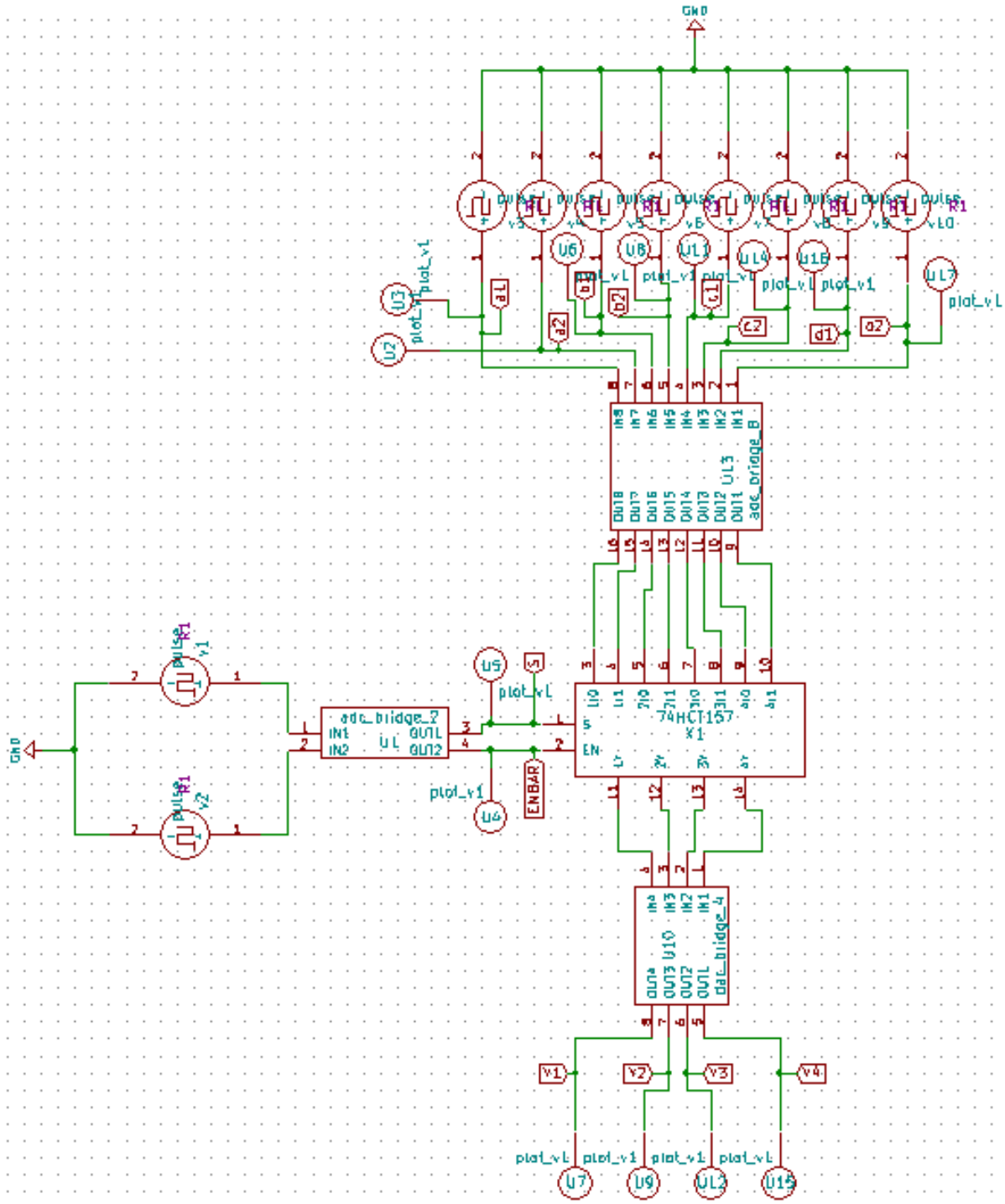

Figure 4.3: Test Circuit of the 74HC157

4.7 Function Table

FUNCTION TABLE

INPUTS				OUTPUT
$\overline{E}$	S	nI_0	nI_1	nY
H	X	X	X	L
L	L	L	X	L
L	L	H	X	H
L	H	X	L	L
L	H	X	H	H

Figure 4.4: Function Table of the 74HC157

4.8 Output Plot

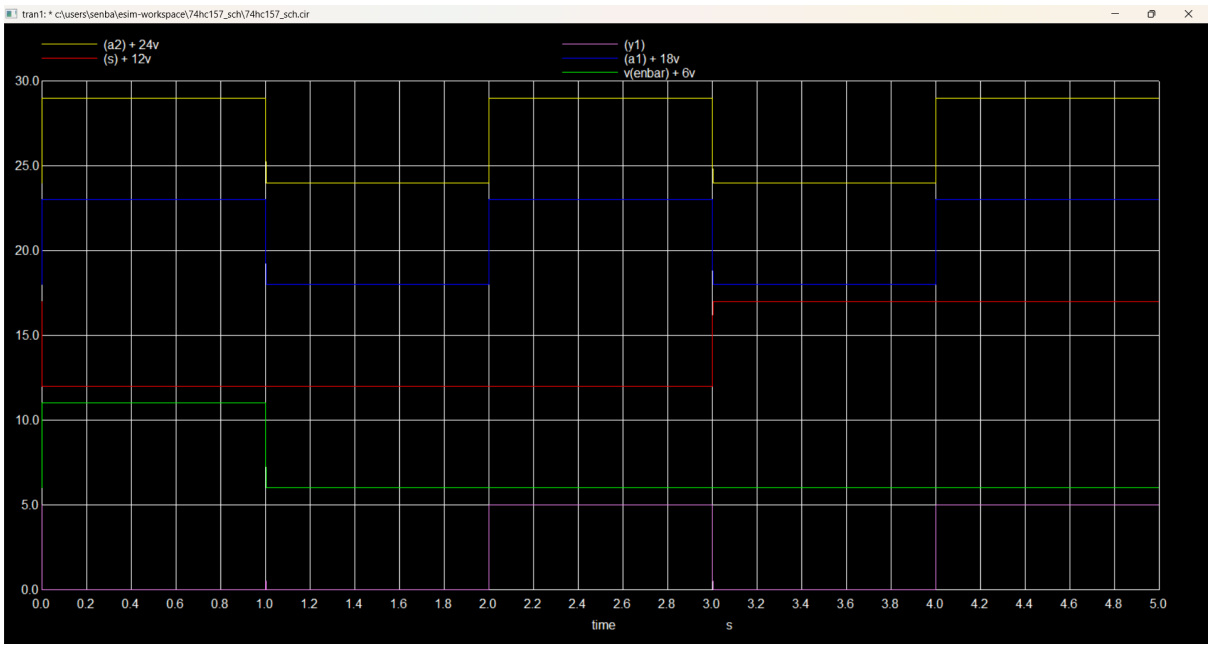

Figure 4.5: Output of the 74HC157

Chapter 5

74LS74

5.1 General Description

The 74LS74 is a dual D flip-flop with clear and preset inputs, featuring edge-triggered operation on the rising clock edge [4]. Each flip-flop has D, clock (CLK), clear (CLR), and preset (PR) inputs along with Q and $\overline{Q}$ outputs. Built using low-power Schottky TTL technology, it provides reliable performance with low power consumption for sequential logic designs.

5.2 Key Features

- Two independent D flip-flops with clear and preset
- Edge-triggered on the rising clock edge
- Standard TTL voltage operation (4.75V–5.25V)
- Synchronous control inputs
- Low power consumption (LS series)

5.3 Applications

- Data storage and transfer
- Sequential state machines
- Clock dividers and frequency counters
- Toggle flip-flop in control circuits

5.4 Subcircuit

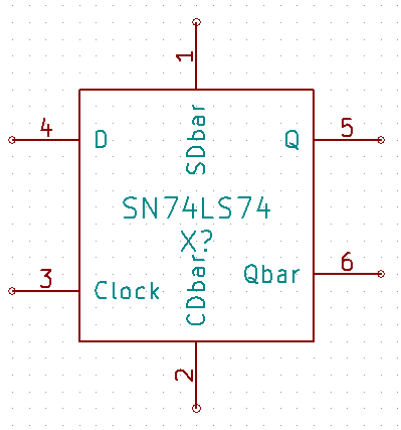

Figure 5.1: Subcircuit of 74LS74

5.5 Subcircuit Schematic Diagram

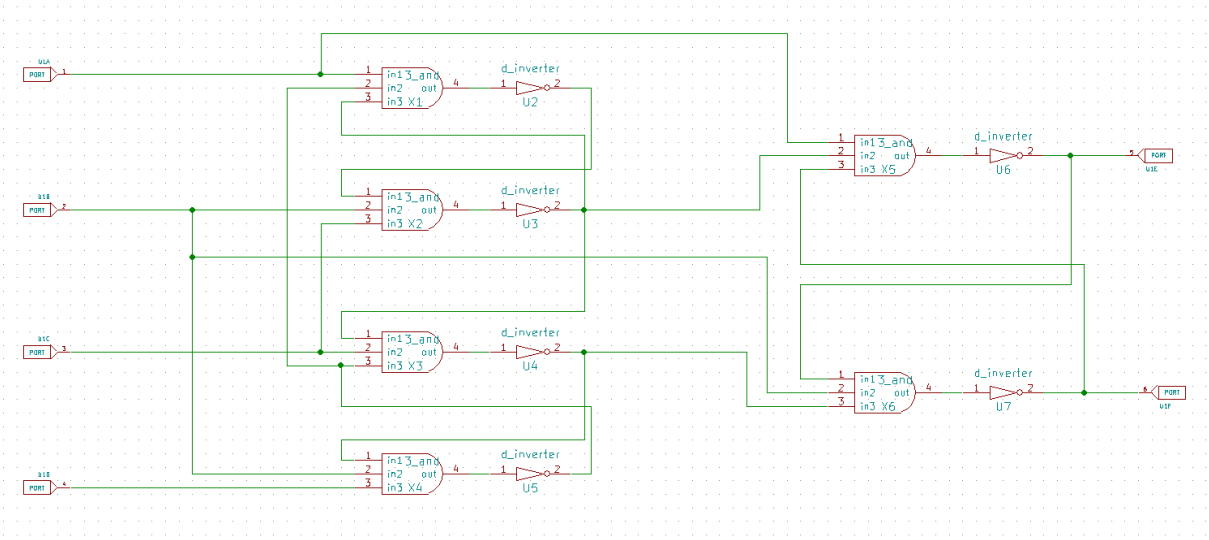

Figure 5.2: Subcircuit Schematic of the 74LS74

5.6 Test Circuit

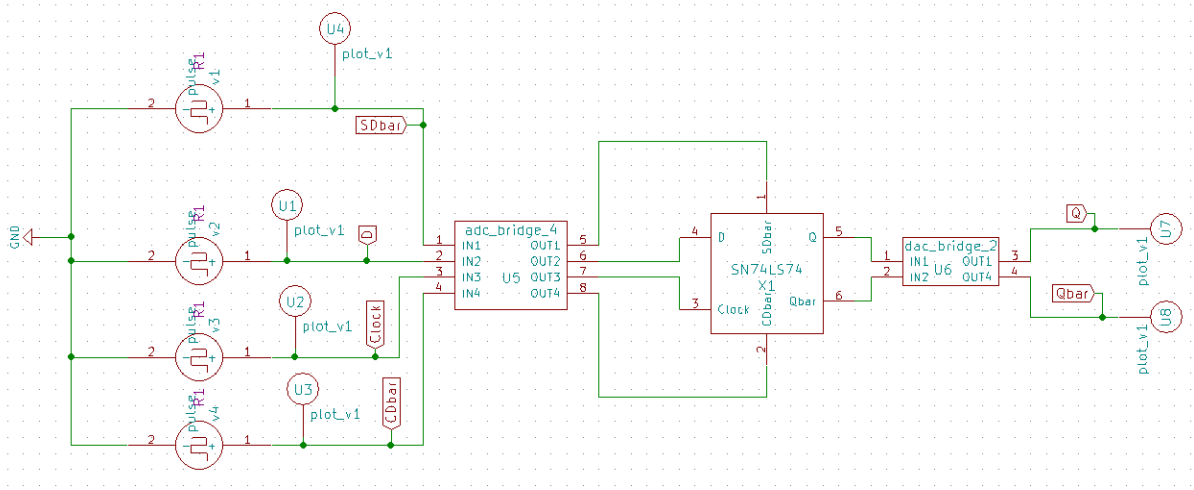

Figure 5.3: Test Circuit of the 74LS74

5.7 Function Table

OPERATING MODE	INPUTS			OUTPUTS	
	$\overline{S_D}$	$\overline{S_D}$	D	Q	$\overline{Q}$
Set	L	H	X	H	L
Reset (Clear)	H	L	X	L	H
*Undetermined	L	L	X	H	H
Load “1” (Set)	H	H	h	H	L
Load “0” (Reset)	H	H	l	L	H

Figure 5.4: Function Table of the 74LS74

5.8 Output Plot

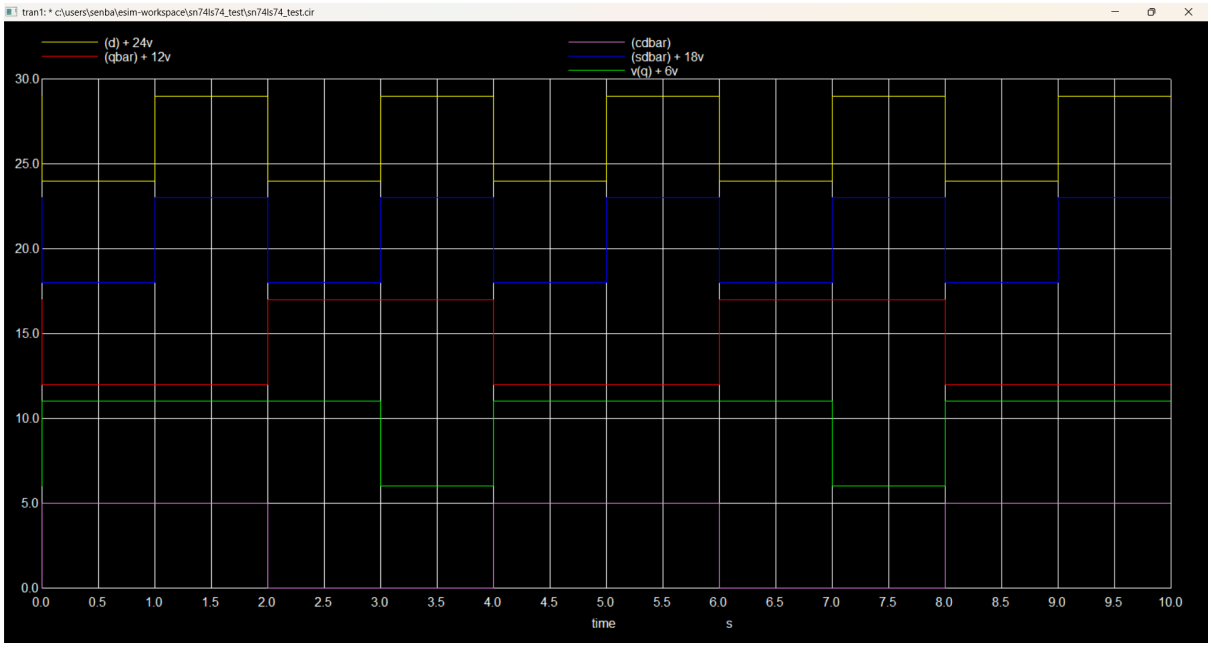

Figure 5.5: Output of the 74LS74

Chapter 6

SN7475

6.1 General Description

The SN7475 is a quad latch IC containing four independent latches with active-LOW enable inputs [5]. It stores and holds 4-bit data, with each latch providing Q and $\overline{Q}$ outputs. Built using TTL logic, it offers reliable performance for data storage and control applications in digital systems.

6.2 Key Features

- Four independent latches for 4-bit data storage
- Active-LOW enable for each pair of latches
- Standard TTL voltage levels
- Direct Q and $\overline{Q}$ outputs
- Simple control logic

6.3 Applications

- Data buffering and temporary storage
- Address latching in memory systems
- Control signal latching
- State holding in sequential circuits

6.4 Subcircuit

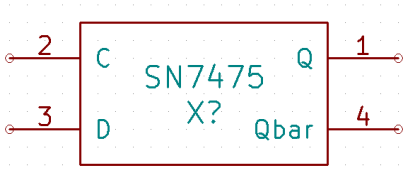

Figure 6.1: Subcircuit of SN7475

6.5 Subcircuit Schematic Diagram

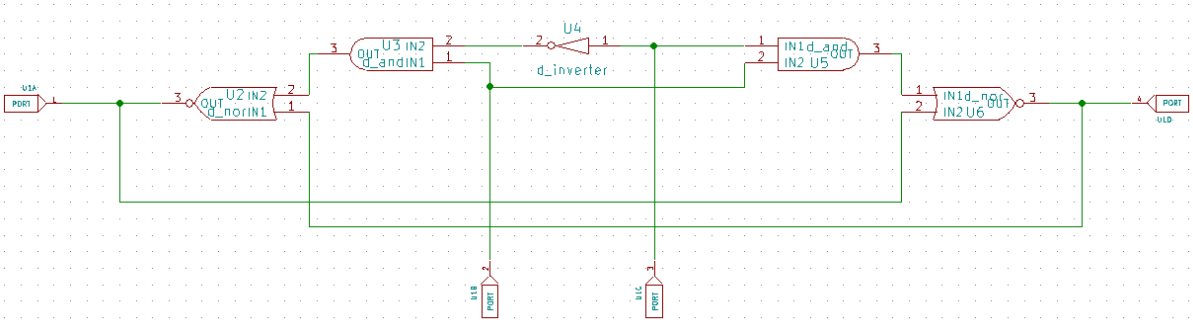

Figure 6.2: Subcircuit Schematic of the SN7475

6.6 Test Circuit

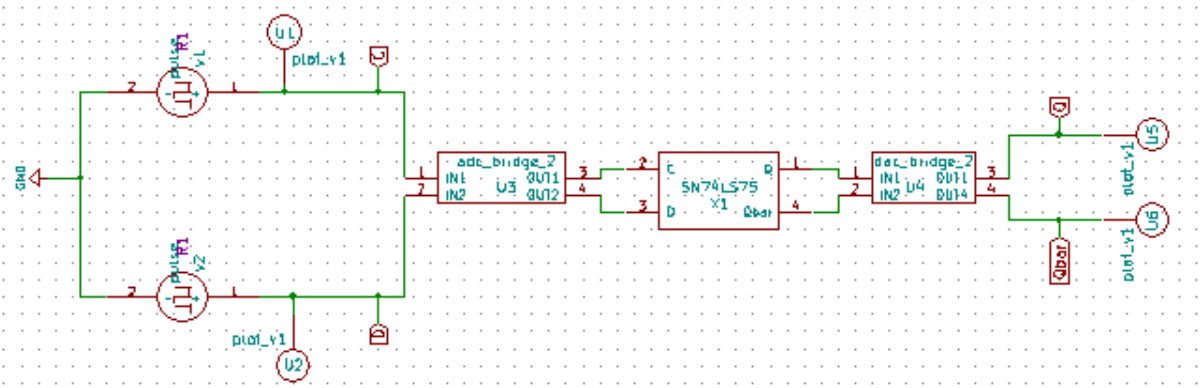

Figure 6.3: Test Circuit of the SN7475

6.7 Function Table

INPUTS		OUTPUTS	
D	C	Q	$\overline{Q}$
L	H	L	H
H	H	H	L
X	L	Q_0	$\overline{Q}_0$

Figure 6.4: Function Table of the SN7475

6.8 Output Plot

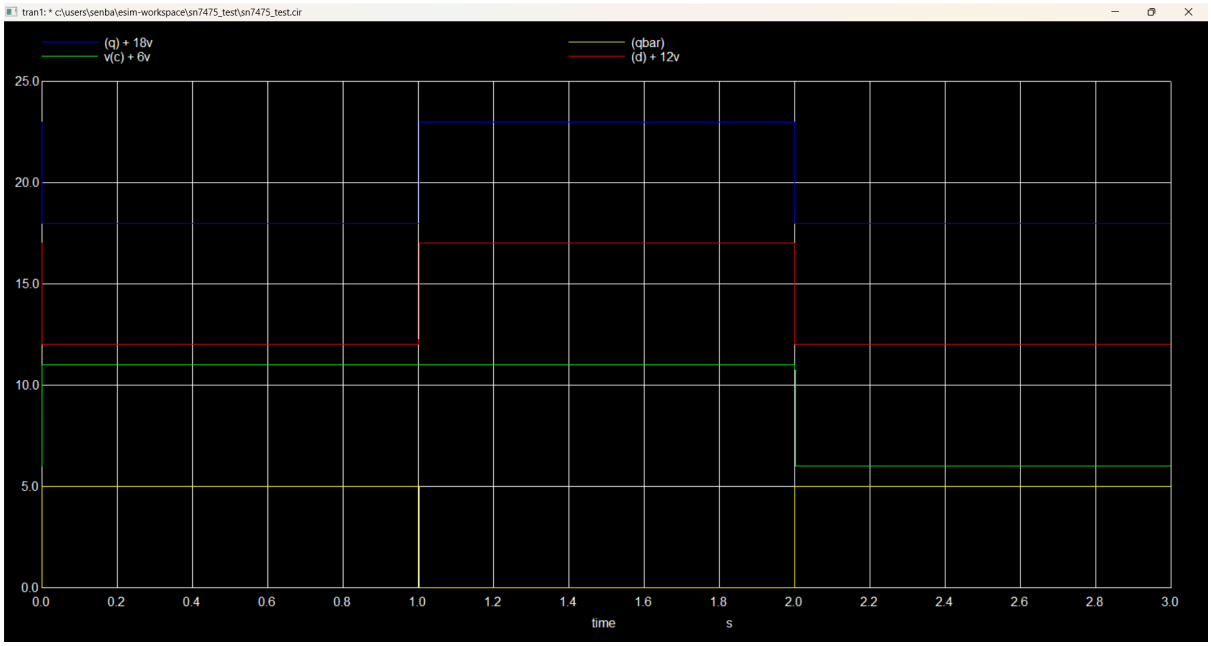

Figure 6.5: Output of the SN7475

Chapter 7

CD4068

7.1 General Description

The CD4068 is a CMOS 8-input NAND gate designed for general-purpose digital logic implementation [6]. It provides a high-speed NAND function with eight independent inputs and a single output. Built using CMOS technology, it offers low power consumption and wide operating voltage range (3V to 15V).

7.2 Key Features

- 8-input NAND gate
- Wide supply voltage range (3V–15V)
- Low power consumption
- High input impedance
- Compatible with TTL and CMOS levels

7.3 Applications

- General-purpose logic implementation
- Control signal generation
- Decoding and gating applications
- Portable and battery-powered systems

7.4 Subcircuit

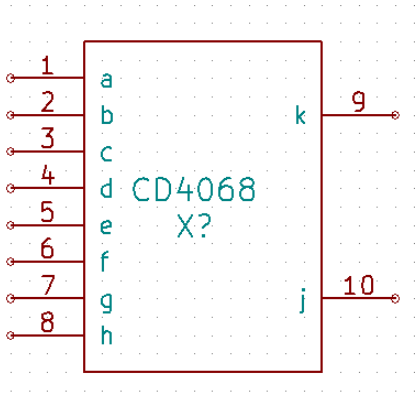

Figure 7.1: Subcircuit of CD4068

7.5 Subcircuit Schematic Diagram

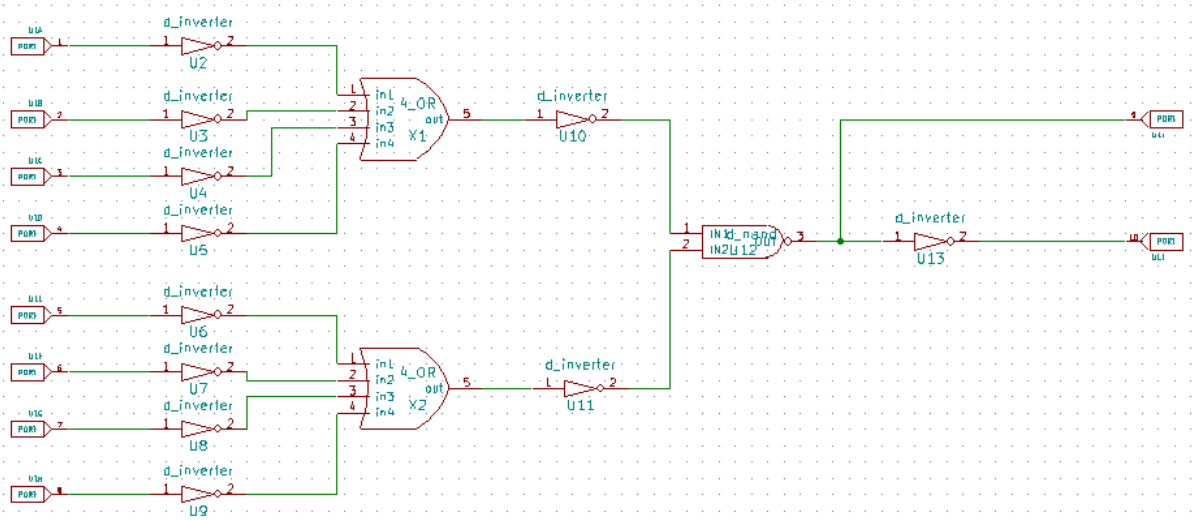

Figure 7.2: Subcircuit Schematic of the CD4068

7.6 Test Circuit

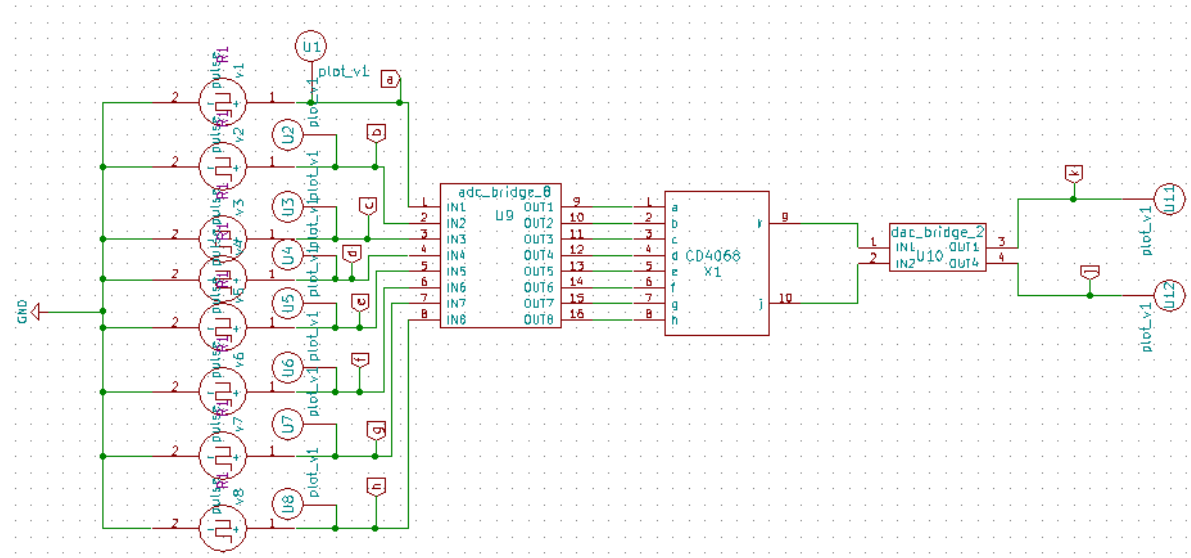

Figure 7.3: Test Circuit of the CD4068

7.7 Function Table

$$J = \overline{A \cdot B \cdot C \cdot D \cdot E \cdot F \cdot G \cdot H}$$

$$K = A \cdot B \cdot C \cdot D \cdot E \cdot F \cdot G \cdot H$$

Figure 7.4: Function Table of the CD4068

7.8 Output Plot

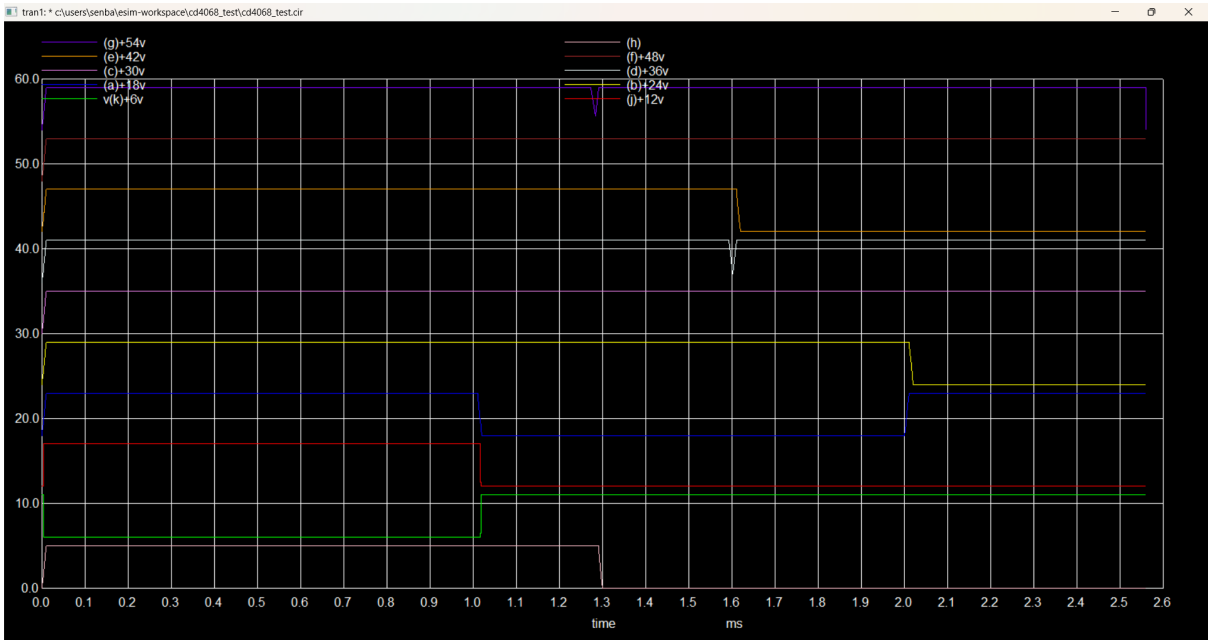

Figure 7.5: Output of the CD4068

Chapter 8

74HC682

8.1 General Description

The 74HC682 is an 8-bit magnitude comparator that compares two 8-bit binary words and provides outputs indicating equality or magnitude relationships [7]. Built using high-speed CMOS technology, it offers fast comparison operations with low power consumption and TTL-compatible logic levels.

8.2 Key Features

- 8-bit binary magnitude comparator
- Provides A $>$ B, A $=$ B, and A $<$ B outputs
- High-speed CMOS operation
- Low power dissipation
- TTL input/output compatibility

8.3 Applications

- Multi-bit magnitude comparison
- Address comparison in memory systems
- Data validation and sorting
- Digital control and decision logic

8.4 Subcircuit

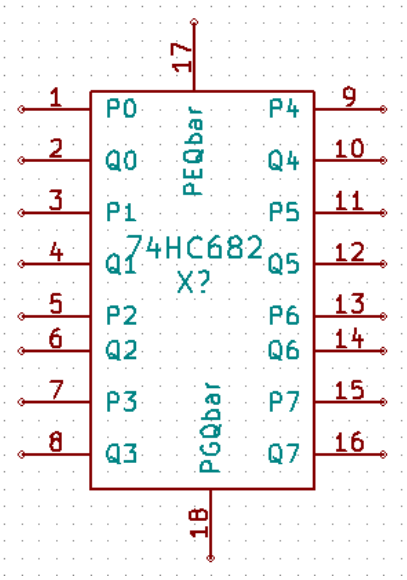

Figure 8.1: Subcircuit of 74HC682

8.5 Subcircuit Schematic Diagram

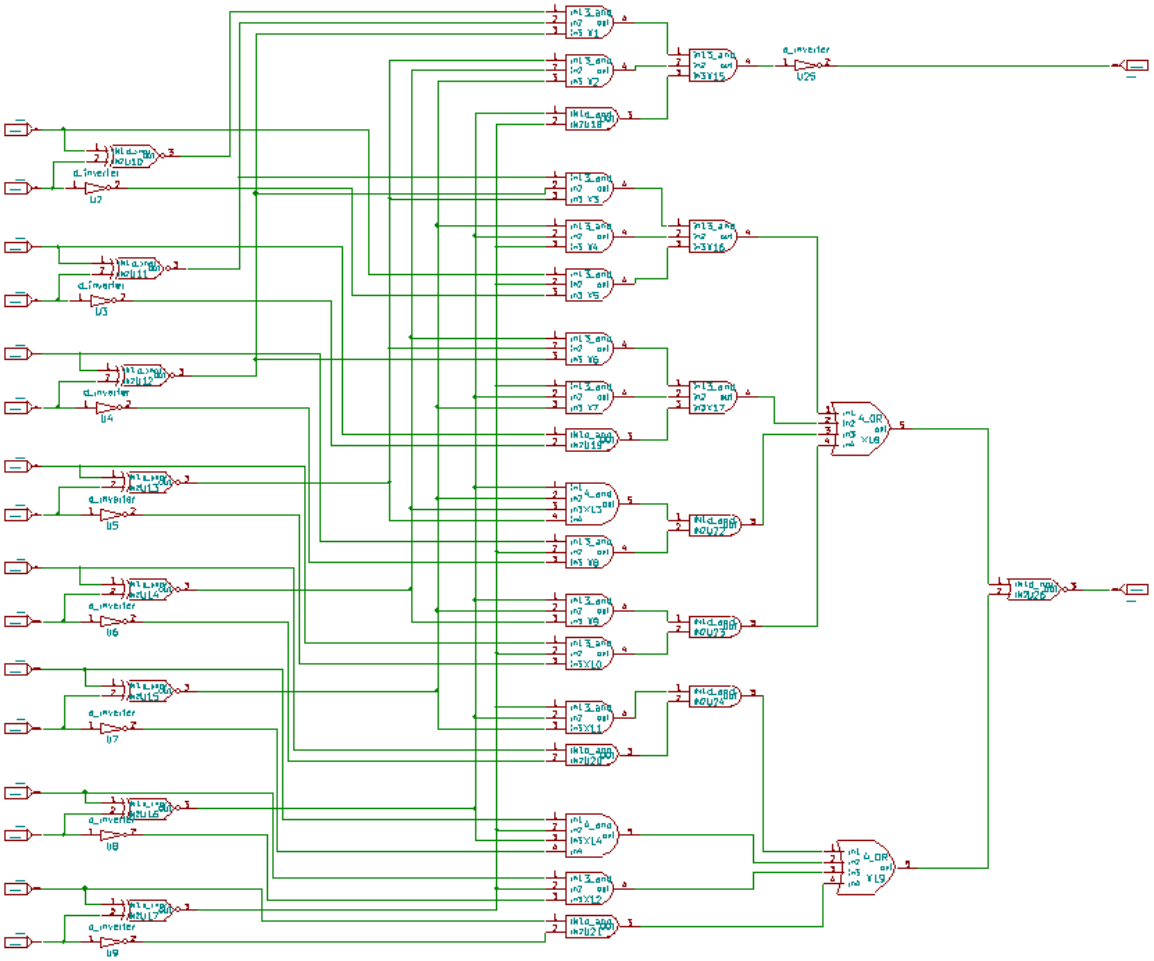

Figure 8.2: Subcircuit Schematic of the 74HC682

8.6 Test Circuit

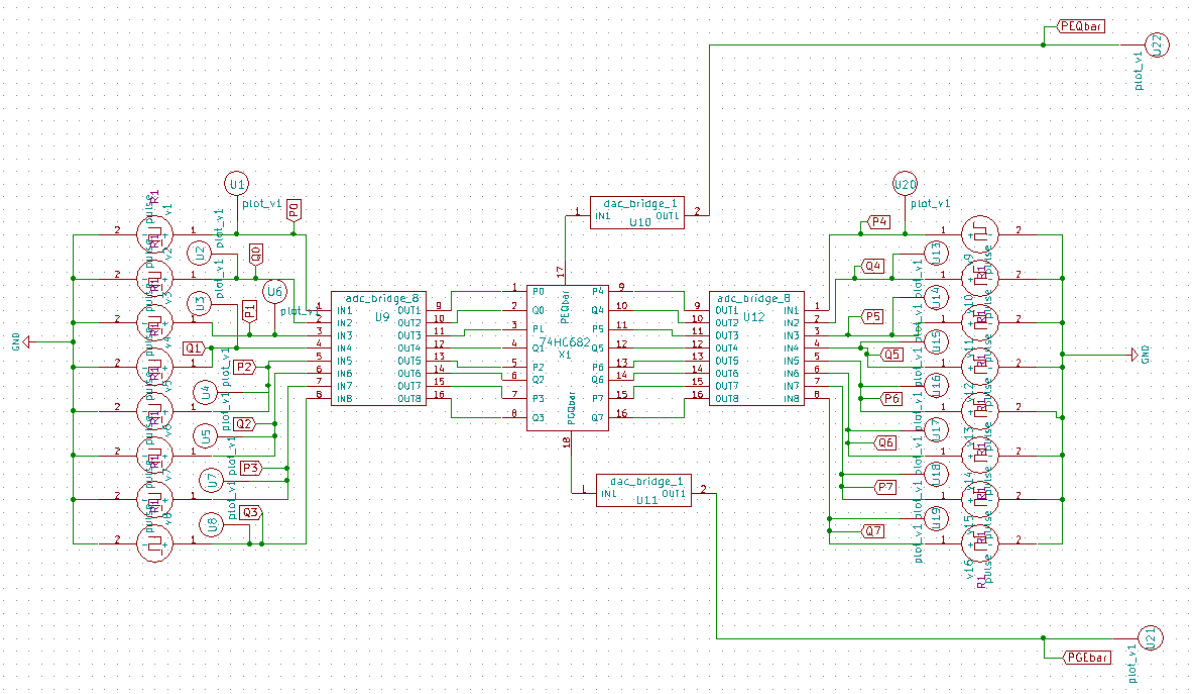

Figure 8.3: Test Circuit of the 74HC682

8.7 Function Table

FUNCTION TABLE

DATA INPUTS P, Q	OUTPUTS	
	$\overline{P = Q}$	$\overline{P > Q}$
P = Q	L	H
P > Q	H	L
P < Q	H	H

Figure 8.4: Function Table of the 74HC682

8.8 Output Plot

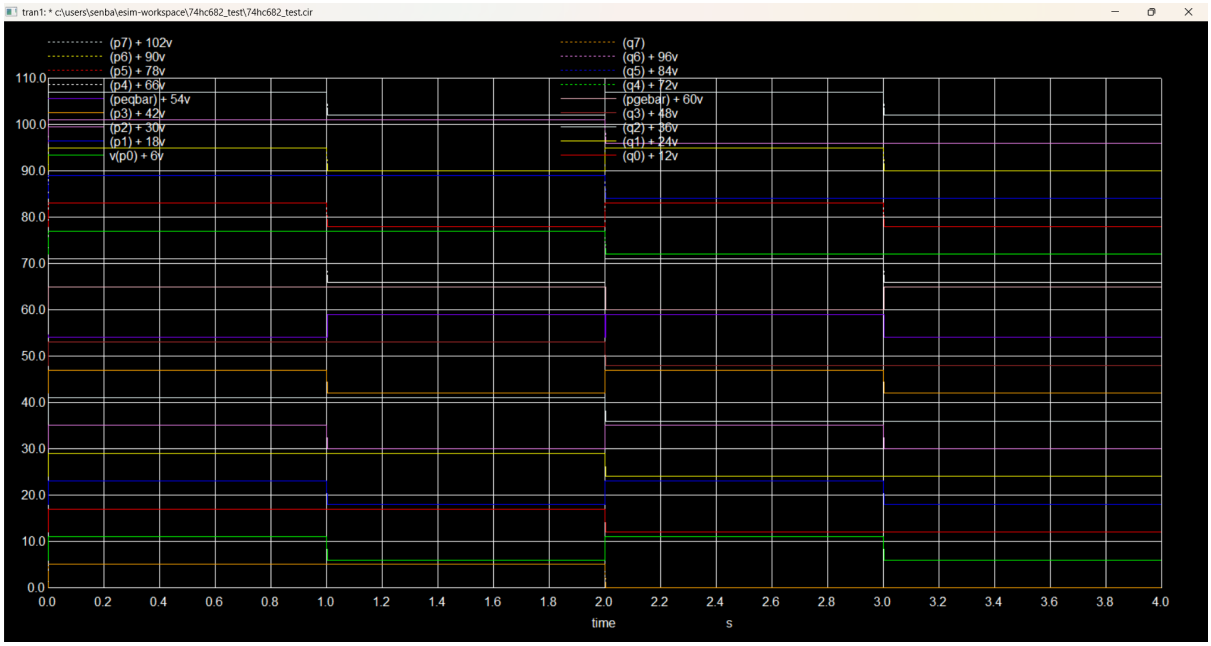

Figure 8.5: Output of the 74HC682

Chapter 9

74LVC1G58

9.1 General Description

The 74LVC1G58 is a configurable single logic gate from the LVC (Low-Voltage CMOS) family [8]. It allows implementation of various 2-input logic functions such as AND, OR, NAND, and NOR based on configuration pins. Designed for 1.65V to 5.5V operation, it is ideal for mixed-voltage systems and space-constrained applications.

9.2 Key Features

- Configurable 2-input logic gate
- Operates from 1.65V to 5.5V supply
- High-speed CMOS with low power usage
- TTL-compatible inputs
- Small form factor package

9.3 Applications

- Logic function replacement in embedded systems
- Signal conditioning
- Compact control logic implementation
- General-purpose logic in space-limited designs

9.4 Subcircuit

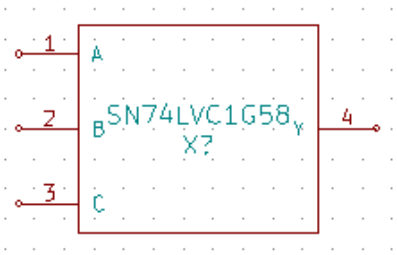

Figure 9.1: Subcircuit of 74LVC1G58

9.5 Subcircuit Schematic Diagram

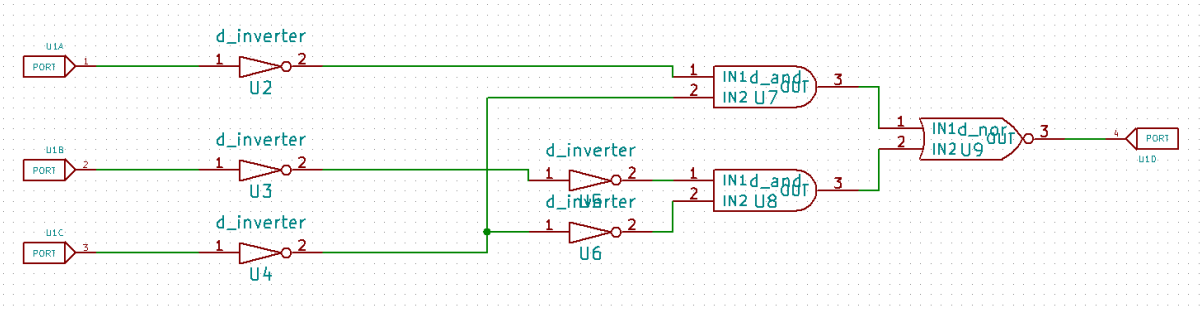

Figure 9.2: Subcircuit Schematic of the 74LVC1G58

9.6 Test Circuit

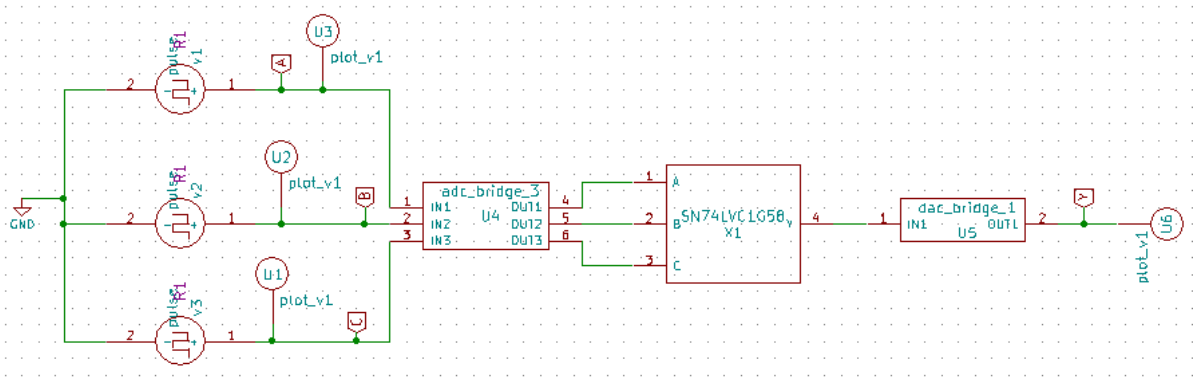

Figure 9.3: Test Circuit of the 74LVC1G58

9.7 Function Table

Inputs			Output
C	B	A	Y
L	L	L	L
L	L	H	H
L	H	L	L
L	H	H	H
H	L	L	H
H	L	H	H
H	H	L	L
H	H	H	L

Figure 9.4: Function Table of the 74LVC1G58

9.8 Output Plot

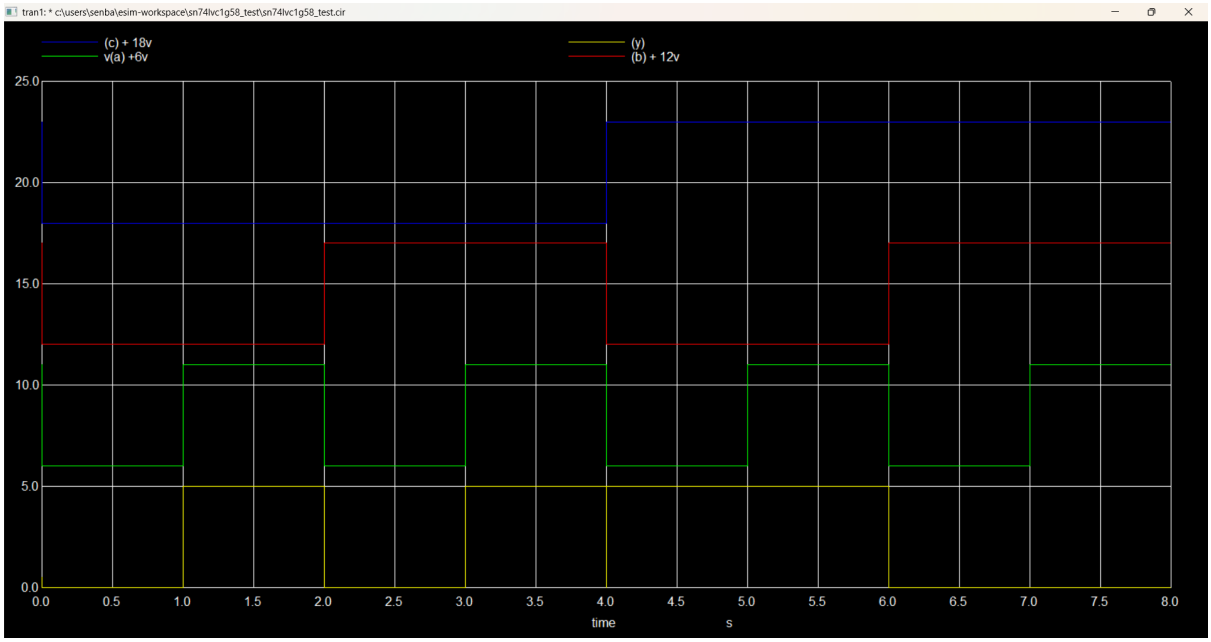

Figure 9.5: Output of the 74LVC1G58

Chapter 10

74LVC1G98

10.1 General Description

The 74LVC1G98 is a single 2-to-1 multiplexer/selector from the LVC (Low-Voltage CMOS) family [9]. It selects one of two data inputs and routes it to the output based on a select input. Built using low-voltage CMOS technology, it provides high-speed operation with low power consumption and TTL-compatible logic levels.

10.2 Key Features

- 2-to-1 multiplexer/selector
- Operates from 1.65V to 5.5V supply
- High-speed CMOS performance
- Low power consumption
- TTL input/output compatibility

10.3 Applications

- Data routing in digital systems
- Input selection in microcontroller circuits
- Signal multiplexing
- Logic switching applications

10.4 Subcircuit

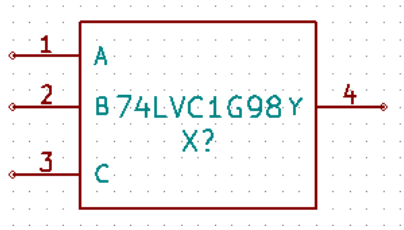

Figure 10.1: Subcircuit of 74LVC1G98

10.5 Subcircuit Schematic Diagram

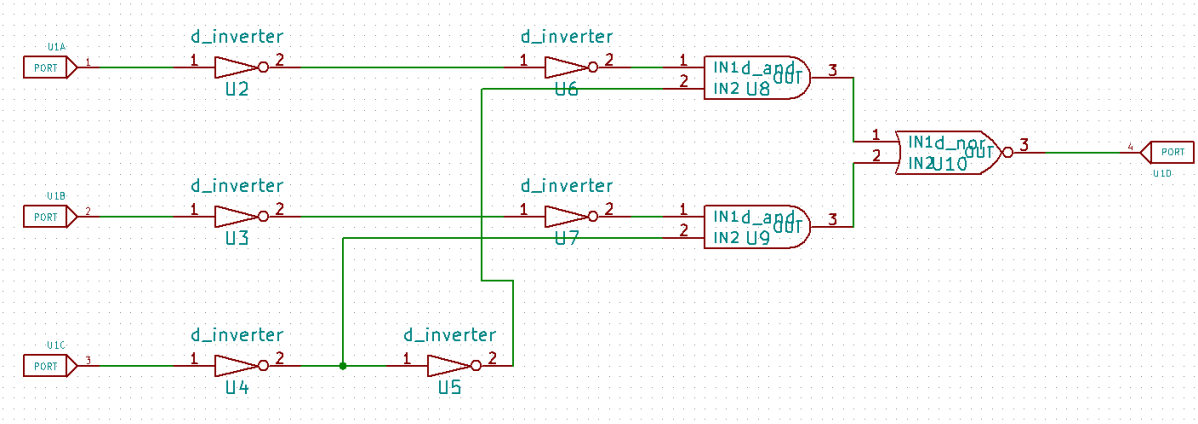

Figure 10.2: Subcircuit Schematic of the 74LVC1G98

10.6 Test Circuit

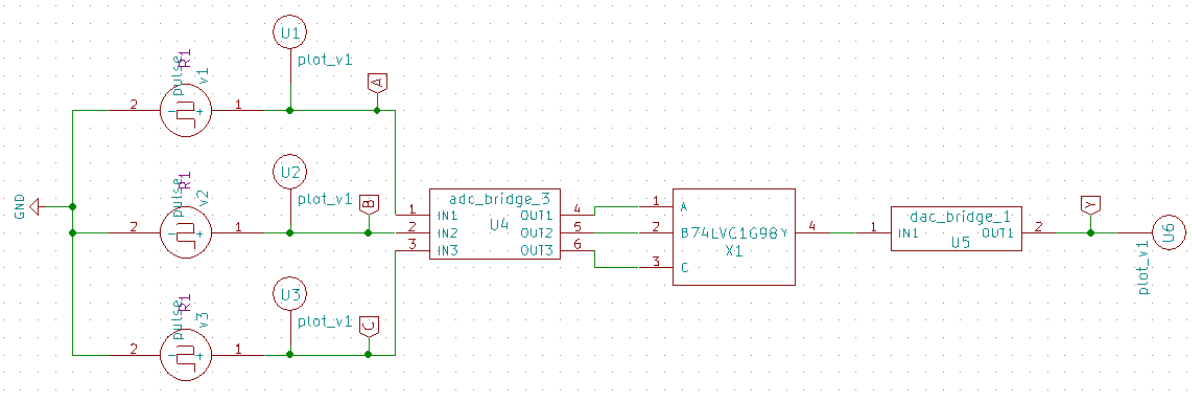

Figure 10.3: Test Circuit of the 74LVC1G98

10.7 Function Table

Input			Output
C	B	A	Y
L	L	L	H
L	L	H	H
L	H	L	L
L	H	H	L
H	L	L	H
H	L	H	L
H	H	L	H
H	H	H	L

Figure 10.4: Function Table of the 74LVC1G98

10.8 Output Plot

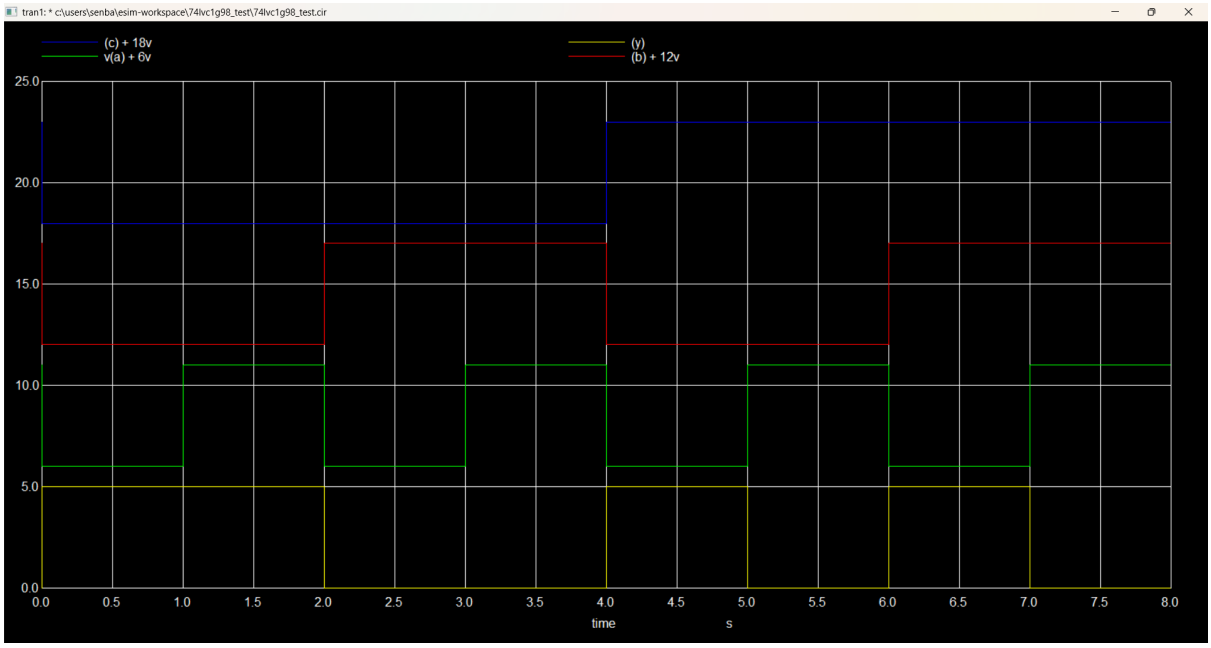

Figure 10.5: Output of the 74LVC1G98

Chapter 11

SN74155

11.1 General Description

The SN74155 is a dual 2-to-4 line decoder/demultiplexer with active-LOW outputs and common control inputs [10]. It decodes two select lines into one of four outputs, with independent enable control for each decoder. Built using TTL logic, it provides reliable performance for address decoding and data routing applications.

11.2 Key Features

- Dual 2-to-4 line decoder/demultiplexer
- Active-LOW outputs
- Independent enable inputs
- Standard TTL voltage operation
- Fast switching speeds

11.3 Applications

- Address decoding in memory systems
- Data demultiplexing
- Control signal routing
- Cascadable decoder networks

11.4 Subcircuit

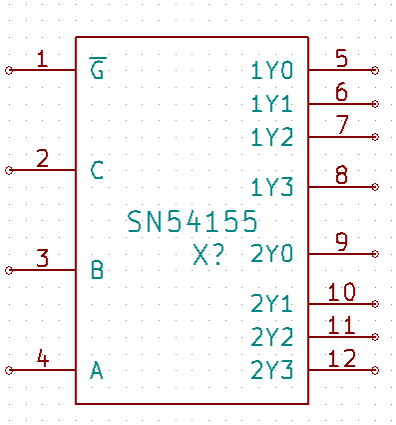

Figure 11.1: Subcircuit of SN74155

11.5 Subcircuit Schematic Diagram

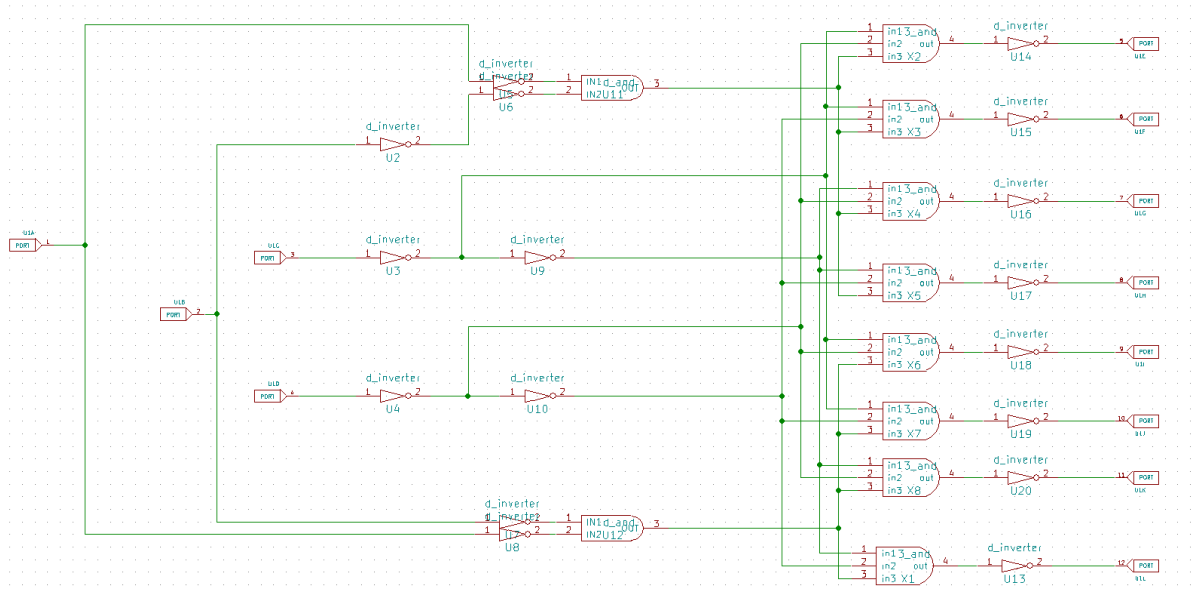

Figure 11.2: Subcircuit Schematic of the SN74155

11.6 Test Circuit

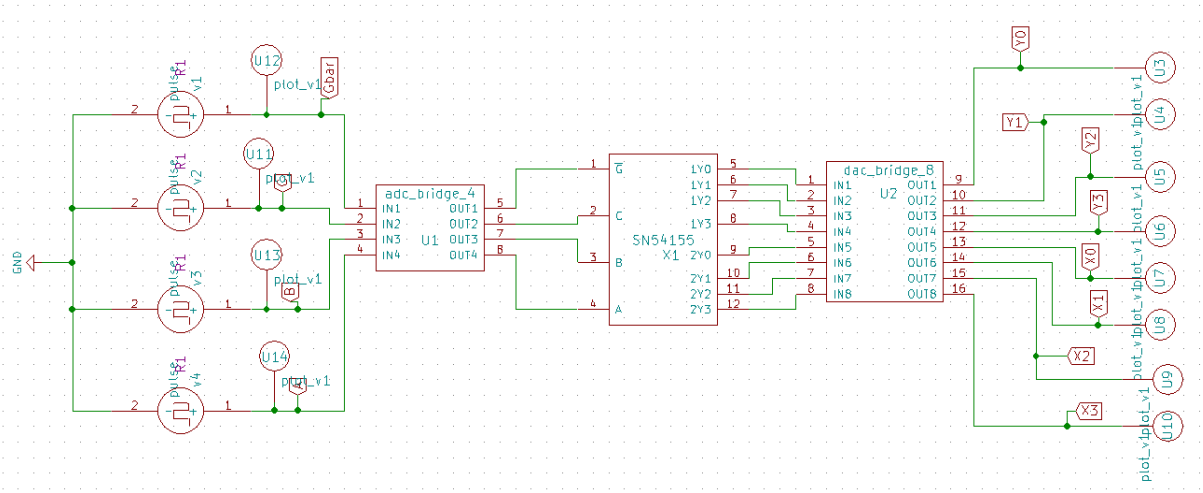

Figure 11.3: Test Circuit of the SN74155

11.7 Function Table

INPUTS				OUTPUTS			
SELECT		STROBE	DATA				
B	A	$1\overline{G}$	1C	1Y0	1Y1	1Y2	1Y3
X	X	H	X	H	H	H	H
L	L	L	H	L	H	H	H
L	H	L	H	H	L	H	H
H	L	L	H	H	H	L	H
H	H	L	H	H	H	H	L
X	X	X	L	H	H	H	H

Figure 11.4: Function Table of the SN74155

11.8 Output Plot

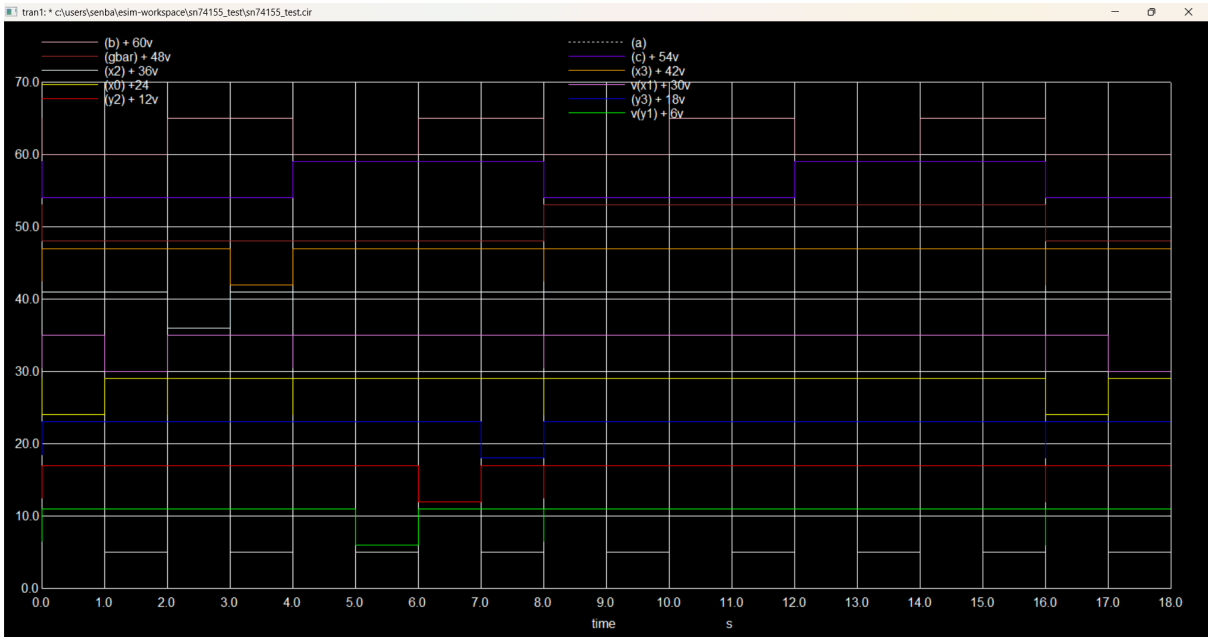

Figure 11.5: Output of the SN74155

Chapter 12

74HC279

12.1 General Description

The 74HC279 is a quad S-R (Set-Reset) latch from the HC (High-speed CMOS) family [11]. It contains four independent latches with active-LOW S and R inputs and Q outputs. Built using high-speed CMOS technology, it provides low power consumption with fast switching and TTL-compatible logic levels.

12.2 Key Features

- Four independent S-R latches
- Active-LOW set and reset inputs
- High-speed CMOS performance
- Low power consumption
- Direct Q outputs for interfacing

12.3 Applications

- Memory and state holding circuits
- Control logic and timing systems
- Debouncing and signal latching
- Sequential digital systems

12.4 Subcircuit

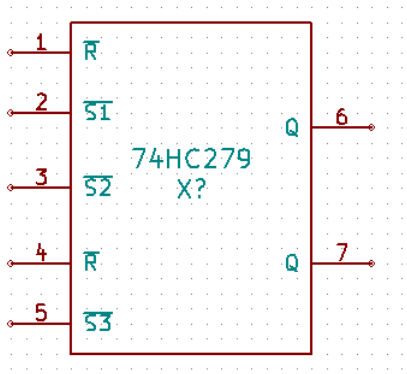

Figure 12.1: Subcircuit of 74HC279

12.5 Subcircuit Schematic Diagram

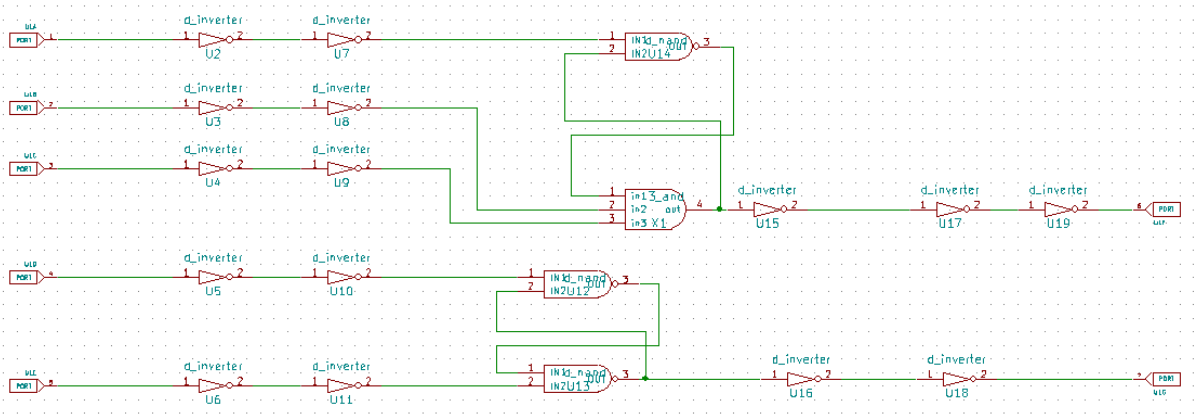

Figure 12.2: Subcircuit Schematic of the 74HC279

12.6 Test Circuit

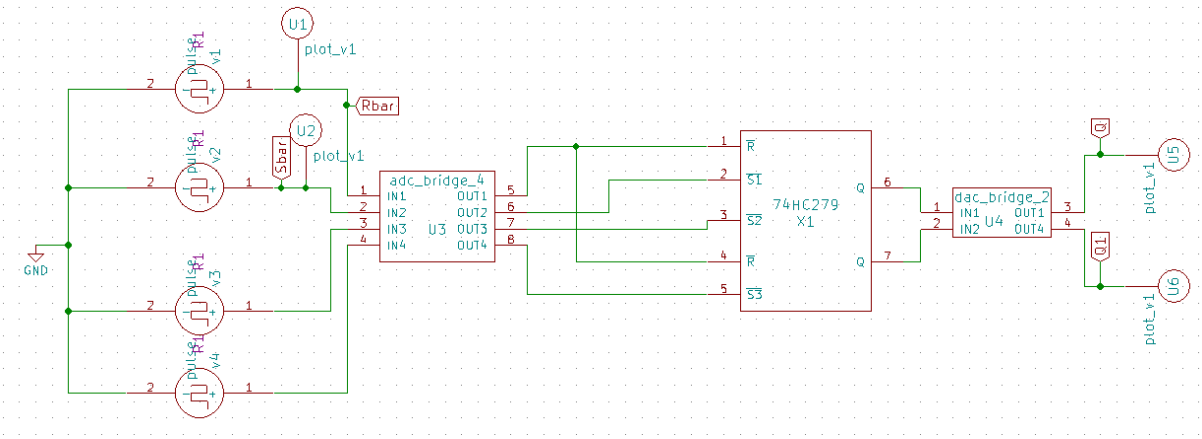

Figure 12.3: Test Circuit of the 74HC279

12.7 Function Table

Inputs		Output
$\overline{S}$*2	$\overline{R}$	**Q**
H	H	Q_0
L	H	H
H	L	L
L	L	H*1

Figure 12.4: Function Table of the 74HC279

12.8 Output Plot

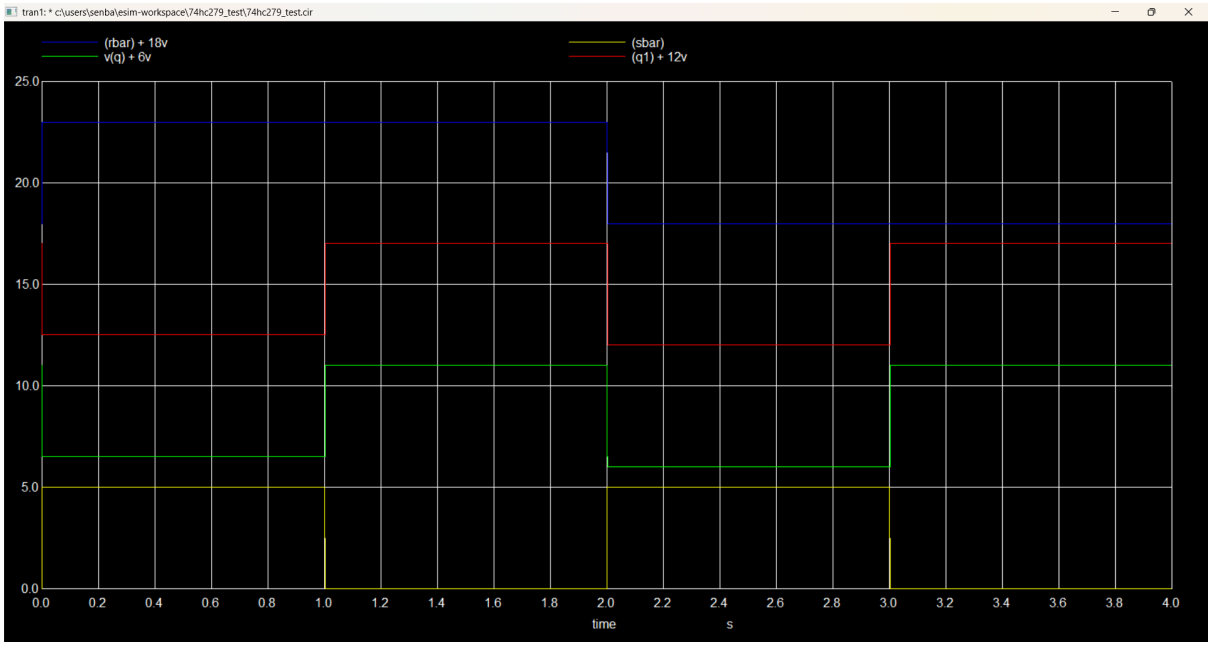

Figure 12.5: Output of the 74HC279

Chapter 13

74HC126

13.1 General Description

The 74HC126 is a quad tri-state buffer with active-HIGH enable inputs from the HC (High-speed CMOS) family [12]. It provides four independent buffers that can be placed in high-impedance state, allowing for bus control applications. Built using high-speed CMOS technology, it ensures low power consumption with fast switching speeds.

13.2 Key Features

- Quad tri-state buffer with active-HIGH enable
- High-speed CMOS performance
- Low power consumption
- High-impedance output state
- TTL input/output compatibility

13.3 Applications

- Bus control and multiplexing
- Output buffering and isolation
- Tri-state logic networks
- Data line switching and control

13.4 Subcircuit

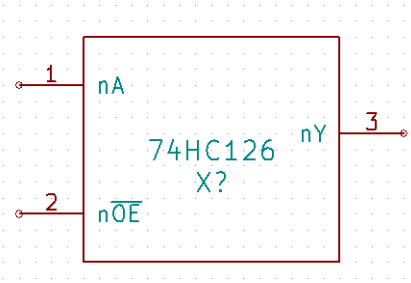

Figure 13.1: Subcircuit of 74HC126

13.5 Subcircuit Schematic Diagram

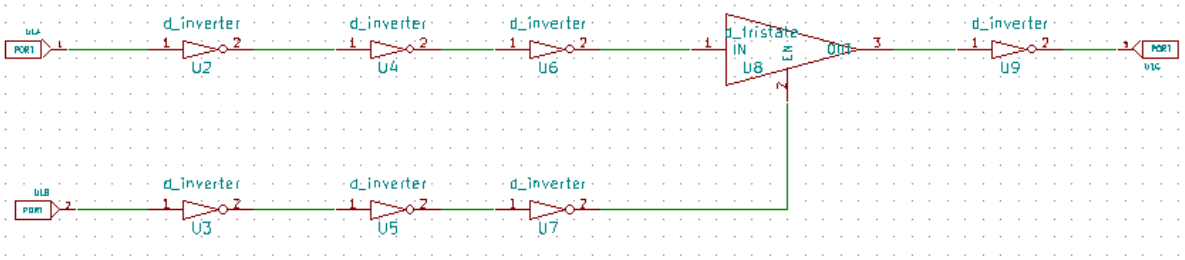

Figure 13.2: Subcircuit Schematic of the 74HC126

13.6 Test Circuit

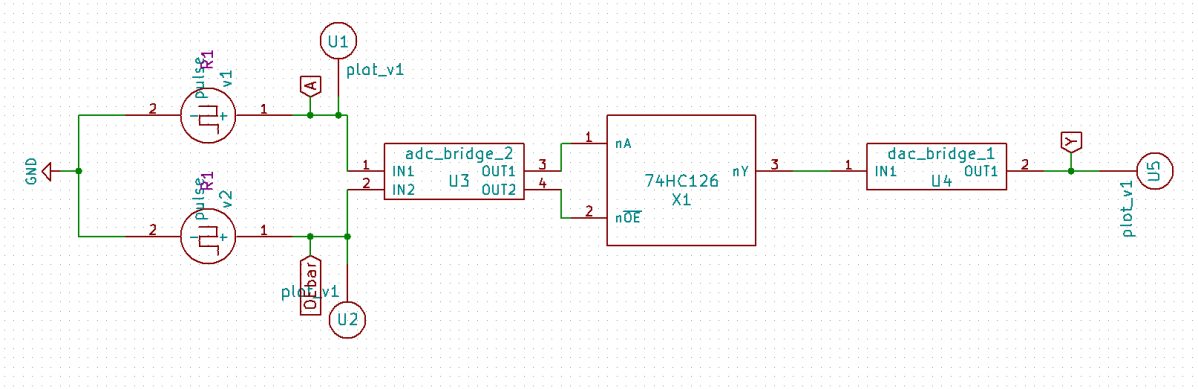

Figure 13.3: Test Circuit of the 74HC126

13.7 Function Table

INPUTS		OUTPUT
nOE	nA	nY
H	L	L
H	H	H
L	X	Z

Figure 13.4: Function Table of the 74HC126

13.8 Output Plot

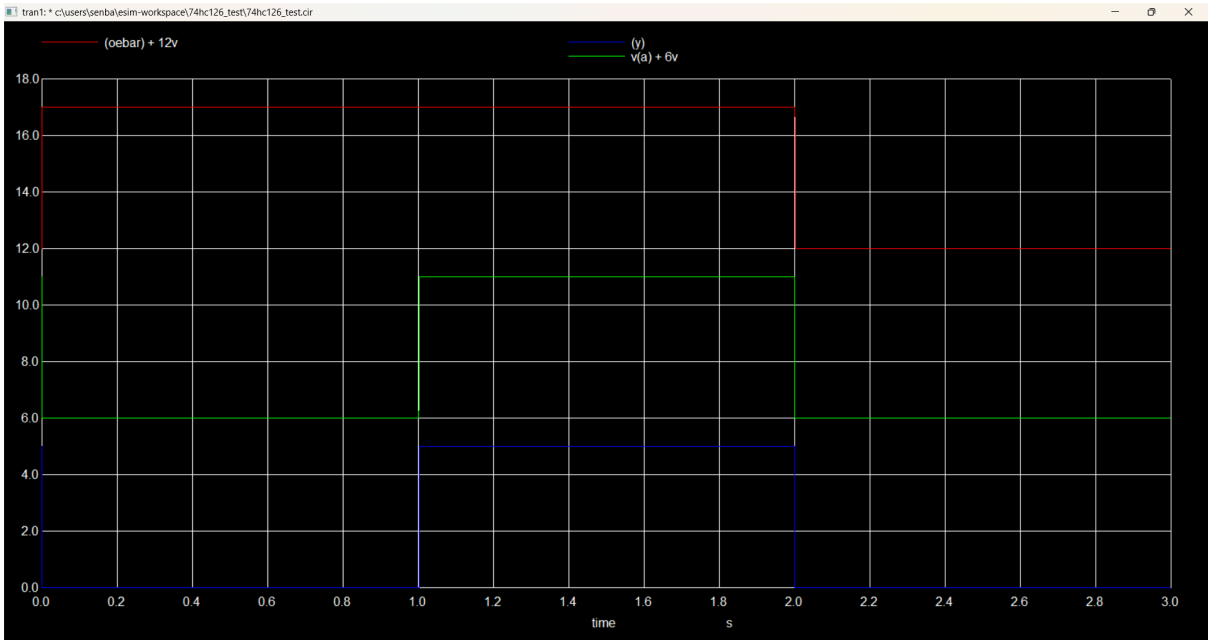

Figure 13.5: Output of the 74HC126

Chapter 14

74HC348

14.1 General Description

The 74HC348 is an 8-to-3 line priority encoder from the HC (High-speed CMOS) family [13]. It accepts up to eight active-LOW inputs and encodes them into a 3-bit binary output, giving priority to the highest-numbered active input. Built using high-speed CMOS technology, it provides low power consumption with TTL-compatible logic levels.

14.2 Key Features

- 8-to-3 line priority encoder
- Active-LOW inputs
- High-speed CMOS performance
- Low power consumption
- Valid output indicator

14.3 Applications

- Interrupt priority handling
- Keyboard or sensor input encoding
- Data compression in digital systems
- Priority logic implementation

14.4 Subcircuit

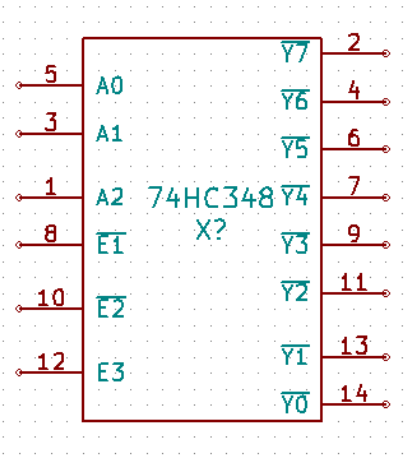

Figure 14.1: Subcircuit of 74HC348

14.5 Subcircuit Schematic Diagram

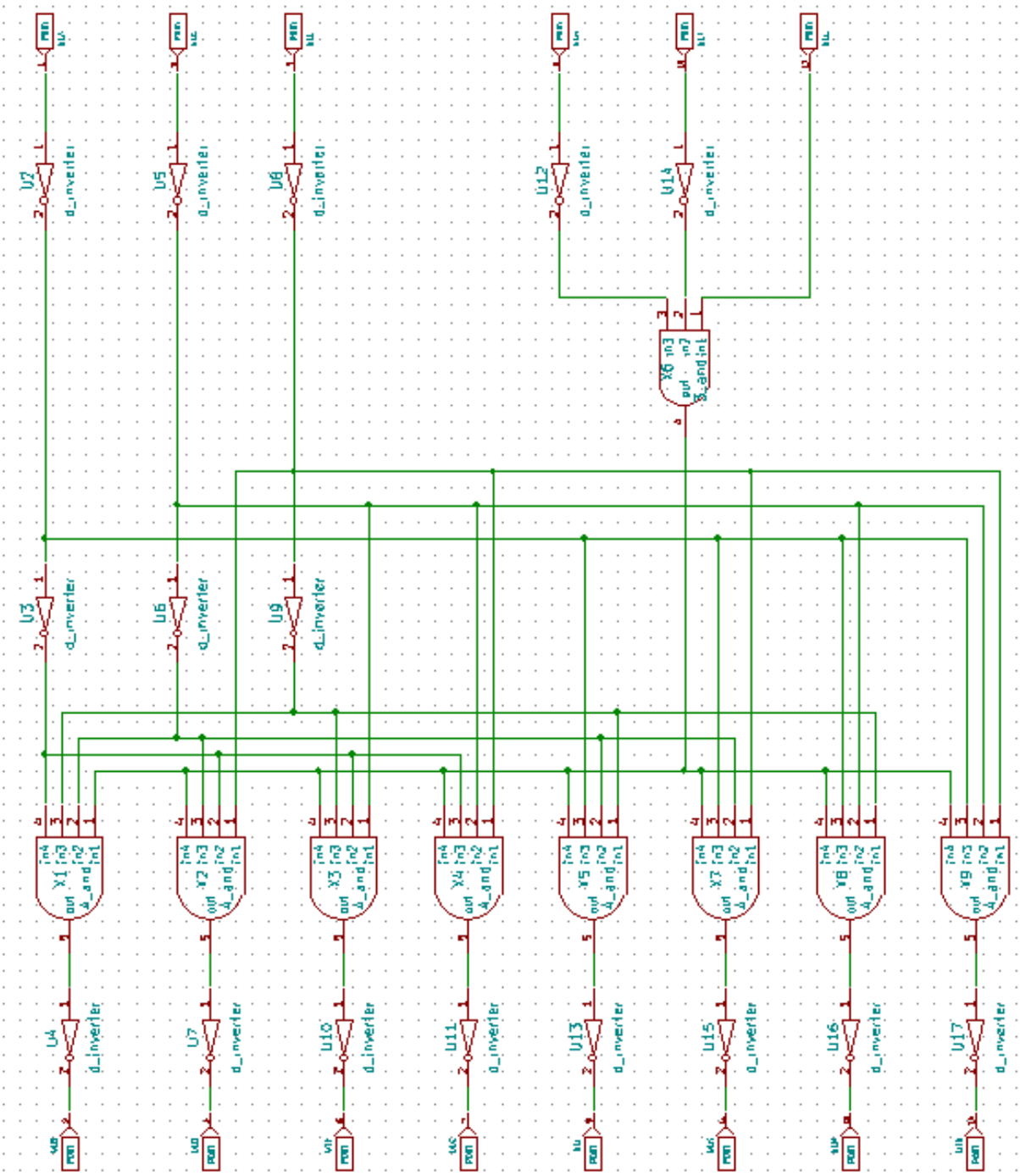

Figure 14.2: Subcircuit Schematic of the 74HC348

14.6 Test Circuit

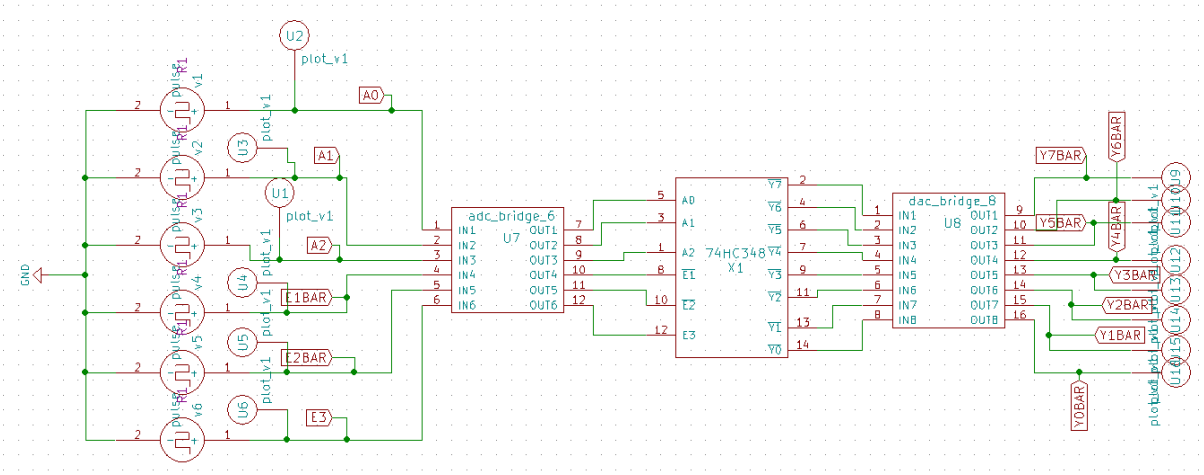

Figure 14.3: Test Circuit of the 74HC348

14.7 Function Table

INPUTS									OUTPUTS				
EI	0	1	2	3	4	5	6	7	A2	A1	A0	GS	EO
H	X	X	X	X	X	X	X	X	H	H	H	H	H
L	H	H	H	H	H	H	H	H	H	H	H	H	L
L	X	X	X	X	X	X	X	L	L	L	L	L	H
L	X	X	X	X	X	X	L	H	L	L	H	L	H
L	X	X	X	X	X	L	H	H	L	H	L	L	H
L	X	X	X	X	L	H	H	H	L	H	H	L	H
L	X	X	X	L	H	H	H	H	H	L	L	L	H
L	X	X	L	H	H	H	H	H	H	L	H	L	H
L	X	L	H	H	H	H	H	H	H	H	L	L	H
L	L	H	H	H	H	H	H	H	H	H	H	L	H

Figure 14.4: Function Table of the 74HC348

14.8 Output Plot

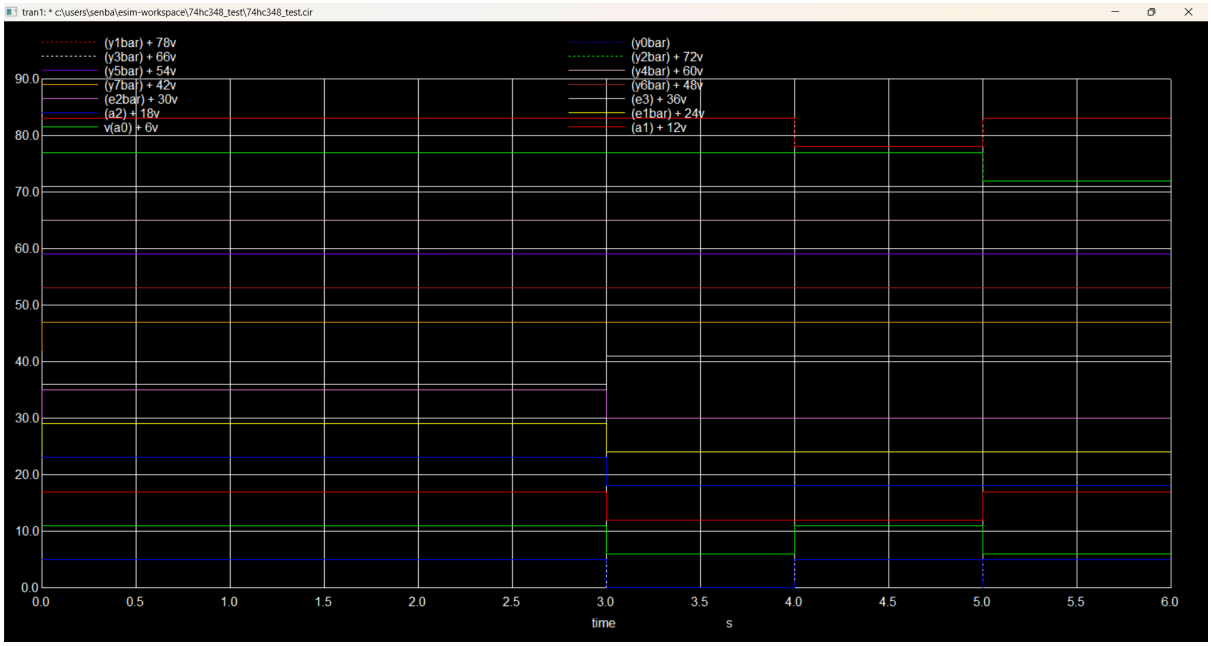

Figure 14.5: Output of the 74HC348

Chapter 15

Conclusion and Future Scope

The project successfully fulfilled its objective of contributing a diverse set of accurately modeled digital logic ICs to the eSim subcircuit library. Each IC was implemented based on its official datasheet and rigorously tested through appropriate simulation testbenches to ensure its functional correctness and reliability. The contributions include a variety of fundamental digital components such as Adders, Encoders, Decoders, Multiplexers, Flip-Flops, Latches, Comparators, and Display Drivers.

These digital IC models serve as essential building blocks for designing and simulating complex digital systems, making them valuable resources for students, educators, and researchers using eSim. By integrating these verified models into the eSim library, the project has enhanced the platform's capability to support real-world digital logic design and experimentation.

This initiative not only reinforces the importance of open-source EDA tools in academic and research settings but also lays the groundwork for future developments. As the eSim device model library continues to grow, we anticipate a broader adoption among the engineering community and the creation of increasingly sophisticated circuits. The outcomes of this project thus represent a meaningful step forward in strengthening the ecosystem of accessible, open-source circuit simulation tools.

Chapter 16

Circuits Contribution

This chapter lists all the Integrated Circuits (ICs) contributed during the fellowship. Each IC has been carefully modeled and tested, and is now part of the eSim library. The contributions include both analog and digital ICs, covering a wide range of functionalities.

16.1 Senbagaseelan V – List of ICs

1. 74HC157 – Quad 2-to-1 Line Multiplexer
2. 74LS74 – Dual D Flip-Flop with Clear and Preset
3. SN7475 – Quad Latch
4. CD4068 – 8-Input NAND Gate
5. 74HC682 – 8-Bit Magnitude Comparator
6. 74LVC1G58 – Configurable 2-Input Logic Gate
7. 74LVC1G98 – 2-to-1 Multiplexer/Selector
8. SN74155 – Dual 2-to-4 Line Decoder/Demultiplexer
9. 74HC279 – Quad S-R Latch
10. 74HC126 – Quad Tri-State Buffer
11. 74HC348 – 8-to-3 Line Priority Encoder

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