eSim Semester Long Internship Autumn 2025 Report

On

Integrated Circuit Design using Subcircuit feature of eSim

Submitted by

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Acknowledgment

I would like to express my deepest gratitude to Prof. Prabhu Ramachandran for providing me the opportunity to be a part of the FOSSEE internship program and for supporting open-source engineering tool development at IIT Bombay. His guidance and vision have encouraged students and researchers to actively contribute to the open-source ecosystem.

I would also like to acknowledge Prof. Kannan M. Moudgalya for his foundational role in establishing and nurturing the FOSSEE initiative. His contributions toward open-source education and the creation of the FOSSEE fellowship framework have directly shaped the platform through which this internship was undertaken.

My sincere appreciation extends to my mentor, **Sumanto Kar**, for his continual support, technical guidance, and encouragement throughout the duration of this project. His insights and feedback played a key role in refining ideas, overcoming challenges, and ensuring timely completion of the tasks assigned to me.

I would also like to thank my internal mentors, **Mr. Varad Patil**, **Ms. Shanthi Priya K**, and **Mr. Aditya M**, for their valuable guidance, coordination, and technical inputs during the internship. Their mentorship contributed significantly to the clarity, progress, and successful execution of the work.

This internship has been an enriching learning experience, allowing me to work closely with open-source EDA tools, develop IC subcircuits in eSim, and gain exposure to real-world circuit modeling and simulation workflows. The knowledge acquired during this period will undoubtedly support my future academic and professional pursuits.

I would also like to thank the entire FOSSEE team for their coordination, assistance, and timely interactions at various stages of this work. Their collective efforts ensured smooth workflow, resource accessibility, and effective project execution.

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Chapter 1

Introduction

eSim is an open-source Electronic Design Automation (EDA) platform developed under the FOSSEE initiative at IIT Bombay. The software enables schematic capture, circuit simulation, and analysis by integrating multiple open-source tools into a unified environment. eSim provides a viable alternative to proprietary EDA solutions and makes electronic circuit design accessible for academic research, prototyping, and learning purposes.

1.1 eSim

The eSim toolchain supports analog, digital, and mixed-signal designs. It combines netlist generation, SPICE-based simulation, and VHDL-based digital verification under a single workflow. By leveraging open-source utilities, eSim eliminates licensing barriers and encourages experimentation in circuit design and system validation.

1.1.1 NgSpice

NgSpice serves as the simulation engine within eSim. It interprets SPICE netlists generated from schematic diagrams and performs time-domain and frequency-domain analysis. The simulator is capable of handling analog and mixed-signal circuits, enabling users to observe transient responses, node voltages, and current waveforms. This makes NgSpice suitable for evaluating circuit behavior and validating design performance.

1.1.2 Makerchip

Makerchip is an online platform for modeling and testing digital hardware using TL-Verilog. Through eSim, Makerchip can be integrated into the design flow to implement combinational and sequential digital circuits. It offers waveform visualization, hierarchical design support, and debugging features that make it valuable for FPGA-style development and educational training.

1.1.3 KiCad

KiCad is an open-source suite for schematic capture and PCB design. Within eSim, KiCad is used to construct circuit schematics that can be converted into SPICE netlists for simulation. It also supports component libraries, footprints, annotation, and multi-layer PCB layout. KiCad bridges the gap between simulation and hardware fabrication, giving users exposure to real-world PCB design workflows.

1.1.4 GHDL

GHDL facilitates the simulation and verification of VHDL-based digital hardware descriptions. In the eSim environment, GHDL is used for compiling and executing digital logic designs. This capability enables mixed-signal circuit development, where both analog and digital components coexist and interact. The integration of GHDL strengthens eSim's support for digital verification and system-level modeling.

Chapter 2

Features of eSim

eSim offers an integrated environment for electronic circuit design, verification, and analysis. The software combines various open-source utilities, enabling users to design mixed-signal circuits and perform simulations without the need for expensive licensed EDA tools. The platform is particularly suited for academic and research applications due to its accessibility and modular architecture.

One of the key advantages of eSim is its ability to seamlessly interface with external toolsets for both analog and digital simulation. This compatibility promotes an end-to-end development workflow where schematic capture, netlist generation, simulation, and performance observation are carried out through a unified interface. eSim also supports hierarchical design structures, making it suitable for constructing complex circuit systems.

In addition, eSim supports SPICE modeling, VHDL verification, and mixed-domain interactions which allow designers to evaluate circuits at multiple abstraction levels. This promotes better experimentation and understanding of circuit behavior and performance characteristics.

Major features of eSim can be summarized as follows:

- **Open-source platform:** Eliminates licensing costs associated with commercial EDA tools.
- **Mixed-signal support:** Allows the coexistence of analog and digital modules within a single design.
- **Schematic capture:** Enables construction of circuit schematics using KiCad.
- **SPICE-based simulation:** Utilizes NgSpice for transient, AC, and DC analysis.
- **VHDL/HDL support:** Provides digital logic verification using GHDL and Makerchip.
- **Component libraries:** Offers a wide range of analog, digital, and mixed-signal components for circuit design.
- **Hierarchy and modularity:** Supports multi-level hierarchical schematics suitable for complex designs.
- **Waveform visualization:** Allows visualization of simulated results for validation and debugging.
- **PCB design compatibility:** Interfaces with KiCad for PCB layout and fabrication workflows.

- **Educational applicability:** Useful for electronics education, research, and prototyping environments.

Overall, eSim enables users to experiment with design methodologies, improve circuit understanding, and validate electronic systems using open-source tools. Its interoperability and accessibility make it suitable for academic institutions, hobbyists, and embedded systems developers.

Chapter 3

Problem Statement

The objective of this internship was to design and implement a collection of analog and digital Integrated Circuit (IC) models in the form of subcircuits using the device model files available within the eSim library. These IC models are intended to be incorporated into the eSim subcircuit library, enabling designers, students, and developers to utilize them for future circuit design and simulation tasks. Once successfully integrated, the developed components enhance the capability of eSim by providing reusable building blocks for electronic system development.

3.1 Approach

The development workflow adopted during this internship consisted of several stages, outlined as follows:

1. **Datasheet Analysis:** The first step involved surveying a variety of analog and digital IC datasheets to identify suitable components that were not already present in the eSim library. Based on the device specifications, electrical characteristics, pin descriptions, truth tables, and internal schematics, appropriate ICs were shortlisted for implementation.

2. **Subcircuit Modeling:** After selecting the ICs, they were modeled as subcircuits using the component and device models available within the eSim framework. The subcircuits were constructed strictly according to the datasheet specifications. During this phase, the corresponding symbol and pin layout were also created to match the physical packaging and pin configuration of each IC.

3. **Test Circuit Development:** Once the subcircuit models were prepared, test circuits were designed using the newly created components. These test setups replicated the operating conditions and validation circuits typically shown in the datasheets, enabling functional verification.

4. **Simulation and Verification:** The test circuits were simulated using the eSim workflow involving KiCad schematic capture and NgSpice simulation. The generated waveforms and plots were examined to verify whether the subcircuits behaved according to the expected results. If discrepancies were observed, the design was revisited and corrected until proper functionality was achieved. Successful validation confirmed that the IC models operated as intended, completing the design cycle.

Chapter 4

Integrated Circuit Design

4.1 CD4518B - Dual D-Type Flip-Flop

Description: Dual edge-triggered D-type flip-flop IC.

General Description: The CD4518B provides two independent D-type flip-flops with asynchronous set and reset controls. Data present on the D input is latched to Q on the rising clock edge. The device can be used for toggle, latch, counting, and shift register applications and operates with low-power CMOS logic levels.

4.1.1 IC Layout

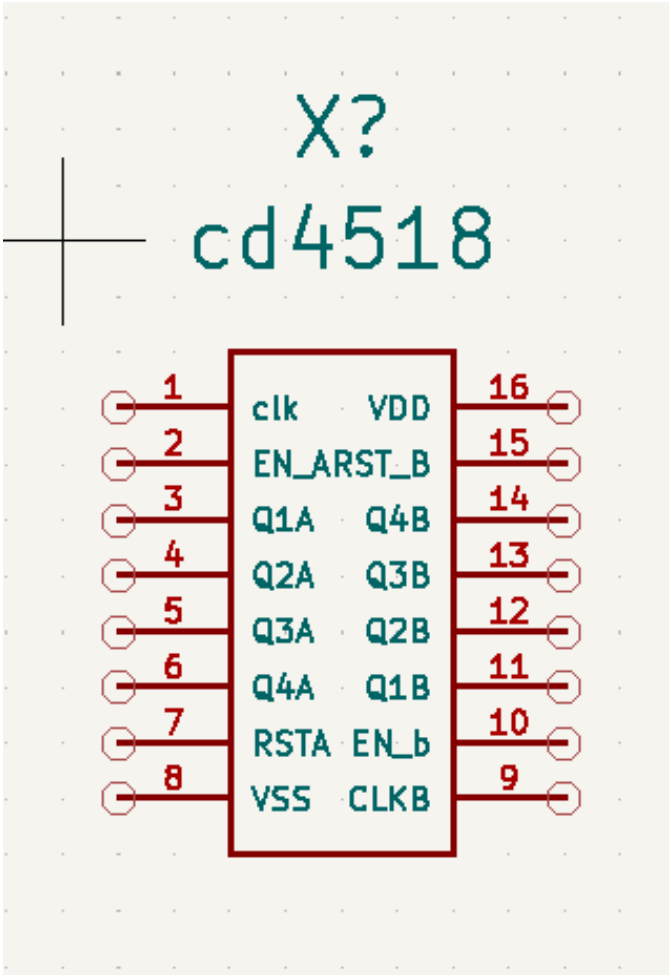

Figure 4.1: Pin diagram of CD4518B

4.1.2 Subcircuit Schematic Diagram

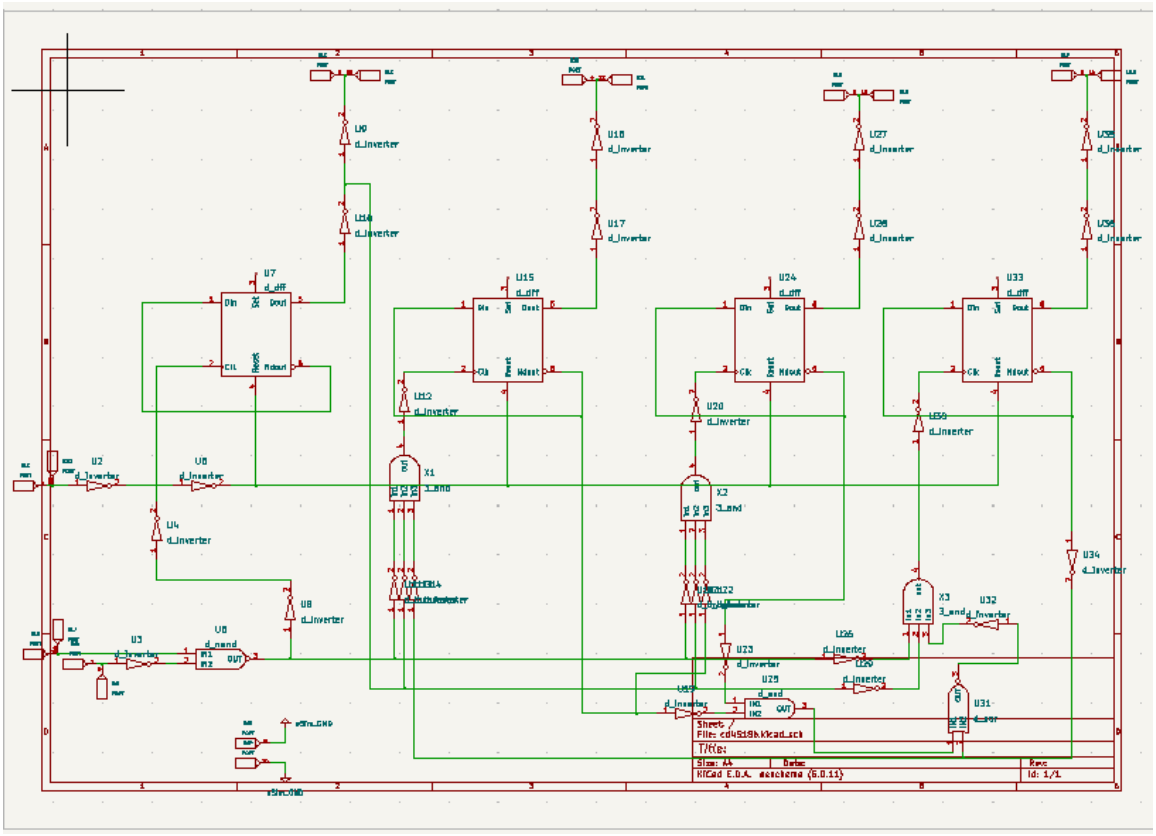

Figure 4.2: Subcircuit schematic diagram of CD4518B implemented in eSim

4.1.3 Test Circuit

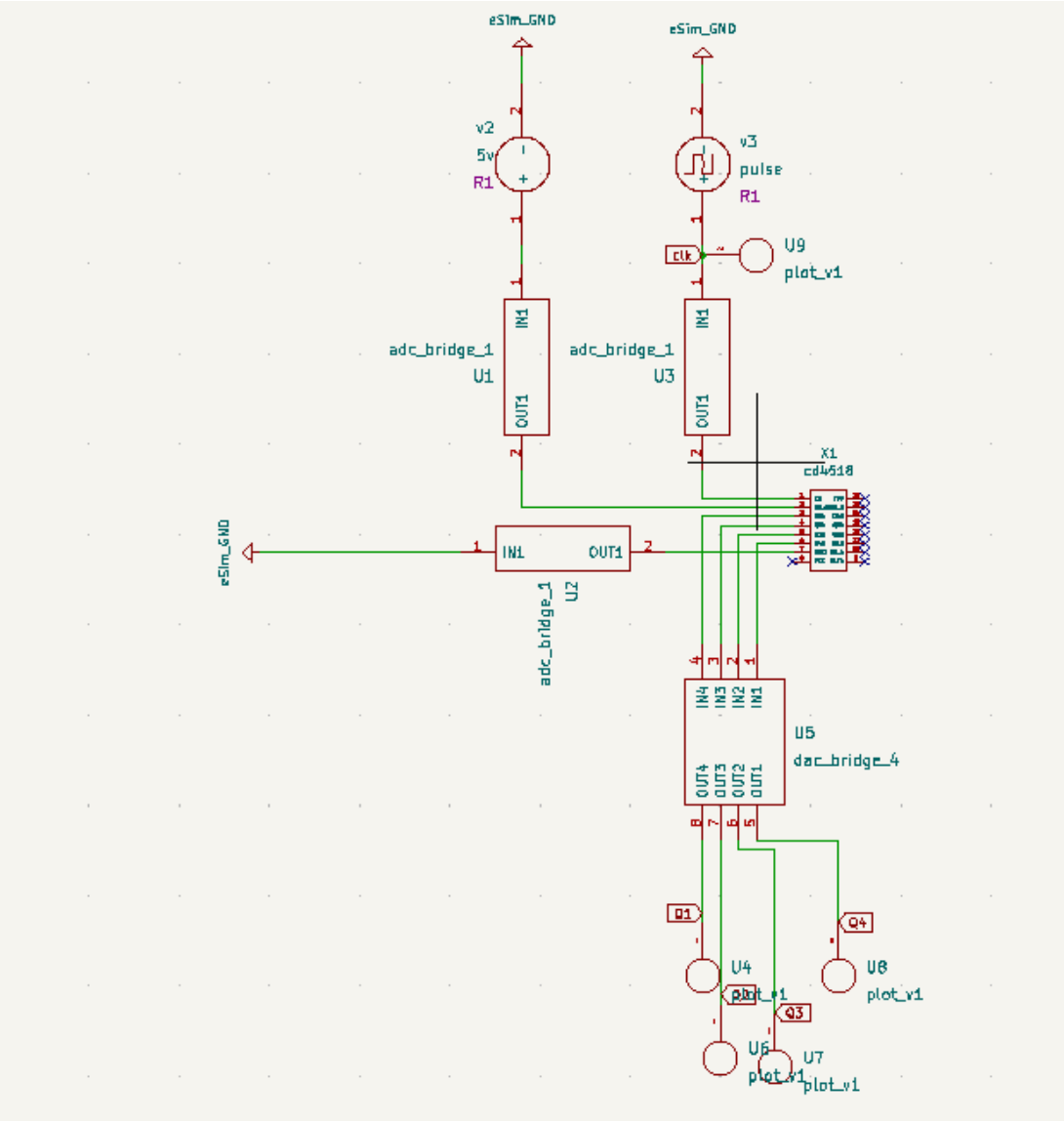

Figure 4.3: Test circuit used for functional validation of CD4518B

4.1.4 Input and Output Plots

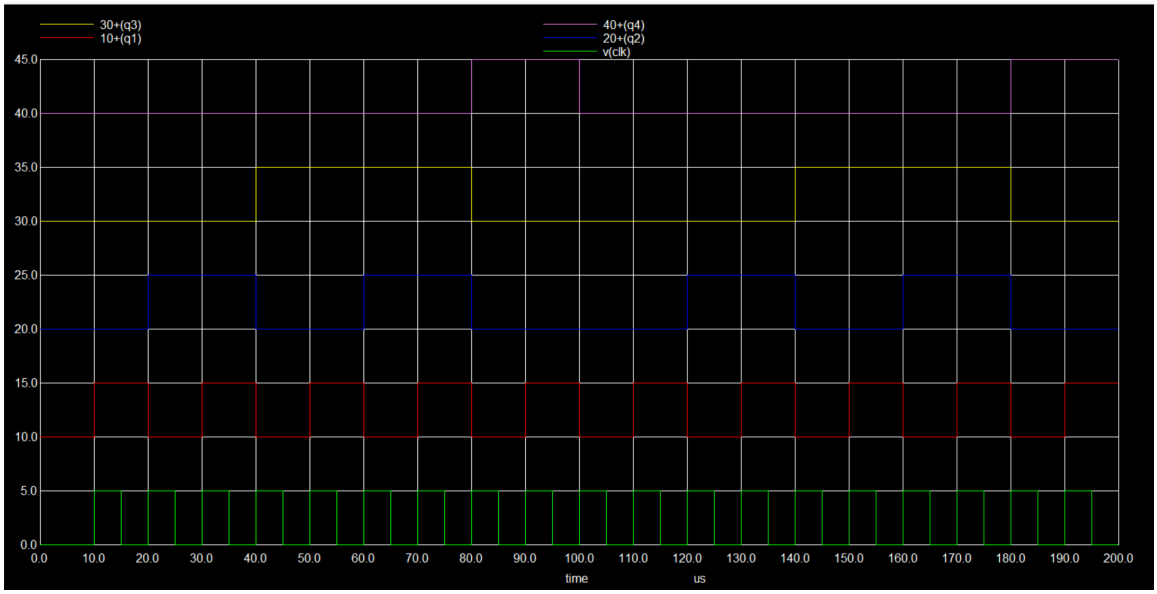

Figure 4.4: Simulated waveform outputs obtained for CD4518B test circuit

4.2 CD4520

Description: Dual binary counter IC.

General Description: The CD4520 is a dual 4-bit binary counter consisting of two independent counter stages that advance on the rising edge of the clock. Each stage can be used for frequency division, event counting, or timing applications. The device supports synchronous counting and low-power CMOS operation, making it suitable for digital logic and clocking systems.

4.2.1 IC Layout

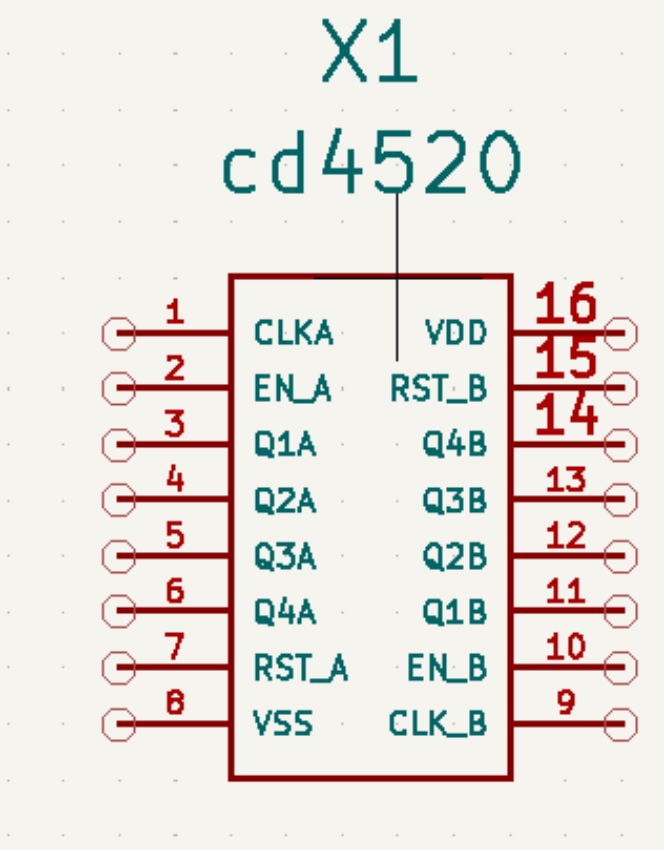

Figure 4.5: Pin configuration of CD4520

4.2.2 Subcircuit Schematic Diagram

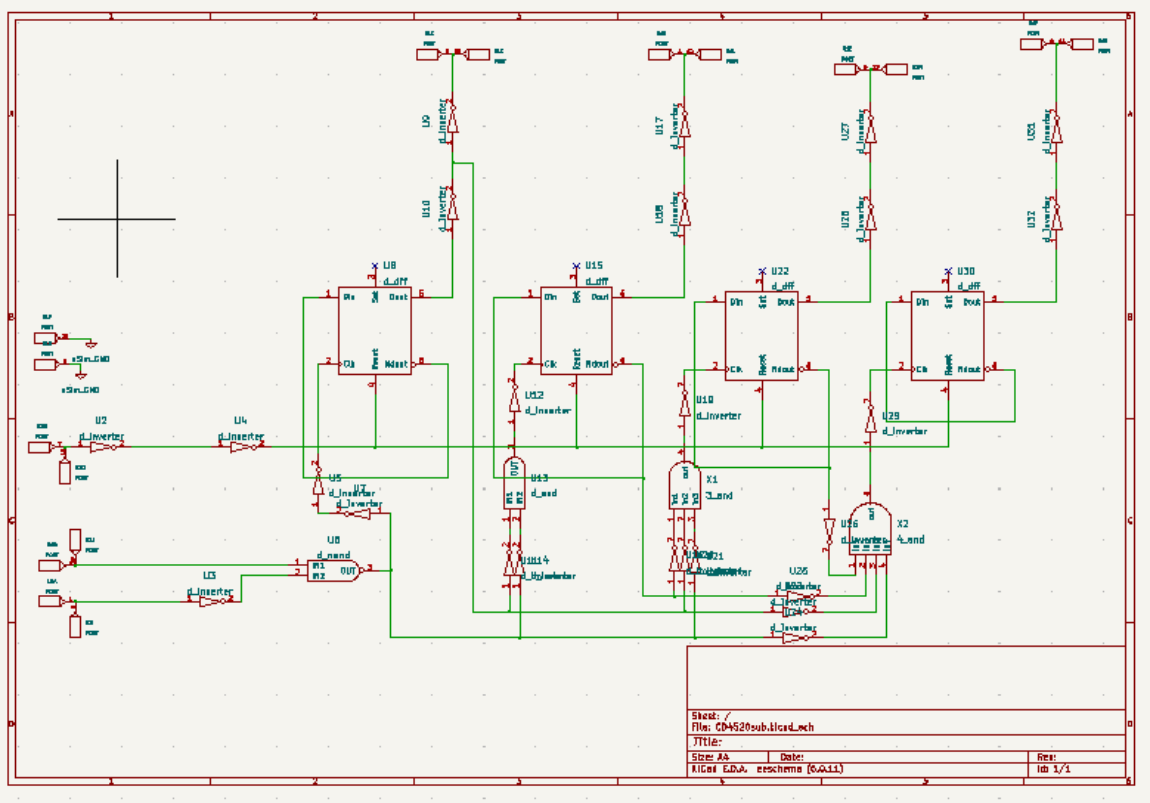

Figure 4.6: Subcircuit schematic diagram of CD4520 implemented in eSim

4.2.3 Test Circuit

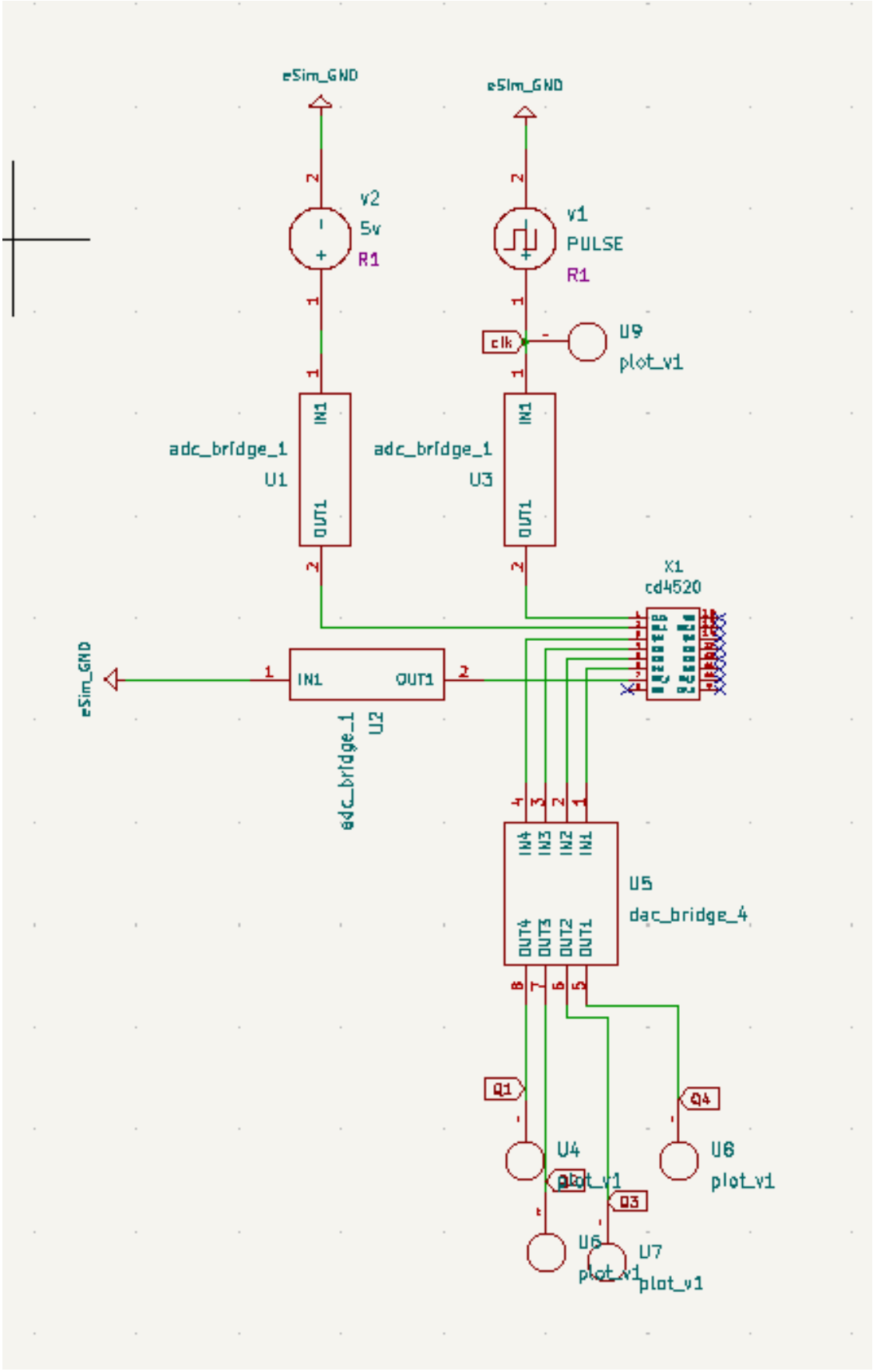

Figure 4.7: Test circuit used for functional validation of CD4520

4.2.4 Input and Output Plots

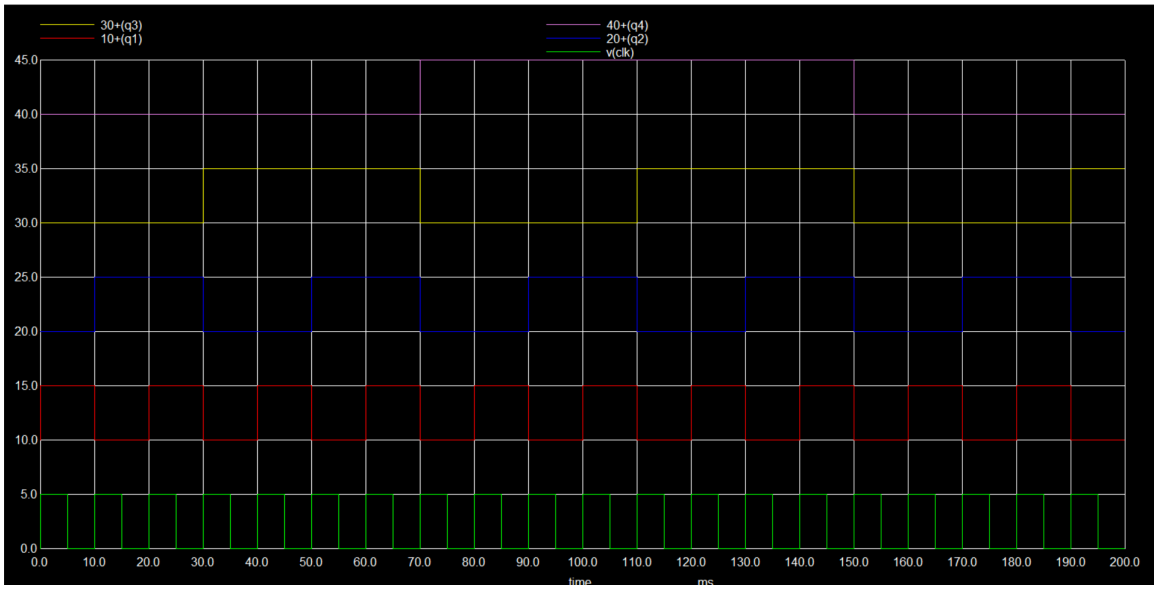

Figure 4.8: Simulated input/output waveforms obtained for CD4520 test circuit

4.3 74HCT573

Description: Octal D-type transparent latch.

General Description: The 74HCT573 is an octal D-type latch with 3-state outputs. Data on the D inputs is latched to the Q outputs when the latch enable signal is active. The device supports bidirectional bus interfacing and buffering operations and is commonly used for temporary data storage, address latching, and microprocessor system interfacing. Its HCT CMOS implementation provides TTL logic compatibility and low power consumption.

4.3.1 IC Layout

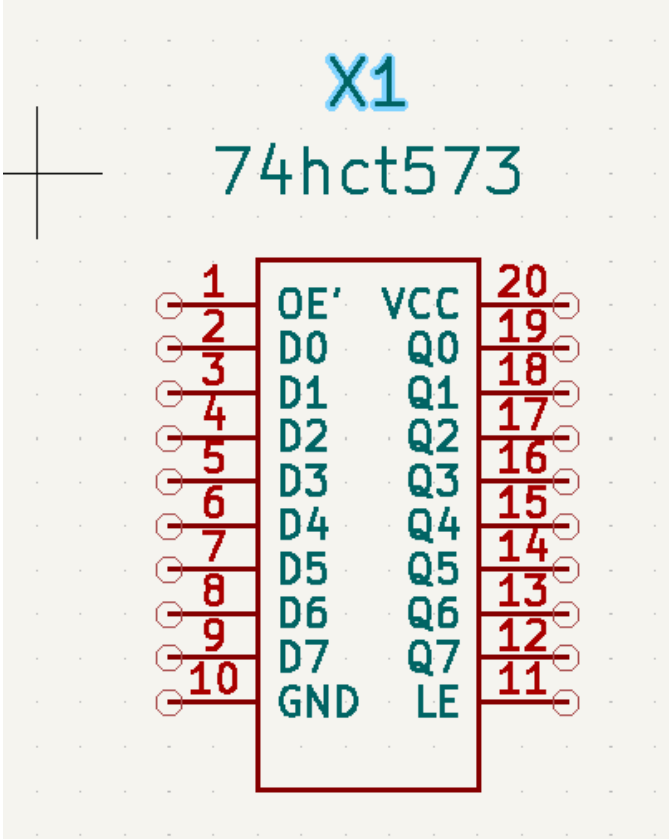

Figure 4.9: Pin configuration of 74HCT573

4.3.2 Subcircuit Schematic Diagram

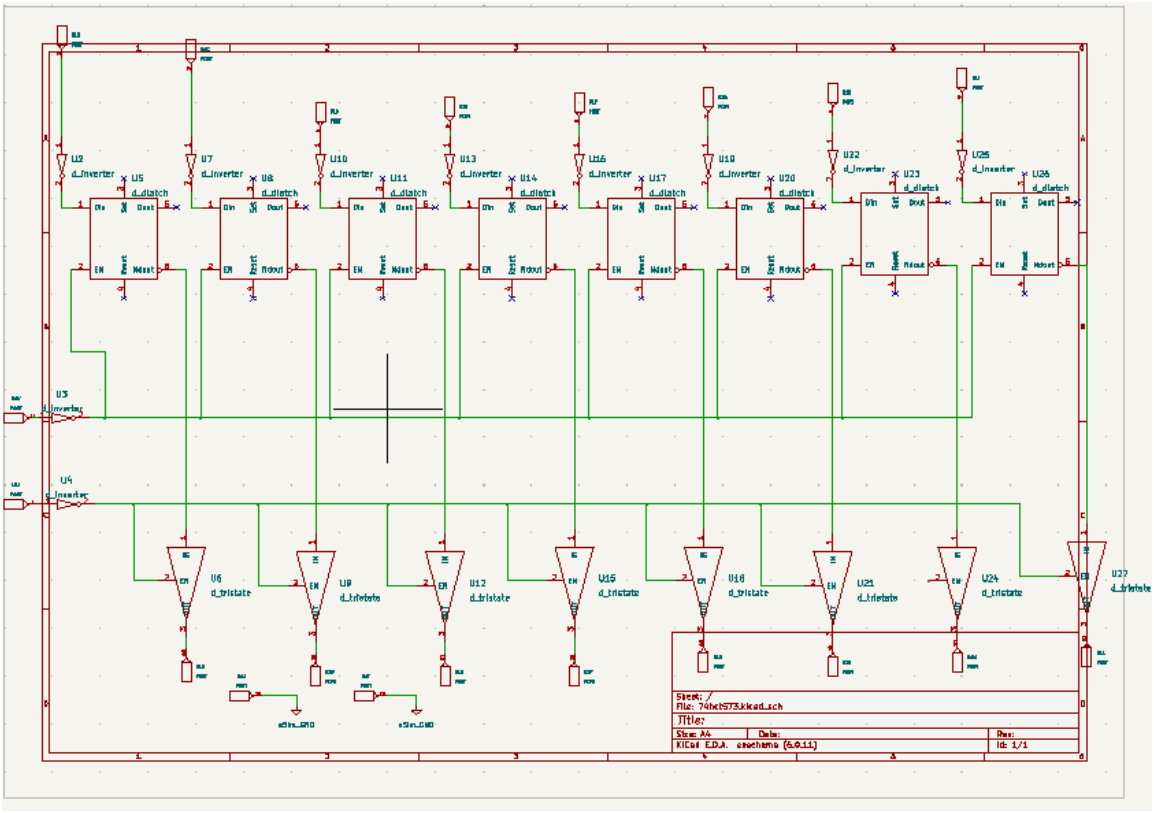

Figure 4.10: Subcircuit schematic diagram of 74HCT573 implemented in eSim

4.3.3 Test Circuit

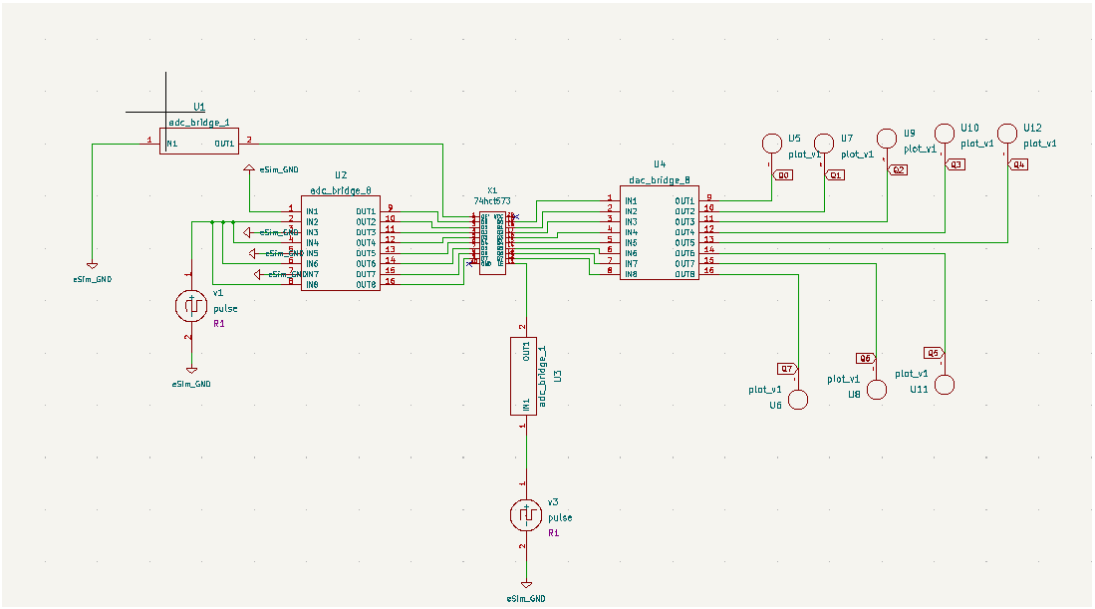

Figure 4.11: Test circuit used for functional validation of 74HCT573

4.3.4 Input and Output Plots

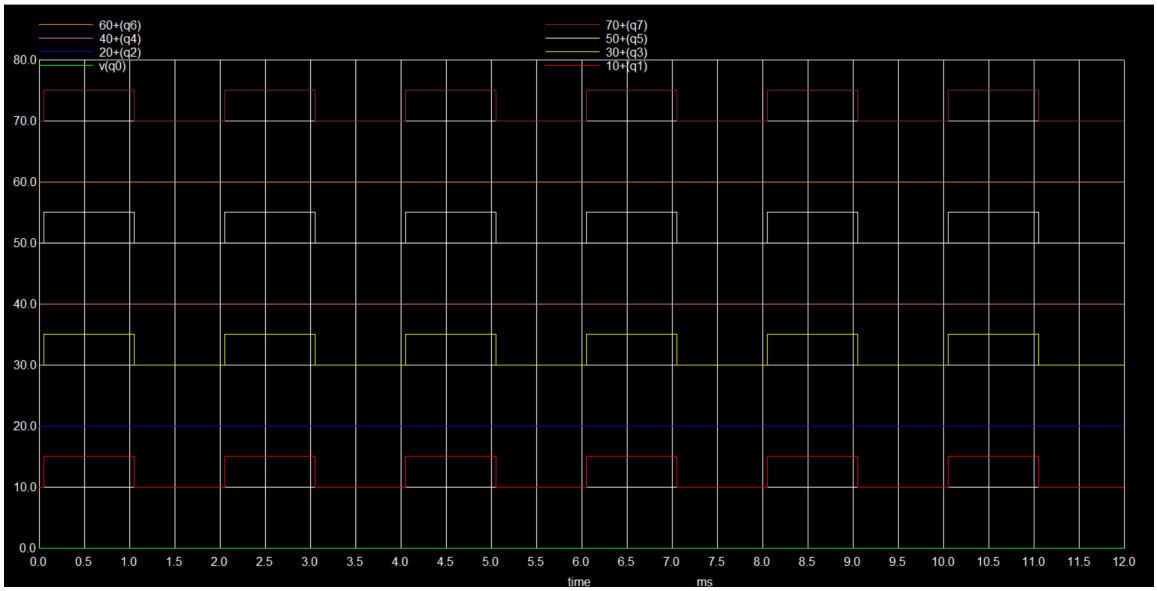

Figure 4.12: Simulated input/output waveforms for 74HCT573 test circuit

4.4 74LS257

Description: Quad 2-to-1 multiplexer with 3-state outputs.

General Description: The 74LS257 is a quad 2-to-1 data multiplexer capable of selecting one of two data sources for output on four parallel channels. The device includes a common data-select line and an output-enable control, allowing the outputs to be placed in a high-impedance state for bus-oriented applications. The TTL-based LS family provides high switching speed, making the 74LS257 suitable for digital logic, data routing, and memory addressing operations.

4.4.1 IC Layout

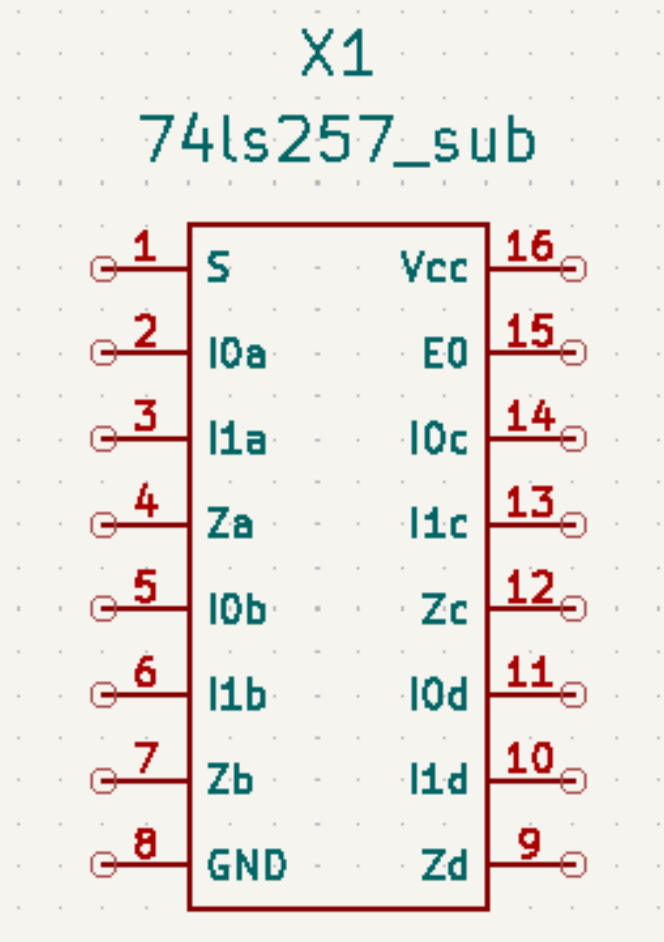

Figure 4.13: Pin configuration of 74LS257

4.4.2 Subcircuit Schematic Diagram

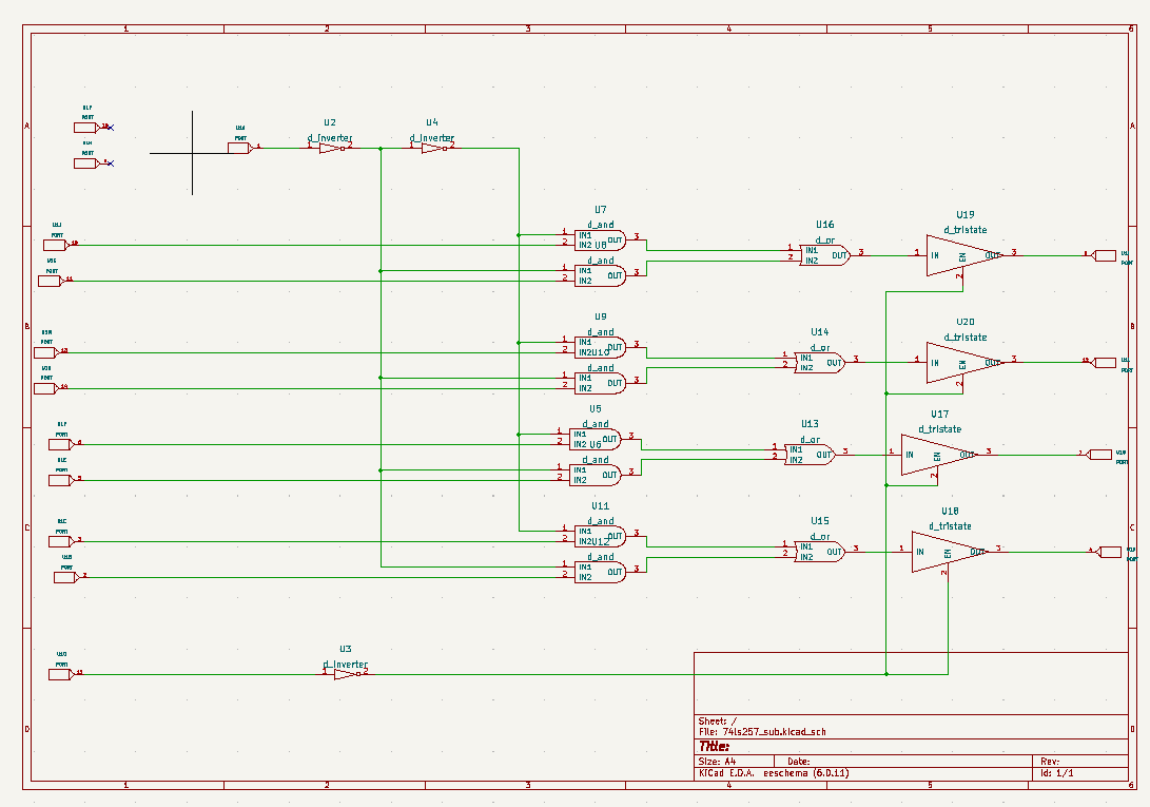

Figure 4.14: Subcircuit schematic diagram of 74LS257 implemented in eSim

4.4.3 Test Circuit

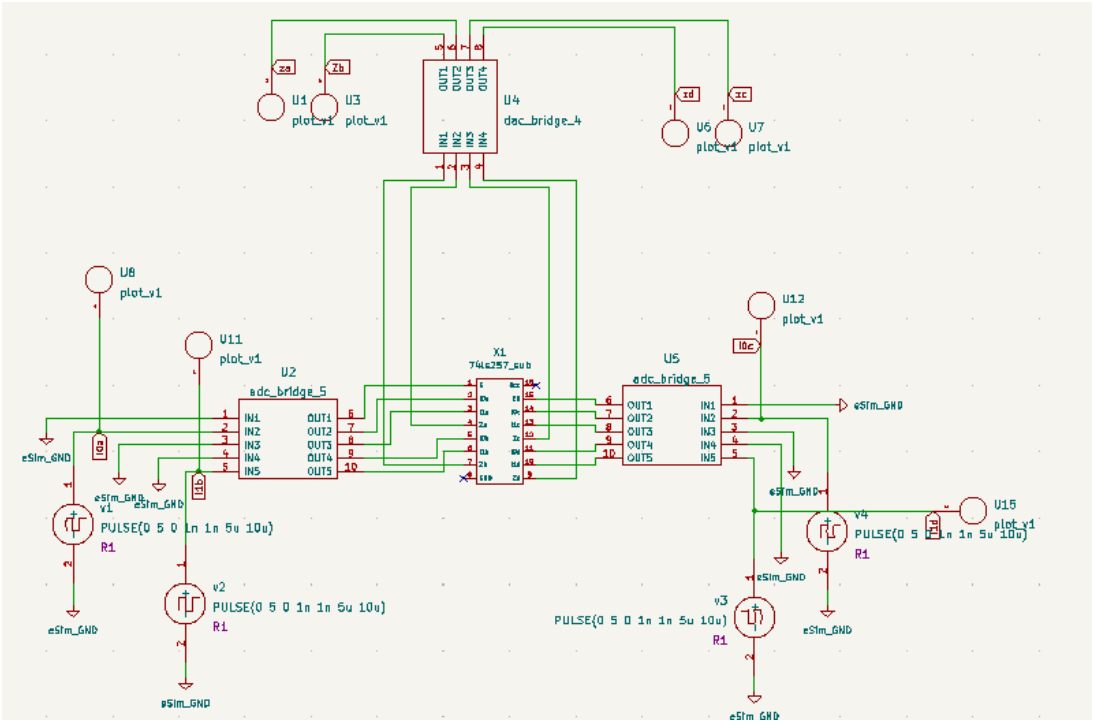

Figure 4.15: Test circuit used for functional validation of 74LS257

4.4.4 Input and Output Plots

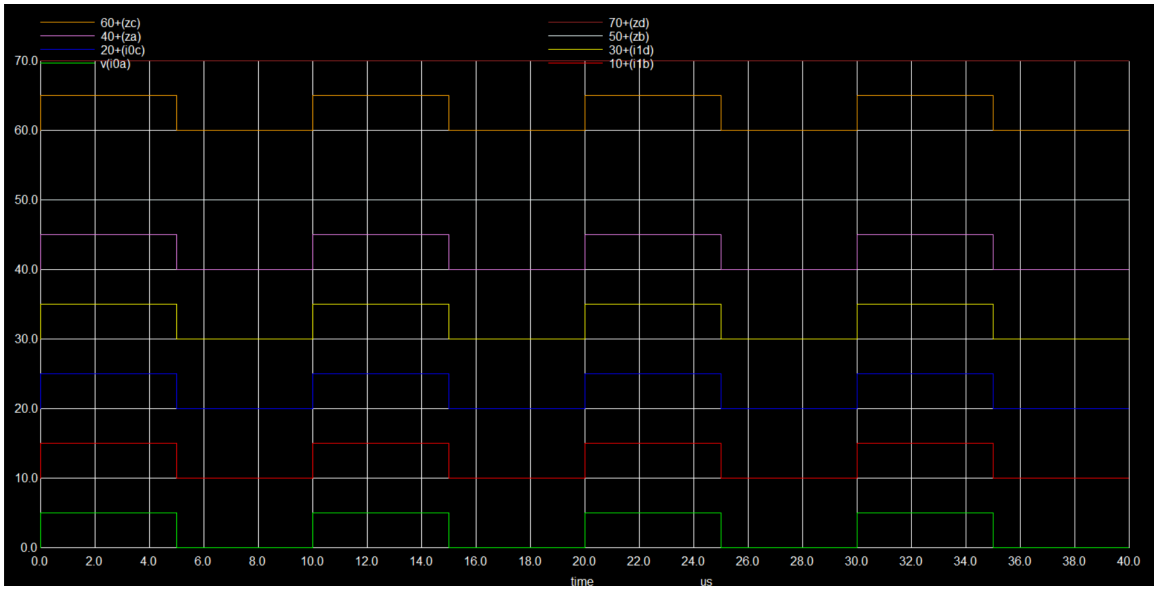

Figure 4.16: Simulated input/output waveforms for 74LS257 test circuit

4.5 SN74160

Description: Synchronous 4-bit decade counter.

General Description: The SN74160 is a 4-bit synchronous decade counter that counts from 0 to 9 and then resets to 0 on the next clock pulse. It includes synchronous clear, load, and enable controls, allowing flexible counting and preset operations. The device is commonly used in frequency division, digital timing, and event counting systems. As part of the TTL family, it offers fast switching characteristics suitable for high-speed logic applications.

4.5.1 IC Layout

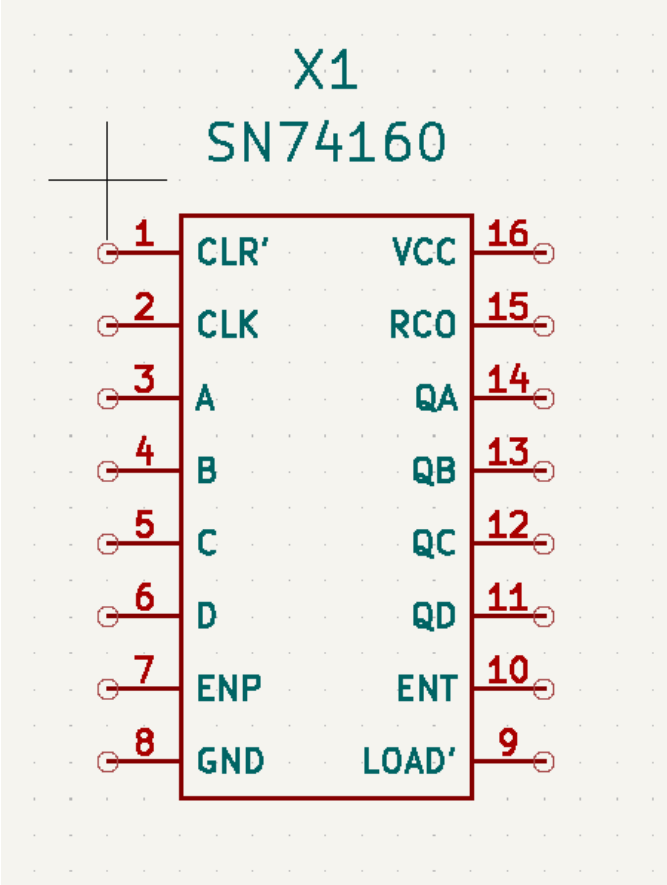

Figure 4.17: Pin configuration of SN74160

4.5.2 Subcircuit Schematic Diagram

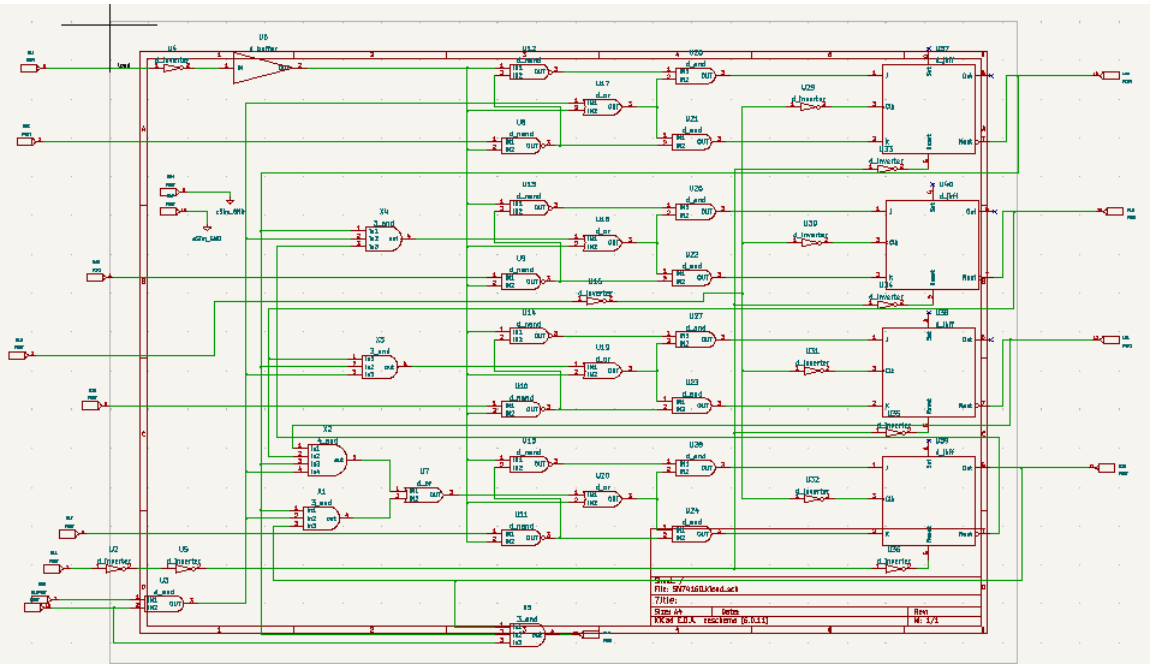

Figure 4.18: Subcircuit schematic diagram of SN74160 implemented in eSim

4.5.3 Test Circuit

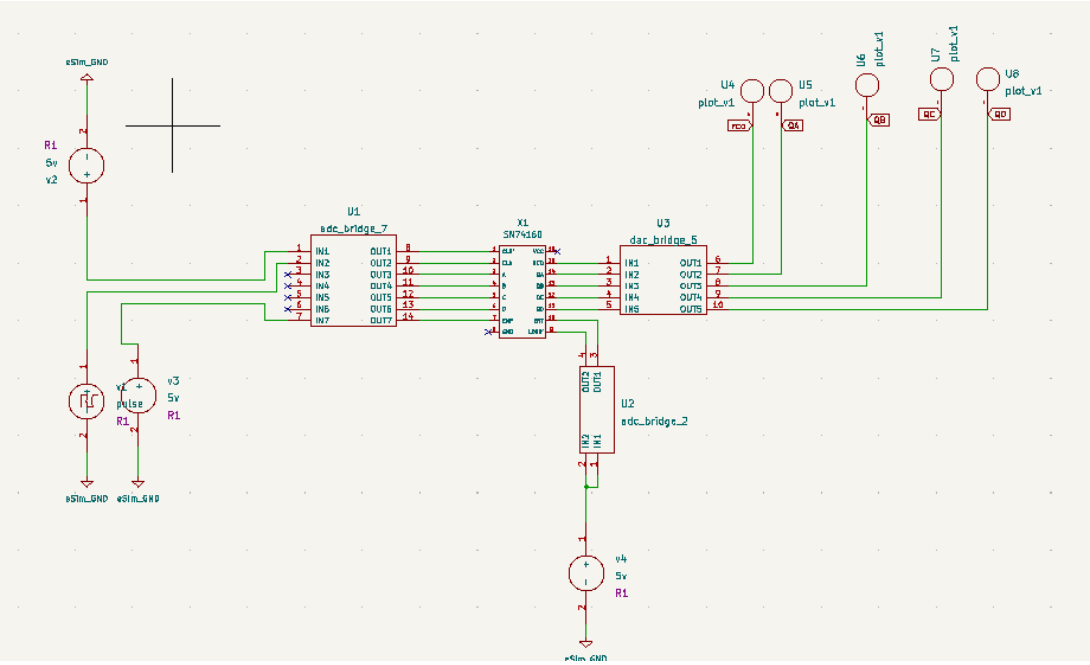

Figure 4.19: Test circuit used for functional validation of SN74160

4.5.4 Input and Output Plots

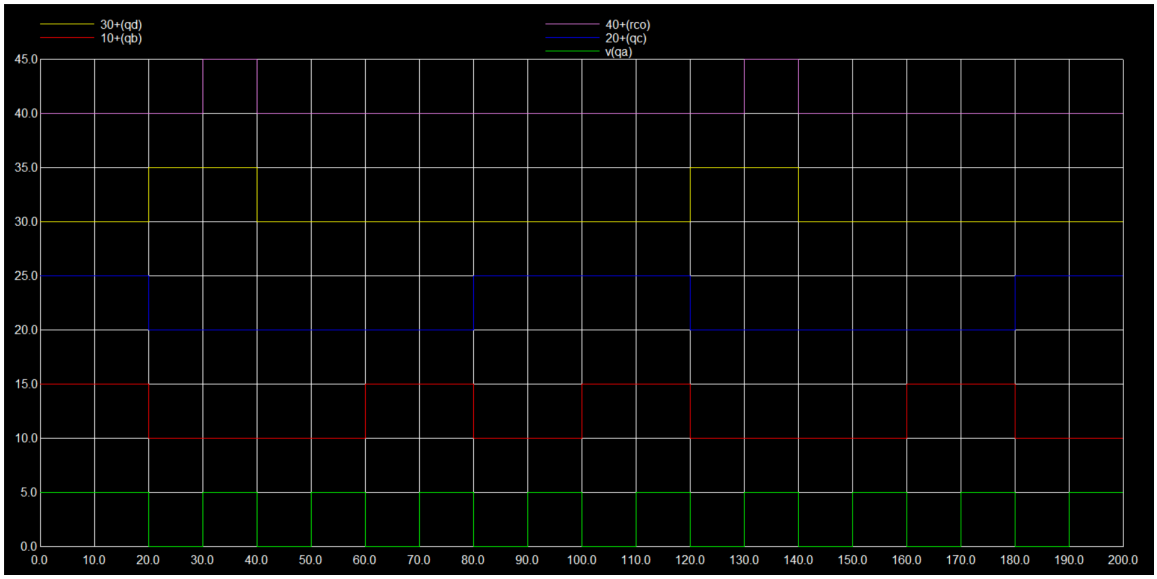

Figure 4.20: Simulated input/output waveforms for SN74160 test circuit

4.6 74HC377

Description: Octal D-type flip-flop with clock enable.

General Description: The 74HC377 consists of eight edge-triggered D-type flip-flops that latch input data on the rising edge of the clock signal when the enable input is asserted. The device is commonly used for temporary data storage, buffering, and synchronization in digital systems. Its CMOS implementation provides high-speed operation

with low power consumption, making it suitable for microprocessor and FPGA interfacing applications.

4.6.1 IC Layout

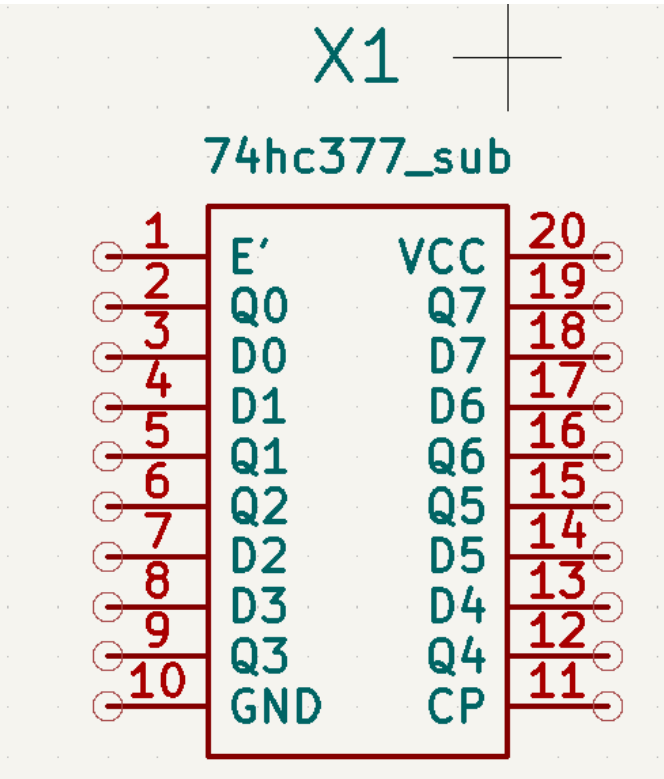

Figure 4.21: Pin configuration of 74HC377

4.6.2 Subcircuit Schematic Diagram

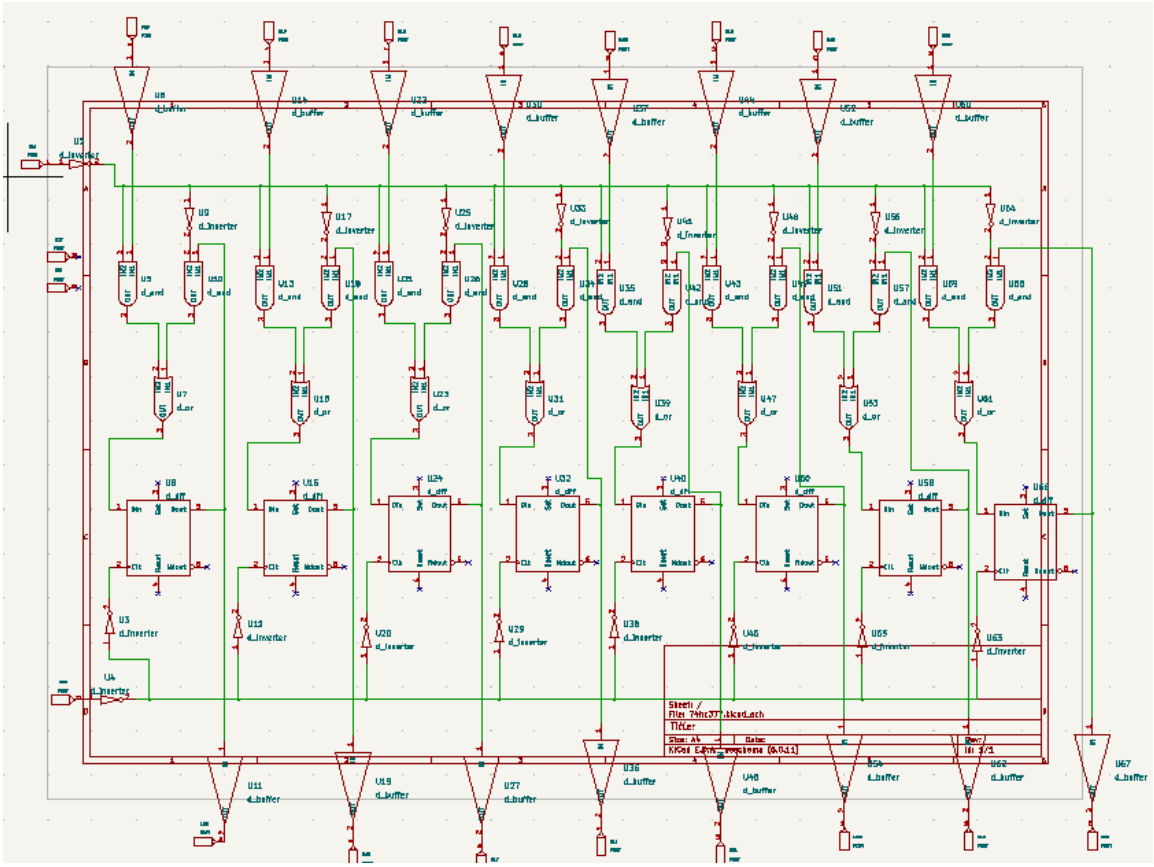

Figure 4.22: Subcircuit schematic diagram of 74HC377 implemented in eSim

4.6.3 Test Circuit

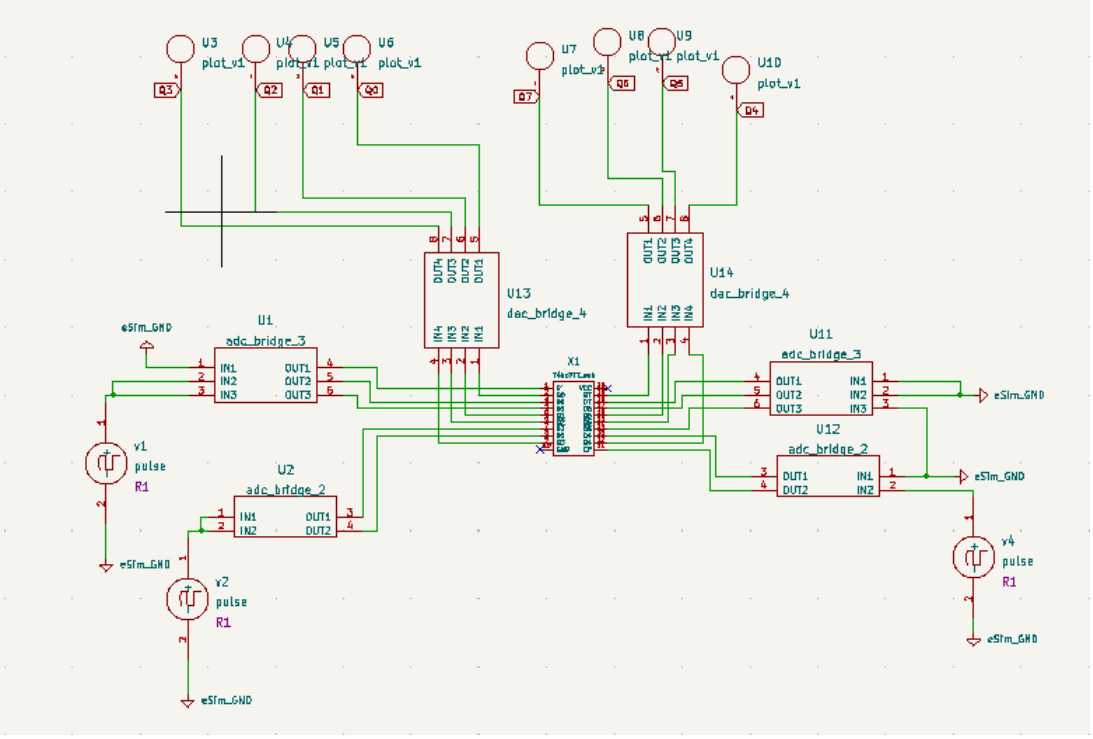

Figure 4.23: Test circuit used for functional validation of 74HC377

4.6.4 Input and Output Plots

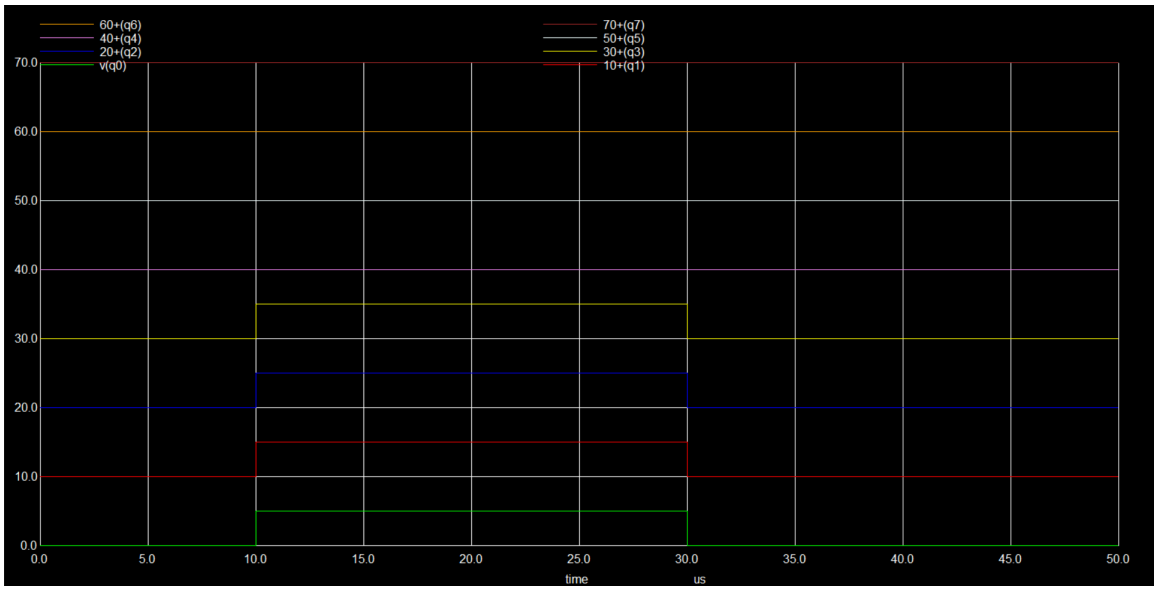

Figure 4.24: Simulated input/output waveforms for 74HC377 test circuit

4.7 HEF4502B

Description: Strobed hex non-inverting buffer.

General Description: The HEF4502B is a CMOS strobed hex buffer consisting of six non-inverting buffer stages controlled by a common strobe input. When the strobe

signal is active, the input data is transferred to the corresponding output. When the strobe input is inactive, the stored output remains unchanged, allowing temporary data retention. The device provides high input impedance, high noise immunity, and low static power dissipation due to its CMOS implementation. Typical applications include signal buffering, bus driving, fan-out expansion, level shifting, and digital interfacing in mixed-logic environments.

4.7.1 IC Layout

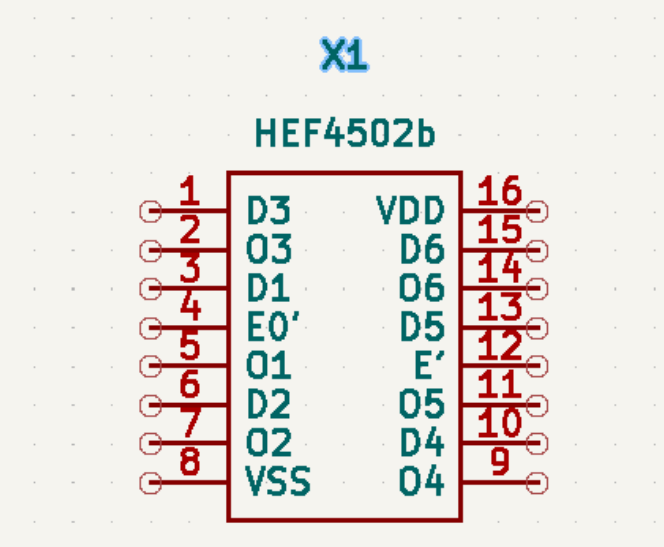

Figure 4.25: Pin configuration of HEF4502B

4.7.2 Subcircuit Schematic Diagram

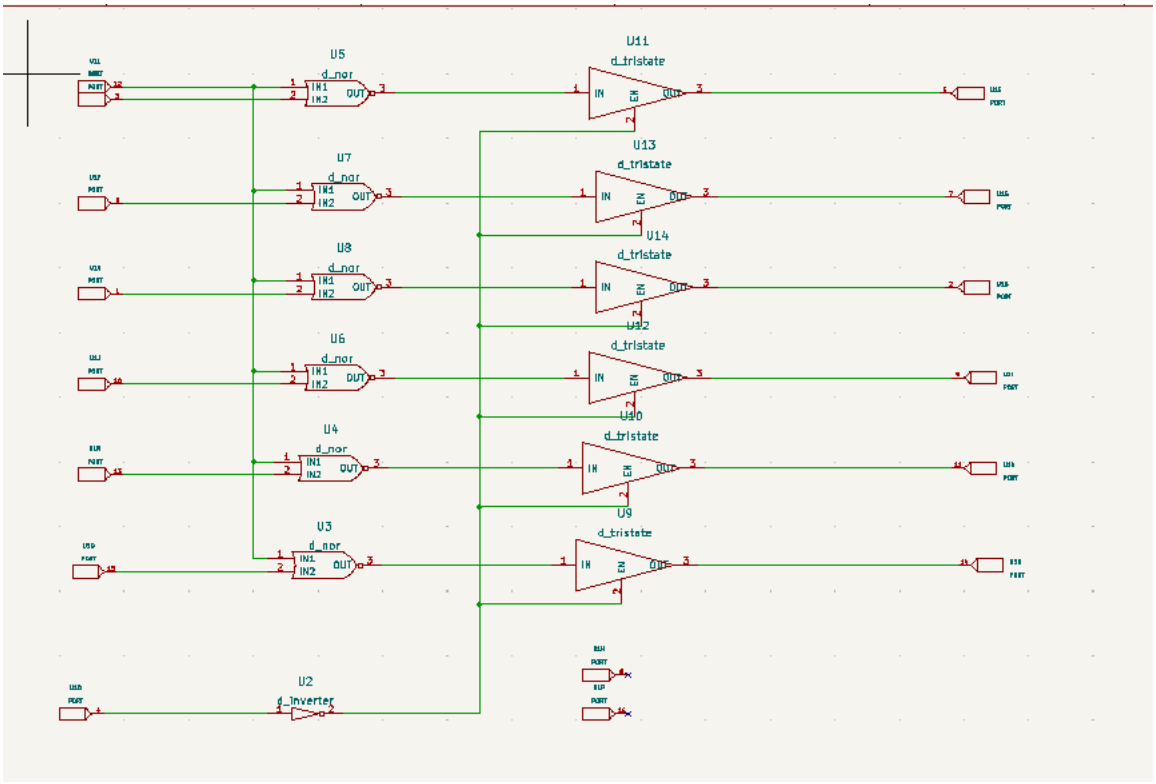

Figure 4.26: Subcircuit schematic diagram of HEF4502B implemented in eSim

4.7.3 Test Circuit

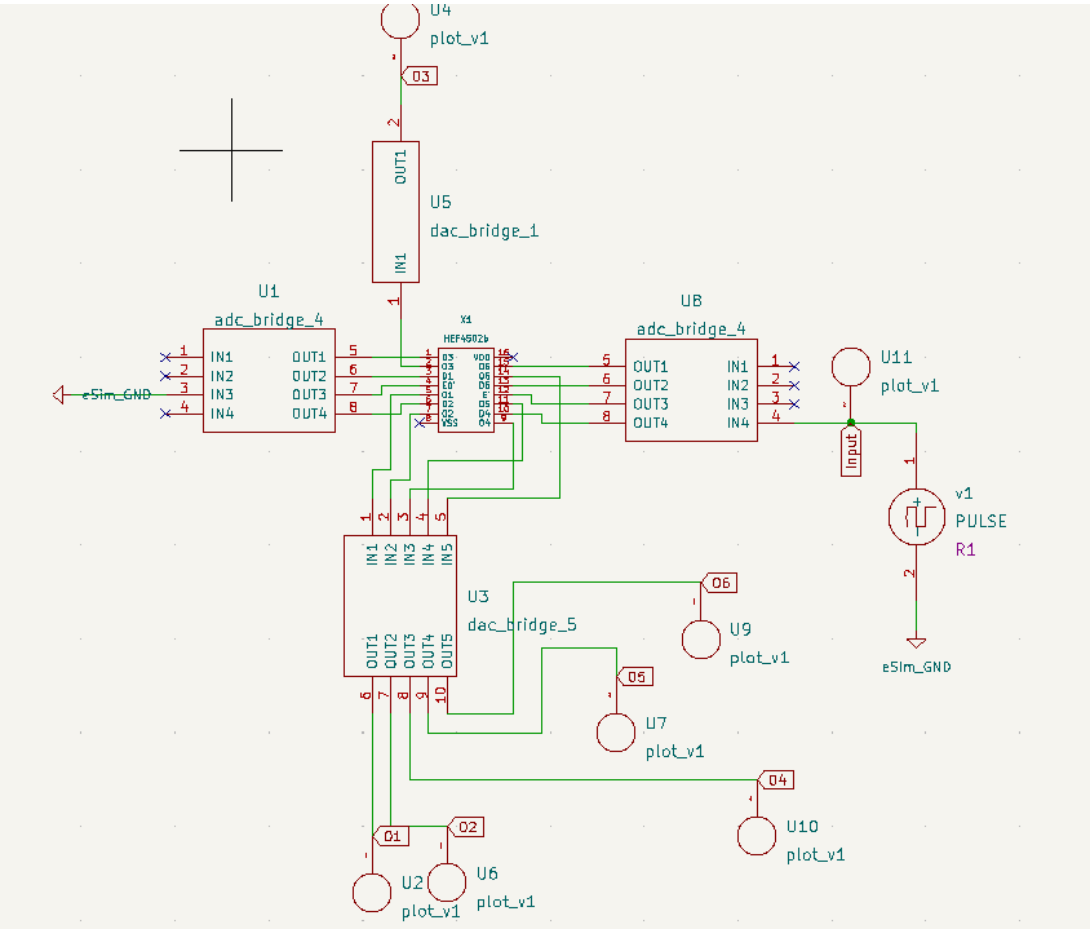

Figure 4.27: Test circuit used for functional validation of HEF4502B

4.7.4 Input and Output Plots

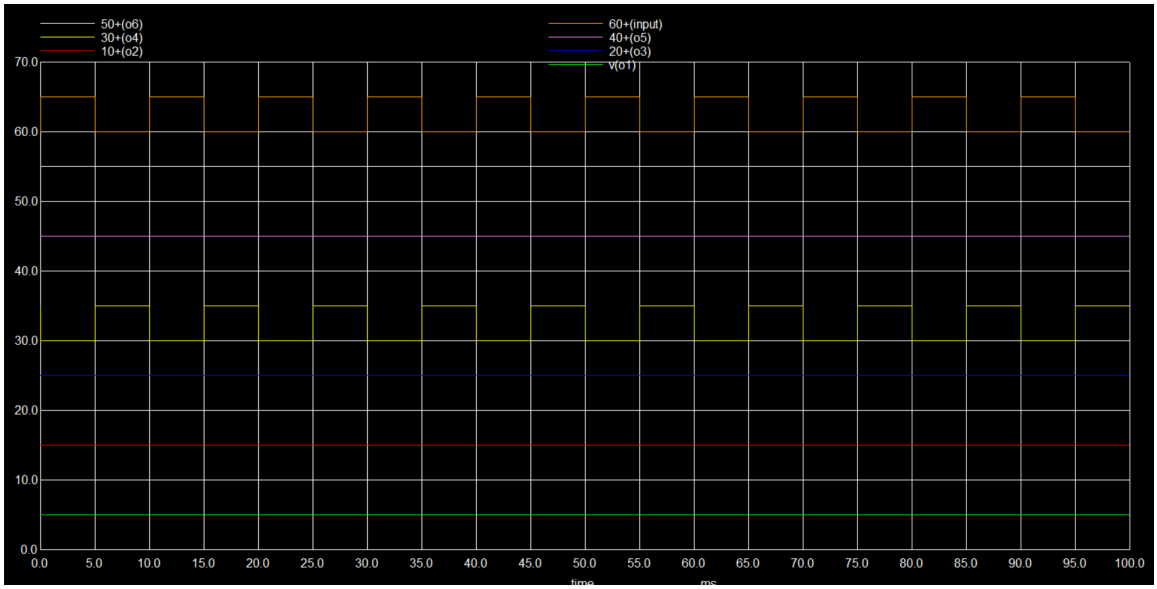

Figure 4.28: Simulated input/output waveforms for HEF4502B test circuit

4.8 CA3094

Description: Operational transconductance amplifier (OTA) with integrated Darlington buffer.

General Description: The CA3094 is a monolithic operational transconductance amplifier featuring a built-in Darlington output transistor stage. The OTA converts an input differential voltage into an output current, which can be externally controlled through a bias current input. The integrated Darlington buffer allows voltage-mode interfacing and enables higher output drive capability than a standard OTA. The device is commonly used in AGC circuits, filters, oscillators, audio processing, and non-linear analog designs where gain control and current-mode operation are required. The CA3094 offers high linearity in current-controlled gain and wide dynamic range for analog signal processing applications.

4.8.1 IC Layout

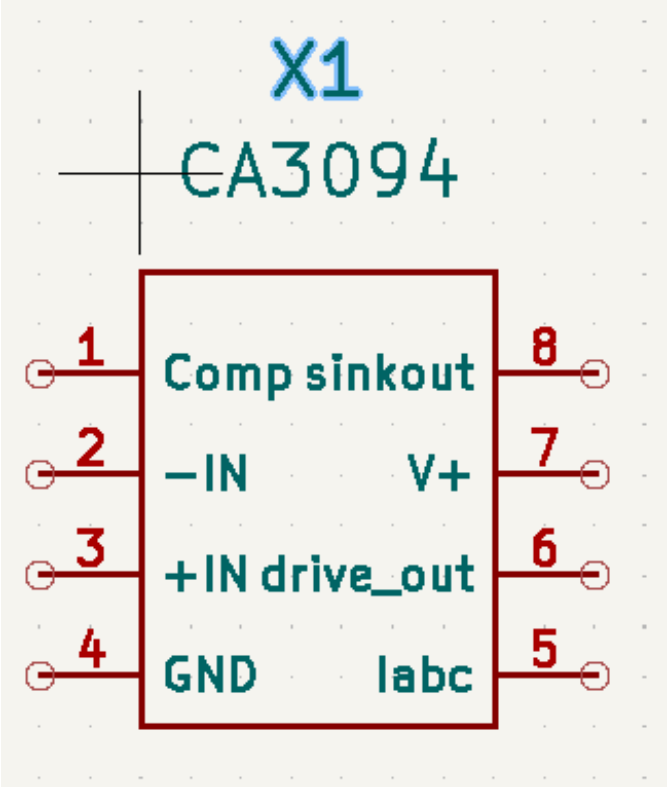

Figure 4.29: Pin configuration of CA3094

4.8.2 Subcircuit Schematic Diagram

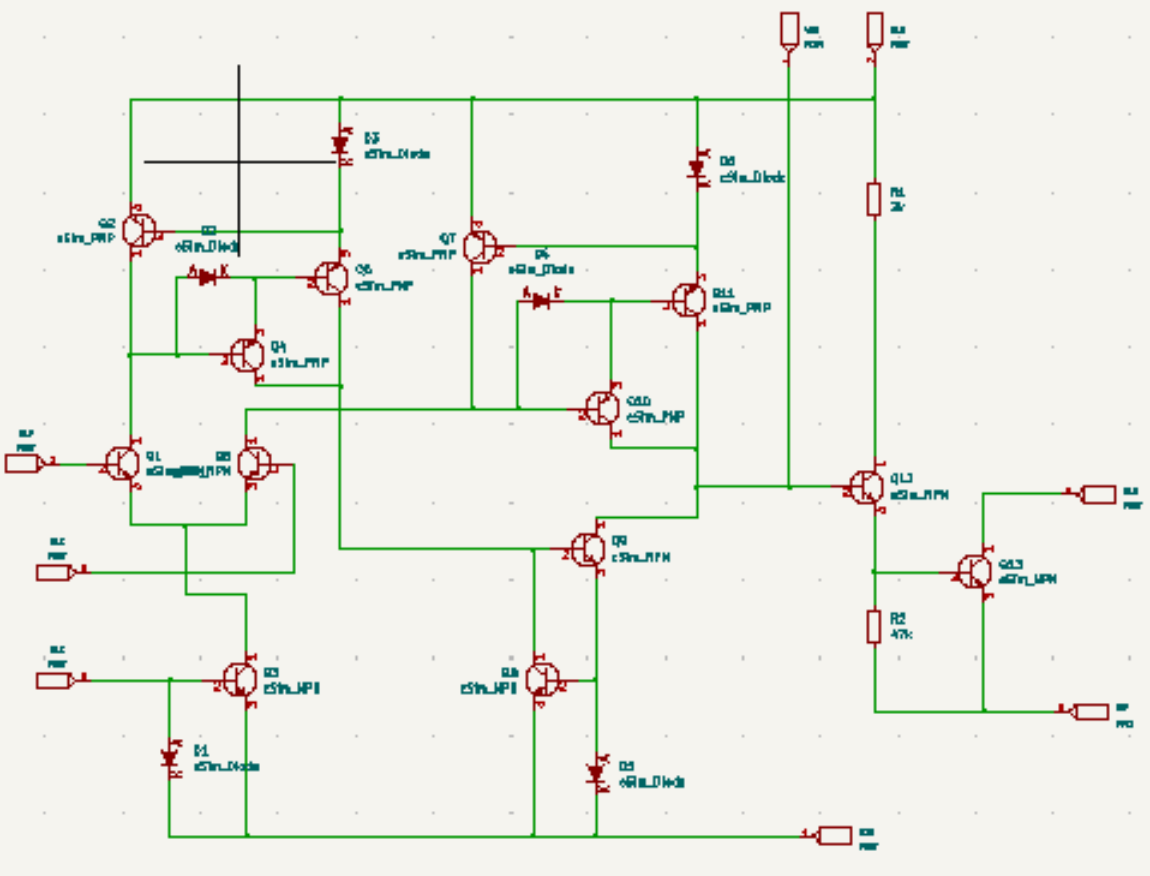

Figure 4.30: Subcircuit schematic diagram of CA3094 implemented in eSim

4.8.3 Test Circuit

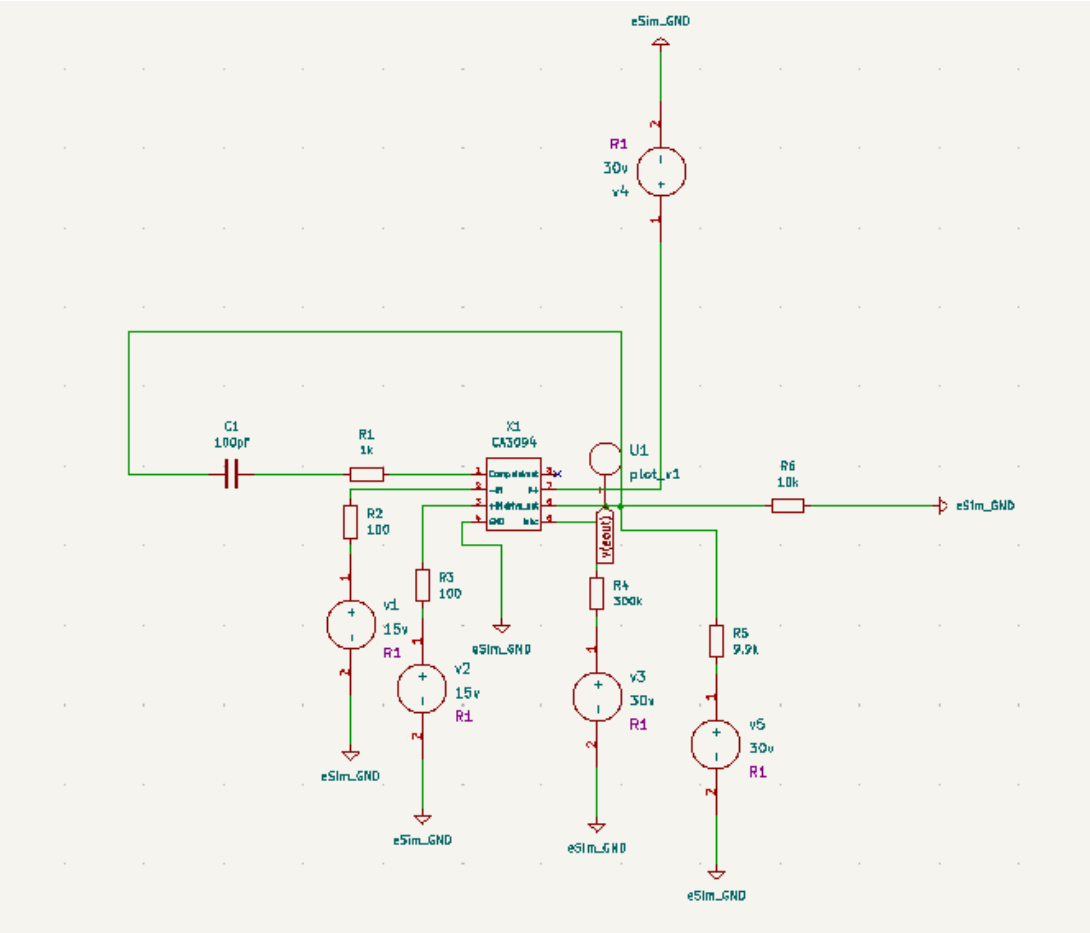

Figure 4.31: Test circuit used for functional validation of CA3094

4.8.4 Input and Output Plots

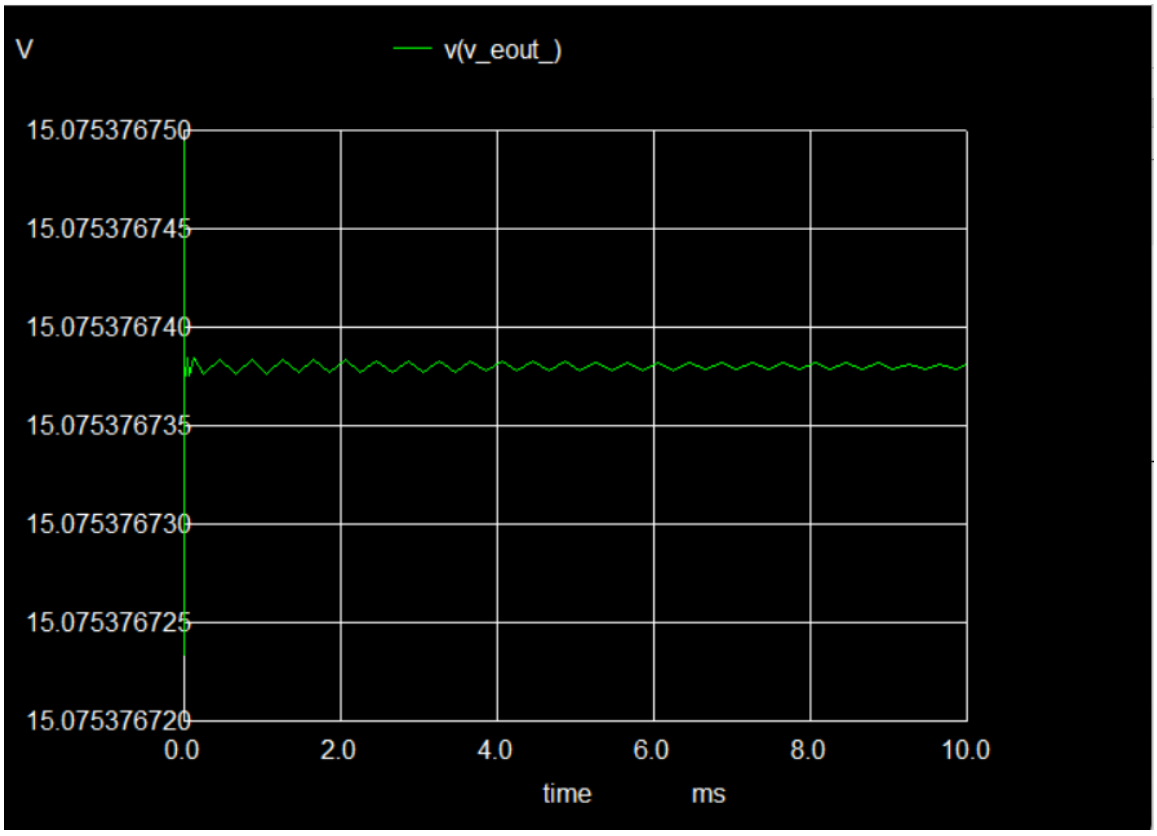

Figure 4.32: Simulated input/output waveforms for CA3094 test circuit

4.9 LM387

Description: Dual low-noise audio preamplifier.

General Description: The LM387 is a dual low-noise preamplifier designed for audio signal conditioning and microphone-level amplification. It integrates two independent amplifier channels with high input impedance and low distortion characteristics, making it suitable for audio recording, communication equipment, and instrumentation systems. The device provides voltage gain with low noise floor, supports single-supply operation, and is intended for preamplifier stages preceding power amplification or processing circuitry.

4.9.1 IC Layout

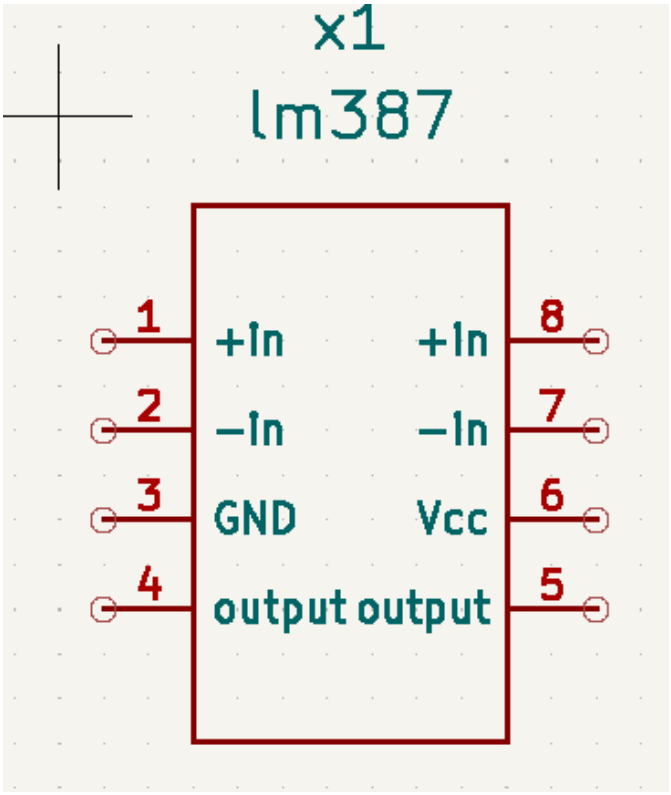

Figure 4.33: Pin configuration of LM387

4.9.2 Subcircuit Schematic Diagram

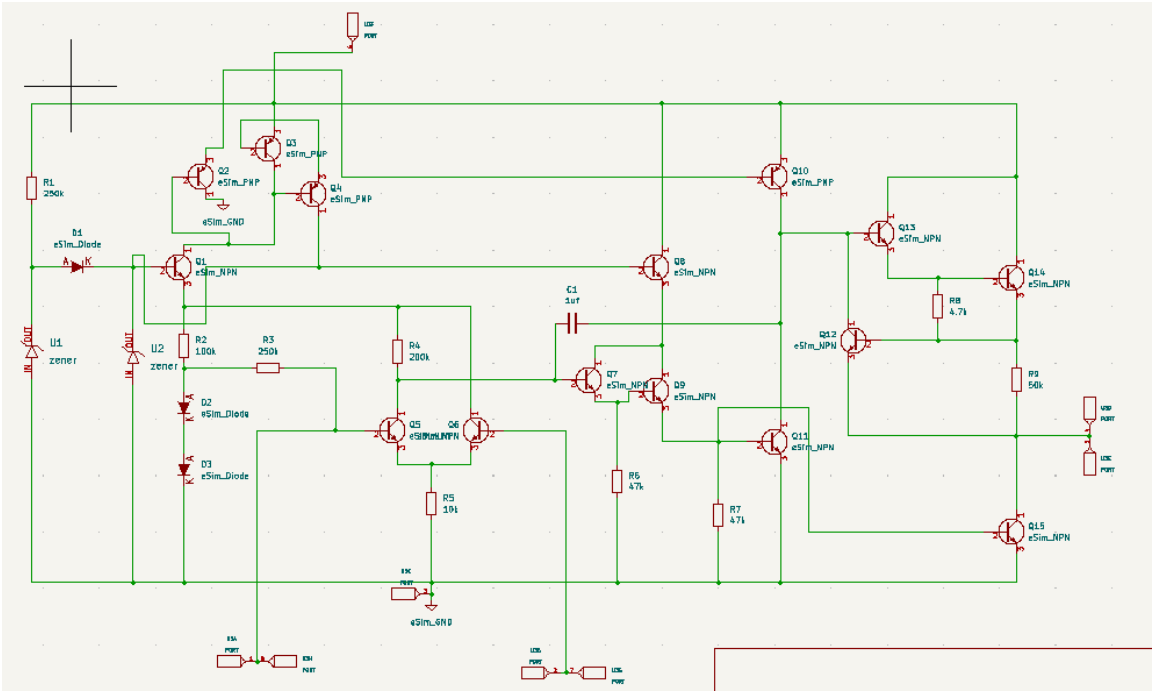

Figure 4.34: Subcircuit schematic diagram of LM387 implemented in eSim

4.9.3 Test Circuit

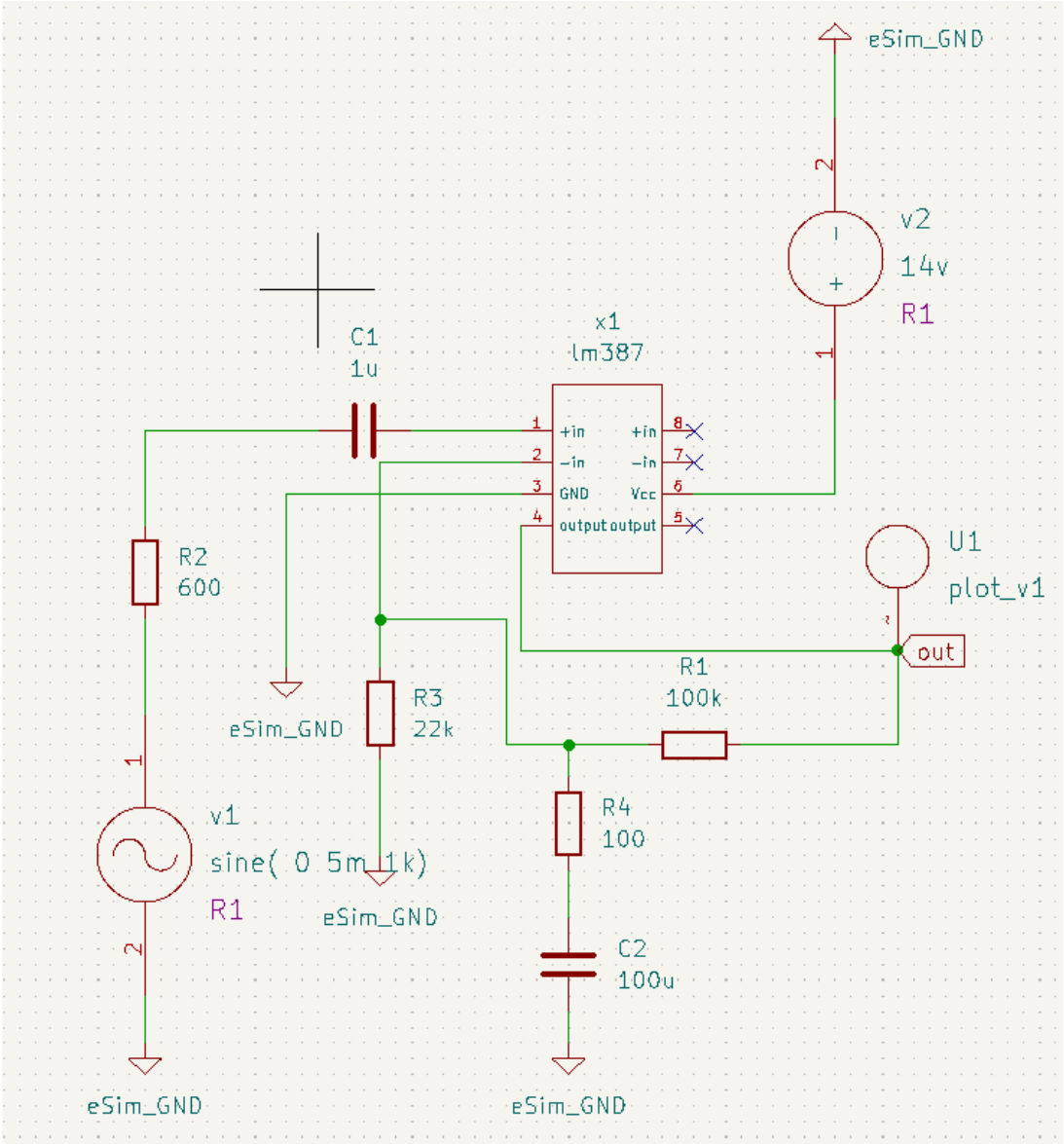

Figure 4.35: Test circuit used for functional validation of LM387

4.9.4 Input Plots

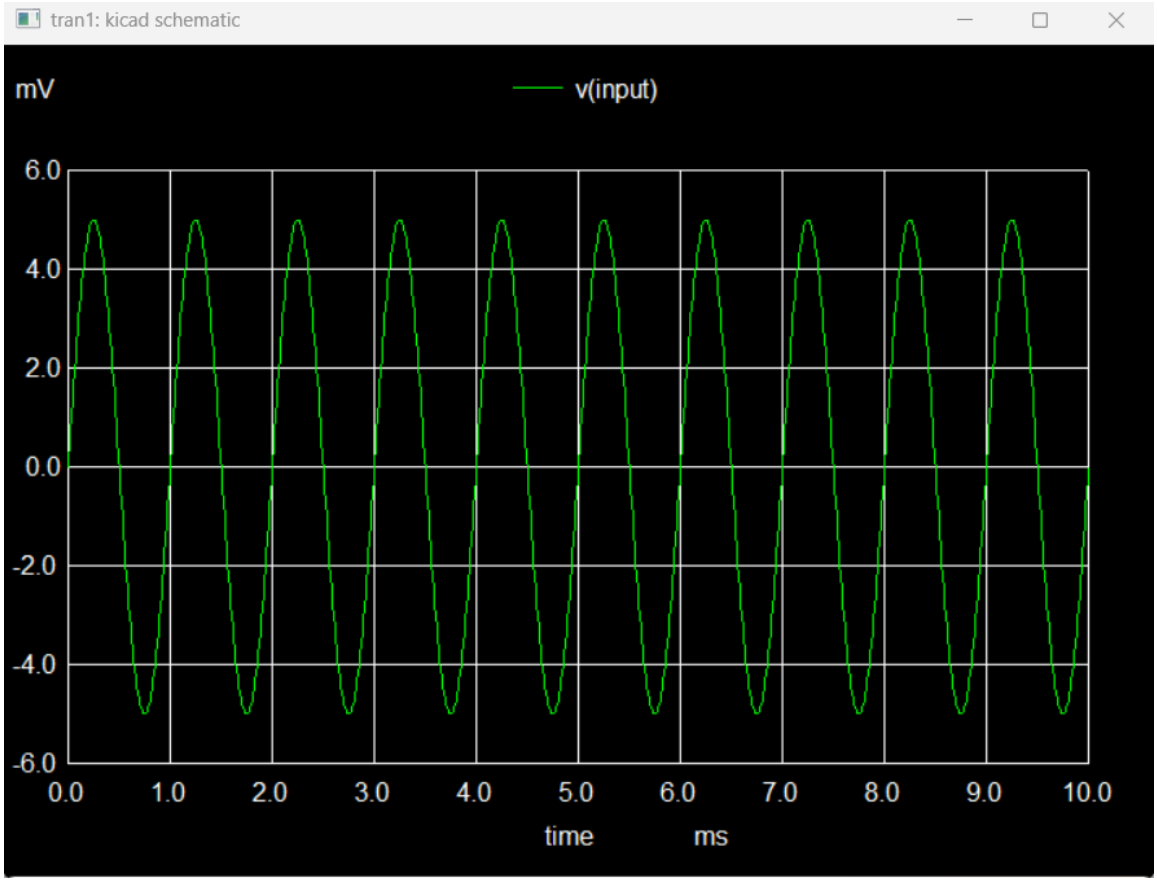

Figure 4.36: Simulated input waveform for LM387 test circuit

4.9.5 Output Plots

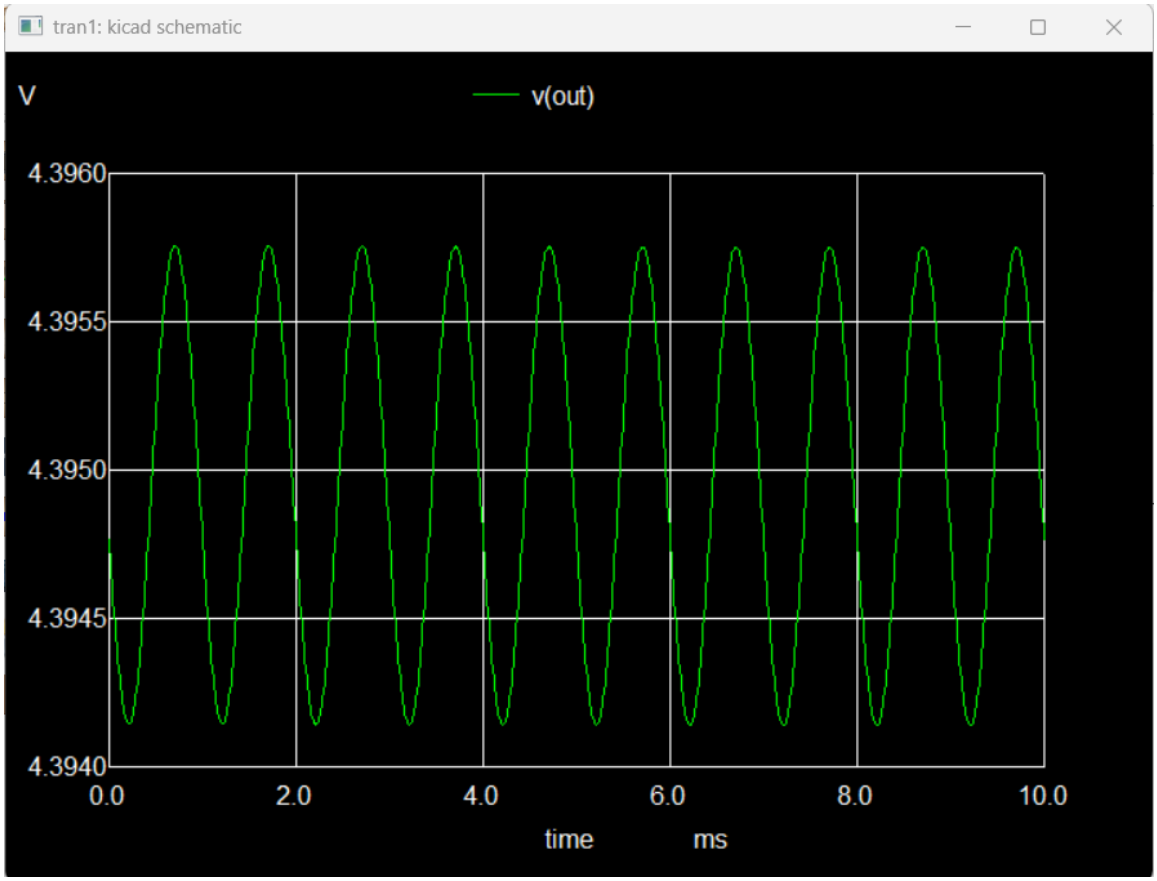

Figure 4.37: Simulated output waveform for LM387 test circuit

4.10 MC1514

Description: Dual high-speed differential voltage comparator.

General Description: The MC1514 is a dual high-speed differential comparator that compares two analog input voltages and produces corresponding logic-level outputs. The device is capable of fast switching and offers TTL-compatible output stages, making it suitable for interfacing with standard digital logic families. Differential input operation provides improved immunity against noise and common-mode disturbances. Typical applications include level detection, zero-cross detection, pulse shaping, signal conditioning, and communication interface circuits where rapid voltage comparison is required.

4.10.1 IC Layout

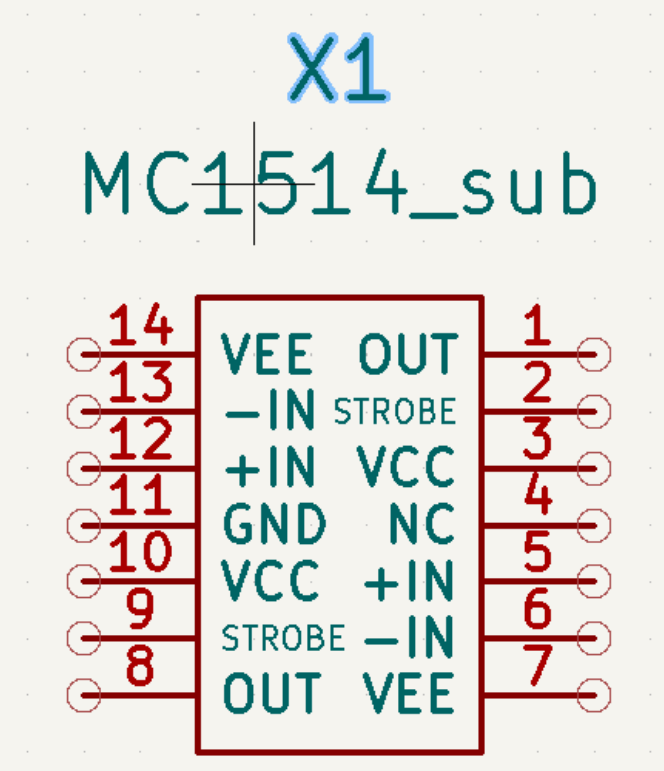

Figure 4.38: Pin configuration of MC1514

4.10.2 Subcircuit Schematic Diagram

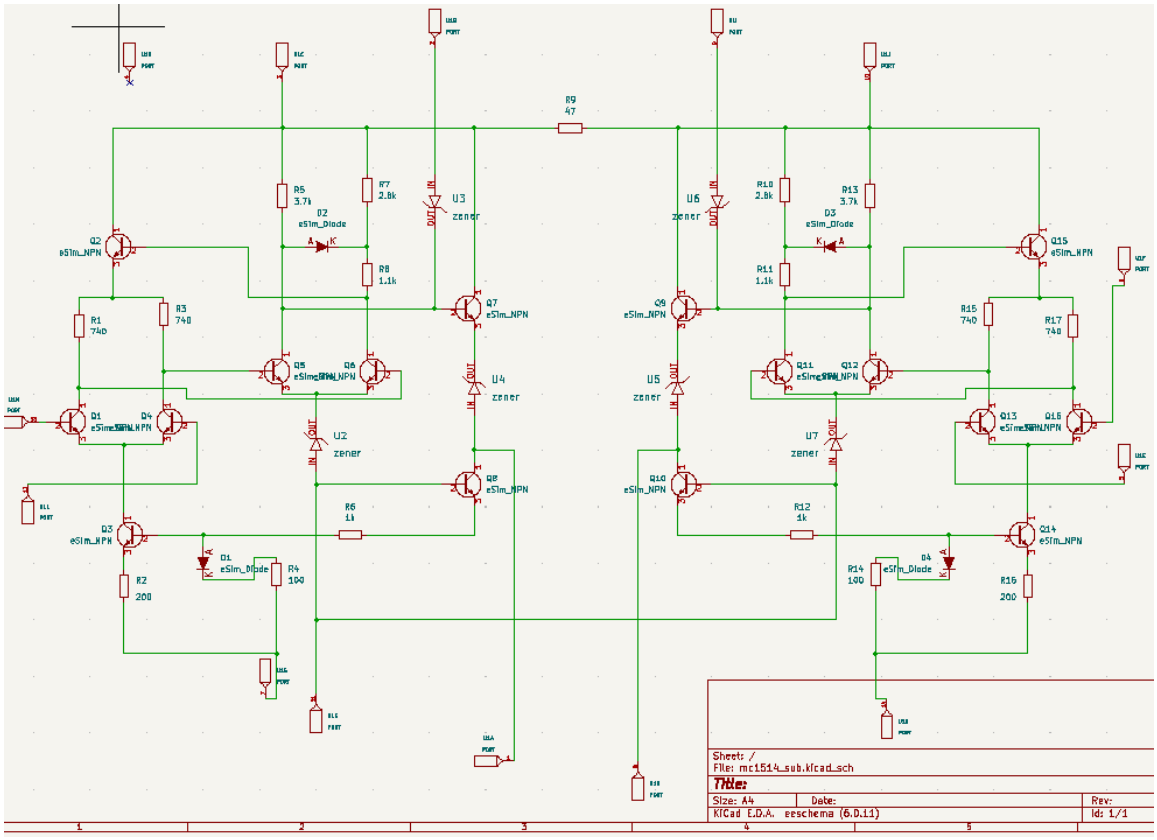

Figure 4.39: Subcircuit schematic diagram of MC1514 implemented in eSim

4.10.3 Test Circuit

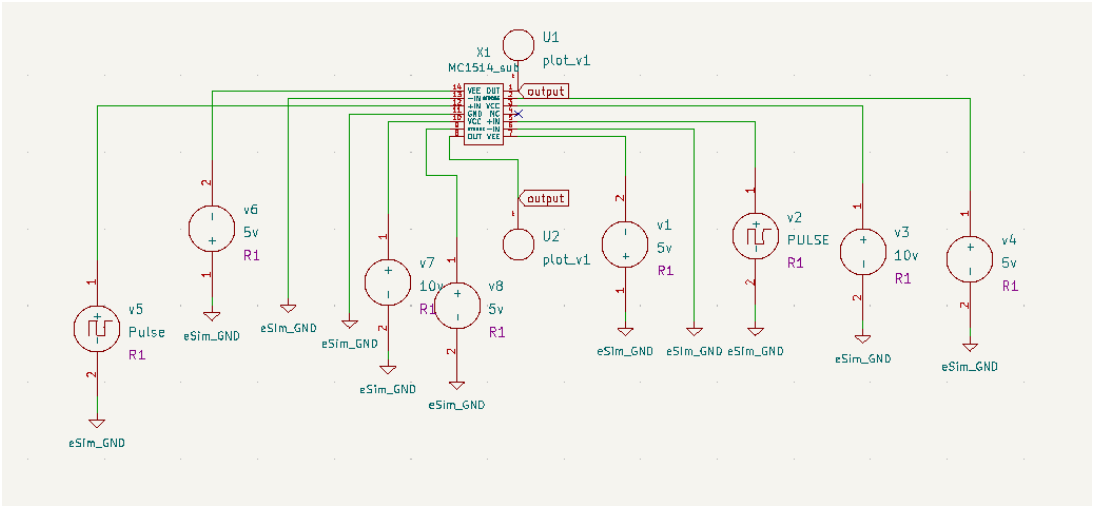

Figure 4.40: Test circuit used for functional validation of MC1514

4.10.4 Input and Output Plots

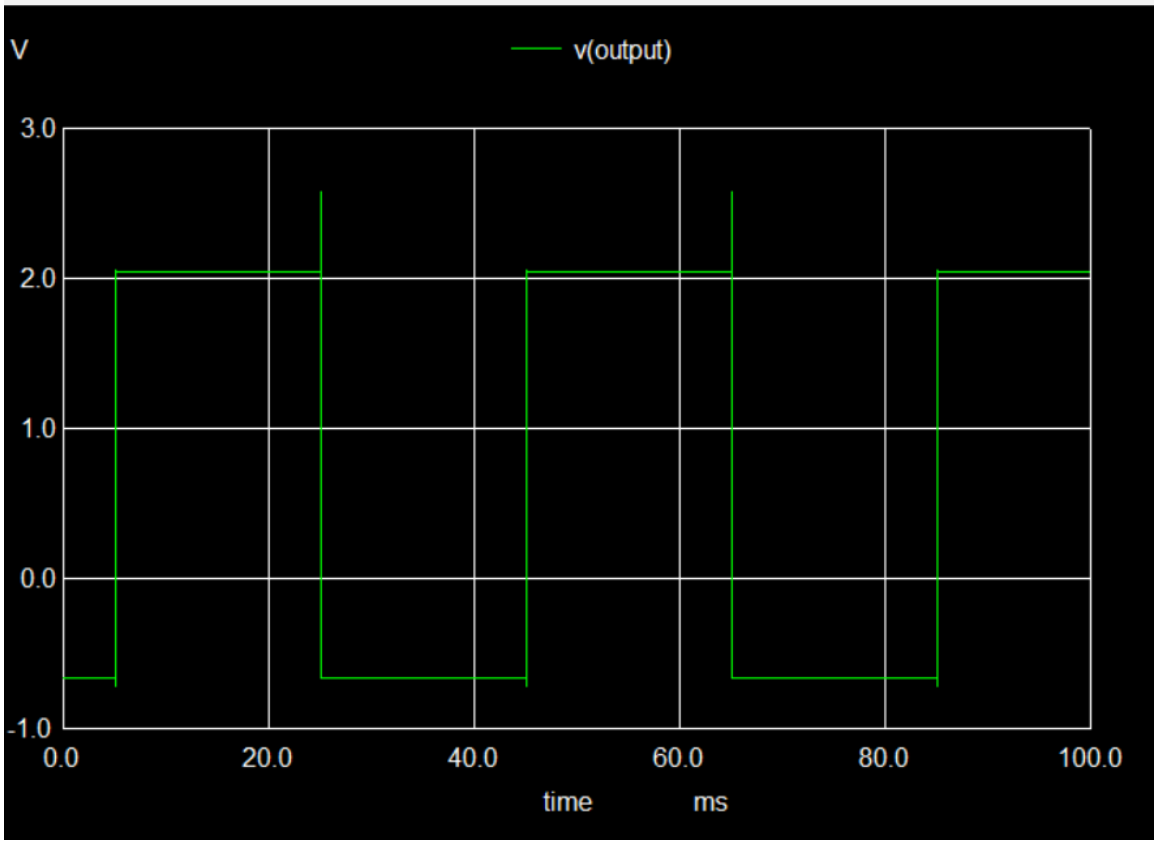

Figure 4.41: Simulated input/output waveforms for MC1514 test circuit

Chapter 5

Conclusion and Future Scope

Conclusion

The objectives of this internship were successfully accomplished through the design, implementation, and verification of multiple digital Integrated Circuit models in eSim. Each IC subcircuit was developed in accordance with its respective datasheet specifications and validated using suitable test circuits to ensure accurate functional behavior. The verified IC models can now be incorporated into the eSim subcircuit library and serve as reusable components for circuit simulation, experimentation, and academic applications. The work carried out contributes to the continuous development of open-source EDA tools and expands the availability of verified device models for the user community.

Future Scope

There is considerable scope to extend this work in future efforts. Additional digital and analog ICs can be modeled and verified to further enhance the eSim device library. Introducing support for complex mixed-signal components and standardized testbench frameworks would streamline the verification process and improve model reliability. The integration of HDL-based components and co-simulation capabilities offers potential for more advanced system-level design workflows. With continued development, the availability of validated IC models will support rapid prototyping, research, and educational activities, further strengthening eSim as a valuable open-source EDA platform.

Chapter 6

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