eSim Semester Long Internship Autumn Report 2025

On

Designing Integrated Circuit(IC) in eSim

Submitted by

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Acknowledgment

I would like to express my deepest gratitude to Prof. Prabhu Ramachandran for providing me the opportunity to be a part of the FOSSEE internship program and for supporting open-source engineering tool development at IIT Bombay. His guidance and vision have encouraged students and researchers to actively contribute to the open-source ecosystem.

I would also like to acknowledge Prof. Kannan M. Moudgalya for his foundational role in establishing and nurturing the FOSSEE initiative. His contributions toward open-source education and the creation of the FOSSEE fellowship framework have directly shaped the platform through which this internship was undertaken.

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I would also like to thank my internal mentors, **Mr. Varad Patil, Ms. Shanthi Priya K.**, and **Mr. Aditya M.**, for their valuable guidance, coordination, and technical inputs during the internship. Their mentorship contributed significantly to the clarity, progress, and successful execution of the work.

This internship has been an enriching learning experience, allowing me to work closely with open-source EDA tools, develop IC subcircuits in eSim, and gain exposure to real-world circuit modeling and simulation workflows. The knowledge acquired during this period will undoubtedly support my future academic and professional pursuits.

I would also like to thank the entire FOSSEE team for their coordination, assistance, and timely interactions at various stages of this work. Their collective efforts ensured smooth workflow, resource accessibility, and effective project execution.

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Chapter 1

Introduction

The FOSSEE (Free/Libre and Open Source Software for Education) project is a nationwide initiative dedicated to promoting the use of open-source software in order to improve the quality of education in India. The central aim of the project is to minimize dependence on proprietary software in academic institutions by encouraging the adoption of free and open-source alternatives. Through various programs and activities, FOSSEE facilitates the transition from commercial software to reliable, freely accessible open-source tools. Additionally, the project focuses on developing new FLOSS tools and enhancing existing ones to meet the continuously evolving requirements of education and research.

FOSSEE functions under the National Mission on Education through Information and Communication Technology (NMEICT), an initiative launched by the Ministry of Education (formerly the Ministry of Human Resource Development), Government of India. The project offers a comprehensive support framework that includes extensive documentation, interactive learning resources, hands-on training programs, and workshops. These efforts are aimed at enabling students, educators, and professionals to effectively incorporate open-source tools into their academic and research activities. By fostering a culture of collaboration, inclusivity, and innovation, FOSSEE has played a significant role in making technology more accessible and has created new avenues for learning and experimentation across a wide range of disciplines.

1.1 eSim

eSim, created by the FOSSEE project at IIT Bombay, is a versatile open-source software tool for circuit design and simulation. It combines various open-source software packages into one cohesive platform, making it easier to design, simulate, and analyze electronic circuits. This tool is particularly useful for students, educators, and professionals who need an affordable and accessible alternative to proprietary software. eSim offers features for schematic creation, circuit simulation, PCB design, and includes an extensive library of components. The Subcircuit feature is a significant enhancement, enabling users to design complex circuits by integrating simpler subcircuits. Through eSim, FOSSEE promotes the use of open-source so-

lutions in engineering education and professional fields, encouraging innovation and collaboration.

1.2 KiCad

KiCad is an open-source software suite for electronic design automation (EDA), used primarily for creating schematics and designing printed circuit boards (PCBs).Developed and maintained by a global community of contributors, KiCad offers a professional-grade alternative to proprietary PCB design tools, supporting multilayer board layouts and complex routing.

The tool includes an intuitive schematic editor for drawing circuit diagrams, a powerful PCB layout editor with design rule checking, and integrated 3D visualization tools for inspecting board designs. KiCad also provides extensive libraries of symbols and footprints, with the flexibility to create custom components as needed.

One of KiCads major strengths is its interoperability with simulation tools like NgSpice, enabling seamless integration of schematic design and circuit simulation.This makes KiCad an ideal choice for both students and professionals seeking a free, open-source solution for end-to-end PCB developmentfrom conceptual design to fabrication-ready outputs.

1.3 NgSpice

NgSpice is a widely used open-source SPICE simulator for electrical and electronic circuit analysis. It supports a broad range of circuit elements, including passive components (resistors, capacitors, and inductors), active devices such as diodes, JFETs, BJTs, and MOSFETs, as well as transmission lines and various other componentsall defined through a netlist.

NgSpice is capable of simulating both analog and digital circuits, including event driven digital simulations and mixed-signal systems. It efficiently handles everything from simple logic gates to highly complex circuits. The simulator comes with an extensive library of device models for analog, digital, active, and passive elements.These models are sourced from NgSpices internal collections, semiconductor manufacturers, or foundries.

Users describe circuits using netlists, and the simulator provides output in the form of graphical waveforms or tabulated data, including voltage, current, and other electrical parameters. This makes NgSpice a powerful tool for both academic learning and advanced circuit analysis.

1.4 Makerchip

Makerchip is a user-friendly platform that provides convenient access to a suite of tools for digital circuit design, catering to both beginners and experienced users.

It offers both browser-based and desktop environments for coding, compiling, simulating, and debugging Verilog, SystemVerilog, and Transaction-Level Verilog (TL Verilog) designs. By integrating open-source and proprietary tools, Makerchip ensures a robust and feature-rich design experience.

A key integration exists between eSim and Makerchip through a Python-based utility known as the Makerchip-App, which launches the Makerchip IDE directly from within eSim. This interface facilitates a seamless workflow for users wishing to simulate digital designs as part of their overall circuit development process.

Makerchip emphasizes accessibility and ease of use through its clean interface, intuitive workflows, and comprehensive simulation features, aiming to make digital design both engaging and efficient for users across varying proficiency levels.

However, a notable limitation in the current open-source ecosystem is the lack of a unified platform that supports schematic capture, circuit simulation, and PCB layout within a single tool. While tools such as KiCad focus primarily on PCB designand others like gEDA support circuit simulation, none offer complete end-to-end functionality. In contrast, eSim addresses this gap by combining schematic creation,simulation, and layout design within a single cohesive environmentmaking it a comprehensive open-source alternative to proprietary EDA software.

Chapter 2

Features of eSim

eSim offers a comprehensive set of features that make it a powerful open-source alternative for electronic design automation. Some of the key features include:

1.**Open-source and Free**: eSim is fully open-source, allowing unrestricted access without licensing costs, making it ideal for academic and research purposes.

2.**Integrated Toolchain**: Combines multiple open-source tools such as KiCad for schematic capture and PCB design, NgSpice for analog simulation, GHDL for digital simulation, and Makerchip for advanced digital design.

3.**Mixed-Signal Simulation**: Supports both analog and digital simulation, allowing users to design and simulate mixed-signal circuits efficiently.

4.**Subcircuit Feature**: Enables hierarchical and modular design by allowing complex circuits to be broken into reusable subcircuits.

5.**Device Modeling**: Supports custom device modeling, allowing users to simulate real-world semiconductor devices using user-defined parameters.

6.**SkyWater SKY130 PDK Support**: Provides access to open-source 130nm process design kit for IC design and simulation.

7.**Python Integration**: Allows automation, scripting, and advanced analysis using Python interfaces.

8.**User-Friendly Interface**: Offers an intuitive GUI that simplifies circuit creation, simulation setup, and result analysis, making it suitable for both beginners and advanced users.

9.**Cross-Platform Support**: Compatible with major operating systems like Linux and Windows.

10.**Active Community and Documentation**: Extensive documentation, tutorials, and community support provided through FOSSEE ensure smoothlearning and troubleshooting.

Chapter 3

Problem Statement

3.1 Problem Statement

To design and develop various Analog and Digital Integrated Circuit (IC) models in the form of subcircuits using device model files already available in the eSim library .These IC models, once successfully integrated into the eSim Subcircuit Library, will serve as reusable components for circuit design purposes by developers and end users.

3.2 Approach

Our implementation began with a detailed study of datasheets from reputed IC manufacturers such as Texas Instruments, Analog Devices, and NXP Semiconductors. We identified a diverse set of ICs that provide functionalities such as precision amplification, voltage comparison, encoding, and audio amplification. Each subcircuit was constructed based on verified datasheet information and subsequently tested using NgSpice simulations to validate basic configurations.The step-by-step roadmap followed is outlined below:

3.2.1 Analyzing datasheets:

The first step involved reviewing datasheets of various analog and digital ICs to identify models not currently present in the eSim library. Once a candidate IC was shortlisted, we analyzed its detailed schematic, electrical characteristics, and truth table. Upon verifying these design elements, the IC was finalized for implementation.

3.2.2 Subcircuit Creation:

The selected IC was modeled as a subcircuit in eSim using only the existing device model files in the eSim library. The design process strictly adhered to official datasheet specifications. This phase also included creating the symbol and pin diagram of the IC based on its package type and pin configuration.

3.2.3 Test Circuit Design:

After the subcircuit was modeled, we designed test circuits as recommended in the respective datasheets. These test cases werespecifically constructed to validate the functional behavior of the IC under various input conditions.

3.2.4 Schematic Testing:

The designed test circuits were then simulated using eSims KiCad-to-NgSpice conversion and simulation interface. Output waveforms and plots were analyzed to verify expected performance. If the outputs did not align with datasheet specifications, the process reverted to the design phase to identify and rectify potential errors. The subcircuit and its associated test circuit were then revalidated.

Chapter 4

IC integration and subcircuit Creation

4.1 SN74AS20

The SN74AS20 is a high-speed Advanced Schottky TTL IC that contains two independent 4-input NAND gates.It operates on a 5 V supply and provides fast switching with low propagation delay, making it suitable for complex digital logic and control circuits. Each output goes LOW only when all four inputs are HIGH otherwise, the output remains HIGH.

FUNCTION TABLE (each gate)

INPUTS				OUTPUT
A	B	C	D	Y
H	H	H	H	L
L	X	X	X	H
X	L	X	X	H
X	X	L	X	H
X	X	X	L	H

Figure 4.1: Truth Table of NAND GATE

4.1.1 Subcircuit Layout

The SN74AS20 subcircuit, expressed using only NAND gates, implements each 4-input NAND function by internally combining multiple 2-input NAND GATE. The four inputs are first paired and processed through two 2-input NAND gates. Their outputs are then fed into a final NAND GATE to generate the output. This NAND-

only structure preserves the NAND logic behavior, where the output goes LOW only when all four inputs are HIGH, making it suitable for implementation using standard NAND-based digital logic design.

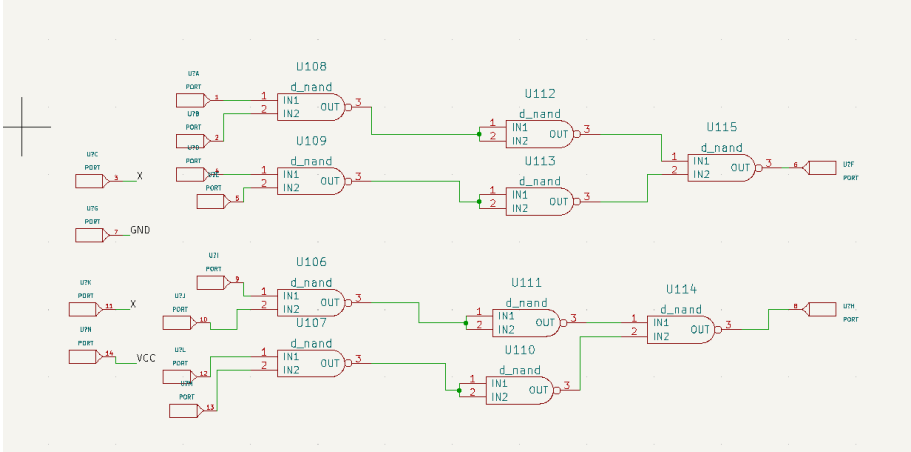

Figure 4.2: Internal Schematic of SN74AS20

4.1.2 IC Layout

The figure shows the physical representation of the SN74AS20 iC indicating the arrangement of its pins. It includes input pins, an output pin,a power supply pin, and ground pin.The pin diagram is essential for correctly integrating the IC into a circuit, ensuring proper connections and functionality in digital applications.

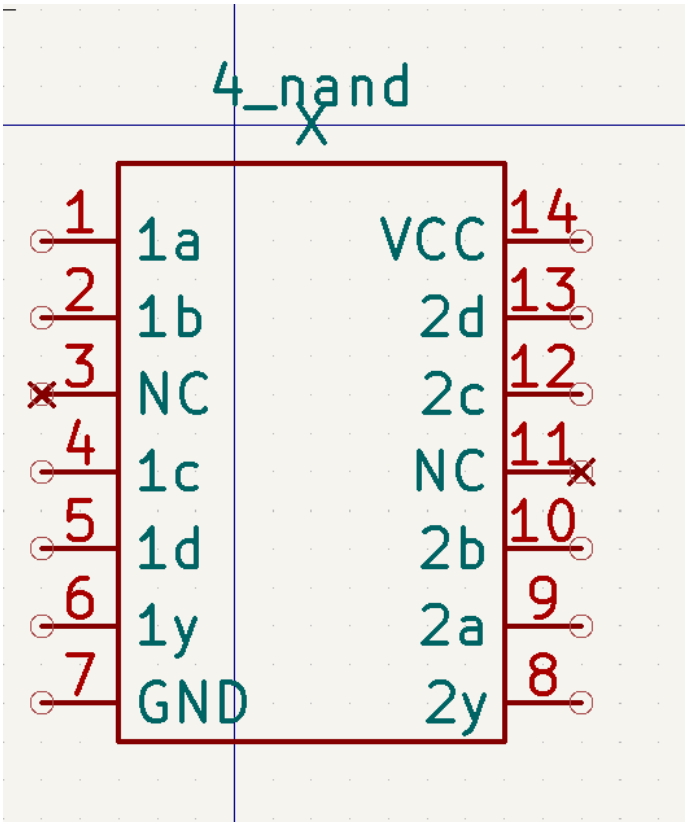

Figure 4.3: IC Pin Diagram of SN74AS20

4.1.3 Test Circuit

The figure illustrates a test setup used to verify the performance of the SN74AS20 IC in eSim. The test circuit includes a 5 V DC power source, four pulse signal sources applied to the input pins, and an output monitered using the plot function. The pulse sources generate different input combinations over time, while the plot component is used to observe the output waveform. This setup helps evaluate the logic functionality, response time, and switching behavior of the 4-input NAND gate, confirming that the output goes LOW only when all four inputs are simultaneously HIGH.

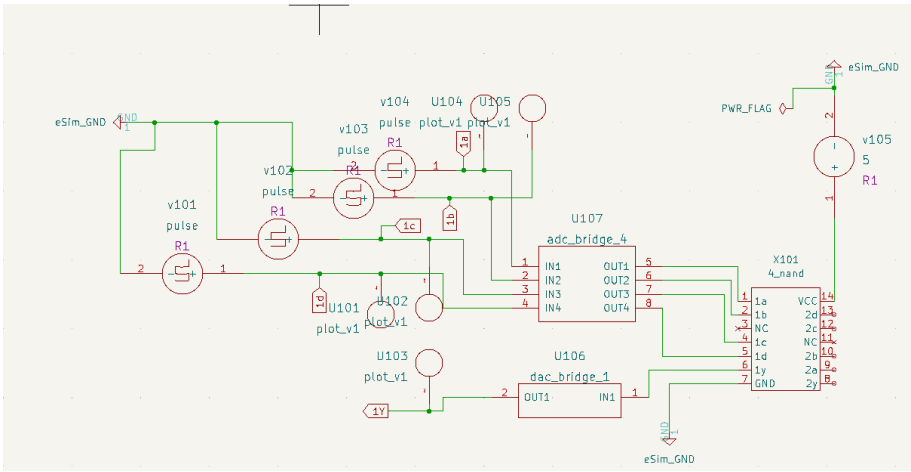

Figure 4.4: Test Circuit of SN74AS20

4.1.4 Output Waveforms

The output waveform obtained from the plot function shows the correct 4-input NAND behavior of the SN74AS20. For most time intervals, when one or more input pulse signals are LOW, the output remains HIGH. When all four input pulses overlap at the HIGH level, the output waveform transitions to LOW. The waveform also shows sharp rising and falling edges, indicating fast switching and low propagation delay of the Advanced Schottky TTL logic. This confirms proper logic operation and reliable timing performance of the IC.

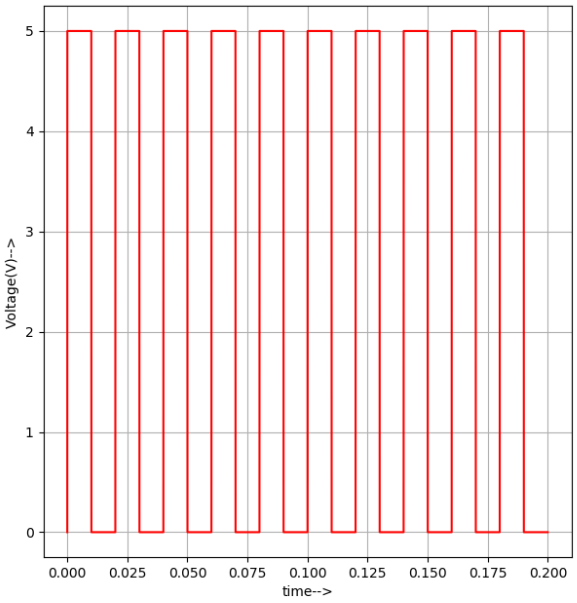

Figure 4.5: Input Waveform 1A

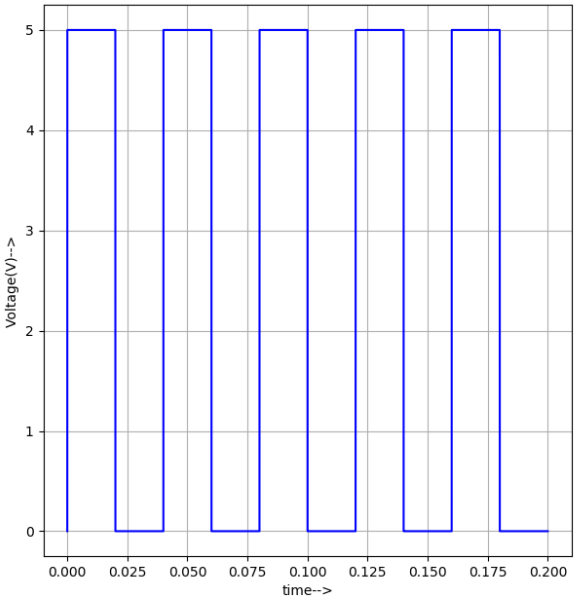

Figure 4.6: Input Waveform 1B

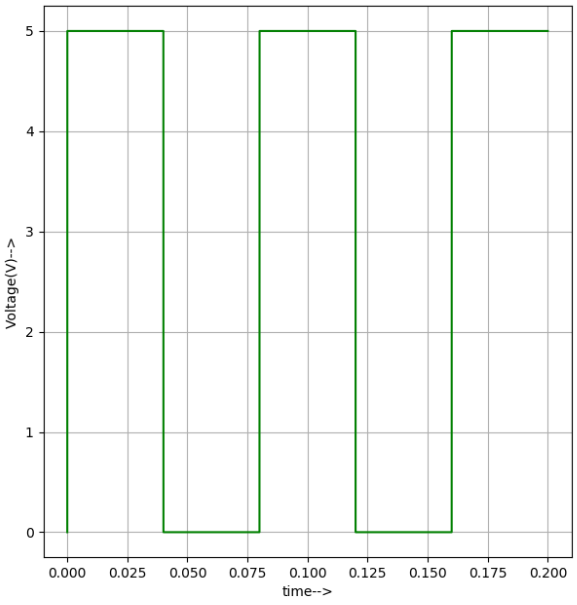

Figure 4.7: Input Waveform 1C

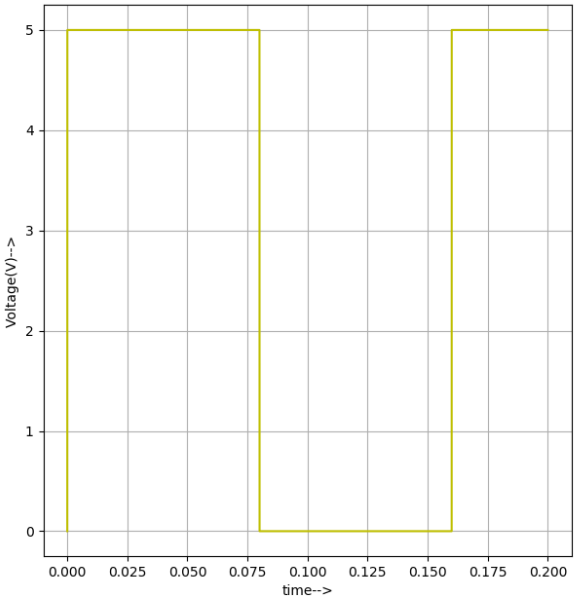

Figure 4.8: Input Waveform 1D

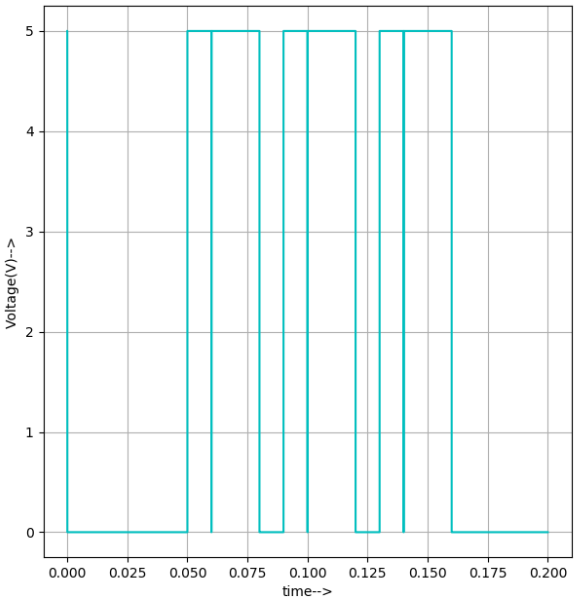

Figure 4.9: Output Waveform

4.2 SN74LS27

The SN74LS27 is a TTL logic IC that contains three independent 3-input NOR gates in a single package. It operates from a 5 V supply and belongs to the Low-power Schottky (LS) family, offering a good balance between speed and power consumption. Each gate produces a HIGH output only when all three inputs are LOW. If any input is HIGH, the output becomes LOW. The IC is widely used in digital control, decoding, and logic processing circuits where multi-input NOR operations are required.

FUNCTION TABLE (each gate)

INPUTS			OUTPUT
A	B	C	Y
H	X	X	L
X	H	X	L
X	X	H	L
L	L	L	H

Figure 4.10: Truth Table of NOR

4.2.1 Subcircuit Layout

The sub-circuit layout of the SN74LS27 represents the internal schematic of each 3-input NOR gate, which is implemented using TTL technology. Each gate consists of a BJT-based input stage formed by multiple input transistors, where the three inputs are combined to control the conduction path. Resistors are used for biasing and current limiting, while Schottky diodes are included to prevent transistor saturation and improve switching speed. The intermediate stage drives a totem-pole BJT output configuration, ensuring fast and reliable logic-level transitions. This BJTdioderesistor network realizes the NOR function, producing a HIGH output only when all three inputs are LOW.

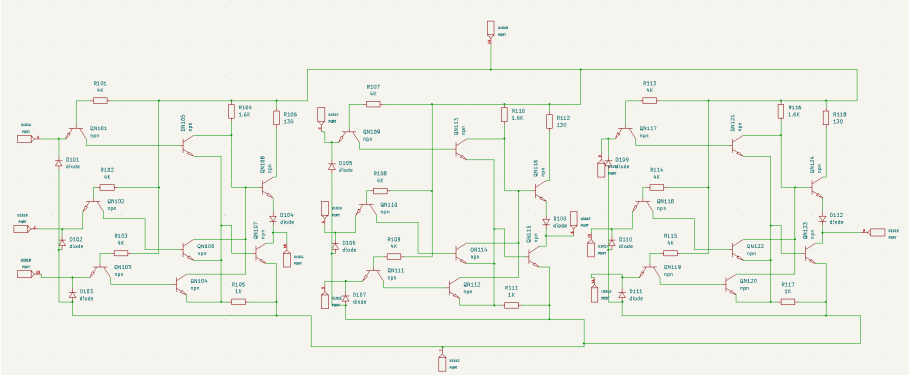

Figure 4.11: Internal Schematic of SN74LS27

4.2.2 IC Layout

The IC pin diagram of the SN74LS27 shows a 14-pin dual in-line package (DIP) containing three independent 3-input NOR gates. Each gate has three input pins and one output pin, clearly grouped in the pin layout for easy identification. Pin 14 is connected to VCC (+5 V) and Pin 7 is connected to GND. The remaining pins are assigned to the inputs and outputs of the three NOR gates, allowing each gate to operate independently within the same IC. This pin arrangement simplifies circuit design and integration in digital logic applications.

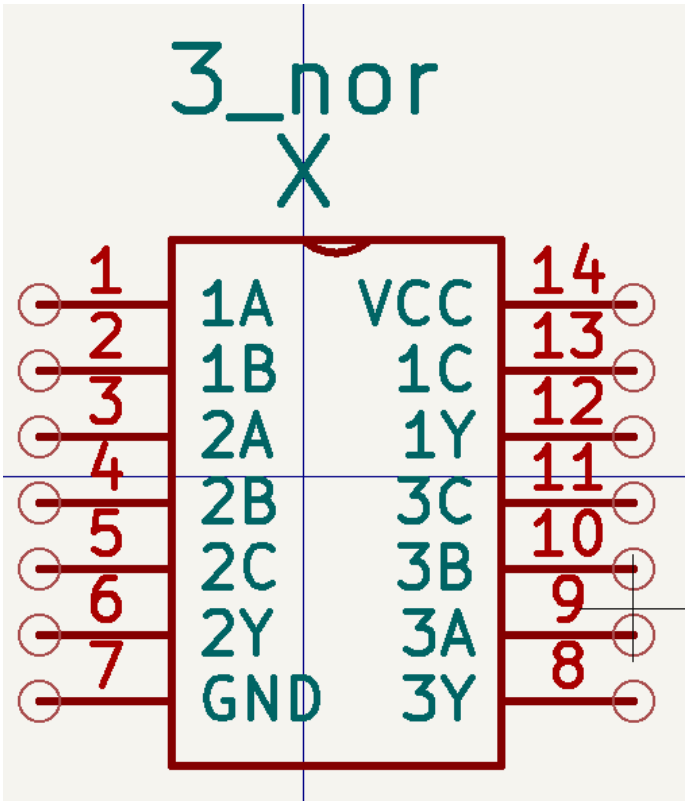

Figure 4.12: Pin Diagram of SN74LS27

4.2.3 Test Circuit

The test circuit for the SN74LS27 is designed to verify the operation of its three independent 3-input NOR gates. The IC is powered using a 5 V DC supply connected to VCC and GND. For each gate, the three input pins are driven by pulse sources, allowing different input combinations to be applied over time. The output of each NOR gate is connected to a plot component. During testing, the output remains HIGH only when all three inputs are LOW, and transitions to LOW when any input becomes HIGH, confirming correct NOR gate functionality and timing behavior.

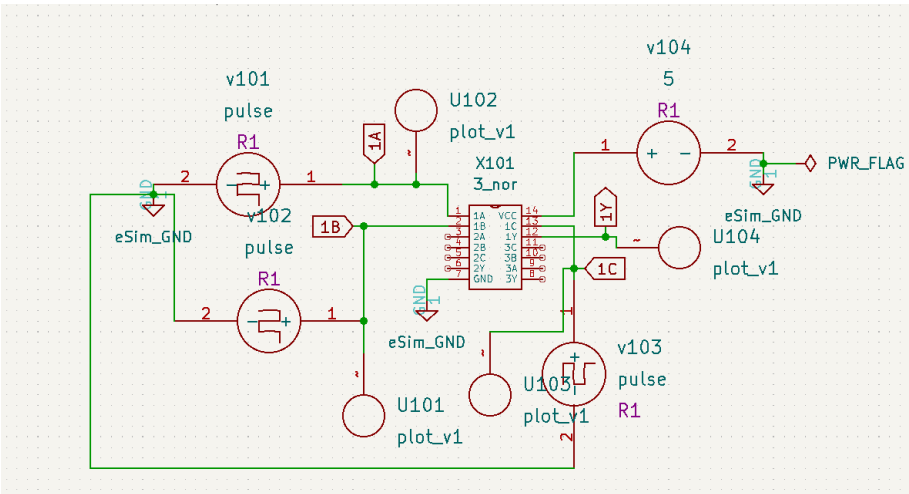

Figure 4.13: Test Circuit of SN74LS27

4.2.4 Output Waveform

The output waveform observed for the SN74LS27 shows the correct 3-input NOR logic behavior. When all three input signals are LOW, the output waveform stays HIGH. As soon as any one of the input pulses goes HIGH, the output transitions to LOW. The plot also shows clean and fast transitions between logic levels, indicating proper switching action of the TTL circuitry. This confirms that the IC responds correctly to changing input conditions and performs the intended NOR operation reliably.

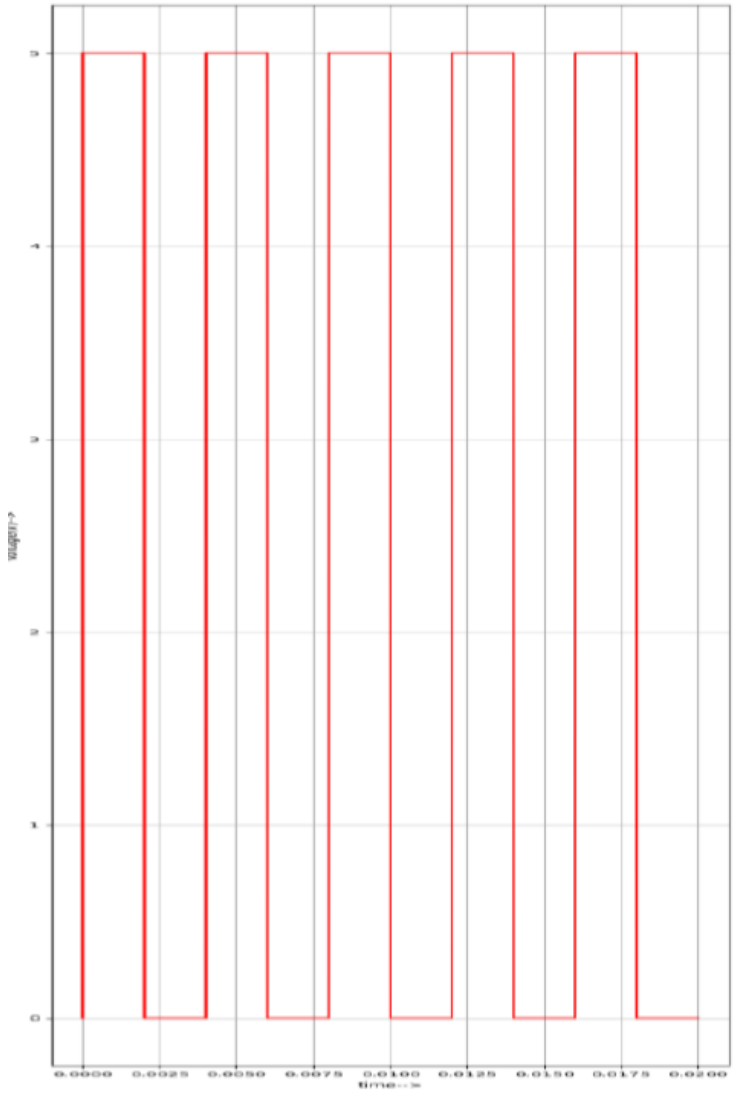

Figure 4.14: Input Waveform 1A

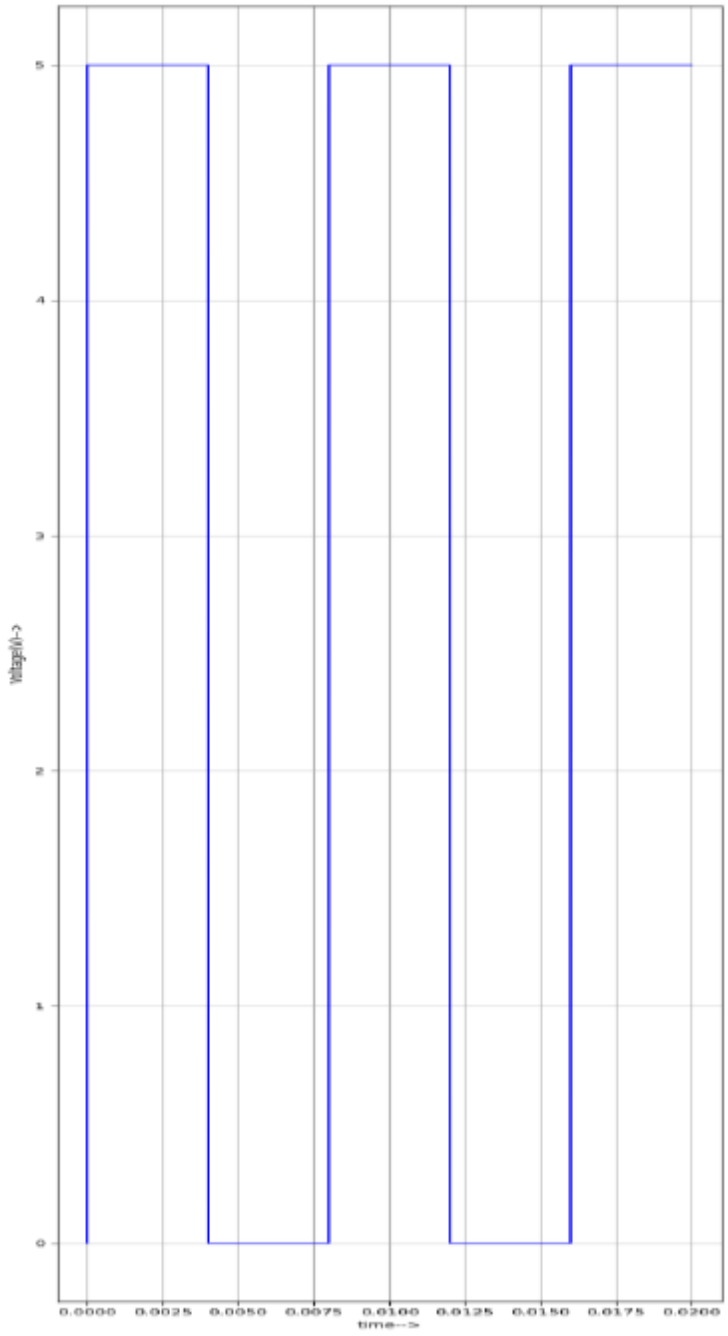

Figure 4.15: Input Waveform 1B

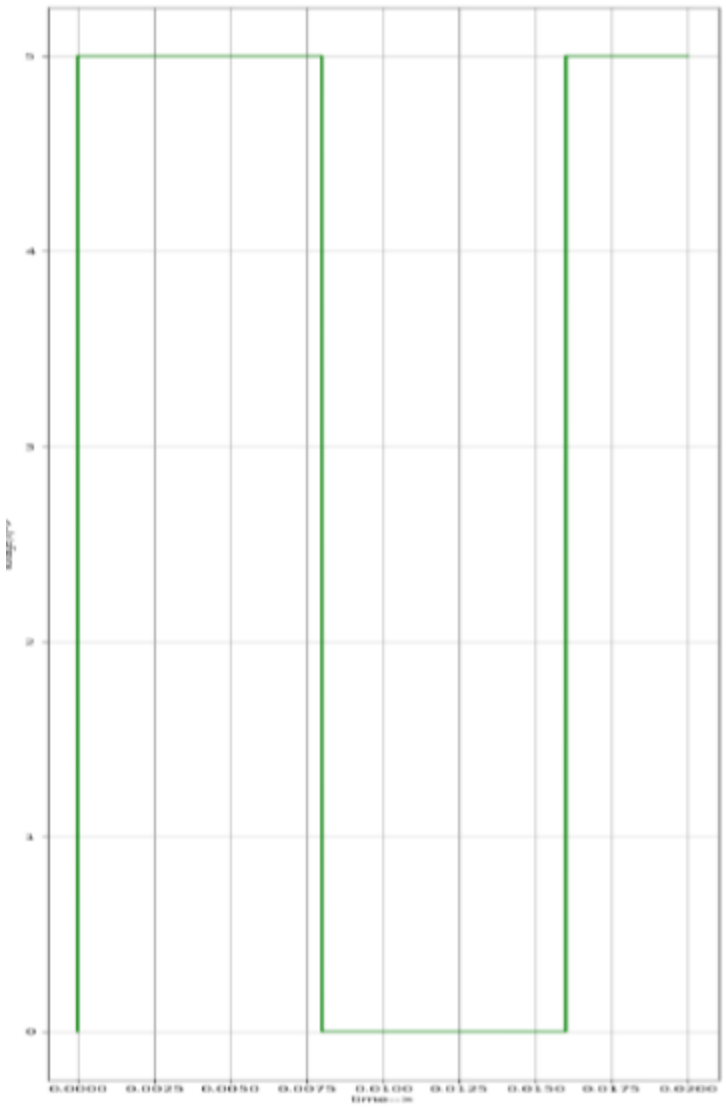

Figure 4.16: Input Waveform 1C

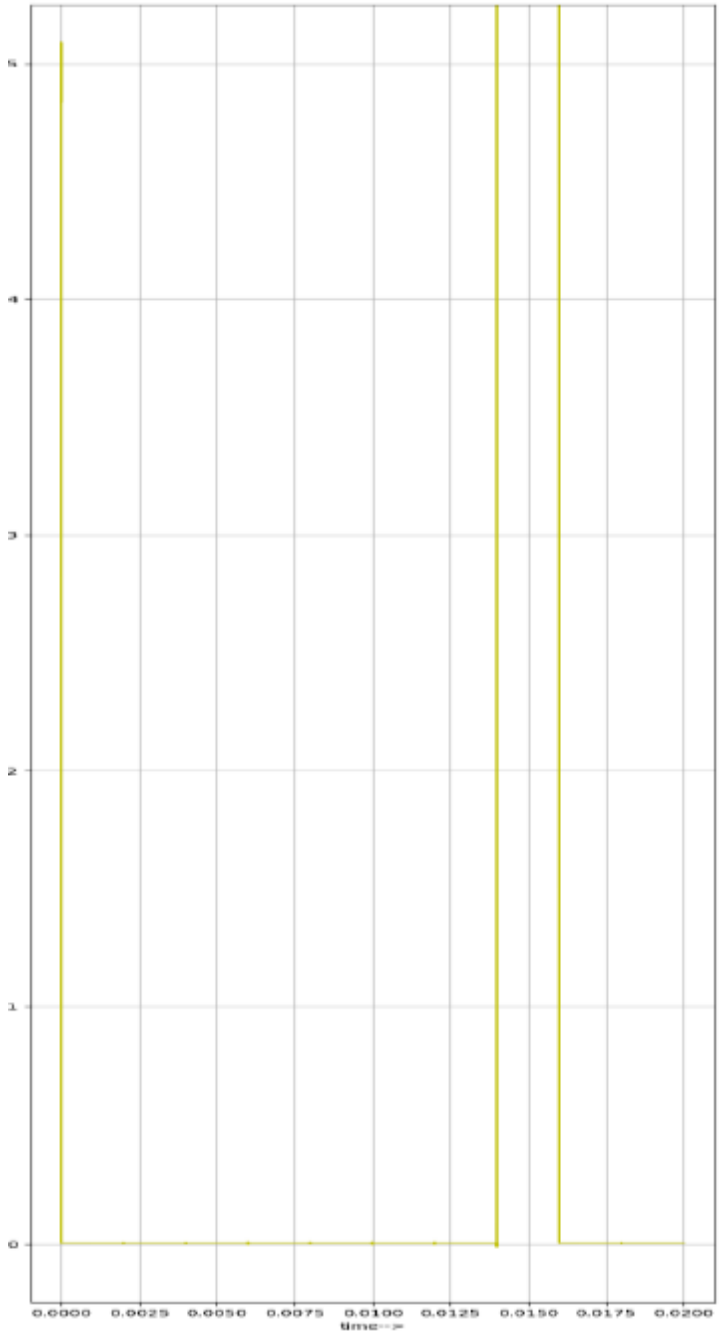

Figure 4.17: Output Waveform

4.3 SN74157

The SN74157 is a TTL logic IC that functions as a quad 2-to-1 multiplexer. It contains four independent 2-input multiplexers that select one of two data inputs for each channel based on a common select line. The IC has active-low outputs, meaning the selected input is passed to the output through an inverting logic stage. It operates from a 5 V supply and belongs to the standard 74 TTL family, offering fast switching and reliable performance. The SN74157 is widely used in data routing,

signal selection, and digital control applications where multiple data lines need to be selectively passed to outputs.

FUNCTION TABLE

INPUTS				OUTPUT Y	
STROBE $\overline{G}$	SELECT $\overline{A}$/B	A	B	'157, 'LS157, 'S157	'LS158 'S158
H	X	X	X	L	H
L	L	L	X	L	H
L	L	H	X	H	L
L	H	X	L	L	H
L	H	X	H	H	L

H = high level, L = low level, X = irrelevant

Figure 4.18: Function Table for SN74157

4.3.1 Subcircuit Layout

The sub-circuit of the SN74157 (2:1 multiplexer) is implemented using basic logic gates and inverters. For each channel, the select (A/B) input is first passed through an inverter to generate A. One data input is ANDed with A, while the other data input is ANDed with B. The outputs of these two AND gates are then combined using an OR gate to produce the selected output. Since the SN74157 has inverting (active-LOW) outputs, the final stage includes an inverter, ensuring that the output reflects the inverted selected input. This gate-level structure realizes the 2:1 multiplexing function for each of the four independent channels.

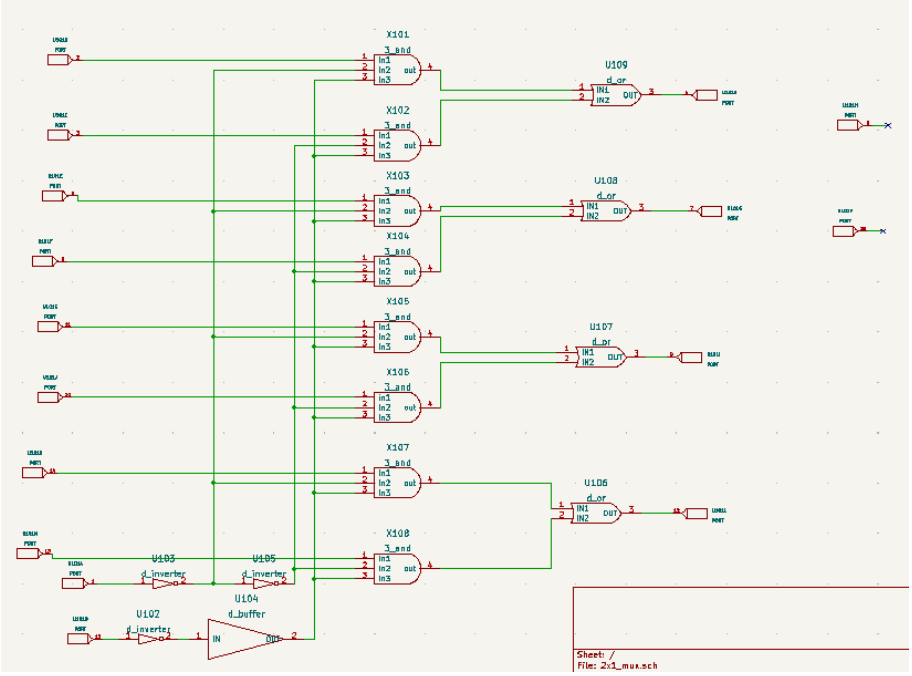

Figure 4.19: Internal Schematic of SN74157

4.3.2 IC Layout

In the SN74157, the A/B (select) pin is used to choose between the two data inputs, while G acts as the strobe (enable) control. Each of the four channels has two data inputs, A and B, and one output. When A/B = LOW, the A inputs are selected; when A/B = HIGH, the B inputs are selected. The G pin is active-LOW, so when G = LOW, the multiplexer is enabled and the selected input appears at the output (in inverted form). When G = HIGH, the outputs are disabled and forced HIGH, regardless of the select or input states.

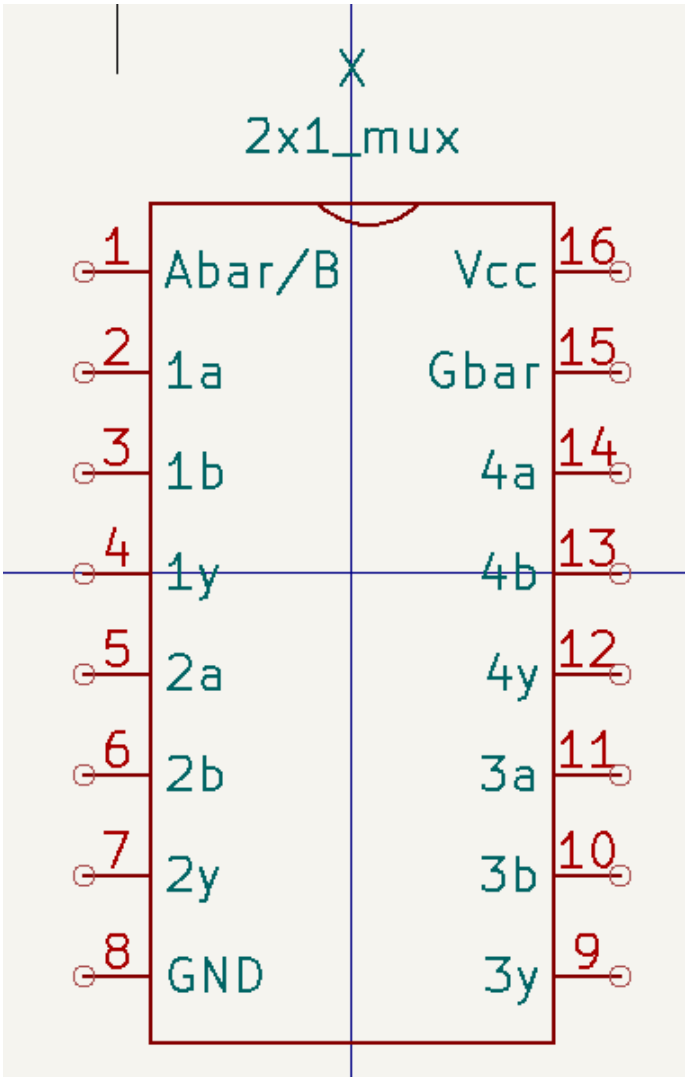

Figure 4.20: Pin Diagram

4.3.3 Test Circuit

The test circuit for the SN74157 (2:1 multiplexer) is designed to verify its data-selection and strobe operation. The IC is powered using a 5 V DC supply connected to VCC and GND. The A and B data input pins of each channel are driven using pulse or logic signal sources to represent two different input data streams. The A/B select pin is controlled by a separate logic source to switch between the A and B inputs, while the G (strobe) pin is driven by another control signal to enable or disable the outputs. The four output pins are connected to plot components or logic probes to observe the selected output signals. This setup allows verification that, when G is LOW, the output follows the selected input (based on A/B), and when G is HIGH, all outputs remain HIGH, confirming correct multiplexer operation.

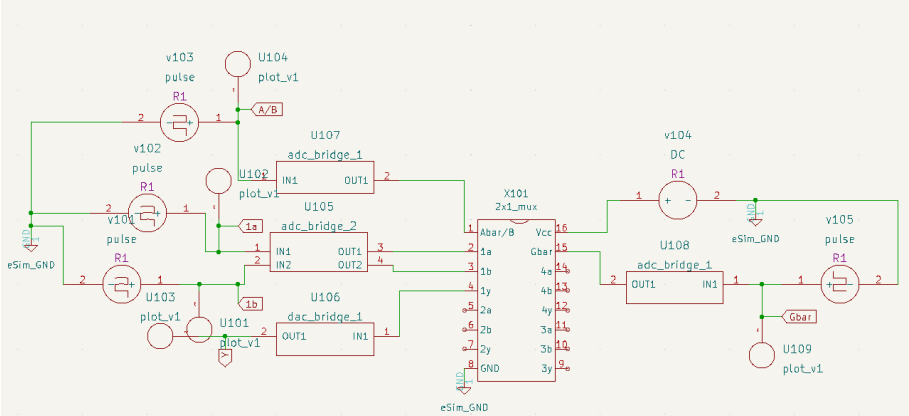

Figure 4.21: Test Circuit

4.3.4 Output Waveform

The waveforms show the operation of the SN74157 2:1 multiplexer by displaying the A input, B input, A/B select signal, G enable (strobe) signal, and the output Y. When G is LOW (enabled), the output waveform Y follows the selected inputit follows A when A/B is LOW and B when A/B is HIGH, with inversion due to the active-LOW output. When G is HIGH (disabled), the output Y remains HIGH, independent of the A, B, or select inputs. The waveforms clearly demonstrate correct data selection, enable control, and timing relationships between inputs and output.

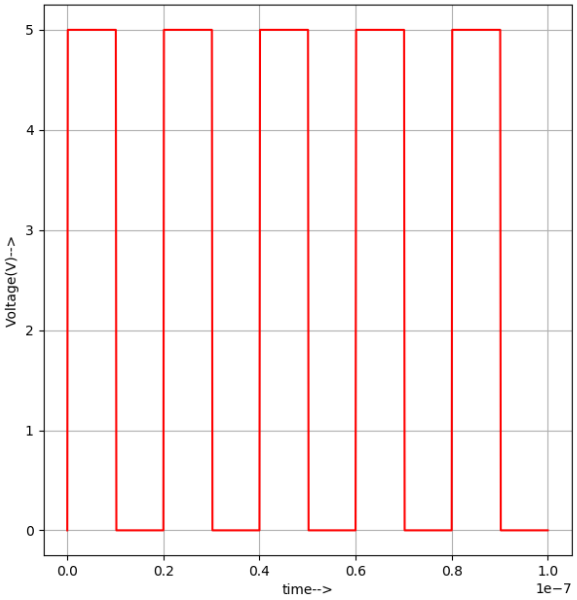

Figure 4.22: Input Waveform A

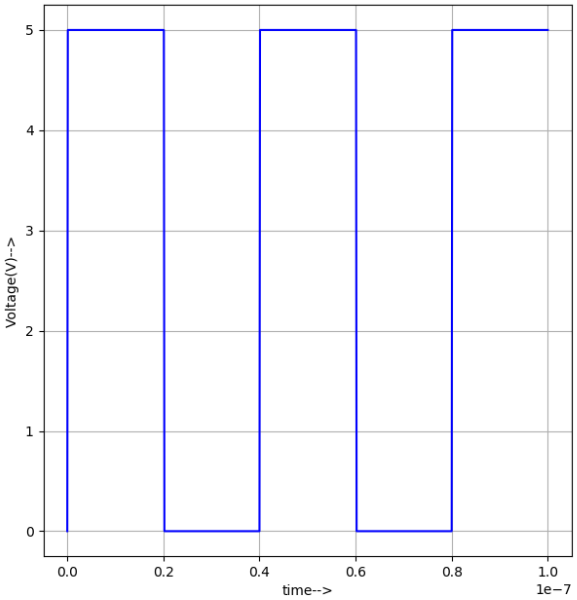

Figure 4.23: Input Waveform B

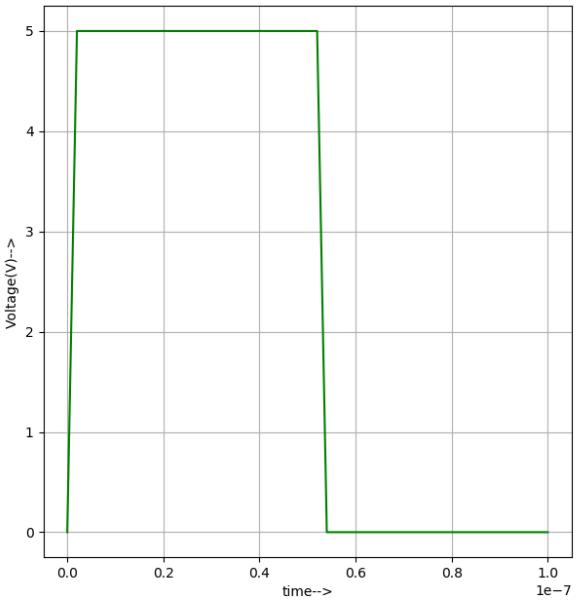

Figure 4.24: Selection Pin A/B

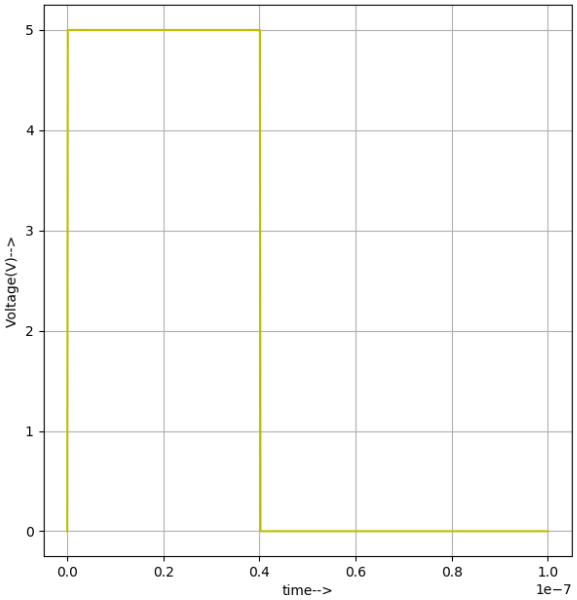

Figure 4.25: Enable/Disable ,G

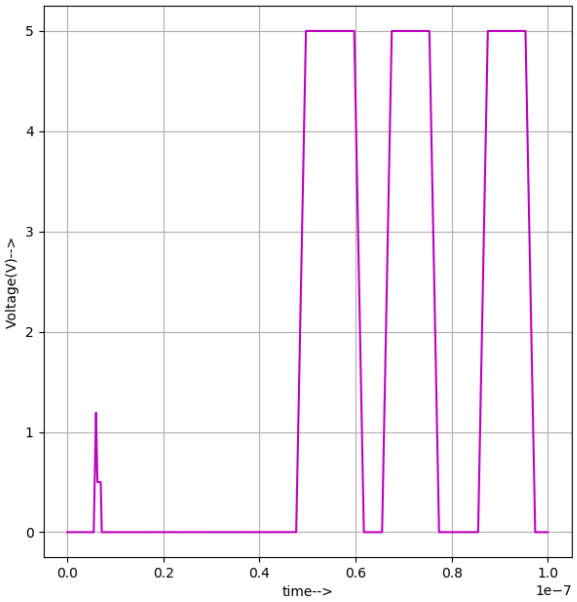

Figure 4.26: Output Waveform

4.4 SN74HC04

The SN74HC04 is a high-speed CMOS hex inverter IC that contains six independent NOT gates in a single package. Each inverter performs the Boolean function Y = in positive logic, producing an output that is the logical complement of its input. The device operates over a wide supply voltage range and offers low power consumption, high noise immunity, and fast switching speed, making it suitable for signal inversion, waveform shaping, and digital logic applications.

INPUT	OUTPUT
A	Y
L	H
H	L

Figure 4.27: Functional Table of SN74HC04

4.4.1 Subcircuit Layout

The subcircuit of the SN74HC04 is composed of six identical inverter stages, each implemented using CMOS bufferinverter structures. Every stage consists of a complementary pair of MOSFETs (PMOS and NMOS) arranged as a buffered inverter, where the input simultaneously drives both transistors. When the input is LOW, the PMOS conducts and the NMOS is off, pulling the output HIGH; when the input is HIGH, the NMOS conducts and the PMOS is off, pulling the output LOW. This buffered inverter design provides strong output drive, fast transitions, and improved noise immunity, ensuring reliable inversion for each of the six independent channel.

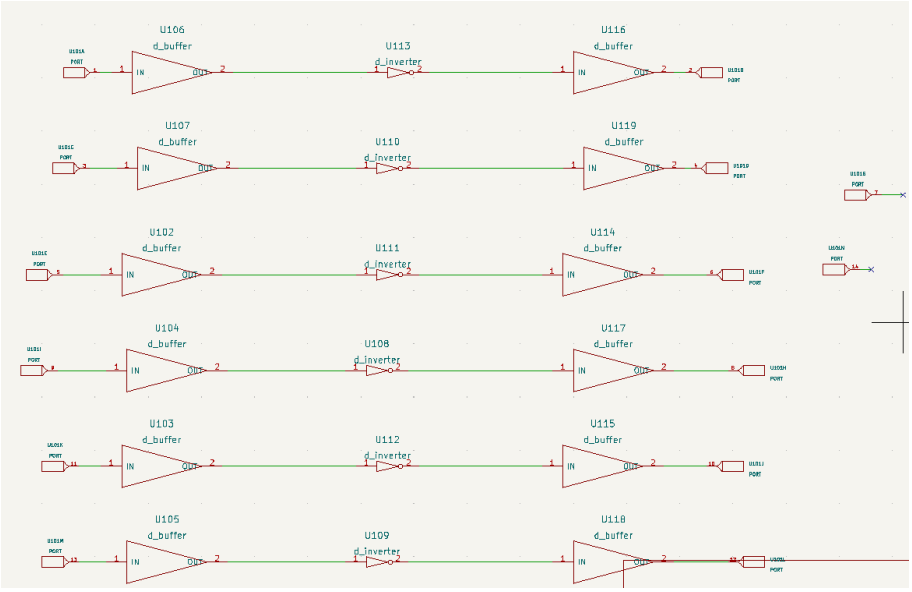

Figure 4.28: Internal Schematic of SN74HC04

4.4.2 IC Layout

The pin diagram of the SN74HC04 corresponds to a 14-pin dual in-line package (DIP) containing six independent inverter gates. Each inverter has one input pin and one output pin, arranged in pairs across the package for easy identification. Pin 14 is connected to the positive supply voltage (VCC) and Pin 7 is connected to ground (GND). The remaining pins are assigned to the inputs and outputs of the six inverters, allowing each gate to operate independently. This pin configuration makes the SN74HC04 convenient for use in a wide range of digital logic and signal-conditioning circuits.

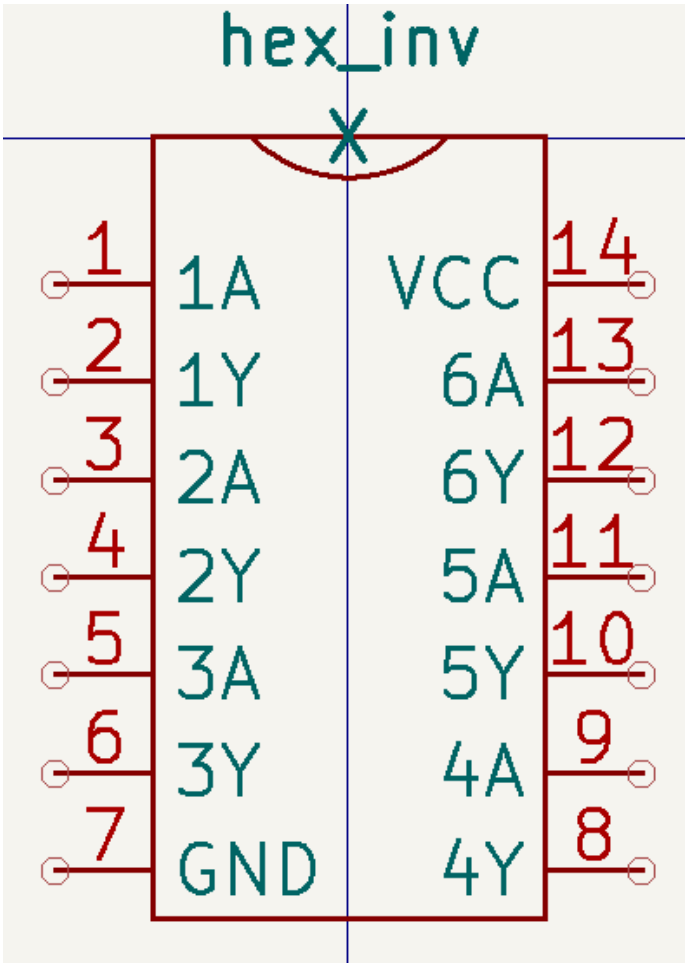

Figure 4.29: Pin Diagram

4.4.3 Test Circuit

The test circuit for the SN74HC04 is designed to verify the operation of its six independent inverter gates. The IC is powered with a 5 V DC supply connected to VCC (pin 14) and GND (pin 7). Each inverter input is driven by a pulse signal source to provide alternating HIGH and LOW logic levels. The corresponding outputs are connected to plot components, LEDs with current-limiting resistors, or logic probes to observe the inverted signals. During testing, the output of each gate should be

HIGH when the input is LOW and LOW when the input is HIGH, confirming proper inversion, fast switching, and correct functioning of all six inverters.

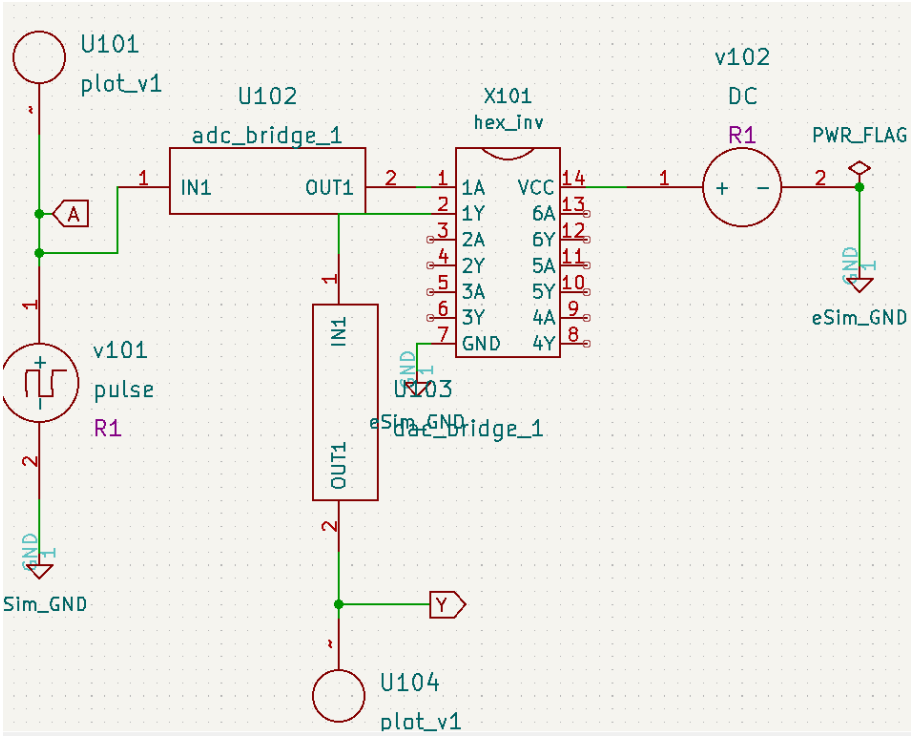

Figure 4.30: Test Circuit

4.4.4 Output Waveform

The output waveform of the SN74HC04 hex inverter shows the inverted response of each gate to its input pulses. When an input signal goes HIGH, the corresponding output goes LOW, and when the input goes LOW, the output goes HIGH, producing a clear complementary waveform. The waveforms exhibit sharp rising and falling edges, reflecting the fast switching speed of the CMOS inverters. This confirms that all six inverters in the IC are functioning correctly and reliably inverting the applied logic signals.

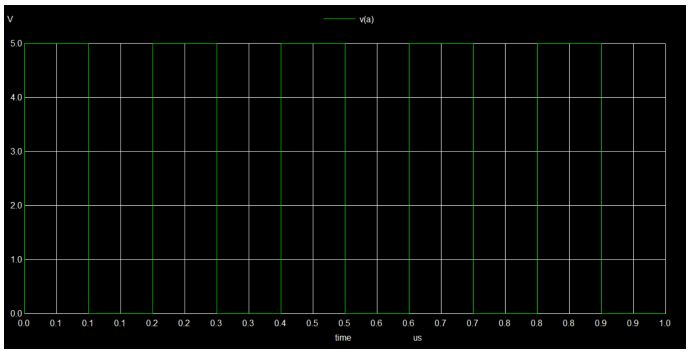

Figure 4.31: Input Waveform

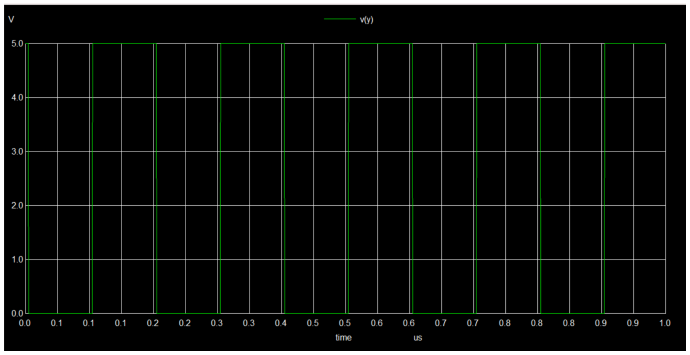

Figure 4.32: Output Waveform

4.5 LF356

The LF356 is a monolithic JFET-input operational amplifier that uses BI-FET technology, combining well-matched high-voltage JFETs with standard bipolar transistors on a single chip. It features very low input bias and offset currents, low offset voltage, and minimal offset voltage drift, with an adjustable offset that does not affect drift or common-mode rejection. The LF356 is designed for high-speed and precision applications, offering a high slew rate, wide bandwidth, extremely fast settling time, low voltage and current noise, and a low 1/f noise corner, making it suitable for precision analog signal processing, active filters, and instrumentation applications.

4.5.1 Subcircuit Layout

The subcircuit of the LF356 consists of a JFET-input differential stage followed by bipolar transistor (BJT) gain and output stages. The JFET input transistors provide high input impedance, low bias current, and low noise, while the BJT stages amplify the signal, ensure high gain, and drive the output with low impedance. Internal resistors, current sources, and compensation capacitors stabilize the circuit, support offset adjustment, and improve frequency response. This combination of JFETs at the input and BJTs in the amplification/output stages enables the LF356 to achieve high-speed, low-noise, and precise analog performance.

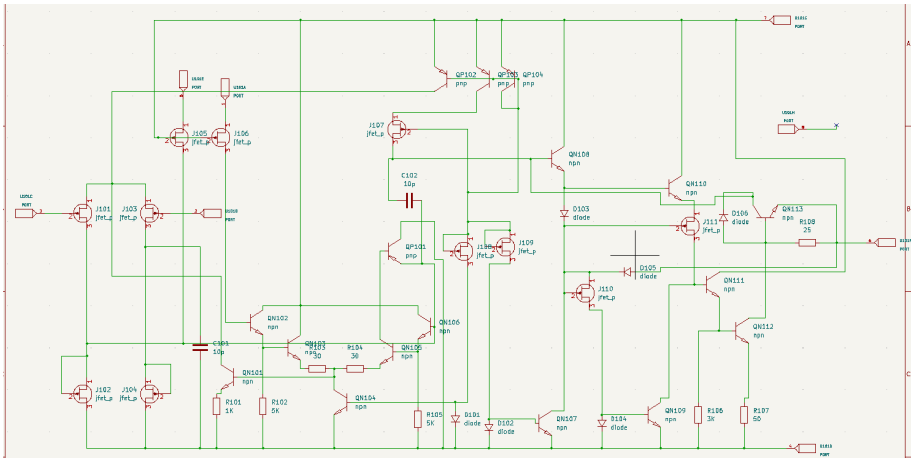

Figure 4.33: Internal Schematic of LF356

4.5.2 IC Layout

The LF356 comes in an 8-pin DIP package with pins arranged for high-performance analog operation. It has two offset balance pins (Pins 1 and 5) for adjusting the input offset voltage, a non-inverting input (Pin 3) and an inverting input (Pin 2) for signal application, and an output pin (Pin 6) for the amplified signal. The power supply pins include V+ (Pin 7) and V (Pin 4), while Pin 8 is NC (no connection). This pin configuration allows precise signal amplification with offset adjustment and dual supply operation, making the LF356 suitable for low-noise, high-speed, and precision analog circuits.

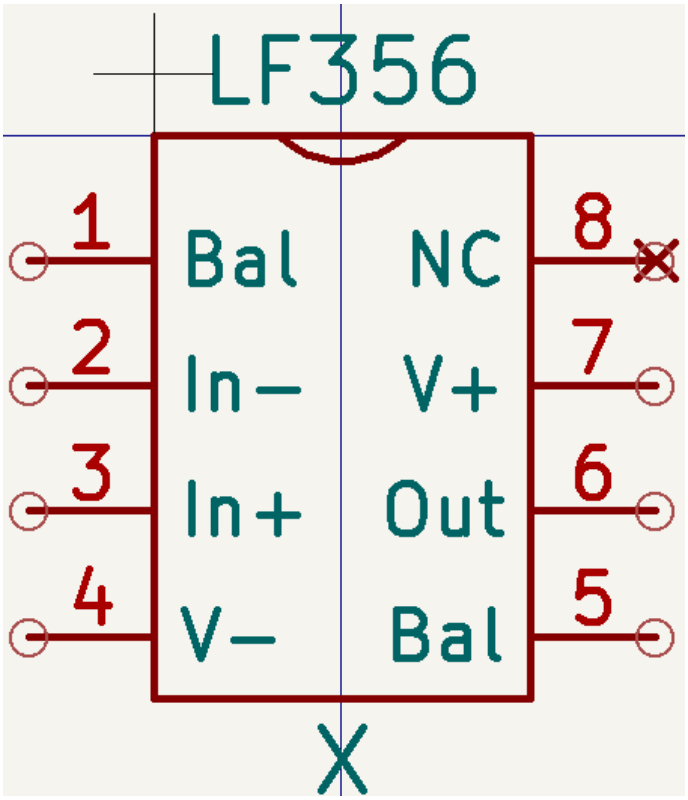

Figure 4.34: Pin Diagram of LF356

4.5.3 Test Circuit

A test circuit for the LF356 can be set up to verify its basic inverting or non-inverting amplification using two external JFETs and one pulse source. In this setup, the pulse source provides the input signal to the op-amp. The two JFETs are used as input devices to simulate high-impedance conditions and minimize loading on the op-amp inputs, reflecting the LF356s JFET-input characteristics. The op-amp is powered with a dual supply (V+ and V), and the output is connected to a plot component or oscilloscope to observe the amplified waveform. When the pulse signal is applied, the output waveform shows the inverted or amplified version of the input, demonstrating the op-amps high input impedance, low noise, and fast response in the test configuration.

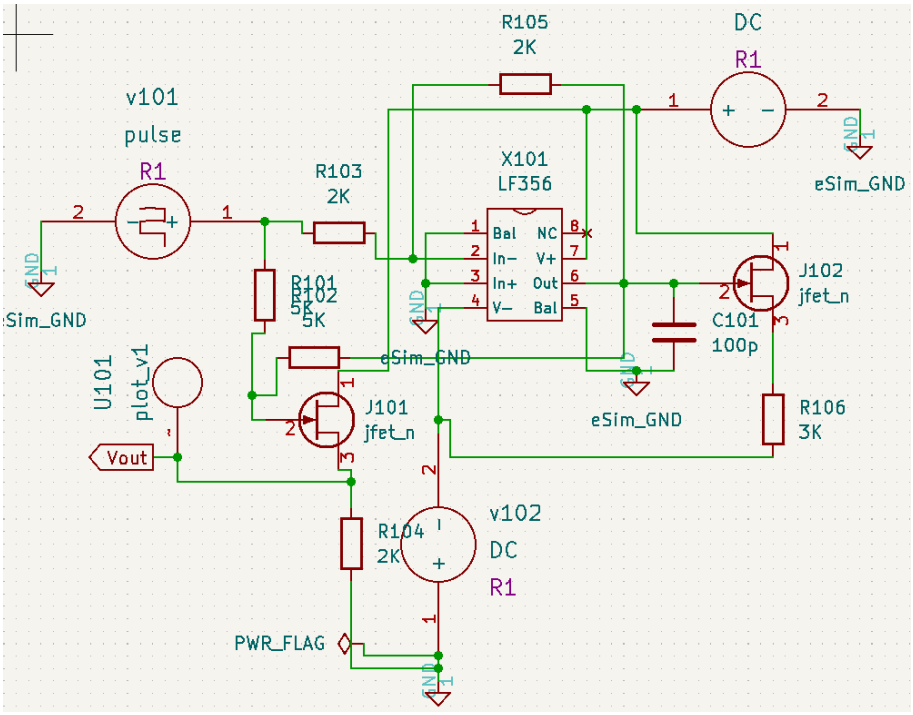

Figure 4.35: Test Circuit of LF356

4.5.4 Output Waveform

The output waveform observed from the LF356 test circuit shows a clean and fast response to the applied pulse input. When the pulse source is applied through the JFET-based input stage, the output follows the expected amplified (or inverted) pulse shape, depending on the circuit configuration. The waveform exhibits sharp rising and falling edges, indicating the high slew rate and wide bandwidth of the LF356. Minimal distortion, low noise, and quick settling of the output confirm the proper operation of the JFETBJT hybrid architecture, validating the op-amps suitability for high-speed and precision analog applications.

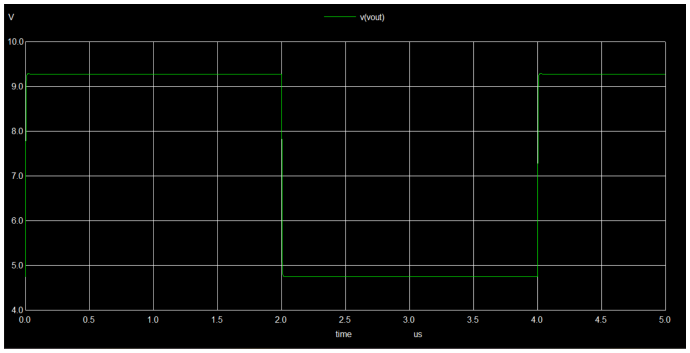

Figure 4.36: Output Waveform

4.6 CD4075

The CD4075B is a CMOS logic IC that contains three independent 3-input OR gates in a single package. Each gate performs the Boolean function Y=A+B+C in positive logic, producing a HIGH output when any one or more of the three inputs is HIGH. The device operates over a wide supply voltage range, offers low power consumption, high noise immunity, and stable operation, and is well suited for digital logic, signal combining, and control applications

4.6.1 Subcircuit Layout

The subcircuit schematic of the CD4075B can be explained using basic logic blocks such as inverters, NAND gates, and an active-LOW buffer. Each 3-input OR gate is internally realized by first passing the three inputs through inverters to generate their complements. These inverted signals are then applied to a 3-input NAND gate, which produces an inverted OR function according to De Morgans theorem. The output of the NAND gate is finally fed through an inverter / active-LOW buffer to restore positive logic at the output. This inverterNANDinverter structure ensures correct OR operation while providing proper signal drive, noise immunity, and stable CMOS performance for each of the three independent gates.

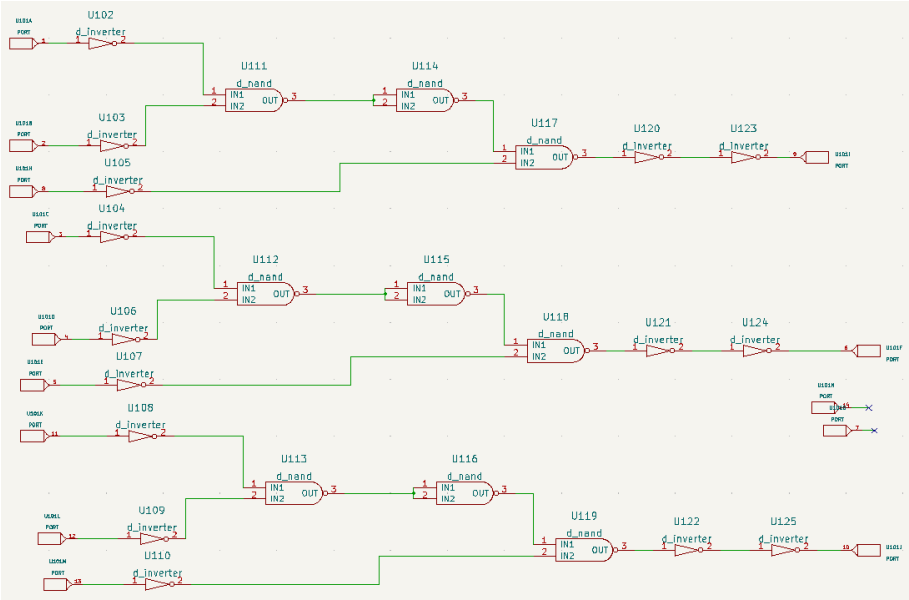

Figure 4.37: Internal Schematic

4.6.2 IC Layout

The IC pin diagram of the CD4075B corresponds to a 14-pin dual in-line package (DIP) that contains three independent 3-input OR gates. Each OR gate has three input pins and one output pin, grouped logically in the pin layout for easy identification. Pin 14 is connected to the positive supply voltage (VDD) and Pin 7 is connected to ground (VSS). The remaining pins are assigned to the input and out-

put terminals of the three OR gates, allowing each gate to operate independently. This pin arrangement simplifies circuit design and makes the CD4075B suitable for a wide range of CMOS digital logic applications.

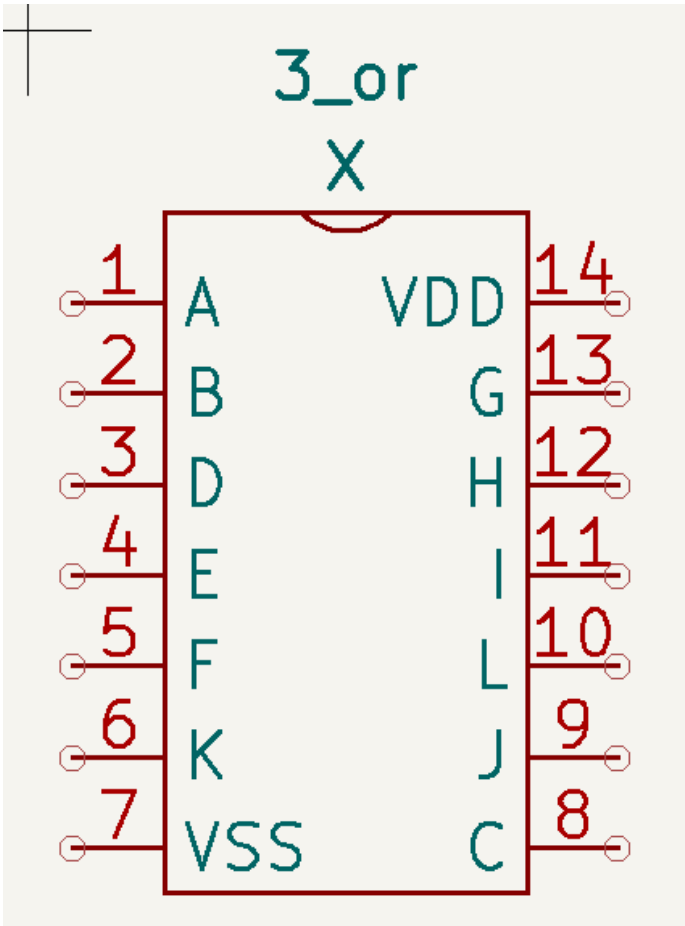

Figure 4.38: Pin Diagram

4.6.3 Test Circuit

The test circuit for the CD4075B is designed to verify the operation of its three independent 3-input OR gates. The IC is powered using a DC supply connected to VDD and VSS. For one OR gate under test, the three input pins are driven by pulse or logic signal sources to generate different input combinations over time. The output pin is connected to a plot component, logic probe, or LED with a current-limiting resistor to observe the response. During testing, the output remains LOW only when all three inputs are LOW, and transitions to HIGH whenever any one or more inputs go HIGH, confirming correct OR-gate functionality and reliable CMOS switching behavior.

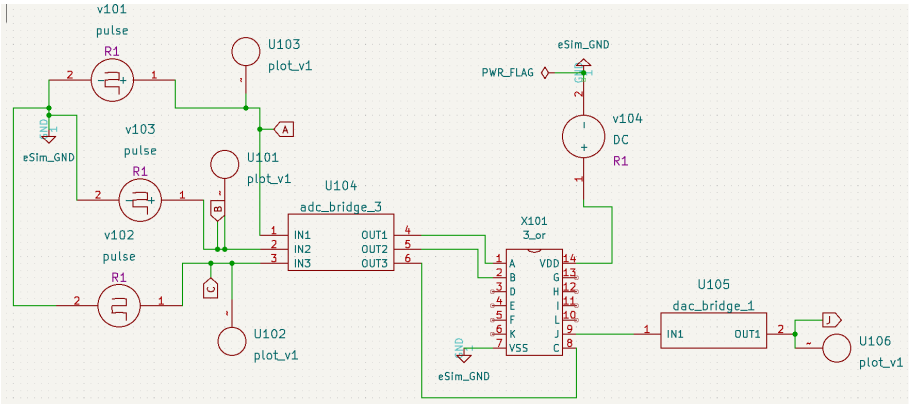

Figure 4.39: Test Circuit

4.6.4 Output Waveform

The output waveform plot shows the operation of the CD4075B 3-input OR gate along with the three input waveforms (A, B, and C). When all three input signals are LOW, the output waveform remains LOW. As soon as any one of the input waveforms goes HIGH, the output transitions to HIGH. When multiple inputs overlap at the HIGH level, the output stays HIGH for the entire duration of the overlap. The waveforms clearly demonstrate correct OR logic behavior, smooth CMOS switching, and proper timing alignment between the inputs and the output.

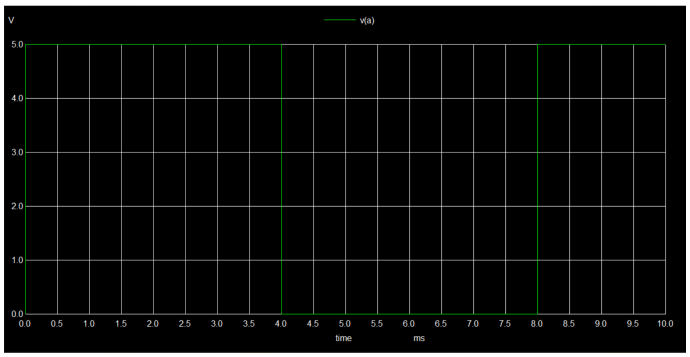

Figure 4.40: Input Waveform A

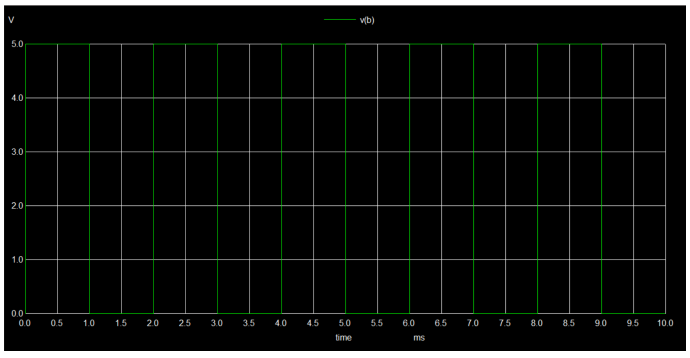

Figure 4.41: Input Waveform B

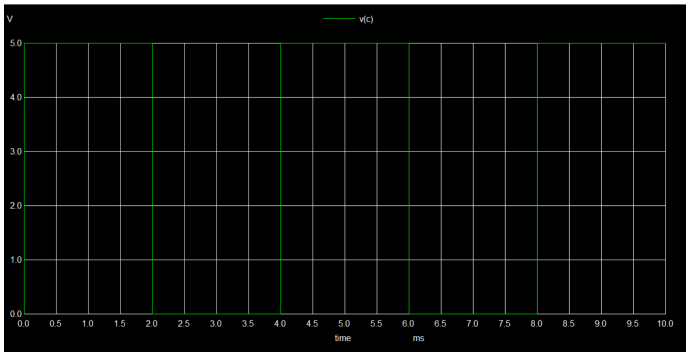

Figure 4.42: Input Waveform C

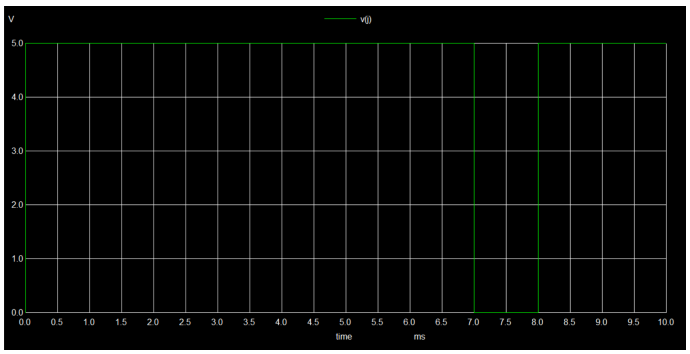

Figure 4.43: Output Waveform

4.7 SN74LVC1G386

The SN74LVC1G386 is a single 3-input XOR gate IC based on LVC (Low-Voltage CMOS) logic technology. It performs the Boolean function Y=ABC producing a HIGH output when an odd number of inputs are HIGH and a LOW output when an even number of inputs are HIGH. The device operates over a wide low-voltage supply range, offers very low power consumption, high-speed switching, and high noise immunity, and is suitable for parity generation/checking, digital signal processing, and logic control application

Function Table

INPUTS			OUTPUT
A	B	C	Y
L	L	L	L
L	L	H	H
L	H	L	H
L	H	H	L
H	L	L	H
H	L	H	L
H	H	L	L
H	H	H	H

Figure 4.44: Functional Table

4.7.1 Subcircuit Layout

The internal schematic of the SN74LVC1G386 implements a 3-input XOR function using buffers, inverters, 3-input AND gates, and NOR gates. The inputs are first buffered and inverted to generate both true and complemented signals, which are then combined in AND gates to form the required XOR logic terms. These terms are merged using NOR gates and final inverters to produce a HIGH output when an odd number of inputs are HIGH, ensuring fast, low-power, and reliable CMOS operation.

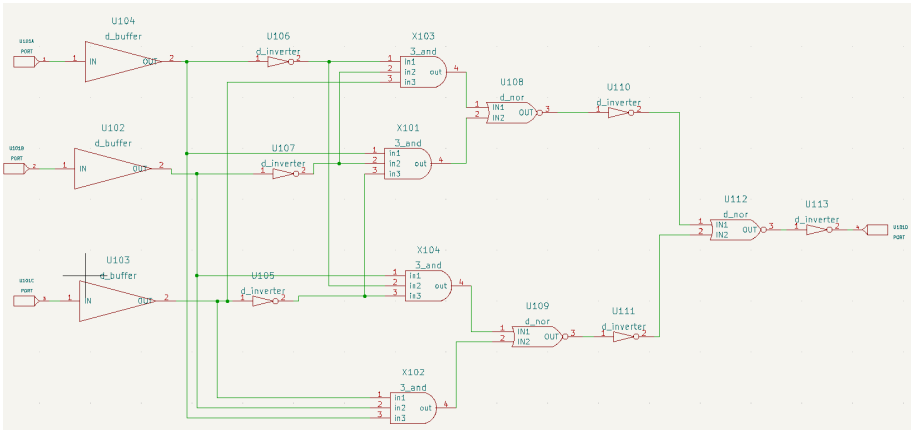

Figure 4.45: Internal Schematic

4.7.2 IC Layout

The IC pin diagram of the SN74LVC1G386 corresponds to a 6-pin dual in-line package (DIP) that contains three independent 3-input XOR gates. There are three input pin and one output pin. Pin 5 is connected to the positive supply voltage (VDD) and Pin 2 is connected to ground (VSS). The remaining pins are assigned

to the input and output terminals of the three XOR gates, allowing each gate to operate independently. This pin arrangement simplifies circuit design and makes the 74LVC1G386 suitable for a wide range of CMOS digital logic applications.

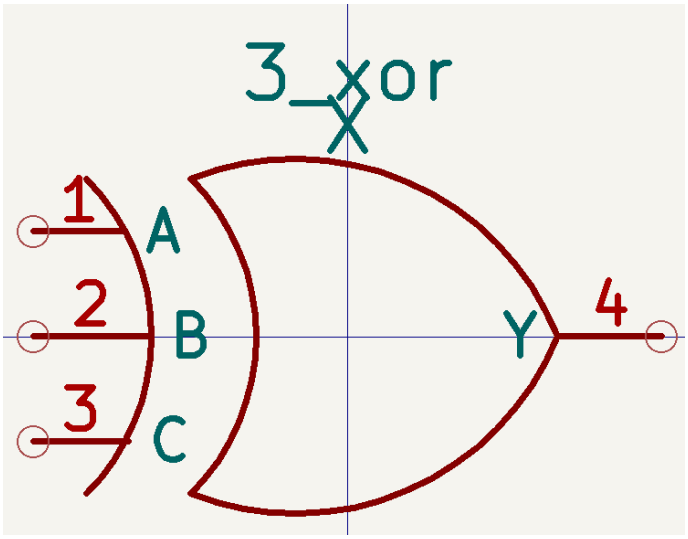

Figure 4.46: IC Symbol

4.7.3 Test Circuit

The test circuit for the XOR GATE IC is designed to verify the operation of its three independent 3-inputs. The IC is powered using a DC supply connected to VDD and VSS. For test, the three input pins are driven by pulse signal sources to generate different input combinations over time. The output pin is connected to a plot component to observe the response.As per XOR functionality, the output goes HIGH only when an odd number of inputs are HIGH. This arrangement allows quick verification of the ICs operation under varying input conditions.

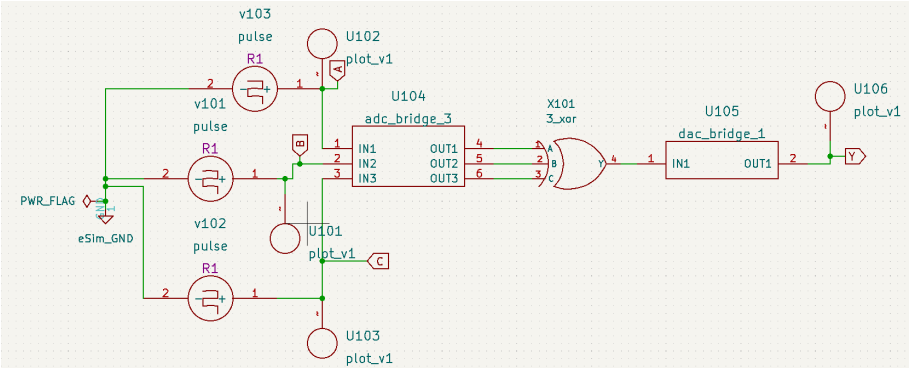

Figure 4.47: Test Circuit

4.7.4 Output Waveform

A 3-input XOR gate IC is tested by applying three pulse signals as inputs, generating all 8 possible combinations (000 to 111). The output, monitored with the inputs,

goes HIGH when an odd number of inputs are HIGH, allowing verification of the XOR functionality.

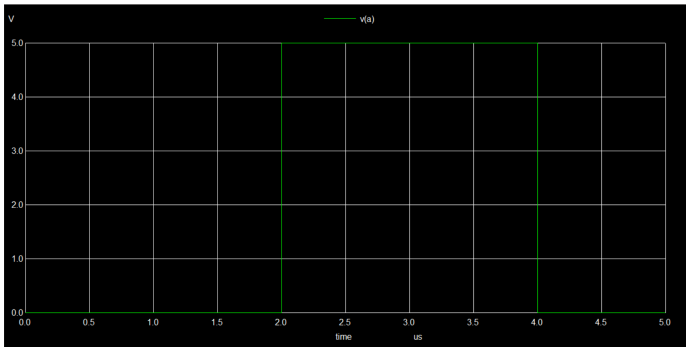

Figure 4.48: Input Waveform A

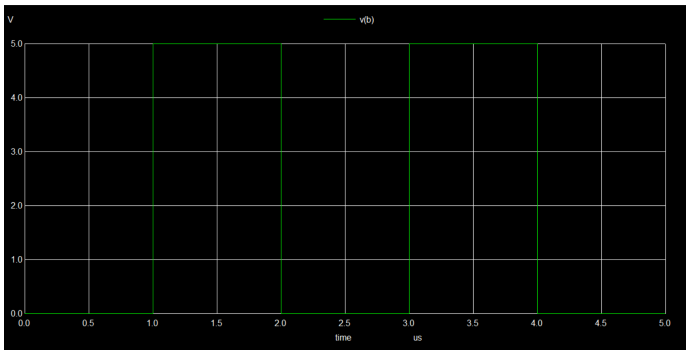

Figure 4.49: Input Waveform B

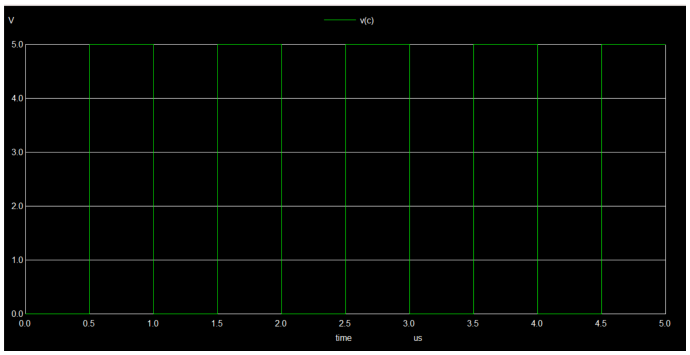

Figure 4.50: Input Waveform C

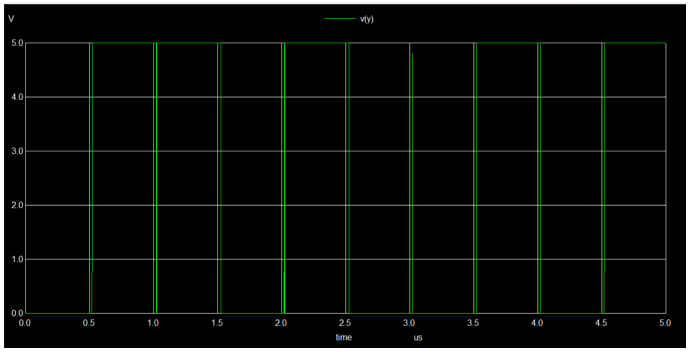

Figure 4.51: Output Waveform

4.8 CD4015B

The CD4015B contains two independent 4-stage serial-in/parallel-out shift registers. Each register has its own CLOCK, RESET, and DATA inputs, with Q outputs available from all four stages. Each stage is a D-type master-slave flip-flop, transferring the DATA input to the first stage and shifting it on every positive clock edge. A high on RESET clears all stages. Multiple CD4015BMS ICs can be cascaded to expand the register length beyond 8 stages.

4.8.1 Subcircuit Layout

The internal schematic of the CD4015B subcircuit consists of two identical and independent 4-stage shift registers, each built using a chain of D-type masterslave flip-flops. In each register, the DATA input feeds the first D flip-flop, and the output of each stage is connected to the input of the next stage, enabling serial data shifting. All flip-flops in a register share a common CLOCK line, which shifts the data one stage forward on every positive clock edge, and a common RESET line, which asynchronously clears all stages when driven HIGH. The Q outputs are taken from each flip-flop stage to provide parallel outputs of the stored data.

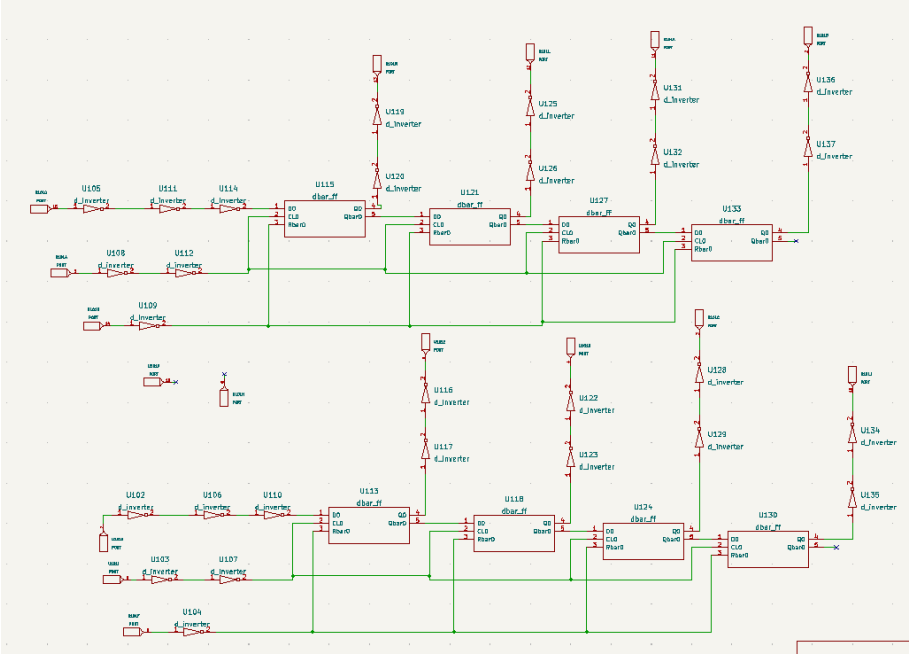

Figure 4.52: Internal Schematic

4.8.2 IC Layout

This IC layout represents the CD4015B dual 4-stage shift register in a 16-pin DIP package. It contains two independent sections: Register A and Register B. Each register has its own DATA input, CLOCK input, and RESET input, along with four parallel outputs (Q1 to Q4). Pins Q1AQ4A and DATA_A, CLOCK_A, RESET_A belong to Register A, while Q1BQ4B and DATA_B, CLOCK_B, RESET_B belong to Register B. VDD (pin 16) is the positive supply, and VSS (pin 8) is ground. This pin configuration allows independent operation or cascading of the two shift registers.

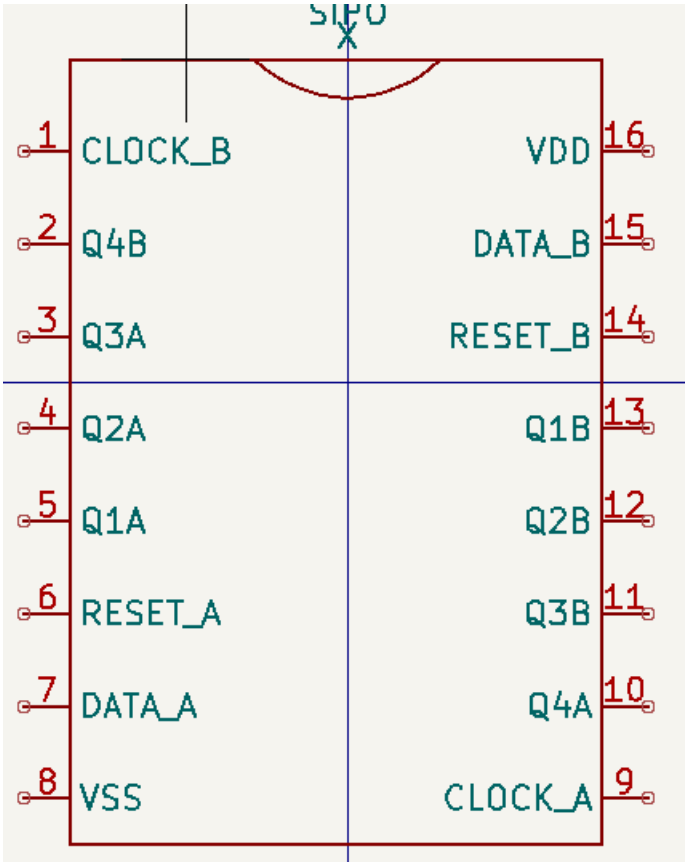

Figure 4.53: Pin Diagram

4.8.3 Test Circuit

In the CD4015BMS test circuit, VDD is connected to the positive supply and VSS to ground. DATA, CLOCK, and RESET inputs of the selected register are driven using pulse or logic sources. The RESET input is initially set HIGH to clear all stages, then pulled LOW for normal operation. Serial data is applied at the DATA pin and shifted through the register on each positive clock edge. The Q outputs (Q1Q4) are connected to plot function to observe correct shifting and verify proper IC operation.

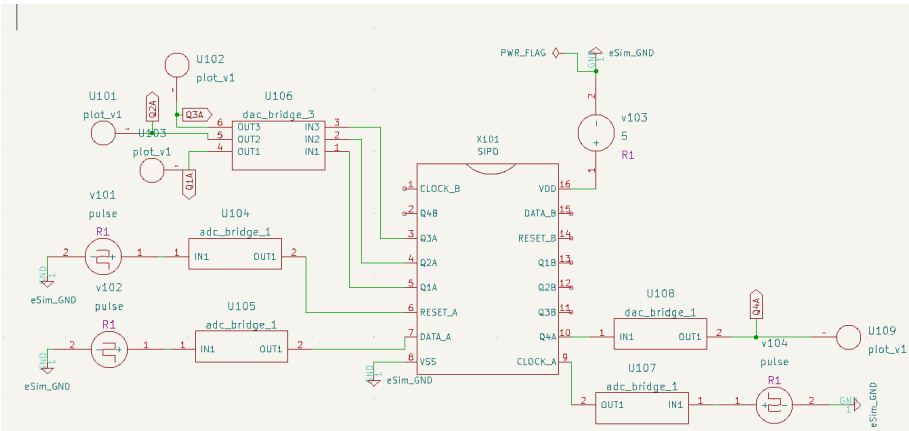

Figure 4.54: Test Circuit

4.8.4 Output Waveform

The output waveform of the CD4015BMS shows the serial data shifting through the register stages with each positive clock edge. As clock pulses are applied, the DATA input appears first at Q1, then sequentially at Q2, Q3, and Q4, each delayed by one clock period. When RESET is asserted HIGH, all output waveforms drop to LOW simultaneously. Observing the Q outputs together confirms correct timing, shifting action, and proper reset operation of the shift register.

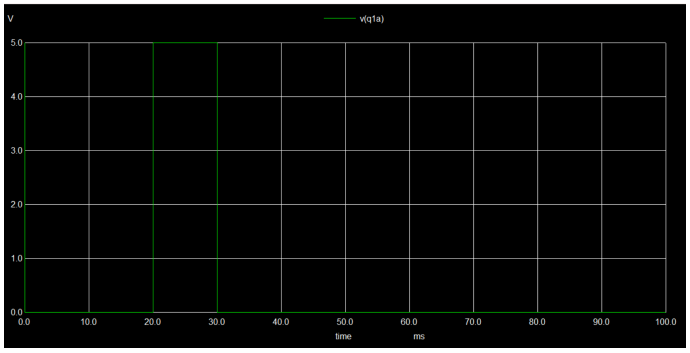

Figure 4.55: Output Q1

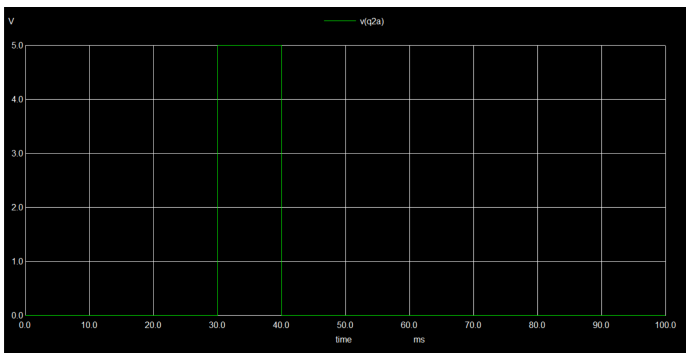

Figure 4.56: Output Q2

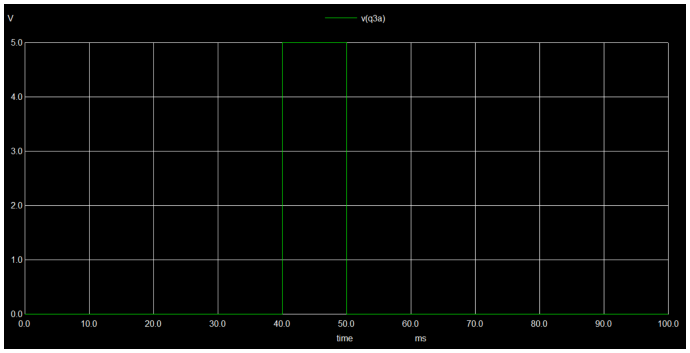

Figure 4.57: Output Q3

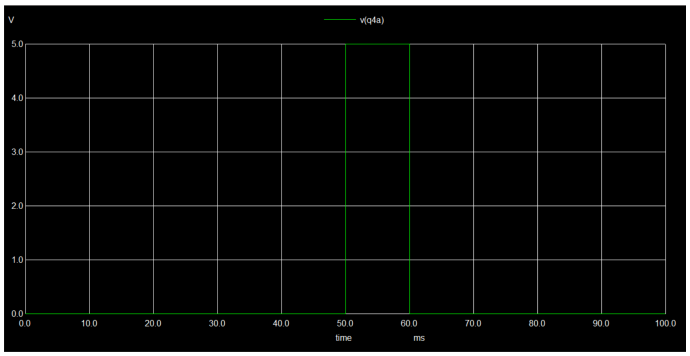

Figure 4.58: Output Q4

Chapter 5

Conclusion

The objective of this work to develop and validate subcircuits for both analog and digital integrated circuitswas successfully achieved. Each IC subcircuit was meticulously designed in accordance with the specifications provided in the respective official datasheets, and their performance was thoroughly verified using appropriate test circuits. The developed models include essential analog and digital building blocks such as multiplexers, inverters, shift registers, Operational amplifier, AND logic gates, OR logic gates and XOR logic gates.

All verified IC models are now ready to be integrated into the eSim subcircuit library, enabling students, educators, and developers to efficiently use them as modular components in circuit design and simulation. As the eSim device model library continues to expand, future work may focus on incorporating additional industry-relevant ICs, improving model accuracy, and developing application-specific subcircuits. This will further enhance eSim as a comprehensive and accessible platform for electronic system design and learning.

Reference

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- Texas Instruments: chrome-extension://efaidnbmnnnibpcajpcglclefindmkaj/https://www.ti.com/lit/ds/symlink/sn54als27a.pdf?ts=1768850120139&ref_url=https%253A%252F%252Fwww.google.com%252F
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- Texas Instruments: chrome-extension://efaidnbmnnnibpcajpcglclefindmkaj/https://www.ti.com/lit/ds/symlink/sn74hc04.pdf
- Texas Instruments: chrome-extension://efaidnbmnnnibpcajpcglclefindmkaj/https://www.ti.com/lit/ds/symlink/lf356-mil.pdf?ts=1768848039017&ref_url=https%253A%252F%252Fwww.google.com%252F
- Texas Instruments: chrome-extension://efaidnbmnnnibpcajpcglclefindmkaj/https://www.ti.com/lit/ds/symlink/cd4071b.pdf?ts=1768848090756&ref_url=https%253A%252F%252Fwww.google.com%252F
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