eSim Semester Long Internship
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On

Designing Integrated Circuit in eSim

Submitted by

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Contents

Acknowledgment **1**

1 Introduction **5**
1.1 Introduction . . . 5
1.1.1 FOSSEE . . . 5
1.1.2 eSim . . . 5
1.1.3 Ngspice . . . 6
1.1.4 Makerchip . . . 6

2 Features Of eSim **7**

3 Problem Statement **8**
3.1 Approach . . . 8

4 SN74LS164 **10**
4.1 General Description . . . 10
4.2 Key Features . . . 10
4.3 Application . . . 11
4.4 Pin Diagram . . . 11
4.5 Subcircuit Schematic Diagram . . . 12
4.6 Test Circuit Schematic Diagram . . . 12
4.7 Analysis details . . . 13
4.8 Source Details . . . 13
4.9 Input Plots . . . 14
4.10 Output Plots . . . 15

5 SN74LS173 **17**
5.1 General Description . . . 17
5.2 Key Features . . . 17
5.3 Application . . . 18
5.4 Pin Diagram . . . 18
5.5 Subcircuit Schematic Diagram . . . 19
5.6 Test Circuit Schematic Diagram . . . 19
5.7 Analysis details . . . 20
5.8 Source Details . . . 20
5.9 Input Plots . . . 22
5.10 Output Plots . . . 23

6 SN74LS169 **25**
6.1 General Description . . . 25

6.2 Key Features . . . 25
6.3 Application . . . 26
6.4 Pin Diagram . . . 26
6.5 Subcircuit Schematic Diagram . . . 27
6.6 Test Circuit Schematic Diagram . . . 27
6.7 Analysis details . . . 28
6.8 Source Details . . . 28
6.9 Input Plots . . . 29
6.10 Output Plots . . . 30

7 SN74HC157 31
7.1 General Description . . . 31
7.2 Key Features . . . 31
7.3 Application . . . 32
7.4 Pin Diagram . . . 32
7.5 Subcircuit Schematic Diagram . . . 33
7.6 Test Circuit Schematic Diagram . . . 33
7.7 Analysis details . . . 34
7.8 Source details . . . 34
7.9 Input Plots . . . 35
7.10 Output Plots . . . 36

8 SN74HC42 37
8.1 General Description . . . 37
8.2 Key Features . . . 38
8.3 Application . . . 38
8.4 Pin Diagram . . . 39
8.5 Subcircuit Schematic Diagram . . . 40
8.6 Test Circuit Schematic Diagram . . . 40
8.7 Analysis details . . . 41
8.8 Source Details . . . 41
8.9 Input Plots . . . 42
8.10 Output Plots . . . 43

9 SN74HC541 45
9.1 General Description . . . 45
9.2 Key Features . . . 45
9.3 Application . . . 46
9.4 Pin Diagram . . . 46
9.5 Subcircuit Schematic Diagram . . . 47
9.6 Test Circuit Schematic Diagram . . . 48
9.7 Analysis details . . . 48
9.8 Source details . . . 48
9.9 Input Plots . . . 49
9.10 Output Plots . . . 49

10 MC14532B 50
10.1 General Description . . . 50
10.2 Key Features . . . 50

10.3 Application . . . 51
10.4 Pin Diagram . . . 51
10.5 Subcircuit Schematic Diagram . . . 52
10.6 Test Circuit Schematic Diagram . . . 53
10.7 Analysis details . . . 53
10.8 Source details . . . 53
10.9 Input Plots . . . 54
10.10Output Plots . . . 55

11 74F182 **57**
11.1 General Description . . . 57
11.2 Key Features . . . 57
11.3 Application . . . 58
11.4 Pin Diagram . . . 58
11.5 Subcircuit Schematic Diagram . . . 59
11.6 Test Circuit Schematic Diagram . . . 60
11.7 Analysis details . . . 60
11.8 Source details . . . 61
11.9 Input Plots . . . 62
11.10Output Plots . . . 63

12 SN74F257 **64**
12.1 General Description . . . 64
12.2 Key Features . . . 64
12.3 Application . . . 65
12.4 Pin Diagram . . . 65
12.5 Subcircuit Schematic Diagram . . . 66
12.6 Test Circuit Schematic Diagram . . . 67
12.7 Analysis details . . . 67
12.8 Source details . . . 68
12.9 Input Plots . . . 69
12.10Output Plots . . . 70

13 Failed ICs **71**
13.1 Failed IC: 74F385 . . . 71
13.1.1 General Overview . . . 71
13.1.2 Test Circuit Schematic . . . 72
13.1.3 Issues Faced . . . 73
13.2 Failed IC: MC14518B . . . 74
13.2.1 General Overview . . . 74
13.2.2 Test Circuit Schematic . . . 74
13.2.3 Issues Faced . . . 74

14 Conclusion and Future Scope **75**

Chapter 1

Introduction

1.1 Introduction

1.1.1 FOSSEE

FOSSEE, an abbreviation for Free/Libre and Open Source Software for Education, is an initiative based at the Indian Institute of Technology (IIT) Bombay. It operates under the National Mission on Education through Information and Communication Technology (NMEICT), a program by the Ministry of Education (MoE), Government of India.

It promotes the adoption and integration of FLOSS (Free/Libre and Open Source Software) tools to enhance the quality of education in India. FOSSEE aims to reduce the reliance on proprietary software in educational institutions by advocating for the use of open-source alternatives. Through various outreach and development activities, the project supports the replacement of commercial software with equally capable FLOSS tools. Additionally, FOSSEE actively contributes to the creation of new tools and the enhancement of existing ones to better align with the evolving needs of academia and research.

1.1.2 eSim

eSim (previously known as Oscad/FreeEDA) is a free/libre and open-source Electronic Design Automation (EDA) tool developed as part of the FOSSEE project, based at IIT Bombay. It supports circuit design, simulation, analysis, and PCB design, making it a comprehensive platform for electronics design.

Built using a suite of open-source tools such as KiCad, Ngspice, GHDL, OpenModelica, Verilator, Makerchip, and the SkyWater SKY130 PDK, eSim is released under the GNU General Public License (GPL). eSim can effectively replace commercially licensed software such as OrCAD, PSpice, LTspice, Xpedition, and HSPICE, thus serving as a cost-effective and accessible alternative for educational institutions, students, researchers, and small and medium enterprises (SMEs), along with supporting the broader mission of reducing reliance on commercial software in academia and industry.

The key features of eSim include:

- Schematic design and simulation using KiCad and Ngspice
- PCB layout and Gerber file generation

- Mixed-signal simulation support
- Model and subcircuit editing via Model Builder and Subcircuit Builder
- OpenModelica interface for system-level modeling
- Compatible with Ubuntu and Windows

1.1.3 Ngspice

NgSpice is an open-source, text-based SPICE simulator used for analyzing analog, digital, and mixed-signal electronic circuits. It supports a wide range of simulations including DC, AC, transient, and noise analysis, and can handle various components such as MOSFETs, BJTs, JFETs, diodes, resistors, capacitors, and inductors. Users define circuits using netlists, and the simulator generates outputs like voltage and current waveforms or data files. NgSpice is customizable, integrates well with tools like KiCad and eSim, and is widely used in both academic and professional environments for circuit design and research.

1.1.4 Makerchip

Makerchip is an easy-to-use platform for digital circuit design that works both in a web browser and on a desktop. It allows users to write, simulate, and debug Verilog, SystemVerilog, and Transaction-Level Verilog code. Makerchip uses a mix of open-source and other tools to offer a wide range of features. It connects with eSim through a Python tool called Makerchip-App, which helps open the Makerchip interface. The platform is designed to be simple and helpful for users at any level, with clear workflows and useful features. While most open-source tools focus only on one task like simulation or PCB design, eSim fills this gap by combining design, simulation, and layout in one place.

Chapter 2

Features Of eSim

The objective behind the development of eSim is to provide an open source EDA solution for electronics and electrical engineers. The software should be capable of performing schematic creation, PCB design and circuit simulation (analog, digital and mixed-signal). It should provide facilities to create new models and components. Thus, eSim offers the following features:

1. **Schematic Creation:** eSim provides an easy-to-use graphical interface for drawing circuit schematics, making it accessible for users of all levels. Users can drag and drop components from the library onto the schematic, simplifying the design process. Comprehensive editing tools allow for easy modification of schematics, including moving, rotating, and labeling components.

2. **Circuit Simulation:** eSim supports SPICE (Simulation Program with Integrated Circuit Emphasis), a standard for simulating analog and digital circuits. Users can perform various types of analysis such as transient, AC, and DC, providing insights into circuit behavior over time and frequency. An integrated waveform viewer helps visualize simulation results, aiding in the analysis and debugging of circuit designs.

3. **PCB Design:** The PCB layout editor allows users to place components and route traces with precision. eSim includes DRC capabilities to ensure that the PCB design adheres to manufacturing constraints and electrical rules. Users can generate Gerber files, which are standard for PCB fabrication, directly from their designs.

4. **Subcircuit Feature:** This feature enables users to create complex circuits by integrating smaller, simpler subcircuits, promoting modular and hierarchical design approaches. Subcircuits can be reused in different projects, saving time and effort in redesigning common circuit elements.

5. **Open Source Integration:** eSim integrates several open-source tools like KiCad, Ngspice, and GHDL, providing a comprehensive suite for electronic design automation. Being open-source, eSim is free to use, making advanced circuit design tools accessible without the need for expensive licenses.

Chapter 3

Problem Statement

To design and develop various Analog and Digital Integrated Circuit Models in the form of sub-circuits using device model files already present in the eSim library. These IC models should be useful in the future for circuit designing purposes by developers and users, once they get successfully integrated into the eSim subcircuit Library.

3.1 Approach

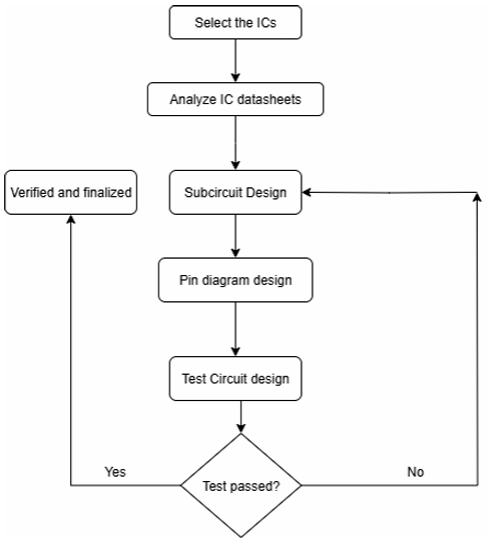


Figure 3.1: Flowchart of approach for designing IC models

Our approach to implementing the problem statement followed a structured methodology, leveraging datasheets from leading IC manufacturers such as Texas Instruments, Analog Devices, and NXP Semiconductors.

The process was carried out in the following stages:

1. **Datasheet Analysis:** We began with a thorough review of datasheets for various analog and digital ICs to identify components not already available in the eSim library. This included analyzing internal schematics, truth tables, and component values to ensure the selected ICs provided unique or enhanced functionalities.

2. **Subcircuit Development:** Based on the datasheet specifications, we modeled the selected ICs as subcircuits in eSim using the available device model files. Special care was taken to replicate the pin configurations and symbols accurately, in alignment with official packaging and pin descriptions.

3. **Test Circuit Design:** We created test circuits for each subcircuit model to validate their functionality. These circuits were designed directly based on datasheet application examples, ensuring realistic and relevant testing.

4. **Simulation and Verification:** The test circuits were simulated using eSim and KiCad, generating NgSpice netlists and waveform outputs. We verified each subcircuit's behavior against expected results. In cases where discrepancies were found, we iteratively debugged and refined the designs until all test cases passed satisfactorily.

This rigorous process ensured the IC models were both accurate and reliable, contributing to the expansion of the eSim subcircuit library for future use in circuit design and simulation.

Chapter 4

SN74LS164

4.1 General Description

8-Bit Serial-In Parallel-Out Shift Register

The SN74LS164 is an 8-bit serial-in, parallel-out (SIPO) shift register fabricated using Schottky TTL (Transistor-Transistor Logic) technology. It is designed to accept serial data input and provide parallel outputs, making it suitable for applications requiring data conversion from serial to parallel form. The device consists of eight edge-triggered flip-flops connected in series, with each clock pulse shifting the input data one stage forward through the register.

The SN74LS164 features two serial data inputs (A and B), which are internally ANDed to allow flexible data control. An asynchronous active-low clear input is provided to reset all outputs to a low state independent of the clock. The device operates with a common clock input and offers reliable performance in high-speed digital systems. Its buffered outputs ensure compatibility with standard TTL logic levels and allow direct interfacing with other TTL-based components.

4.2 Key Features

The key features of SN74LS164 include:

- **8-Bit Serial-In Parallel-Out Operation:** Converts serial input data into eight parallel outputs efficiently.
- **Dual Serial Inputs:** Two serial inputs (A and B) are internally ANDed, enabling flexible data gating and control.
- **Asynchronous Clear:** Active-low clear input resets all outputs independently of the clock.
- **High-Speed Operation:** Designed using Schottky TTL technology for fast switching performance.
- **Buffered Outputs:** Outputs are buffered to reduce loading effects and improve drive capability.
- **TTL Compatible:** Fully compatible with standard TTL logic levels and interfaces easily with other LS-series devices.

4.3 Application

The various applications of SN74LS164 are:

- **Serial-to-Parallel Data Conversion:** Used to convert serial data streams into parallel outputs for interfacing serial communication devices with parallel processing systems.
- **LED and Display Driving:** Commonly employed to drive LEDs, seven-segment displays, and indicator panels where multiple outputs are controlled using a minimal number of input lines.
- **Data Storage and Buffering:** Acts as a temporary storage element for serial data before parallel processing, improving data handling efficiency.
- **Digital Control Systems:** Utilized in digital control and automation systems to expand output ports of microcontrollers and processors.
- **Timing and Sequencing Applications:** Used in applications requiring sequential control of outputs based on clock pulses, such as counters and shift-based logic circuits.

4.4 Pin Diagram

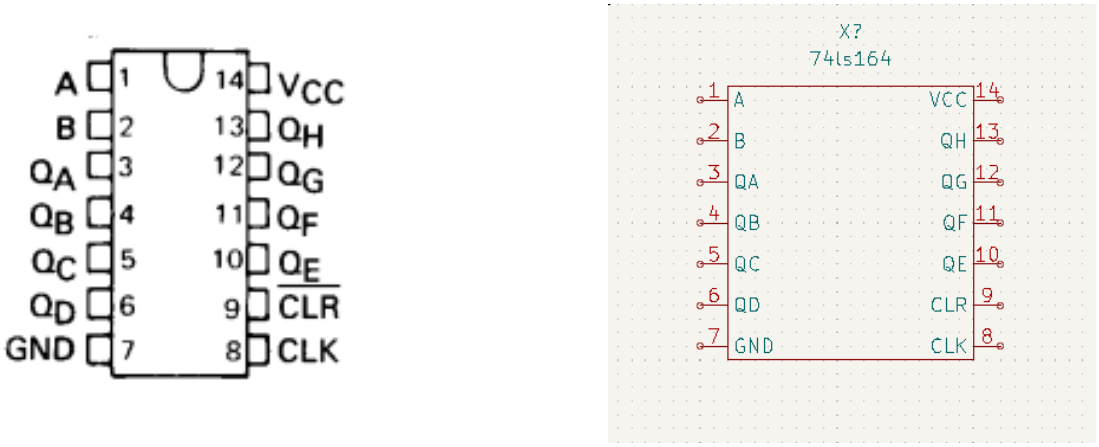


Figure 4.1: Pin diagram

4.5 Subcircuit Schematic Diagram

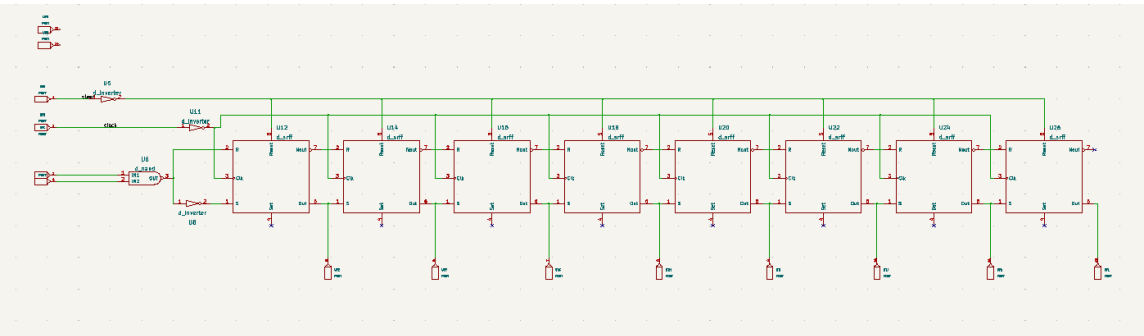


Figure 4.2: Subcircuit Schematic Diagram of SN74LS164

4.6 Test Circuit Schematic Diagram

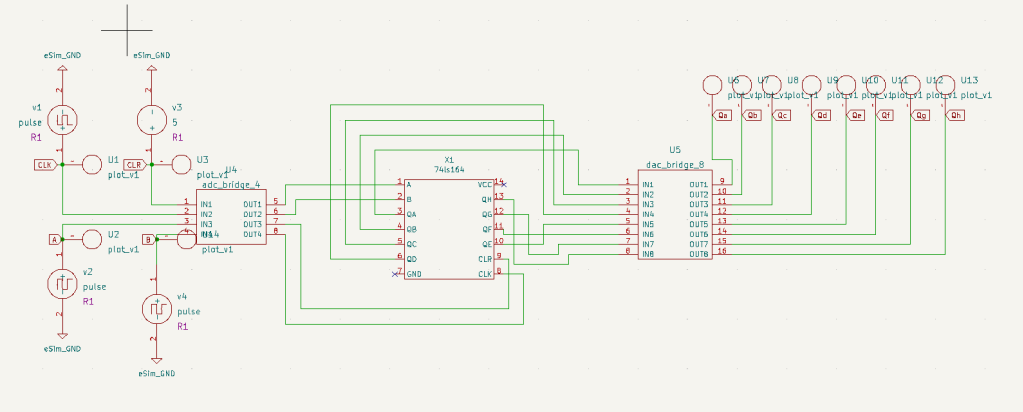


Figure 4.3: Test Circuit Schematic Diagram of SN74LS164

4.7 Analysis details

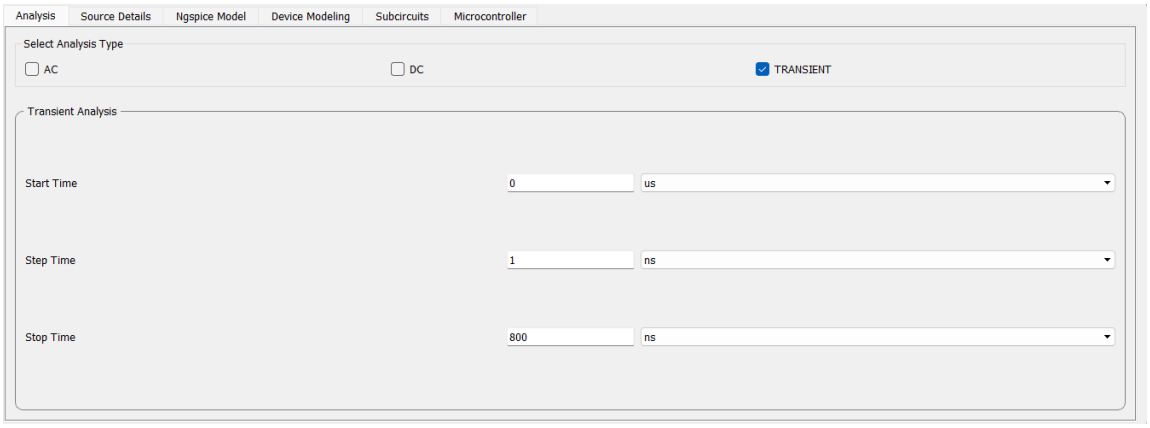


Figure 4.4: Analysis details of SN74LS164

4.8 Source Details

Figure 4.5: Source Details of SN74LS164

4.9 Input Plots

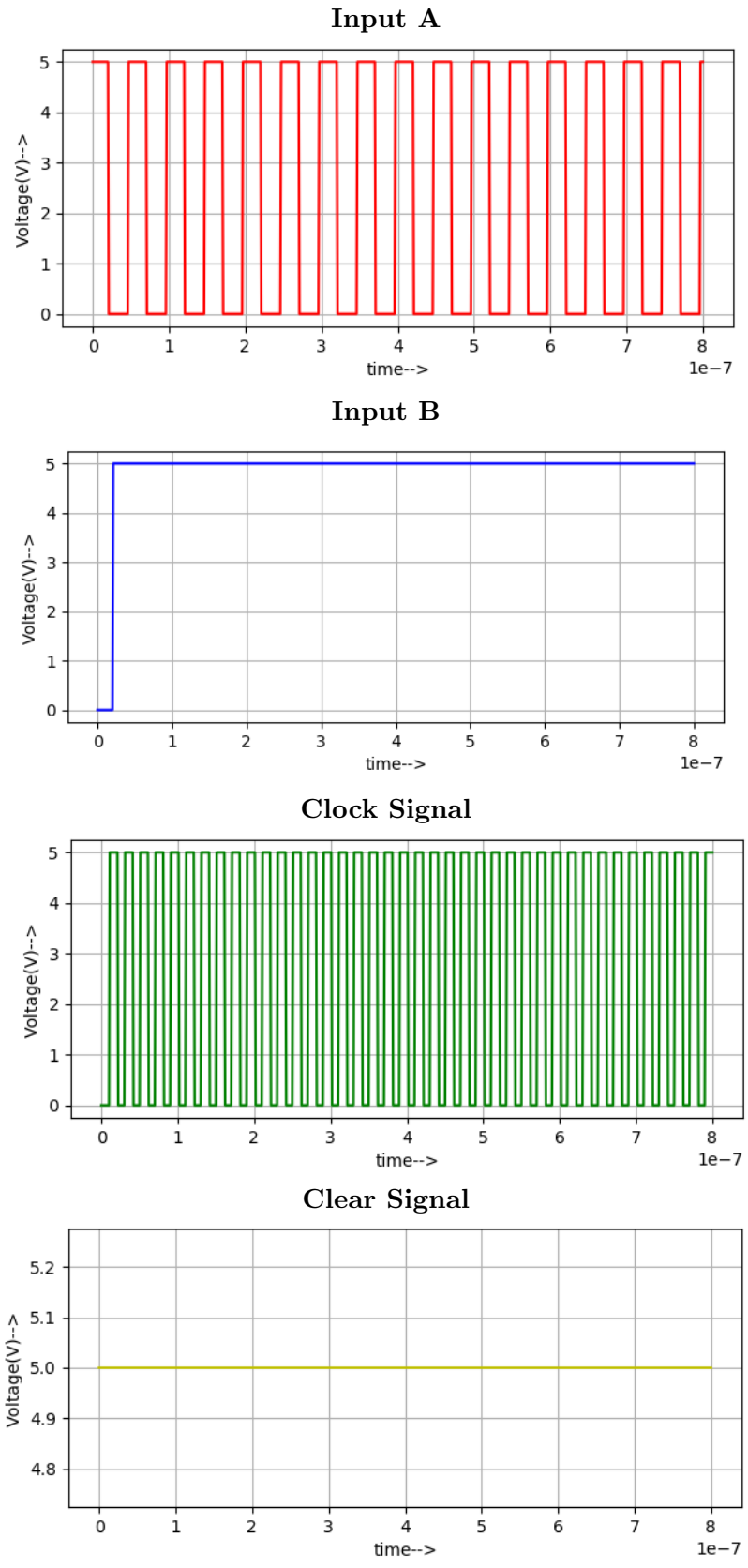


Figure 4.6: Input plots of SN74LS164

4.10 Output Plots

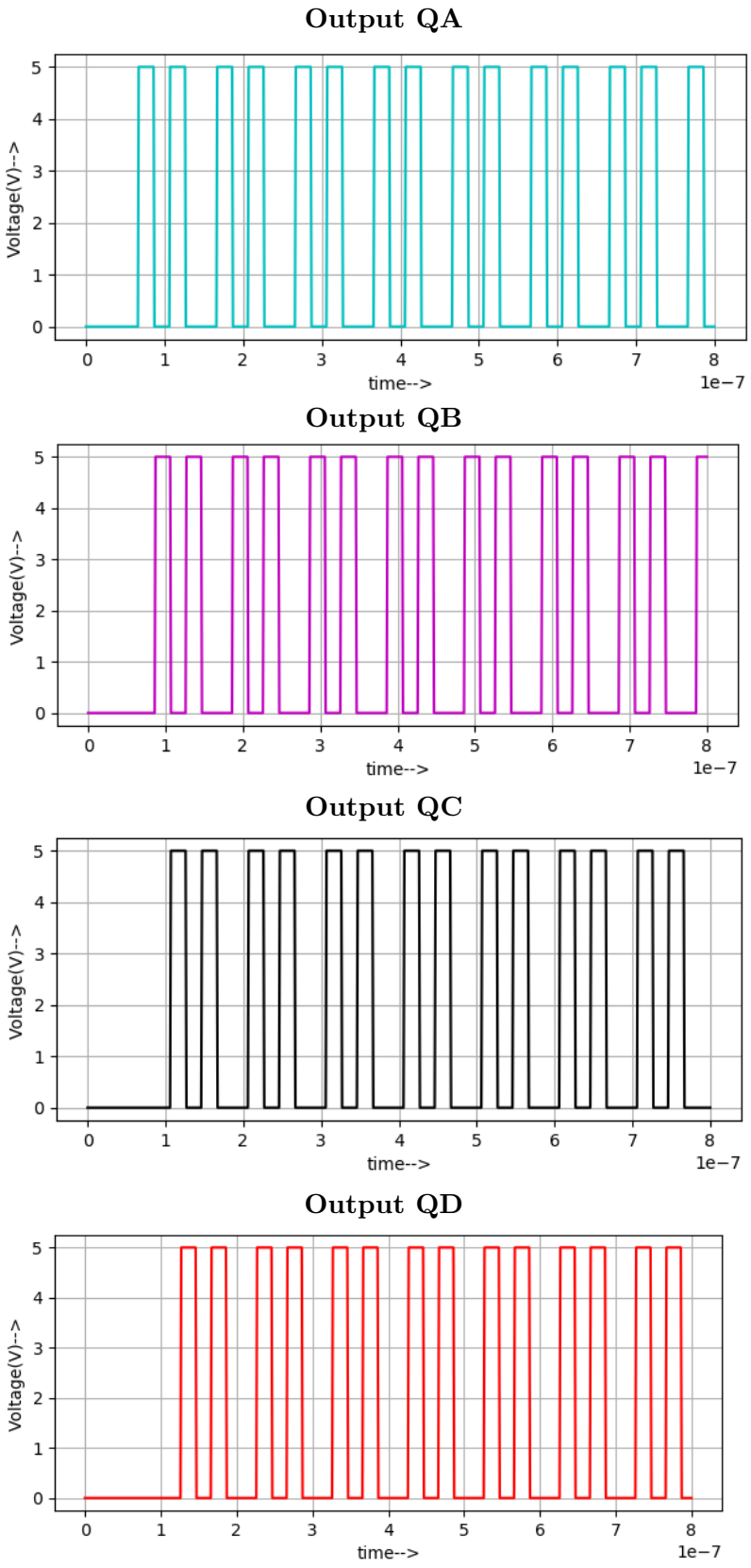


Figure 4.7: Output plots of SN74LS164

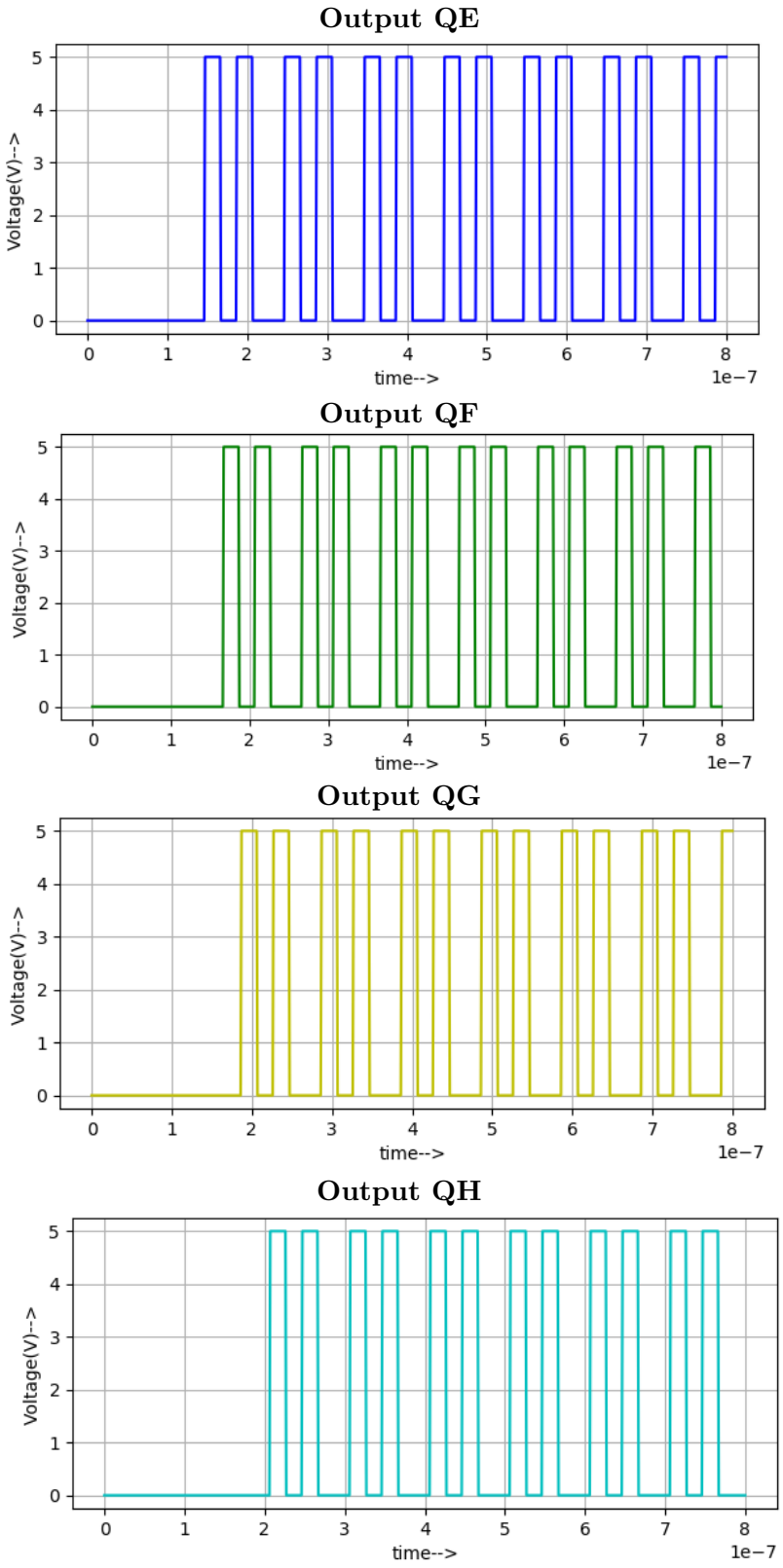


Figure 4.8: Output plots of SN74LS164

Chapter 5

SN74LS173

5.1 General Description

4-Bit D-Type Register with 3-State Outputs

The SN74LS173 is a 4-bit D-type register fabricated using Schottky TTL (Transistor-Transistor Logic) technology. It is designed to store and transfer 4-bit binary data and is commonly used in data storage and temporary buffering applications within digital systems.

The device features four D-type flip-flops that are clocked simultaneously by a common clock input. Data present at the inputs is transferred to the outputs on the active clock edge, provided that the enable conditions are satisfied. The SN74LS173 includes two active-low enable inputs that control the loading of data into the register, allowing selective data storage.

In addition, the SN74LS173 provides 3-state outputs, enabling multiple registers to share a common bus without interference. When the output enable inputs are inactive, the outputs enter a high-impedance state, effectively disconnecting the register from the bus. This makes the SN74LS173 particularly suitable for bus-oriented architectures and microprocessor-based systems.

5.2 Key Features

The key features of SN74LS173 include:

- **4-Bit Parallel Data Storage:** Stores and transfers 4-bit binary data efficiently.
- **D-Type Flip-Flops:** Four edge-triggered D-type flip-flops ensure reliable data storage.
- **3-State Outputs:** Outputs can be placed in a high-impedance state, allowing safe connection to shared data buses.
- **Dual Enable Inputs:** Two active-low enable inputs provide flexible control over data loading.
- **Synchronous Operation:** Data is transferred in synchronization with the clock signal.

- **TTL Compatible:** Fully compatible with standard TTL logic levels and interfaces easily with other LS-series devices.

5.3 Application

The various applications of SN74LS173 are:

- **Data Storage and Register Applications:** Used as a temporary data storage register in digital systems, enabling reliable storage and transfer of 4-bit parallel data.
- **Bus-Oriented Systems:** The 3-state outputs allow the SN74LS173 to be connected to shared data buses, making it suitable for bus-based architectures without causing bus contention.
- **Microprocessor and Microcontroller Interfacing:** Commonly employed as an output or input register to interface microprocessors and microcontrollers with peripheral devices.
- **Buffering and Latching Applications:** Acts as a buffer or latch to hold data stable during processing, improving synchronization and data integrity in digital circuits.
- **Control and Automation Systems:** Used in control logic circuits where controlled storage and conditional transfer of data are required, such as in state machines and timing control units.

5.4 Pin Diagram

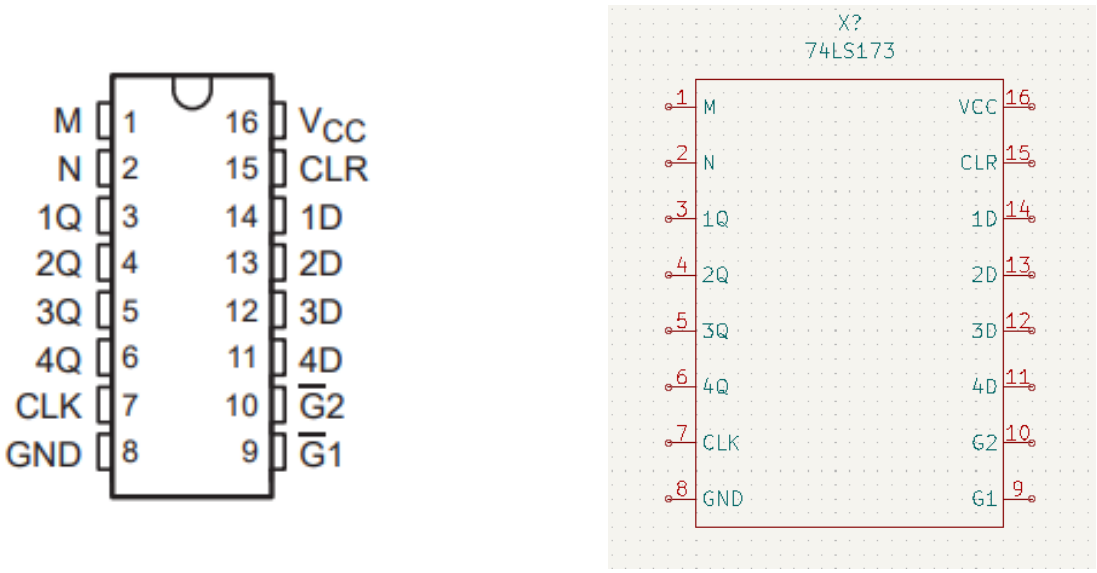


Figure 5.1: Pin diagram of SN74LS173

5.5 Subcircuit Schematic Diagram

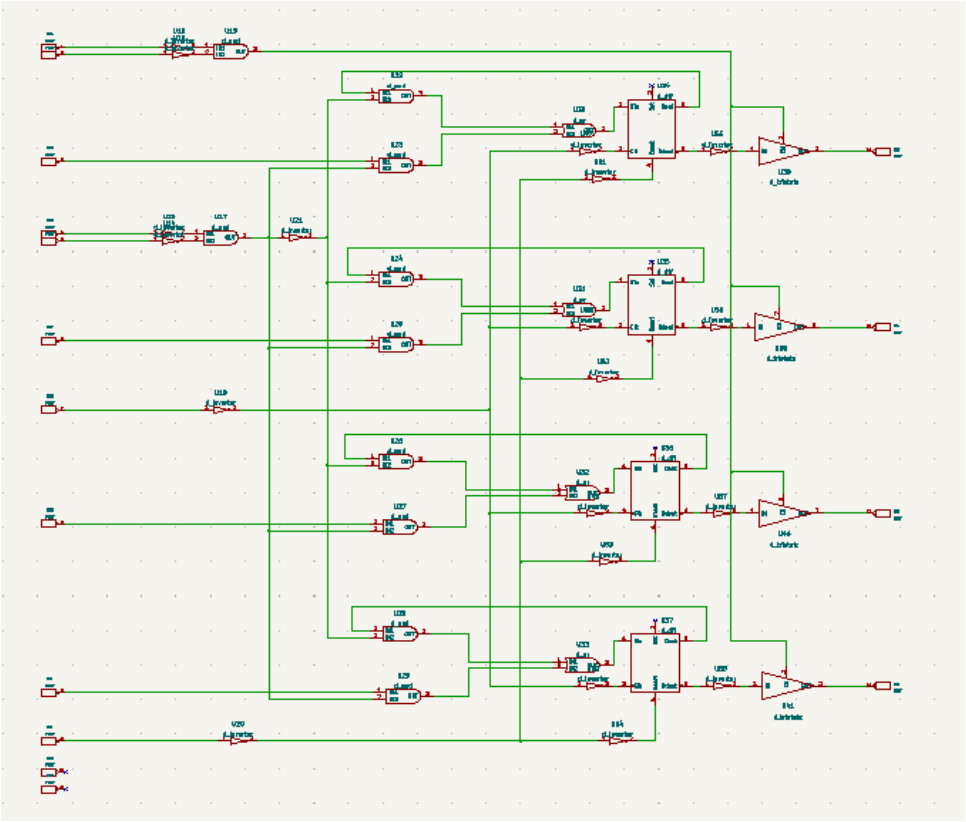


Figure 5.2: Subcircuit Schematic Diagram of SN74LS173

5.6 Test Circuit Schematic Diagram

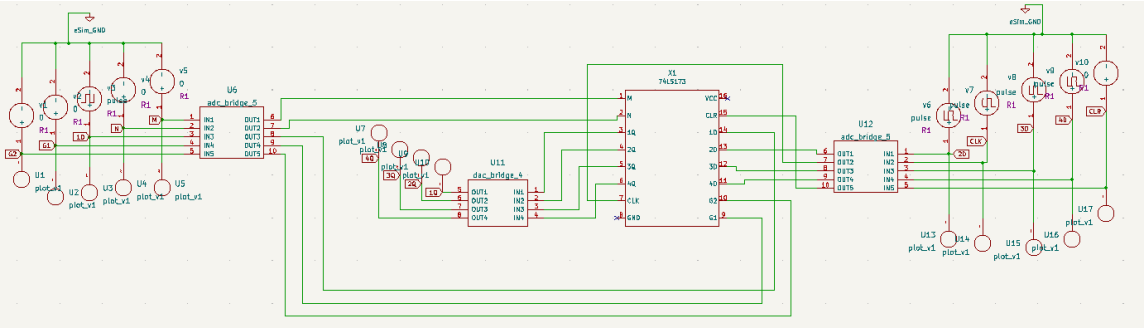


Figure 5.3: Test Circuit Schematic Diagram of SN74LS173

5.7 Analysis details

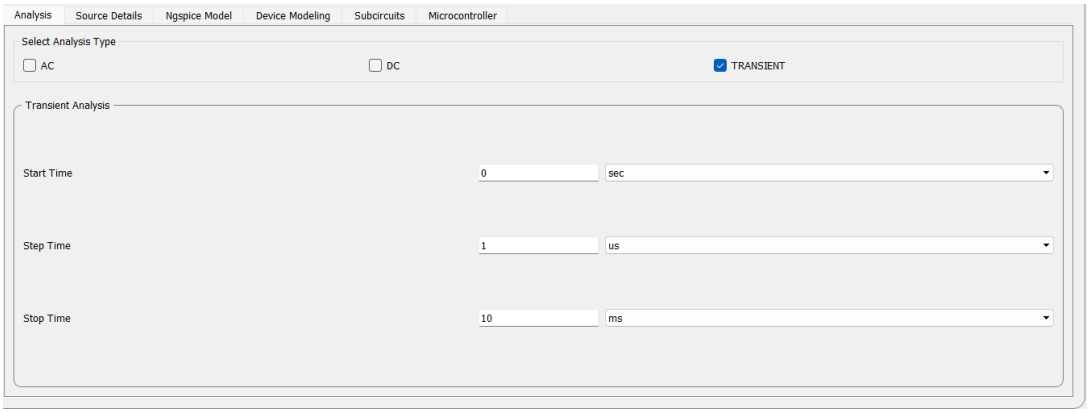


Figure 5.4: Analysis details of SN74LS173

5.8 Source Details

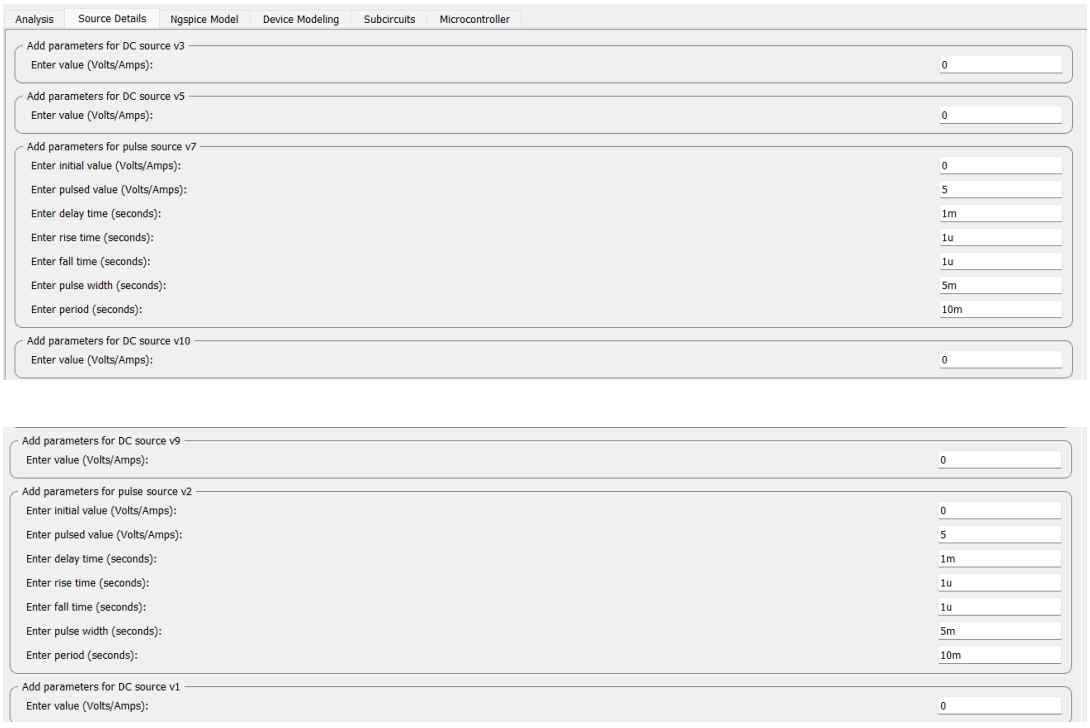


Figure 5.5: Source Details of SN74LS173

Figure 5.6: Source Details of SN74LS173

5.9 Input Plots

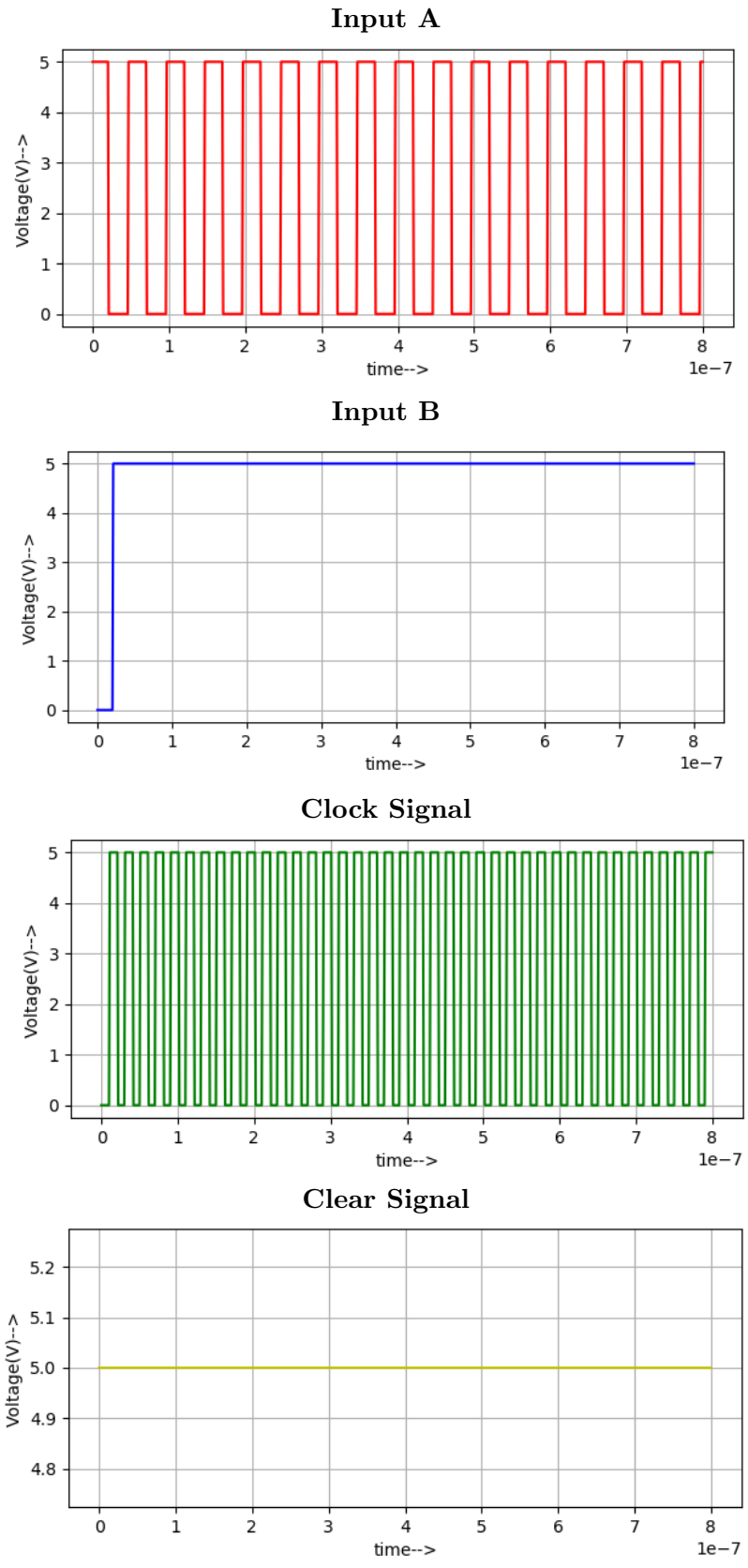


Figure 5.7: Input plots of SN74LS164

5.10 Output Plots

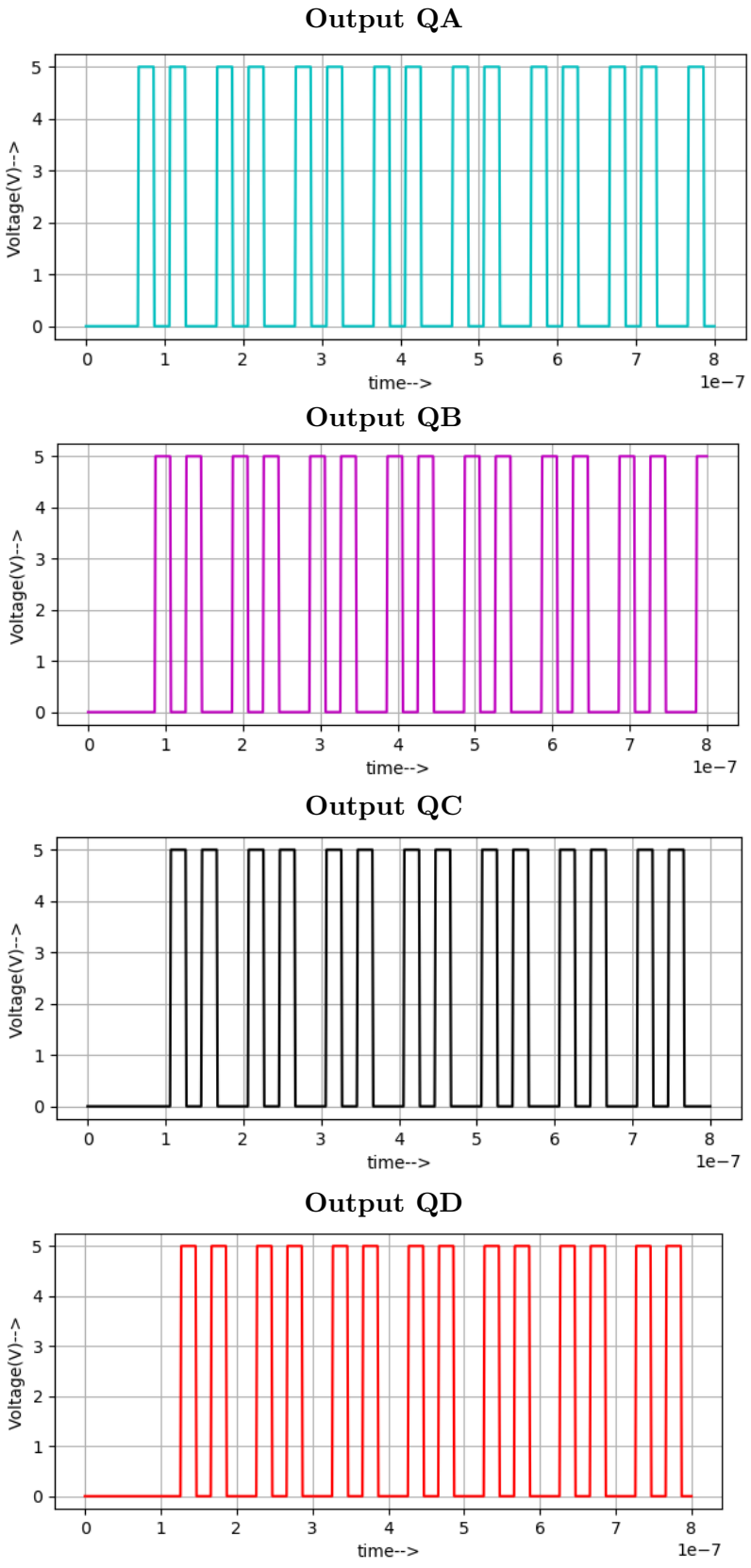


Figure 5.8: Output plots of SN74LS164

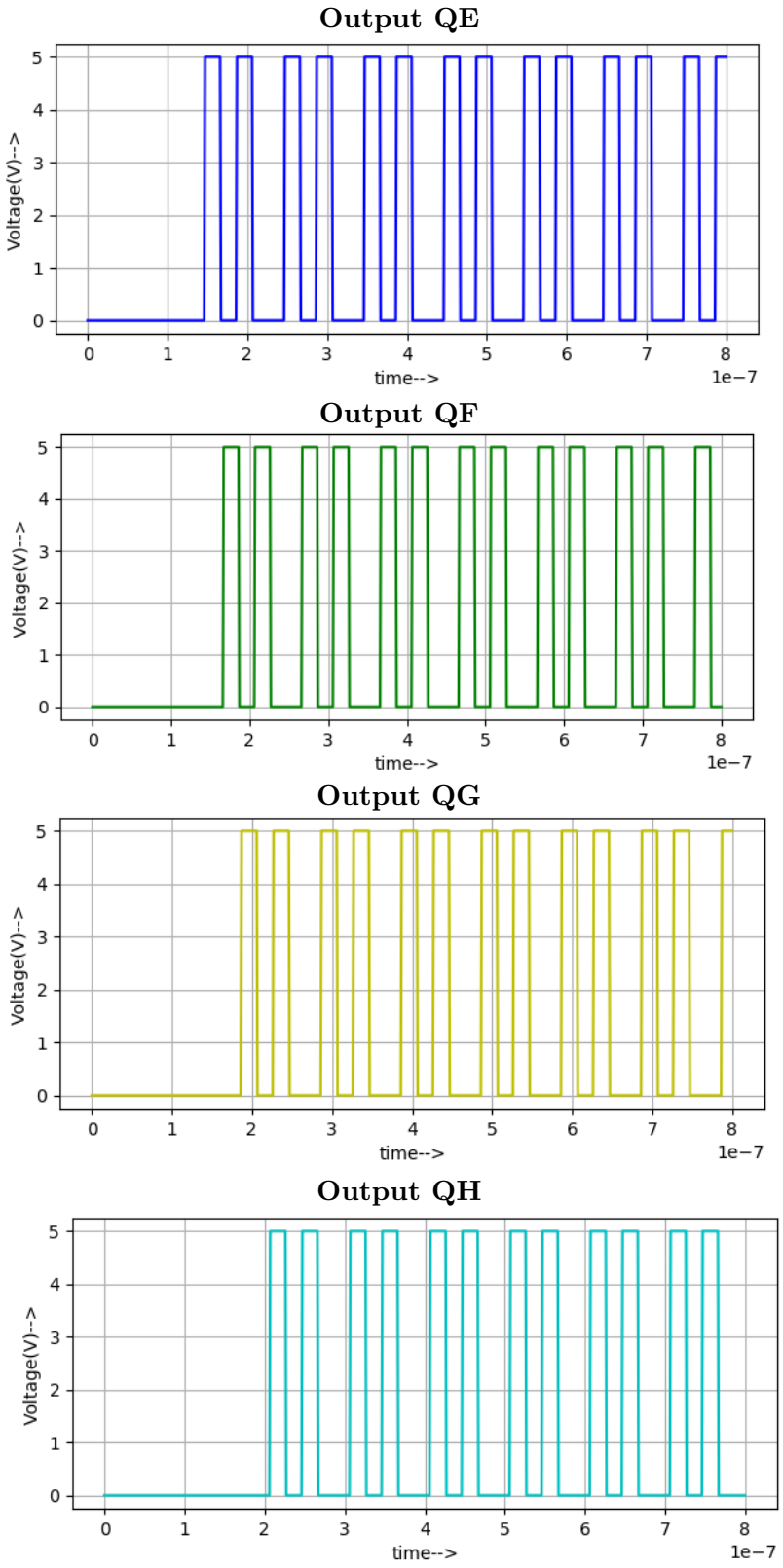


Figure 5.9: Output plots of SN74LS164

Chapter 6

SN74LS169

6.1 General Description

4-Bit Synchronous Up/Down Binary Counter

The SN74LS169 is a 4-bit synchronous up/down binary counter fabricated using Schottky TTL (Transistor-Transistor Logic) technology. It is designed to count in either ascending or descending order based on the control inputs, making it suitable for a wide range of counting and sequencing applications in digital systems.

The device features synchronous operation, meaning that all flip-flops are triggered simultaneously by a common clock signal. This eliminates the propagation delays commonly associated with ripple counters and ensures reliable high-speed performance. The SN74LS169 includes separate inputs for count enable and direction control, allowing precise control over the counting process.

An asynchronous clear input is provided to reset the counter to a known state. The outputs are buffered and TTL-compatible, enabling easy interfacing with other digital components. Due to its synchronous up/down counting capability and reliable operation, the SN74LS169 is commonly used in counters, timers, and control logic circuits.

6.2 Key Features

The key features of SN74LS169 include:

- **4-Bit Up/Down Counting:** Supports both upward and downward binary counting operations.
- **Synchronous Operation:** All flip-flops are clocked simultaneously, ensuring predictable and high-speed performance.
- **Direction Control Input:** Allows selection between up-counting and down-counting modes.
- **Count Enable Inputs:** Provides controlled counting and cascading capability.
- **Asynchronous Clear:** Resets the counter to a known initial state independent of the clock.
- **TTL Compatible Outputs:** Buffered outputs ensure compatibility with standard TTL logic levels.

6.3 Application

The various applications of SN74LS169 are:

- **Up/Down Counting Systems:** Used in digital systems that require both incrementing and decrementing count operations, such as reversible counters and bidirectional timers.
- **Frequency Division:** Commonly employed as a frequency divider in clock generation and timing circuits by utilizing its binary counting capability.
- **Timing and Sequencing Circuits:** Applied in timing control units and sequencing logic where precise synchronous counting is required.
- **Digital Clocks and Timers:** Used in digital clock circuits, stopwatches, and programmable timing applications.
- **Control and Automation Systems:** Integrated into control logic and automation systems for event counting, position tracking, and process monitoring.

6.4 Pin Diagram

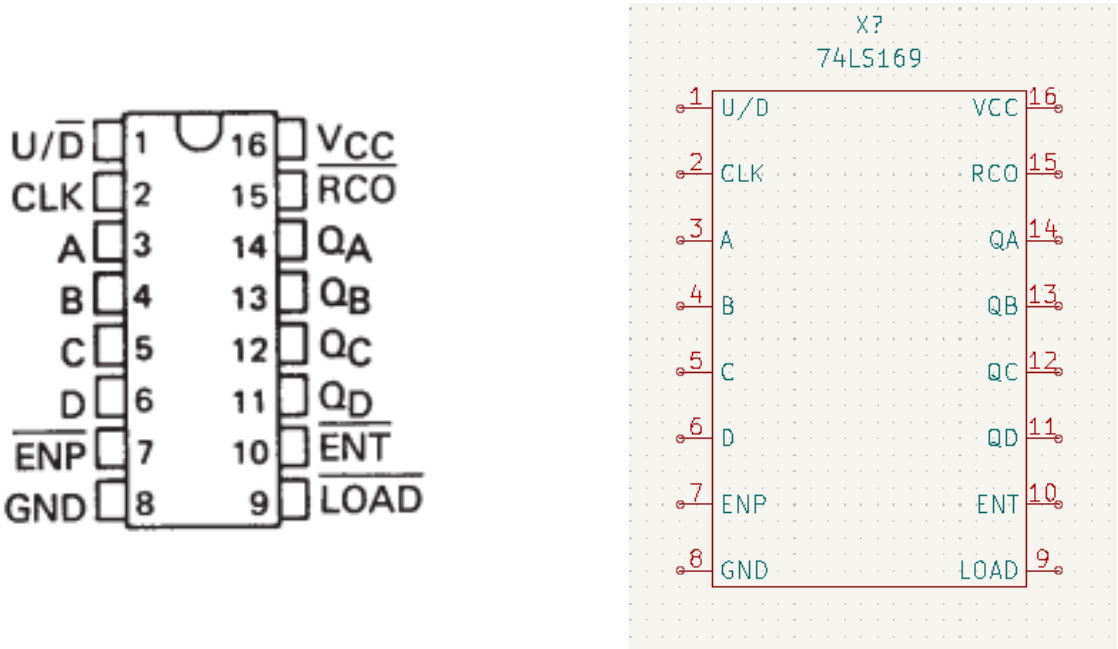


Figure 6.1: Pin diagram of SN74LS169

6.5 Subcircuit Schematic Diagram

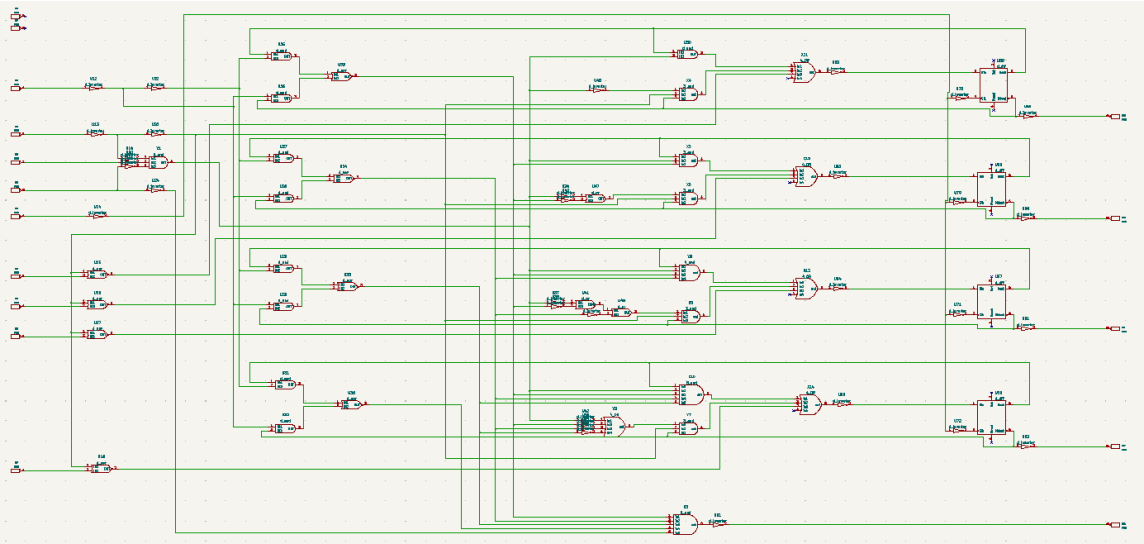


Figure 6.2: Subcircuit Schematic Diagram of SN74LS169

6.6 Test Circuit Schematic Diagram

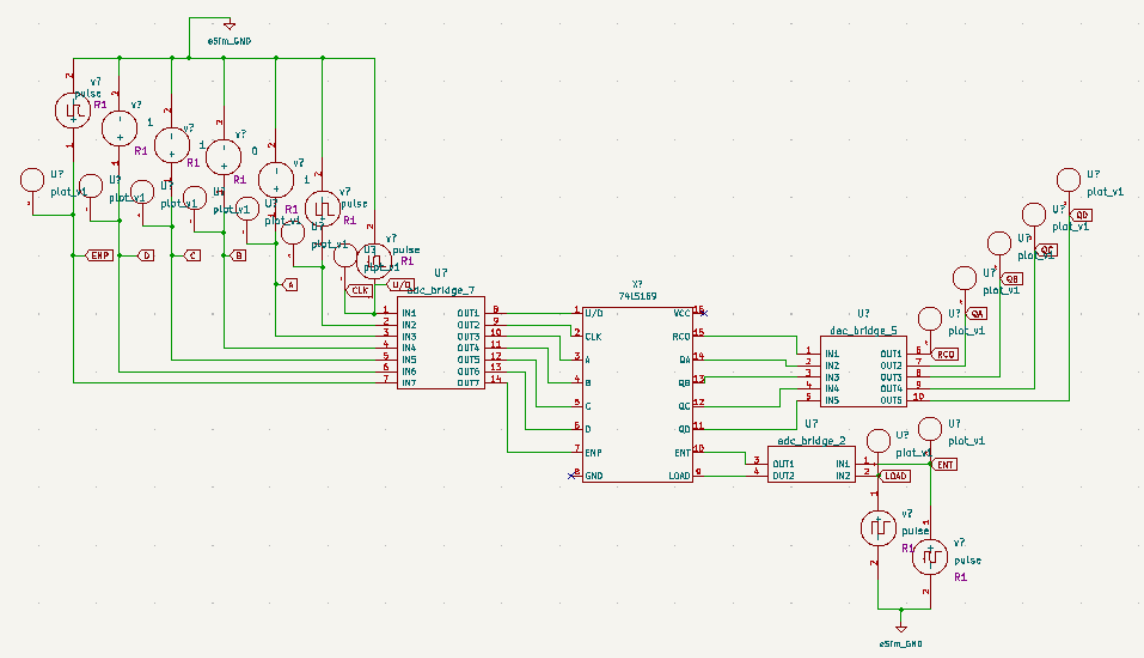


Figure 6.3: Test Circuit Schematic Diagram of SN74LS169

6.7 Analysis details

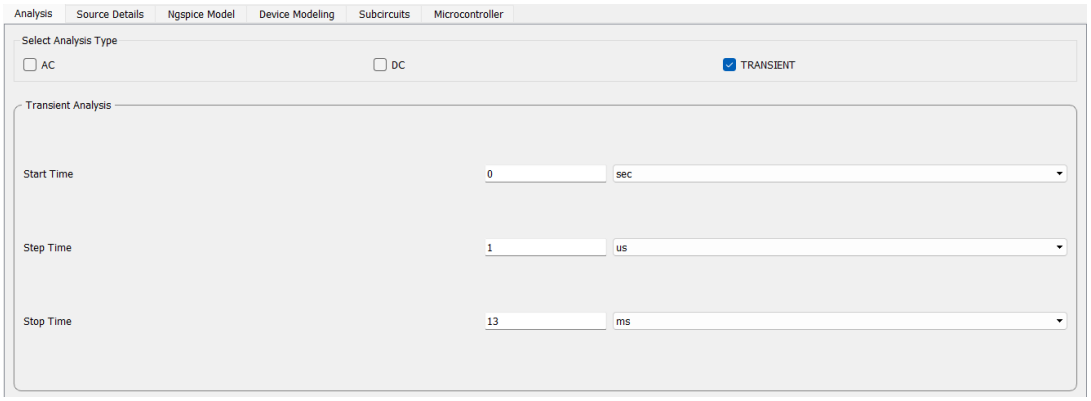


Figure 6.4: Analysis details of SN74LS169

6.8 Source Details

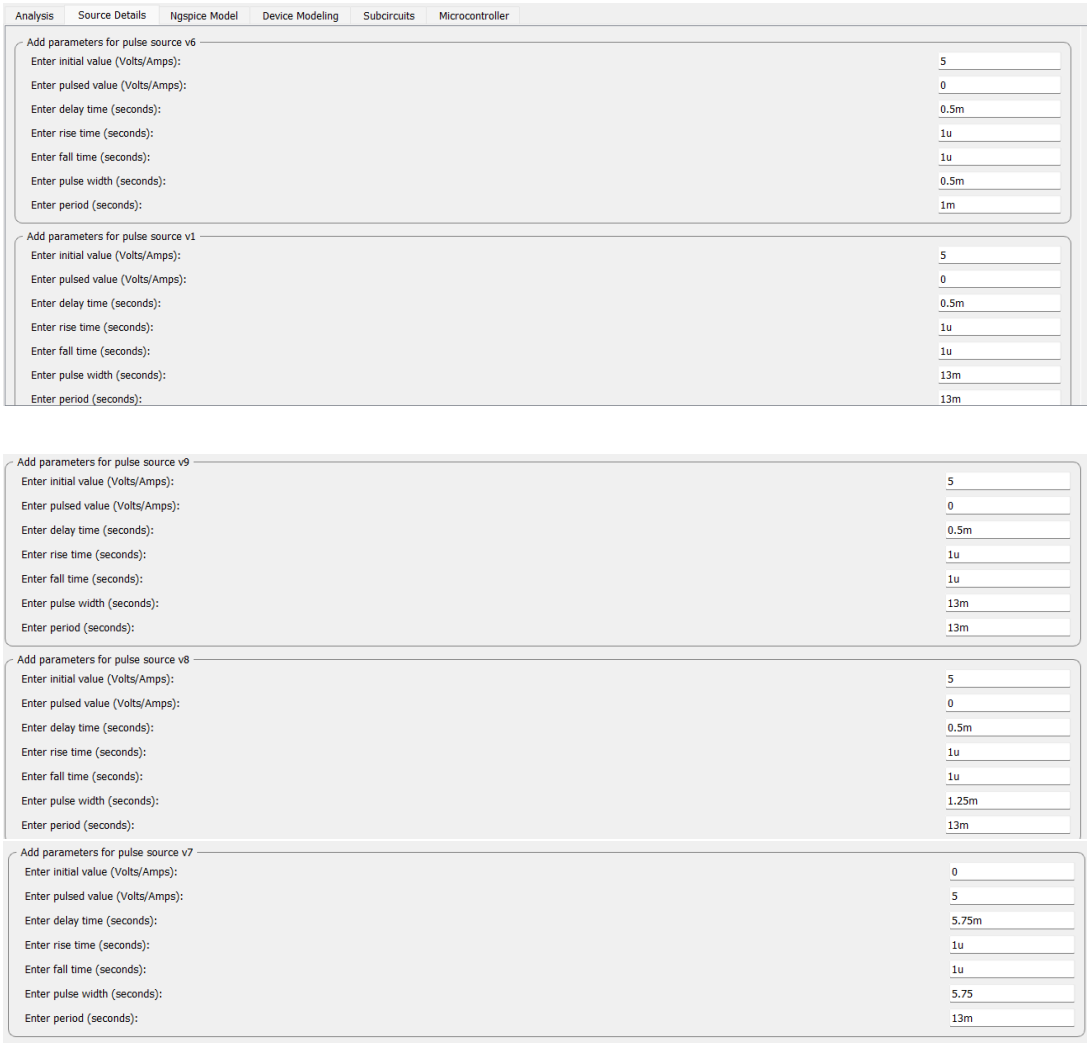


Figure 6.5: Source Details of SN74LS169

6.9 Input Plots

The parallel input bits are set as **1101**, which corresponds to a decimal value of **13**.

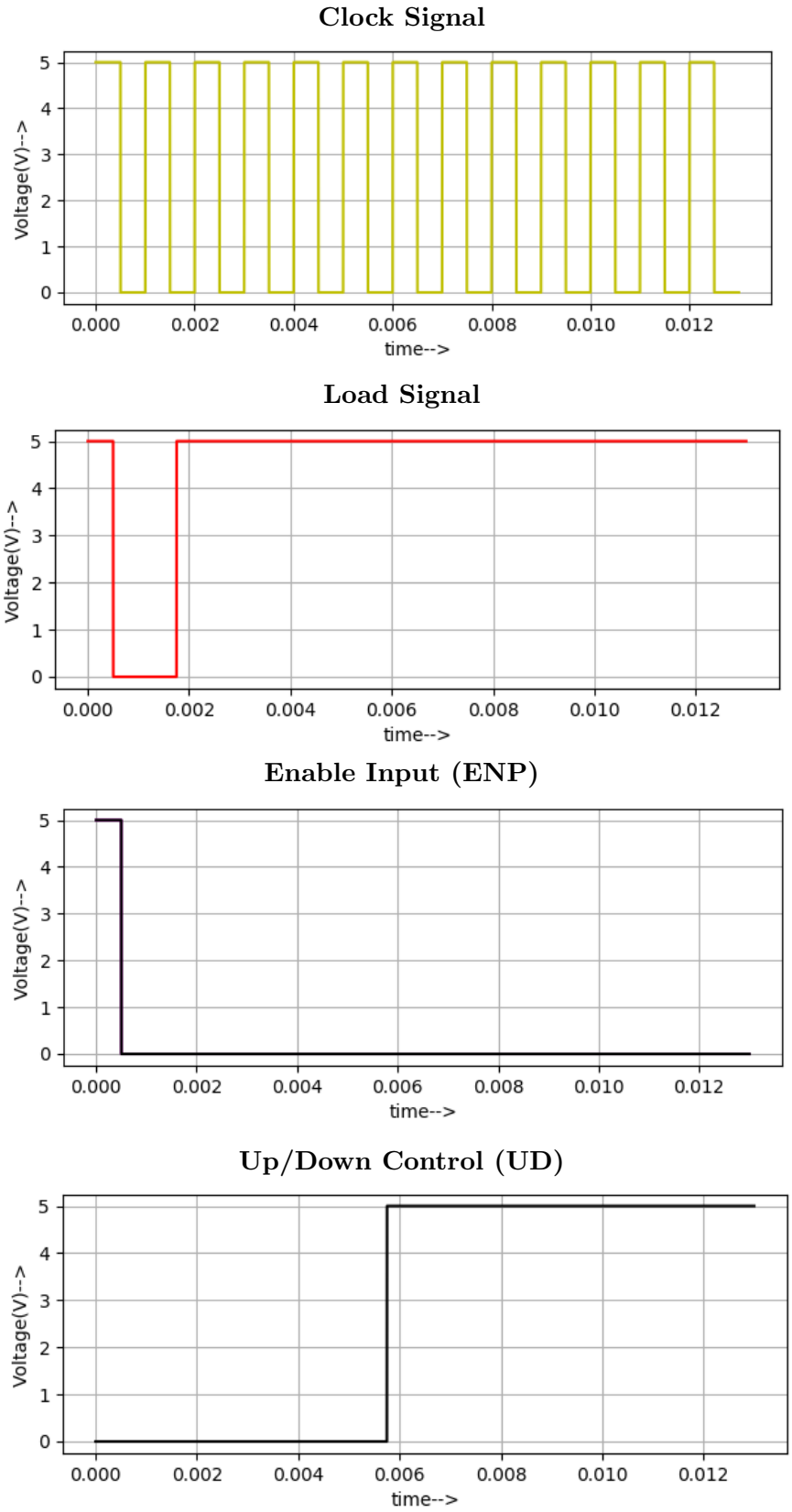
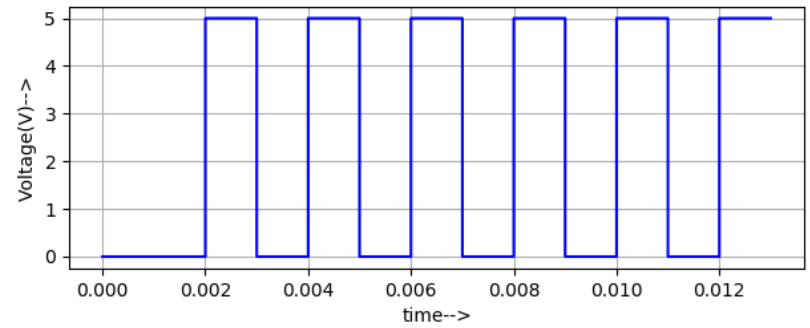


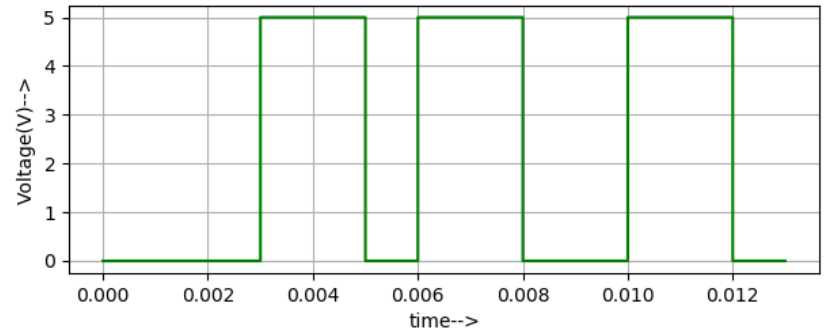
Figure 6.6: Input plots of SN74LS169

6.10 Output Plots

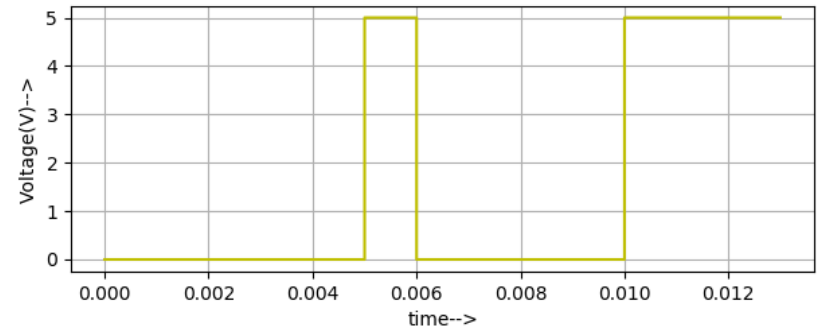
Output QA



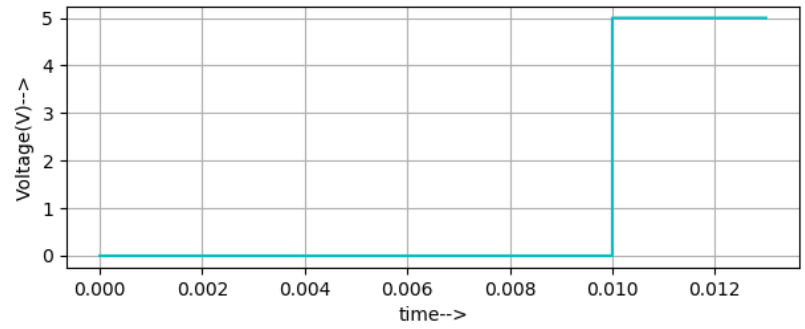
Output QB



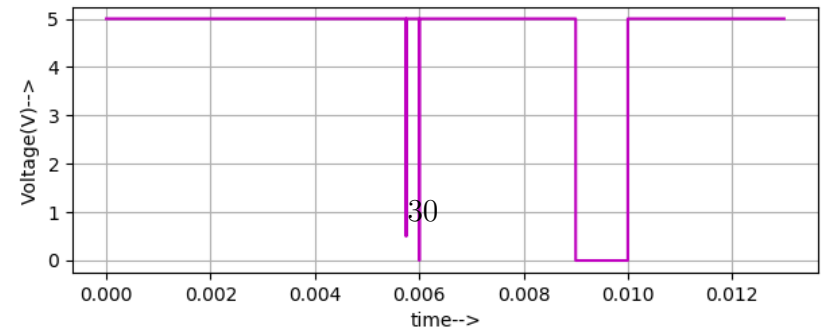
Output QC



Output QD



Ripple Carry Output (RCO)



Chapter 7

SN74HC157

7.1 General Description

Quad 2-to-1 Multiplexer

The SN74HC157 is a quad 2-to-1 multiplexer fabricated using High-Speed CMOS (HC) technology. It is designed to select one of two input signals for each of the four channels and route the selected inputs to the corresponding outputs based on a common select control signal.

The device consists of four independent multiplexers, each capable of selecting between two data inputs. A single select line determines which set of inputs is transferred to the outputs, making the SN74HC157 useful in applications requiring data routing, signal selection, and bus multiplexing.

An active-low enable input is provided to control the overall operation of the device. When the enable input is asserted, the selected data inputs are passed to the outputs. When disabled, the outputs are forced to a known low state. The SN74HC157 offers low power consumption, high noise immunity, and compatibility with standard CMOS and TTL logic levels, making it suitable for modern digital systems.

7.2 Key Features

The key features of SN74HC157 include:

- **Quad 2-to-1 Multiplexer:** Provides four independent 2-to-1 multiplexing channels in a single package.
- **Common Select Input:** A single select control line simultaneously controls all four multiplexers.
- **Active-Low Enable Input:** Allows enabling or disabling of the entire device operation.
- **High-Speed CMOS Technology:** Fabricated using HC CMOS technology for low power consumption and high noise immunity.
- **TTL Compatible Inputs:** Accepts standard TTL logic levels, enabling easy interfacing with TTL-based devices.

- **Wide Operating Voltage Range:** Supports operation over a wide voltage range, enhancing design flexibility.

7.3 Application

The various applications of SN74HC157 are:

- **Data Selection and Routing:** Used to select and route one of two data sources to a common output line in digital systems.
- **Bus Multiplexing:** Employed in bus-oriented architectures to multiplex multiple data lines using a single select control signal.
- **Microprocessor and Microcontroller Systems:** Used to switch between different data paths or peripheral inputs in processor-based systems.
- **Signal Switching Applications:** Applied in digital switching circuits where controlled selection between multiple input signals is required.
- **Control and Automation Systems:** Utilized in control logic and automation circuits for conditional data transfer and signal management.

7.4 Pin Diagram

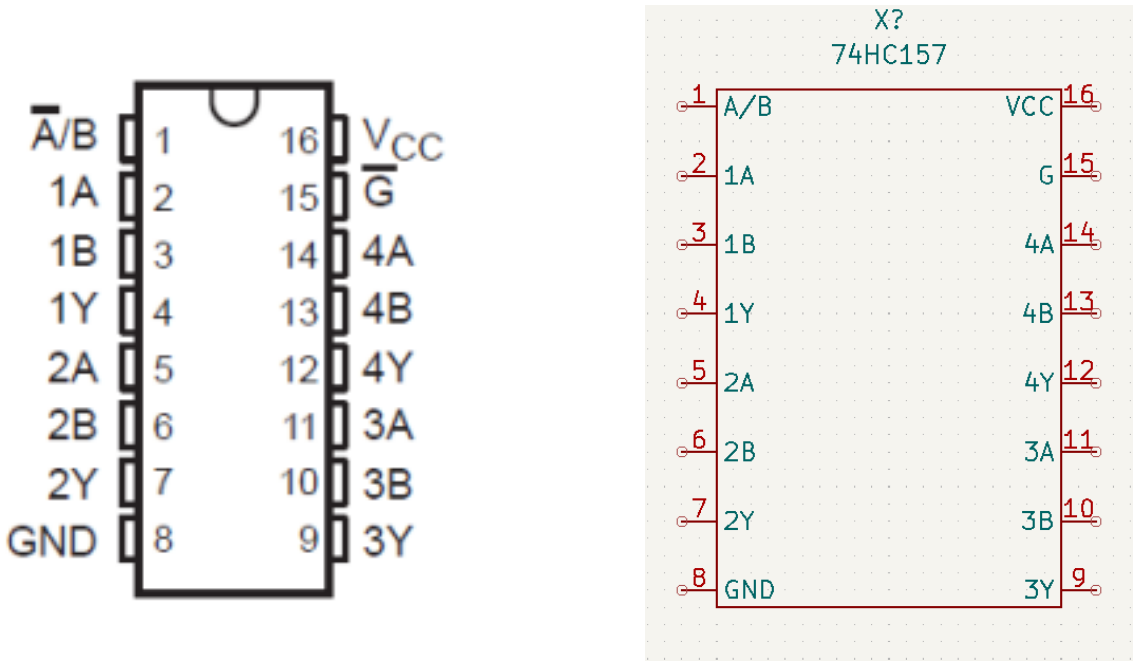


Figure 7.1: Pin diagram of SN74HC157

7.5 Subcircuit Schematic Diagram

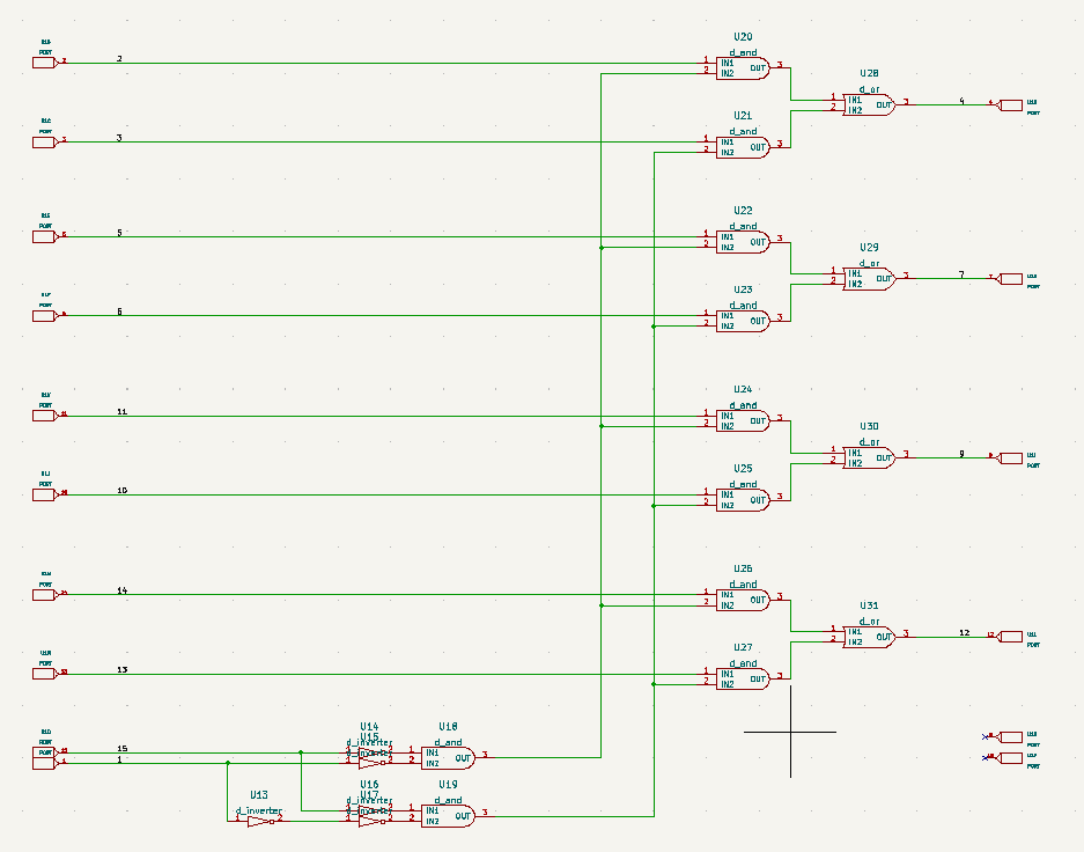


Figure 7.2: Subcircuit Schematic Diagram of SN74HC157

7.6 Test Circuit Schematic Diagram

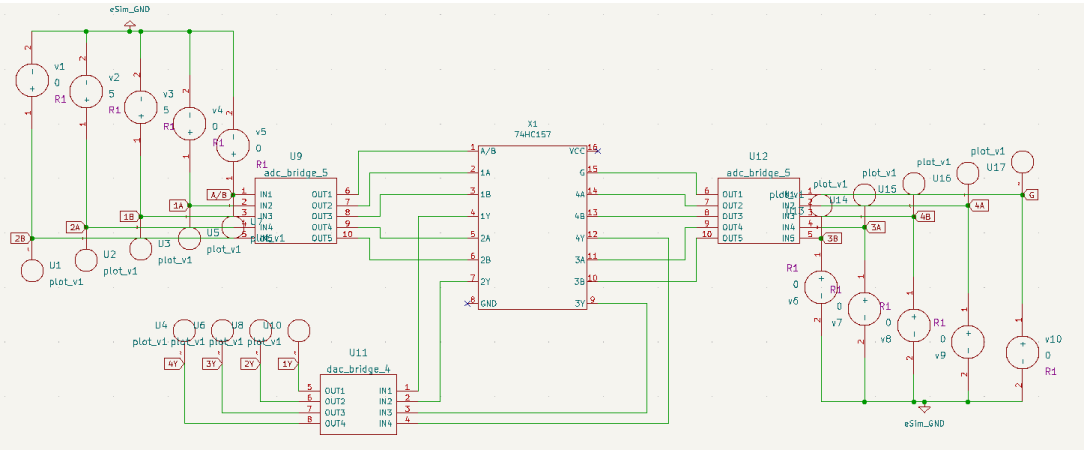


Figure 7.3: Test Circuit Schematic Diagram of SN74HC157

7.7 Analysis details

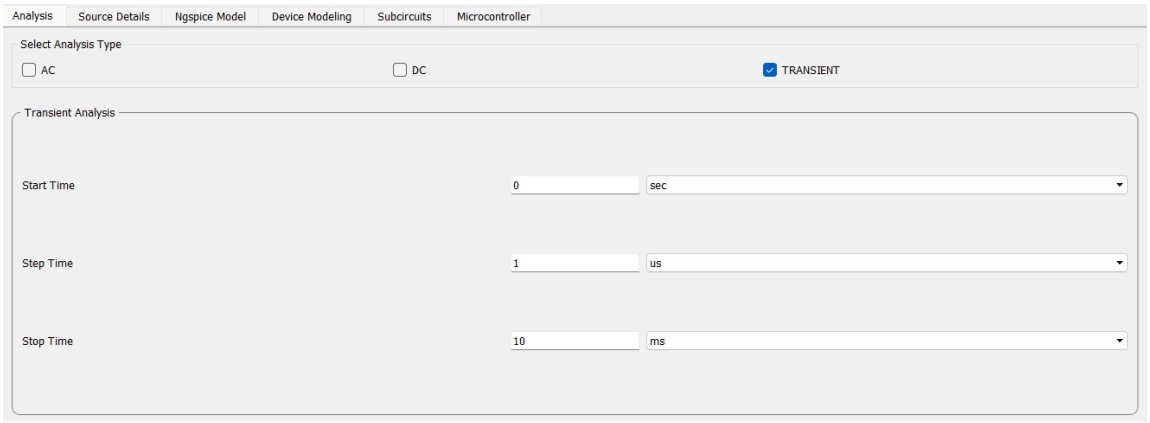


Figure 7.4: Analysis details of SN74HC157

7.8 Source details

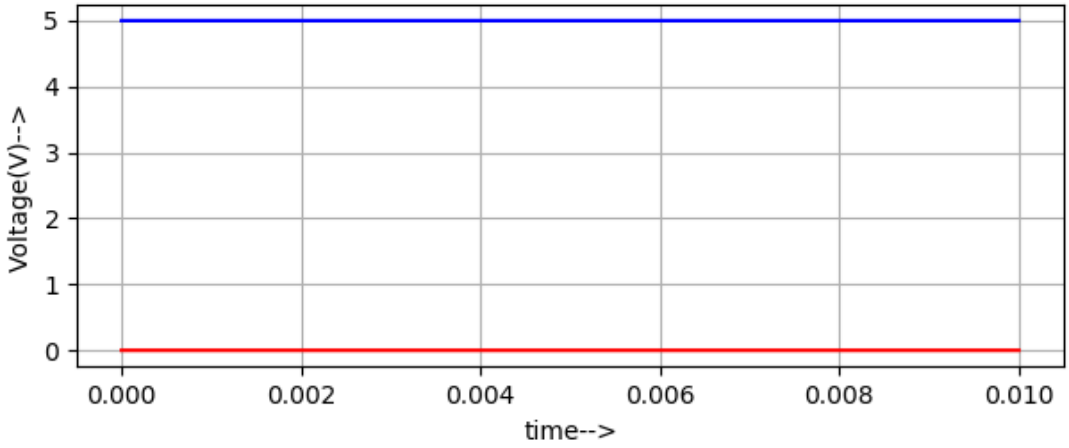
DC source values for the inputs A/B, G, 1A,1B,2A,2B,3A,3B,4A and 4B given based on this function table:

INPUTS(1)				OUTPUT
$\overline{G}$	SELECT	DATA		
	$\overline{A}$/B	A	B	Y
H	X	X	X	L
L	L	L	X	L
L	L	H	X	H
L	H	X	L	L
L	H	X	H	H

(1) H = High Voltage Level, L = Low Voltage Level, X = Do not Care

7.9 Input Plots

Inputs 1A and 1B



Inputs 2A and 2B

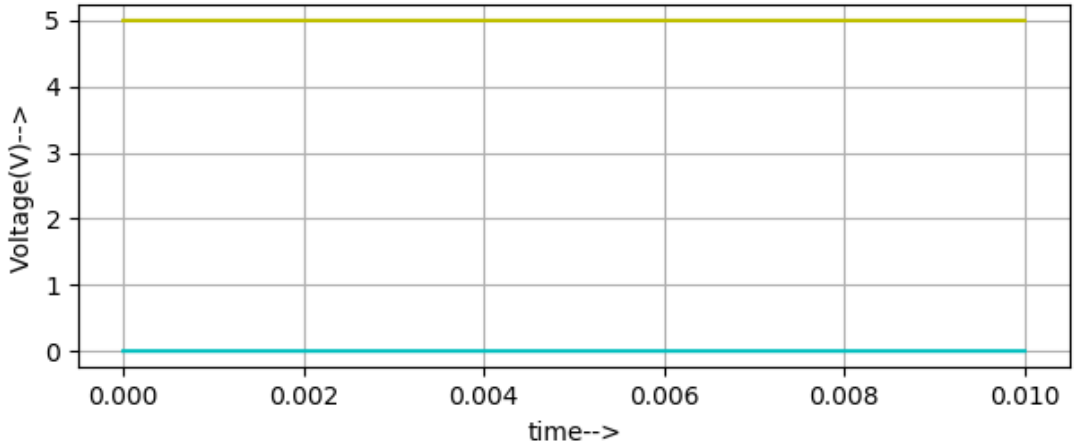


Figure 7.5: Input plots of SN74HC157

7.10 Output Plots

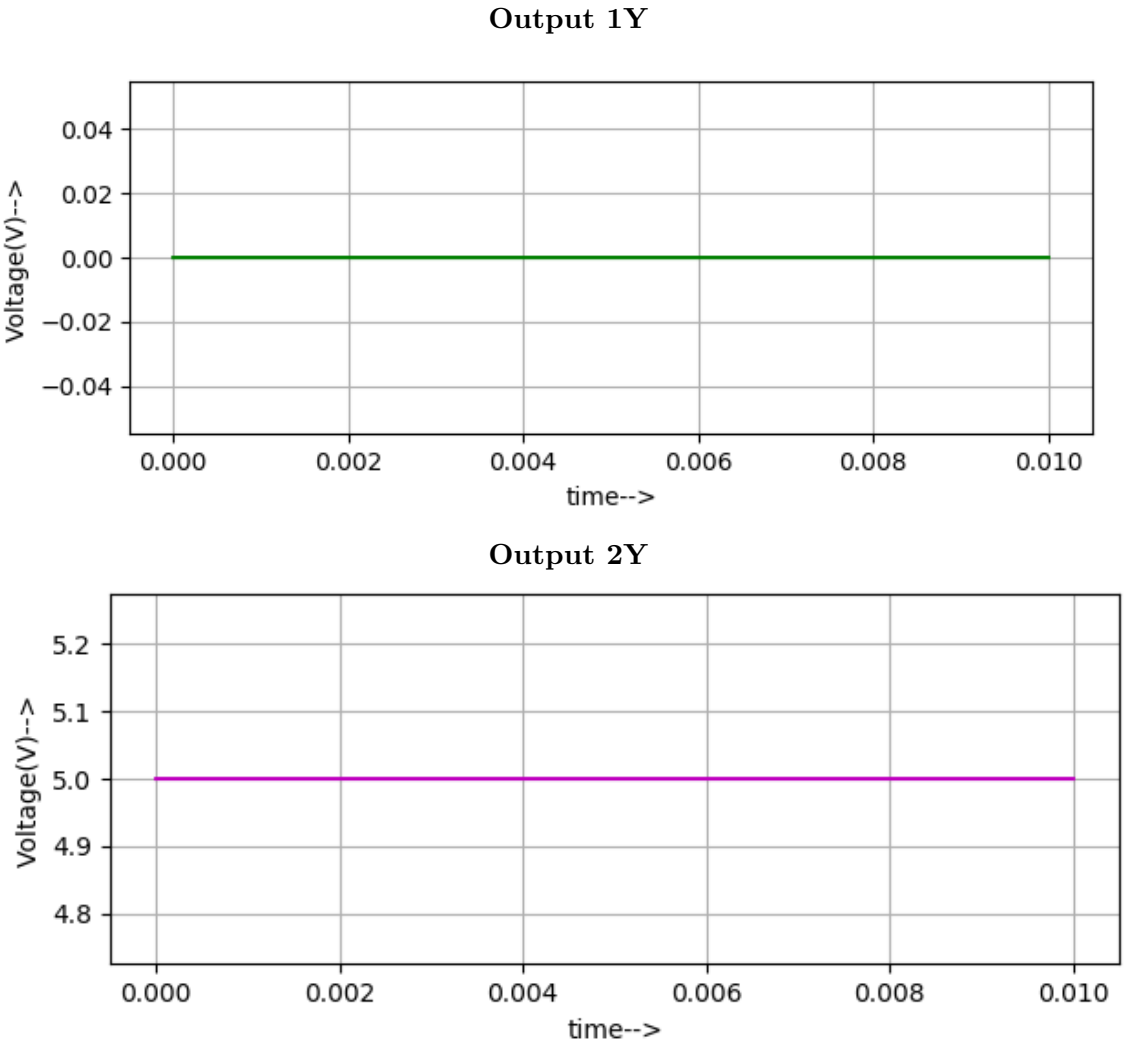


Figure 7.6: Output plots of SN74HC157

Chapter 8

SN74HC42

8.1 General Description

4-Line to 10-Line Decoder

The SN74HC42 is a 4-line to 10-line decoder fabricated using High-Speed CMOS (HC) technology. It is designed to decode a 4-bit binary-coded decimal (BCD) input into one of ten mutually exclusive output lines. Each output corresponds to a decimal digit from 0 to 9, making the device suitable for applications requiring numeric decoding and one-of-ten selection.

The decoder consists of internal inverters and 4-input NAND gates that provide full decoding of the input logic. Valid BCD input combinations activate exactly one output, while all other outputs remain in the HIGH state. For invalid BCD input conditions, all outputs remain HIGH, ensuring safe and predictable operation.

All outputs of the SN74HC42 are active LOW, meaning the selected output is driven LOW while the remaining outputs stay HIGH. The device operates over a wide supply voltage range from 2 V to 6 V and offers low power consumption with high noise immunity. Due to its CMOS construction and TTL-compatible inputs, the SN74HC42 can be easily interfaced with both CMOS and TTL logic families and is widely used in digital decoding and control systems.

8.2 Key Features

The key features of SN74HC42 include:

- **4-Line to 10-Line Decoding:** Decodes a 4-bit BCD input into ten mutually exclusive decimal outputs (0 through 9).
- **Active-Low Outputs:** Only the selected output is driven LOW, while all other outputs remain HIGH.
- **Wide Operating Voltage Range:** Operates with supply voltages from 2 V to 6 V, providing flexibility in system design.
- **Low Power Consumption:** CMOS implementation results in low static power dissipation, with a maximum ICC of approximately 80 µA.
- **High-Speed Operation:** Typical propagation delay of approximately 14 ns at 5 V enables use in high-speed digital applications.
- **TTL-Compatible Inputs:** Accepts standard TTL logic levels, allowing easy interfacing with TTL-based devices.
- **Full Decoding of Input Logic:** Ensures that all outputs remain HIGH for invalid BCD input combinations, preventing unintended output activation.

8.3 Application

The various applications of SN74HC42 are:

- **BCD-to-Decimal Decoding:** Used to decode 4-bit BCD outputs from counters or registers into individual decimal signals for numeric processing.
- **Digital Display Systems:** Commonly employed in digital display circuits to drive decimal-based indicators such as LED displays and numeric selection logic.
- **Counter Output Decoding:** Used in conjunction with BCD counters to decode count values into one-of-ten outputs for control and sequencing applications.
- **Control and Selection Circuits:** Applied in control systems where a single output must be selected from multiple possible outputs based on a binary input condition.
- **Automation and Industrial Control:** Utilized in automation systems for position decoding, event selection, and process control where decimal decoding is required.

8.4 Pin Diagram

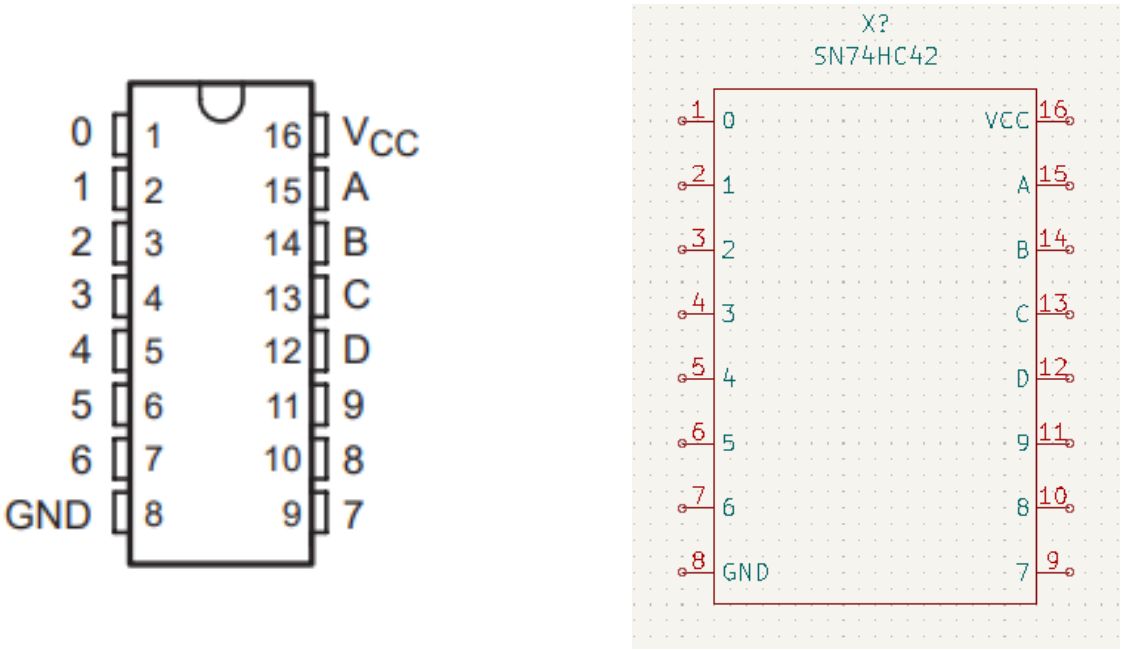


Figure 8.1: Pin diagram of SN74HC42

8.5 Subcircuit Schematic Diagram

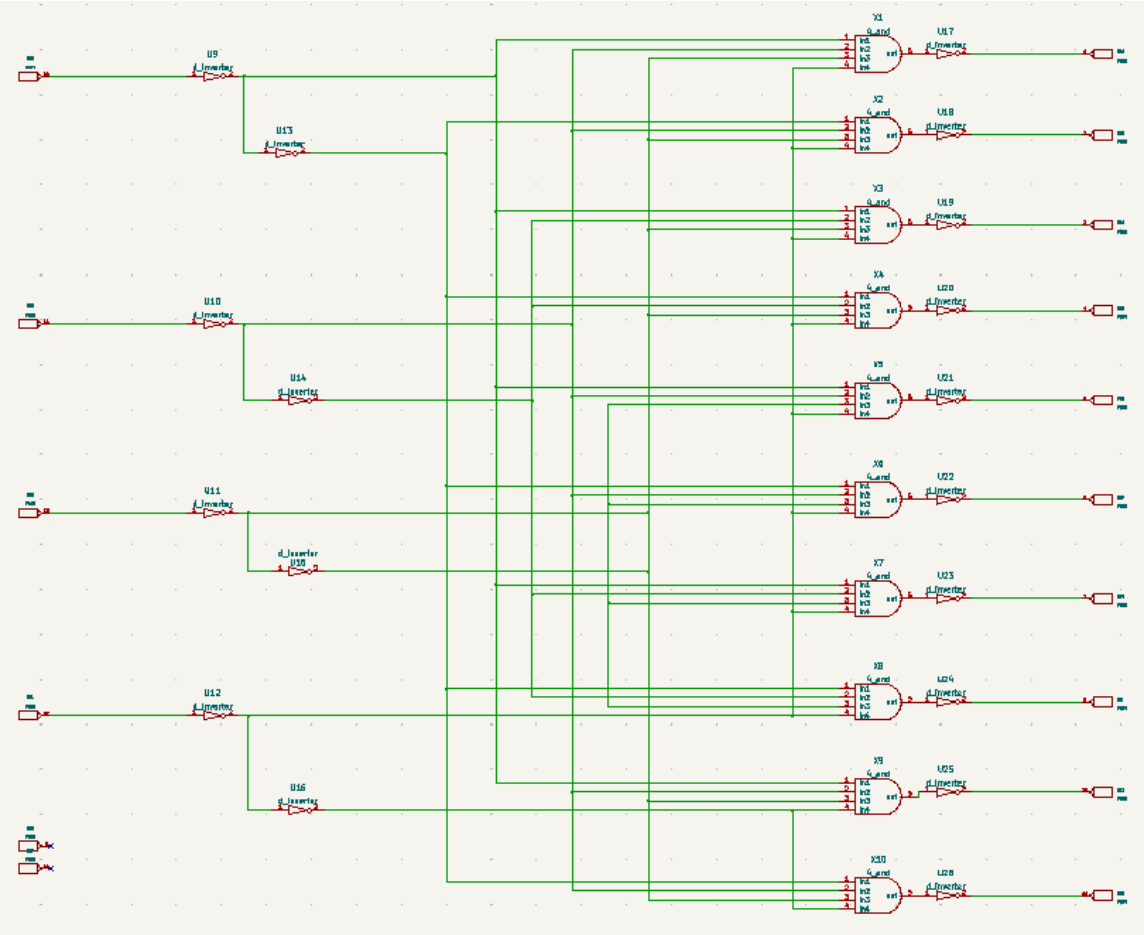


Figure 8.2: Subcircuit Schematic Diagram of SN74HC42

8.6 Test Circuit Schematic Diagram

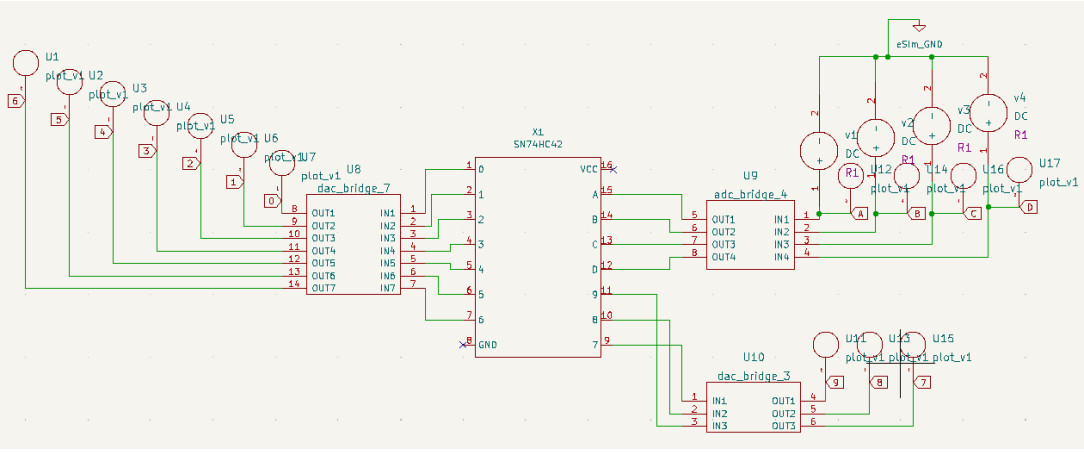


Figure 8.3: Test Circuit Schematic Diagram of SN74HC42

8.7 Analysis details

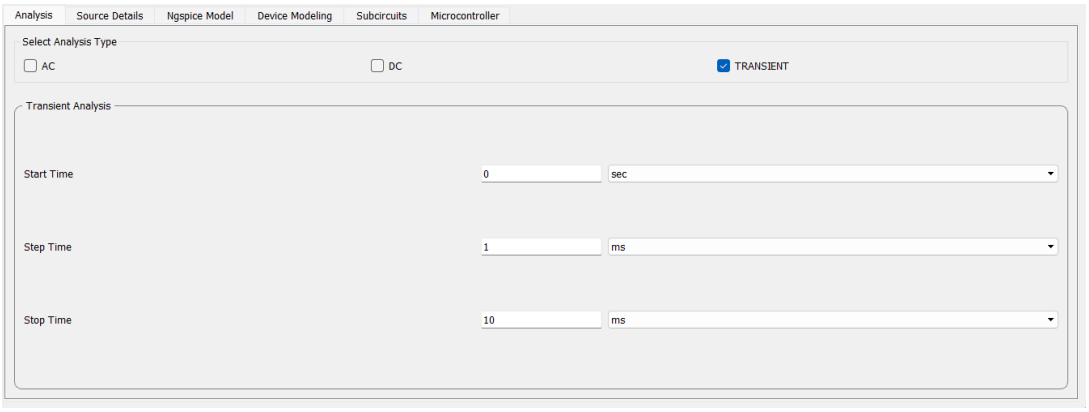


Figure 8.4: Analysis details of SN74HC42

8.8 Source Details

Figure 8.5: Source details of SN74HC42

8.9 Input Plots

The input conditions applied are as follows: A = 0, B = 0, C = 0 and D = 1.

8.10 Output Plots

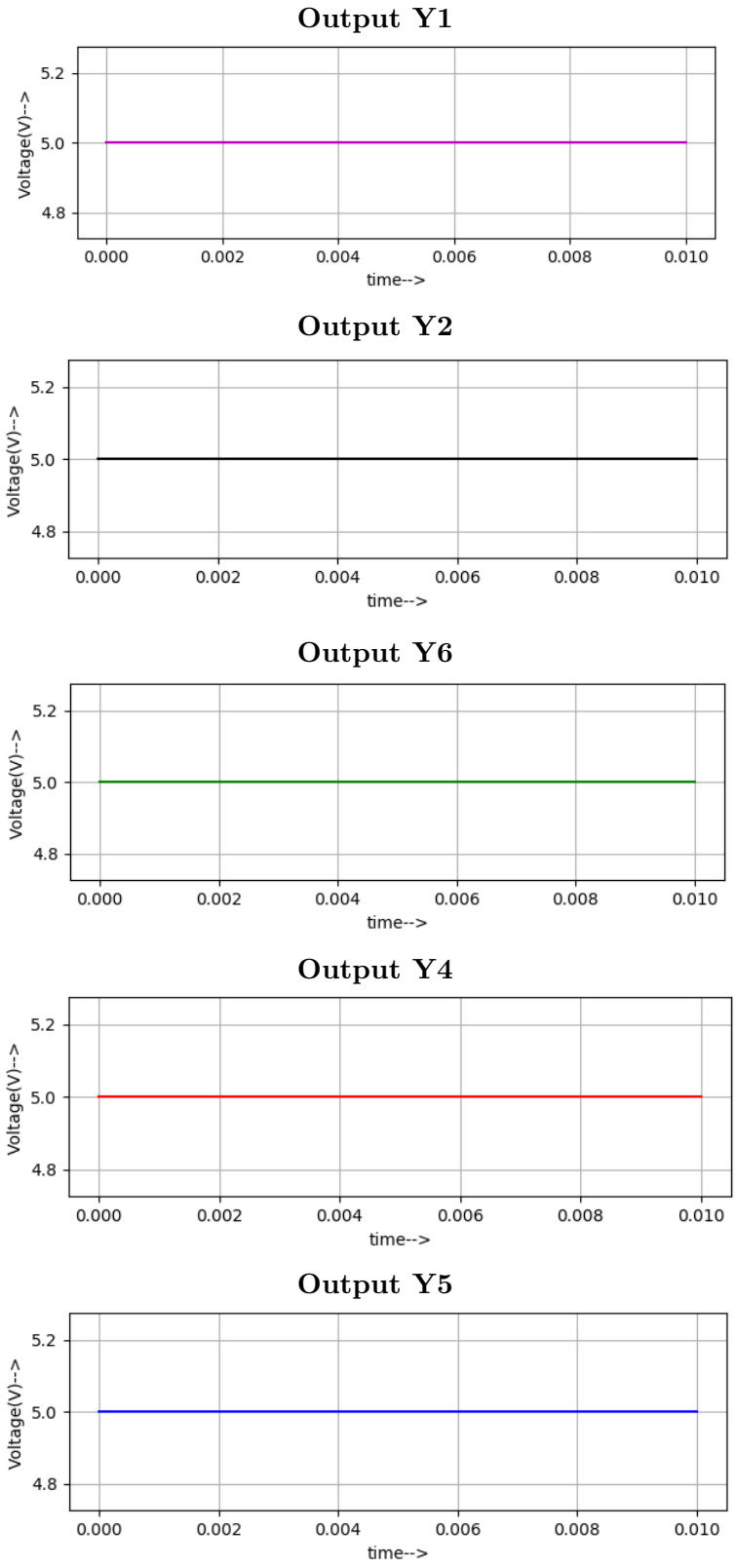


Figure 8.6: Output plots of SN74HC42

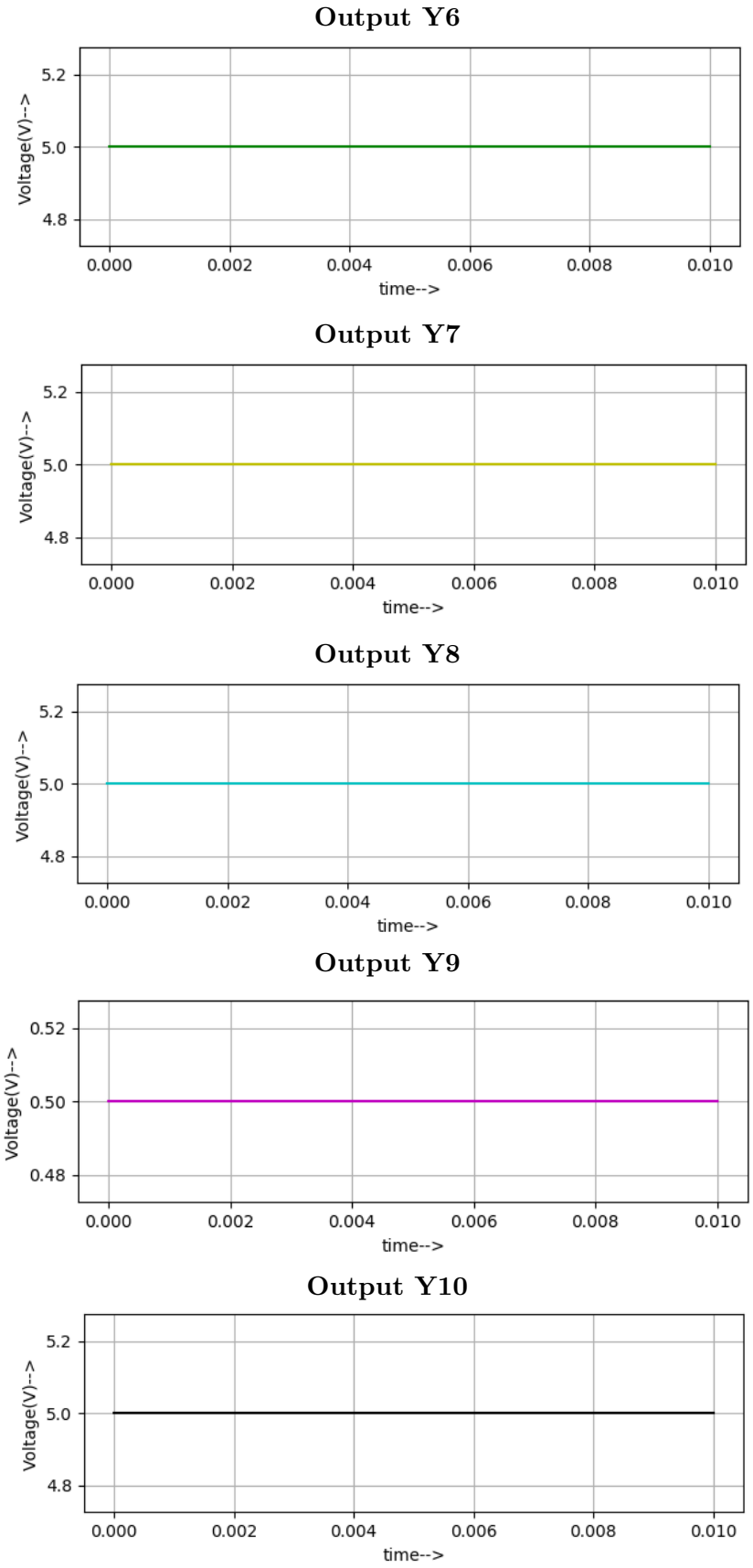


Figure 8.7: Output plots of SN74HC42

Chapter 9

SN74HC541

9.1 General Description

Octal Buffer/Line Driver with 3-State Outputs

The SN74HC541 is an octal buffer and line driver fabricated using High-Speed CMOS (HC) technology. It is designed to provide high-current drive capability and signal buffering for digital systems while allowing multiple devices to share a common data bus through its 3-state output feature.

The device consists of eight non-inverting buffer circuits, each capable of driving heavy capacitive loads and long transmission lines. Two independent active-low output enable inputs are provided to control the 3-state outputs. When both enable inputs are asserted, data applied at the inputs is transferred to the corresponding outputs. When either enable input is deasserted, the outputs are placed in a high-impedance state.

The SN74HC541 offers low power consumption, high noise immunity, and fast switching characteristics. Its TTL-compatible inputs and CMOS output structure make it suitable for interfacing between different logic families and for use in bus-oriented and high-speed digital applications.

9.2 Key Features

The key features of SN74HC541 include:

- **Octal Buffer/Line Driver:** Provides eight non-inverting buffer channels in a single package.
- **3-State Outputs:** Enables multiple devices to share a common bus without output contention.
- **Dual Active-Low Output Enables:** Two independent enable inputs provide flexible control of the output state.
- **High-Speed CMOS Technology:** Fabricated using HC CMOS for low power consumption and fast switching performance.
- **TTL-Compatible Inputs:** Accepts standard TTL logic levels for easy interfacing with TTL-based devices.

- **High Drive Capability:** Capable of driving high fan-out loads and long interconnects.

9.3 Application

The various applications of SN74HC541 are:

- **Bus Buffering:** Used to buffer and isolate data buses in microprocessor and microcontroller-based systems.
- **Line Driving Applications:** Employed to drive long transmission lines or heavily loaded signals without signal degradation.
- **Memory and I/O Interfacing:** Used to interface memory devices and I/O peripherals with processors.
- **Data Isolation:** Provides isolation between different sections of a digital system to improve reliability and noise immunity.
- **Control and Automation Systems:** Applied in control circuits where controlled enabling and disabling of signal paths is required.

9.4 Pin Diagram

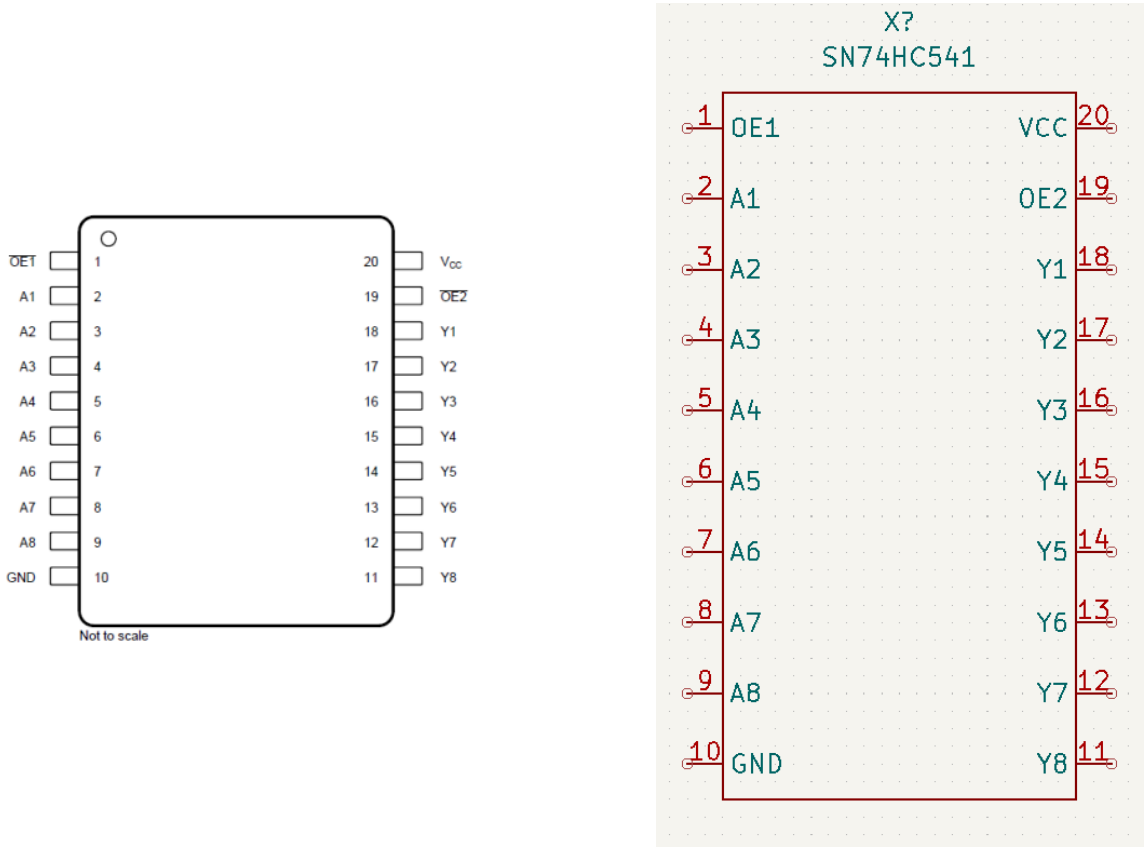


Figure 9.1: Pin diagram of SN74HC541

9.5 Subcircuit Schematic Diagram

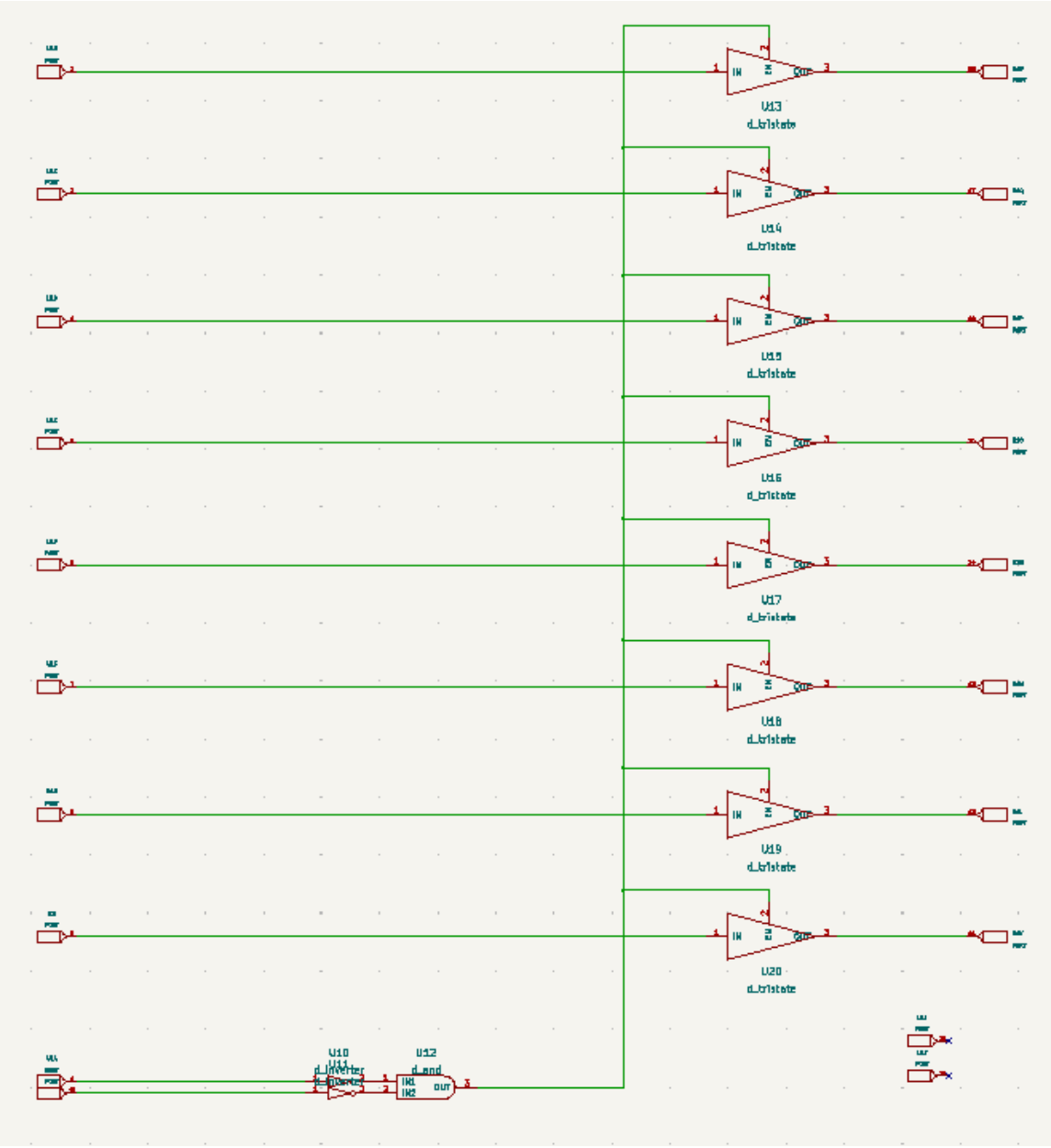


Figure 9.2: Subcircuit Schematic Diagram of SN74HC541

9.6 Test Circuit Schematic Diagram

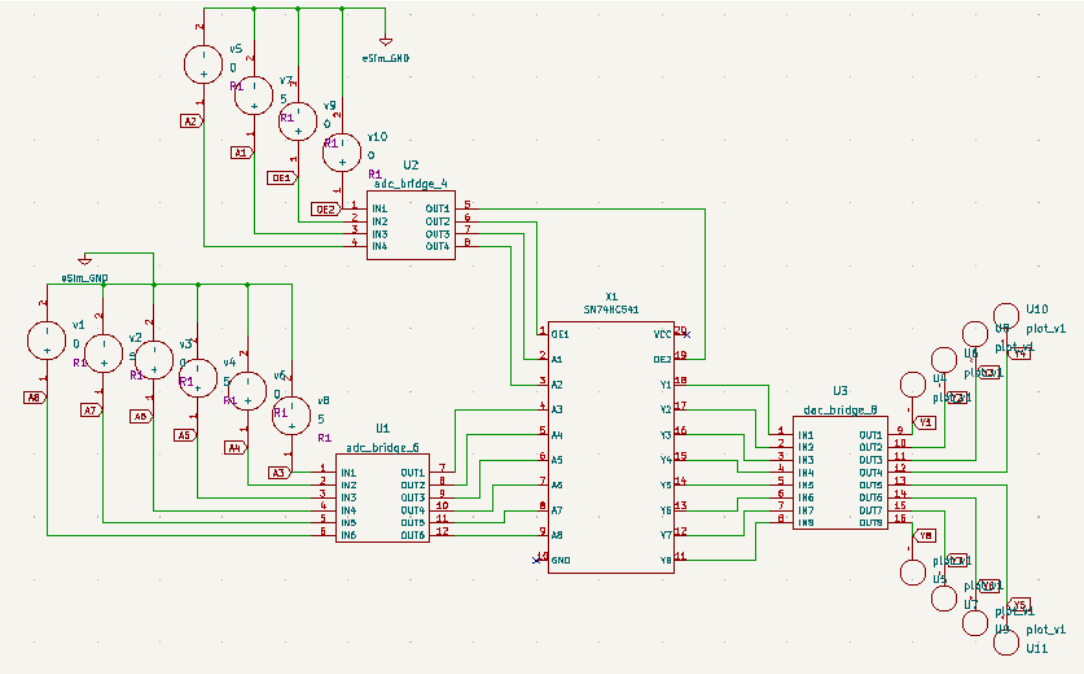


Figure 9.3: Test Circuit Schematic Diagram of SN74HC541

9.7 Analysis details

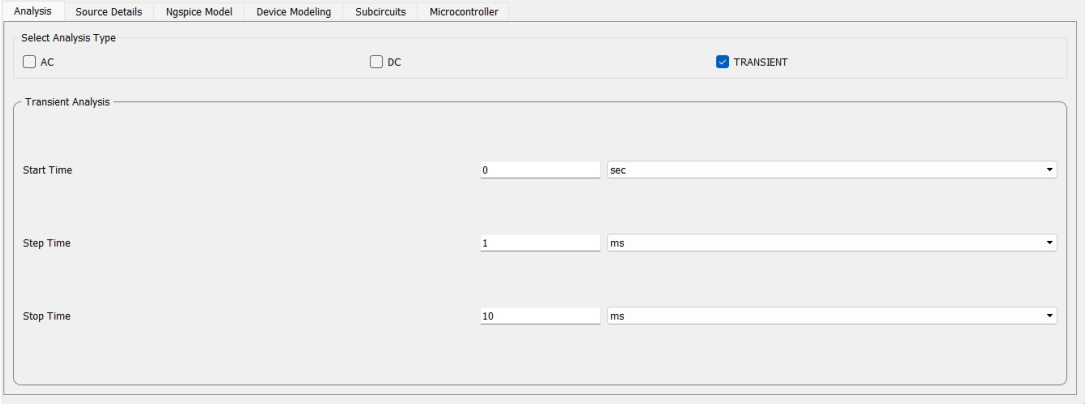


Figure 9.4: Analysis details of SN74HC541

9.8 Source details

A1=5V, A2=0V, A3=5V, A4=0V, A5=5V, A6=0V, A7=5V, A8=0V, OE1=0, OE2=0

9.9 Input Plots

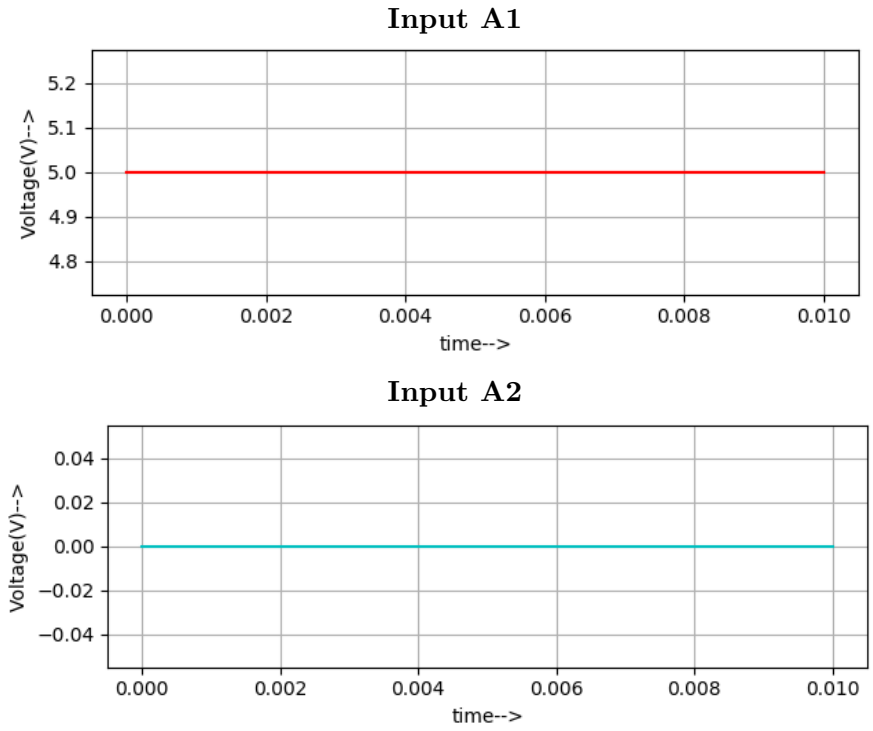


Figure 9.5: Input plots of SN74HC541

9.10 Output Plots

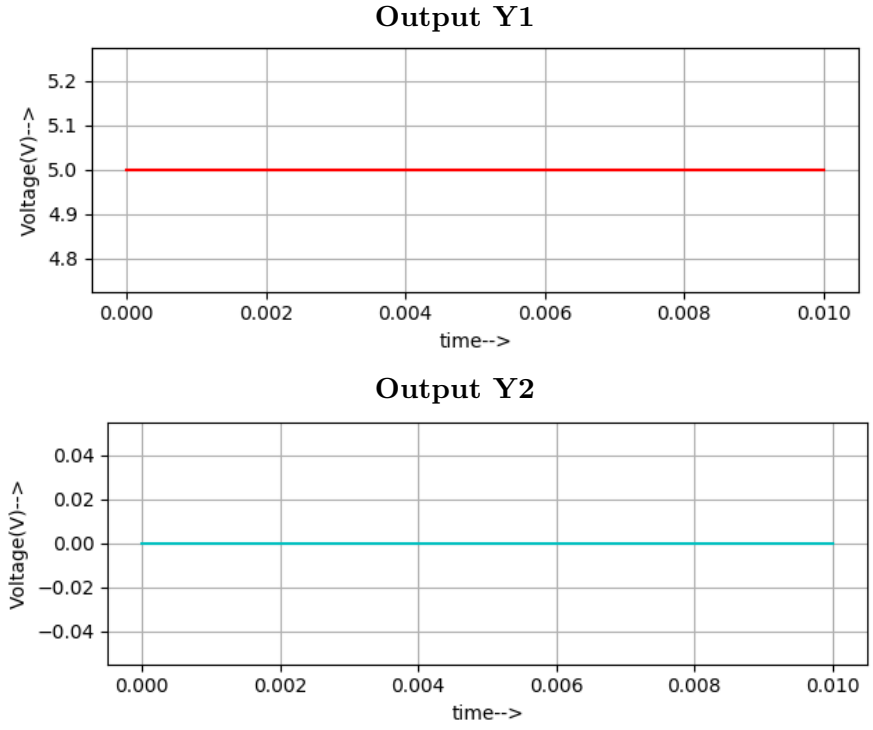


Figure 9.6: Output plots of SN74HC541

Chapter 10

MC14532B

10.1 General Description

8-Bit Priority Encoder

The MC14532B is an 8-bit priority encoder fabricated using complementary MOS (CMOS) technology. The primary function of a priority encoder is to generate a binary-coded output corresponding to the highest-priority active input. The device accepts eight data inputs (D0 through D7) along with an enable input (Ein).

The MC14532B provides five outputs, consisting of three address outputs (Q0, Q1, and Q2), a group select output (GS), and an enable output (Eout). When multiple inputs are active simultaneously, the encoder assigns priority to the highest-numbered input and generates the corresponding binary address at the output.

The device operates over a wide supply voltage range from 3 V to 18 V and includes diode protection on all inputs. Its CMOS construction ensures low power consumption, high noise immunity, and reliable operation, making the MC14532B suitable for use in digital encoding, control, and interface applications.

10.2 Key Features

The key features of MC14532B include:

- **8-Bit Priority Encoding:** Encodes the highest-priority active input among eight input lines into a 3-bit binary output.
- **Multiple Output Signals:** Provides three address outputs (Q0–Q2), one group select output (GS), and one enable output (Eout).
- **Wide Supply Voltage Range:** Operates with supply voltages ranging from 3 V to 18 V.
- **CMOS Technology:** Ensures low power consumption and high noise immunity.
- **Input Protection:** Includes diode protection on all inputs to enhance device robustness.
- **TTL Drive Capability:** Capable of driving low-power TTL and Schottky TTL loads.

10.3 Application

The various applications of MC14532B are:

- **Priority Encoding Systems:** Used in digital systems to determine the highest-priority request among multiple input signals.
- **Interrupt Handling Circuits:** Commonly employed in microprocessor-based systems for interrupt prioritization.
- **Data Routing and Selection:** Used in control logic to select one input source from multiple competing signals.
- **Keyboard and Input Encoding:** Applied in keypad and input scanning systems to encode multiple input lines into binary form.
- **Digital Control and Interface Logic:** Used in automation and control systems requiring priority-based decision making.

10.4 Pin Diagram

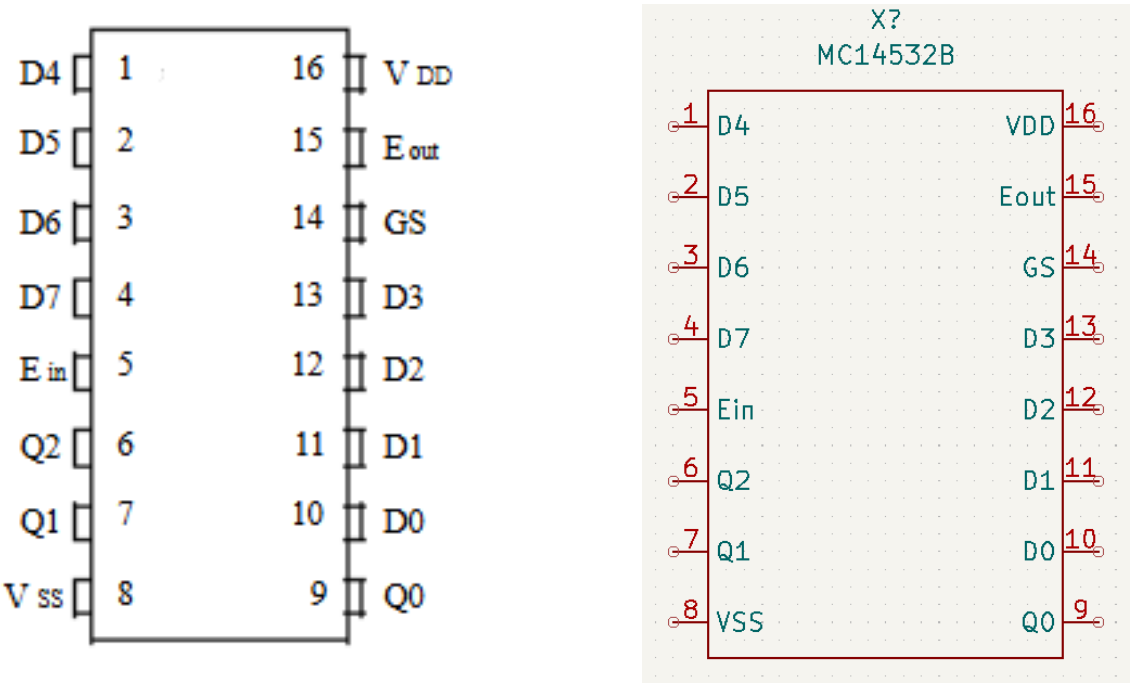


Figure 10.1: Pin diagram of SN74HC541

10.5 Subcircuit Schematic Diagram

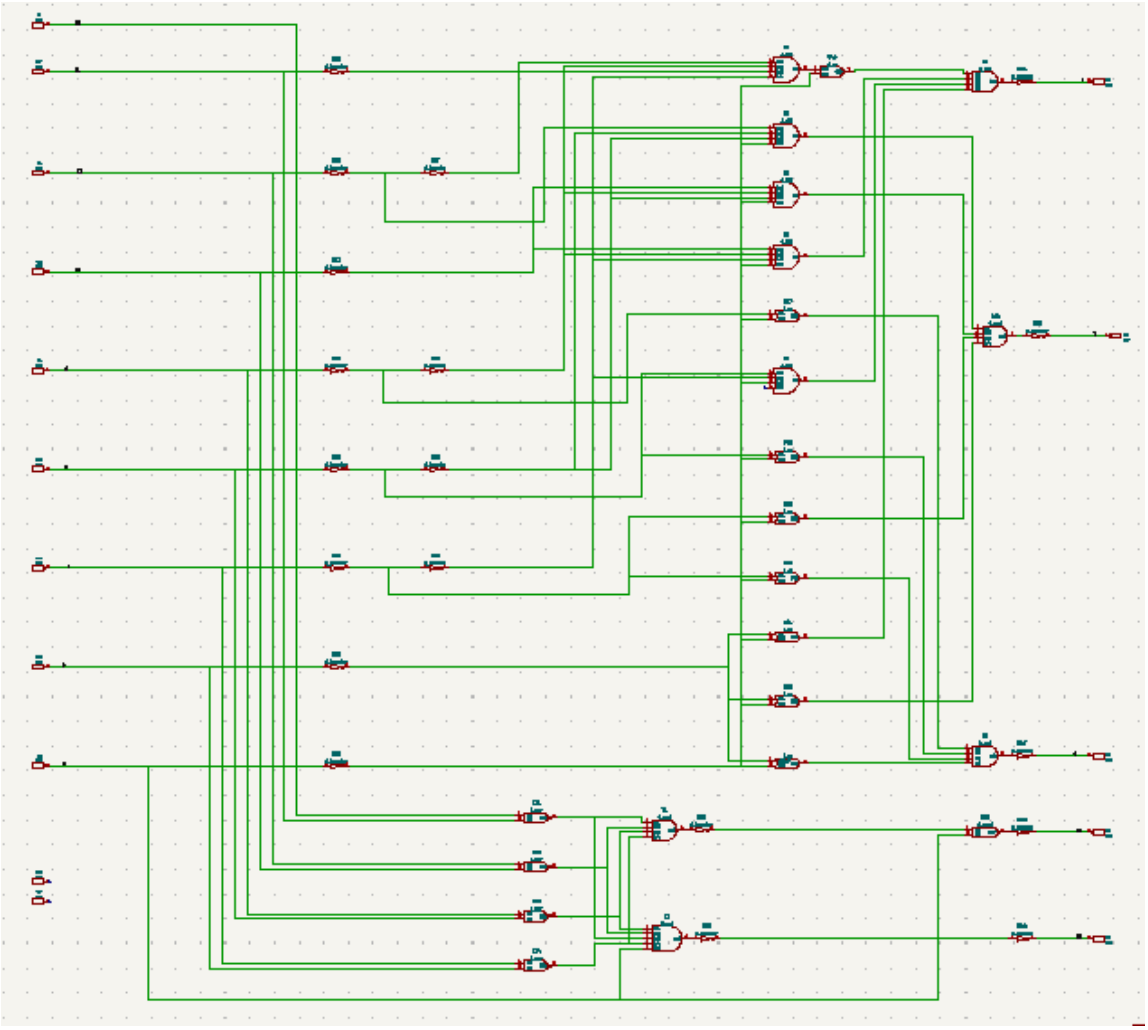


Figure 10.2: Subcircuit Schematic Diagram of MC14532B

10.6 Test Circuit Schematic Diagram

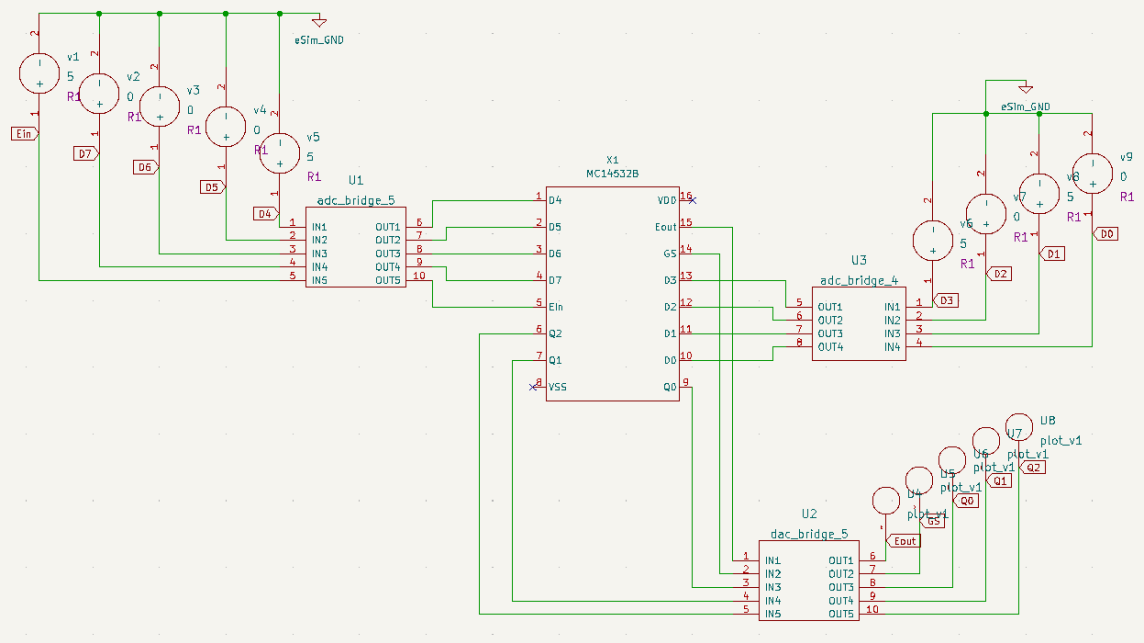


Figure 10.3: Test Circuit Schematic Diagram of MC14532B

10.7 Analysis details

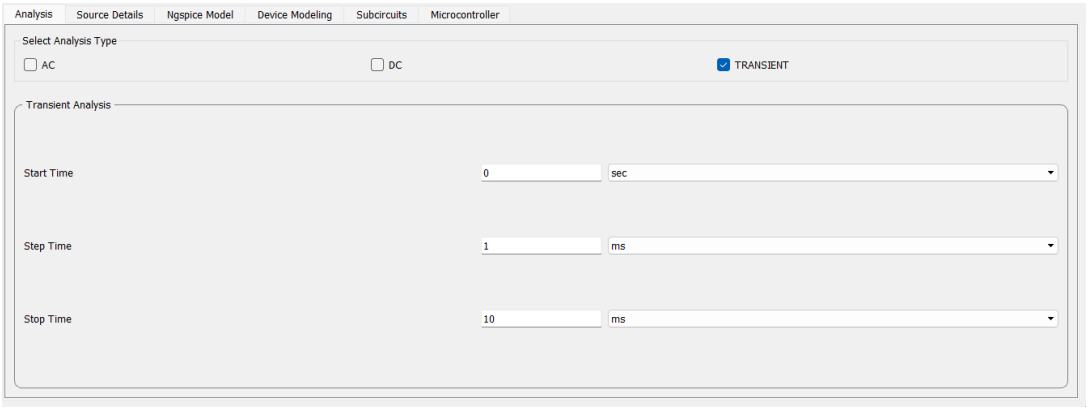


Figure 10.4: Analysis details of MC14532B

10.8 Source details

D7= D6= D5= 0, D4= 5V, Ein=5V

10.9 Input Plots

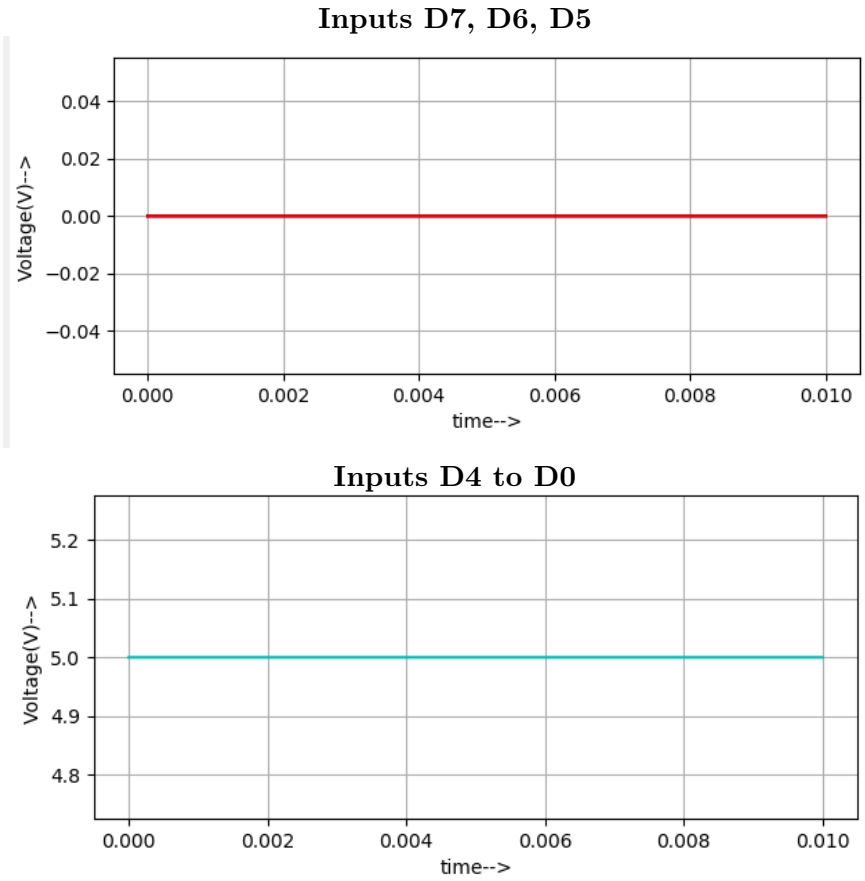


Figure 10.5: Input plots of MC14532B

10.10 Output Plots

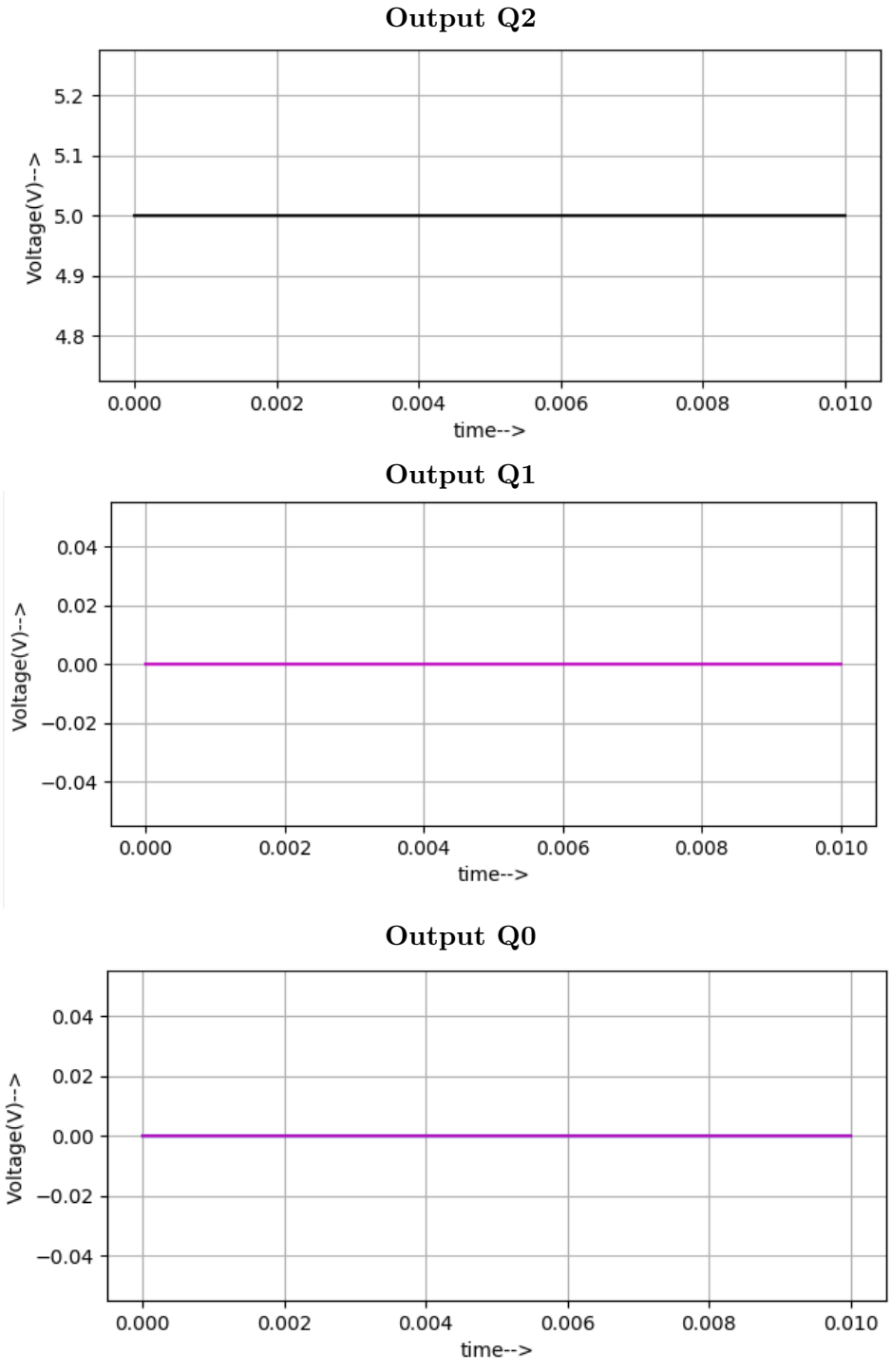


Figure 10.6: Output plots of MC14532B

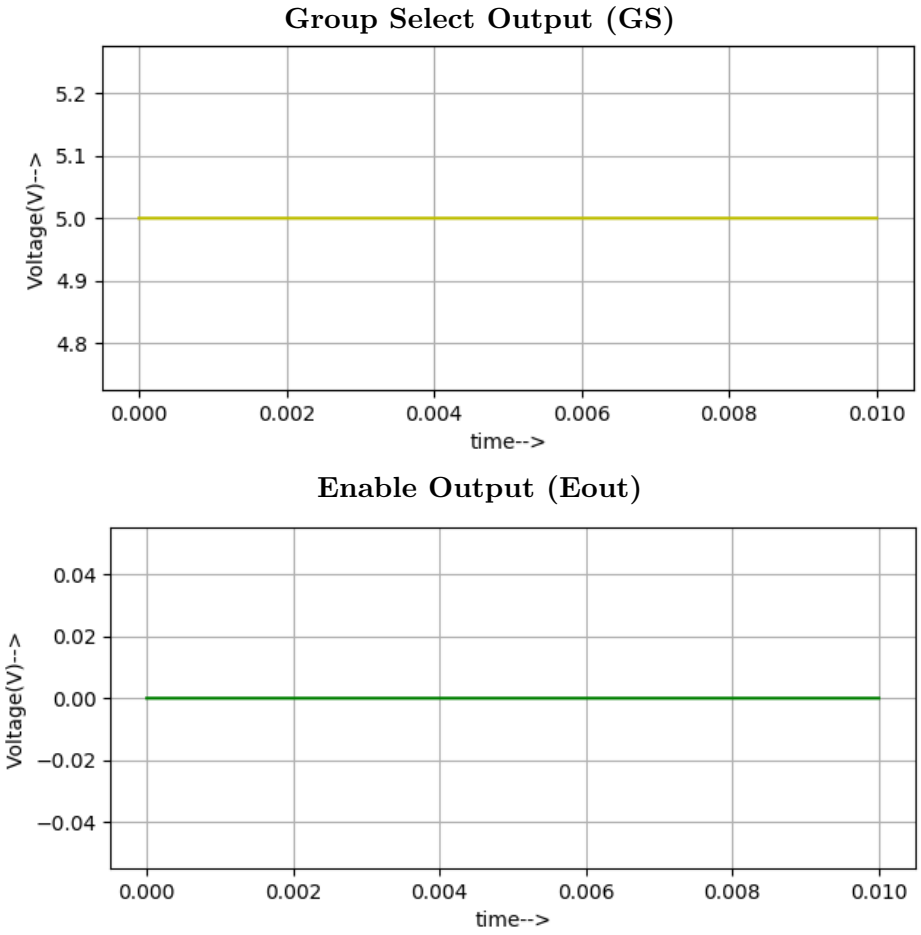


Figure 10.7: Output plots of MC14532B

Chapter 11

74F182

11.1 General Description

Look-Ahead Carry Generator

The 74F182 is a high-speed Look-Ahead Carry Generator designed to improve the speed of binary addition in digital systems. It is fabricated using Fast TTL (F-Series) technology and is commonly used in conjunction with 4-bit binary adders such as the 74LS83 or 74LS283 to implement fast multi-bit arithmetic units.

The primary function of the 74F182 is to generate carry signals in advance based on propagate and generate inputs, thereby eliminating the cumulative delay associated with ripple-carry adders. By computing the carry outputs simultaneously rather than sequentially, the device significantly reduces overall addition time in large-word-length arithmetic circuits.

The IC accepts propagate (P) and generate (G) signals from multiple adder stages and produces intermediate carry outputs as well as group propagate and group generate signals. These outputs allow multiple 74F182 devices to be cascaded efficiently for higher-bit arithmetic operations.

Due to its high-speed operation and efficient carry computation, the 74F182 is widely used in arithmetic logic units (ALUs), processors, and other high-performance digital systems requiring fast addition.

11.2 Key Features

The key features of 74F182 include:

- **Look-Ahead Carry Generation:** Generates carry outputs in advance to reduce propagation delay.
- **High-Speed Operation:** Fabricated using Fast TTL technology for improved switching speed.
- **Supports Multi-Bit Addition:** Designed to work with multiple 4-bit adders to form wide arithmetic units.
- **Group Propagate and Generate Outputs:** Provides group propagate (PG) and group generate (GG) signals for easy cascading.

- **Reduced Carry Delay:** Eliminates ripple-carry delay, significantly improving arithmetic performance.
- **TTL Compatible:** Fully compatible with standard TTL logic levels.

11.3 Application

The various applications of 74F182 are:

- **High-Speed Adders:** Used to implement fast multi-bit adders in digital arithmetic circuits.
- **Arithmetic Logic Units (ALUs):** Commonly employed in ALUs to improve addition and subtraction speed.
- **Microprocessors and CPUs:** Used in processor datapaths to accelerate arithmetic operations.
- **Digital Signal Processing Systems:** Applied in systems where fast arithmetic computation is critical.
- **High-Performance Computing Circuits:** Suitable for any digital system requiring reduced arithmetic latency.

11.4 Pin Diagram

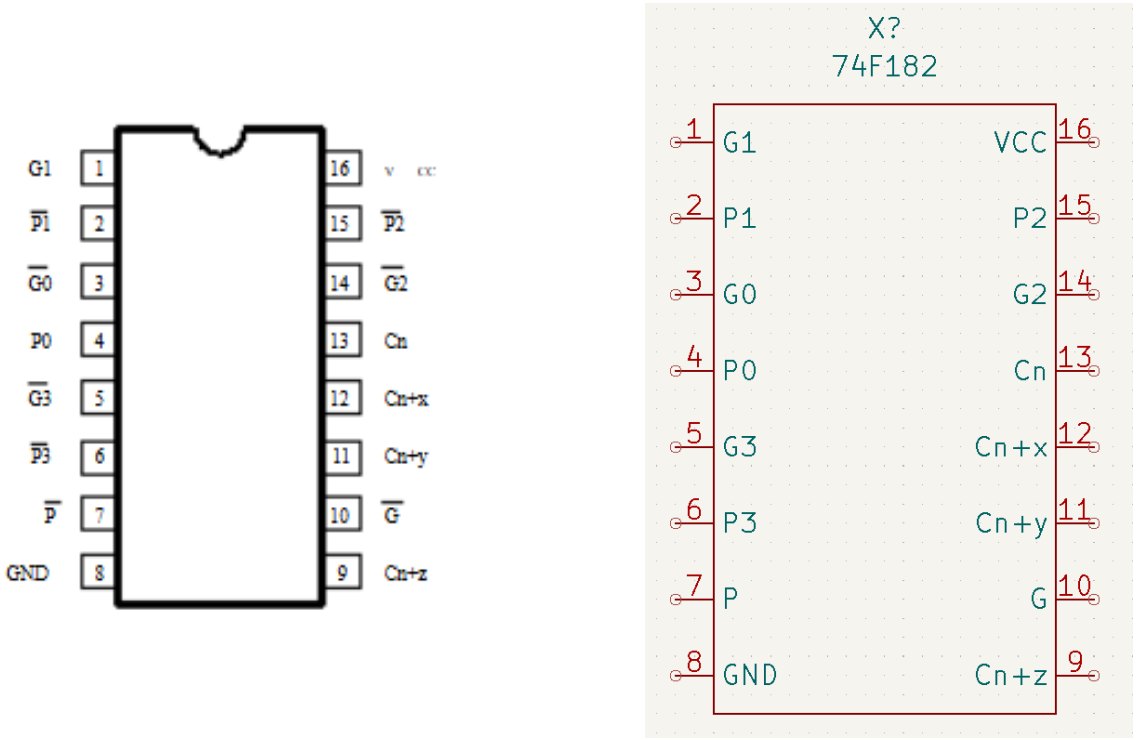


Figure 11.1: Pin diagram of 74F182

11.5 Subcircuit Schematic Diagram

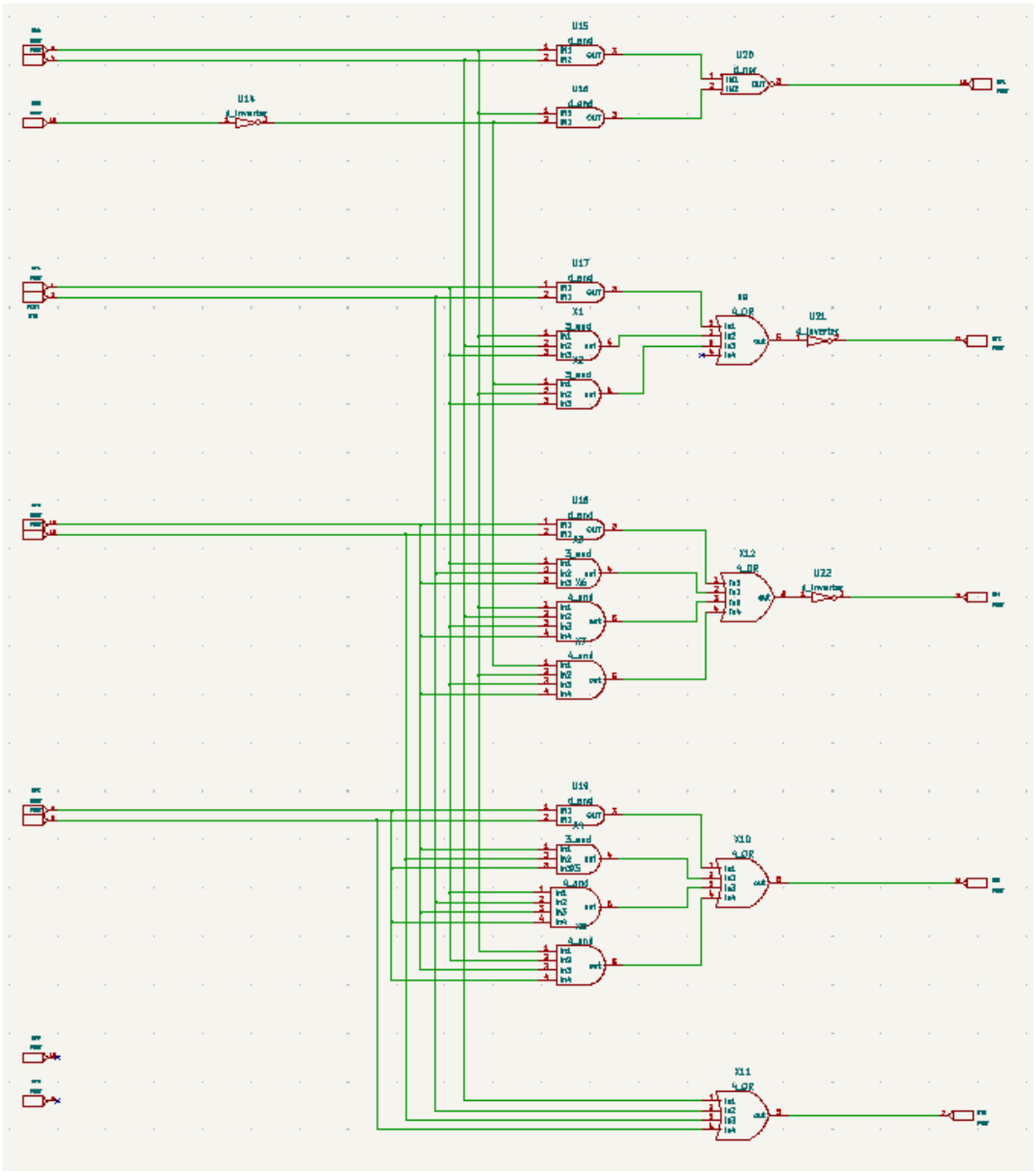


Figure 11.2: Subcircuit Schematic Diagram of 74F182

11.6 Test Circuit Schematic Diagram

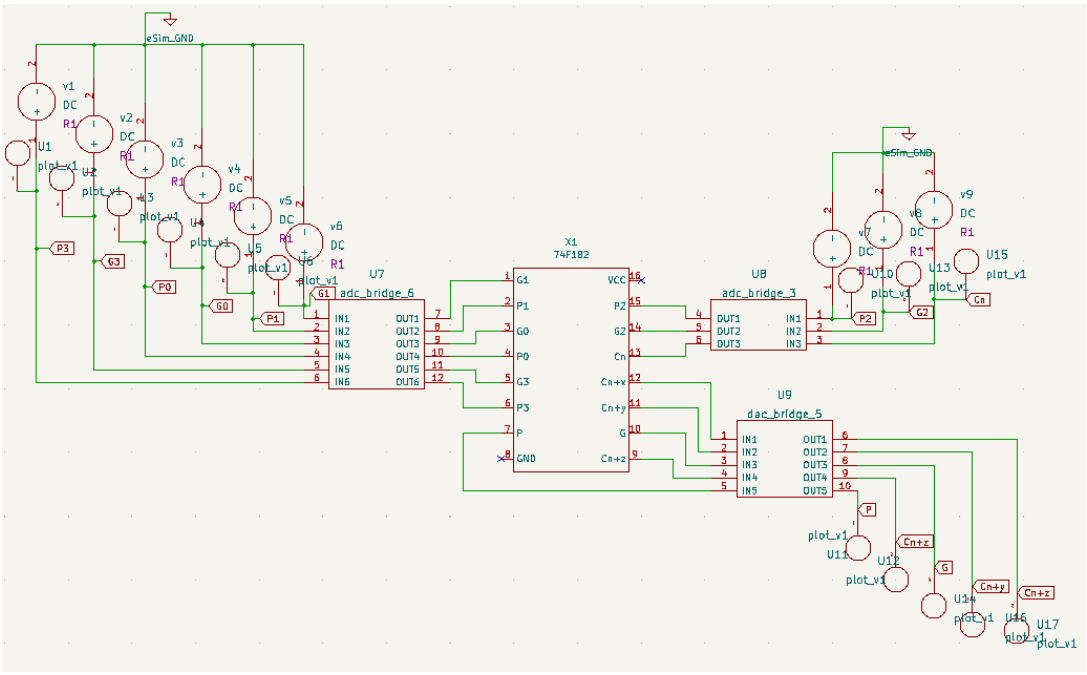


Figure 11.3: Test Circuit Schematic Diagram of 74F182

11.7 Analysis details

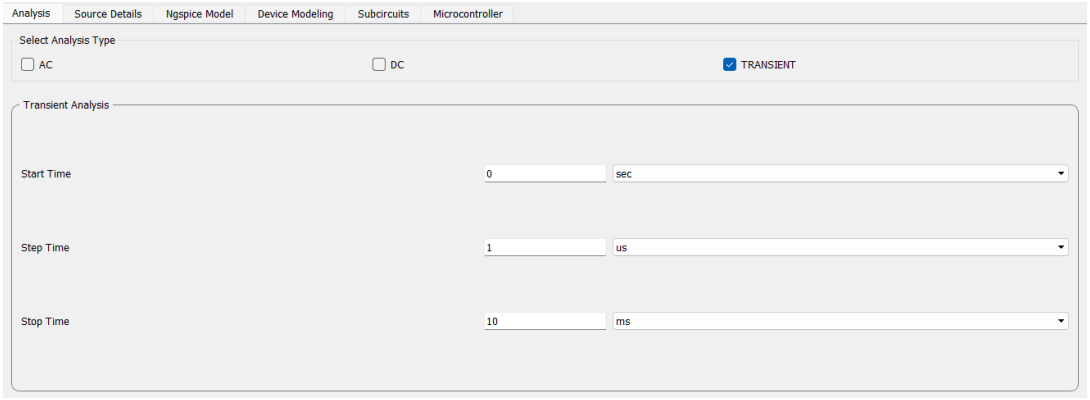


Figure 11.4: Analysis details of 74F182

11.8 Source details

FUNCTION TABLE

INPUTS									OUTPUTS				
Cn	$\overline{G0}$	$\overline{P0}$	$\overline{G1}$	$\overline{P1}$	$\overline{G2}$	$\overline{P2}$	$\overline{G3}$	$\overline{P3}$	Cn+x	Cn+y	Cn+z	$\overline{G}$	$\overline{P}$
X	H	H							L				
L	H	X							L				
X	L	X							H				
H	X	L							H				
X	X	X	H	H						L			
X	H	H	H	X						L			
L	H	X	H	X						L			
X	X	X	L	X						H			
X	L	X	X	L						H			
H	X	L	X	L						H			
X	X	X	X	X	H	H					L		
X	X	X	H	H	H	X					L		
X	H	H	H	X	H	X					L		
L	H	X	H	X	H	X					L		
X	X	X	X	X	L	X					H		
X	X	X	L	X	X	L					H		
X	L	X	X	L	X	L					H		
H	X	L	X	L	X	L					H		
	X		X	X	X	X	H	H				H	
	X		X	X	H	H	H	X				H	
	X		H	H	H	X	H	X				H	
	H		H	X	H	X	H	X				H	
	X		X	X	X	X	L	X				L	
	X		X	X	L	X	X	L				L	
	X		L	X	X	L	X	L				L	
	L		X	L	X	L	X	L				L	
		H		X		X		X					H
		X		H		X		X					H
		X		X		H		X					H
		X		X		X		H					H
		L		L		L		L					L

NOTES:
H = High voltage level
L = Low voltage level
X = Don't care

Figure 11.5: Source details of 74F182

11.9 Input Plots

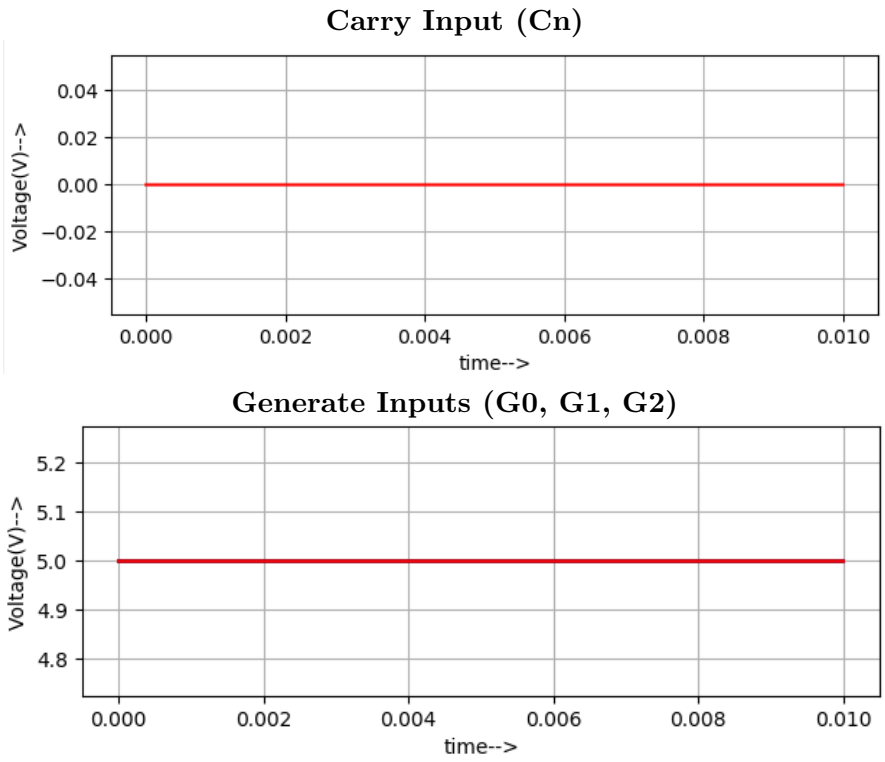


Figure 11.6: Input plots of 74F182

11.10 Output Plots

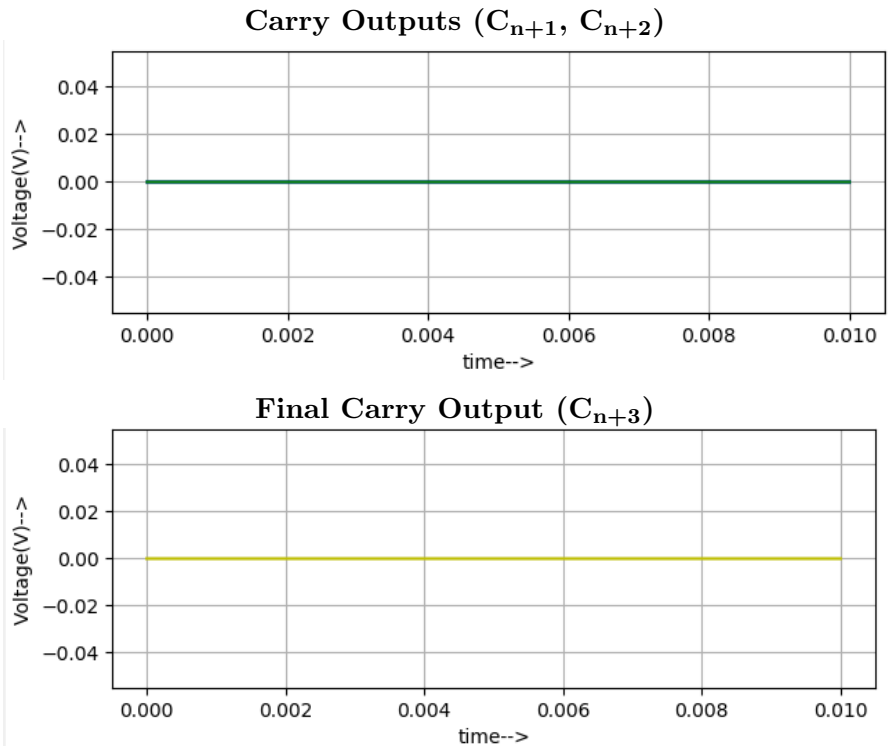


Figure 11.7: Output plots of 74F182

Chapter 12

SN74F257

12.1 General Description

Quad 2-to-1 Multiplexer with 3-State Outputs

The SN74F257 is a quad 2-to-1 multiplexer fabricated using Fast TTL (F-Series) technology. It is designed to select one of two input signals for each of the four channels and route the selected inputs to the corresponding outputs based on a common select control input.

The device consists of four independent multiplexers with a shared select line and an active-low output enable input. When enabled, the selected inputs are transferred to the outputs. When the output enable input is deasserted, the outputs are placed in a high-impedance state, allowing multiple devices to share a common data bus without contention.

Due to its high-speed operation, 3-state output capability, and TTL compatibility, the SN74F257 is widely used in bus-oriented systems, data routing applications, and digital control circuits requiring fast and reliable signal selection.

12.2 Key Features

The key features of SN74F257 include:

- **Quad 2-to-1 Multiplexer:** Provides four independent 2-to-1 multiplexing channels.
- **3-State Outputs:** Enables connection to shared data buses without output conflicts.
- **Common Select Input:** A single select control line simultaneously controls all four channels.
- **Active-Low Output Enable:** Allows enabling or disabling of all outputs together.
- **High-Speed Fast TTL Technology:** Ensures fast switching and reliable performance.
- **TTL Compatible:** Fully compatible with standard TTL logic levels.

12.3 Application

The various applications of SN74F257 are:

- **Bus Multiplexing:** Used to select between multiple data sources on a shared bus.
- **Data Routing and Selection:** Employed in digital systems for controlled signal routing.
- **Microprocessor and Microcontroller Systems:** Used to multiplex address or data lines in processor-based designs.
- **Memory and I/O Interfacing:** Applied in systems requiring selection between different memory or peripheral devices.
- **Digital Control Circuits:** Used in control logic where fast and reliable signal selection is required.

12.4 Pin Diagram

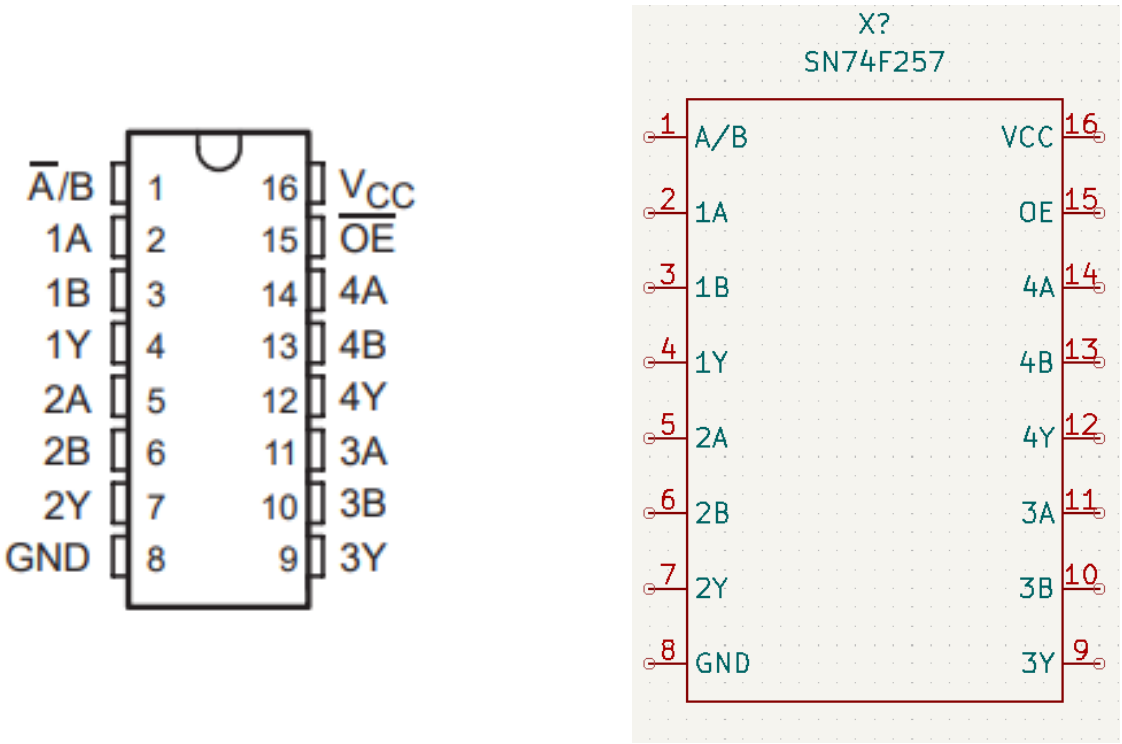


Figure 12.1: Pin diagram of SN74F257

12.5 Subcircuit Schematic Diagram

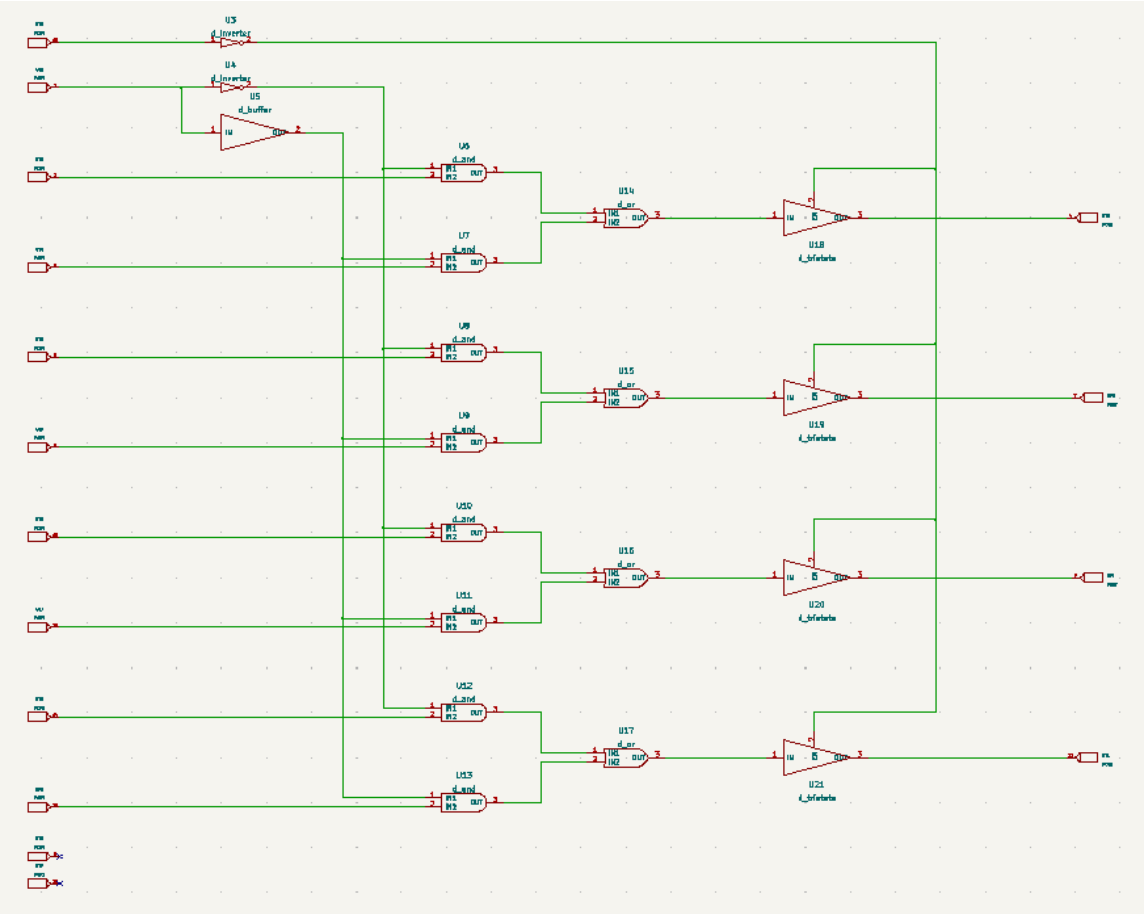


Figure 12.2: Subcircuit Schematic Diagram of SN74F257

12.6 Test Circuit Schematic Diagram

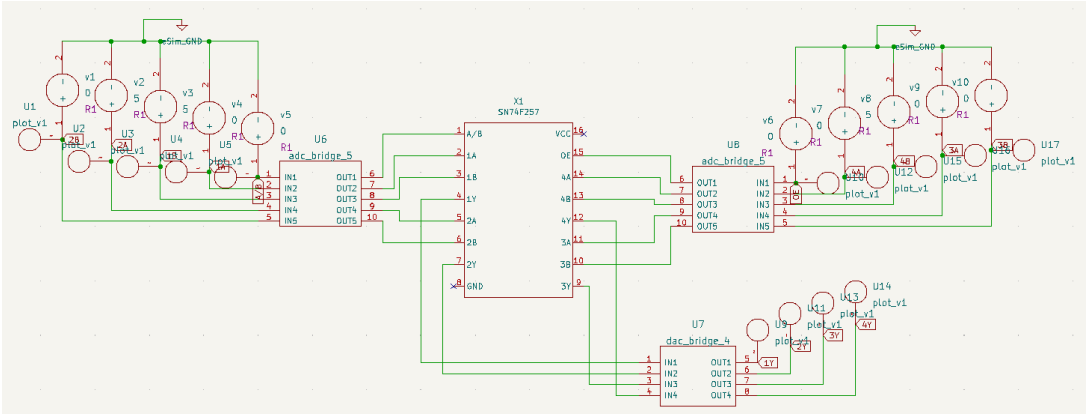


Figure 12.3: Test Circuit Schematic Diagram of SN74F257

12.7 Analysis details

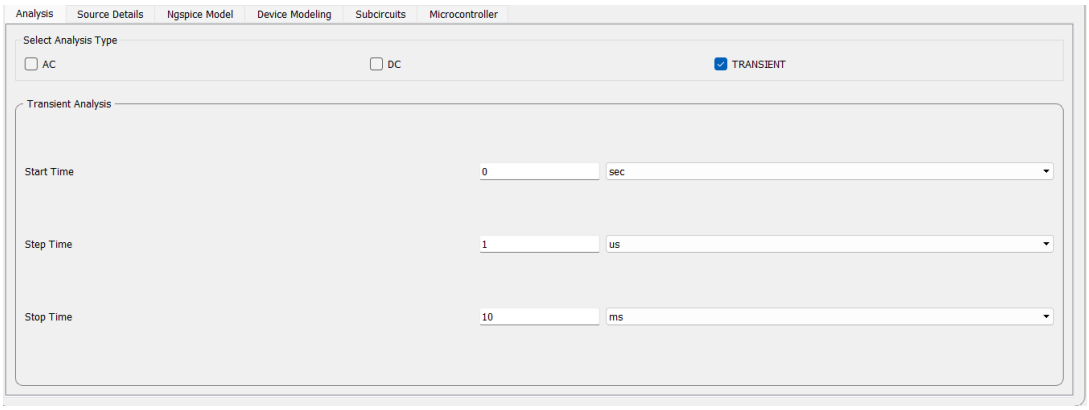


Figure 12.4: Analysis details of SN74F257

12.8 Source details

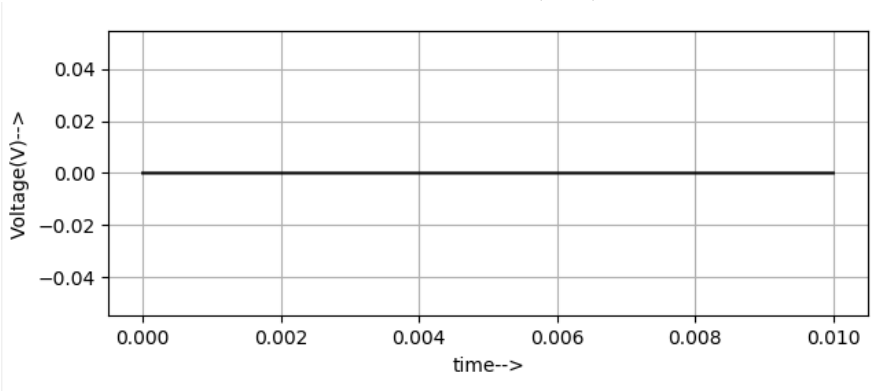
FUNCTION TABLE

INPUTS				OUTPUT
$\overline{OE}$	$\overline{A}$/B	A	B	Y
H	X	X	X	Z
L	L	L	X	L
L	L	H	X	H
L	H	X	L	L
L	H	X	H	H

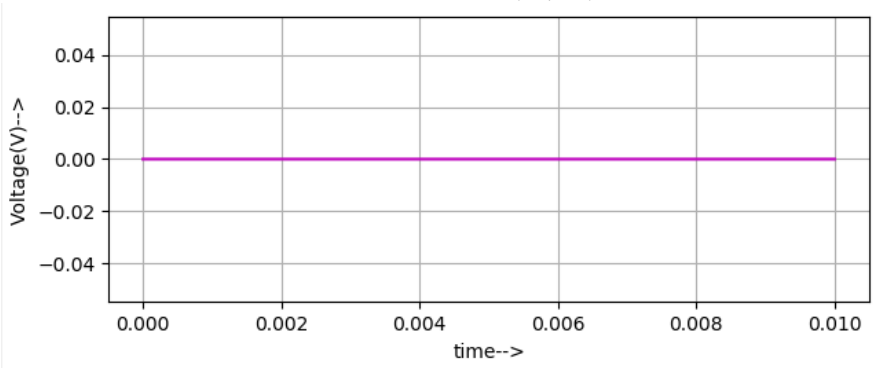
Figure 12.5: Source details of SN74F257

12.9 Input Plots

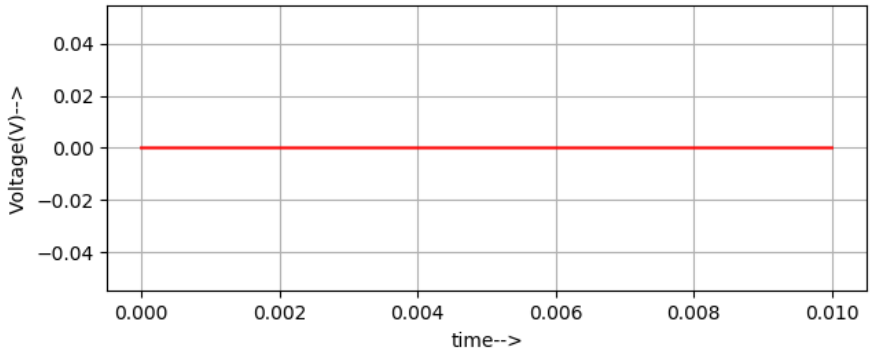
Output Enable (OE)



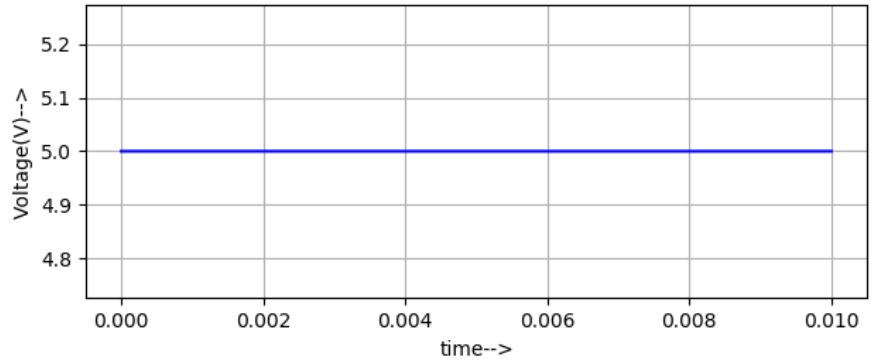
Select Inputs (A/B)



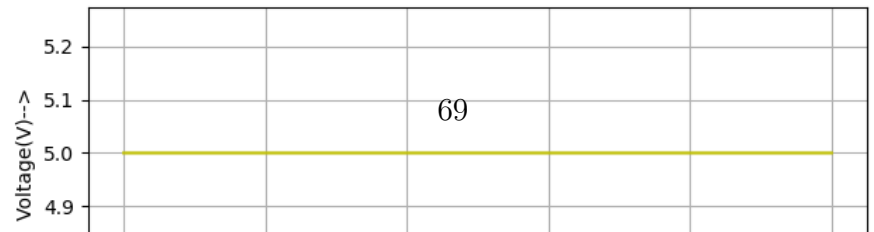
Input 1A



Input 1B



Input 2A



12.10 Output Plots

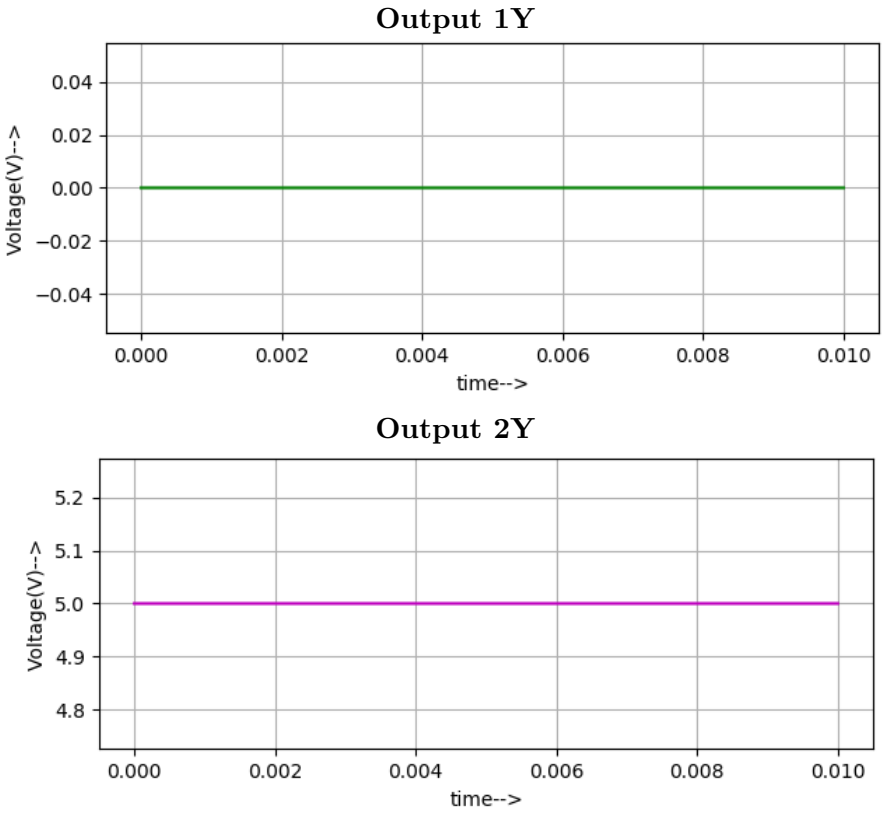


Figure 12.7: Output plots of SN74F257

Chapter 13

Failed ICs

13.1 Failed IC: 74F385

13.1.1 General Overview

The 74F385 is a high-speed Quad Serial Adder/Subtractor fabricated using Fast TTL (F-Series) technology. It is designed to perform serial arithmetic operations on binary data streams, supporting both addition and subtraction functions under the control of mode selection inputs.

The device consists of four identical serial adder/subtractor stages that operate on serial input data synchronized by a clock signal. Each stage processes one bit per clock cycle, allowing arithmetic operations on multi-bit data words in a serial manner. The IC includes carry storage and control logic to support proper arithmetic sequencing.

Serial adders such as the 74F385 are commonly used in applications where hardware resource optimization is required and parallel arithmetic is not essential. Due to the complexity of internal timing, carry propagation, and clock synchronization, accurate behavioral modeling of the device presents significant challenges in circuit simulation environments.

13.1.2 Test Circuit Schematic

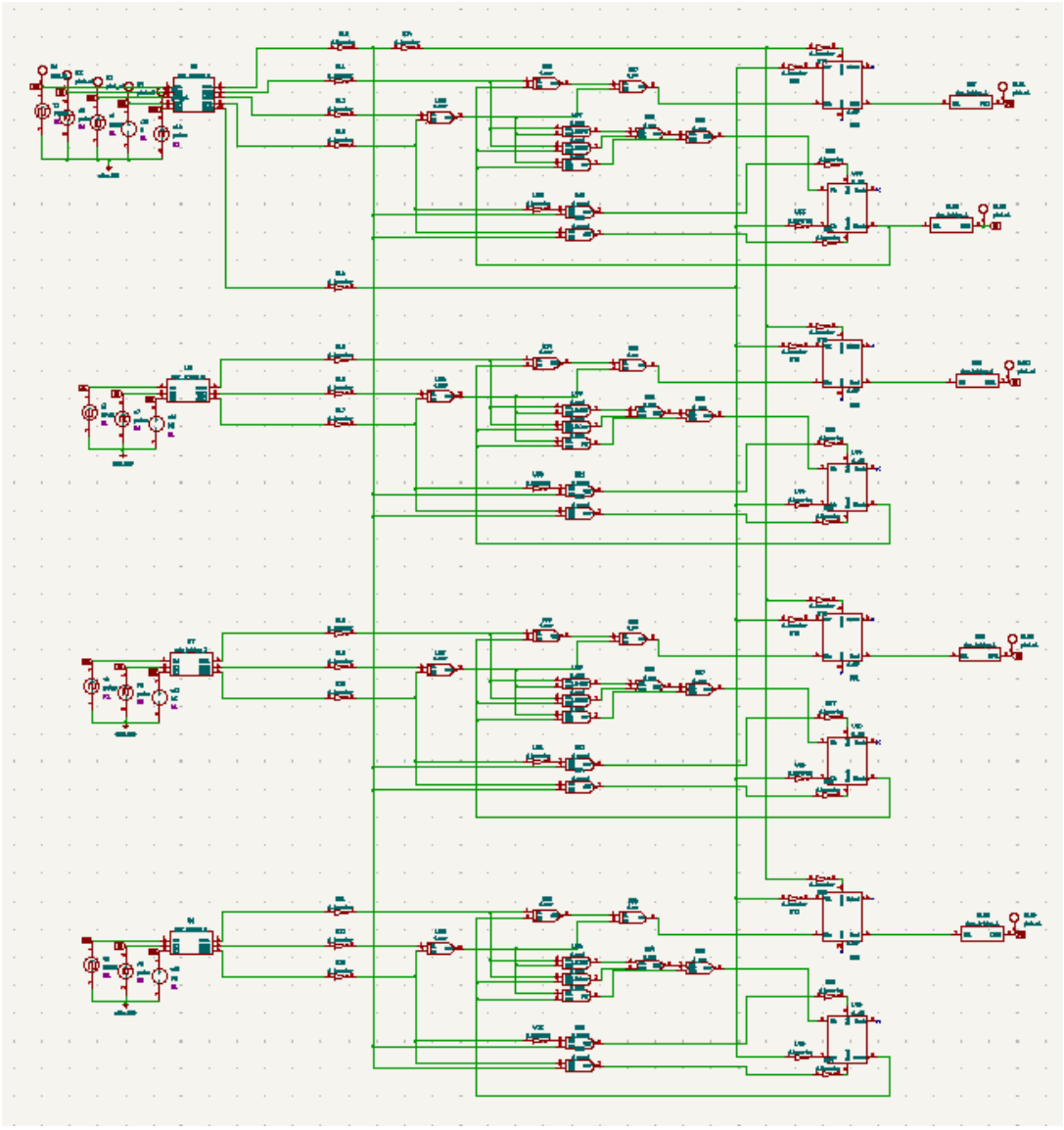


Figure 13.1: Test circuit schematic of 74F385

13.1.3 Issues Faced

Despite multiple implementation attempts, the 74F385 IC could not be successfully simulated. The primary challenges encountered are listed below:

- The D flip flops used in the datasheet schematic had asynchronous set and reset whereas the eSim D flip flop component has synchronous set and reset due to which the IC couldnt reset before performing the operations.
- Timing mismatches were observed between the serial inputs, clock, and carry outputs, leading to incorrect arithmetic results.
- The internal control logic governing addition and subtraction modes could not be faithfully replicated due to limited access to internal device behavior.

Due to these unresolved timing and synchronization issues, the 74F385 model could not be validated.

13.2 Failed IC: MC14518B

13.2.1 General Overview

The MC14518B is a dual BCD up-counter fabricated using CMOS technology. It is designed to count decimal values from 0 to 9 in each counter stage and is commonly used in digital clocks, frequency counters, and timing applications. The device consists of two independent BCD counters with separate clock and control inputs.

The IC supports cascading and includes internal logic to handle decimal counting, carry generation, and reset operations. Due to the dual-counter architecture and internal timing dependencies, accurate modeling of the device requires precise synchronization between clock, reset, and carry signals.

13.2.2 Test Circuit Schematic

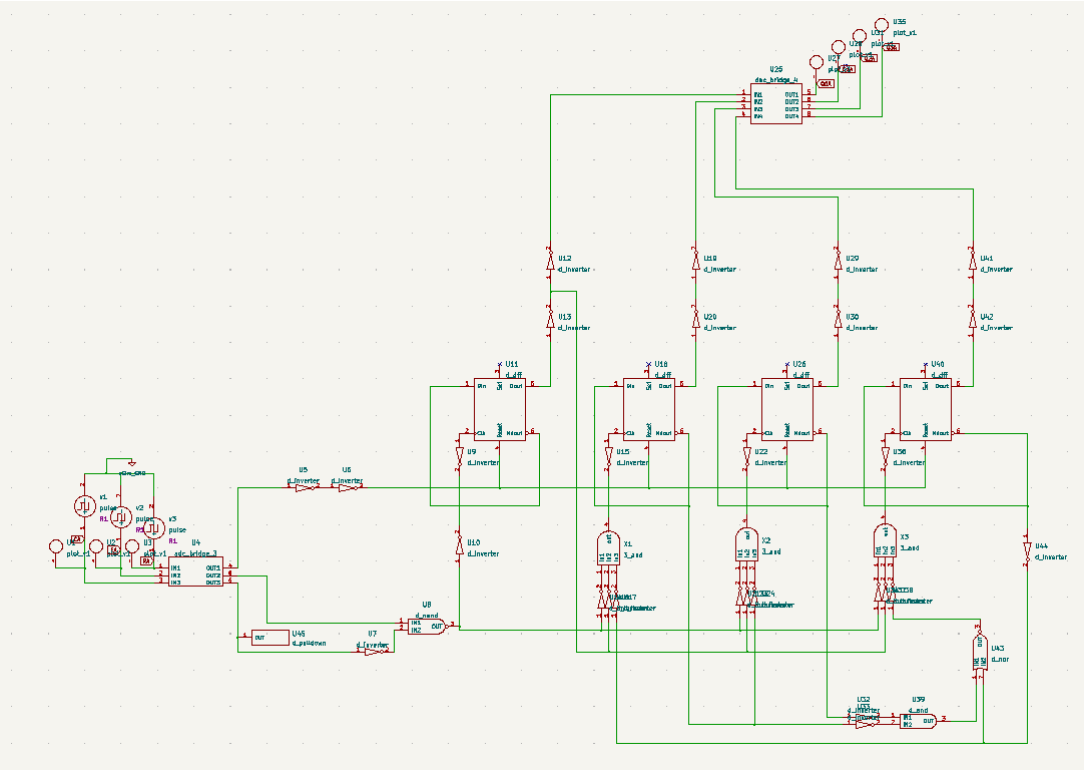


Figure 13.2: Test circuit schematic of MC14518B

13.2.3 Issues Faced

Despite multiple implementation attempts, the MC14518B IC could not be successfully simulated. The primary challenges encountered include:

- Clock pulse couldnt be given accurately as depicted in the timing diagram. Clock goes low after the 12th cycle and its not possible to vary pulse parameter based on number of cycles so couldnt proceed with the simulation.

Due to this issue the MC14518B model could not be validated and was therefore classified as a failed IC.

Chapter 14

Conclusion and Future Scope

This project was undertaken as part of the eSim Semester Long Internship Autumn 2025 with the primary objective of implementing and simulating a diverse range of analog and digital integrated circuits using the open-source EDA tool eSim. The workflow involved modeling each IC based on its official datasheet specifications, creating schematic representations, designing custom symbols, and developing corresponding test circuits for functional verification. Simulations were conducted using KiCad and Ngspice, ensuring that each IC model closely adhered to the expected logical and behavioral characteristics.

Through this endeavor, a comprehensive understanding of the internal operation of ICs, circuit-level design principles, and debugging techniques in open-source EDA environments was gained. The project culminated in the successful development of numerous subcircuits, including Logic Gates, Multiplexers,De-Multiplexers, Encoders,Decoders,counters etc. These models have now been validated for accuracy and are ready for integration into the eSim subcircuit library, offering a valuable resource for students, educators, researchers, and developers alike.

Beyond its technical outcomes, the project significantly enhanced practical skills in schematic design, simulation-based validation, and structured documentation, all of which are critical in the domain of VLSI and circuit design. Moreover, it lays a strong foundation for the future expansion of eSim's component library. As open-source EDA tools continue to gain traction, this work contributes meaningfully to the ecosystem, empowering the eSim community and supporting the broader goal of accessible, high-quality electronic design education and research.