Winter Internship Report

On

Integrated Circuit Design using Subcircuit Feature of eSim

Submitted by

Rachith H

Under the guidance of

Prof.Kannan M. Moudgalya
Chemical Engineering Department
IIT Bombay

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Acknowledgment

We take this opportunity to express our sincere gratitude to FOSSEE, IIT Bombay for providing us with the platform to work on the design and integration of multiple sub-circuits in eSim. This internship has been an enriching journey, offering us valuable exposure to open-source EDA tools and their significance in circuit simulation and design. The hands-on experience we gained has deepened our understanding of circuit modeling, simulation, and verification, preparing us for future challenges in the field of electronics and semiconductor design.

We extend our heartfelt appreciation to Prof. Kannan M. Moudgalya for his support. His emphasis on open-source innovation has been truly inspiring, and we feel privileged to have been a part of this initiative.

A special note of thanks to our mentor, Mr. Sumanto Kar for his invaluable assistance, constructive feedback, and mentorship. His expertise and willingness to help at every stage ensured that we could effectively navigate challenges and successfully complete our project tasks. His patience and technical insights have played a crucial role in enhancing our problem-solving skills.

This internship has been a remarkable learning experience, helping us develop not just technical skills but also a deeper appreciation for collaborative development in open-source projects. As we aspire to build careers in the VLSI industry, the knowledge and skills gained here will serve as a strong foundation for our professional growth.

We are immensely grateful for this opportunity and look forward to applying our learnings in meaningful ways in the future.

Contents

Chapter 1

Introduction

1.1 FOSSEE

FOSSEE (Free and Open Source Software for Education) is an initiative by IIT Bombay aimed at promoting the use of open-source software in educational institutions. The project focuses on providing free and open-source tools for various domains like electronics, mathematics, simulation, and engineering design.
FOSSEE encourages the adoption of open-source alternatives to expensive proprietary software, making tools for learning, research, and development more accessible to students, educators, and professionals. The initiative supports a range of tools, such as eSim for circuit design, Scilab for numerical computations, and other software for system modeling, simulation, and visualization. Through its efforts, FOSSEE has contributed significantly to making high-quality educational resources available to a global community while fostering the use of open-source software.

1.2 eSim

eSim is an open-source Electronic Design Automation (EDA) tool developed by FOSSEE, IIT Bombay, designed to assist engineers, students, and researchers in creating, simulating, and analyzing electronic circuits. It integrates several open-source tools like Ngspice for circuit simulation, KiCad for PCB design, Scilab for numerical computation, and Python for scripting and automation. eSim also supports mixed-signal simulation through NGHDL (combining Ngspice with GHDL) and system-level modeling with OpenModelica. With its completely free and open-source nature, eSim provides an accessible and cost-effective alternative to proprietary EDA tools, making it an ideal platform for learning and research in electronics design.

1.3 Ngspice

Ngspice is an open-source, powerful circuit simulator based on the SPICE (Simulation Program with Integrated Circuit Emphasis) model, used for simulating and analyzing electronic circuits. It supports a wide range of simulations, including DC, AC, transient, and noise analysis, making it suitable for both analog and mixed-signal circuit designs. Ngspice uses a text-based input format for defining circuit components and their connections, which is simple to understand and modify. It is highly customizable and can be extended with new models and components, making it a flexible tool for research and development. Ngspice integrates well with other open-source tools, such as KiCad and eSim, and is widely used in educational and professional environments due to its cost-free nature and reliability.

1.4 KiCad

KiCad is an open-source PCB design tool that is widely used for designing electronic circuits, including schematic capture and PCB layout. In eSim, KiCad plays a vital role by providing users with the ability to design and lay out printed circuit boards (PCBs). It offers features like component libraries, schematic design, automatic routing, and Gerber file generation, which are essential for PCB manufacturing. By integrating KiCad, eSim enables a seamless workflow where users can design circuits and move on to the PCB layout stage without needing separate software tools. This integration enhances the overall design process, especially for students and researchers working on electronic projects.

Chapter 2

Problem Statement

- **Internship Focus:** During my internship, I utilized the Subcircuit Builder feature of eSim to design practical, real-life integrated circuits (ICs) based on standard datasheets provided by various companies.
- **Problem Definition:** The main challenge was to accurately translate the specifications from datasheets into functional circuit models within eSim. This involved understanding the characteristics and behavior of individual components as specified in the datasheets.
- **Circuit Design:** I created subcircuits that replicated the design of real-world ICs, ensuring they matched the given datasheet characteristics and worked as intended.
- **Simulation and Analysis:** After building the subcircuits, I simulated them using eSim to analyze their performance under different conditions, ensuring their behavior aligned with the datasheet data.
- **Objective:** The primary objective was to create accurate circuit models that could be used for further analysis, testing, or development while ensuring a high level of fidelity to real-world specifications.
- **Skills Gained:** This experience helped me develop a deeper understanding of circuit design, the process of interpreting datasheet information, and applying it to practical simulation tasks in eSim.

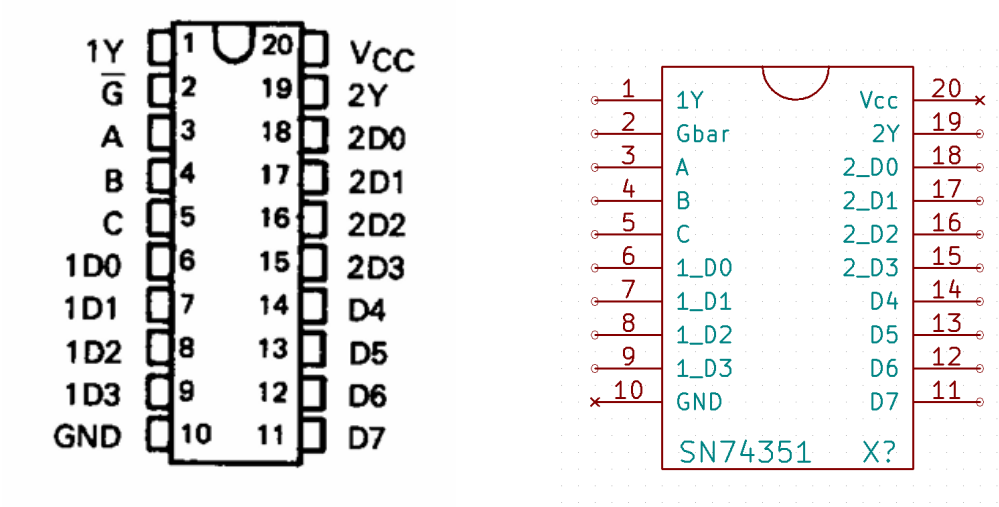
Chapter 3

SN74351

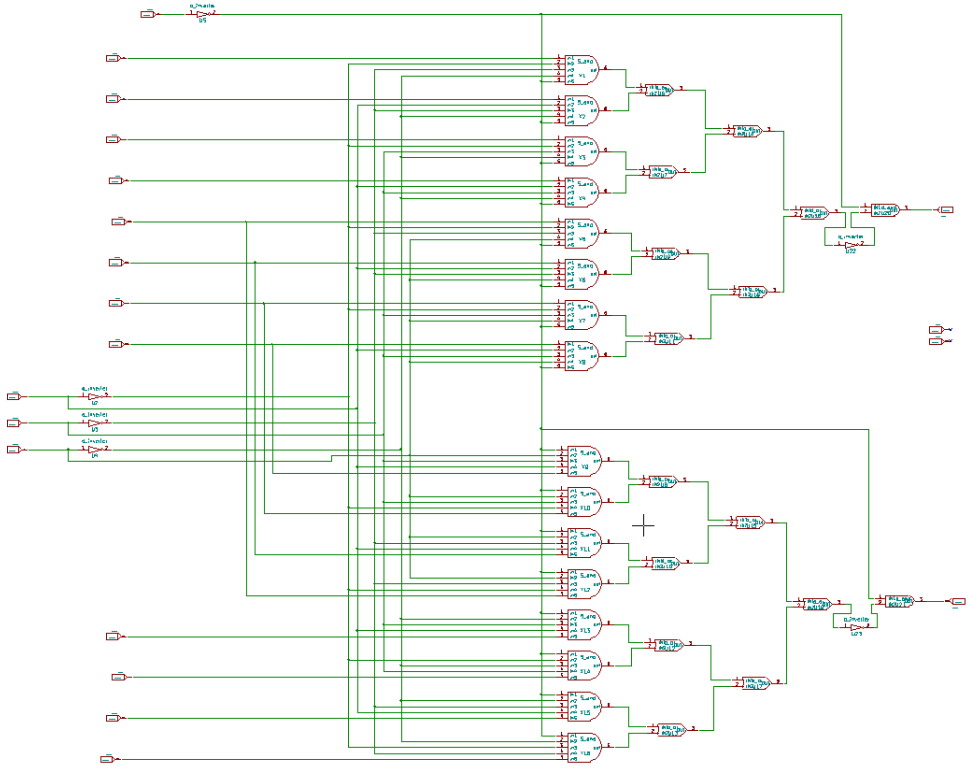
3.1 General Description

Dual data selector with 3 state output
The SN74351 comprises two 8-line-to-1-line data selectors/multiplexers with full decoding on one monolithic chip. Symmetrically switching, complementary decode generators minimize decoder skew during changes at the select inputs and ensure that potentially erroneous effects are minimized at the data outputs. Four data inputs are exclusive to each multiplexer and four are common to both. A common enable input is provided which, when high, causes both outputs to assume the high-impedance (off) state. A low logic level at the enable input activates both outputs so that each will assume the complement of the level of the selected input.

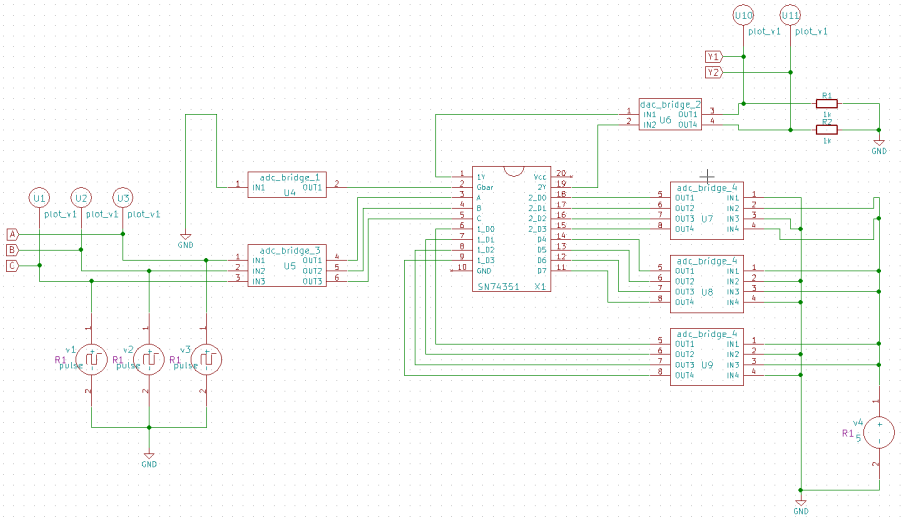
3.2 Pin Diagram



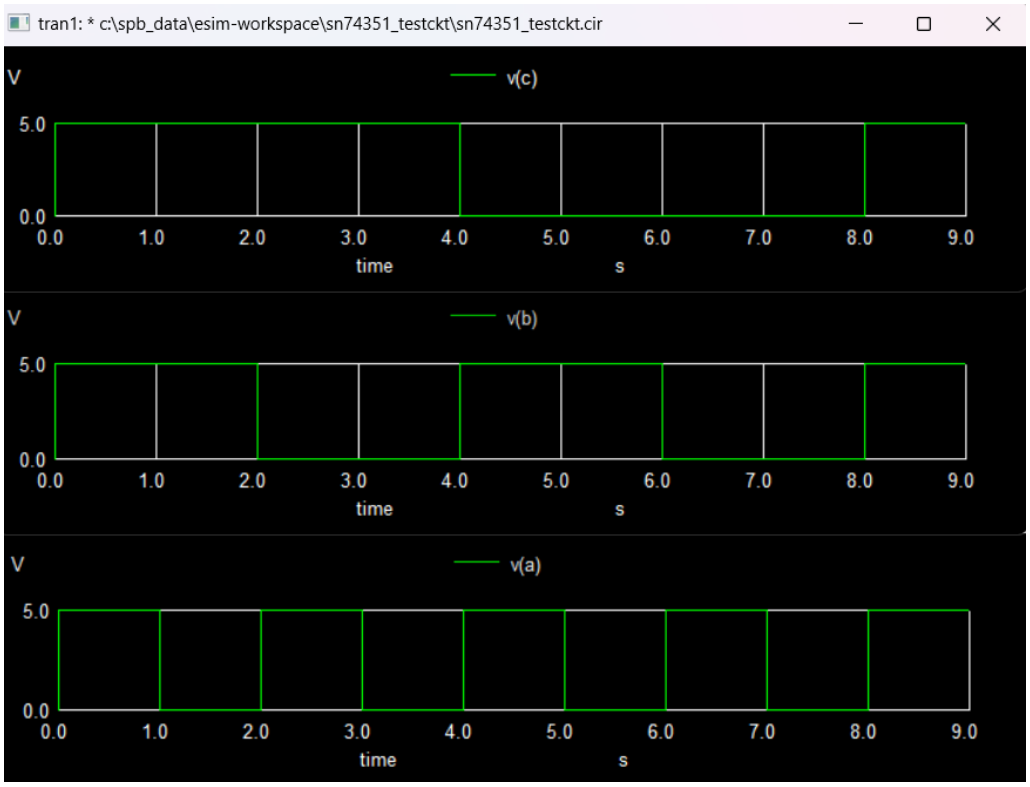
3.3 Subcircuit Schematic



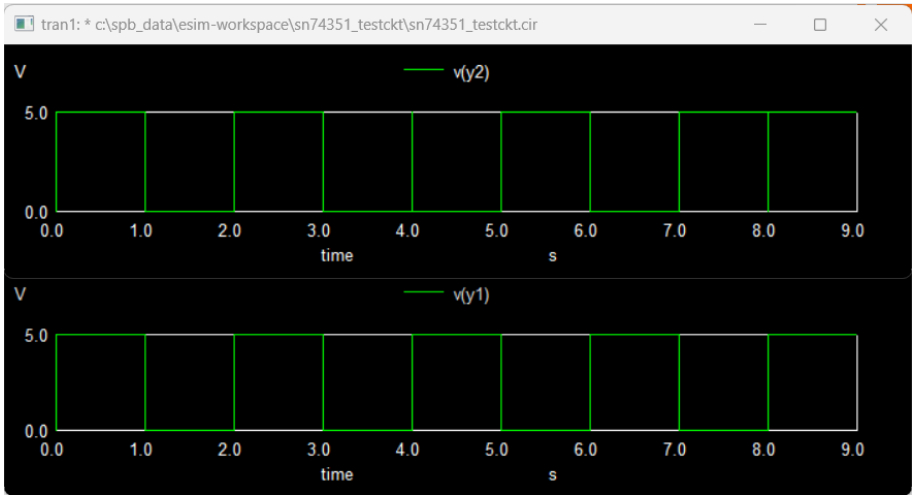
3.4 Test Circuit Schematic



3.5 Input Plots



3.6 Output Plots



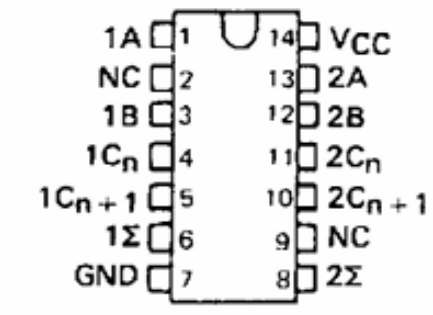
Chapter 4

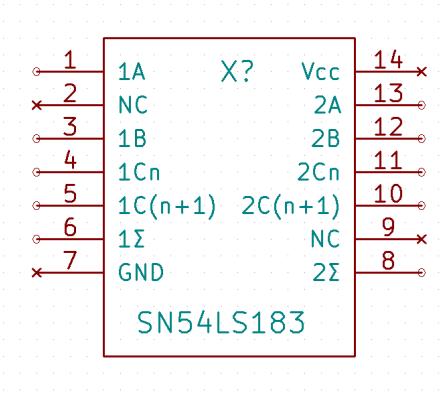
SN54LS183

4.1 General Description

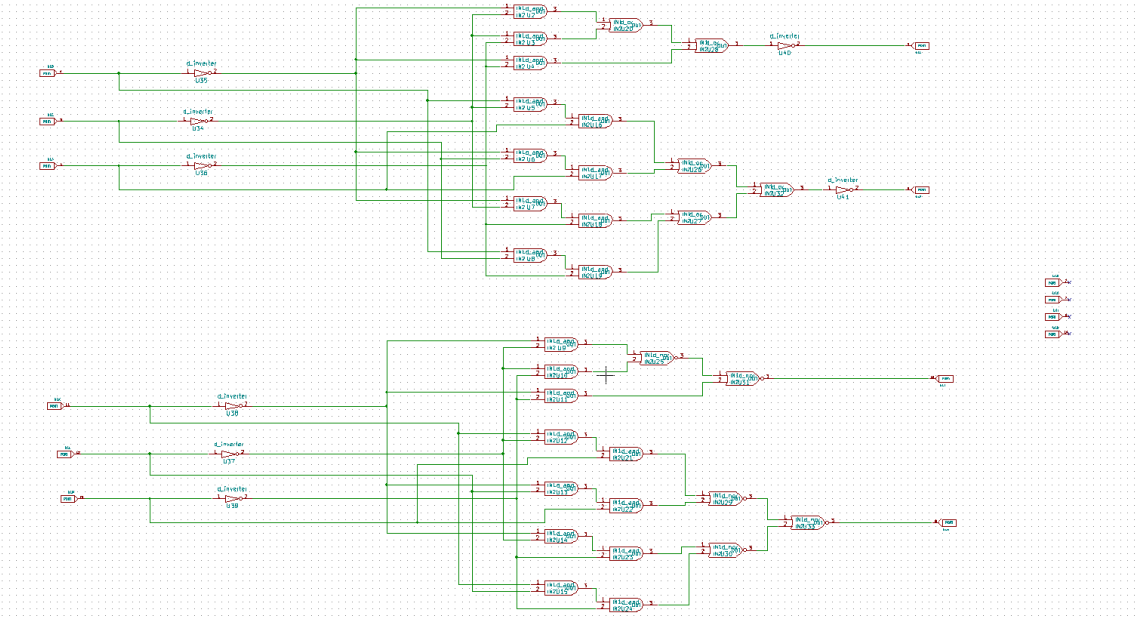
Dual carry save full adders
These dual full adders feature an individual carry output from each bit for use in multiple-input, carry-save techniques to produce the true sum and true carry outputs with no more than two gate delays.The SN54LS183 Dual Carry Save Adder is used in high-speed arithmetic operations, particularly in multipliers like the Wallace Tree and Booth's algorithm, where it efficiently reduces partial sums before final addition.

4.2 Pin Diagram

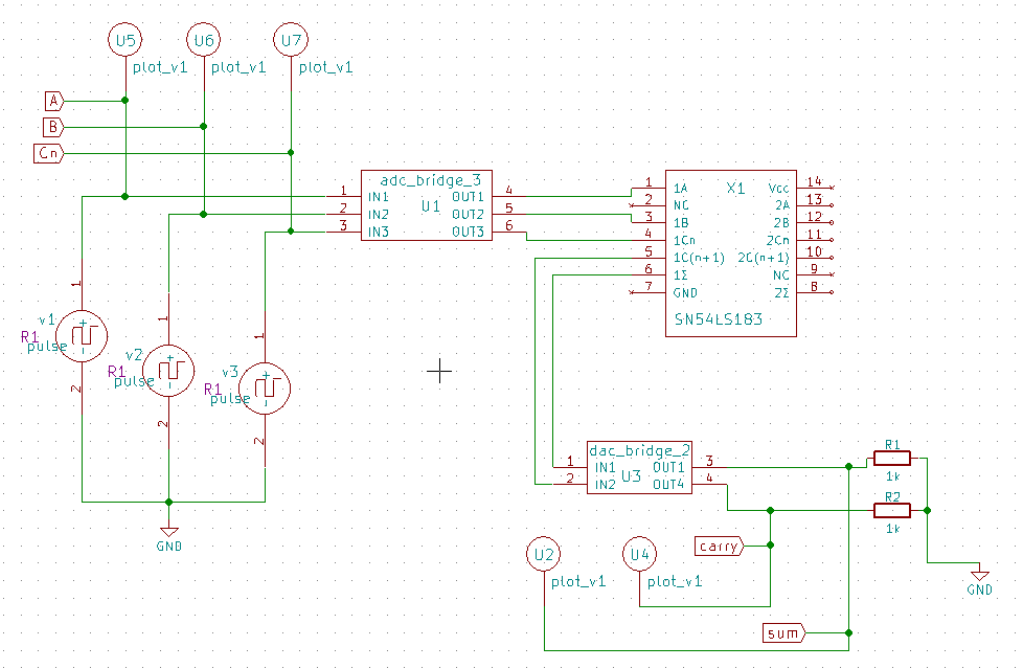




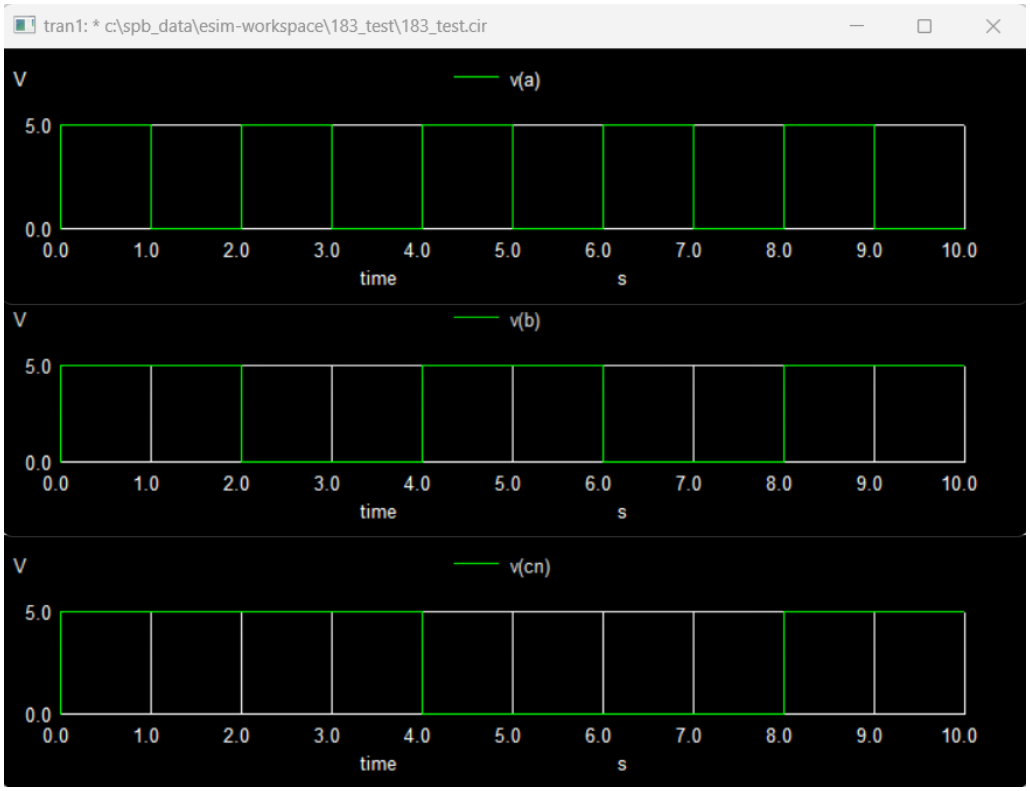
4.3 Subcircuit Schematic



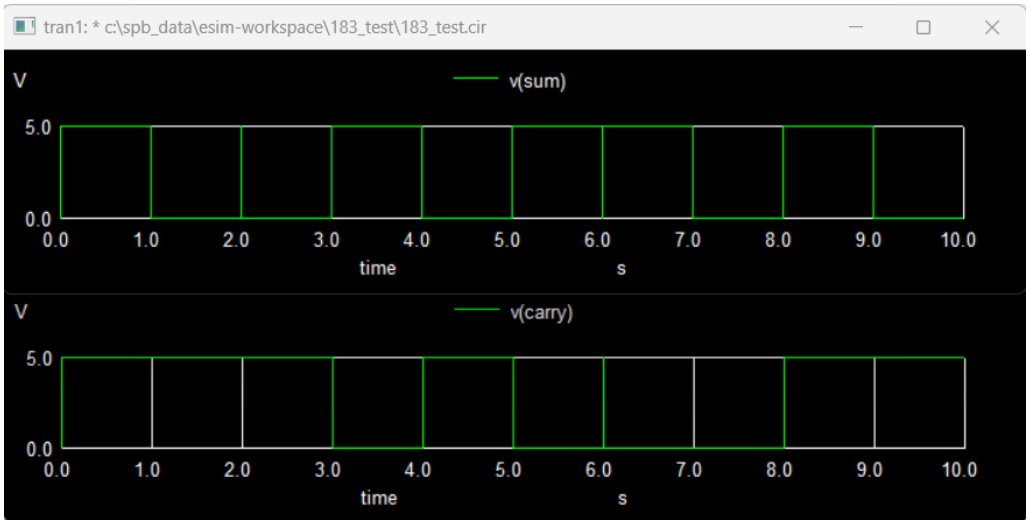
4.4 Test Circuit Schematic



4.5 Input Plots



4.6 Output Plots



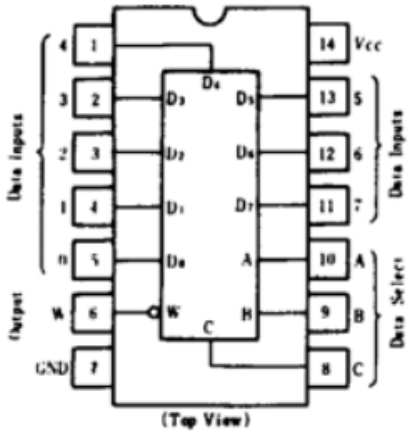
Chapter 5

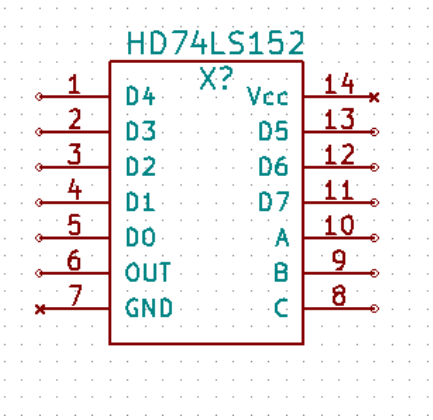
HD74LS152

5.1 General Description

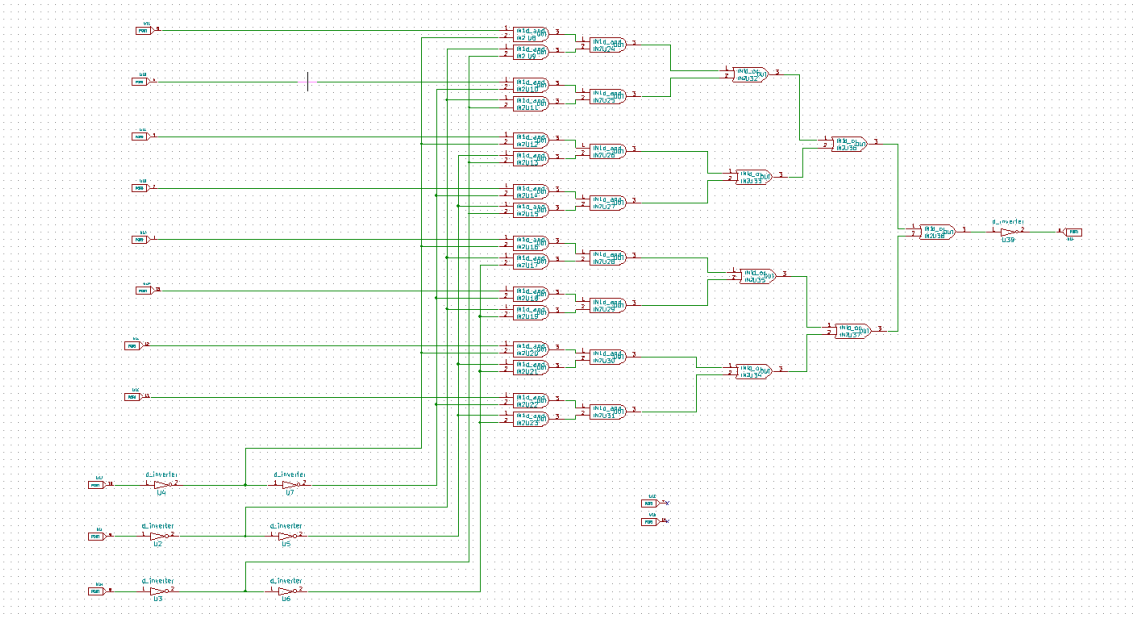
1-of-8 Data Selector / Multiplexer
The HD74LS152 is a high-speed 8-to-1 multiplexer with active-low outputs. It selects one of the eight data inputs based on a 3-bit select input and outputs the corresponding value in an inverted form. Common applications include data selection, signal routing, digital signal processing (DSP), and address decoding in memory and microprocessor systems. Its low power consumption and high-speed operation make it suitable for various digital logic applications.

5.2 Pin Diagram

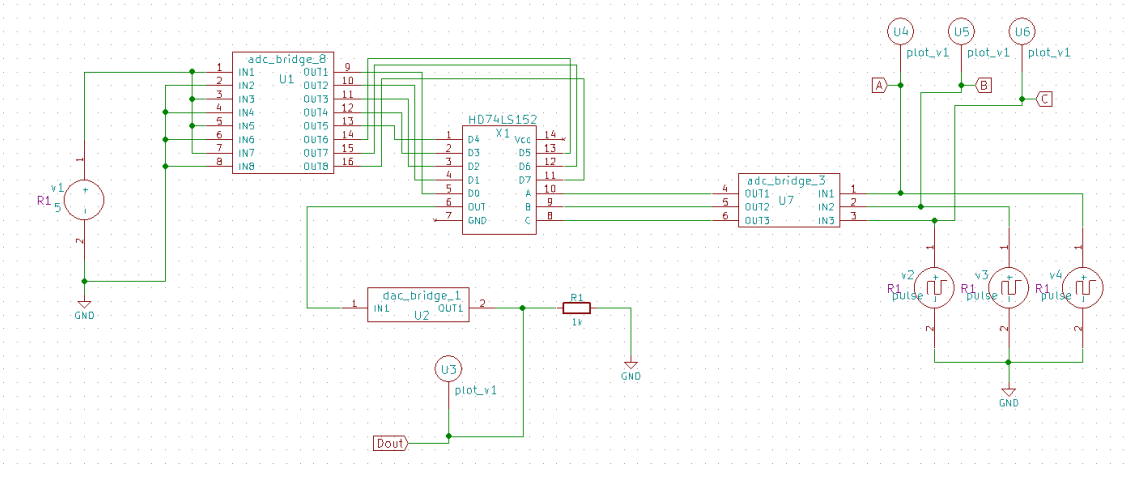




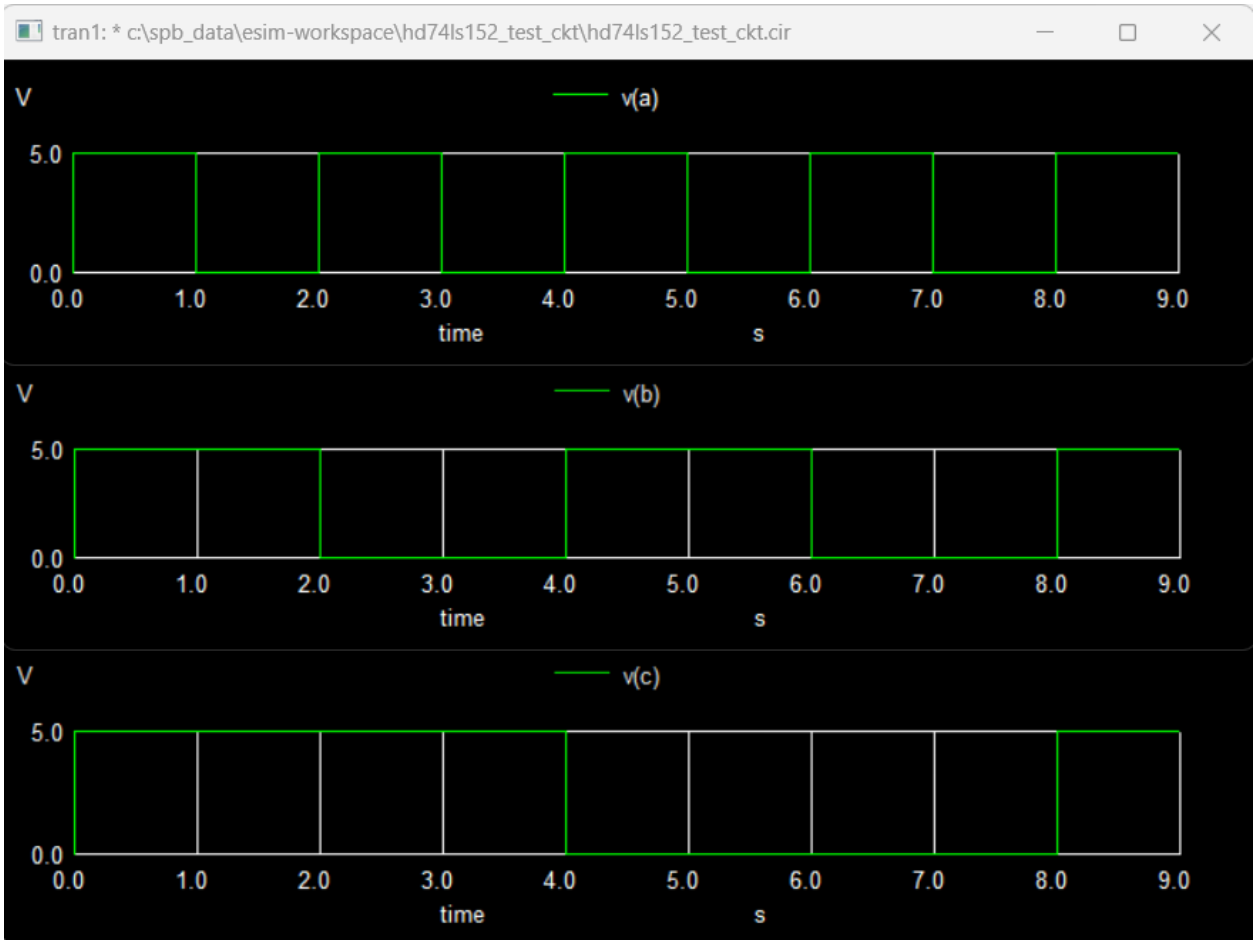
5.3 Subcircuit Schematic



5.4 Test Circuit Schematic



5.5 Input Plots



5.6 Output Plots

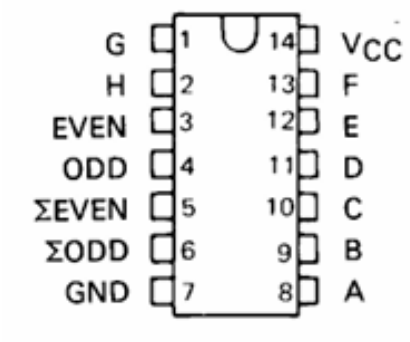
Chapter 6

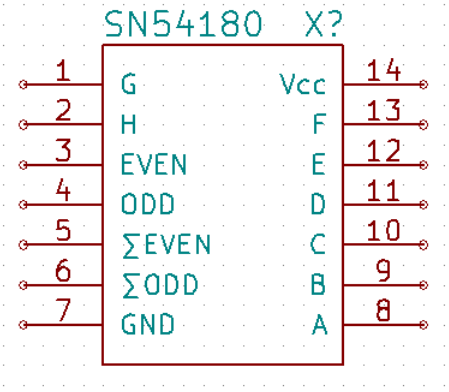
SN54180

6.1 General Description

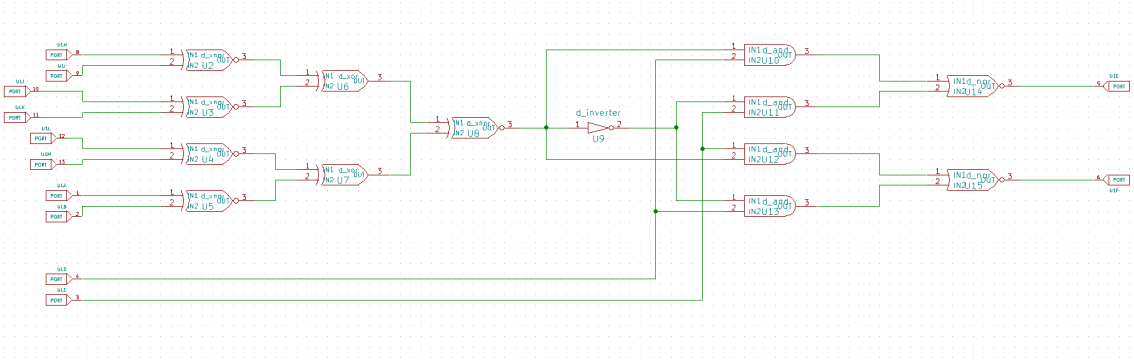
9 bit odd/even parity generator
These universal, monolithic, 9-bit (8 data bits plus 1 parity bit) parity generators/checkers, utilize familiar Series 54/74 TTL circuitry and feature odd/even outputs and control inputs to facilitate operation in either odd or even-parity applications. Depending on whether even or odd parity is being generated or checked, the even or odd inputs can be utilized as the parity or 9th-bit input. The word-length capability is easily expanded by cascading.

6.2 Pin Diagram

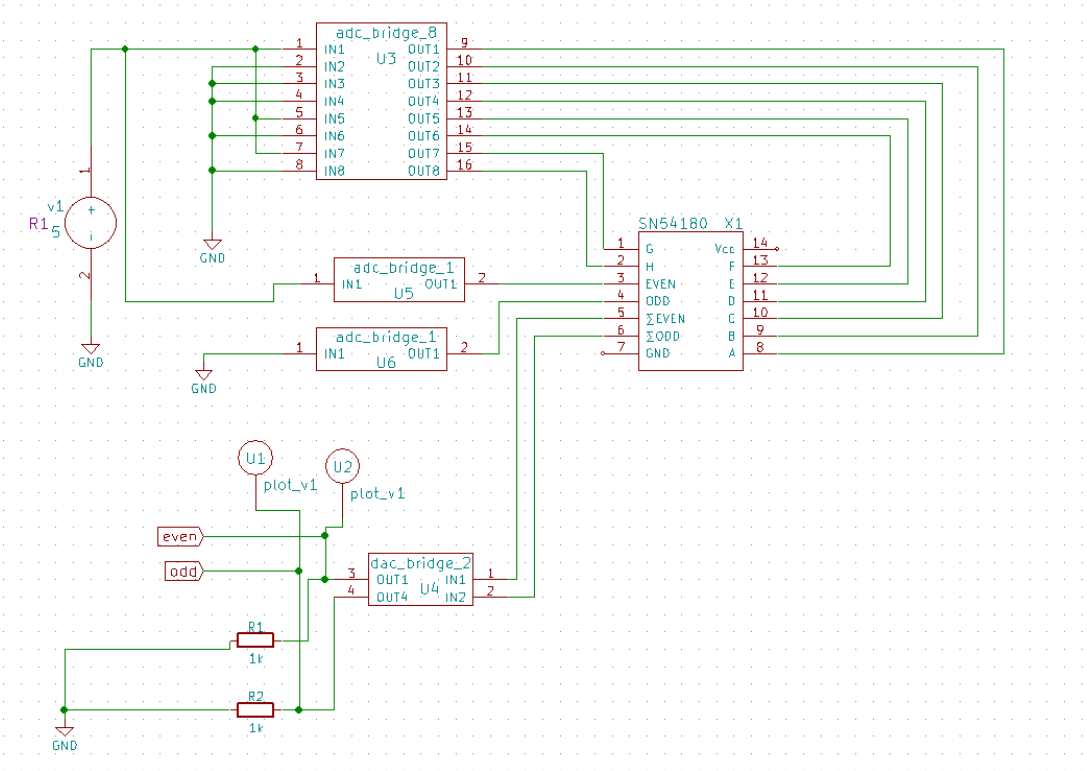




6.3 Subcircuit Schematic



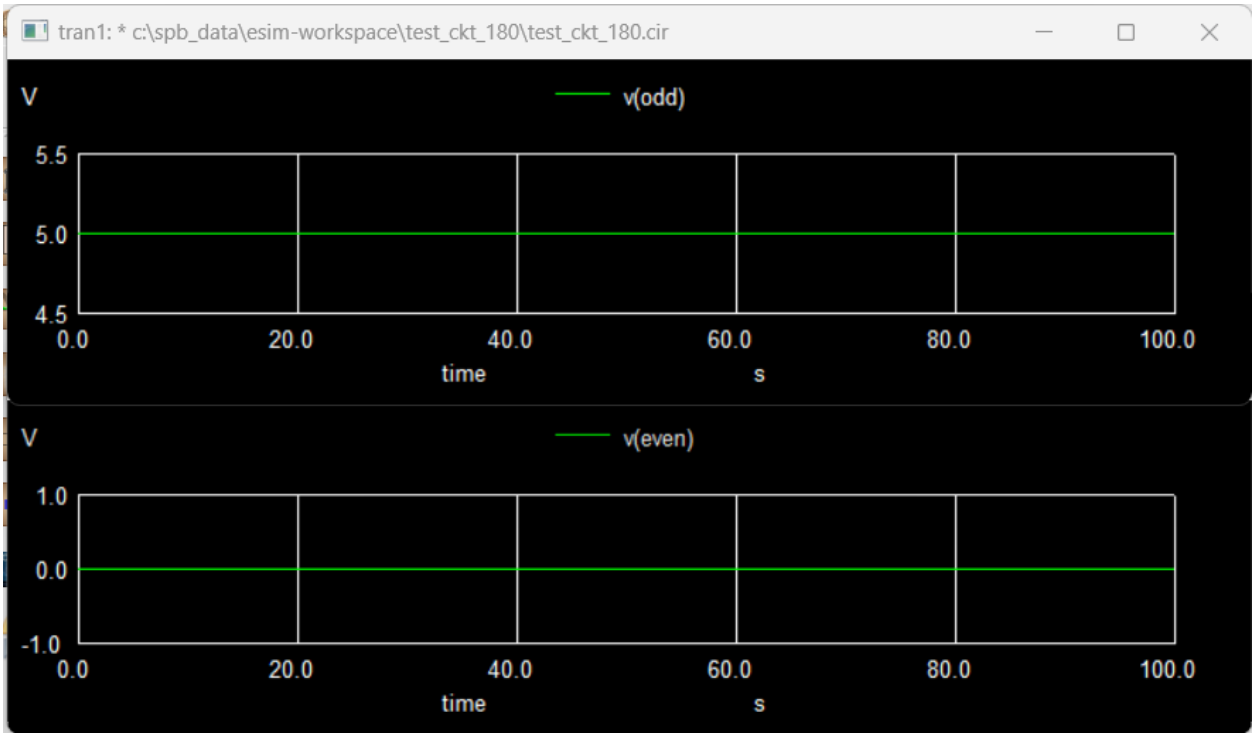
6.4 Test Circuit Schematic



6.5 Inputs

Input Bits : 10001010

6.6 Output Plots



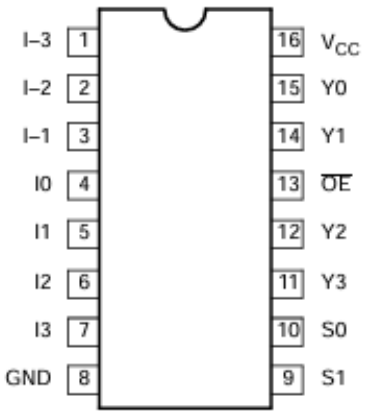
Chapter 7

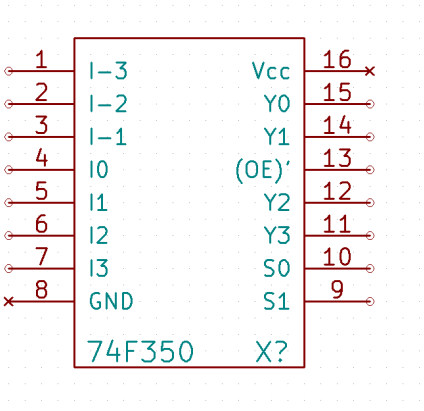
74F350

7.1 General Description

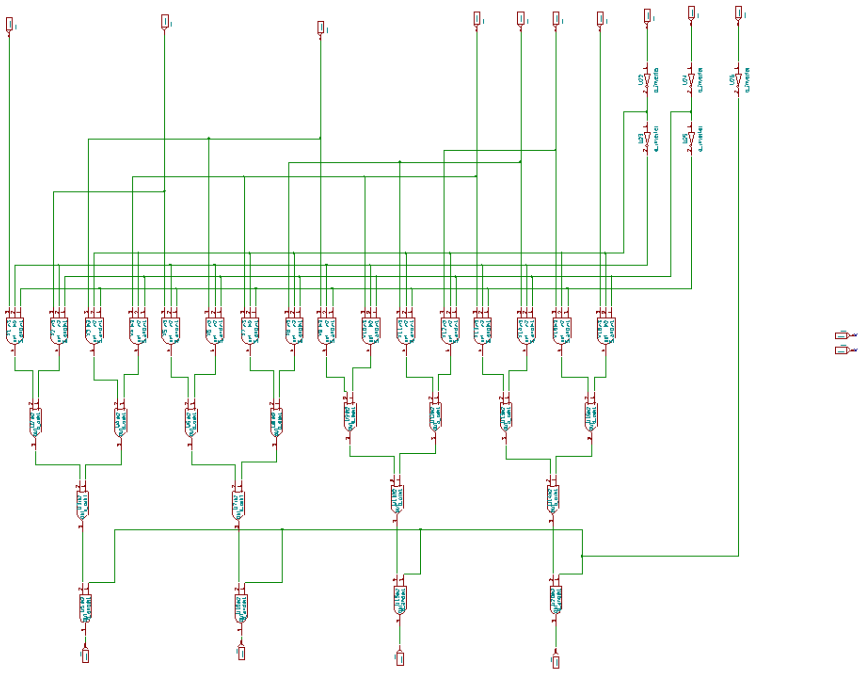
4-bit shifter
The 74F350 is a combination logic circuit that shifts a 4-bit word from 0 to 3 places. No clocking is required as with shift registers. The 74F350 can be used to shift any number of bits any number of places up or down by suitable interconnection. The 3-State outputs are useful for bus interface applications or expansion to a larger number of shift positions in end around shifting. The active Low Output Enable (OE) controls the state of the outputs. The outputs are in the high impedance off state when OE is High, and they are active when OE is Low

7.2 Pin Diagram

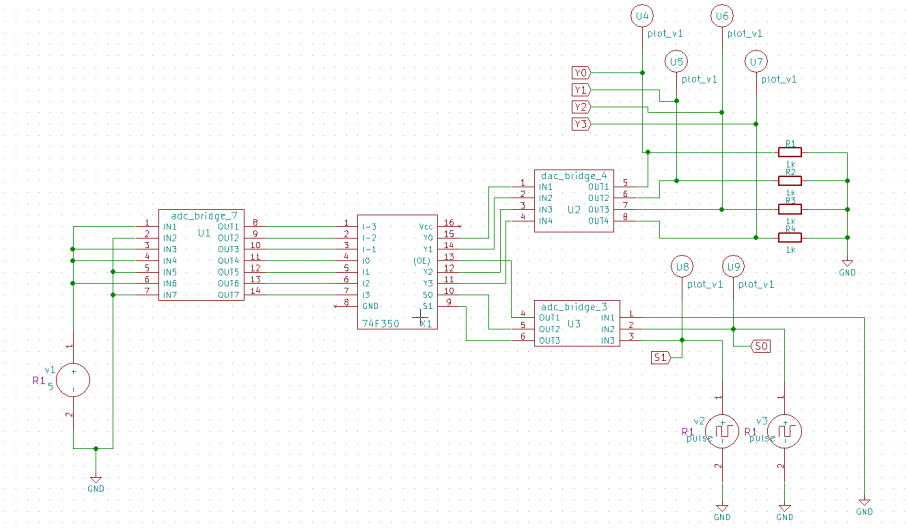




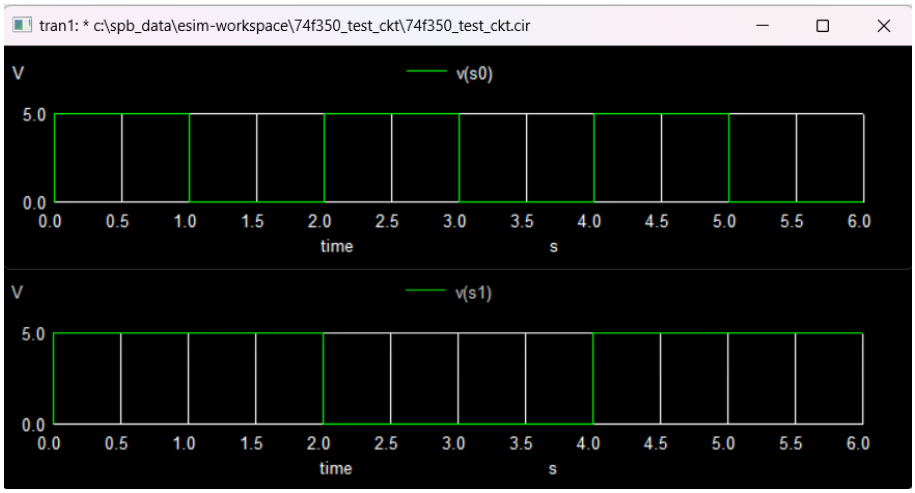
7.3 Subcircuit Schematic



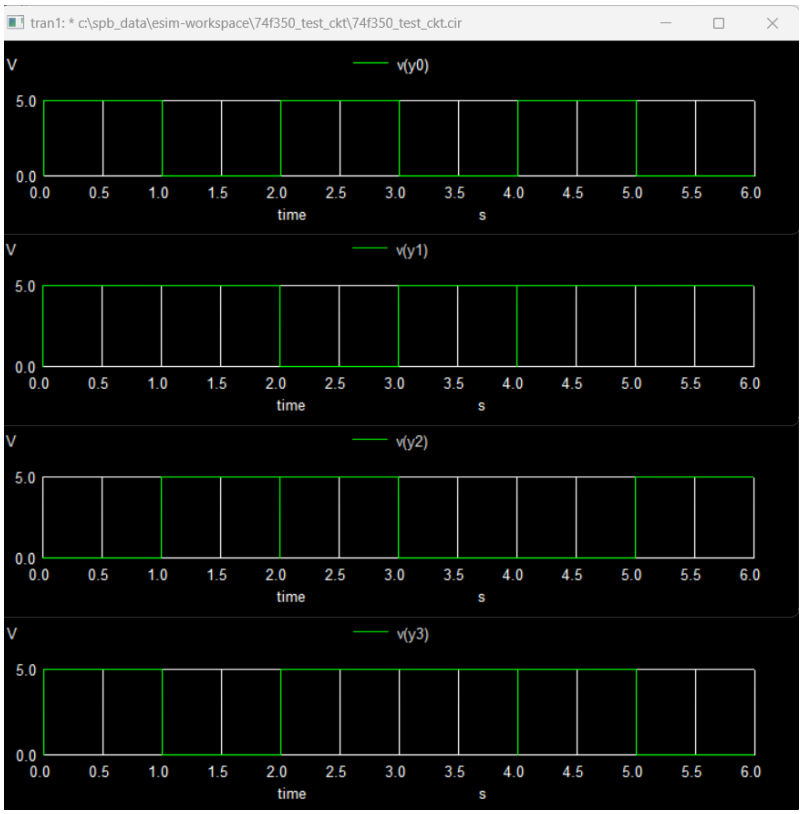
7.4 Test Circuit Schematic



7.5 Input Plots



7.6 Output Plots



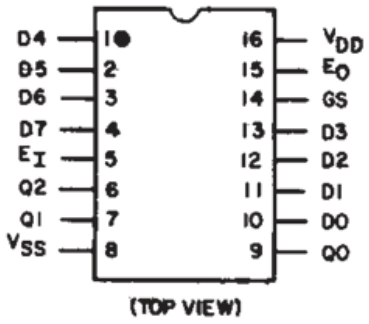
Chapter 8

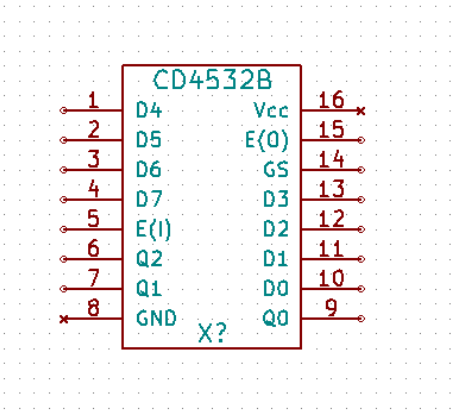
CD4532B

8.1 General Description

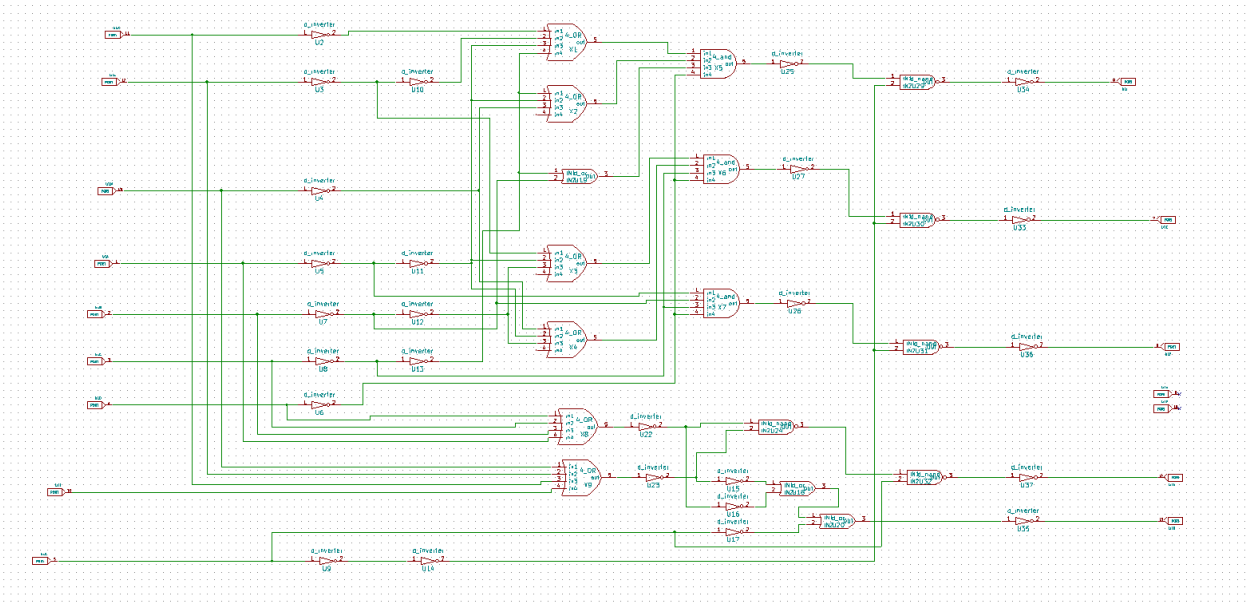
8 bit priority encoder
CD4532B consists of combinational logic that encodes the highest priority input (D7-DO) to a 3-bit binary code. The eight inputs, D7 through DO, each have an assigned priority; D7 is the highest priority and DO is the lowest. The priority encoder is inhibited when the chip-enable input E(i) is low. When E(i) is high, the binary representation of the highest-priority input appears on output lines Q2-Q0, and the group select line GS is high to indicate that priority inputs are present. The enable-out (EO) is high when no priority inputs are present. If any one input is high, Eo is low and all cascaded lower-order stages are disabled

8.2 Pin Diagram

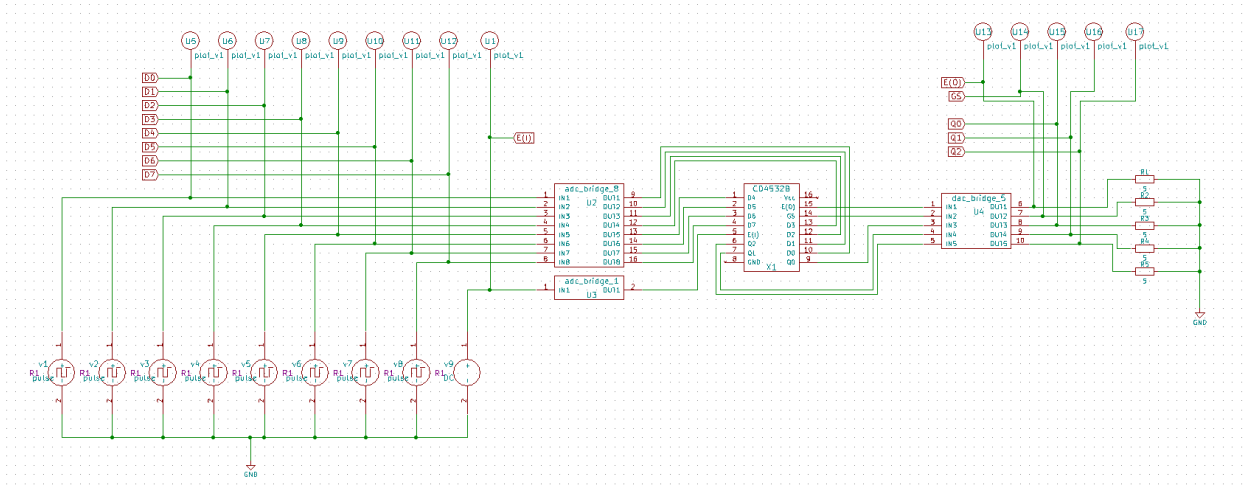




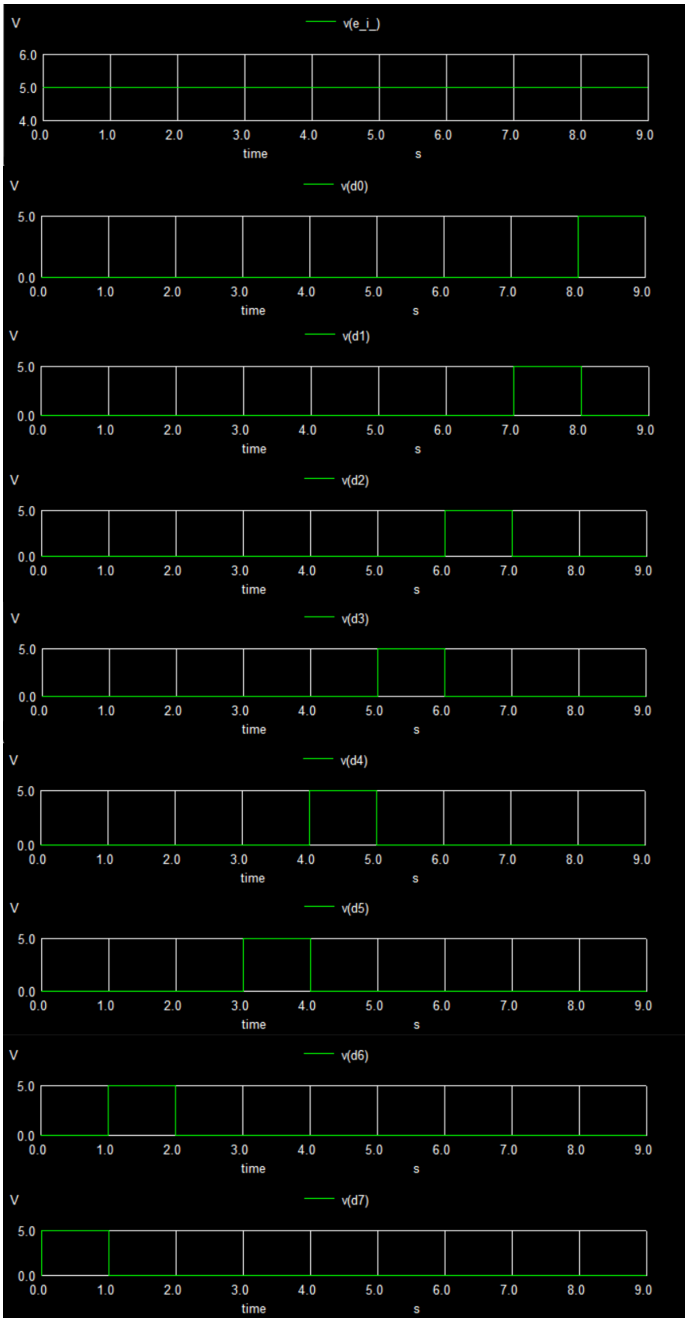
8.3 Subcircuit Schematic



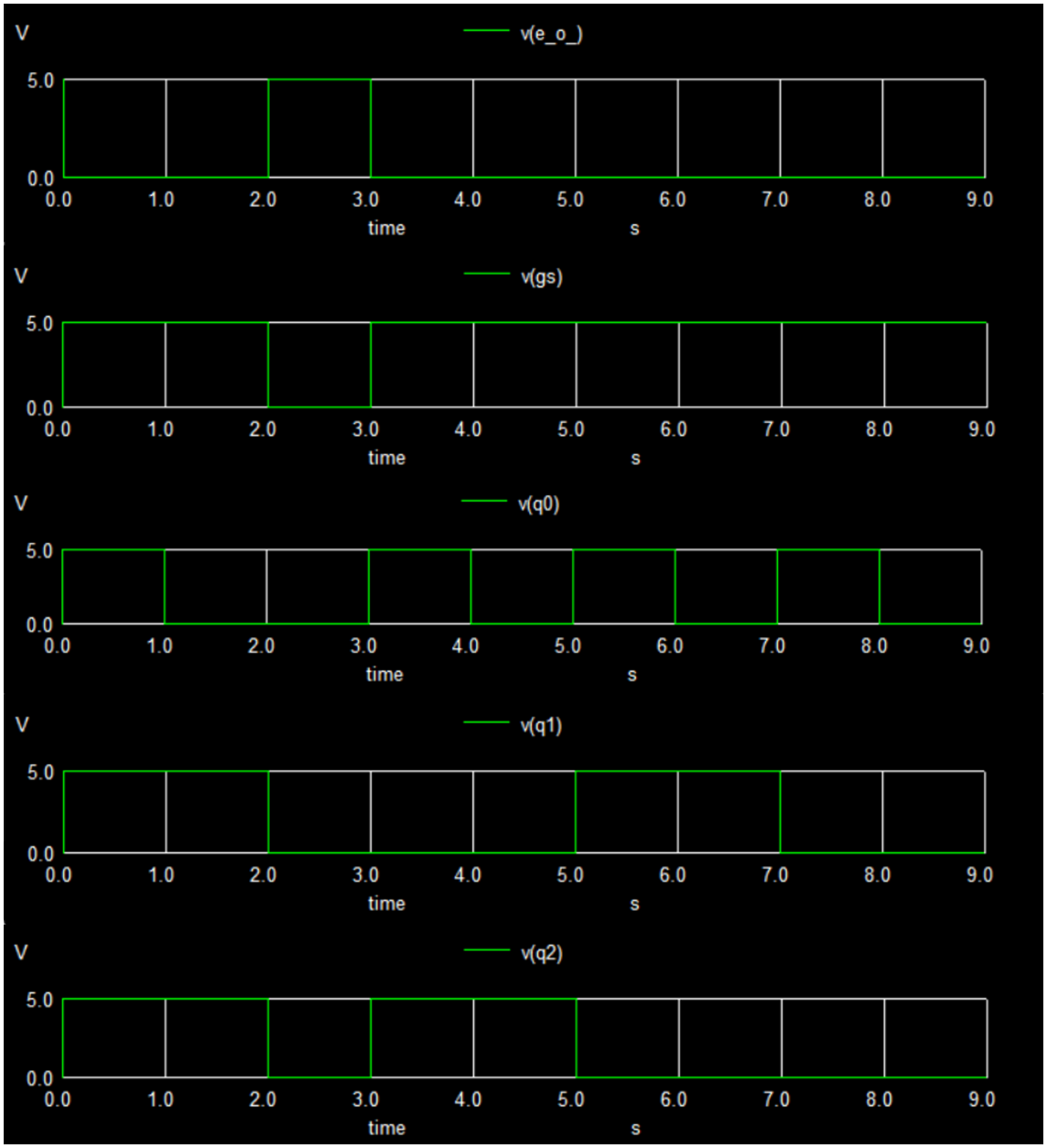
8.4 Test Circuit Schematic



8.5 Input Plots



8.6 Output Plots



Bibliography

[1] FOSSEE Official Website Click here to visit

[2] eSim Official Website Click here to visit

[3] Datasheet - SN74351 Click here to view

[4] Datasheet - SN54LS183 Click here to view

[5] Datasheet - HD74LS152 Click here to view

[6] Datasheet - SN54180 Click here to view

[7] Datasheet - 74F350 Click here to view

[8] Datasheet - CD4532B Click here to view