Semester Long Internship Report

On

Designing Integrated Circuit in eSim

Submitted by

Ashwini Kumar

Under the guidance of

Prof.Kannan M. Moudgalya
Chemical Engineering Department
IIT Bombay

June 30, 2024

Acknowledgment

I would like to express my sincerest gratitude to the entire FOSSEE team for providing me this golden opportunity to be part of their Semester Long Internship program. The experience of working with an open-source organization such as FOSSEE has been immensely informative. It has given me the opportunity to learn about the complexities of simulation programs like eSim and develop valuable problem-solving abilities. My sincere gratitude goes out to Prof. Kannan M. Moudgalya for his visionary leadership and commitment to the advancement of this project.

In addition, I want to express my gratitude to Mr. Sumanto Kar and Mrs. Usha Vishwanathan, who served as our mentors. Throughout my internship, their constant support and mentoring have been helpful. They were always there to offer advice and assist me in navigating through complexities so that I could find practical solutions whenever I ran into problems.

Overall, I had a great time interning with FOSSEE. My future will undoubtedly be shaped by the amazing thoughts and information I have learned. This internship is an important turning-point in my career aspirations as a professional in the semiconductor sector.

Contents

Chapter 1

Introduction

FOSSEE (Free/Libre and Open Source Software for Education) project promotes the use of FLOSS tools to improve the quality of education in our country. It aims to reduce dependency on proprietary software in educational institutions. It encourages the use of FLOSS tools through various activities to ensure commercial software is replaced by equivalent FLOSS tools. It also develops new FLOSS tools and upgrade existing tools to meet requirements in academia and research.[1]

The FOSSEE project is part of the National Mission on Education through Information and Communication Technology (ICT), Ministry of Human Resource Development (MHRD), Government of India.

eSim is a free/libre and open source EDA tool for circuit design, simulation, analysis and PCB design developed by FOSSEE, IIT Bombay. It is an integrated tool built using free/libre and open source software such as KiCad, Ngspice, NGHDL and GHDL.

Ngspice is a general purpose circuit simulation program for nonlinear dc, nonlinear transient, and linear ac analysis. Circuits may contain resistors, capacitors, inductors, mutual inductors, independent voltage and current sources, four types of dependent sources, lossless and lossy transmission lines (two separate implementations), switches, uniform distributed RC lines, and the five most common semiconductor devices: diodes, BJTs, JFETs, MESFETs, and MOSFET.

Makerchip is a platform that offers convenient and accessible access to various tools for digital circuit design. It provides both browser-based and desktop-based environments for coding, compiling, simulating, and debugging Verilog designs. Makerchip supports a combination of open-source tools and proprietary ones, ensuring a comprehensive range of capabilities.

Verilator is a tool which converts the Verilog files to C++ object. Before converting a verilog file in ngveri in eSim first the design is simulated here with random inputs to check whether the design is producing consistent and desired results. If the design is correctly simulated we proceed with our mixed signal design.

The objective of this internship is to design integrated circuits (IC) to be included in eSim as subcircuit library components. To design IC's, certain tools of eSim would be used like KiCAD to NGSpice convertor and verilog code to NGSpice convertor. This will enable users to simulate and use the IC in designing other complex circuit.

Chapter 2

IC HT12E

Design integrated circuit IC HT12E subcircuit in eSim.

2.1 Circuit Details

The HT12E encodes the 12-bit input data (8 bits address and 4 bits data) into a serial output. This encoded data is then transmitted over a communication channel, typically RF (Radio Frequency) or infrared (IR), to the corresponding decoder IC (HT12D). The HT12E encodes the 12-bit data into a serial bit stream. The encoded serial data is output through the DOUT pin, ready to be transmitted via an RF or IR transmitter module.

2.2 Pin Diagram

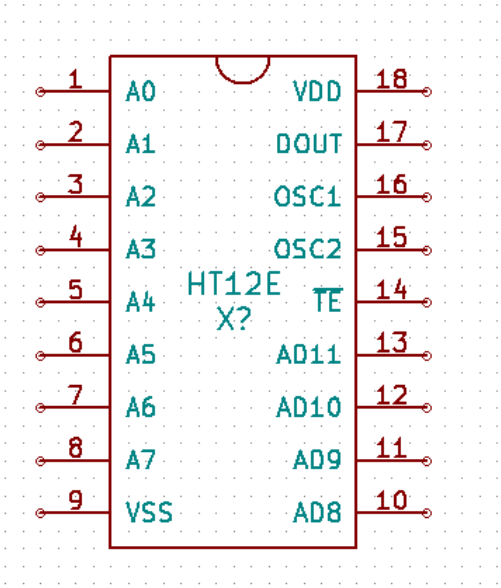

Figure 2.1: The HT12E comes in an 18-pin DIP (Dual Inline Package) configuration

A0 to A7 Address input pins are used to set the address of the encoder. The address must match the address set on the corresponding HT12D decoder for successful communication.
Dout Data output pin output the serial encoded data.
TE Transmission enable pin is pulled low for the HT12E begins to transmit the data.
D11 to D8 Data input pins are used to input the data to be encoded and transmitted.

2.3 Schematic Diagram

Firstly the data is loaded into PISO shift register using pin ld. A clock pulse is input to the clk0 pin PISO shift register. A constant 8 bit address data and 4 bit data is input to address pins and data pins respectively. The output is 1 bit serial data output.

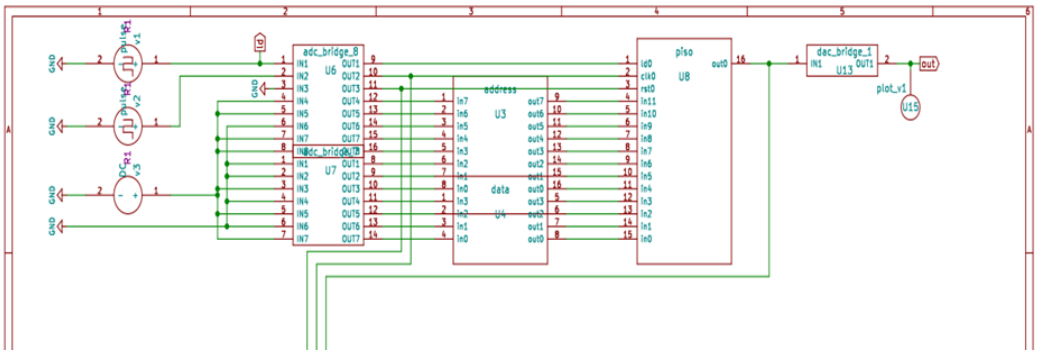

Figure 2.2: The HT12E circuit schematic diagram

2.4 Verilog Code

The verilog code of PISO Shift register used in the above schematic to design component PISO

```
1  module PISO (in, ld, clk, rst, out);
2    input ld,  clk, rst;
3    input [11:0] in;
4    output out;
5    reg [11:0] qq;
6    assign out=qq[0];
7    always @ (posedge clk, posedge rst)
8      begin
9        if(rst)
10         qq<=0;
```

```
11        else if(ld)
12          qq<=in;
13        else
14          qq<={1'b0,qq[11:1]};
15      end
16  endmodule
```

2.5 Simulation Output

For simulation testing address bit is 8b11011001 and data bit is 4b0101. Combining both the 12-bit data is 12b110110010101

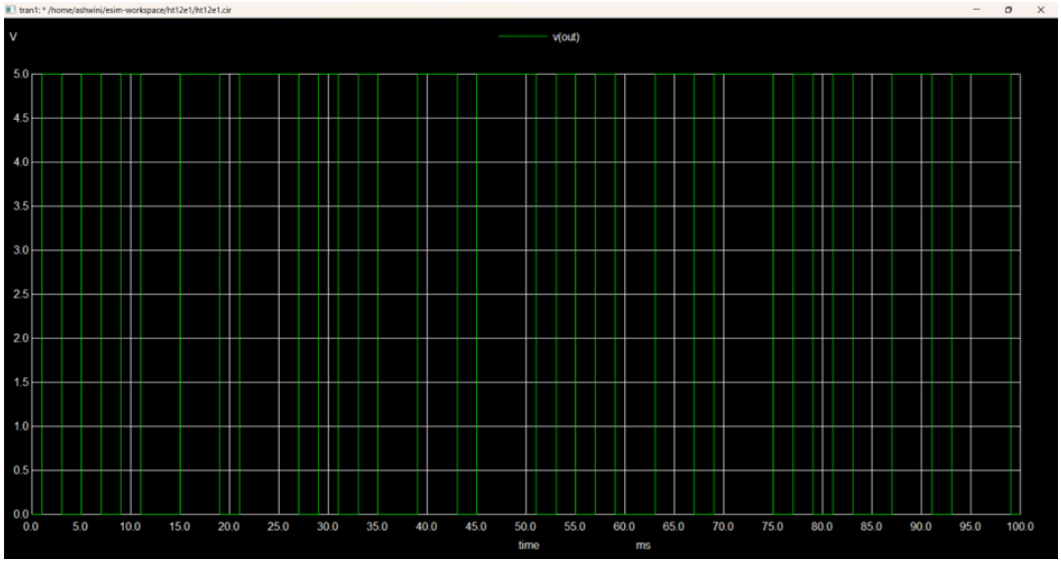

Figure 2.3: The HT12E serial output plot

Chapter 3

IC HT12D

Design integrated circuit IC HT12D subcircuit in eSim.

3.1 Circuit Details

The HT12D is a decoder IC commonly used in remote control systems alongside the HT12E encoder IC. It is part of the same Holtek HT12 series and is designed to decode the data transmitted by the HT12E.The HT12D decodes the 12-bit serial data transmitted by the HT12E encoder. The data consists of 8 address bits and 4 data bits. The decoder checks the received address against its own address setting. If the addresses match, it outputs the received data on the data pins and sets the VT pin high to indicate valid data reception.

3.2 Pin Diagram

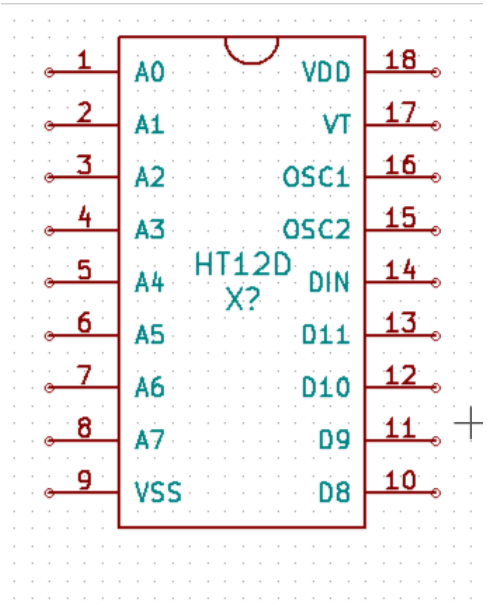

Figure 3.1: The HT12D comes in an 18-pin DIP (Dual Inline Package) configuration

A0 to A7 Address input pins are used to set the address of the encoder. The address must match the address set on the corresponding HT12D decoder for successful communication.
Din Data input pin receives the serial data from the transmitter
VT Valid transmission pin. This pin goes high when valid data is received.
D11 to D8 Data output pins. These pins provide the decoded parallel data.

3.3 Circuit Schematic

Serial Output from HT12D is input to SIPO Shift Register. The Parallel Output is send to split data component of IC where the address is matched with input address to HT12D. If both address found to be equal then the data is obtained at the output of IC.

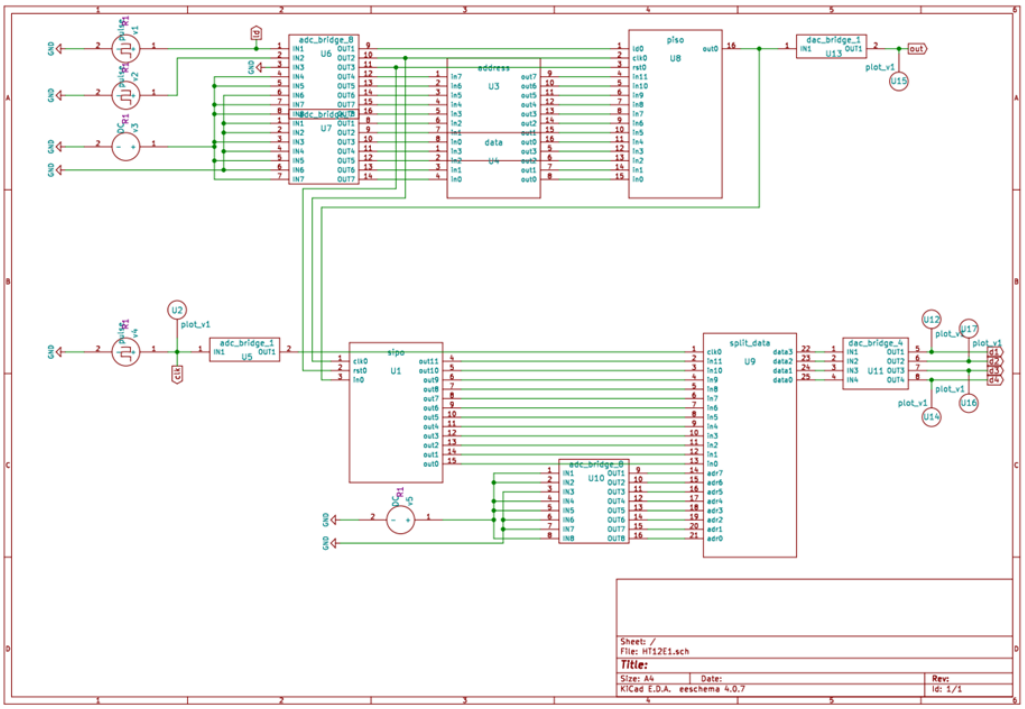

Figure 3.2: The HT12D circuit schematic diagram

3.4 Verilog Code

3.4.1 Verilog Code for SIPO

```
1  module SIPO (in, clk, rst, out);
2    input clk, rst;
3    input in;
4    output reg [11:0] out;
5    always @ (posedge clk, posedge rst)
6      begin
7        if(rst)
8          out<=0;
9        else
10         out<={in,out[11:1]};
11     end
12 endmodule
```

3.4.2 Verilog Code for split_data

Verilog Code for split_data subcircuit created using ngveri

```
1  module split_data (in, adr, clk, data);
2    input clk;
```

```
3     input [11:0] in;
4     input [7:0] adr;
5     output reg [3:0] data;
6     reg [7:0] temp_adr;
7     reg [3:0] temp_data;
8     assign temp_adr=in[11:4];
9     assign temp_data=in[3:0];
10    always @ (negedge clk)
11      begin
12        if(adr==temp_adr)
13          data <= temp_data;
14        else
15          data <=8'd0;
16      end
17  endmodule
```

3.5 Simulation output

3.5.1 When address pin Matches

Input HT12E For simulation testing address bit is 8b11011001 and data bit is 4b0101. Combining both the 12 bit data is 12b110110010101.

Input at HT12D address bit is 8b11011001.

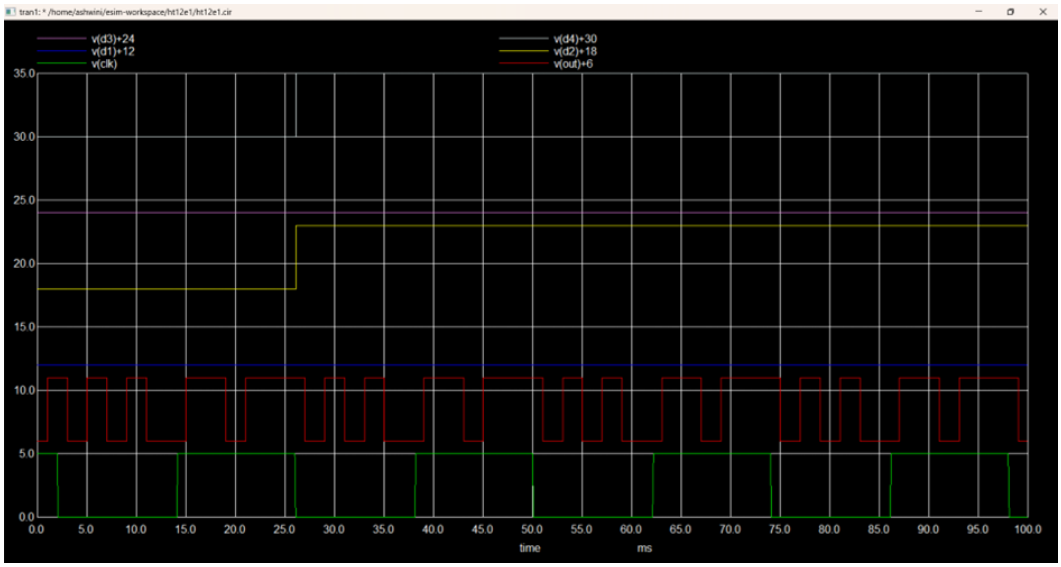

Figure 3.3: The HT12D and HT12E output plots when address pin match

plot 1 (Top) Digital Data Output D3.
plot 2 Digital Data Output D2.

plot 3 Digital Data Output D1.
plot 4 Digital Data Output D0.
plot 5 Serial Output from HT12E
plot 6 (bottom) Clock input

3.5.2 When address pin does not matches

Input HT12E For simulation testing address bit is 8b11011001 and data bit is 4b0101. Combining both the 12 bit data is 12b110110010101.

Input at HT12D address bit is 8b11011101.

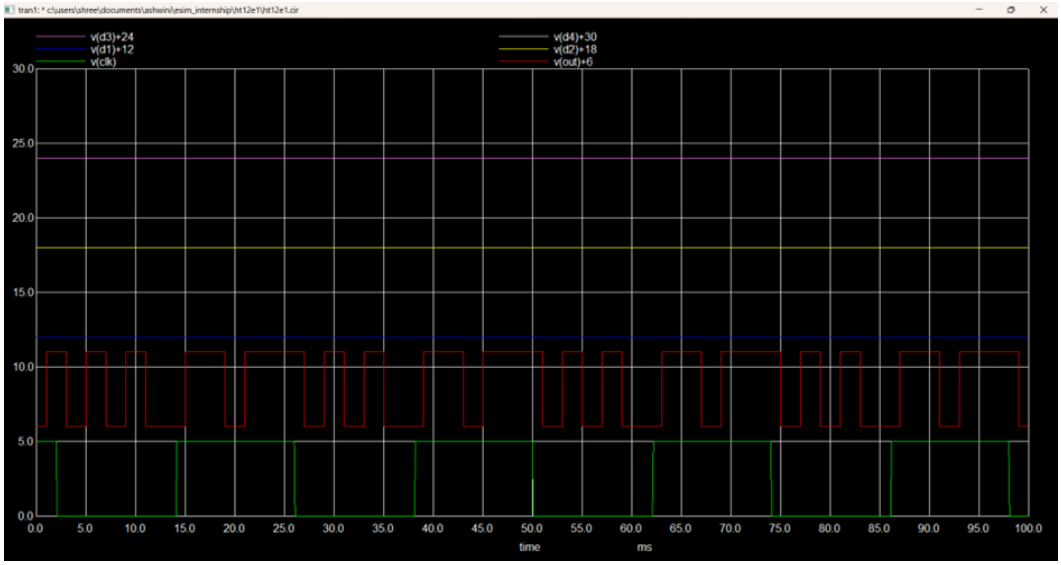

Figure 3.4: The HT12D and HT12E output plots when address pin not match

plot 1 (Top) Digital Data Output D3.
plot 2 Digital Data Output D2.
plot 3 Digital Data Output D1.
plot 4 Digital Data Output D0.
plot 5 Serial Output from HT12E
plot 6 (bottom) Clock input

Chapter 4

IC LF298

Design integrated circuit IC LF298 subcircuit in eSim.

4.1 Circuit Details

The LF298 is a sample and hold amplifier IC used in analog circuits to capture (sample) an analog signal and hold it for a specified period. This is essential in analog to digital conversion systems, data acquisition systems, and other applications where an analog signal needs to be maintained for processing. The LF298 typically comes in an 8-pin Dual Inline Package configuration.

The LF298 functions by sampling an analog input signal when the control pin is activated. The sampled voltage is stored on an external capacitor connected to the hold capacitor pin. When the control signal is deactivated, the voltage on the hold capacitor is maintained and can be read from the output pin.

4.2 Pin Diagram

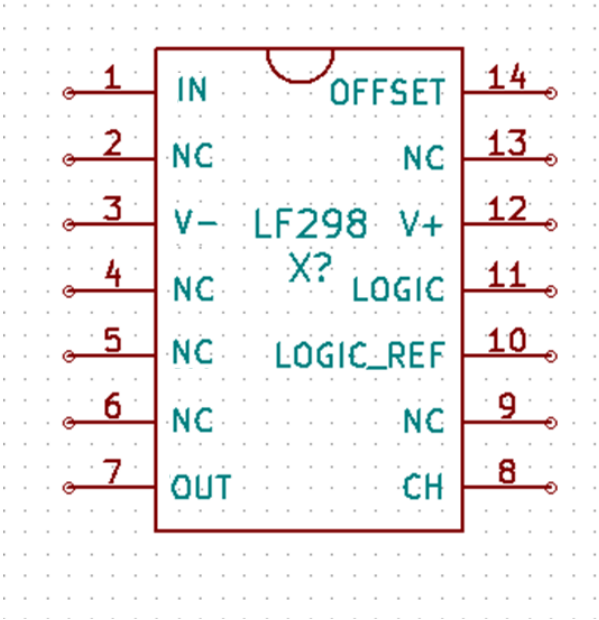

Figure 4.1: The IC LF298 comes in an 14-pin DIP (Dual Inline Package) configuration

IN Input pin. The analog signal to be sampled is applied to this pin.
CH Holding Capacitor pin. A capacitor connected to this pin holds the sampled voltage.
LOGIC Logic input for Sample and Hold modes.
LOGIC REF Reference for LOGIC input
OFFSET DC offset compensation pin
OUT Output pin. The held sample voltage is output from this pin.

4.3 Circuit Schematic

In the IN pin, a sinusoidal wave is given. The Holding capacitor is 0.5 uF connected to CH. A pulse or square wave is given as input to the LOGIC pin. LOGIC REF pin is kept half of voltage as that of LOGIC pin. This can be done using voltage divider. The OFFEST pin is grounded. The output of sample and hold circuit is analysed at the OUT pin.

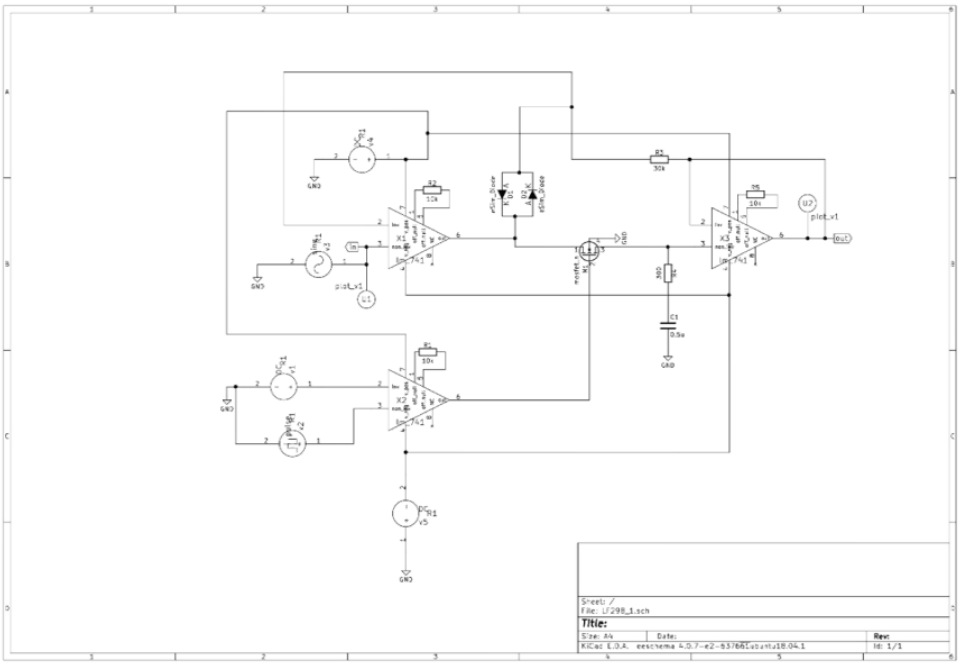

Figure 4.2: IC LF298 Circuit Schematic Diagram

4.4 Simulation output

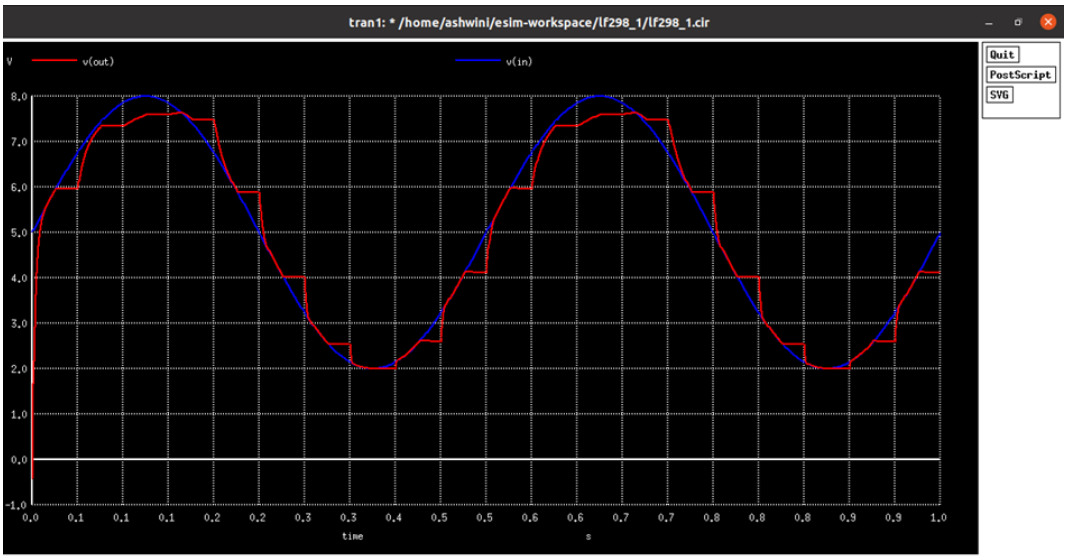

Figure 4.3: IC LF298 Circuit Simulation output plot

vout (Top) Sampled and hold output plot.
vin 2 input sine wave plot to be sampled.

Chapter 5

IC 74LS56

Design integrated circuit IC 74LS56 subcircuit in eSim.

5.1 Circuit Details

A 100:1 frequency divider is a circuit that reduces the frequency of an input signal by a factor of 100. This means if you input a signal with a frequency of 100 kHz, the output will be 1 kHz. Frequency dividers are essential in digital electronics for clock generation, timing, and signal processing.

5.2 Pin Diagram

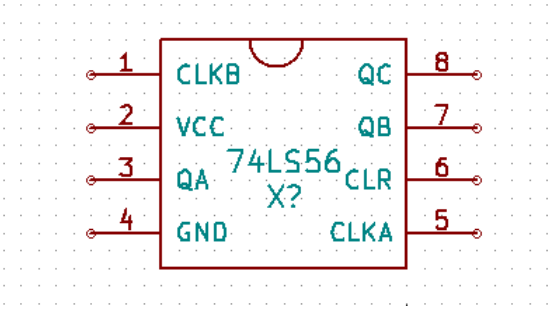

Figure 5.1: The IC 74LS56 comes in an 8-pin DIP (Dual Inline Package) configuration

CLKA Clock input for A component of IC
CLKB Clock input for B component of IC.
QA output is high when count of clock A is 5.
QB output of clock Frequency divider 5:1
QC output of clock Frequency divider 100:1

5.3 Circuit Schematic 5:1 Frequency Divider

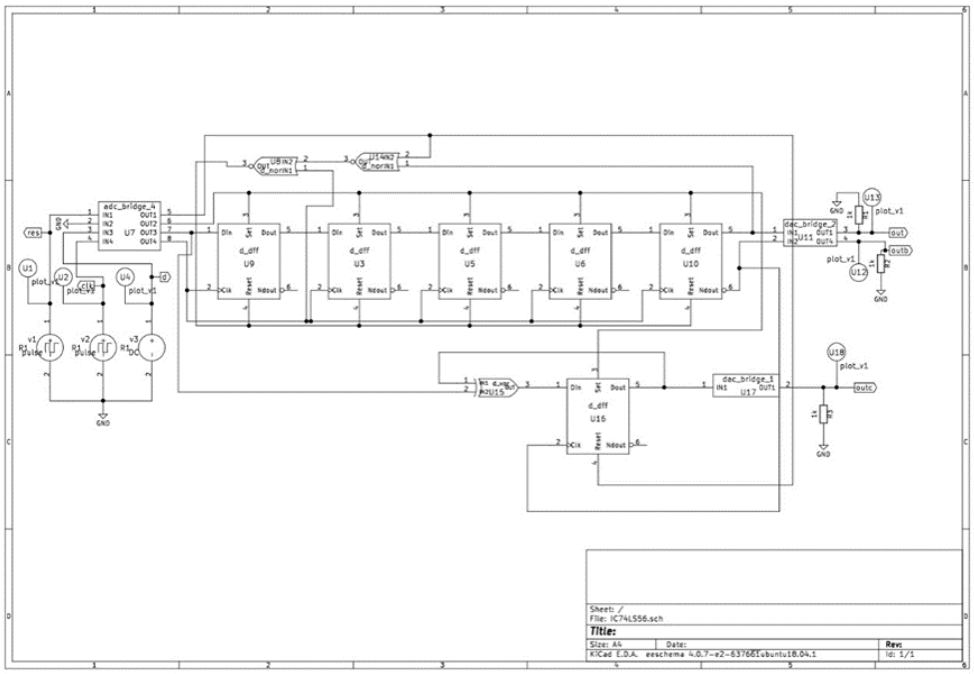

Figure 5.2: Circuit Schematic diagram 5:1 Frequency Divider using flip-flops

5.4 Verilog Code D Flip Flop

```
1  module d_dff(Din,Clk,Reset,Set,Dout,Ndout);
2  input Din, Clk, Set, Reset;
3  output reg Dout, Ndout;
4    always @ (posedge Clk)
5      begin
6        if (Reset == 1)
7          begin
8            Dout <= 0;
9            Ndout <= 1;
10         end
11       else if (Set == 1)
12         begin
13           Dout <= 1;
14           Ndout <= 0;
15         end
16       else
17         begin
18           Dout <= Din;
19           Ndout = !Din;
```

```
20          end
21      end
22  endmodule
```

5.5 Simulation output 5:1 Frequency Divider

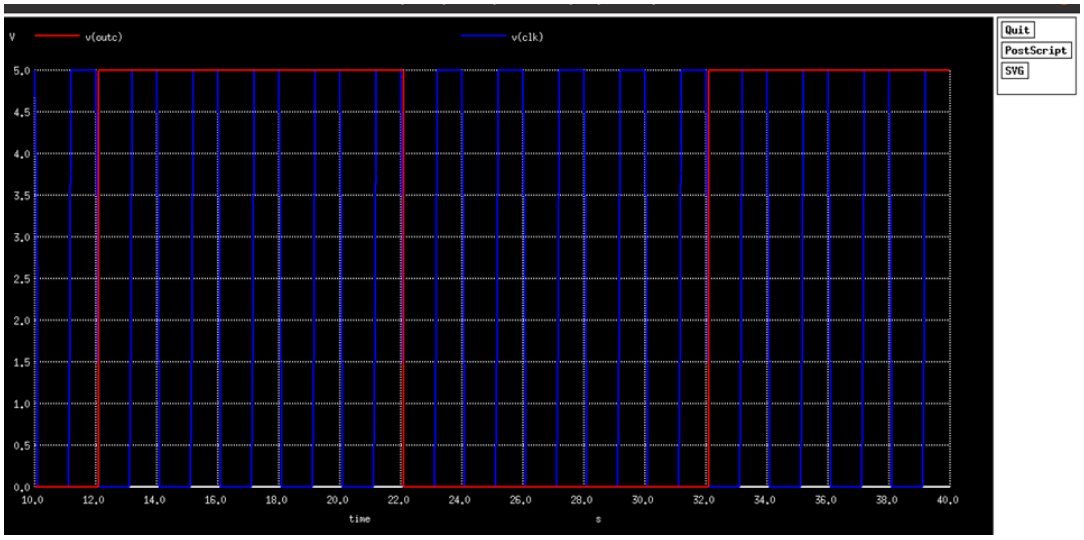

Figure 5.3: Output plot of 5:1 frequency divider

5.6 Circuit Schematic IC 74LS56

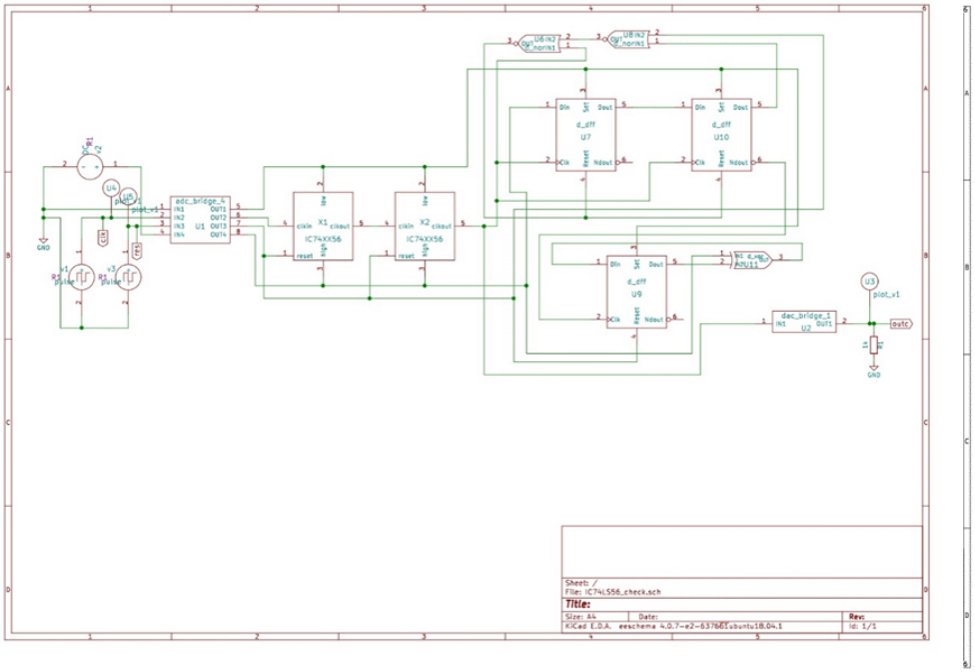

Figure 5.4: Circuit Schematic diagram 5:1 Frequency Divider using flip-flops

5.7 Simulation output IC 74LS56

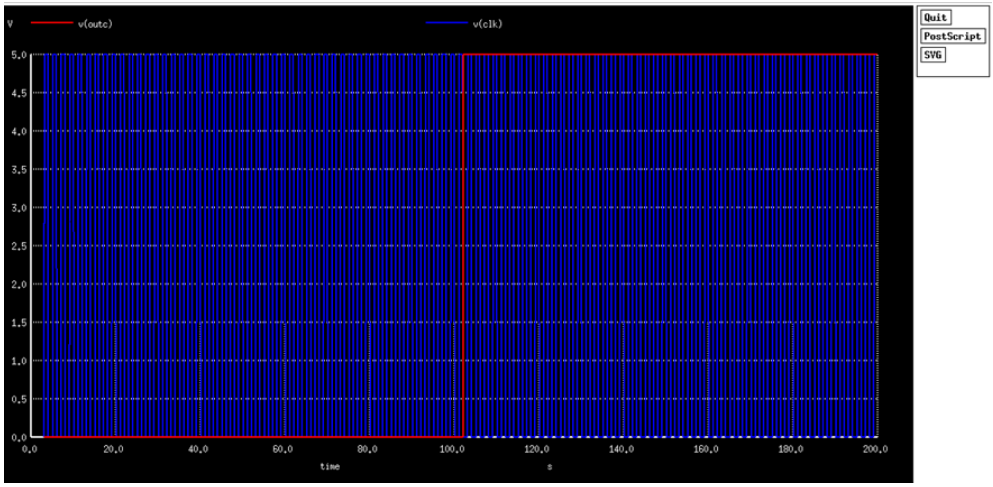

Figure 5.5: Output plot of 100 : 1 frequency divider

Chapter 6

IC 7481A

Design integrated circuit IC 7481A subcircuit in eSim.

6.1 Circuit Details

The 7481A is a 16-bit RAM (Random Access Memory) chip. It is a part of the TTL (Transistor-Transistor Logic) series of integrated circuits, commonly used in digital systems for small memory applications. It provides 16 bits of storage, organized as 16 words by 1 bits each. Address input pins (A0, A1, A2, A3) for selecting one of the 16 memory locations. Data input/output pins (D0, D1, D2, D3) for reading from or writing to the memory.

6.2 Pin Diagram

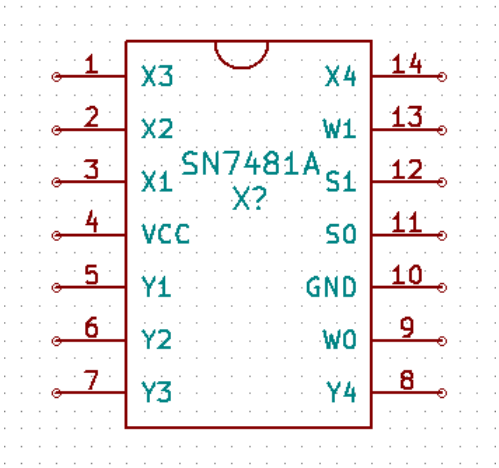

Figure 6.1: The IC 7481A comes in an 14-pin DIP (Dual Inline Package) configuration

X4 to X1 4 bit input pins for selecting row
Y4 to Y1 4 bit input pins for selecting column
W1 and W0 write 1 bit data to row and column selected

S1 and S0 sense 1 bit data of row and column selected

6.3 Circuit Schematic IC 7481A

For testing the circuit, A single address is choosen. The input to X is 4b0001 and input to Y is 4b0001. Now, firstly 1b0 data is input to memory address at X row and Y column using W. Then the data is sensed at memory address at X row and Y column. The data obtain at S0 should be HIGH. Now, 1b1 data is input to memory address at X row and Y column using W. Then the data is sensed at memory address at X row and Y column. The data obtain at S1 should be HIGH.

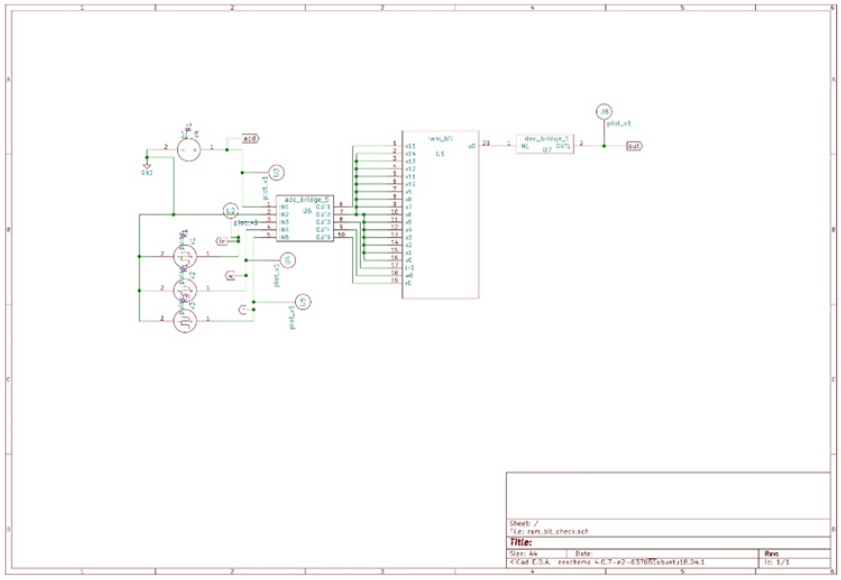

Figure 6.2: Circuit Schematic diagram of IC 7481A

6.4 Verilog Code

```
1  module ram_bit (x, in ,w , r, o );
2    input [15:0] x;
3    input in;
4    input w;
5    input r;
6    output reg o;
7    reg s[15:0];
8    always @ (in, w, r)
9      begin
10       if (w==1'b1)
11         begin
```

```
12              s [x] <= in;
13            end
14          if (r==1'b1)
15            begin
16              o <= s [x];
17            end
18        end
19  endmodule
```

6.5 Simulation output IC 7481A

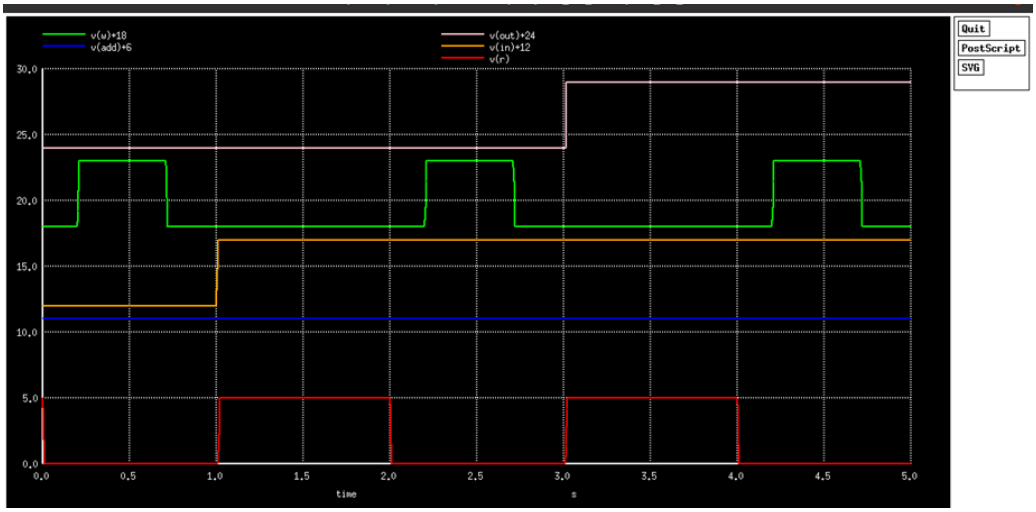

Figure 6.3: Simulation output plot of IC 7481A

plot 1 (Top) Data output of cell or stored data in cell.
plot 2 Write data to cell
plot 3 Data input to cell
plot 4 address of cell choosed to read and write data
plot 5 (bottom) Read data from cell

Chapter 7

IC LM566

Design integrated circuit IC LM566 subcircuit in eSim.

7.1 Circuit Details

The NE566 is a voltage-controlled oscillator (VCO) integrated circuit that can generate a wide range of frequencies with a variable control voltage. It is widely used in signal generation, function generators, and frequency modulation applications.

Capable of generating frequencies from below 1 Hz to over 1 MHz. The NE566 operates as a VCO by charging and discharging the external timing capacitor through the external timing resistor. The rate of charge and discharge determines the frequency of oscillation. The control voltage applied to the modulation input pin (Pin 3) adjusts the charging rate, thereby varying the frequency.

Its ability to produce both square and triangular waveforms, along with easy frequency modulation through a control voltage, makes it suitable for various applications in signal generation, modulation, and function generation.

7.2 Pin Diagram

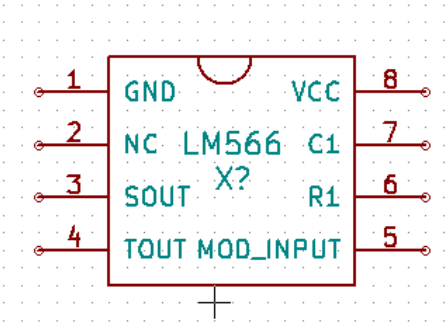

Figure 7.1: The LM566 comes in an 8-pin DIP (Dual Inline Package) configuration

C1 Capacitor connection pin for adjusting frequency of free running oscillation wave
R1 Resistance connection pin for adjusting frequency of free running oscillation wave
MOD INPUT Modulating signal input pin.
TOUT triangular wave output pin
SOUT square wave output pin

7.3 Circuit Schematic

Connect the positive supply voltage (+12V) to pin 8 of the NE566N. Connect the negative supply voltage (-12V) to pin 4 of the NE566N. Connect the ground to pin 3 of the NE566N. Connect a resistor (R1) between pin 6 and pin 7. This resistor, along with the capacitor, sets the basic frequency of the VCO. Connect a capacitor (C1) between pin 5 and ground. This capacitor works with R1 to determine the frequency range of the VCO. The control voltage input that varies the frequency is applied to pin 5. In this case, you will connect the output of your sine wave generator to pin 5. The square wave output can be taken from pin 3. You can connect this pin to an oscilloscope or other circuitry to observe the square wave whose frequency varies with the sine wave.

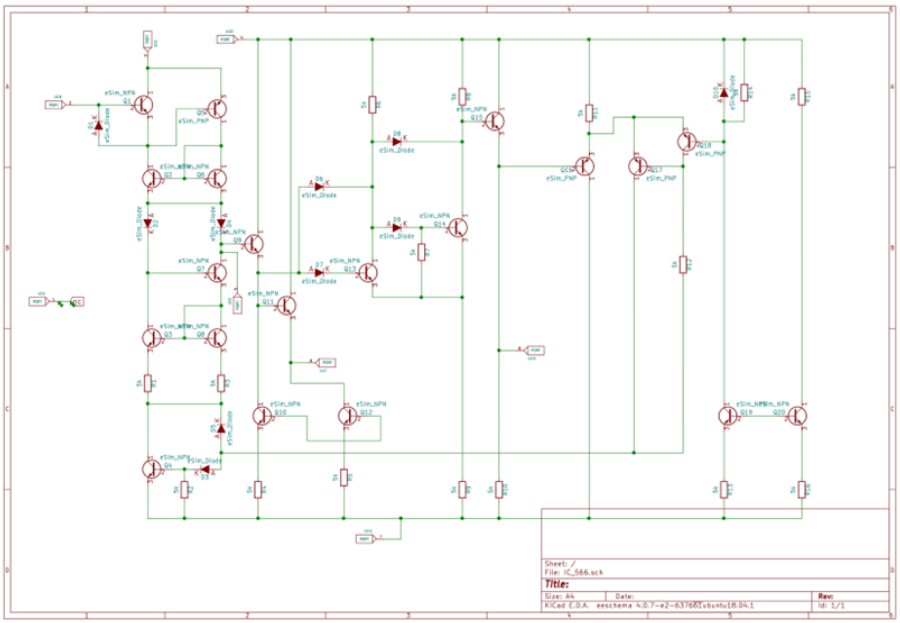

Figure 7.2: Subcircuit diagram of LM566 VCO IC

7.4 Simulation output

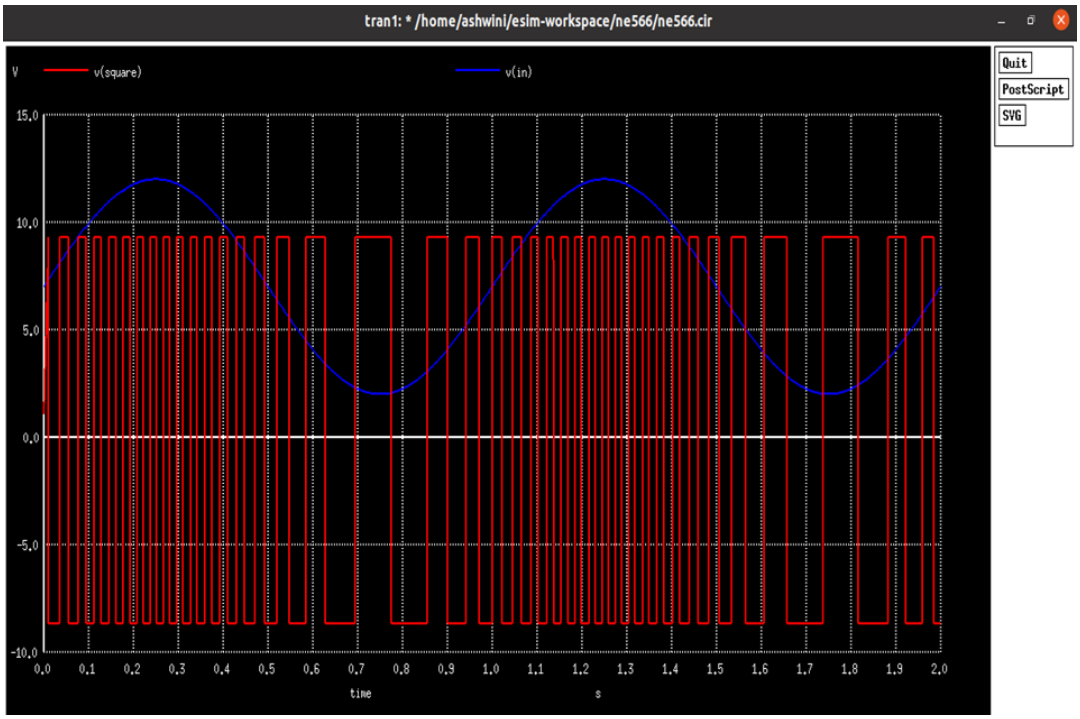

Figure 7.3: Simulation output plot of LM566 voltage controlled oscillator

Chapter 8

Research Migration Project

Research Migration Project is an initiative of FOSSEE that promotes and facilitates the usage of eSim for circuit design and analysis. In this particular initiative, their focus is to create a resource database in the field of circuit design using eSim. .

8.1 Abstract

This project focuses on two prominent modeling techniques for switch mode DC/DC power converters: between (a) the average model and (b) the switched model. The general case of the regular model uses the constant changing of the voltages or currents to that of the average switched model, which applies them for the fractional part of the commutation period. Here I will look into the switched model technique and its application in integrating power switches layout. The simulation model is designed using eSim simulation software, which acts as a powerful environment for circuit simulations and analysis. eSim being the link between the abstract circuit design and the practical implementation, the designers can shortcut the design process. Modelling and simulation methods will be applied on popular control PWM Integrated Circuits UC 1525 and UC 1846. Different elements, including the oscillator, error amplifier, and comparator are designed and simulated with subcircuits.

8.2 Circuit Schematic

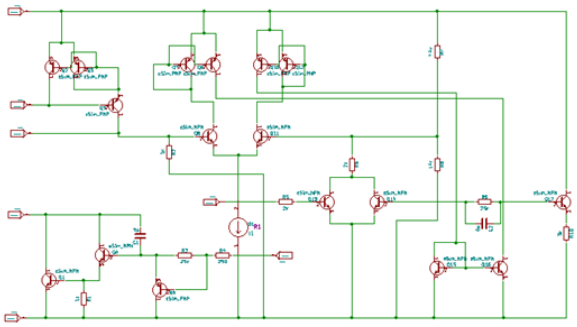

Figure 8.1: Circuit Schematic UC1525 subcircuit oscillator

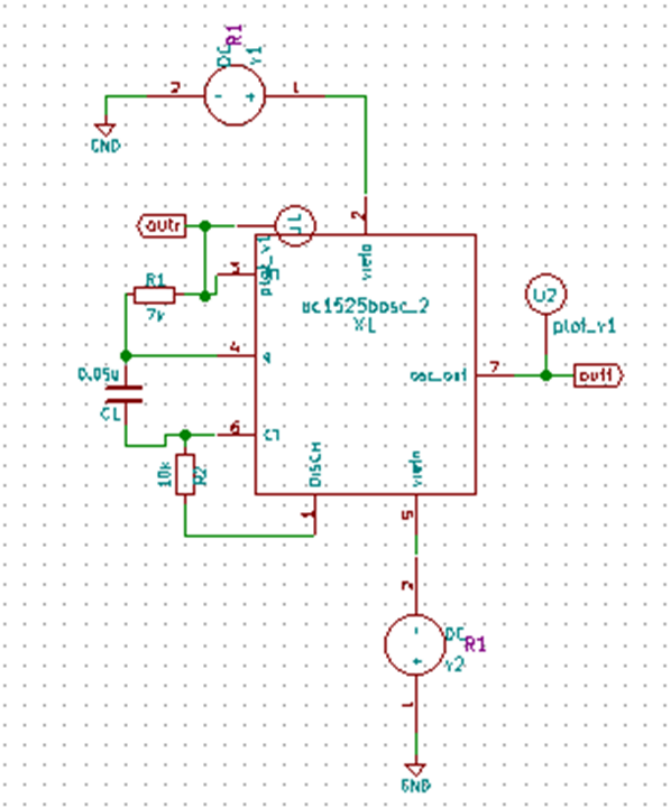

Figure 8.2: Circuit Schematic UC1525 oscillator

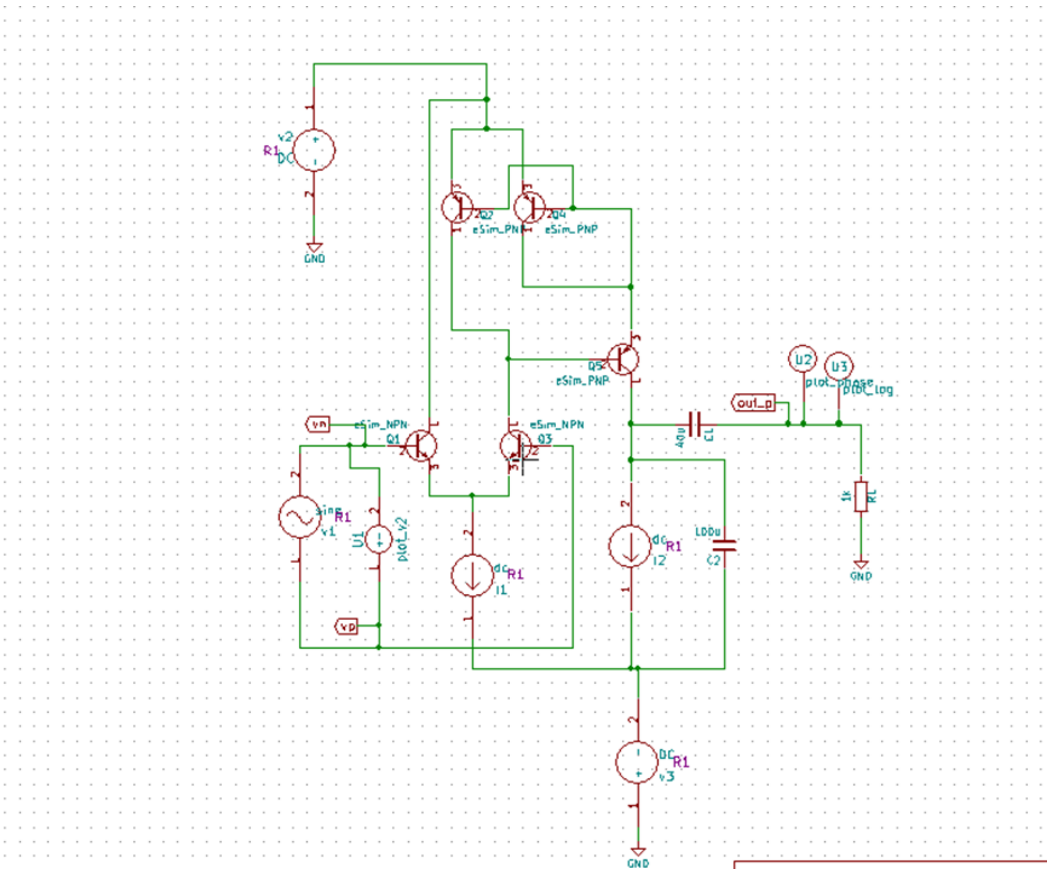

Figure 8.3: Circuit Schematic UC1525 error amplifier

8.3 Simulation output

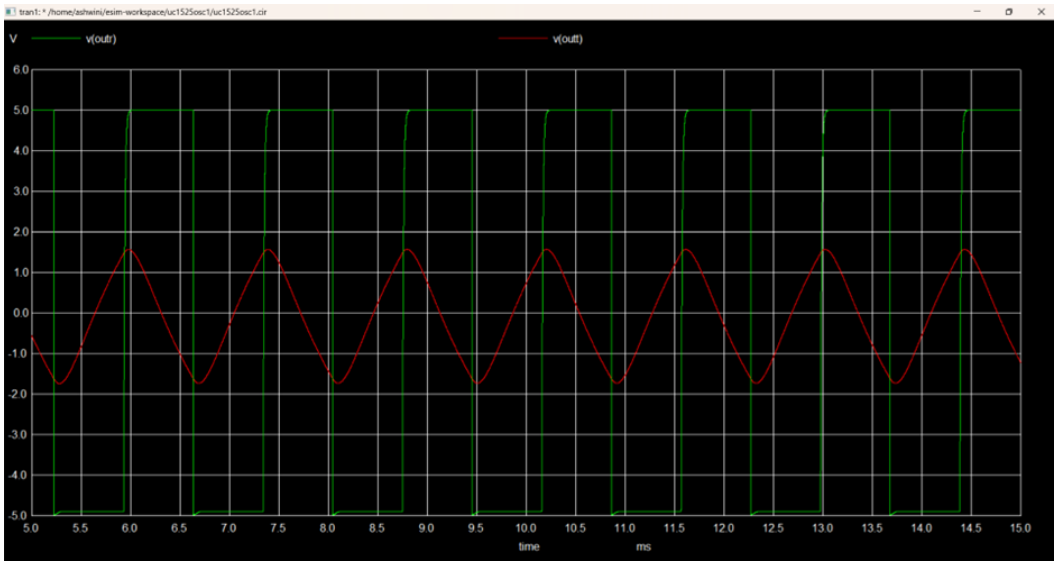

Figure 8.4: Simulation output plot of UC1525 oscillator

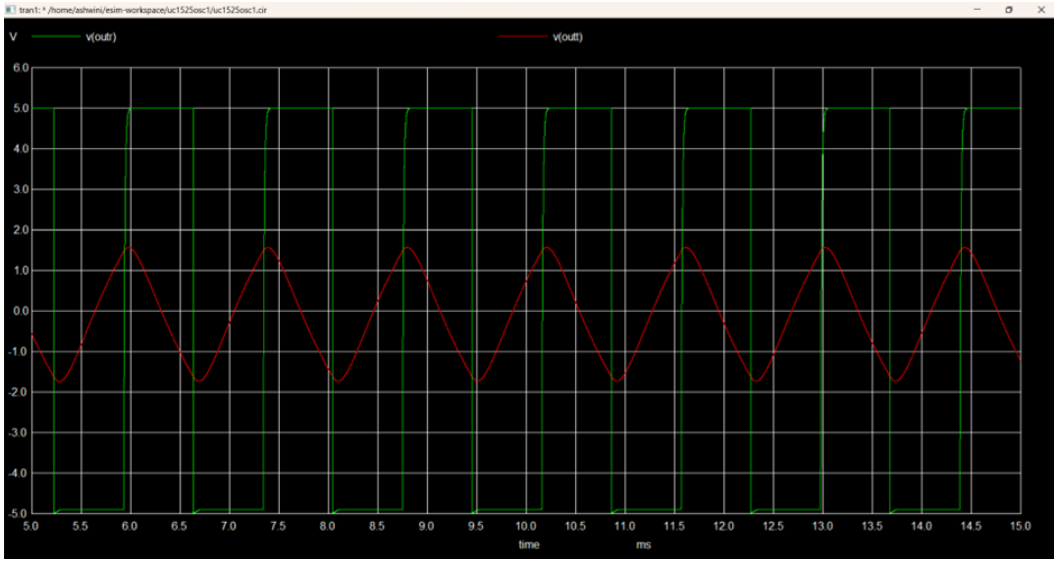

Figure 8.5: Simulation output plot of UC1525 error amplifier

Chapter 9

IC LM134

Design integrated circuit IC LM134 subcircuit in eSim.

9.1 Circuit Details

The LM134 is a versatile 3-terminal adjustable current source that can be used for current regulation in various applications. It is designed to operate over a wide range of voltages and is capable of providing a constant current regardless of supply voltage variations.

The output current can be adjusted over a wide range by changing an external resistor.It provides precise current regulation. It can operate from 1V to 40V. The LM134 operates by maintaining a constant voltage difference (about 18mV) across an external resistor (Rset)

9.2 Pin Diagram

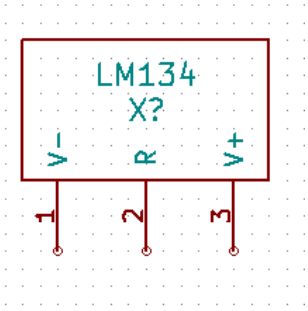

Figure 9.1: The LM134 comes in an 3-pin transistor like configuration

V− negative power input for the IC
R Resistance connection to adjusted current value of the source

V + Constant DC voltage source input

9.3 Current Variation to Change in Resistance

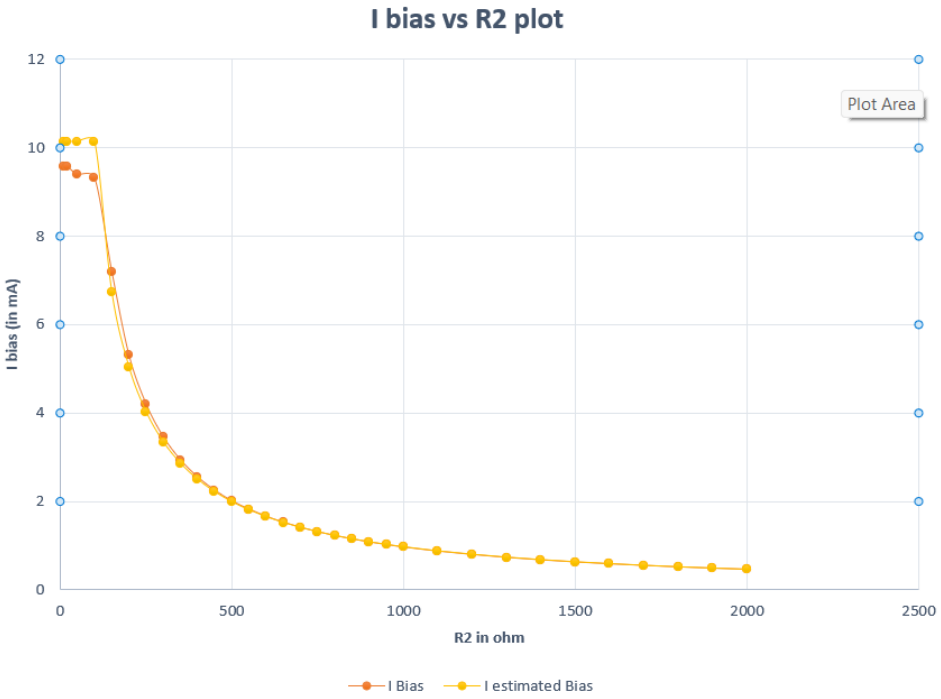

Figure 9.2: I bias vs Resistance R2 plot in IC LM134

9.4 Circuit Schematic

To test the constant current source circuit working, capacitor of 100uF is connected in series with the current source. Now a NPN transistor is used which act as a switch to charge and discharge the capacitor using the square wave pulse in the base terminal. When the base terminal voltage is high, the capacitor discharge to around 0.2 V. When the base terminal voltage is LOW, the capacitor is charged with constant current which will increase the voltage across capacitor linearly. This continous charging and discharging lead to generation of sawtooth wave across capacitor.

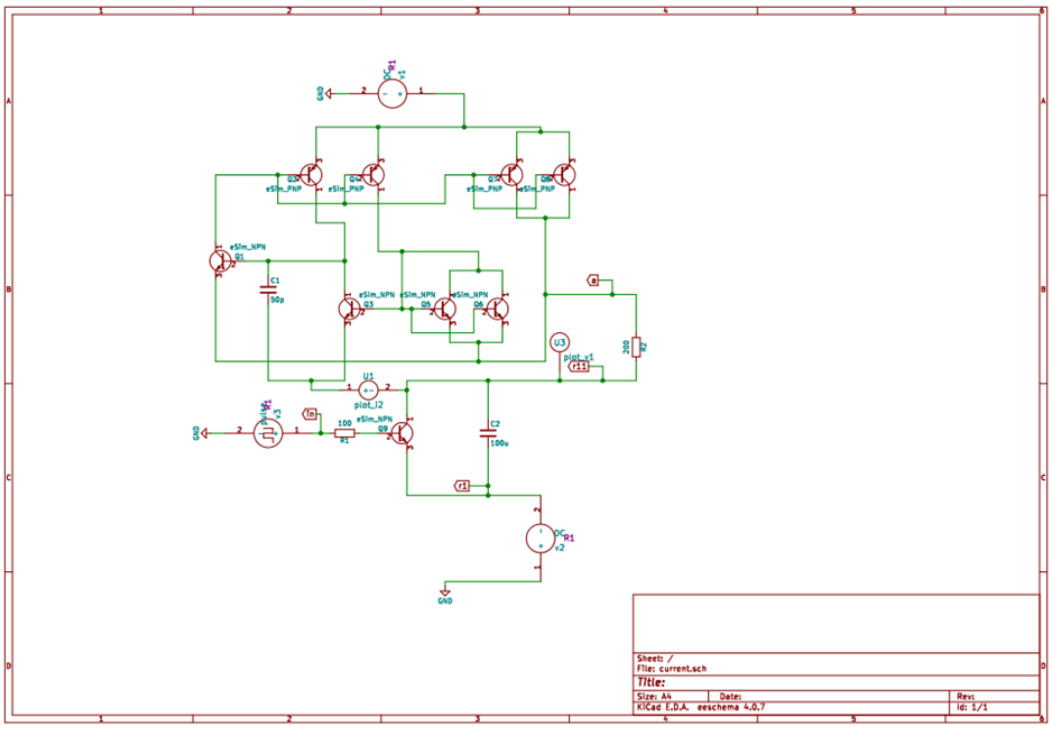

Figure 9.3: Circuit Schematic Diagram of LM134 IC

9.5 Simulation output

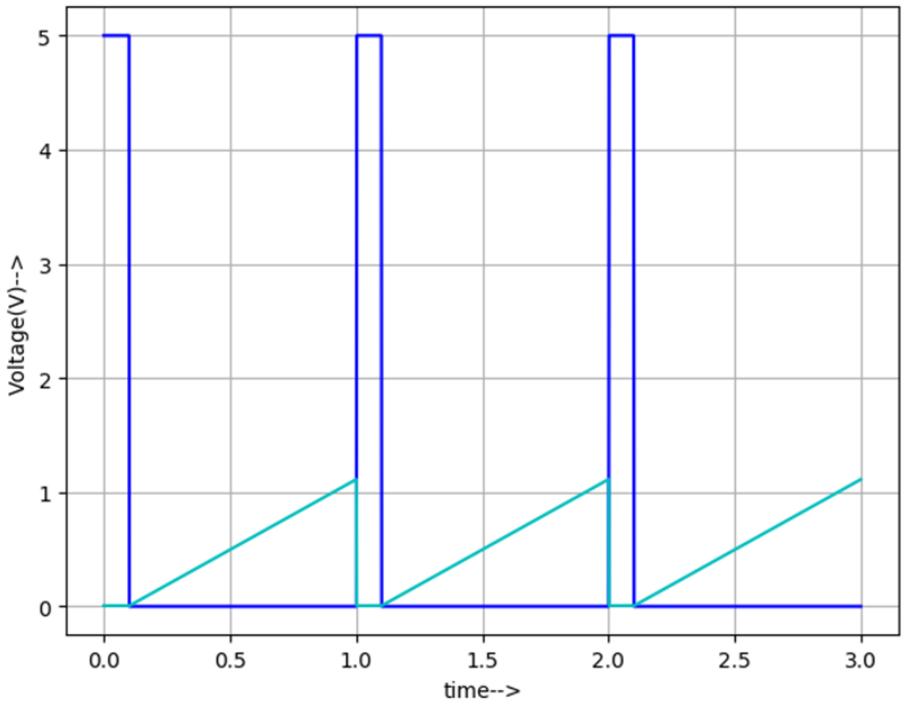

Figure 9.4: Simulation output plot of LM134 IC

dark blue plot Pulse output to discharge capacitor.
Light blue plot Output voltage across capacitor.

Chapter 10

Conclusion and Future Scope

The eSim program was used to successfully design and simulate several integrated circuits (ICs) for this internship. The integrated circuits (ICs) comprised HT12E, HT12D, LF298, 74LS56, 7481A, LM566, LM134, and UC1525. Each IC was methodically created and tested in a virtual environment, showcasing eSim's capabilities for complicated circuit design and validation.

A variety of integrated circuits was created, each with a distinct function. The HT12E and HT12D integrated circuits were utilized for remote control encoding and decoding, LF298 for operational amplifiers, 74LS56 and 7481A for digital logic applications, LM566 for VCOs, LM134 for constant current sources, and UC1525 for PWM control in power supply systems. Using eSim, integrated circuit were simulated, evaluating its operation and performance under various scenarios. This procedure ensures that each integrated circuit worked as anticipated prior to actual implementation. Diverse components were combined to form functional circuits, guaranteeing adequate connectivity and interaction among different ICs. This integration was critical for creating complex systems like frequency dividers, voltage-controlled oscillators, and constant current sources. Each integrated circuit's performance were validated using comprehensive simulations. The simulations provided insights into operating features. The internship's successful completion was dependent on the software's features, which included schematic capture, waveform analysis, and debugging tools. This internship not only allowed us to design and simulate a wide range of integrated circuits, but it also provided us with excellent expertise in using simulation tools for electronic design. The successful completion of this internship emphasizes the value of simulation in current electronics design, as it provides a cost-effective and efficient method for developing and testing complex circuits prior to physical implementation.

I learned about the principles of integrated circuit design, simulation techniques, and performance analysis. It provide hands-on experience with digital and analog components improved our grasp of circuit integration and optimization. The internship also helped us improve our problem-solving and debugging skills, which are critical for real-world VLSI applications. Overall, this initiative considerably improved our VLSI design capabilities, establishing the groundwork for future electronic and integrated circuit design efforts.

Bibliography

[1] FOSSEE Official Website. 2020.
URL: https://fossee.in/about

[2] Microchip Official Website. 2020.
URL: https://www.microchip.com/downloads/en/DeviceDoc/Atmel/

[3] eSim Official website. 2020.
URL: https://esim.fossee.in/

[4] FOSSEE official webpage. 2020.
URL: https://fossee.in/fellowship/2019

[5] TI Official Website 2020. URL:https://ti.com/

[6] GitHub Repo 2020.
URL: https://github.com/ashwini0921/Leveraging-eSim-for-Switched-Model-Simulatio