Summer Fellowship Report

On

Integrated Circuit Design using Subcircuit feature of eSim

Submitted by

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Acknowledgment

I would like to extend my heartfelt gratitude to Mr. Sumanto Kar, my mentor during this internship, for his unwavering guidance, support, and encouragement. His expertise and hands-on assistance were pivotal in helping me navigate challenges and successfully complete the project on IC development using the Subcircuit feature in eSim.

I also express my appreciation to Prof. Kannan M. Moudgalya, the head of the FOSSEE initiative, for leading this impactful program and enabling such valuable opportunities for students like me to grow and contribute to the field of electronic design automation.

This internship has been a significant learning experience, allowing me to develop technical skills and gain deeper insights into circuit simulation and design. It has also fueled my enthusiasm for further exploring the semiconductor industry and open-source tools.

Thank you to everyone who made this experience meaningful and rewarding.

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Chapter 1

Introduction

The **FOSSEE (Free/Libre and Open Source Software for Education)** initiative, spearheaded by **IIT Bombay**, is a pioneering program aimed at promoting the use of open-source software in education, research, and industry. Established with the goal of reducing reliance on expensive proprietary tools, FOSSEE develops and supports open-source alternatives tailored to the needs of academia and professionals alike.

The initiative provides comprehensive resources, including documentation, tutorials, workshops, and hands-on training sessions, to empower students, educators, and researchers. Through its various projects, such as eSim for circuit design and Scilab for numerical computation, FOSSEE facilitates learning and innovation by offering high-quality, free tools that are practical for real-world applications.

By fostering collaboration and accessibility, FOSSEE plays a key role in democratizing technology. Its contributions have opened new pathways for education and research, bridging gaps between industry standards and academic needs, and inspiring a shift towards open-source solutions in engineering and science.

1.1 eSim

eSim is an open-source electronic design automation (EDA) tool developed by the **FOSSEE (Free/Libre and Open Source Software for Education)** initiative at IIT Bombay. It enables users to create, simulate, and analyze electronic circuits. By integrating open-source tools, eSim offers a powerful platform for circuit design, simulation, and PCB layout, supporting various analyses like transient, DC, and AC analysis.

One of eSim's key features is the **Subcircuit** functionality, allowing users to build complex circuits from simpler subcircuits. This modular approach enhances efficiency and reusability. eSim also integrates with tools like **NgSpice** for simulation and **KiCad** for PCB design. It provides an affordable, open-source alternative to proprietary software, making it particularly valuable for educational purposes and fostering innovation in circuit design.

1.2 NgSpice

NgSpice is an open-source circuit simulation software that is widely used for simulating analog, digital, and mixed-signal circuits. It is based on the SPICE (Simulation Program with Integrated Circuit Emphasis) model and offers a comprehensive set of features for circuit analysis. With NgSpice, users can perform a variety of simulations such as transient, DC, and AC analysis, making it a versatile tool for both students and professionals in electronics.

NgSpice supports a wide range of device models, including active components like transistors and diodes, and passive components such as resistors, capacitors, and inductors. Its flexibility and open-source nature make it an excellent tool for circuit simulation and educational purposes. Additionally, NgSpice can be integrated with other tools like eSim, making it part of a broader open-source ecosystem for circuit design and analysis.

1.3 Makerchip

Makerchip is an online platform for designing and simulating digital circuits using **Verilog** and **SystemVerilog**. It provides both browser-based and desktop-based environments, making it accessible and convenient for users of all experience levels. Makerchip's primary focus is to simplify the process of digital circuit design, offering easy-to-use tools for coding, compiling, and simulating designs in real-time.

The platform allows seamless integration with various simulation tools and features a user-friendly interface for testing and debugging digital designs. Makerchip is particularly valuable for educators and students in the field of digital electronics, offering a practical environment for learning and experimentation. It also supports a wide range of projects, from simple digital circuits to more complex system designs.

1.4 KiCad

KiCad is a free and open-source software suite for designing electronic schematic diagrams and printed circuit boards (PCBs). It is widely used by hobbyists, students, and professionals to create detailed circuit designs and PCB layouts. KiCad offers a range of features, including schematic capture, PCB layout, and 3D visualization of the board, making it a comprehensive tool for electronic design automation (EDA). Its open-source nature and extensive library of components make it an ideal choice for users looking for an affordable yet powerful PCB design tool.

KiCad supports a variety of file formats and integrates well with other tools in the EDA ecosystem, including **eSim** for circuit simulation. Its flexibility and robust feature set have made it popular among the maker community, and it is increasingly used in professional applications as well. With a user-friendly interface and strong community support, KiCad continues to be a valuable resource for electronics design.

Chapter 2

Key Features of ESim

1. **Schematic Capture**
   eSim provides an intuitive graphical interface for creating circuit schematics.
   Users can easily drag and drop components from a comprehensive library.

2. **Circuit Simulation**
   Supports various types of simulations, including transient, DC, and AC analysis.
   Integration with **NgSpice** ensures accurate circuit behavior modeling.

3. **Subcircuit Creation**
   Users can create complex circuits by integrating simpler subcircuits.
   This modular approach improves design scalability and reusability.

4. **PCB Design**
   eSim allows users to design printed circuit boards (PCBs).
   It supports generating **Gerber files** for manufacturing PCB layouts.

5. **Open-Source Integration**
   Seamlessly integrates with other open-source tools like **KiCad** and **Makerchip**.
   This integration allows users to leverage a broad range of design tools.

6. **Extensive Component Library**
   eSim provides a wide range of components, from basic resistors to advanced ICs.
   This library makes it easier to design a variety of circuits without external dependencies.

7. **User-Friendly Interface**
   Designed for ease of use, eSim offers an accessible interface for users at all levels.
   The platform is simple enough for students while being powerful for professionals.

Chapter 3

Problem Approach in eSim

The goal of this project is to design and develop various analog and digital integrated circuit models in the form of sub-circuits using device model files that are already present in the eSim library. These IC models should be useful for future circuit design purposes by developers and users, once successfully integrated into the eSim subcircuit library.

1. **Select an IC to Implement on eSim**
   The first step in the approach is to select an integrated circuit (IC) that will be implemented in eSim. The selection is based on the desired functionality and the need for specific components available in the eSim library.

2. **Obtain the IC's Datasheet**
   After selecting the IC, the next step is to find the datasheet for the IC. This can be done by searching online, typically on websites such as *DatasheetCatalog* or *TI (Texas Instruments)*, to ensure accurate component details such as pin configurations, voltage ratings, and electrical characteristics.

3. **Create Subcircuit and Netlist/Output Files**
   Based on the information from the datasheet, a subcircuit is created in eSim. This involves using the components from the eSim library and assembling them into a modular subcircuit. The next step is to generate the corresponding **netlist** and **output files** that will be used in simulations and testing.

4. **Test the Circuit Using Test Circuit Implemented in KiCad**
   Once the subcircuit is created, a test circuit is designed to check the functionality of the IC. This test circuit is implemented in **KiCad**, where it is connected with other necessary components to simulate real-world usage scenarios.

5. **Use NgSpice for Simulation and Check the Output**
   After the circuit is tested in KiCad, the next step is to use **NgSpice** for detailed circuit simulation. The netlist and output files from eSim are imported into NgSpice, where the simulation is run to check the circuit's performance. The output waveforms and parameters are analyzed to verify that the IC works as intended.

Chapter 4

74LS82 - 2-Bit Binary Adder

The **74LS82** is a **2-bit binary adder** IC that contains two **1-bit full adders**. It is part of the **74LS** series, using **Low Power Schottky (LS)** technology for efficient and reliable performance. The 74LS82 is designed to add two 2-bit binary numbers and provide a **sum** and **carry-out** for further calculations.

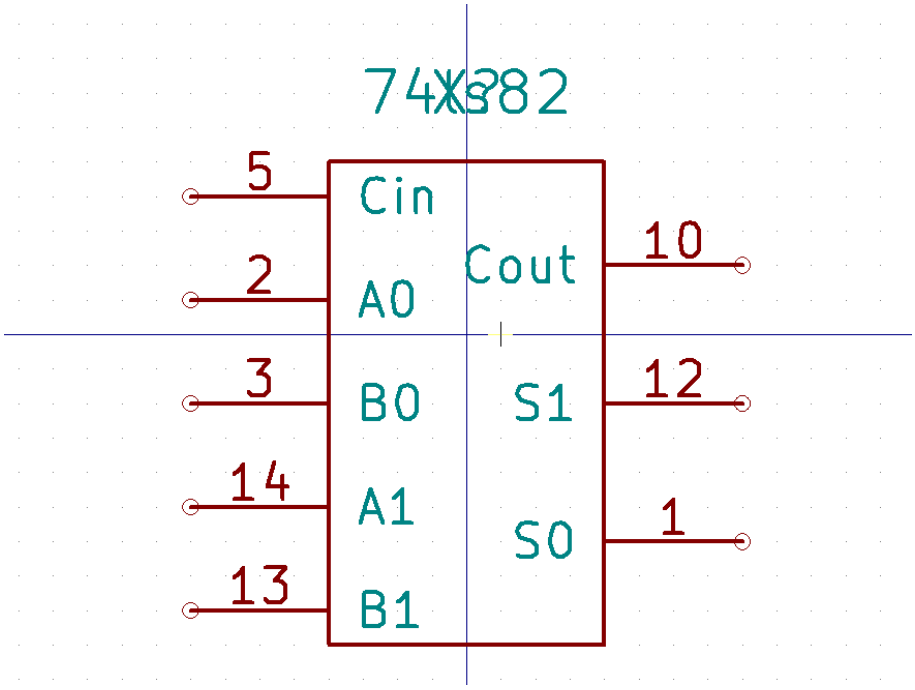
4.1 Truth Table

A1	A0	B1	B0	Carry-In	Sum1	Sum0	Carry-Out
0	0	0	0	0	0	0	0
0	0	0	1	0	0	1	0
0	0	1	0	0	0	1	0
0	0	1	1	0	1	0	0
0	1	0	0	0	0	1	0
0	1	0	1	0	1	0	0
0	1	1	0	0	1	1	0
0	1	1	1	0	0	0	1
1	0	0	0	0	1	0	0
1	0	0	1	0	1	1	0
1	0	1	0	0	0	1	1
1	0	1	1	0	1	0	1
1	1	0	0	0	1	1	0
1	1	0	1	0	0	0	1
1	1	1	0	0	1	0	1
1	1	1	1	0	0	1	1

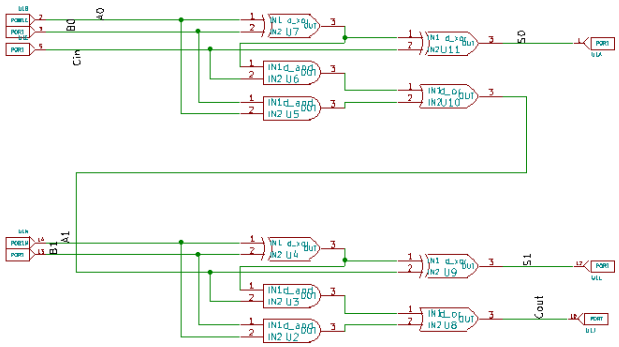
4.2 Features

1. Contains two 1-bit full adders for adding two 2-bit binary numbers.
2. Provides sum and carry-out outputs.
3. Low power consumption due to the Schottky TTL logic family.
4. Ideal for use in **arithmetic circuits**, **binary counters**, and **digital calculators**.

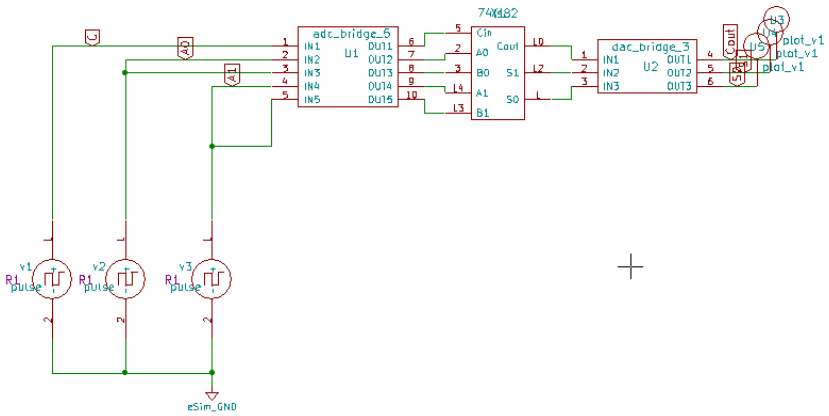
4.3 IC Pin Layout



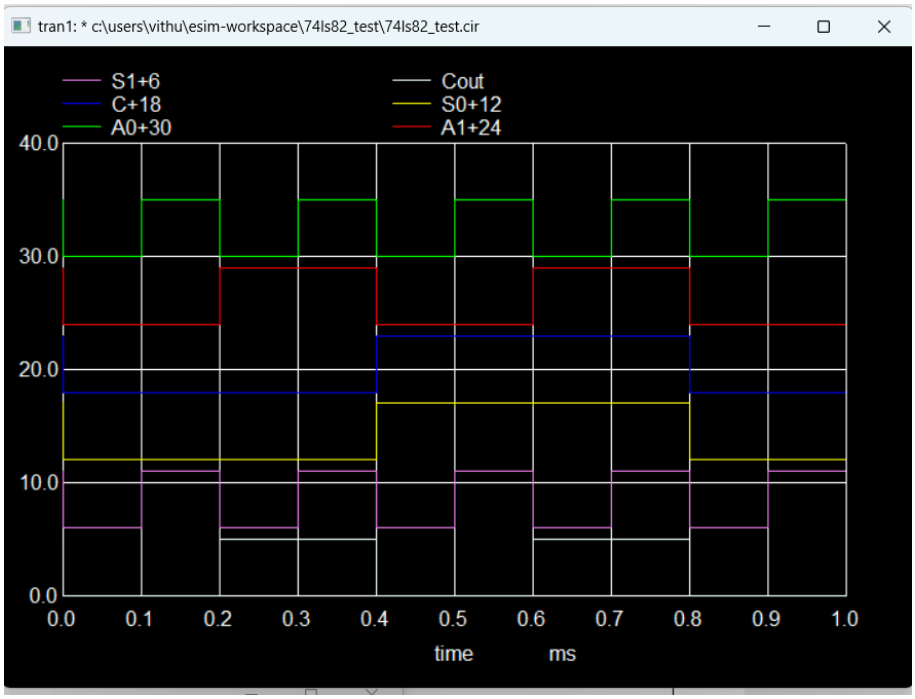
4.4 Large Circuit Schematic Diagram



4.5 Test Circuit Diagram



4.6 Plot



Chapter 5

74HC688 - 8-Bit Magnitude Comparator

The **74HC688** is an 8-bit magnitude comparator IC designed to compare two 8-bit binary words, labeled as **P** and **Q**. The IC has an active-low enable input (**E**) and an active-low equality output (**P=Q**). When the enable input (**E**) is low, the IC compares the two binary inputs bit-by-bit and outputs a low signal on **P=Q** if the two words are equal. Otherwise, the output remains high.

This IC operates at a wide voltage range from 2V to 6V and is built using CMOS technology for high speed and low power consumption. It also features high noise immunity, making it suitable for robust digital applications.

5.1 Truth Table

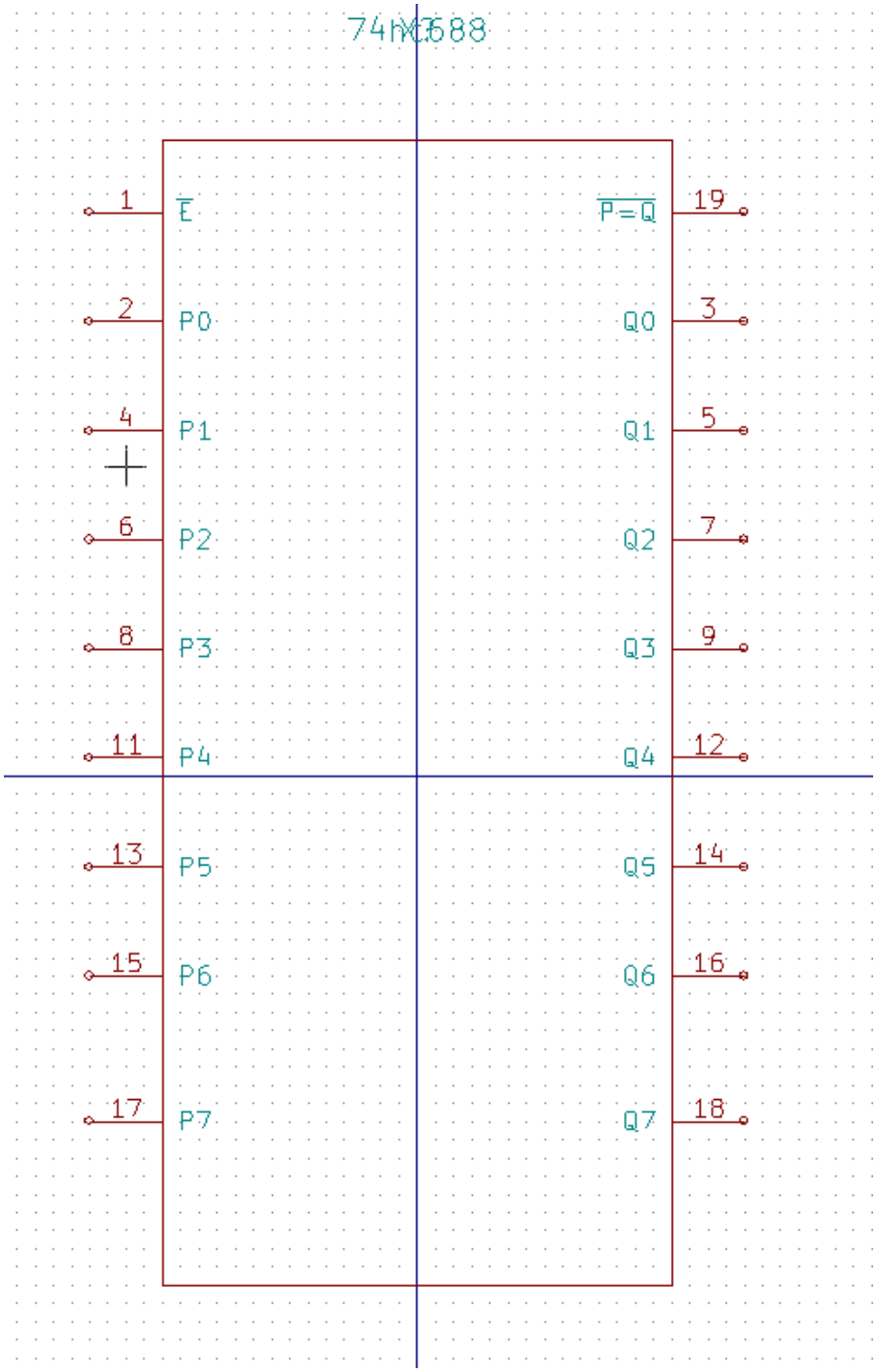
Enable (E)	**Data Pn, Qn**	**P=Q (Output)**
L (Low)	P = Q	L (Low)
L (Low)	P >Q or P <Q	H (High)
H (High)	X (Don't care)	H (High)

5.2 Features:

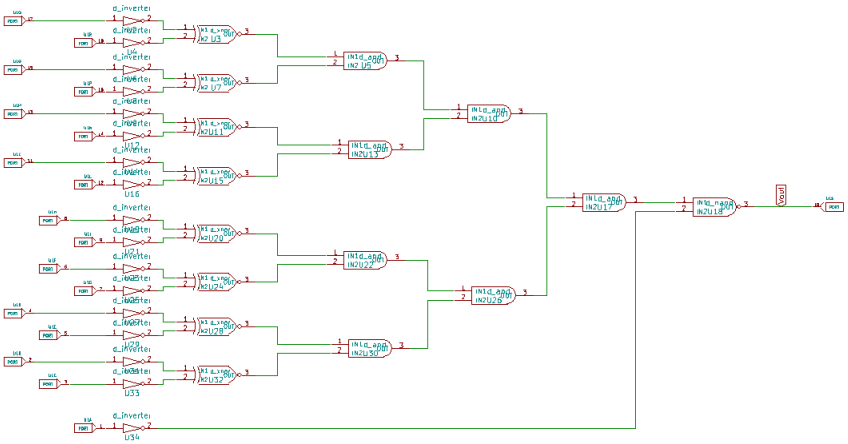
1. Compares two 8-bit binary words (P and Q).
2. Active-low equality output (**P=Q**) for matching words.
3. Active-low enable input (**E**) to control operation.
4. Operates over a wide supply voltage range of 2.0V to 6.0V.

5. CMOS construction ensures low power consumption and high noise immunity.
6. Complies with JEDEC standards and provides robust ESD protection.

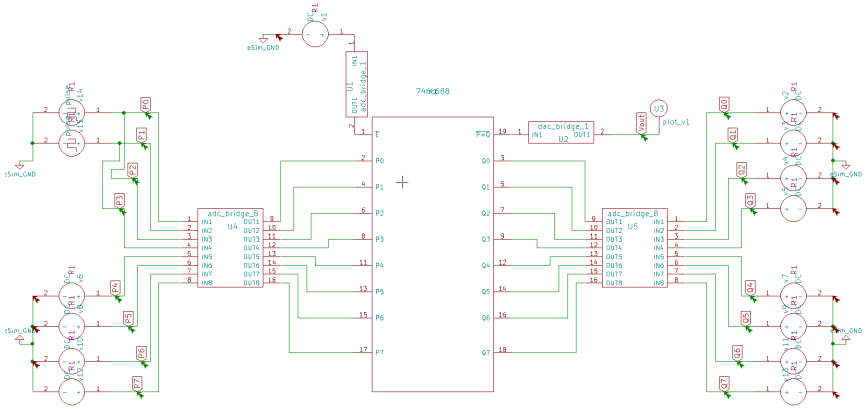
5.3 IC Pin Layout



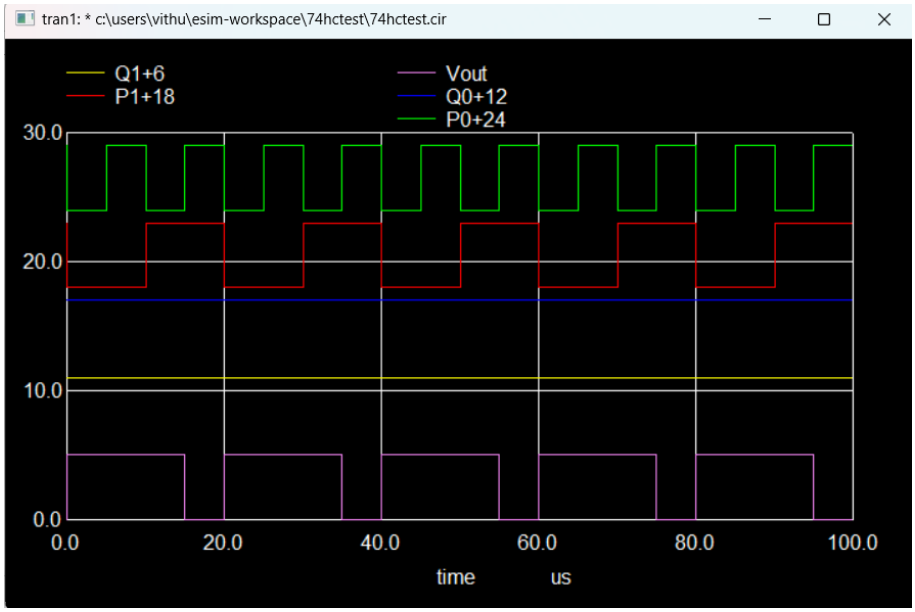
5.4 Circuit Schematic Diagram



5.5 Test Circuit Diagram



5.6 Plot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Q1+6
P1+18
Vout
Q0+12
P0+24
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Chapter 6

LM306 - High-Speed Voltage Comparator

The **LM306** is a high-speed voltage comparator designed for applications requiring fast response times and high precision. It is commonly used in circuits for detecting signal thresholds, zero-crossing detection, and voltage level comparisons. The IC includes two strobe inputs (**STROBE1** and **STROBE2**) for enabling or disabling the comparator output. It also features built-in protection circuitry for input overvoltage and current limiting.

This comparator operates with low propagation delay and can handle a wide range of input voltages, making it suitable for high-speed and precision applications. Its output stage can drive TTL or DTL logic levels, ensuring compatibility with standard digital systems.

6.1 Truth Table

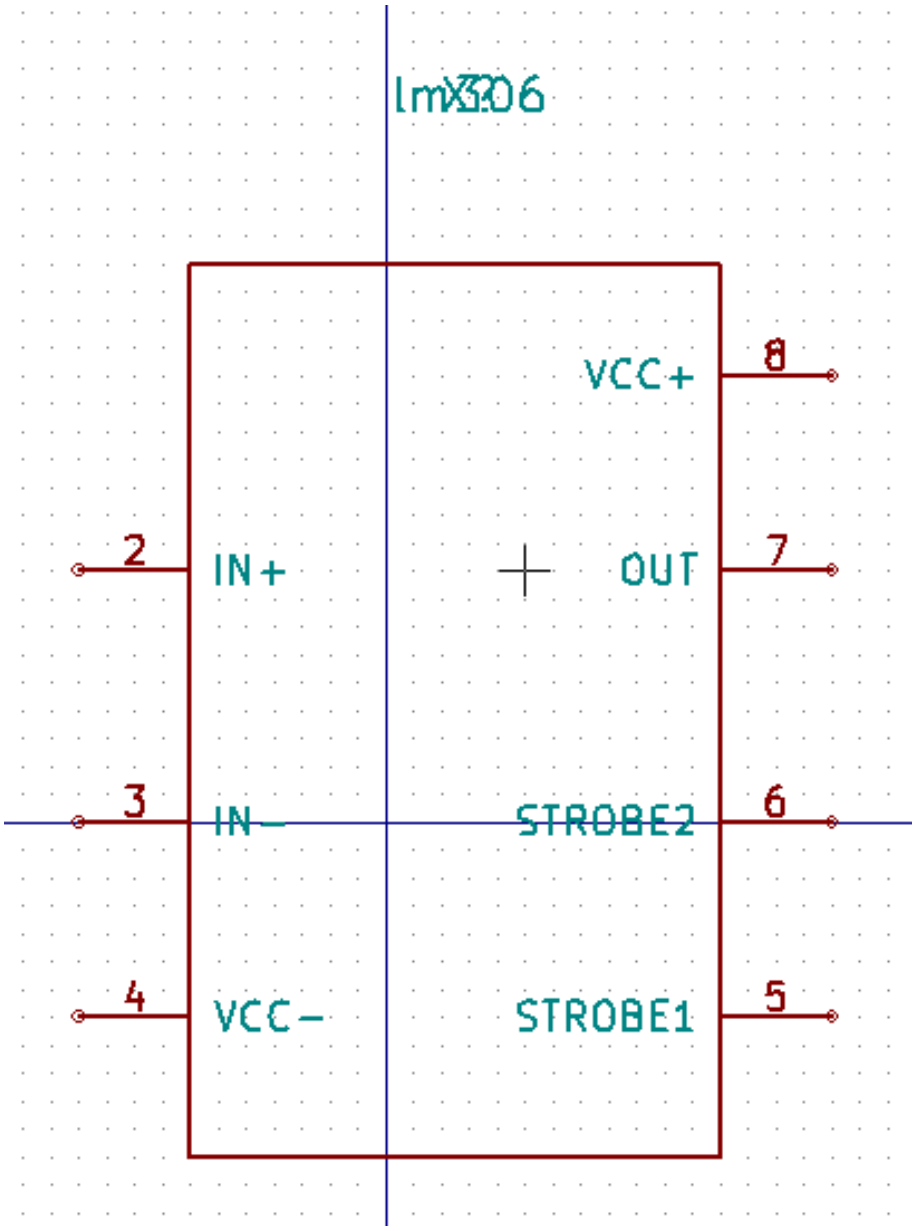
Input+	**STROBE1**	**STROBE2**	**Output**
>Input-	H (High)	H (High)	H (High)
<Input-	H (High)	H (High)	L (Low)
X (Don't care)	L (Low)	X	L (Low)
X (Don't care)	X	L (Low)	L (Low)

6.2 Features:

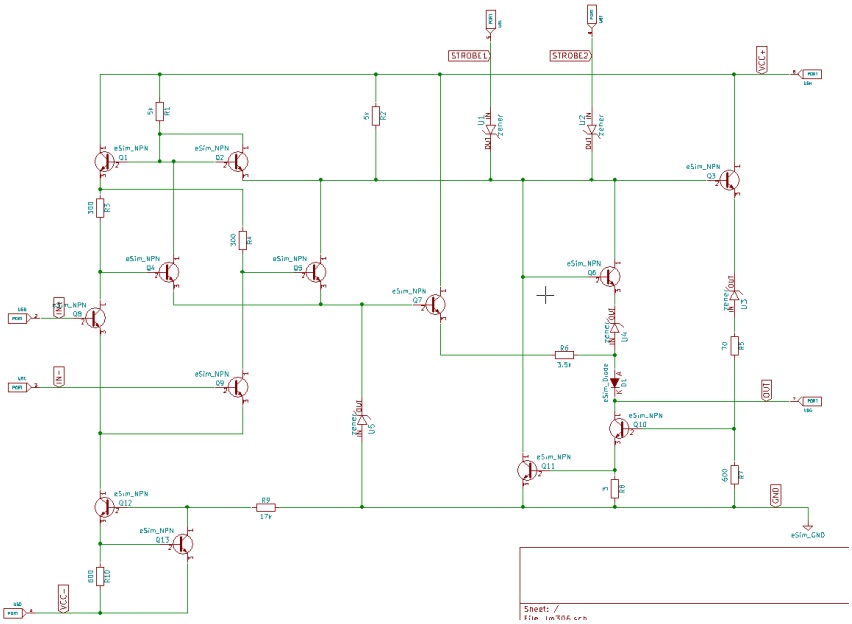
1. High-speed operation with low propagation delay.
2. Wide input voltage range for versatile applications.
3. TTL and DTL compatible output stages.
4. Built-in input protection and current-limiting circuitry.
5. Two strobe inputs (**STROBE1** and **STROBE2**) to enable or disable output.

6. Suitable for signal detection, voltage level comparison, and zero-crossing detection.

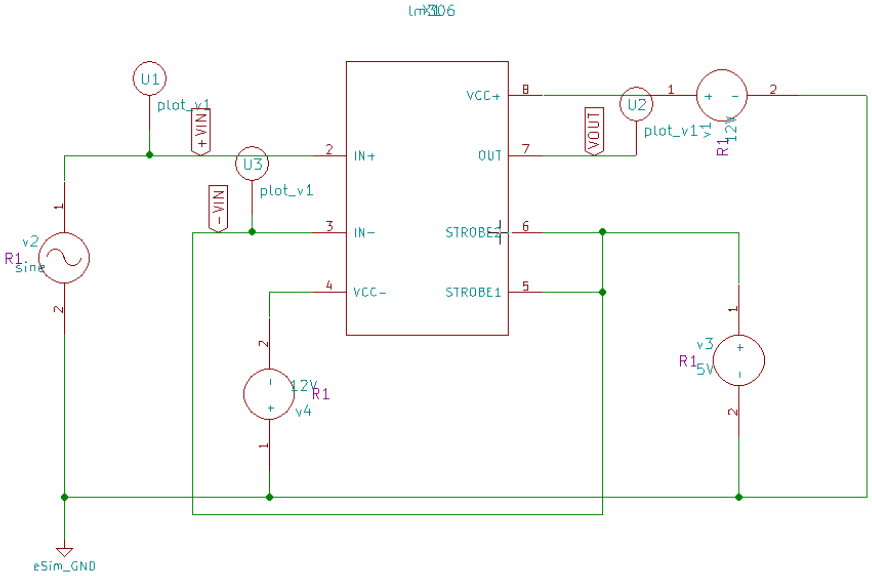
6.3 IC Pin Layout



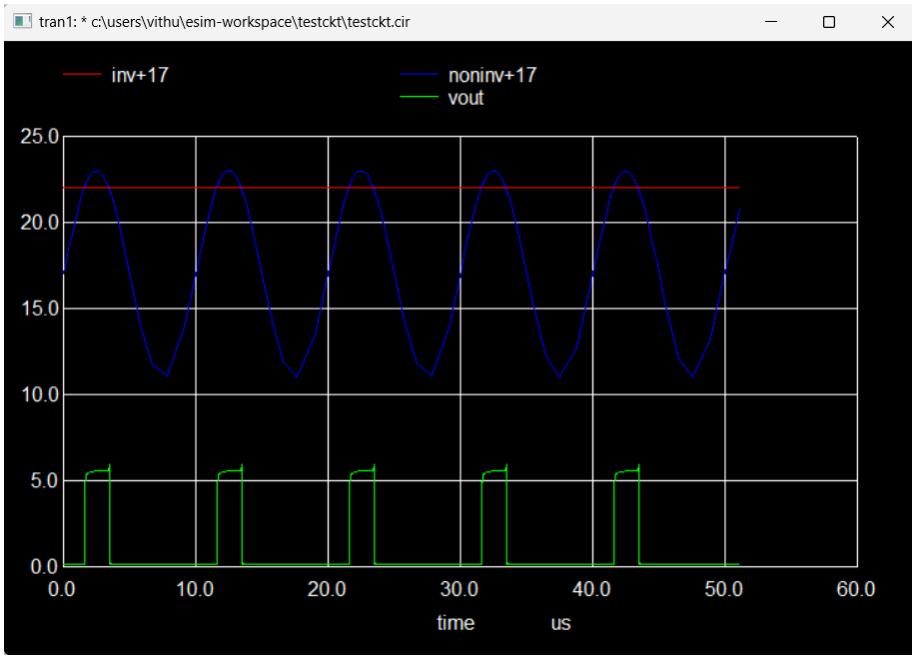
6.4 Circuit Schematic Diagram



6.5 Test Circuit Diagram



6.6 Plot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noninv+17
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Chapter 7

CD4010 - Hex Buffer/Converter

The **CD4010** is a CMOS hex buffer and level shifter designed for applications requiring signal amplification or voltage-level conversion. It is widely used to interface logic signals between different voltage domains, such as CMOS and TTL logic levels, and to buffer signals to improve noise immunity and drive capability.

This IC features six independent buffer stages with symmetrical output drive capability, ensuring compatibility with a variety of logic circuits. Its low power consumption, high noise immunity, and ability to operate over a wide supply voltage range make it an ideal choice for both digital and analog signal processing.

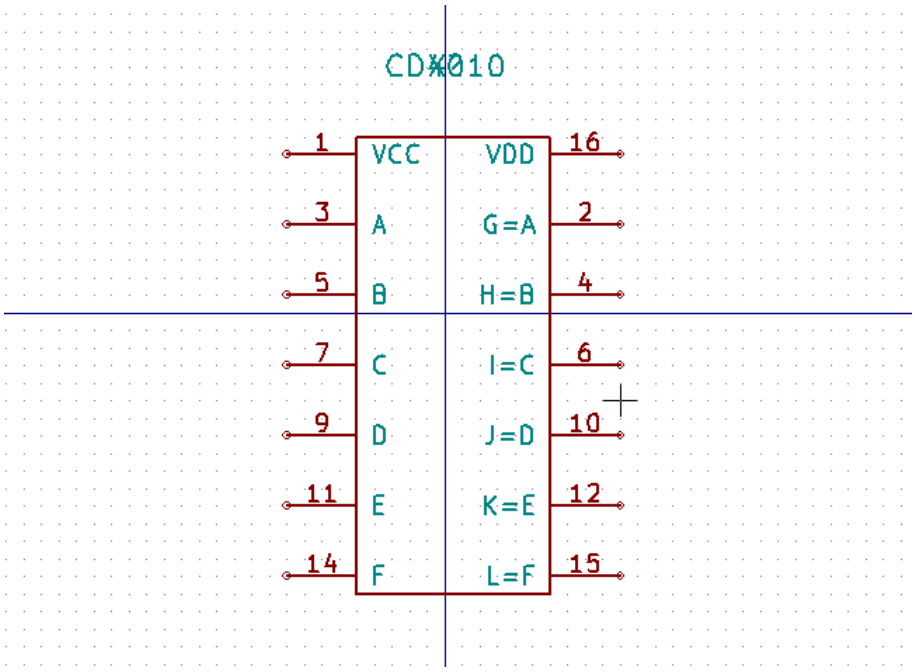
7.1 Truth Table

Input	Output
L (Low)	L (Low)
H (High)	H (High)

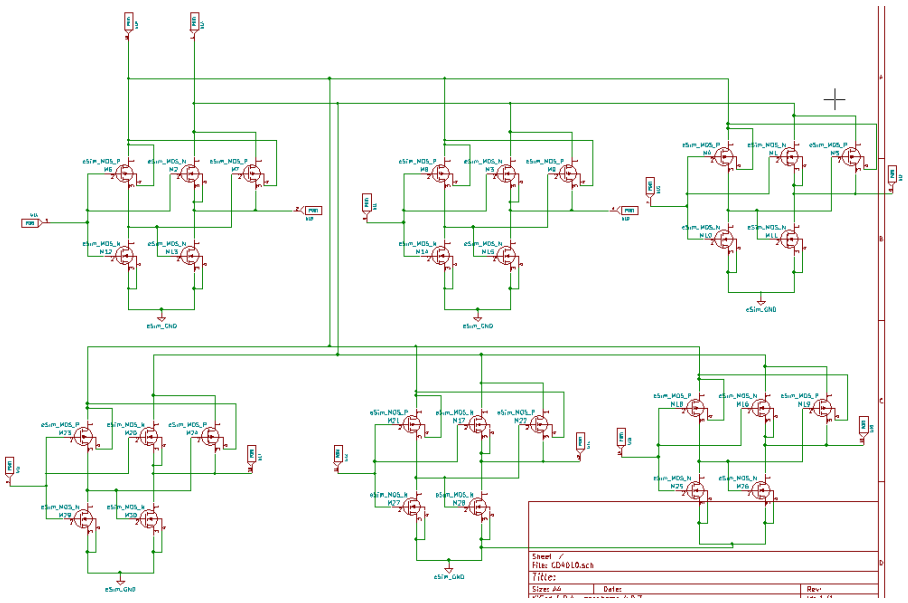
7.2 Features:

1. Six independent buffer stages for signal processing.
2. Wide supply voltage range: 3V to 15V.
3. High noise immunity with a static noise margin of approximately 50
4. Low power consumption characteristic of CMOS technology.
5. Symmetrical output drive ensures compatibility with both CMOS and TTL circuits.
6. Suitable for signal amplification and voltage-level conversion.
7. High-speed operation, ideal for modern digital circuits.

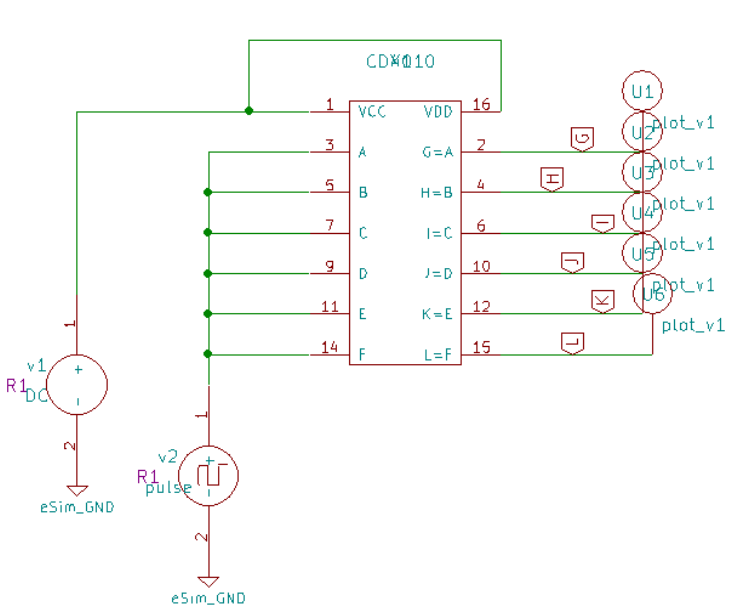
7.3 IC Pin Layout



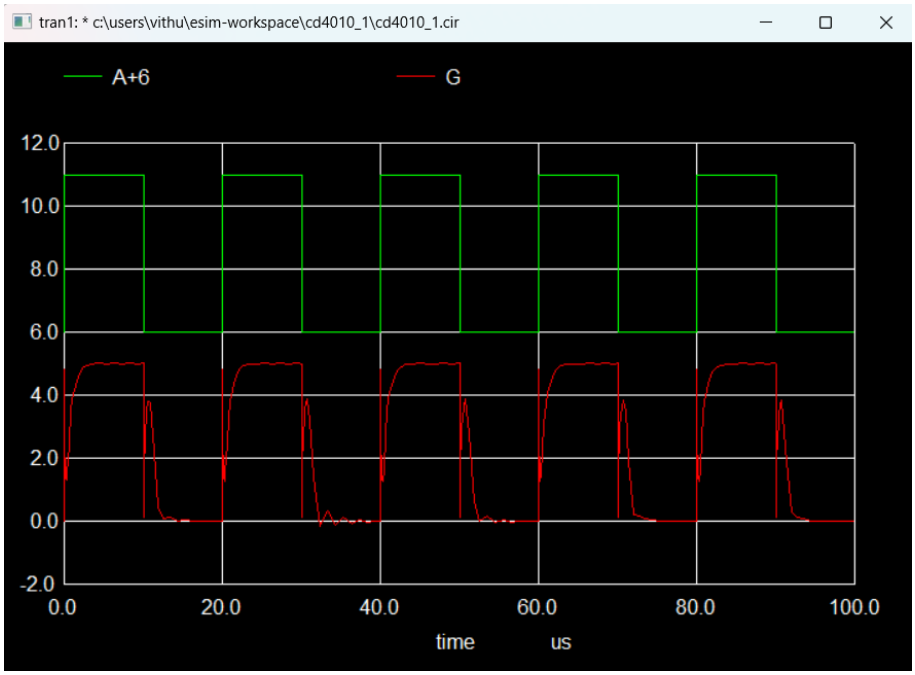
7.4 Circuit Schematic Diagram



7.5 Test Circuit Diagram



7.6 Plot



Chapter 8

CD4030 - Quad XOR Gate

The **CD4030** is a CMOS-based quad XOR gate IC designed for digital logic operations. It consists of four independent XOR gates, each with two inputs, making it suitable for applications such as parity generation, signal processing, and logic circuit design.

This IC operates over a wide supply voltage range and exhibits low power consumption, typical of CMOS technology. Its high noise immunity and symmetrical output drive capabilities make it ideal for interfacing with various digital systems. The CD4030 is widely used in arithmetic circuits, error detection systems, and binary addition circuits.

8.1 Truth Table

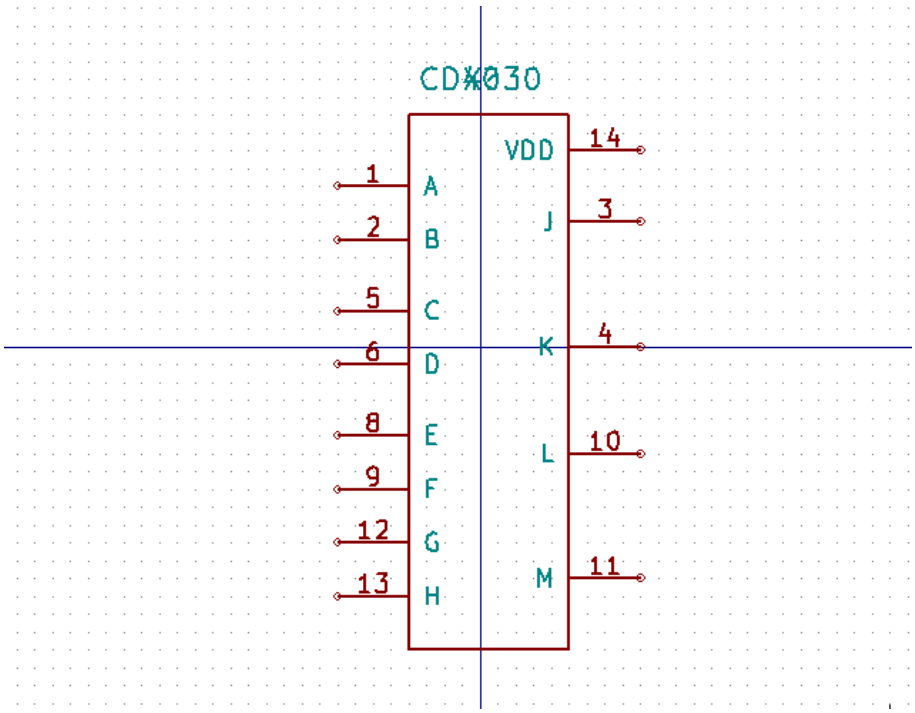
Input A	Input B	Output (A B)
L (Low)	L (Low)	L (Low)
L (Low)	H (High)	H (High)
H (High)	L (Low)	H (High)
H (High)	H (High)	L (Low)

8.2 Features:

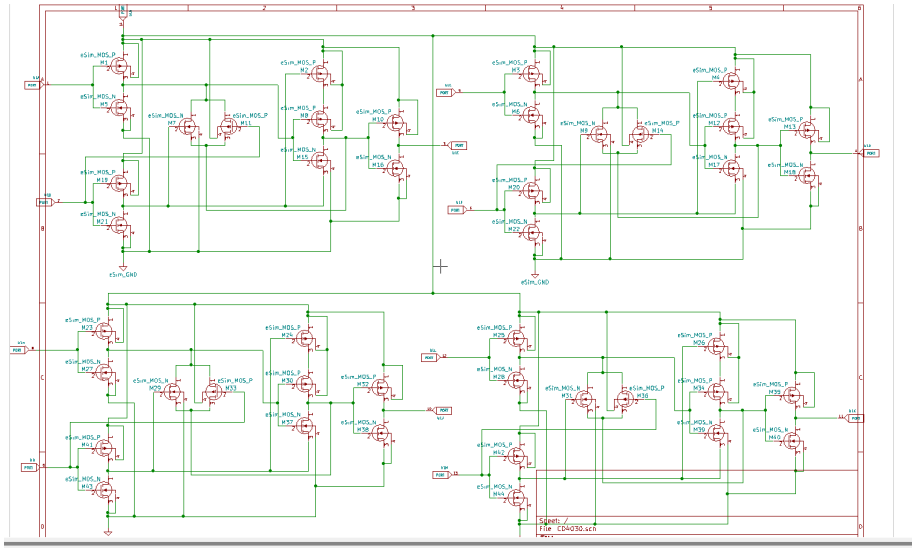
1. Contains four independent XOR gates.
2. Wide supply voltage range: 3V to 15V.
3. Low power consumption characteristic of CMOS technology.
4. High noise immunity for reliable operation in noisy environments.
5. Symmetrical output drive ensures compatibility with other digital circuits.
6. Applications include parity generation, error detection, and digital logic operations.

7. Ideal for use in arithmetic and binary addition circuits.

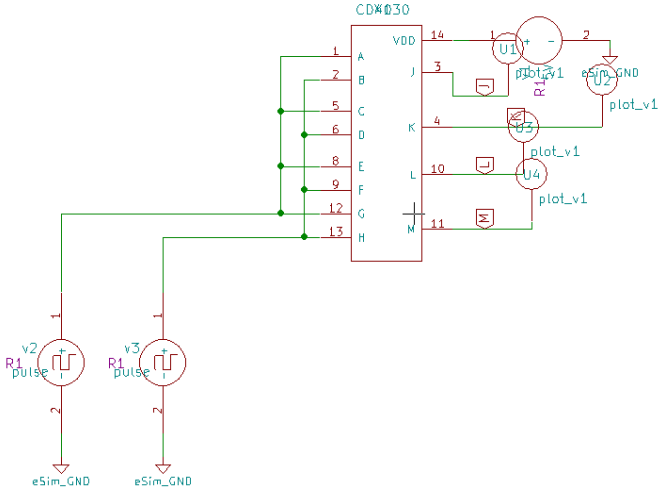
8.3 IC Pin Layout



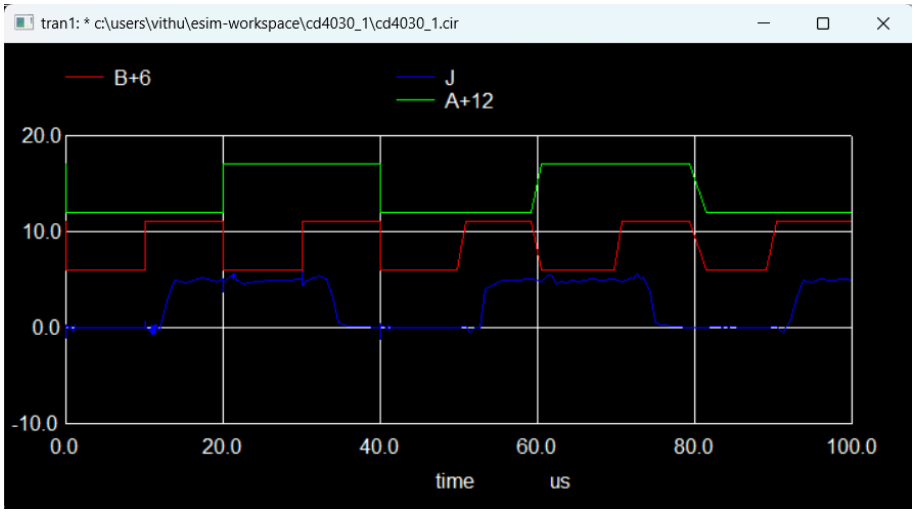
8.4 Circuit Schematic Diagram



8.5 Test Circuit Diagram



8.6 Plot



Chapter 9

CD4068 - 8-Input AND Gate

The **CD4068** is a CMOS-based 8-input AND gate IC designed for digital logic operations requiring multiple input signals. It provides a single output that goes high only when all eight inputs are high, making it suitable for complex logic designs and high-input count applications.

This IC operates over a wide supply voltage range and features low power consumption and high noise immunity. Its symmetrical output drive capability ensures compatibility with other CMOS and TTL circuits. The CD4068 is commonly used in combinational logic circuits, digital systems, and control logic applications.

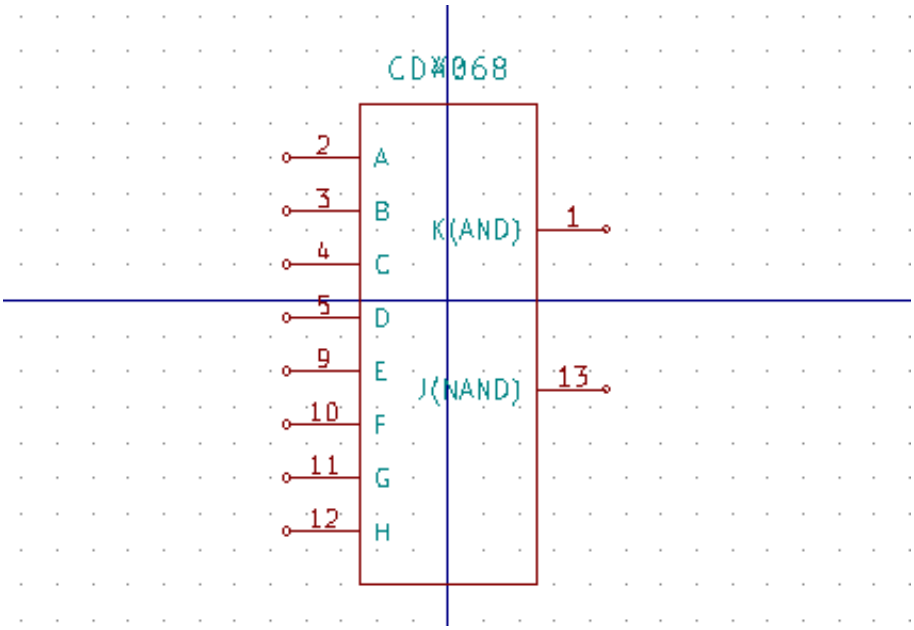
9.1 Truth Table

Inputs (A, B, ..., H)	**Output (Y)**
Any input = L (Low)	L (Low)
All inputs = H (High)	H (High)

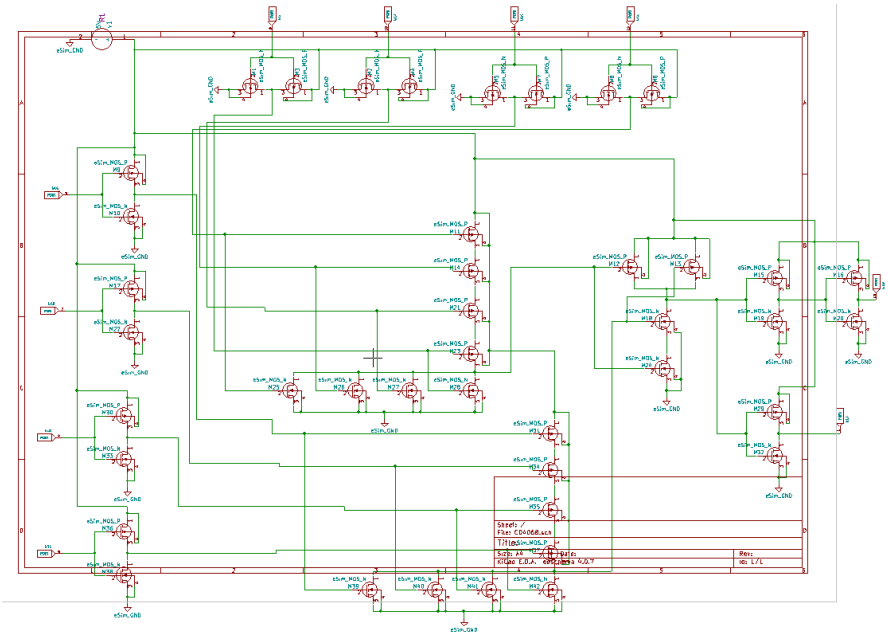
9.2 Features:

1. Single 8-input AND gate.
2. Wide supply voltage range: 3V to 15V.
3. Low power consumption due to CMOS technology.
4. High noise immunity for reliable operation.
5. Symmetrical output drive for compatibility with CMOS and TTL circuits.
6. Ideal for combinational logic applications requiring multiple inputs.
7. Commonly used in digital control systems and decision-making circuits.

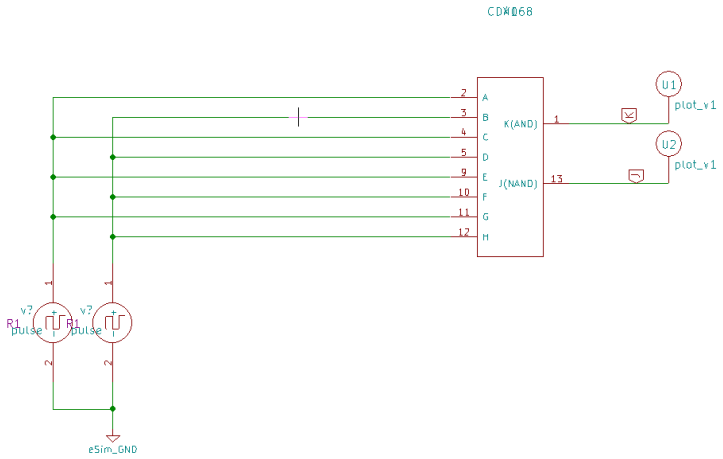
9.3 IC Pin Layout



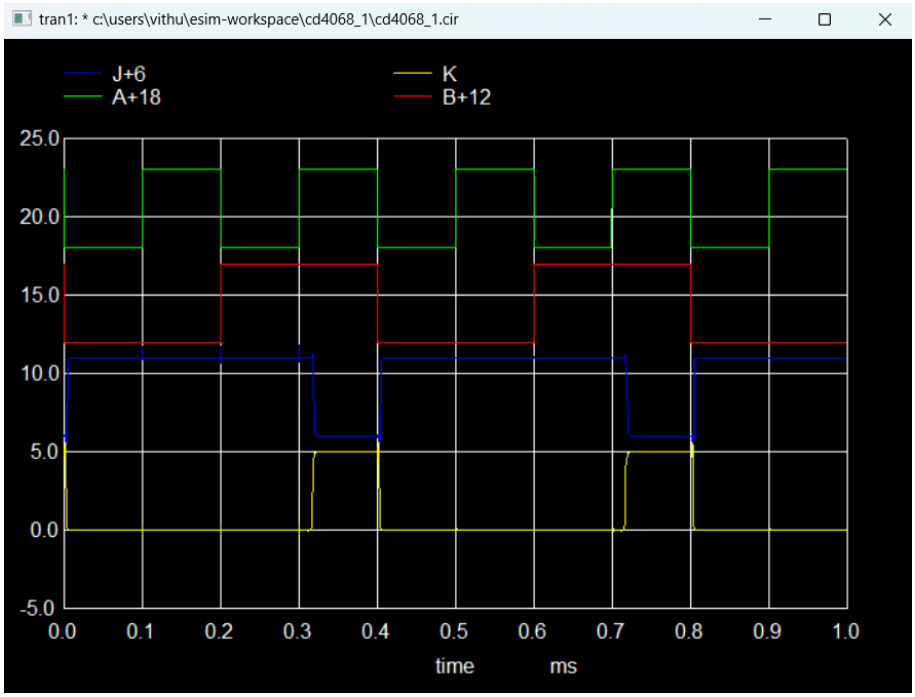
9.4 Circuit Schematic Diagram



9.5 Test Circuit Diagram



9.6 Plot



Chapter 10

CD4082 - Dual 4-Input AND Gate

The **CD4082** is a CMOS-based IC that features two independent 4-input AND gates. It is designed for digital logic operations where multiple input signals are processed to generate a single output per gate. The output is high only when all four inputs of the corresponding gate are high.

This IC operates over a wide voltage range, exhibits low power consumption, and offers high noise immunity, making it ideal for digital applications. Its symmetrical output drive ensures compatibility with both CMOS and TTL circuits. The CD4082 is commonly used in logic control, data processing, and signal gating applications.

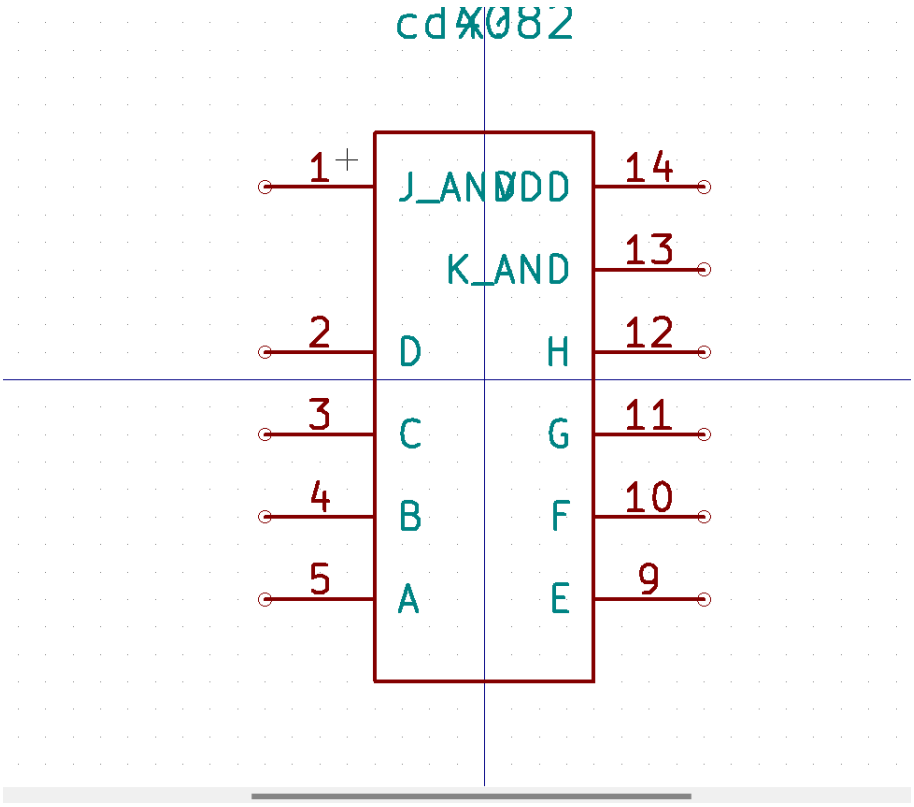
10.1 Truth Table

Inputs (A, B, C, D)	**Output (Y)**
Any input = L (Low)	L (Low)
All inputs = H (High)	H (High)

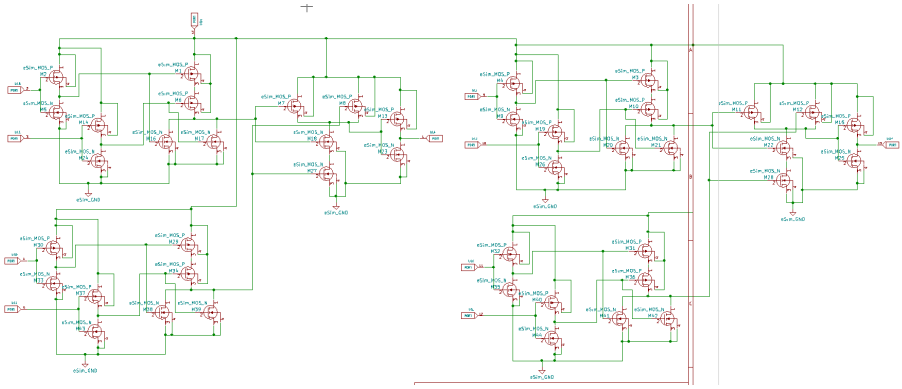
10.2 Features:

1. Two independent 4-input AND gates.
2. Wide supply voltage range: 3V to 15V.
3. Low power consumption due to CMOS technology.
4. High noise immunity for reliable operation in noisy environments.
5. Symmetrical output drive for interfacing with CMOS and TTL logic.
6. Suitable for combinational logic and control applications.
7. Commonly used in data processing and signal selection circuits.

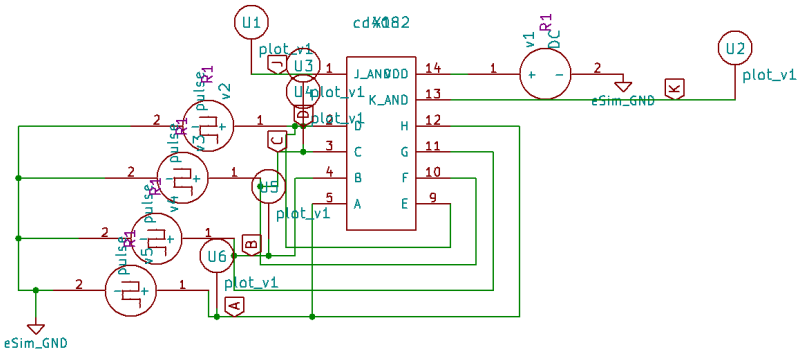
10.3 IC Pin Layout



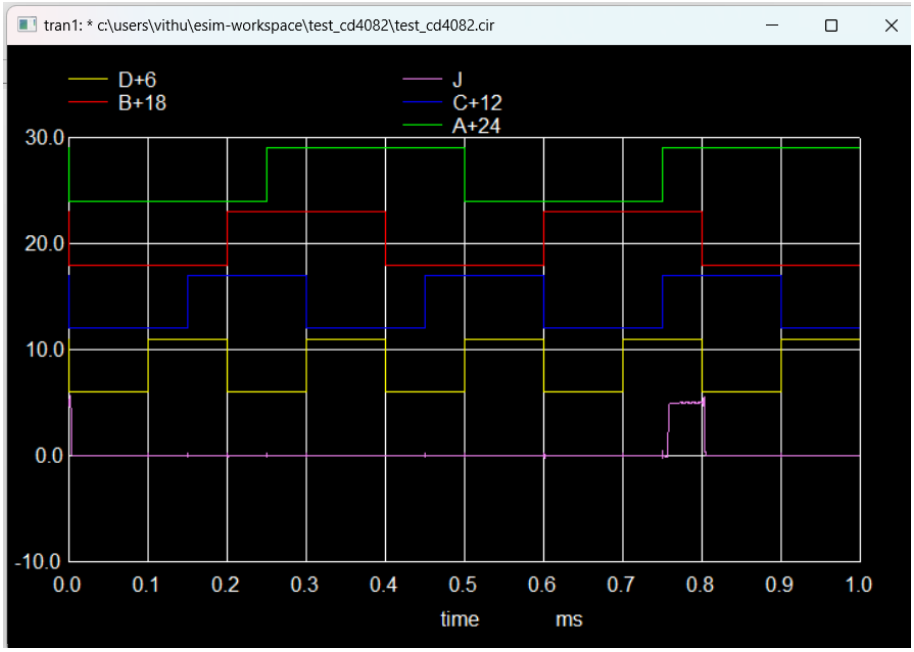
10.4 Circuit Schematic Diagram



10.5 Test Circuit Diagram



10.6 Plot



Chapter 11

CD40101 - 9-Bit Parity Checker/Generator

The **CD40101** is a CMOS-based 9-bit parity checker and generator. It is designed for error detection in digital communication and data transfer systems. The IC can process up to nine input bits and determine whether the overall parity is odd or even.

The IC generates a parity bit for the given input bits or verifies the parity of a transmitted message, helping detect single-bit errors. Additionally, it features an **Inhibit** input that allows disabling the outputs, ensuring flexibility in system integration. Its wide operating voltage range, low power consumption, and high noise immunity make it suitable for use in error detection systems, digital communication, and data integrity verification applications.

11.1 Truth Table (Simplified)

Inputs (A1...A9)	Inhibit	Even Parity (E)	Odd Parity (O)
Any combination	H (High)	L (Low)	L (Low)
Even number of 1s	L (Low)	H (High)	L (Low)
Odd number of 1s	L (Low)	L (Low)	H (High)

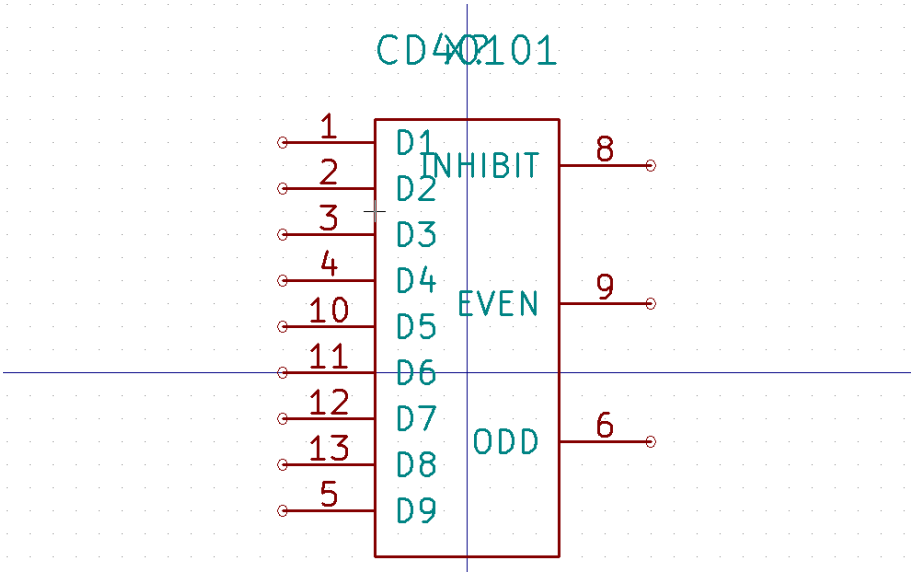
11.2 Features:

1. 9-bit parity checking and generation.
2. Supports both odd and even parity operations.
3. Wide supply voltage range: 3V to 15V.
4. Low power consumption characteristic of CMOS technology.
5. High noise immunity for reliable error detection in noisy environments.

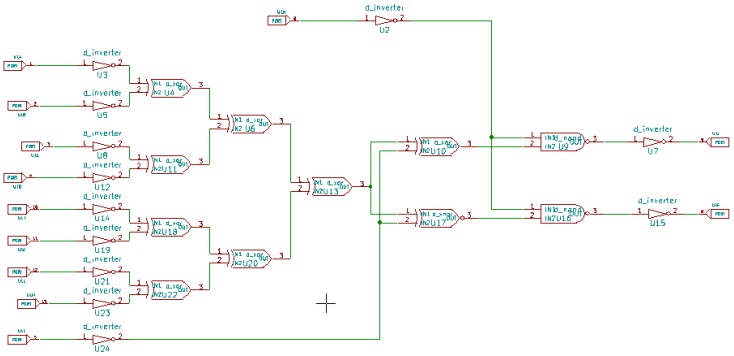
6. **Inhibit** input for output control.

7. Useful in error detection for digital

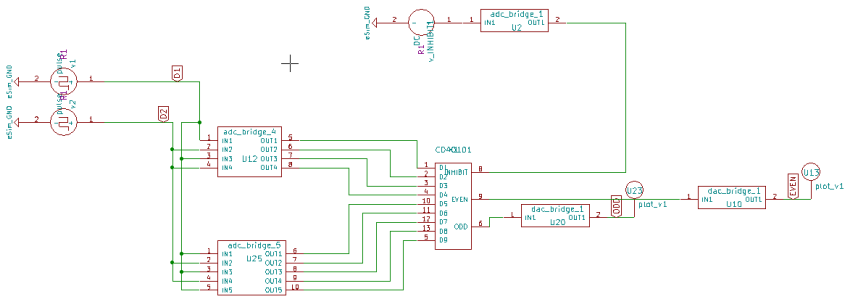
11.3 IC Pin Layout



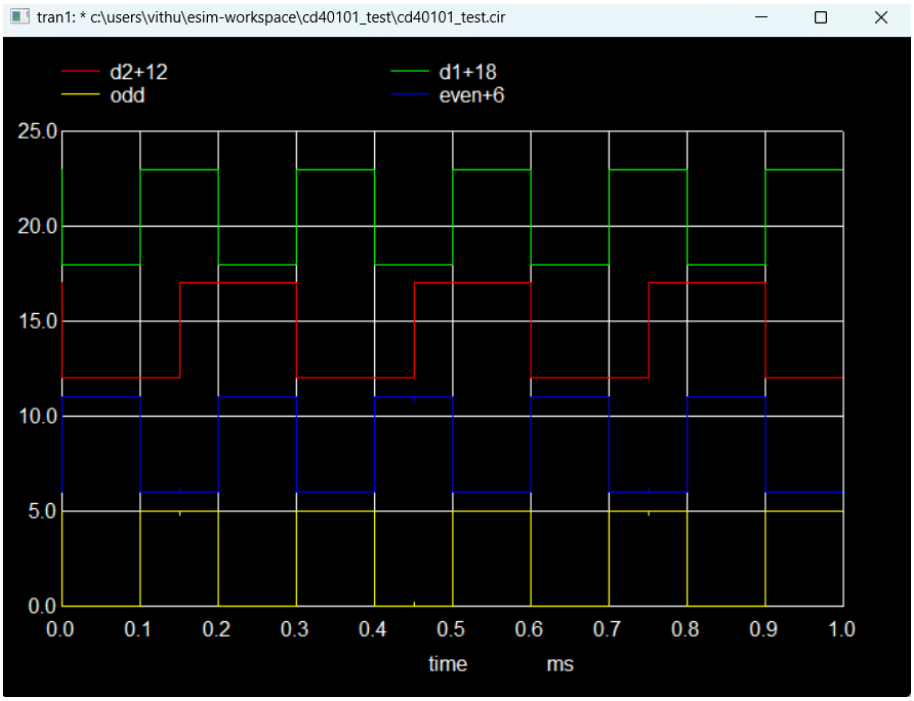
11.4 Circuit Schematic Diagram



11.5 Test Circuit Diagram



11.6 Plot



Chapter 12

CD4555 - Dual 1-of-4 Decoder/Demultiplexer

The **CD4555** is a CMOS-based dual 1-of-4 decoder/demultiplexer IC. It features two independent decoding sections, each capable of taking a 2-bit binary input and selecting one of the four outputs. Each decoder includes an **Enable** input, which allows activation or deactivation of the corresponding decoder.

This IC is widely used in data routing, digital logic circuits, and signal multiplexing applications. It operates with a wide voltage range and provides high noise immunity. Its low power consumption and compatibility with other CMOS or TTL circuits make it ideal for use in digital systems and control applications.

12.1 Truth Table (For One Decoder)

Enable	Select (A1, A0)	Y0	Y1	Y2	Y3
L (Low)	X (Don't Care)	L (Low)	L (Low)	L (Low)	L (Low)
H (High)	00	H (High)	L (Low)	L (Low)	L (Low)
H (High)	01	L (Low)	H (High)	L (Low)	L (Low)
H (High)	10	L (Low)	L (Low)	H (High)	L (Low)
H (High)	11	L (Low)	L (Low)	L (Low)	H (High)

12.2 Features:

(a) Dual 1-of-4 decoder/demultiplexer.

(b) Each decoder has an **Enable** input.

(c) Wide supply voltage range: 3V to 15V.

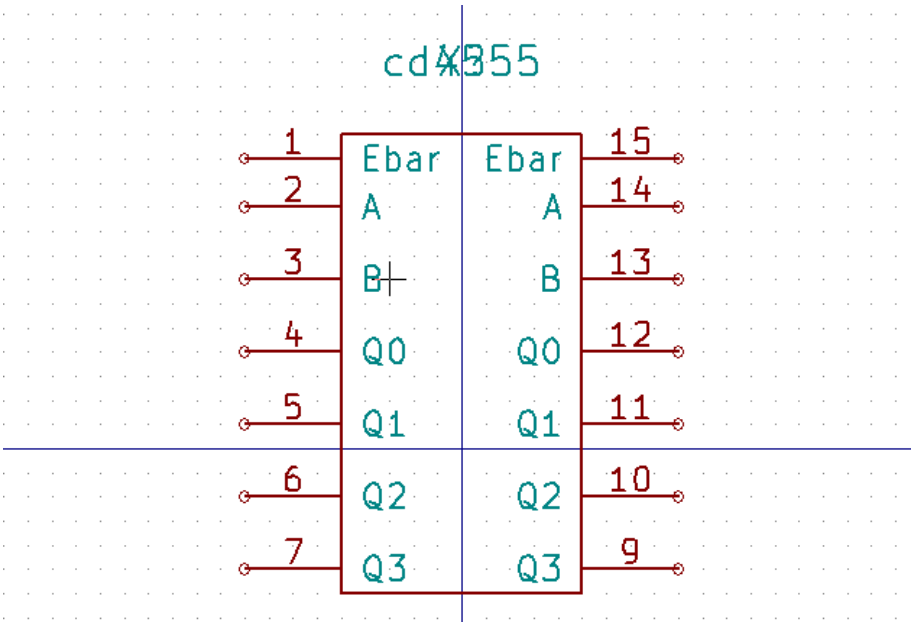
(d) Low power consumption typical of CMOS technology.

(e) High noise immunity for stable operation.

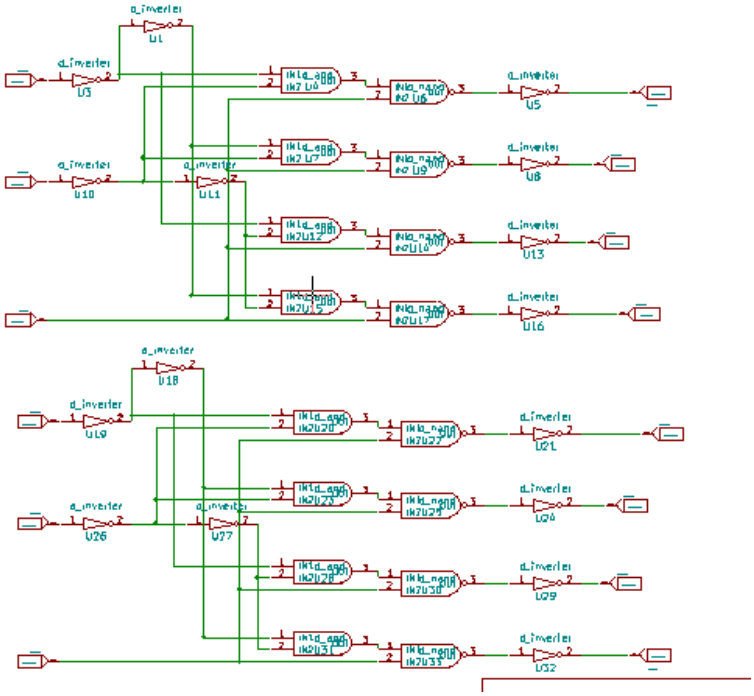
(f) Compatible with CMOS and TTL logic levels.

(g) Suitable for data routing, signal multiplexing, and logic decoding applications.

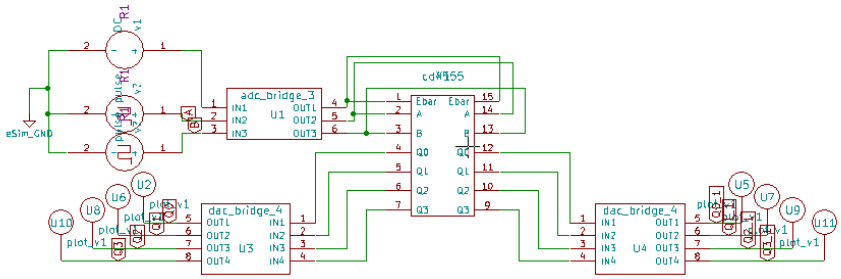
12.3 IC Pin Layout



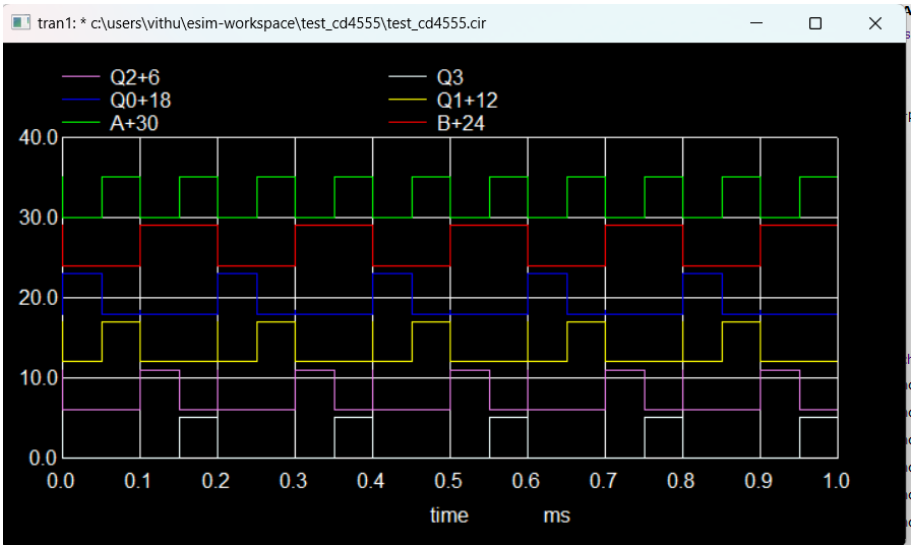
12.4 Circuit Schematic Diagram



12.5 Test Circuit Diagram



12.6 Plot


tran1: * c:\users\vithu\esim-workspace\test_cd4555\test_cd4555.cir
Q2+6
Q0+18
A+30
Q3
Q1+12
B+24
40.0
30.0
20.0
10.0
0.0
0.0
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8
0.9
1.0
time
ms

Chapter 13

CD4556 - Dual 1-of-4 Decoder/Demultiplexer with Inverted Outputs

The **CD4556** is a CMOS-based dual 1-of-4 decoder/demultiplexer IC with inverted outputs. Each decoder includes an **Enable** input that allows activation or deactivation of the corresponding decoder. When the decoder is enabled, it selects one of the four outputs to go low (active low) based on the 2-bit binary input.

This IC is used in applications requiring signal decoding, data routing, or multiplexing with inverted outputs. It operates over a wide voltage range and is compatible with both CMOS and TTL circuits.

13.1 Truth Table (For One Decoder)

Enable	Select (A1, A0)	Y0	Y1	Y2	Y3
L (Low)	X (Don't Care)	H (High)	H (High)	H (High)	H (High)
H (High)	00	L (Low)	H (High)	H (High)	H (High)
H (High)	01	H (High)	L (Low)	H (High)	H (High)
H (High)	10	H (High)	H (High)	L (Low)	H (High)
H (High)	11	H (High)	H (High)	H (High)	L (Low)

13.2 Features:

(a) Dual 1-of-4 decoder/demultiplexer with active-low outputs.

(b) Each decoder has an **Enable** input.

(c) Wide supply voltage range: 3V to 15V.

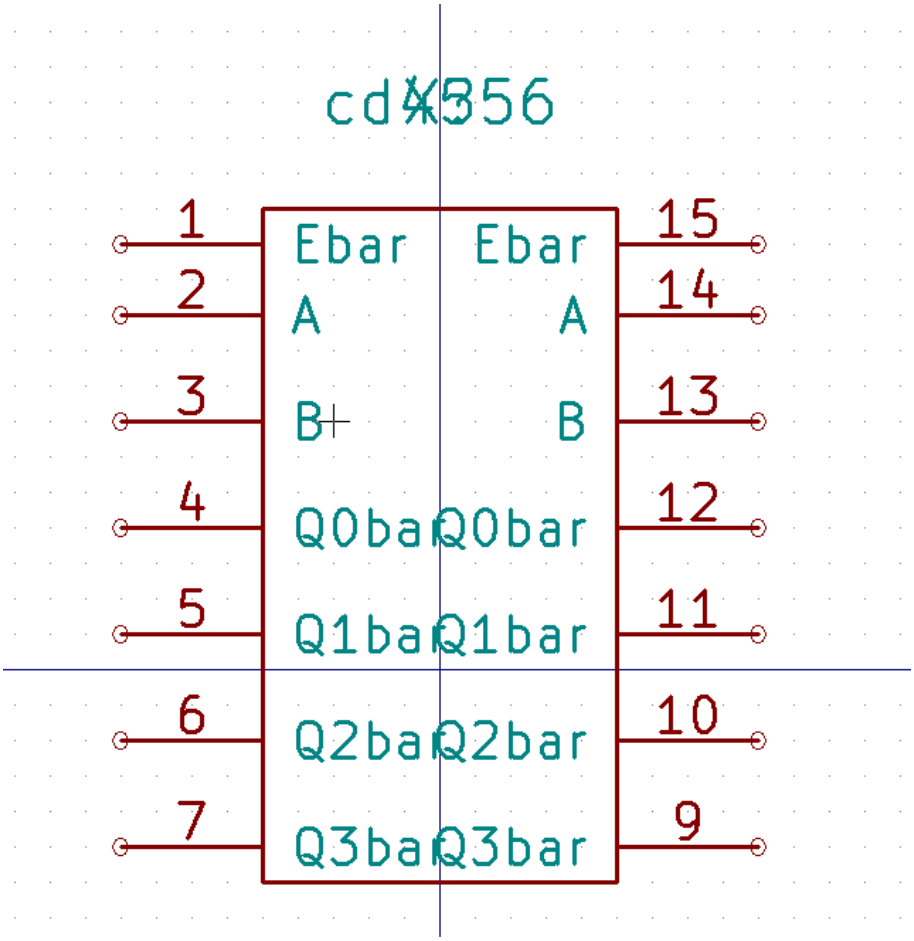
(d) Low power consumption typical of CMOS technology.

(e) High noise immunity for reliable operation.

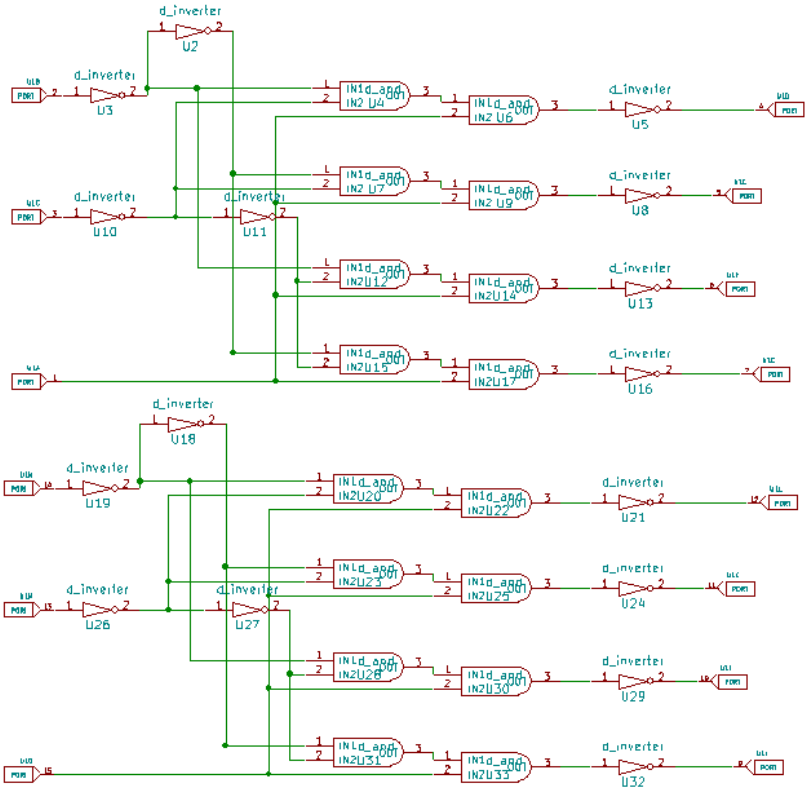
(f) Compatible with CMOS and TTL logic levels.

(g) Suitable for data routing, signal multiplexing, and logic decoding with inverted outputs.

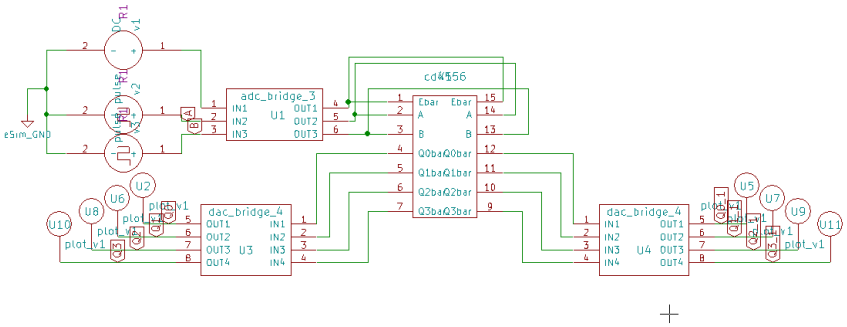
13.3 IC Pin Layout



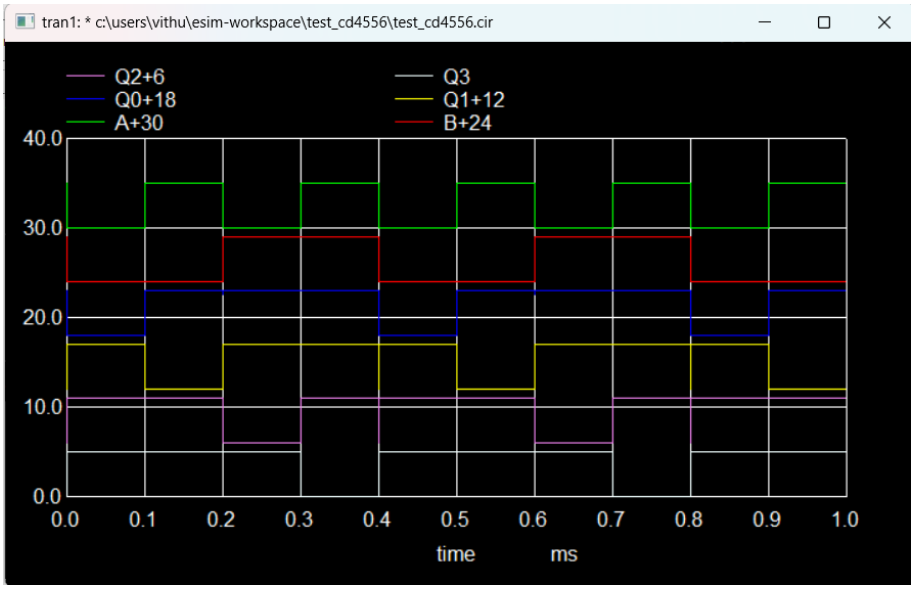
13.4 Circuit Schematic Diagram



13.5 Test Circuit Diagram



13.6 Plot


tran1: * c:\users\vithu\esim-workspace\test_cd4556\test_cd4556.cir
Q2+6
Q0+18
A+30
Q3
Q1+12
B+24
40.0
30.0
20.0
10.0
0.0
0.0
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8
0.9
1.0
time
ms

Chapter 14

CD4086 - Expandable 4-Wide 2-Input AND-OR-INVERT Gate

This implementation uses the CD4086 IC to perform a combination of AND, OR, and INVERT operations. The output J is derived from the following logical expression:

$$J = \overline{(A \cdot B) + (C \cdot D) + (E \cdot F) + (G \cdot H)}$$

Here: - $A \cdot B$, $C \cdot D$, $E \cdot F$, and $G \cdot H$ represent the outputs of four AND gates. - The results of the AND gates are then combined using an OR gate. - The final output is inverted to achieve the desired result.

—

14.1 Truth Table

A	B	C	D	E	F	G	H	J (Output)
0	0	0	0	0	0	0	0	1
0	1	0	1	0	1	0	1	1
1	1	0	0	0	0	0	0	0
1	1	1	1	0	0	0	0	0
1	1	1	1	1	1	1	1	0

The output J is **LOW (0)** when any of the AND conditions evaluate to HIGH (1). It is HIGH (1) only when all AND conditions are false.

—

14.2 Features

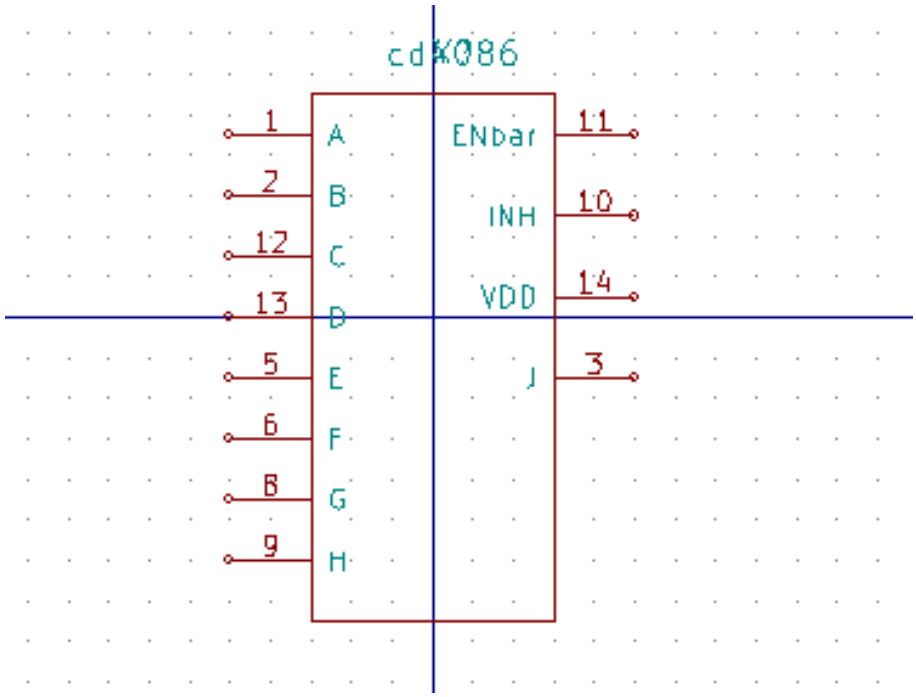
(a) Logic expression: $J = \overline{(A \cdot B) + (C \cdot D) + (E \cdot F) + (G \cdot H)}$.

(b) Combines four AND gates, one OR gate, and one NOT gate.

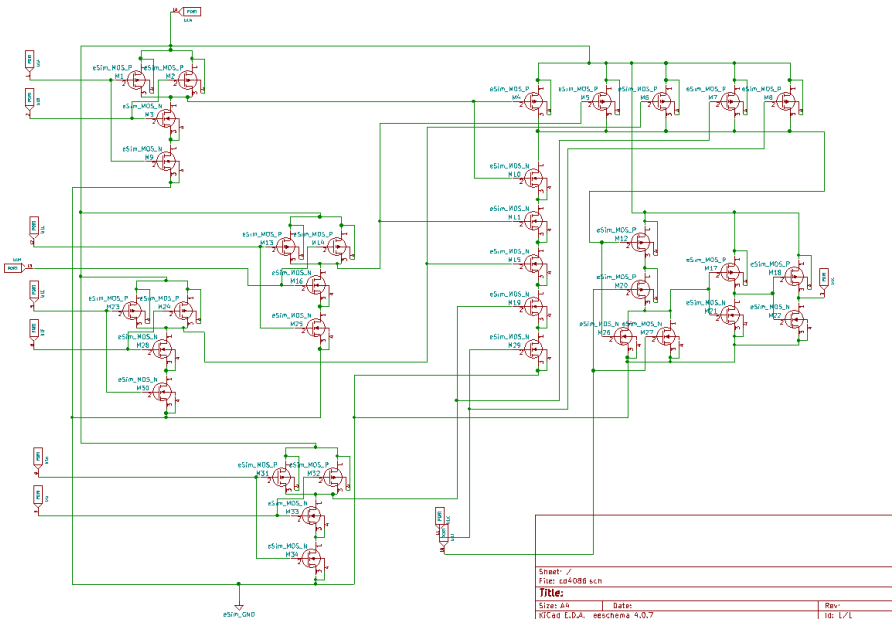
(c) Implements complex logic decisions efficiently.

(d) Suitable for use with CD4086 IC for AND-OR-INVERT (AOI) operation.

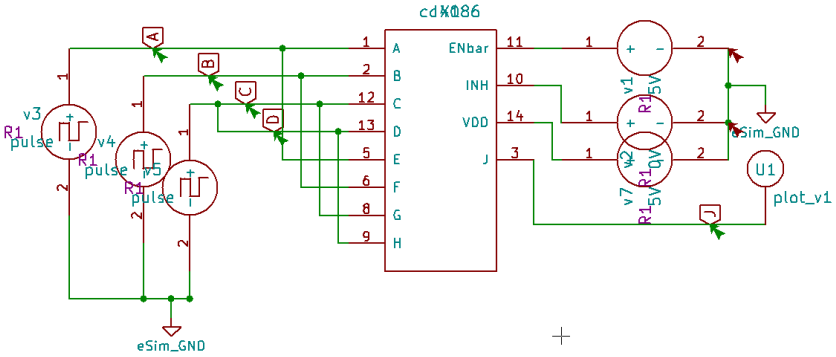
14.3 IC Pin Layout



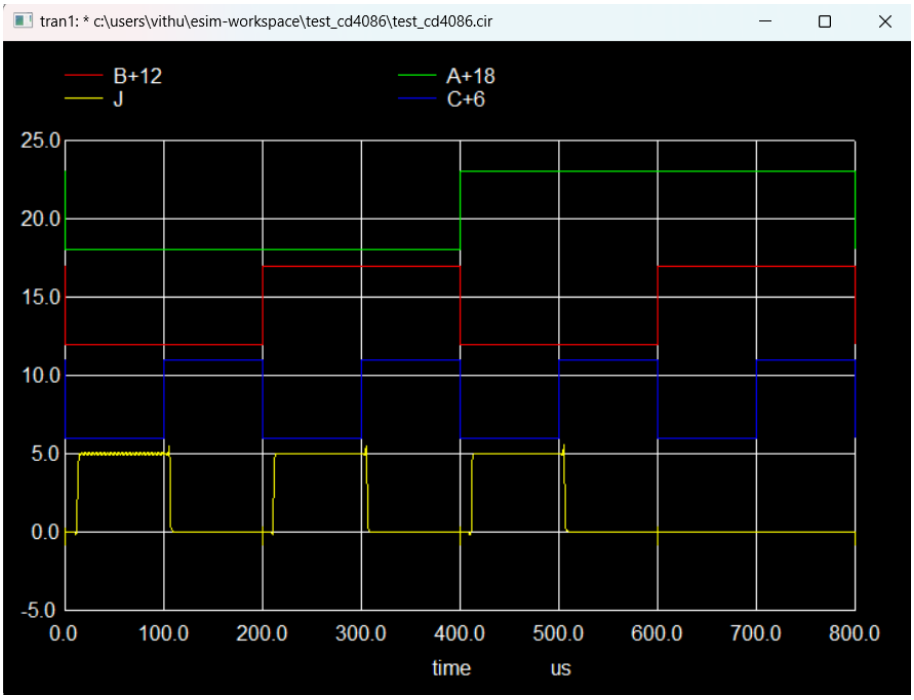
14.4 Circuit Schematic Diagram



14.5 Test Circuit Diagram



14.6 Plot


tran1: * c:\users\vithu\esim-workspace\test_cd4086\test_cd4086.cir
B+12
J
A+18
C+6
25.0
20.0
15.0
10.0
5.0
0.0
-5.0
0.0
100.0
200.0
300.0
400.0
500.0
600.0
700.0
800.0
time
us

Chapter 15

Challenges during Simulation

During my internship, I encountered several challenges while simulating digital ICs, particularly in managing circuit complexity and ensuring accurate, reliable simulations. Addressing these issues required adapting methodologies to suit the type of IC being tested, balancing functionality with efficiency.

1.Complexity of Circuits For logic gate ICs like the CD4010 and CD4030, I used TTL technology, which provided pre-designed, efficient components that simplified multi-gate simulations and ensured realistic performance. However, for other digital ICs like CD40101 and CD4555, using TTL technology made the circuits overly complex and harder to modify. To address this, I directly used individual logic gates, such as AND, OR, and NOT gates, which allowed for greater flexibility in constructing and testing specific logic functions. This approach made it easier to configure, modify, and focus on the behavior of the circuits without unnecessary complications. By adapting my methodology to the type of IC being simulated, I achieved a balance between functionality, efficiency, and simplicity, ensuring accurate and reliable results for different scenarios.

2.Handling Multiple Input Sources For ICs with multiple input sources, I faced runtime and simulation errors caused by using numerous pulse inputs. To overcome this, I minimized the number of power sources by connecting the same pulse source to 3 or 4 input ports, effectively reducing circuit complexity while maintaining accurate outputs. Additionally, for circuits like digital comparator ICs, I replaced excess pulse inputs with DC sources, limiting the use of pulse sources to a maximum of 3 or 4. This strategy resolved simulation errors and ensured reliable circuit performance without compromising functionality.

Chapter 16

Reference

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