Summer Fellowship Report

On

Integrated Circuit Design using Subcircuit feature of eSim

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Acknowledgment

We take this occasion to offer our heartfelt gratitude to the FOSSEE, IIT Bombay Team for offering us this wonderful opportunity to work on the design and integration of multiple sub-circuits in eSim. Working on eSim has prov ided us with invaluable insights into various open-source EDA tools for circuit simulation and their applications in the practical world.

We extend our sincere regards to Prof. Kannan M. Moudgalya for his valuable guidance and motivation to throughout this fellowship program.

We would like to express our heartfelt appreciation to the entire FOSSEE team including our mentors Mr. Sumanto Kar, Mrs. Vineeta Ghavri, and Mrs. Usha Vishwanathan for constantly guiding and mentoring us throughout the duration of our internship.

It is with their support that we have been able to fulfill our project demands successfully. Whenever faced with an issue, our mentors were always accessible to help us assess and debug them. Our learnings from them have been invaluable and shall be of paramount importance to us in the future.

Overall, it was a delightful experience interning at FOSSEE and contributing to its growth and I take away some great insights and knowledge from it. As enthusiastic beginners in the semiconductor industry, this internship is a milestone for us in our pursuit of a successful career.

Contents

Chapter 1

Introduction

FOSSEE which stands for Free/Libre and Open Source Software for Education is an organization, based at IIT Bombay, as a remarkable initiative aimed at promoting the use of open-source software in education and research. It was established with the mission to reduce the dependency on proprietary software and to encourage the adoption of open-source alternatives. FOSSEE offers a wide range of tools and resources that cater to various academic and professional needs.

It provides comprehensive documentation, tutorials, workshops, and hands-on training sessions, for empowering students, educators, and professionals to leverage open-source software for their projects and coursework. The organization's commitment to fostering a collaborative and inclusive environment has significantly contributed to the democratization of technology and has opened up new avenues for innovation and learning.

1.1 eSim

eSim, created by the FOSSEE project at IIT Bombay, is a versatile open-source software tool for circuit design and simulation. It combines various open-source software packages into one cohesive platform, making it easier to design, simulate, and analyze electronic circuits. This tool is particularly useful for students, educators, and professionals who need an affordable and accessible alternative to proprietary software.

eSim offers features for schematic creation, circuit simulation, PCB design, and includes an extensive library of components. The Subcircuit feature is a significant enhancement, enabling users to design complex circuits by integrating simpler subcircuits. Through eSim, FOSSEE promotes the use of open-source solutions in engineering education and professional fields, encouraging innovation and collaboration.

1.2 NgSpice

NgSpice is the open-source spice simulator for electric and electronic circuits. Such a circuit may comprise JFETs, bipolar and MOS transistors, passive elements like R, L, or C, diodes, transmission lines and other devices, all interconnected in a netlist.

Digital circuits are simulated as well, event-driven and fast, from single gates to complex circuits and the combination of both analog and digital as well as a mixed-signal circuits. NgSpice offers a wealth of device models for active, passive, analog, and digital elements. Model parameters are provided by our collections, by the semiconductor device manufacturers, or from semiconductor foundries. The user adds her circuits as a netlist, and the output is one or more graphs of currents, voltages and other electrical quantities or is saved in a data file.

1.3 Makerchip

Makerchip is a platform that offers convenient and accessible access to various tools for digital circuit design. It provides both browser-based and desktop-based environments for coding, compiling, simulating, and debugging Verilog designs. Makerchip supports a combination of open-source tools and proprietary ones, ensuring a comprehensive range of capabilities.

One can simulate Verilog/SystemVerilog/Transaction-Level Verilog code in Makerchip. eSim is interfaced with Makerchip using a Python based application called Makerchip-App which launches the Makerchip IDE. Makerchip aims to make circuit design easy and enjoyable for users of all skill levels. The platform provides a user-friendly interface, intuitive workflows, and a range of helpful features that simplify the design process and enhance the overall user experience.

The main drawback of these open source tools is that they are not comprehensive. Some of them are capable of PCB design (e.g. KiCad) while some of them are capable of performing simulations (e.g. gEDA). To the best of our knowledge, there is no open source software that can perform circuit design, simulation and layout design together. eSim is capable of doing all of the above.

Chapter 2

Features Of eSim

The objective behind the development of eSim is to provide an open source EDA solution for electronics and electrical engineers. The software should be capable of performing schematic creation, PCB design and circuit simulation (analog, digital and mixed-signal). It should provide facilities to create new models and components. Thus, eSim offers the following features -

1. Schematic Creation: eSim provides an easy-to-use graphical interface for drawing circuit schematics, making it accessible for users of all levels. Users can drag and drop components from the library onto the schematic, simplifying the design process. Comprehensive editing tools allow for easy modification of schematics, including moving, rotating, and labeling components.

2. Circuit Simulation: eSim supports SPICE (Simulation Program with Integrated Circuit Emphasis), a standard for simulating analog and digital circuits. Users can perform various types of analysis such as transient, AC, and DC, providing insights into circuit behavior over time and frequency.An integrated waveform viewer helps visualize simulation results, aiding in the analysis and debugging of circuit designs.

3. PCB Design: The PCB layout editor allows users to place components and route traces with precision. eSim includes DRC capabilities to ensure that the PCB design adheres to manufacturing constraints and electrical rules. Users can generate Gerber files, which are standard for PCB fabrication, directly from their designs.

4. Subcircuit Feature: This feature enables users to create complex circuits by integrating smaller, simpler subcircuits, promoting modular and hierarchical design approaches. Subcircuits can be reused in different projects, saving time and effort in redesigning common circuit elements.

5. Open Source Integration: eSim integrates several open-source tools like KiCad, Ngspice, and GHDL, providing a comprehensive suite for electronic design automation. Being open-source, eSim is free to use, making advanced circuit design tools accessible without the need for expensive licenses.

Chapter 3

Problem Statement

To design and develop various Analog and Digital Integrated Circuit Models in the form of sub-circuits using device model files already present in the eSim library. These IC models should be useful in the future for circuit designing purposes by developers and users, once they get successfully integrated into the eSim subcircuit Library.

3.1 Approach

Our approach to implementing the problem statement began with examining datasheets from prominent Integrated Circuit (IC) manufacturers such as Texas Instruments, Analog Devices, and NXP Semiconductors. we selected ICs that offer a diverse range of functionalities, including precision amplifiers, comparators, encoders, and audio amplifiers. After building the subcircuits, we tested them to verify basic circuit configurations using NgSpice simulations. The step-by-step roadmap of this process is outlined below :

1. Analyzing Datasheets : The primary step is to browse through various analog and digital IC datasheets, and hence find suitable circuits to implement in eSim, that are not previously included into the eSim library. Check for the detailed schematic of the IC's and once the component values and the truth table is ascertained, then finalise the IC to be created.

2. Subcircuit Creation : After deciding the IC, we start modeling it as a subcircuit in eSim, using the model files present in the eSim device model library only. The design is strictly according to the information given in the official data-sheets of the ICs.This step also includes building the Symbol/Pin diagram of the IC according to the packaging and pin description given in the data-sheets only.

3. Test Circuit Design : Once the component of the IC is ready, now we can build the test circuits, according to the data-sheets. In this step we build the test cases and test circuits using the component IC.

4. Schematic Testing : Once the test circuits are ready, now it's time to simulate the test circuits so that the output can be obtained in the form of wave-forms and

plots. Here we take help of KiCad to NgSpice conversion and Simulation feature in eSim

If the output of the test circuit is not as per expectation, this implies that the test case has failed, and there is some error in the schematic. In such cases we go back to the design phase of the IC or the test circuits, to look for possible errors and then repeat the testing process again after making required changes.

Once the expected output of the test cases are correct and satisfy the expected results, then in such a case the IC is declared successfully working. The test case has been verified and the designing process is complete.

Chapter 4

Analog IC's

4.1 LM342

The LM342 is a versatile voltage regulator integrated circuit designed to provide a consistent output voltage from a higher input voltage source. It is part of a series of linear regulators known for their simplicity and reliable performance. The LM342 is available in fixed output voltage options, such as 5V or 12V, or it can be adjusted to a specific voltage using external components, making it adaptable for various applications.

This IC incorporates key protection features including current limiting and thermal shutdown. These safeguards help prevent damage to the IC and the circuit it powers by automatically reducing the output current or shutting down if the temperature exceeds safe operating limits. This makes the LM342 a robust choice for maintaining stable voltage in diverse environments and conditions.

4.1.1 Pin Diagram

The pin diagram below provides a detailed illustration of the LM342's pin configuration and connections.Common applications for the LM342 include power supplies for electronic devices, communication equipment, and other systems requiring steady voltage regulation.

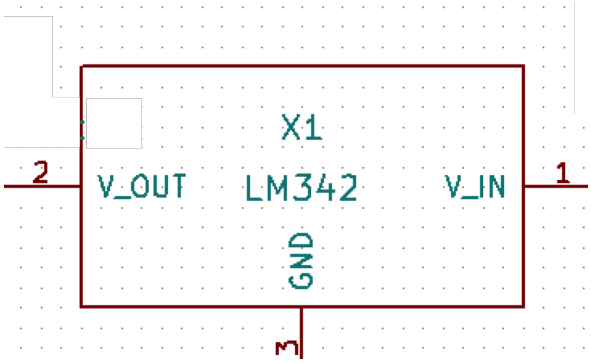


Figure 4.1.1.1: Pin configuration of the LM342 voltage regulator.

4.1.2 Sub Circuit Layout

The subcircuit layout presented here represents the detailed design of the LM342 voltage regulator IC at the transistor level. This layout includes all essential components such as the input and output capacitors, bypass capacitors, and any necessary thermal management features. The design is meticulously crafted to ensure stable operation and optimal performance of the IC in various applications

Its straightforward design, which typically involves only a few additional components like capacitors, makes it a practical choice for both hobbyists and professionals in electronics design.

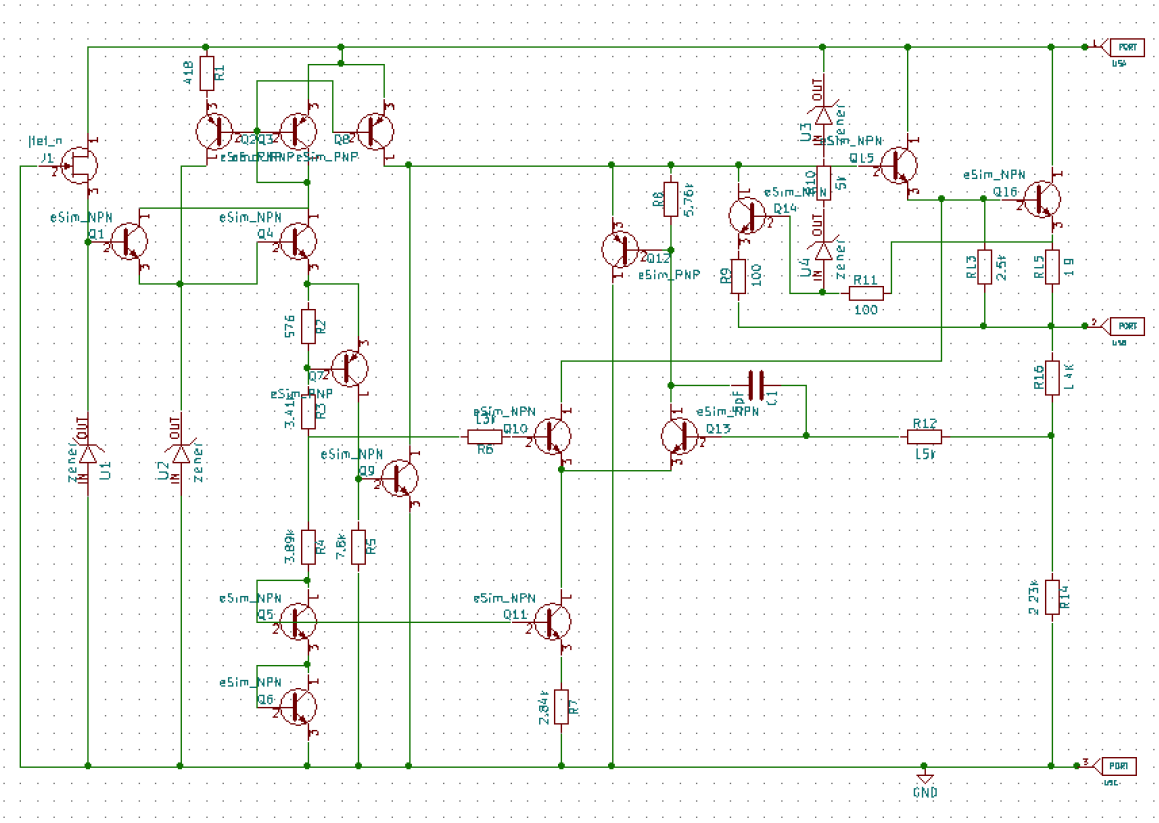


Figure 4.1.2.1: Subcircuit layout of the LM342 voltage regulator.

4.1.3 Test Circuit

The test circuit for the LM342 voltage regulator is designed to evaluate the performance and functionality of the IC using a subcircuit approach. By utilizing the Subcircuit feature, this test circuit can be easily integrated into simulation and analysis environments to verify the IC's behavior under various conditions before final implementation.

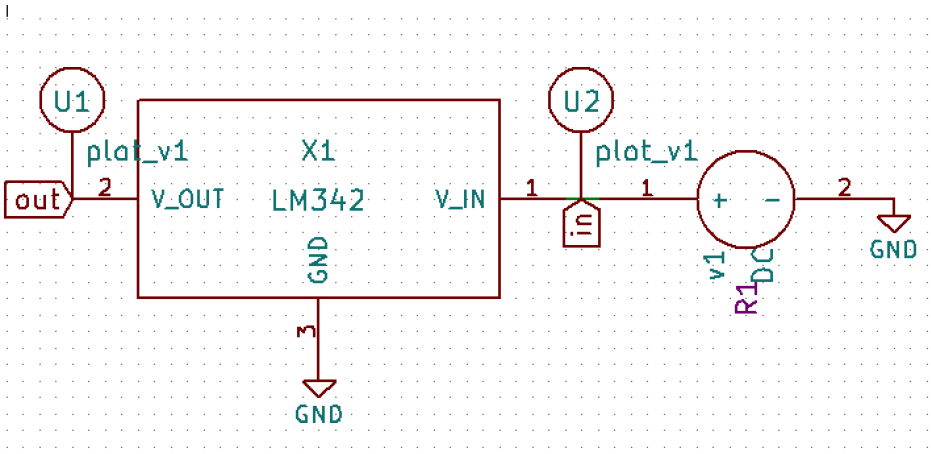


Figure 4.1.3.1: Test circuit setup for the LM342 voltage regulator.

4.1.4 Input Waveform

In this test circuit, the LM342 voltage regulator is provided with a 35 V DC input. This input voltage is regulated by the LM342 to produce a stable lower output voltage. The use of a 35 V DC input ensures that the regulator operates within its designed input range, allowing for a comprehensive evaluation of its performance under high input conditions.

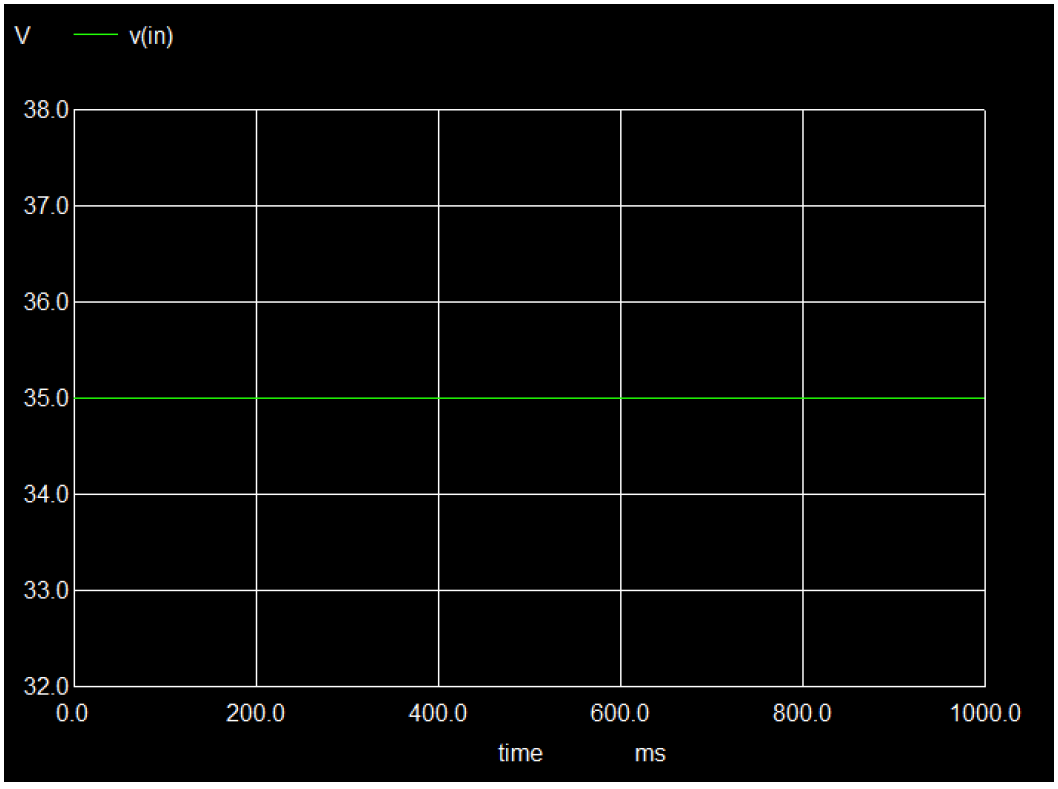


Figure 4.1.4.1: Input waveform for the LM342 voltage regulator.

The image below illustrates the waveform of the 35 V DC input, highlighting its stability and consistency as it enters the voltage regulator:

4.1.5 Output Waveform

The LM342 voltage regulator delivers a regulated output voltage of approximately 5 V. In the test circuit, the LM342 successfully maintains an output of 4.98 V, which is effectively rounded to 5 V. This regulated output is crucial for applications that require a stable 5 V power supply, ensuring reliable operation of connected electronic components.

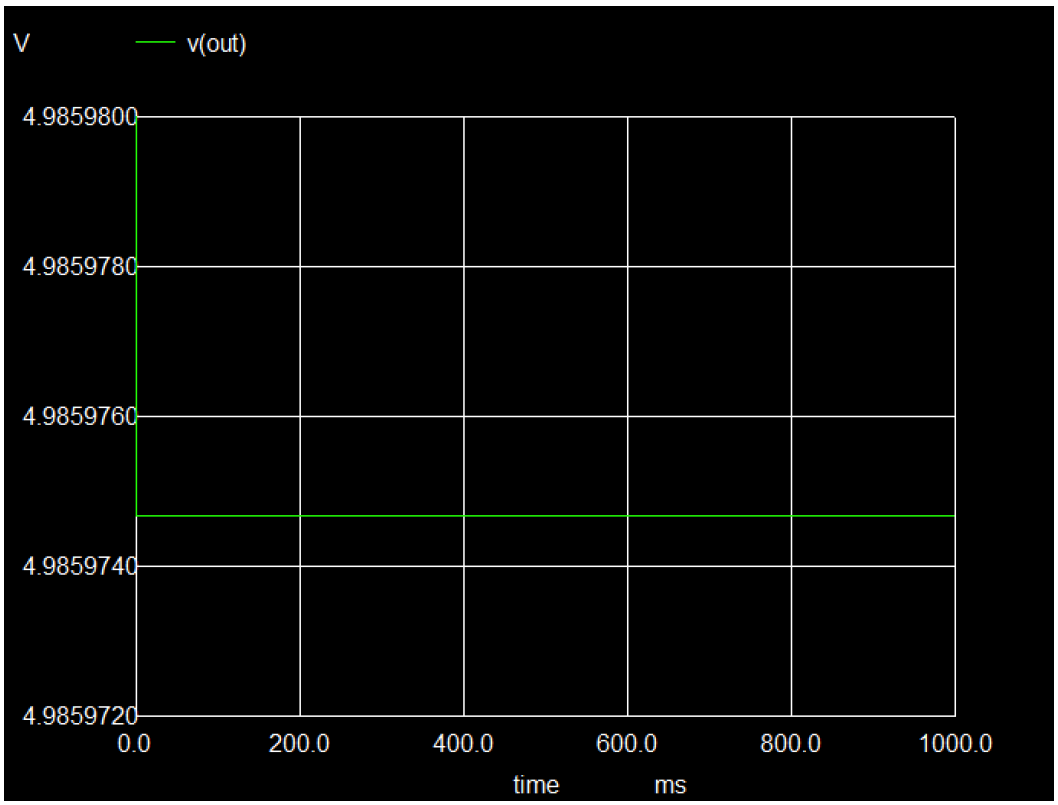


Figure 4.1.5.1: Output waveform of the LM342 voltage regulator.

4.2 LM109

The LM109 is a 5V voltage regulator designed for fixed-output voltage applications. It provides a stable 5V output with a high current capacity and is ideal for use in systems requiring low noise and stable power supply. The LM109 is well-suited for regulated power supplies in computers, communication systems, and other sensitive electronics due to its low dropout voltage and built-in protection features.

4.2.1 Pin Diagram

Describes the pin configuration of the LM109 voltage regulator, showing the input, output, and ground pins. Proper pin connections are essential to ensure stable 5V output from the regulator.

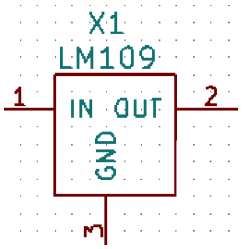


Figure 4.2.1.1: Pin Configuration of LM109

4.2.2 Sub Circuit Layout

Illustrates the internal design of the LM109, highlighting the regulation mechanism that maintains a steady 5V output with built-in short-circuit and thermal protection.

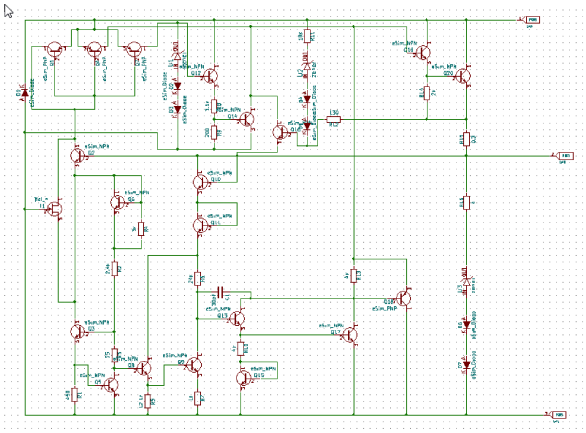


Figure 4.2.2.1: Subcircuit layout of the LM109

4.2.3 Test Circuit

Provides a test circuit setup for evaluating the LM109's performance, showing the correct connection of input voltage, output load, and ground to verify stable operation under various conditions.

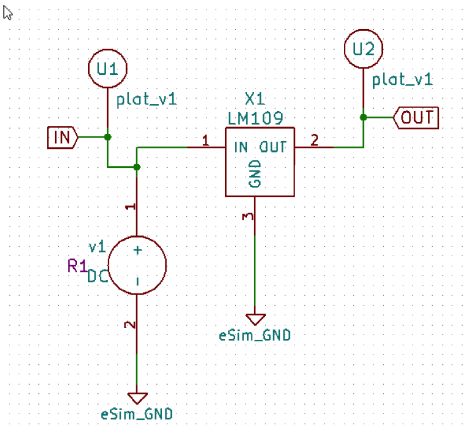


Figure 4.2.3.1: Test Circuit of the LM109

4.2.4 Input Waveform

Depicts the input voltage waveform, showing how the LM109 handles variations in input voltage while maintaining a constant output.

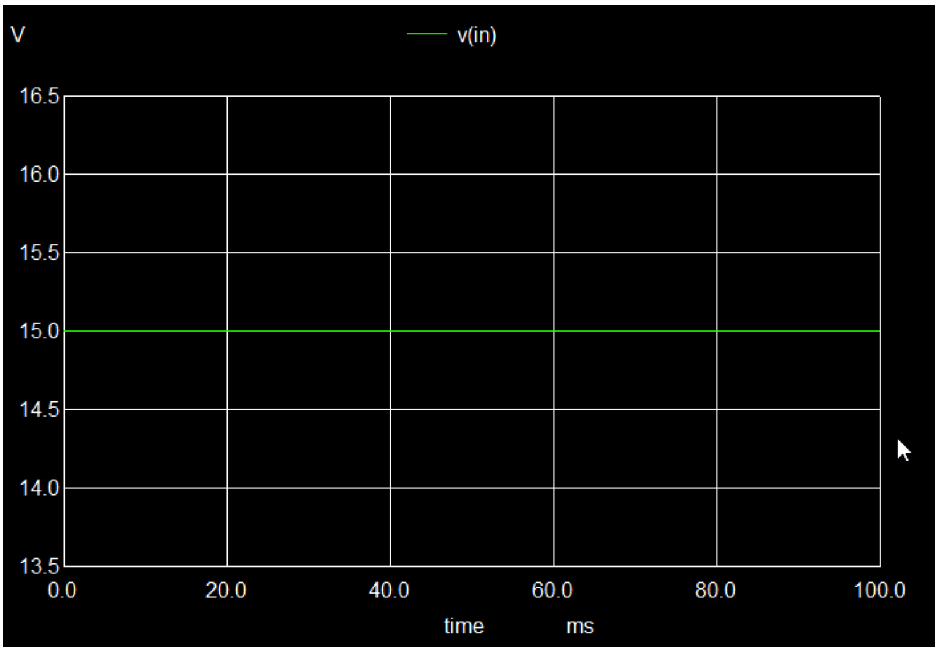


Figure 4.2.4.1: Vin of the LM109

This helps in analyzing the regulator's response to supply fluctuations.

4.2.5 Output Waveform

Displays the output voltage waveform, demonstrating the 5V regulated output under different load conditions and input variations. This showcases the LM109's stability and efficiency.

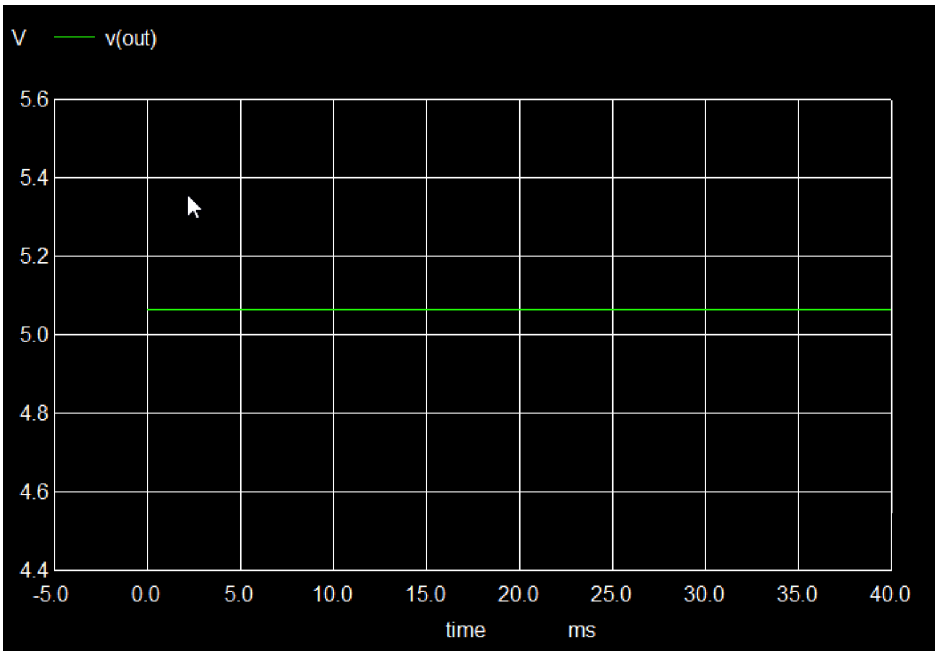


Figure 4.2.5.1: V out of the LM109

4.3 LM124

The LM124 is a quad op-amp (operational amplifier) IC that contains four independent, high-gain, internally compensated amplifiers designed to operate from a single or split power supply. It is commonly used in signal amplification, filtering, and other analog signal processing applications. The LM124 is well-known for its low power consumption, making it suitable for battery-operated devices.

4.3.1 Pin Diagram

Shows the pin configuration of the LM124, indicating the connections for the four operational amplifiers, power supply, and ground. Understanding the pinout is important for integrating the op-amp into circuits.

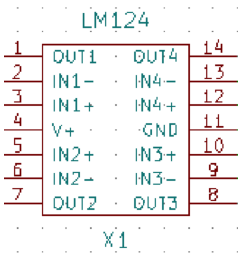


Figure 4.3.1.1: Pin Configuration of LM124

4.3.2 Sub Circuit Layout

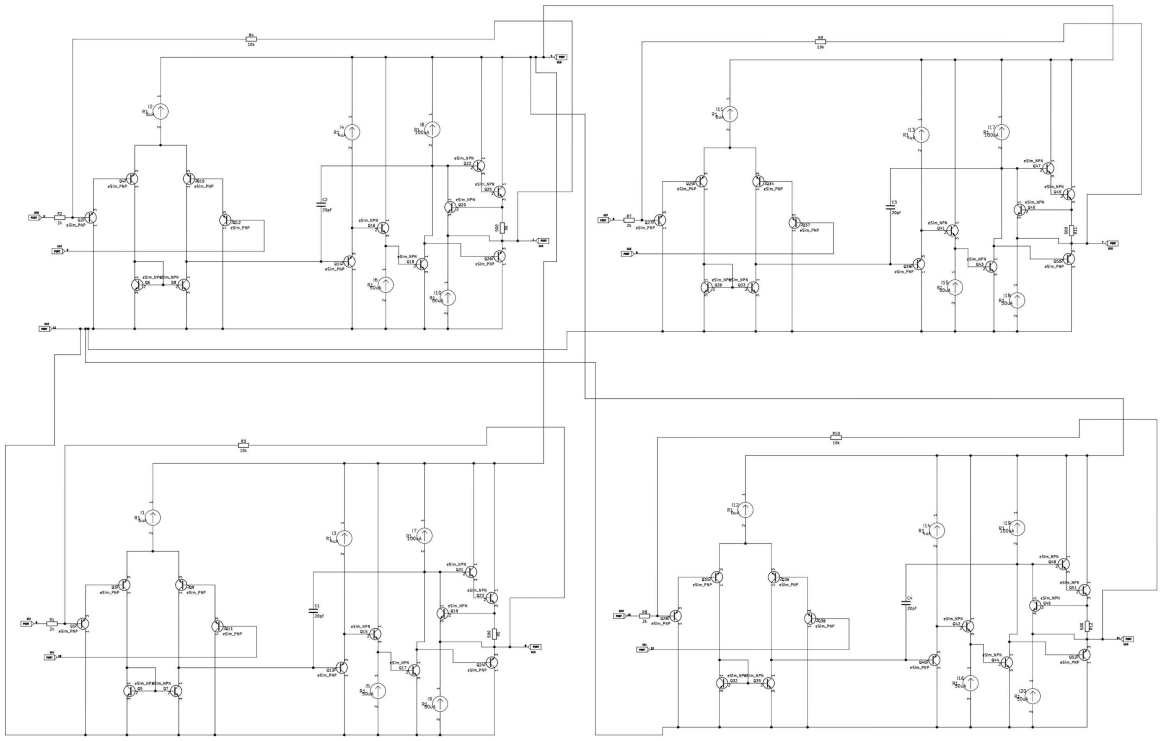


Figure 4.3.2.1: Subcircuit layout of the LM124

Illustrates the internal block diagram of the LM124, showing how the four independent op-amps are connected within the IC, along with their feedback and compensation mechanisms.

4.3.3 Test Circuit

Provides a typical test circuit to demonstrate the operation of each op-amp within the LM124. This includes input, output, power supply connections, and feedback configurations for different applications.

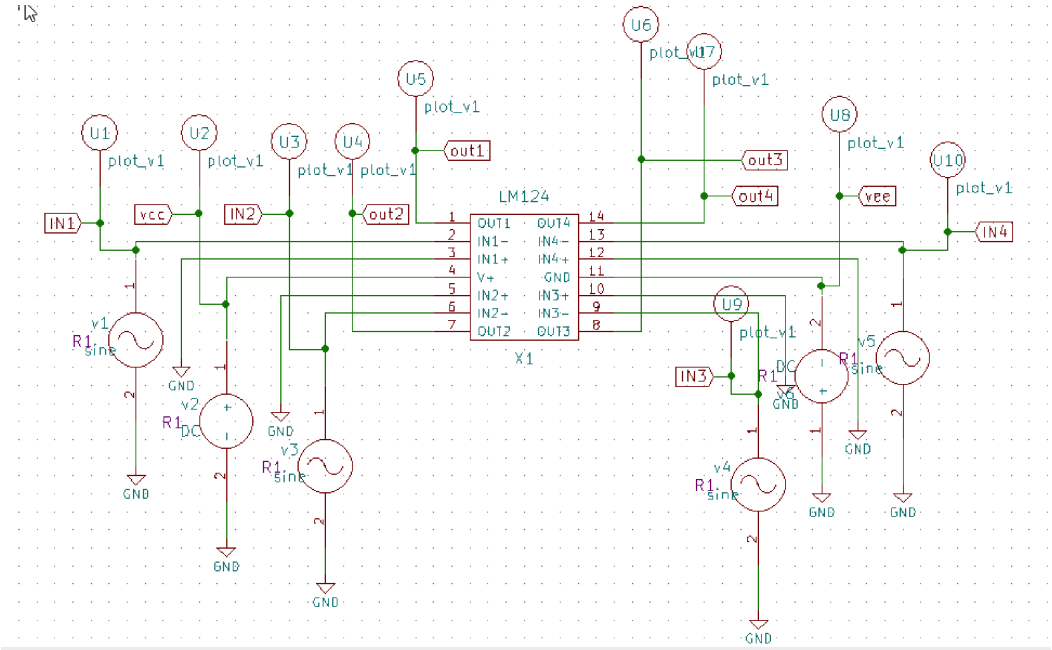


Figure 4.3.3.1: Test Circuit of LM124

4.3.4 Input Waveform

Displays the input signal waveform applied to one of the operational amplifiers, highlighting how the LM124 processes and amplifies the analog input signal.

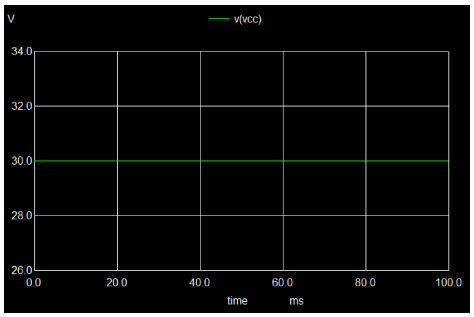


Figure 4.3.4.1: VCC LM124

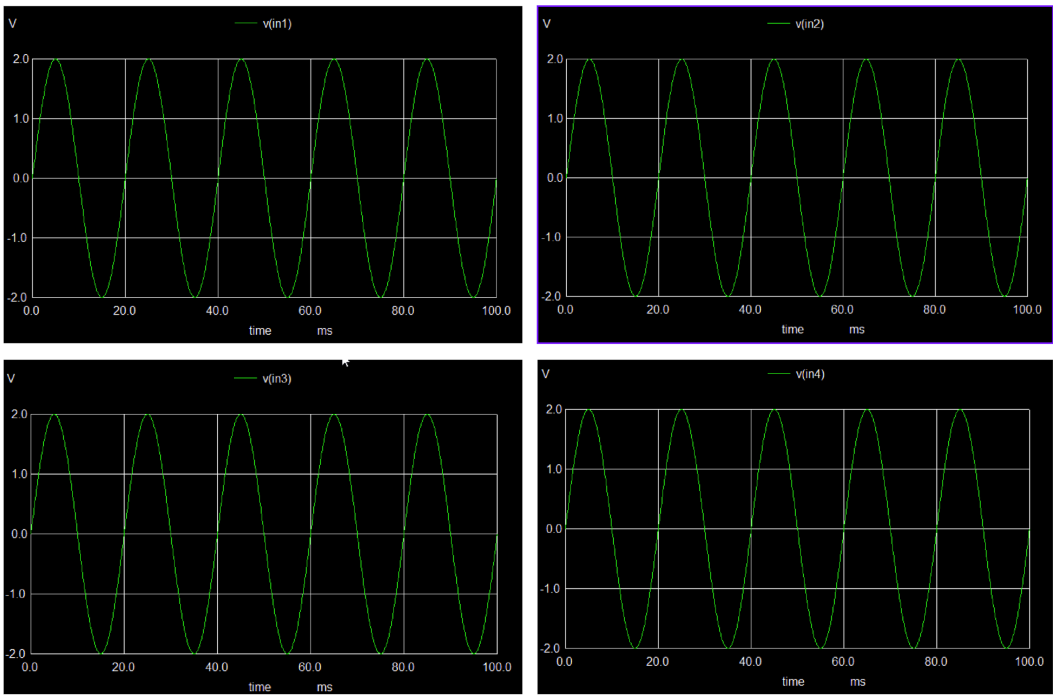


Figure 4.3.4.2: Input Wave form of LM124

4.3.5 Output Waveform

Shows the output waveform generated by the LM124, indicating how the op-amp amplifies the input signal and responds to changes in input, feedback, and power supply conditions.

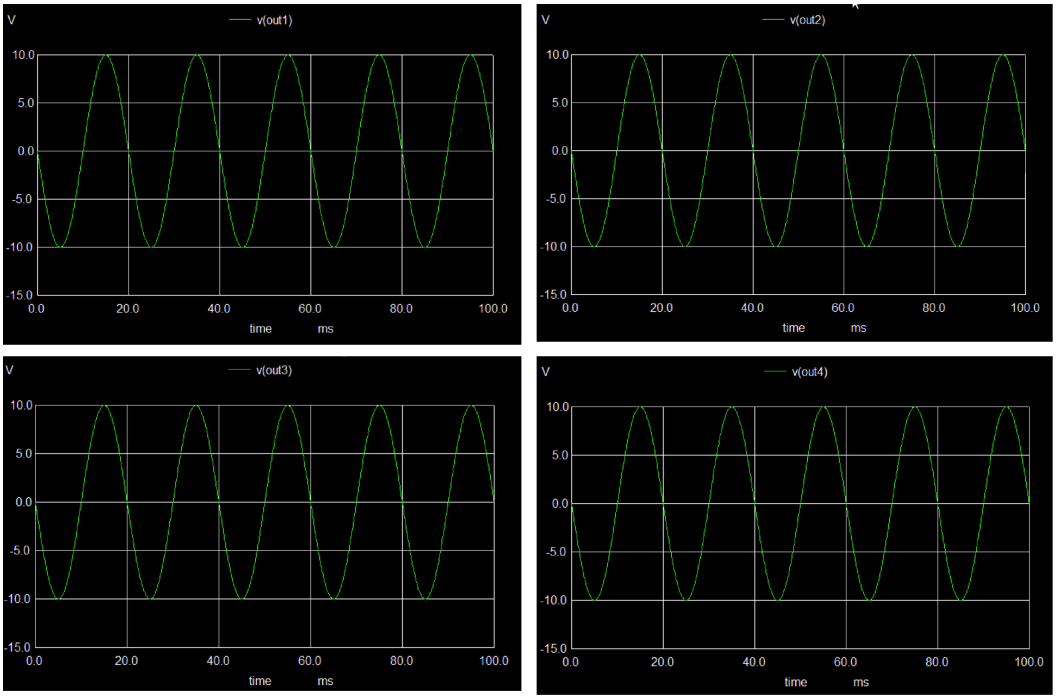


Figure 4.3.5.1: Output Wave form of LM124

4.4 LM2901

The LM2901 is a quad comparator IC that consists of four independent voltage comparators, designed to operate from a single or split power supply. It is widely used in applications such as signal comparison, zero-crossing detectors, and voltage level detection. The LM2901 offers low power consumption and is ideal for industrial, automotive, and consumer electronics applications.

4.4.1 Pin Diagram

Shows the pin configuration of the LM2901, detailing the connections for the four independent comparators, power supply, ground, and input/output pins. This is essential for correctly wiring the IC in circuits.

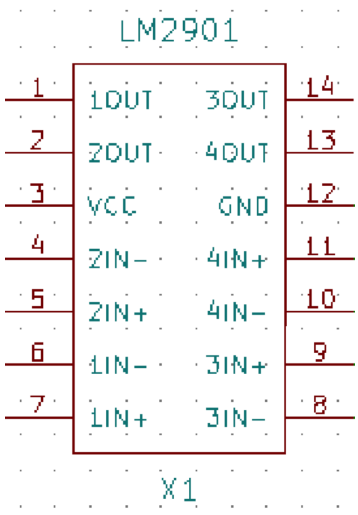


Figure 4.4.1.1: Pin Configuration of LM2901

4.4.2 Sub Circuit Layout

Illustrates the internal block diagram of the LM2901, showing how each of the four comparators is structured and connected to the power supply and control pins. It highlights the voltage comparison mechanism within the IC.

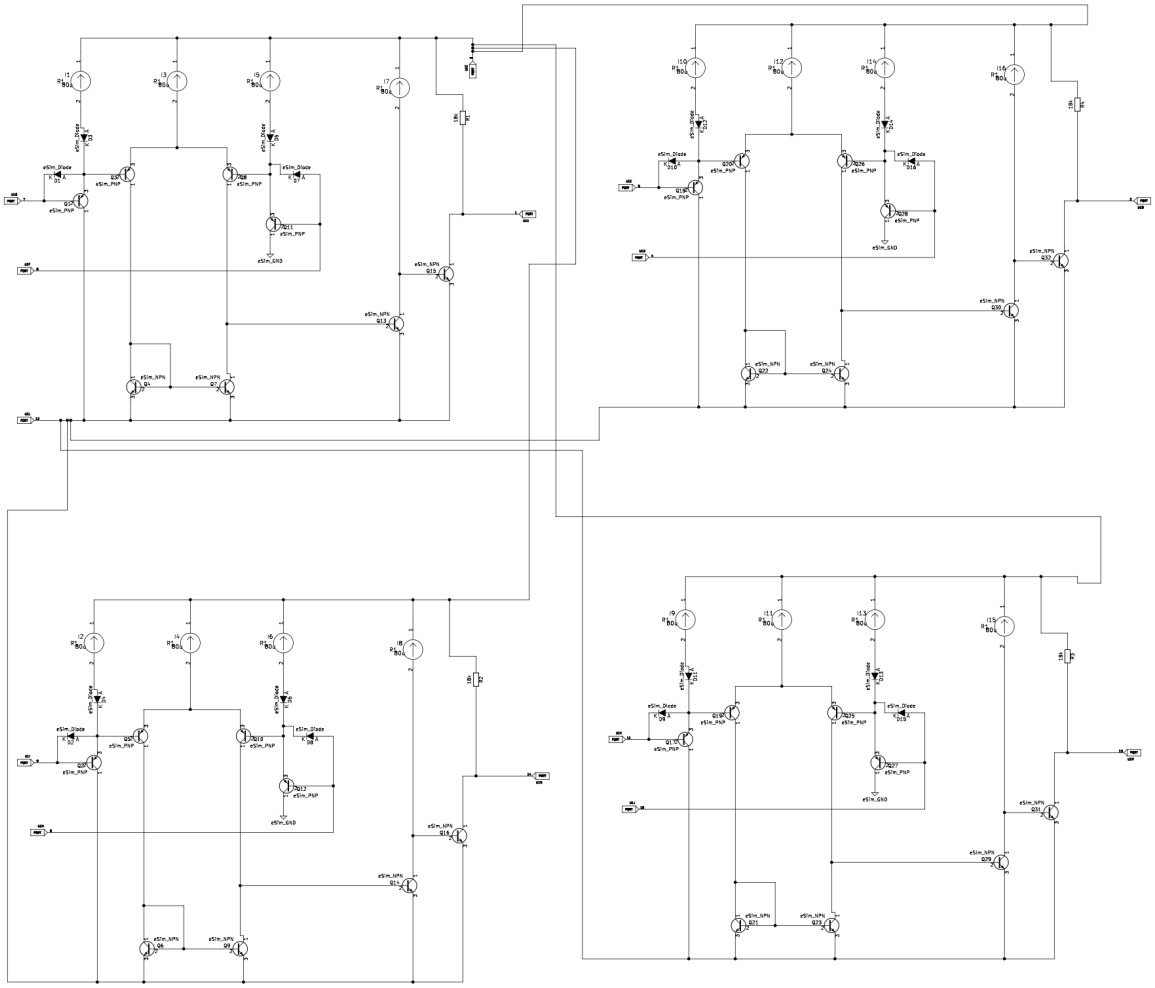


Figure 4.4.2.1: Subcircuit layout of the LM2901

4.4.3 Test Circuit

Describes a typical test circuit for evaluating the performance of one of the comparators in the LM2901, including the input voltage signal, reference voltage, and output connections.

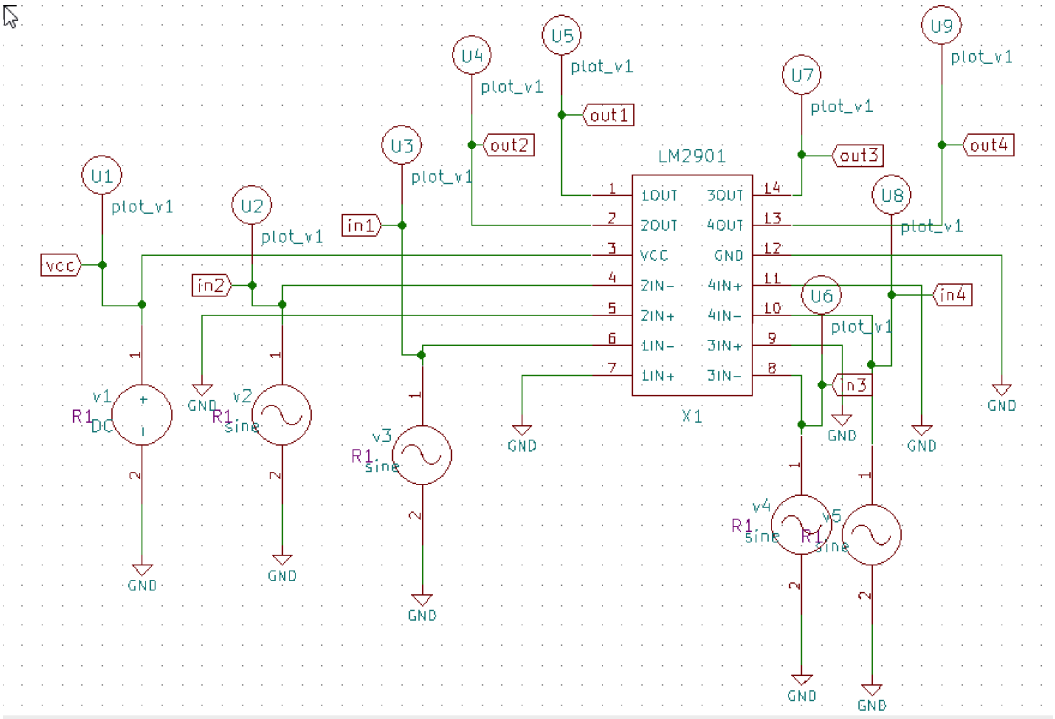


Figure 4.4.3.1: Test Circuit Layout of the LM2901

4.4.4 Input Waveform

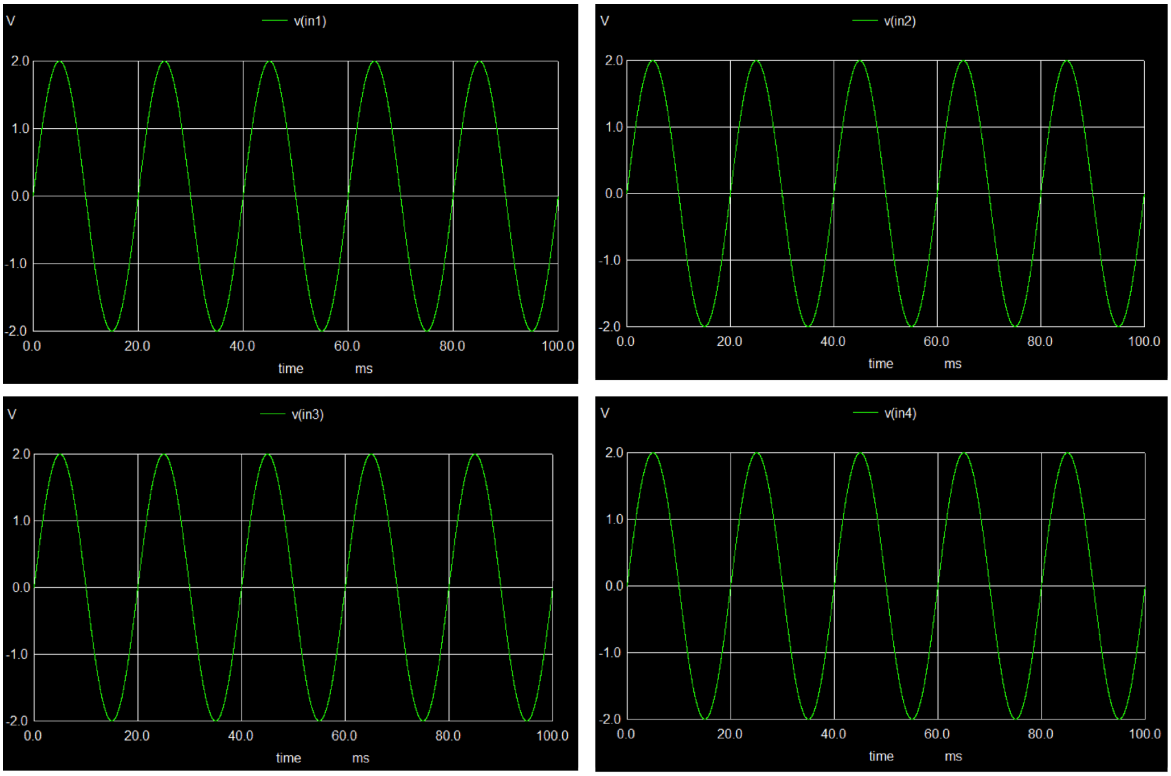


Figure 4.4.4.1: Input Wave form of LM2901

Depicts the input waveform provided to one of the comparators, showing how the input voltage is compared to a reference voltage and how the comparator determines the output.

4.4.5 Output Waveform

Displays the output waveform generated by the LM2901 in response to the input signal, showing how the comparator switches its output when the input voltage crosses the reference threshold.

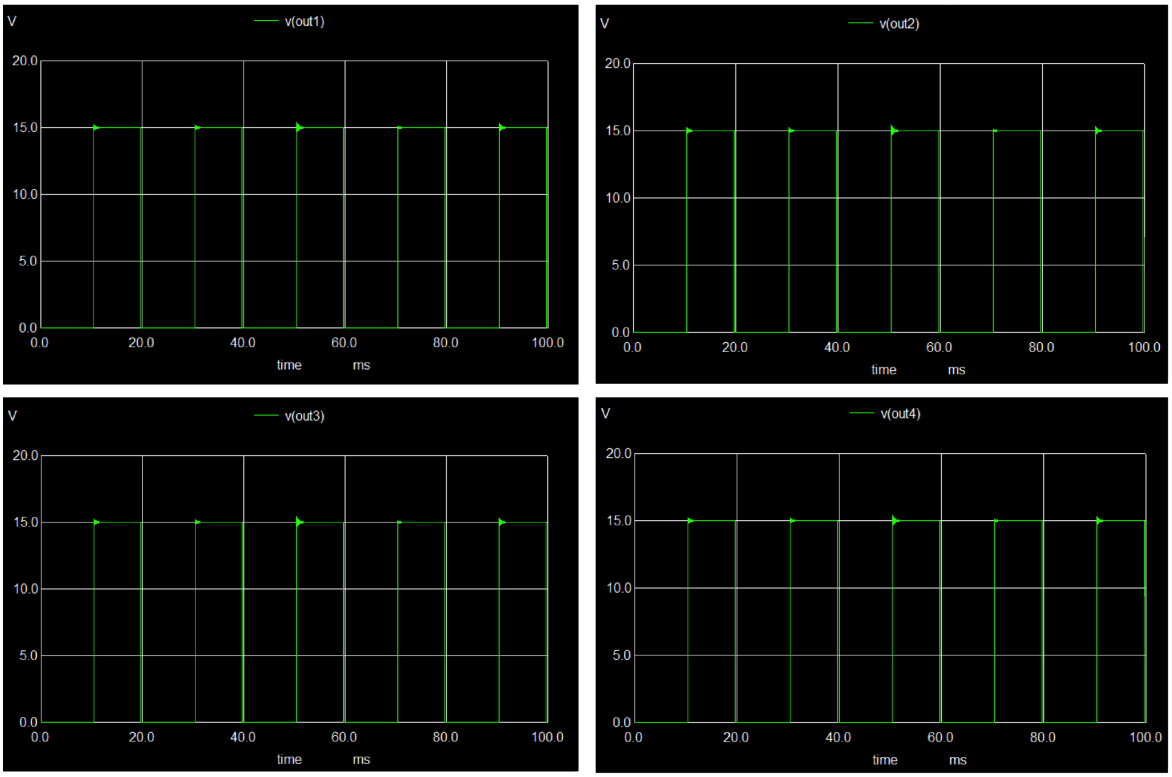


Figure 4.4.5.1: Output Wave form of LM2901

4.5 LM317

The LM317 is an adjustable 3 terminal positive voltage regulator capable of supplying in excess of 1.5 A over an output voltage range of 1.2 V to 37 V. This voltage regulator is exceptionally easy to use and requires only two external resistors to set the output voltage.

4.5.1 Pin Diagram

The LM317 voltage regulator features a simple three-pin layout: Input, Output, and Adjust. The Input pin receives the unregulated voltage, which is then stabilized by the regulator. The Output pin delivers the regulated voltage to the load.

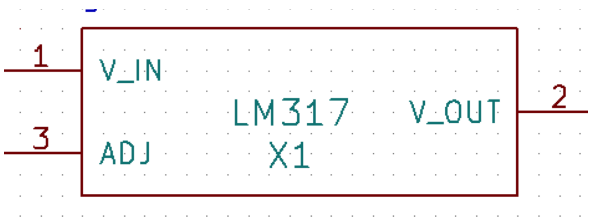


Figure 4.5.1.1: Pin configuration of the LM317 voltage regulator.

The Adjust pin is used to set the output voltage by connecting external resistors. This clear and intuitive pin configuration allows for straightforward integration into circuits and facilitates easy adjustment of the output voltage.

4.5.2 Sub Circuit Layout

The subcircuit layout for the LM317, based on the specifications provided in the datasheet, includes the IC itself along with essential components such as input and output capacitors and resistors for voltage adjustment.

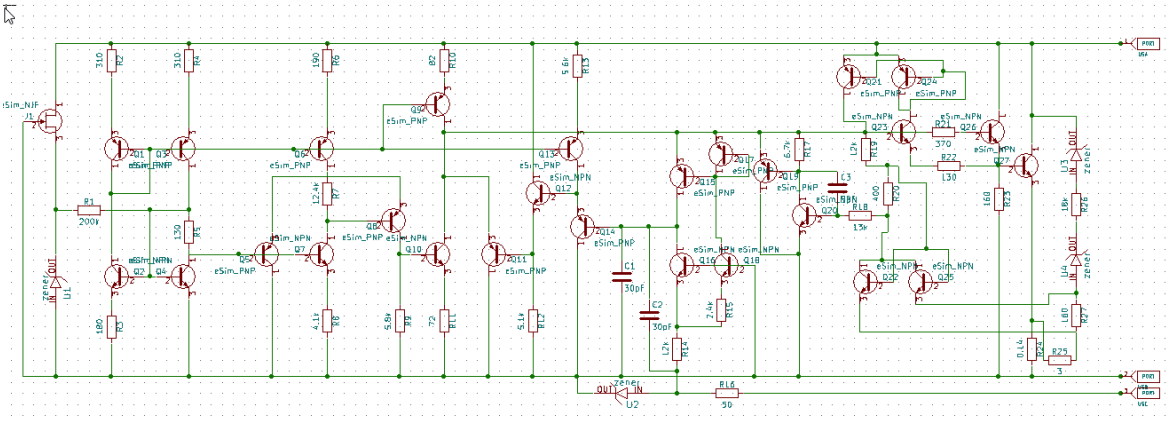


Figure 4.5.2.1: Subcircuit layout of the LM317 voltage regulator.

This layout represents how the LM317 should be integrated into a circuit to achieve precise voltage regulation. The accompanying figure illustrates the construction of the subcircuit, showing how these components are arranged to ensure accurate performance and reliable operation.

4.5.3 Test Circuit

The test circuit for the LM317, constructed according to the guidelines in the datasheet, is designed to evaluate the regulator's performance under realistic conditions. This circuit includes the LM317 IC, an input voltage source, and the necessary capacitors and resistors.

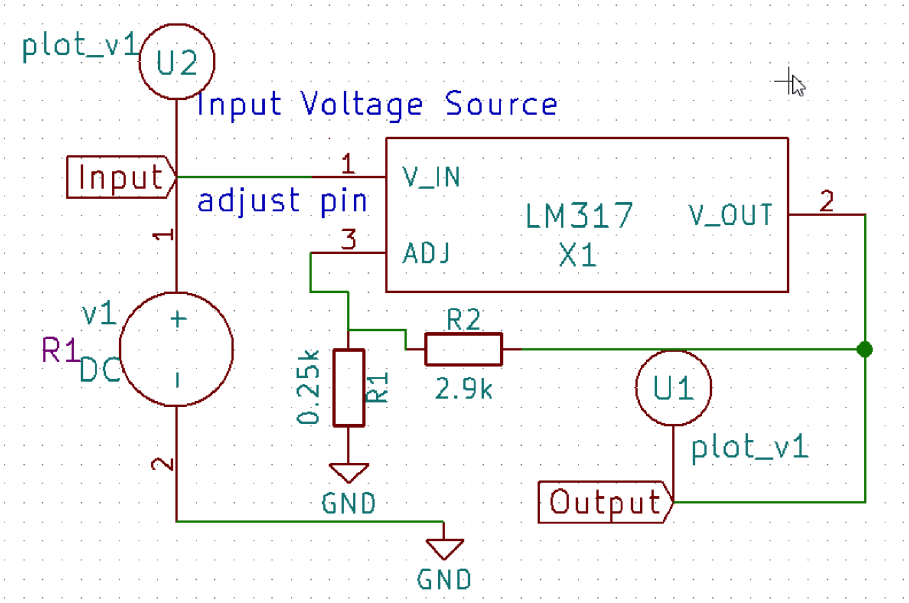


Figure 4.5.3.1: Test circuit setup for the LM317 voltage regulator.

In this setup, the adjust pin is utilized to modify the output voltage. By connecting a resistor, as shown in the test, you can adjust the voltage to achieve the correct or desired output. This configuration is essential for assessing the LM317 regulator's performance before it is used in practical applications.

4.5.4 Input Waveform

The input waveform, as depicted in the provided figure, illustrates the unregulated voltage supplied to the LM317's Input pin. This waveform is crucial for verifying that the input voltage is sufficient for effective regulation.According to the datasheet, the input voltage must be higher than the output voltage to accommodate the regulator's dropout voltage. The waveform visualization helps confirm that the input conditions meet the requirements for reliable performance.

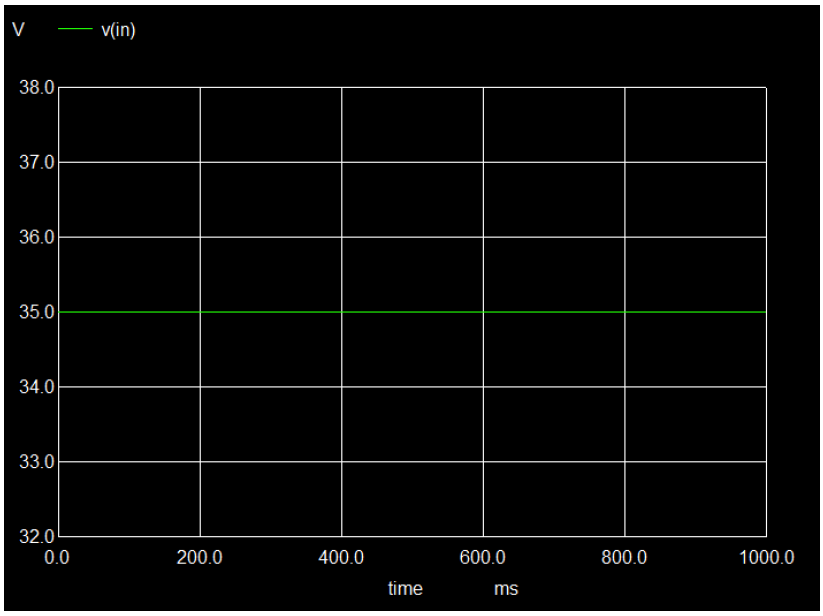


Figure 4.5.4.1: Input waveform for the LM317 voltage regulator.

4.5.5 Output Waveform

The output waveform, shown in the accompanying figure, represents the regulated voltage provided by the LM317. This waveform demonstrates the IC's capability to maintain a stable output voltage despite variations in the input voltage or load conditions.

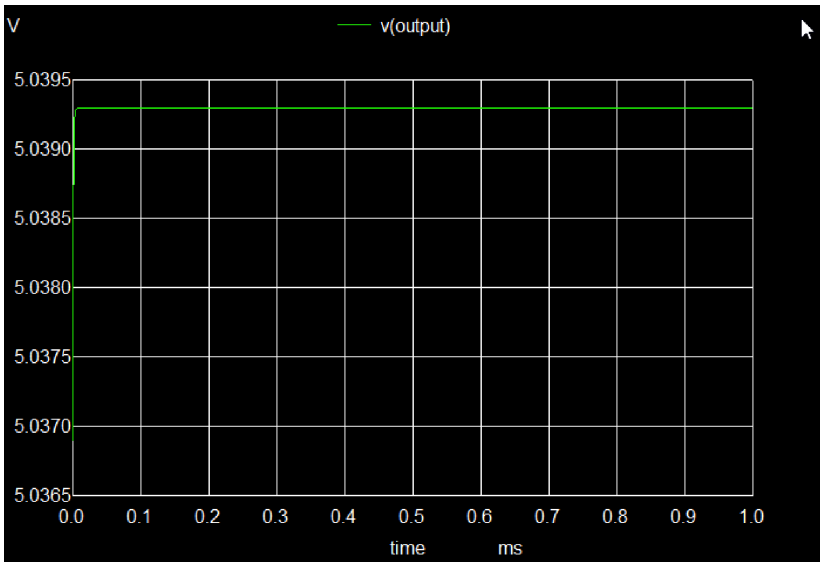


Figure 4.5.5.1: Output waveform of the LM317 voltage regulator.

The datasheet specifies the expected performance, and the waveform analysis verifies that the LM317 delivers the desired output voltage with minimal fluctuation.

Chapter 5

Digital IC's

5.1 SN74ALS280

The SN74ALS280 is an 8-bit parity generator/checker IC that is primarily used for error detection in digital communication systems. It generates both even and odd parity bits, ensuring data integrity by checking for transmission errors.

5.1.1 Pin Diagram

The SN74ALS280 has a 20-pin configuration. Pins 1 to 8 are data inputs (A1-A8), Pin 9 is the ground (GND), Pin 10 gives the even parity output, Pin 11 provides the odd parity output, Pins 12-19 are additional inputs, and Pin 20 is the Vcc (power supply).

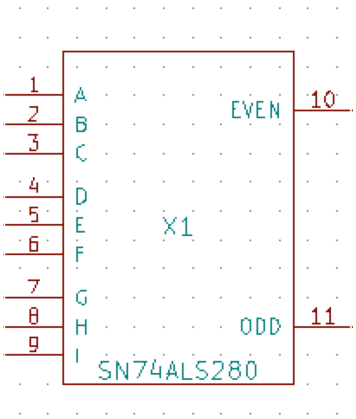


Figure 5.1.1.1: Pin Configuration of SN74ALS280

5.1.2 Sub Circuit Layout

n the sub-circuit layout, data inputs A1-A8 are fed into the IC, which generates even and odd parity bits at Pins 10 and 11. These outputs are then connected to external circuits to monitor and handle errors in the transmitted data.

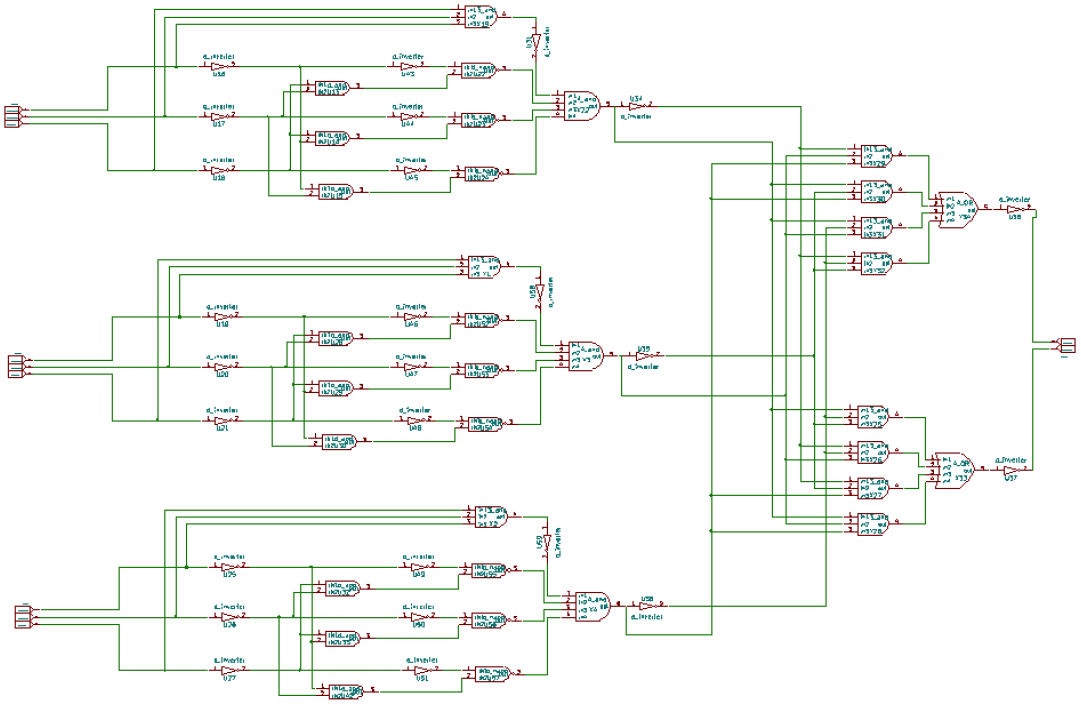


Figure 5.1.2.1: Subcircuit layout of the SN74ALS280

5.1.3 Test Circuit

The test circuit involves using a binary counter connected to the data input pins (A1-A8) to provide a range of input values. The parity outputs are observed using logic probes to verify the accuracy of the parity generation at different input states.

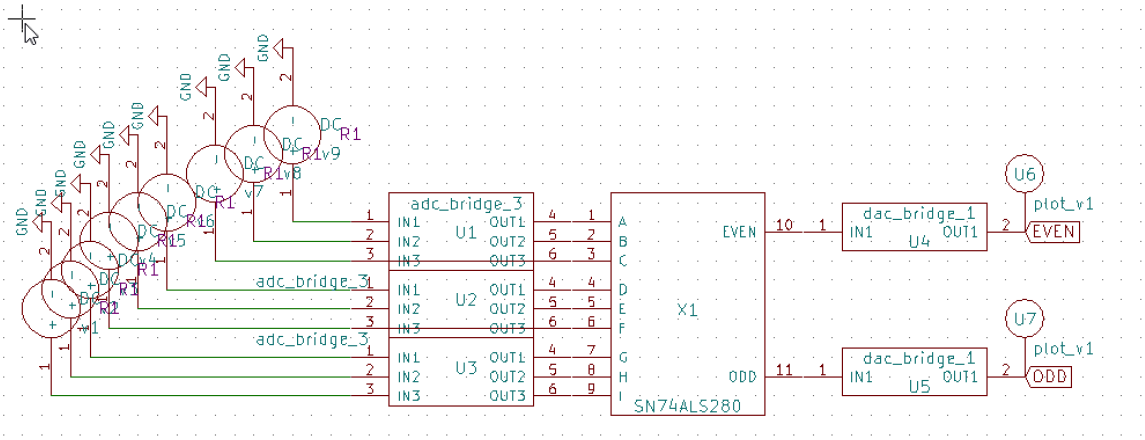


Figure 5.1.3.1: Test Circuit of SN74ALS280

5.1.4 Input Waveform

The input waveform consists of binary data ranging from 00000000 to 11111111, representing all possible 8-bit combinations. This waveform is generated by the binary counter and is fed into the SN74ALS280 to test its parity functionality.

Input as : 1) A=High, rest is Low 2) Addition = 1

5.1.5 Output Waveform

The output waveform shows the even and odd parity bits generated in response to the input data. For example, when the number of '1's in the input data is even, the even parity output is high, and when odd, the odd parity output is high.

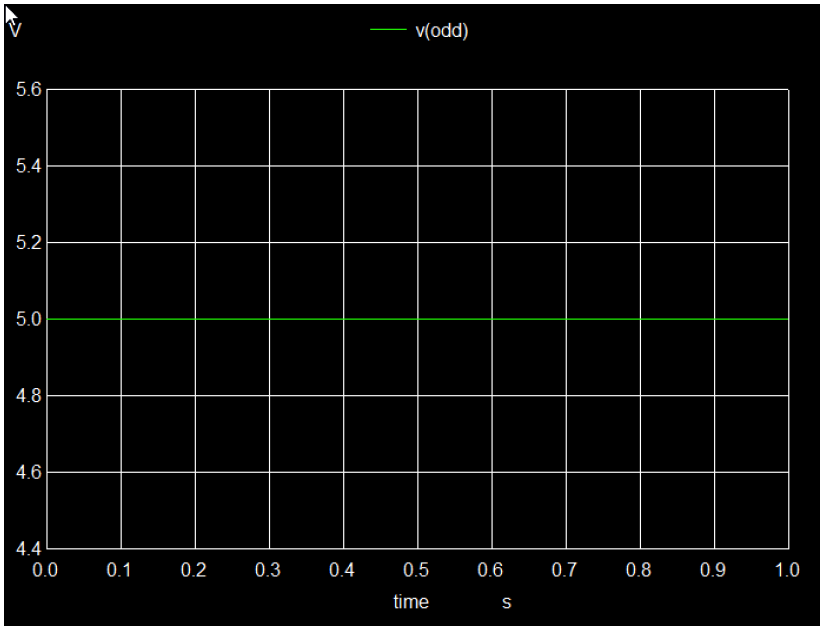


Figure 5.1.5.1: Out 1 of the SN74ALS280

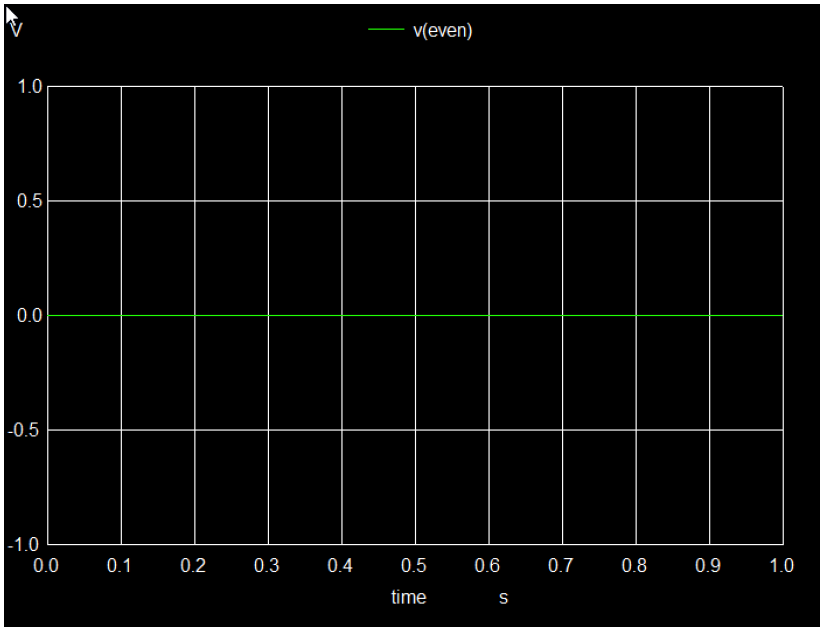


Figure 5.1.5.2: OUT 2 of the SN74ALS280

5.2 MC74HC238

The MC74HC238 is a high-speed CMOS 3-to-8 line decoder/demultiplexer. It is designed to decode a 3-bit binary input into one of eight outputs, each of which is active LOW. This IC is commonly used in digital systems to select one of several outputs or to address multiple lines in memory systems. The high-speed CMOS technology ensures quick response times and low power consumption, making it suitable for a wide range of applications.

5.2.1 Pin Diagram

The MC74HC238 is packaged in a 16-pin configuration. Pins 1, 2, and 3 are the address inputs A0, A1, and A2, respectively. Pin 4 is connected to ground (GND), and Pin 16 is connected to the power supply (Vcc). The active LOW outputs are found on pins 5 through 12 (Y0 to Y7). The output enable pin (OE) is located on pin 13, while the enable inputs (G) are on pins 14 and 15. This arrangement allows for easy integration into various digital circuits.

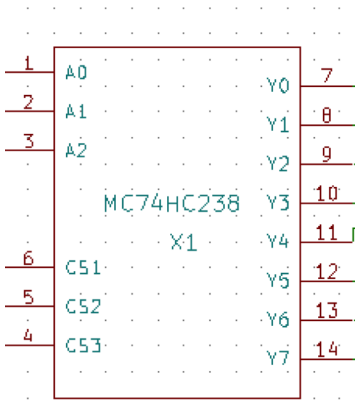


Figure 5.2.1.1: Pin Configuration of MC74HC238

5.2.2 Sub Circuit Layout

In the sub-circuit layout of the MC74HC238, the three address inputs (A0, A1, A2) are connected to a source that provides binary data, such as a binary counter or microcontroller. The IC decodes these inputs to select one of the eight outputs (Y0-Y7). Each output corresponds to a specific binary combination of the address inputs, and only the selected output is activated LOW while the others remain HIGH. This configuration is essential for tasks requiring multiple output selection or address decoding.

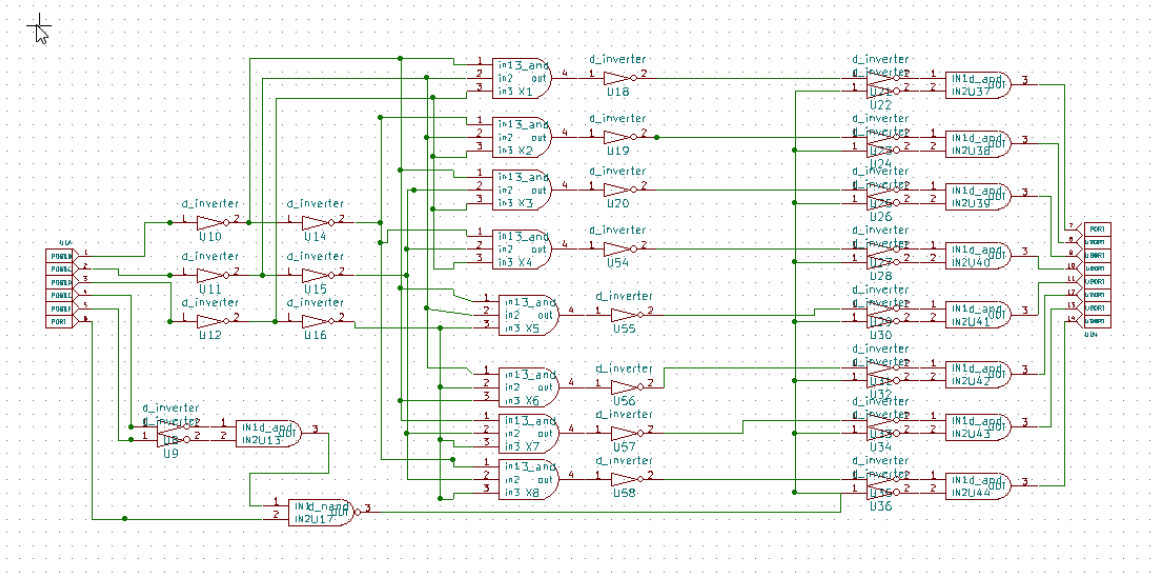


Figure 5.2.2.1: Subcircuit layout of the MC74HC238

5.2.3 Test Circuit

The test circuit for the MC74HC238 involves connecting a binary counter or similar device to the address inputs (A0-A2) to generate all possible 3-bit binary combinations. The outputs (Y0-Y7) are observed to ensure that the correct output line is activated LOW for each input combination. The output enable pin (OE) is typically held LOW during testing to enable the outputs. This setup verifies that the decoder is functioning correctly and that the outputs respond accurately to the address inputs.

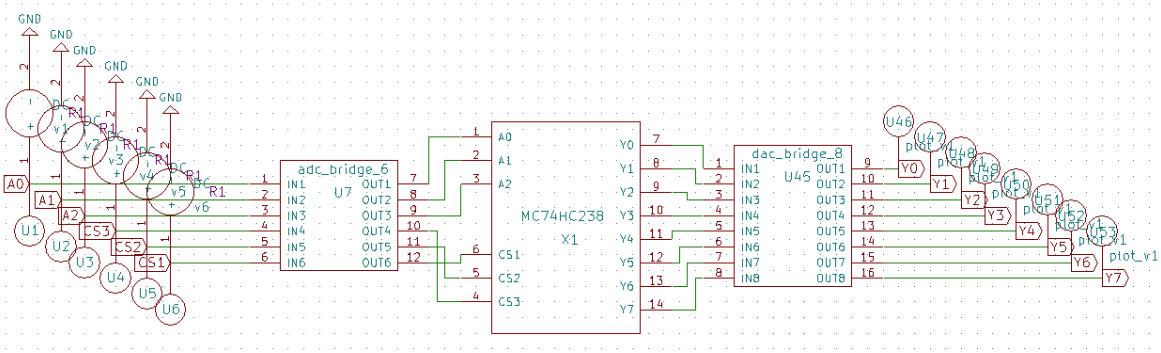


Figure 5.2.3.1: Test Circuit layout of the MC74HC238

5.2.4 Input Waveform

The input waveform for the MC74HC238 consists of three binary signals corresponding to the address inputs (A0, A1, A2). These signals change to represent all possible 3-bit binary values from 000 to 111. Each combination of these inputs selects a different output line. For instance, an input combination of 010 will select output Y2, making it LOW while all other outputs remain HIGH. The waveform is crucial for understanding how the IC processes and decodes the binary inputs.

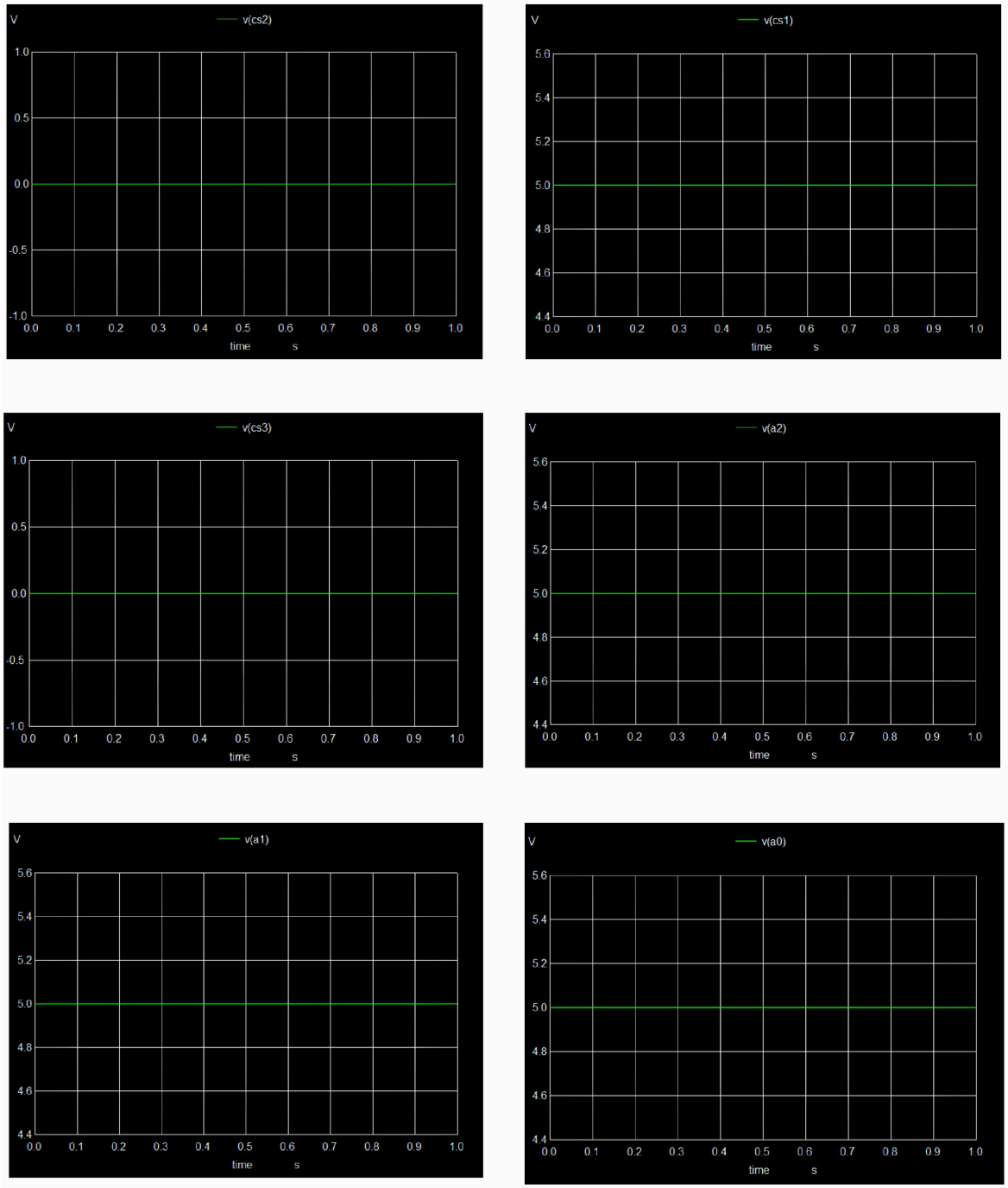


Figure 5.2.4.1: Input

5.2.5 Output Waveform

The output waveform of the MC74HC238 reflects the state of the active LOW outputs based on the binary input values. For each 3-bit input combination, one output (Y0-Y7) will go LOW while all other outputs stay HIGH. For example, if the input is 011 (binary for 3), output Y3 will be LOW, and the remaining outputs will be HIGH. This behavior demonstrates the decoder's functionality in activating the correct output line according to the address inputs.

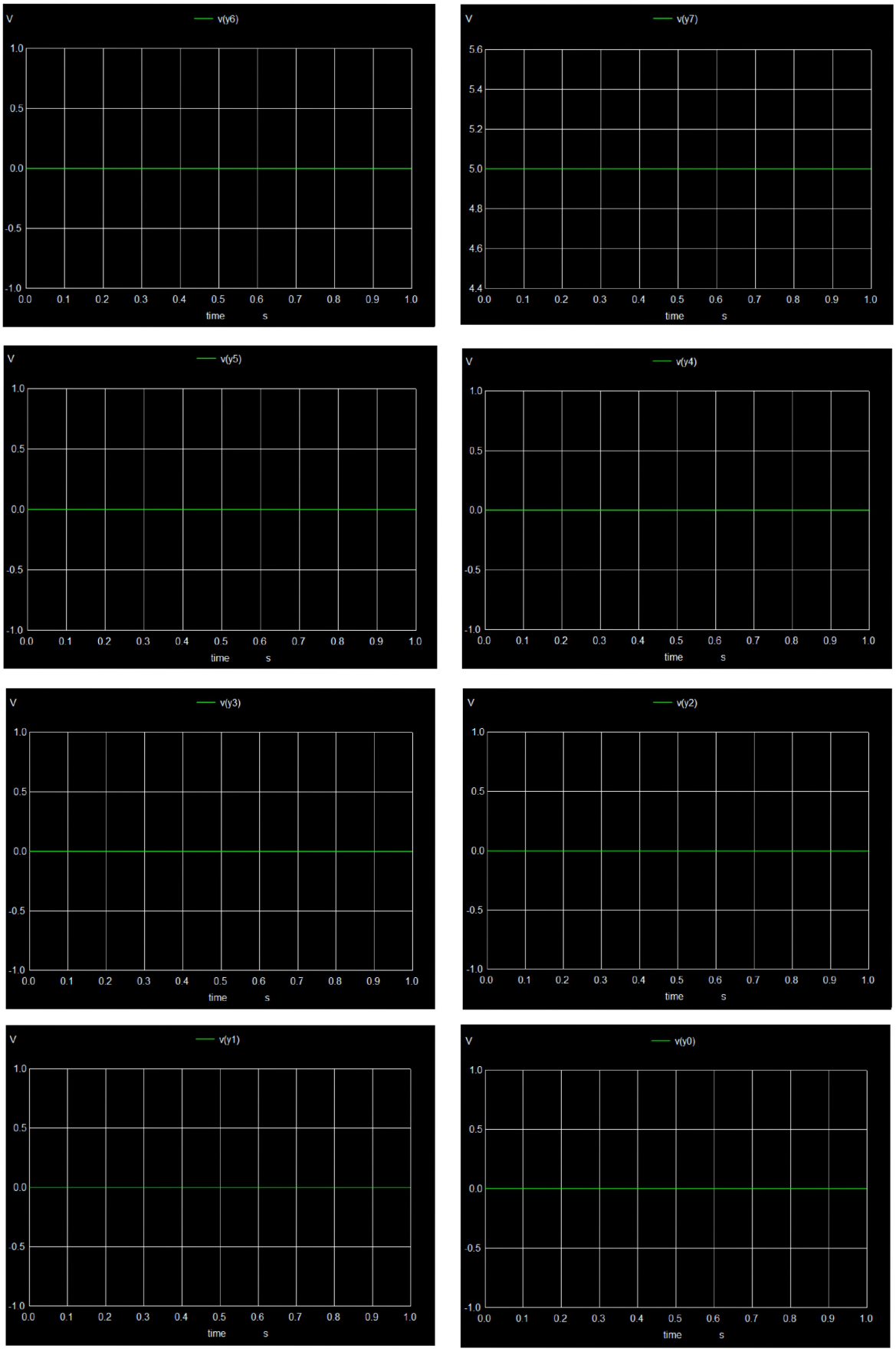


Figure 5.2.5.1: Output

5.3 74ACT11286

The 74ACT11286 is a high-performance 9-bit parity generator/checker IC used in digital communication systems for error detection. It supports both even and odd parity calculations. This IC is commonly used in systems where detecting transmission errors in data streams is essential for maintaining data integrity.

5.3.1 Pin Diagram

The 74ACT11286 comes in a 12-pin configuration. Pins 1 to 9 serve as the data inputs (A1-A9), which are used to check or generate parity.

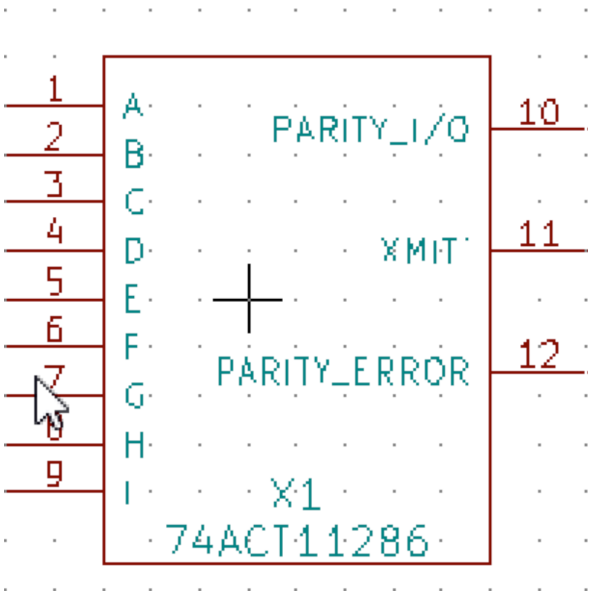


Figure 5.3.1.1: Pin Configuration of 74ACT11286

The image shows the subcircuit layout, illustrating how the internal logic of the IC processes the inputs (A1-A9) to generate even and odd parity outputs. Inside the IC, logic gates are arranged to count the number of '1's in the input data. Depending on whether the count is even or odd, the respective parity bit is generated.

5.3.2 Sub Circuit Layout

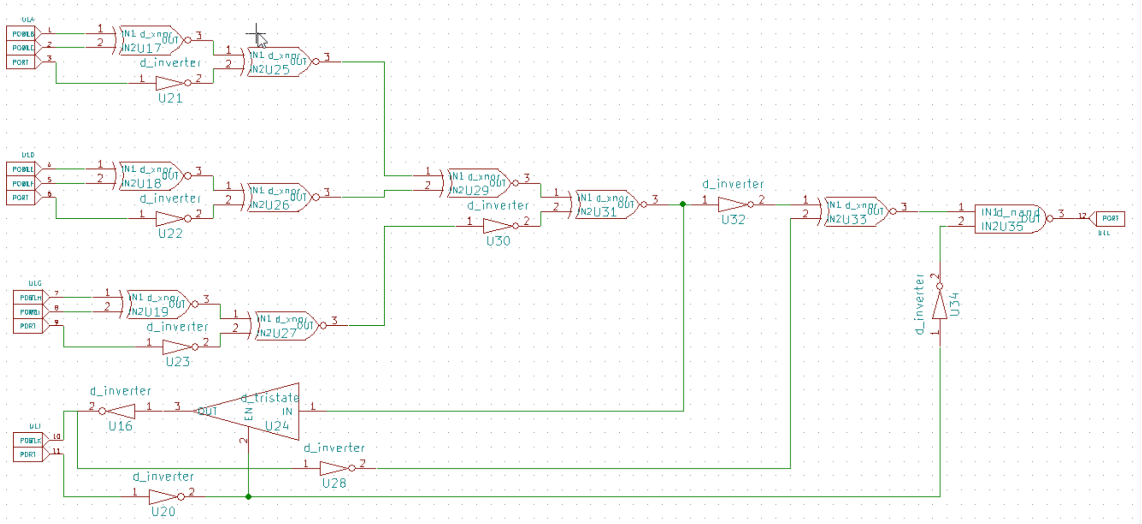


Figure 5.3.2.1: Subcircuit layout of the 74ACT11286

5.3.3 Test Circuit

To test the 74ACT11286, a binary counter is connected to the data input pins (A1-A9) to cycle through all possible input combinations. The even and odd parity outputs are observed using logic probes or an oscilloscope. This test circuit is helpful in verifying that the IC correctly computes parity for every input.

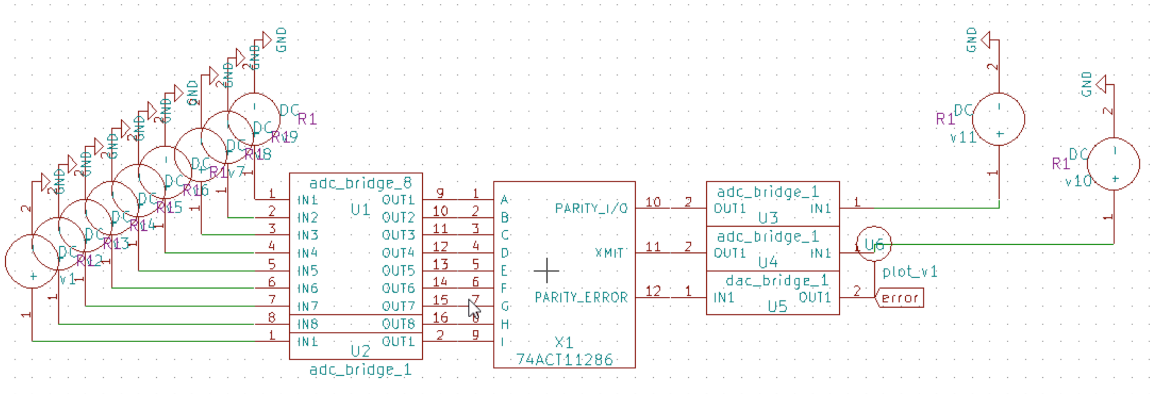


Figure 5.3.3.1: Test Circuit layout of 74ACT11286

5.3.4 Input Condition

The input waveform for testing the IC ranges from 000000000 to 111111111, covering all possible 9-bit binary combinations. This waveform can be generated using a binary counter or logic generator. These binary patterns are fed into the IC to evaluate its parity generation and error-checking functions across different inputs.

FUNCTION TABLE

NUMBER OF INPUTS (A–I) THAT ARE HIGH	$\overline{\text{XMIT}}$ INPUT	PARITY I/O	PARITY ERROR OUTPUT
0, 2, 4, 6, 8	l	H	H
1, 3, 5, 7, 9	l	L	H
0, 2, 4, 6, 8	h h	h l	H L
1, 3, 5, 7, 9	h h	h l	L H

h = high input level, H = high output level, l = low input level, L = low output level

Figure 5.3.4.1: Truth Table for different conditions

5.3.5 Output Waveform

Its observed when the input is given according to figure 5.3.4.1

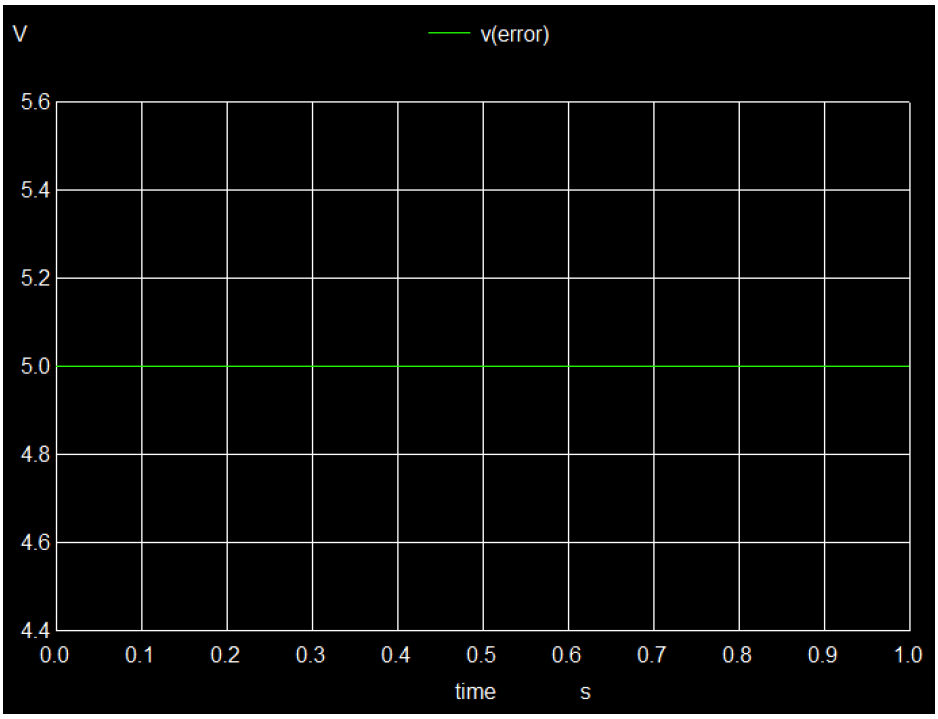


Figure 5.3.5.1: Output of 74ACT11286

5.4 74LVC1G97

The 74LVC1G97 is a configurable multi-function logic gate. It can be programmed to implement different logic functions, such as AND, OR, XOR, and more, based on the input connections. This IC is widely used in systems requiring versatile logic functions, with the ability to handle high-speed operations and low power consumption.

5.4.1 Pin Diagram

The 74LVC1G97 comes in a 4-pin configuration. Pin 1,Pin 2 & Pin 3 are the input (A),(B),(C) respectively. Depending on how the inputs are configured, the output will vary according to the logic function.

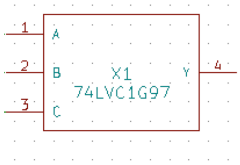


Figure 5.4.1.1: Pin Configuration of 74LVC1G97

5.4.2 Sub Circuit Layout

The image shows the subcircuit layout, where the internal logic gate configuration is highlighted. The IC has three inputs: A, B, and C input, which determines the logic function (AND, OR, XOR, etc.) that the IC will perform. Inside the IC, multiplexers and logic gates are used to route the inputs through the desired function. The output is available at Pin 4, and changes depending on the logic function selected by the configuration of the inputs. The IC provides flexibility by allowing different logic operations in one device.

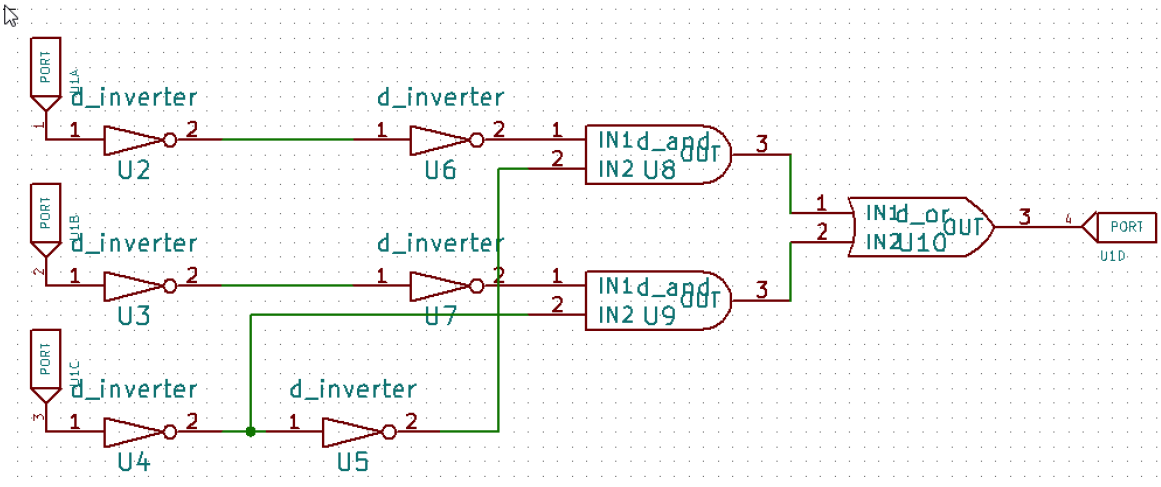


Figure 5.4.2.1: Subcircuit layout of the 74LVC1G97

5.4.3 Test Circuit

The test circuit involves connecting input signals to Pins A, B, and C. By applying different combinations of high (5V) and low (0V) voltages to the inputs, the behavior of the output (Y) can be tested. A logic probe or oscilloscope can be used to observe how the output changes depending on the logic function that is selected by the input conditions.

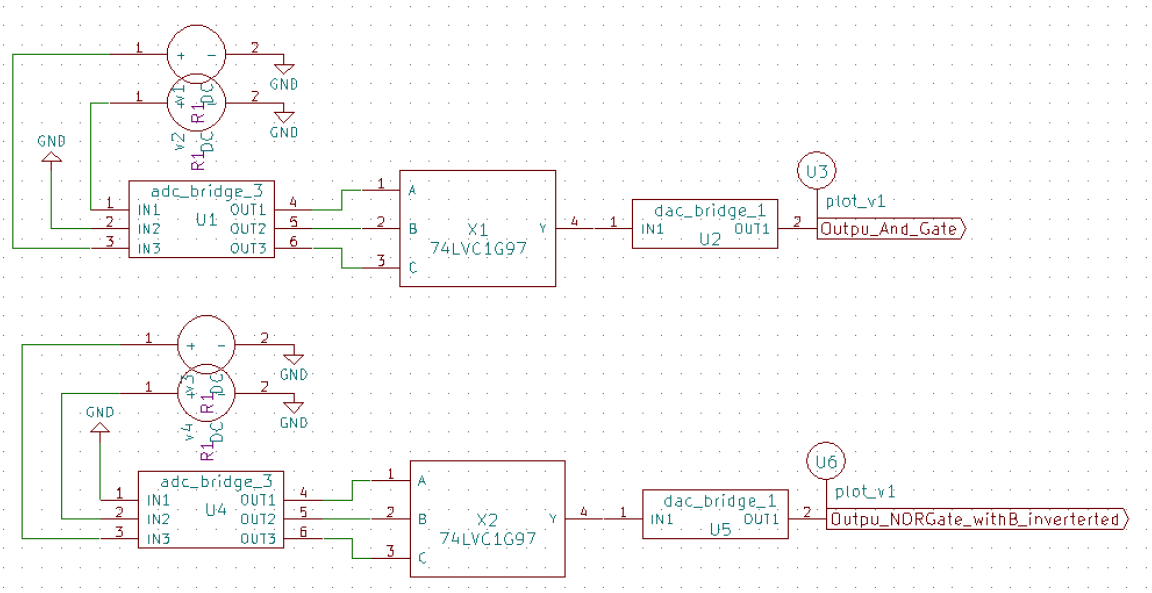


Figure 5.4.3.1: Test Circuit layout of the 74LVC1G97

5.4.4 Input Conditions

The input waveform consists of binary signals applied to the inputs (A, B, and C). A range of input conditions, including 0 (Low) and 1 (High), is applied to the inputs to test the IC's functionality. The input waveforms control which logic function the IC will perform, and the output changes accordingly.

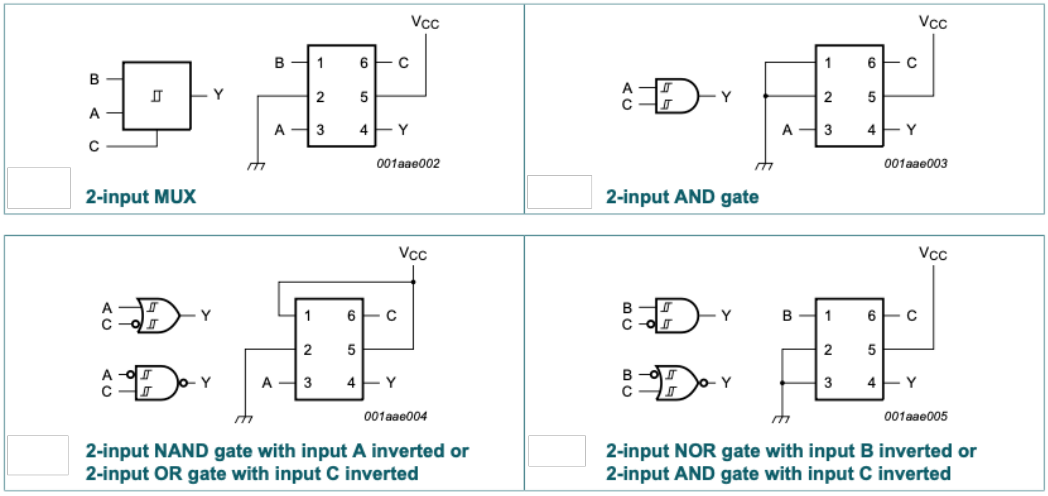


Figure 5.4.4.1: Input and output conditions

5.4.5 Output Waveform

The output waveform will show a high signal only when both A and B inputs are high; otherwise, the output will be low.

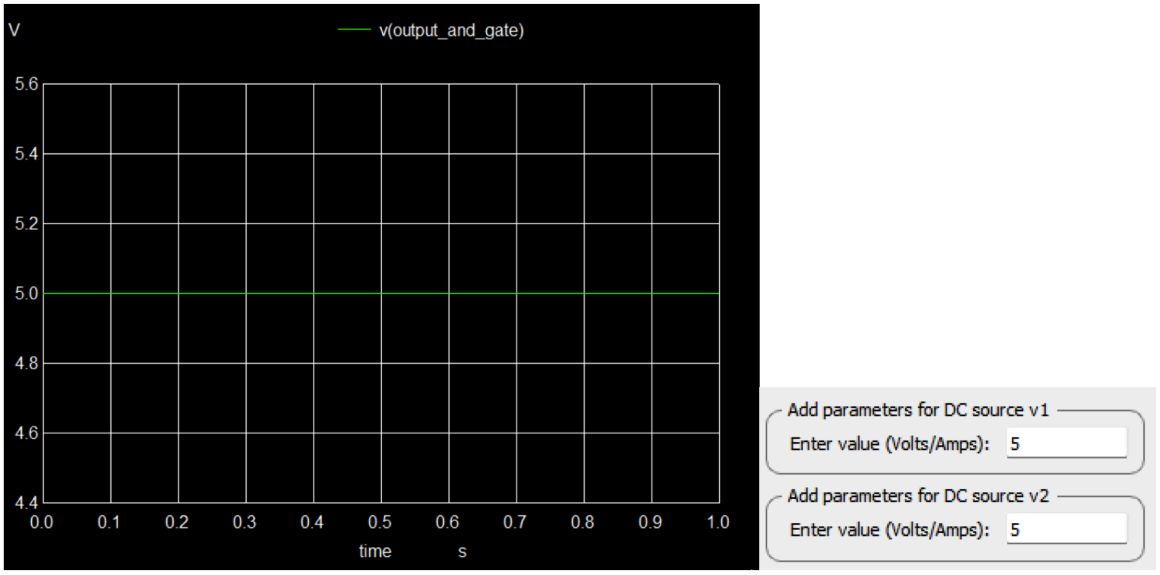


Figure 5.4.5.1: Output Waveform for 74LVC1G97

The output waveform will be low when A is High and B is low (after inversion). For other combinations, the output will be high.

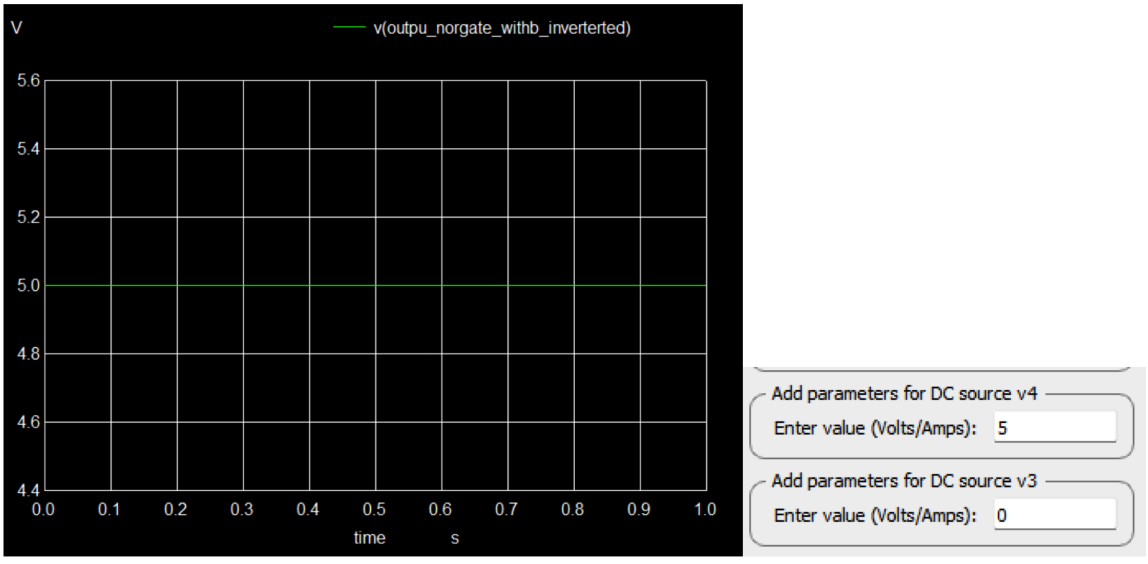


Figure 5.4.5.2: Output Waveform for 74LVC1G97

5.5 CD 4050

The CD4050 is a hex buffer IC that provides non-inverting buffer functionality. It can drive high-current loads and isolate signals.

5.5.1 Pin Diagram

The IC has 14 pins: Inputs (Pins 1, 3, 5, 9, 11, 13), Outputs (Pins 2, 4, 6, 10, 12, 14),

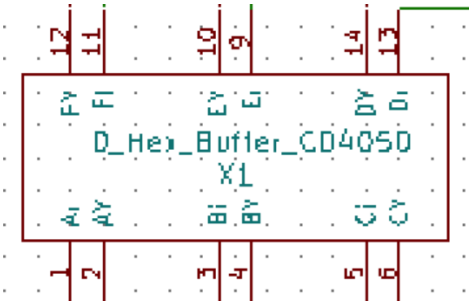


Figure 5.5.1.1: Pin Configuration of the CD4050

5.5.2 Sub Circuit Layout

The image shows the inner structure of the CD4050, detailing the internal arrangement of the buffer stages within the IC.

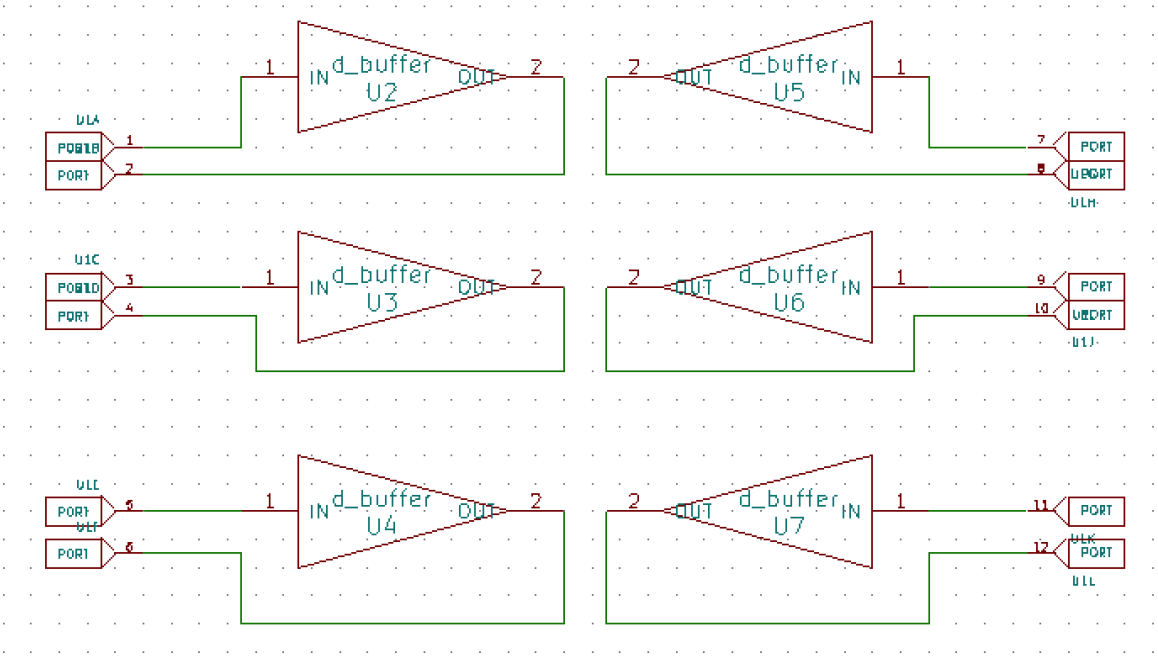


Figure 5.5.2.1: Subcircuit layout of the CD4050

5.5.3 Test Circuit

The test circuit involves connecting a binary signal generator to an input pin of the CD4050 and monitoring the corresponding output pin with a logic probe or oscilloscope. Apply high (5V) and low (0V) signals to the input and observe that the output directly mirrors the input signal without inversion, reflecting the same high or low state.

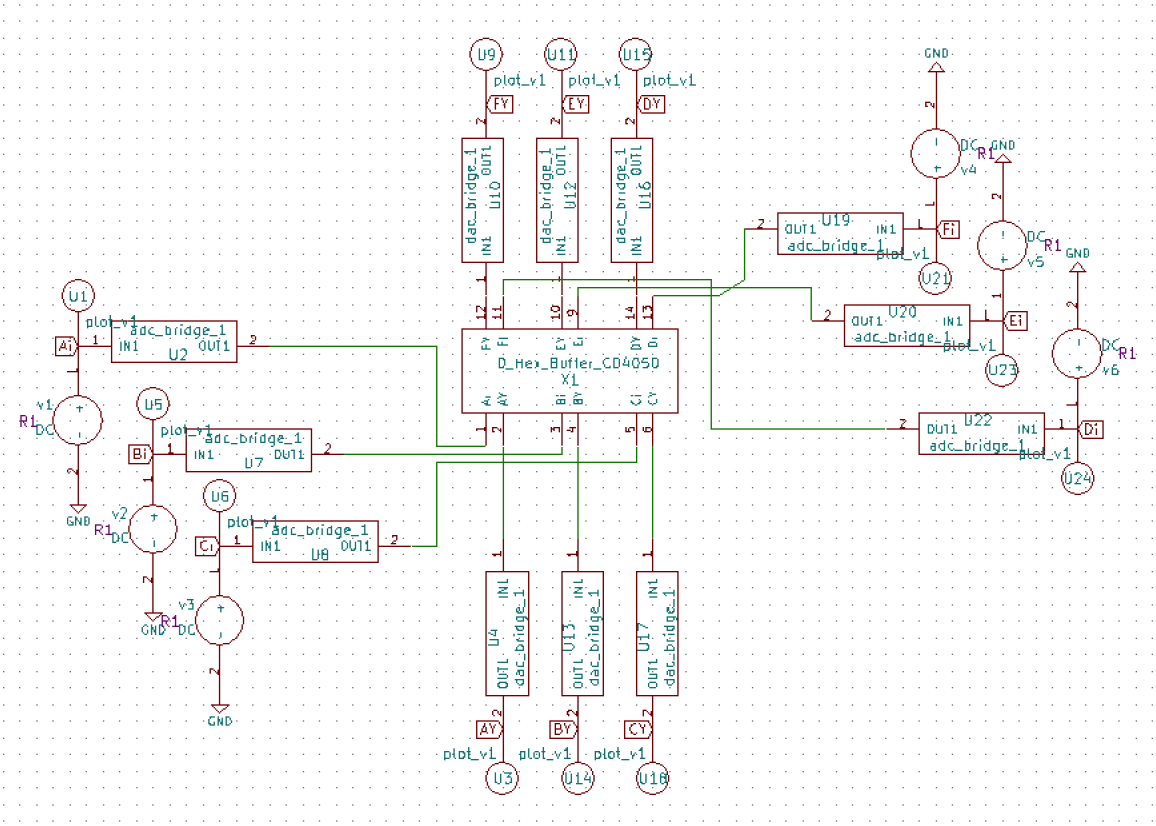


Figure 5.5.3.1: Test circuit layout of the CD4050

5.5.4 Input and Output waveforms of the CD4050

The images illustrate the input and output waveforms of the CD4050 test circuit. The input waveform shows the binary signal being applied to the buffer's input pin, while the output waveform demonstrates how the CD4050 mirrors this signal at the output pin. The output waveform mirrors the input exactly.

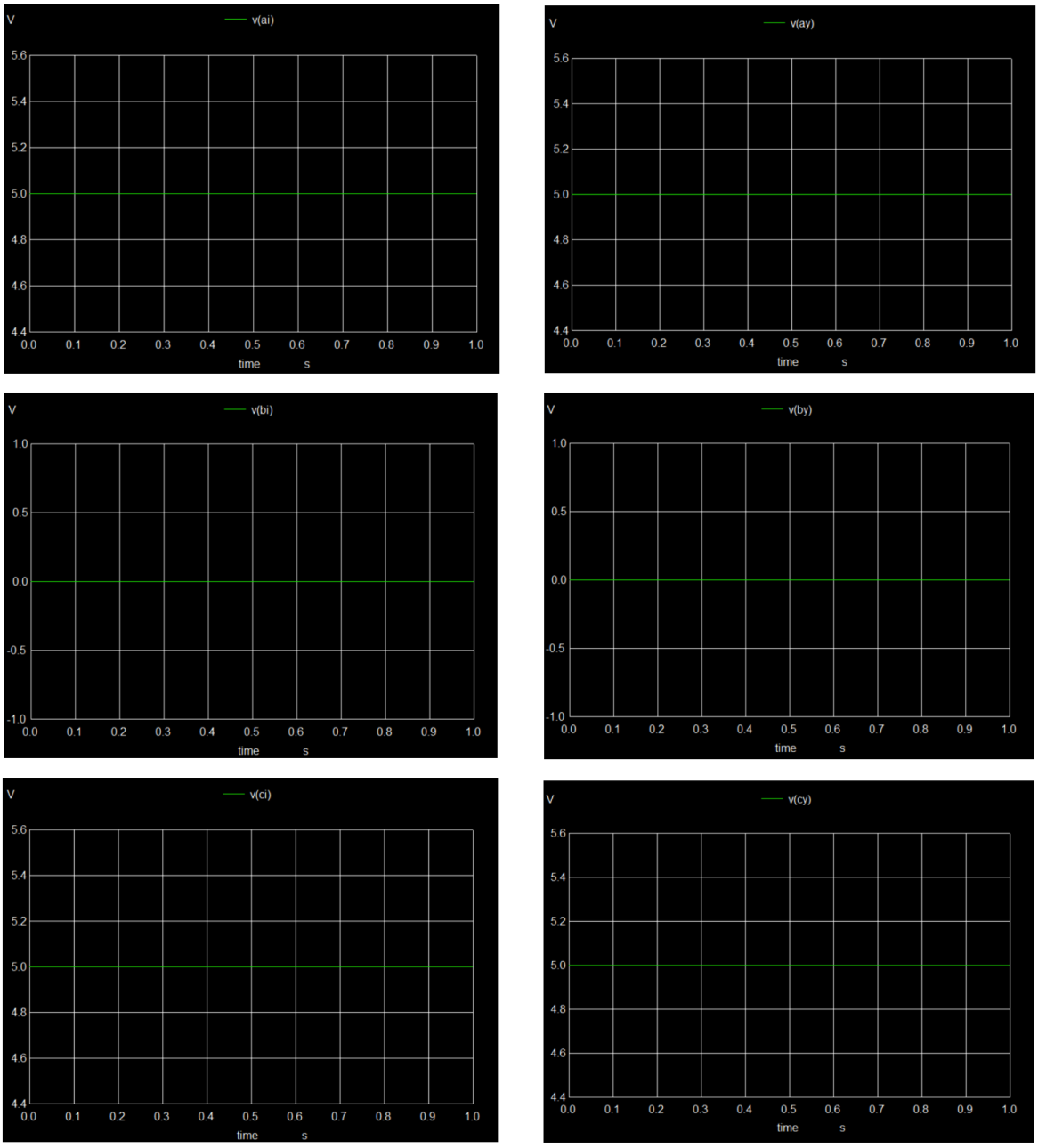


Figure 5.5.4.1: Input & Output Waveform

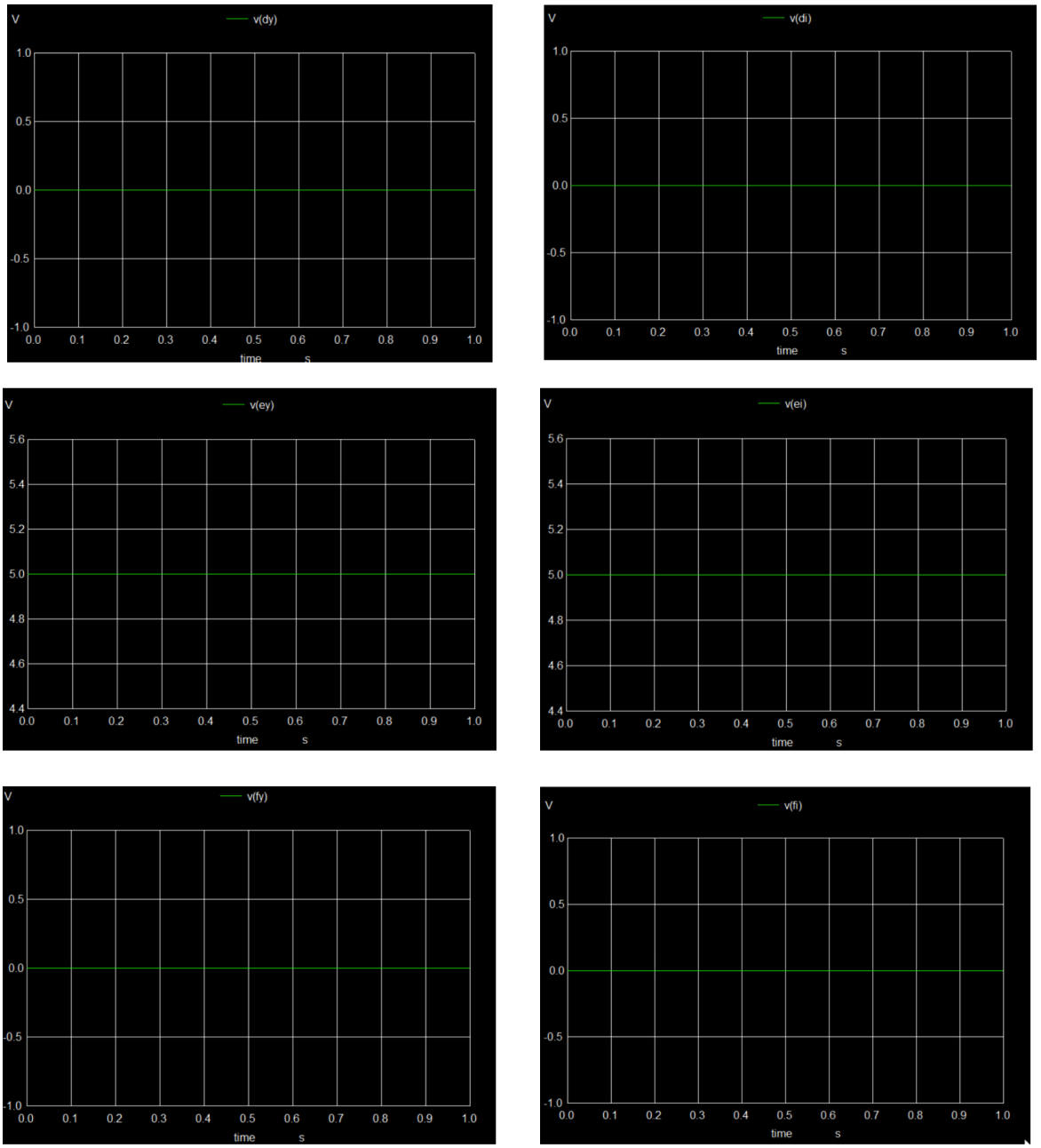


Figure 5.5.4.2: Input & Output Waveform

5.6 CY74FCT827ATQCT

The FCT827T 10-bit bus driver provides high-performancebus interface buffering for wide data/address paths or busescarrying parity. The 10-bit buffers have NAND-ed outputenables for maximum control flexibility

5.6.1 Pin Diagram

Displays the pin configuration of the CY74FCT827, showing the 10 input and 10 output connections, as well as the control pins for enable and disable operations. Understanding the pinout is critical for correct circuit integration.

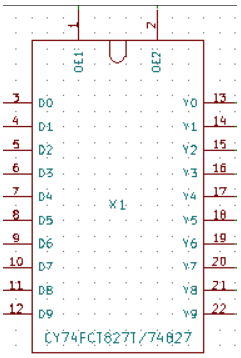


Figure 5.6.1.1: Pin Configuration of the CY74FCT827ATQCT

5.6.2 Sub Circuit Layout

Shows the internal layout of the CY74FCT827, focusing on its 10-bit bus driver functionality and how it uses tri-state buffering. The layout highlights how the internal logic controls the input-to-output data flow.

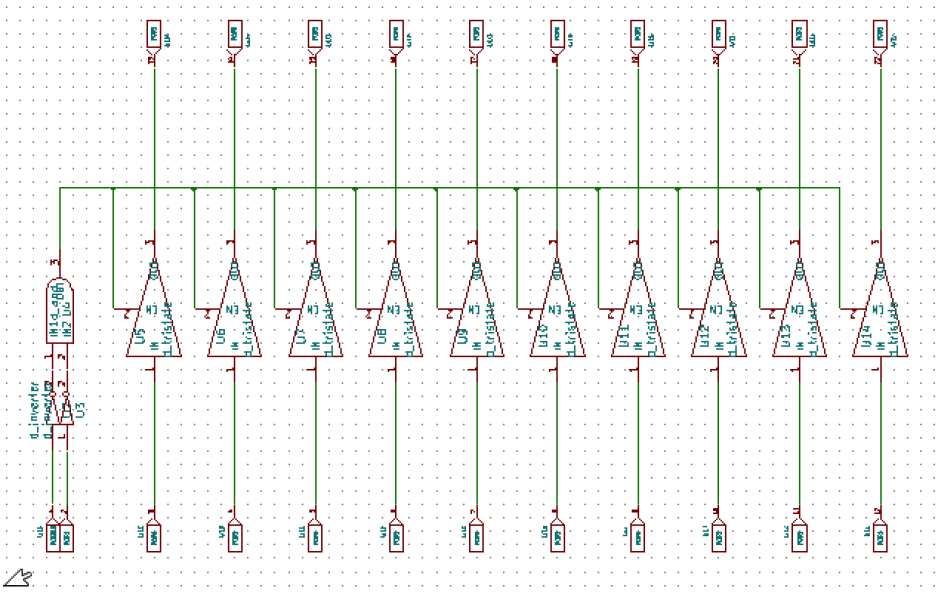


Figure 5.6.2.1: SUB circuit layout of the CY74FCT827ATQCT

5.6.3 Test Circuit

Provides a typical test circuit setup to validate the operation of the CY74FCT827, demonstrating how the inputs, outputs, and control signals should be connected to verify functionality in a practical scenario.

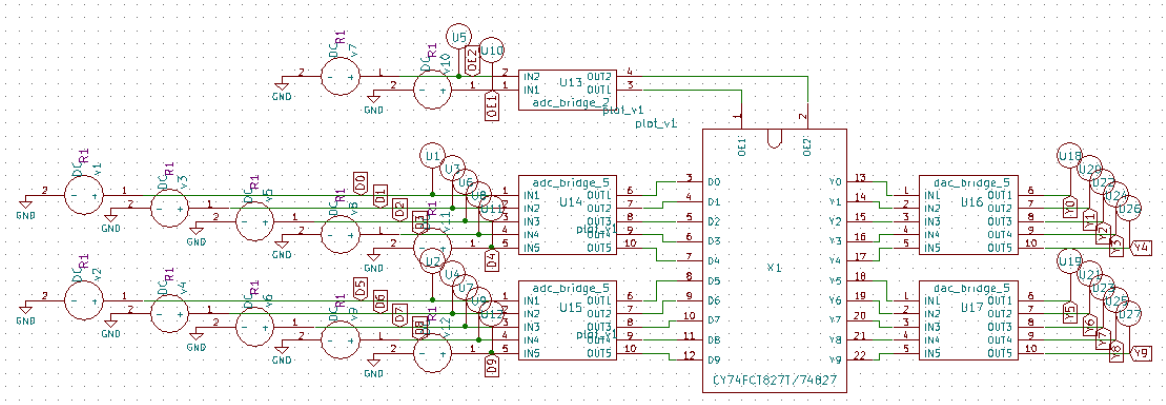


Figure 5.6.3.1: Test circuit layout of the CY74FCT827ATQCT

5.6.4 Input Waveform

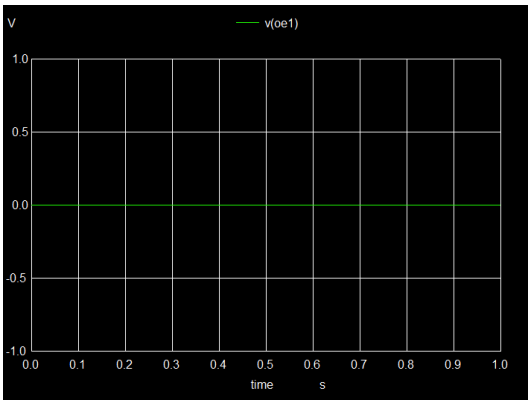
Displays the timing diagram for input signals, including the behavior of the input-enable controls, to demonstrate how the IC handles bus signals when enabled or disabled.

FUNCTION TABLE

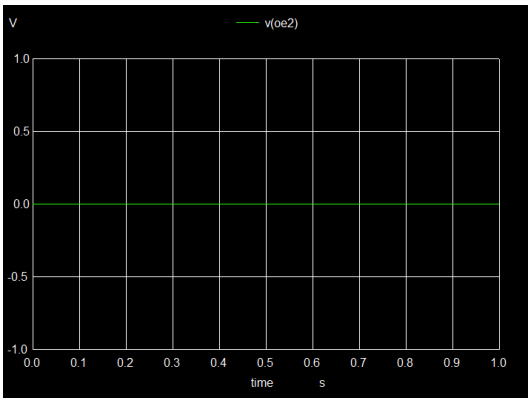
INPUTS			OUTPUT	FUNCTION
$\overline{OE}_1$	$\overline{OE}_2$	D	Y	
L	L	L	L	Transparent
L	L	H	H	
H	X	X	Z	3-state
X	H	X	Z	

H = High logic level, L = Low logic level, X = Don't care,
Z = High-impedance state

Figure 5.6.4.1: Input & Output Condition of the CY74FCT827ATQCT



(a) OE1



(b) OE2

Figure 5.6.4.2: Input OE1 & OE2

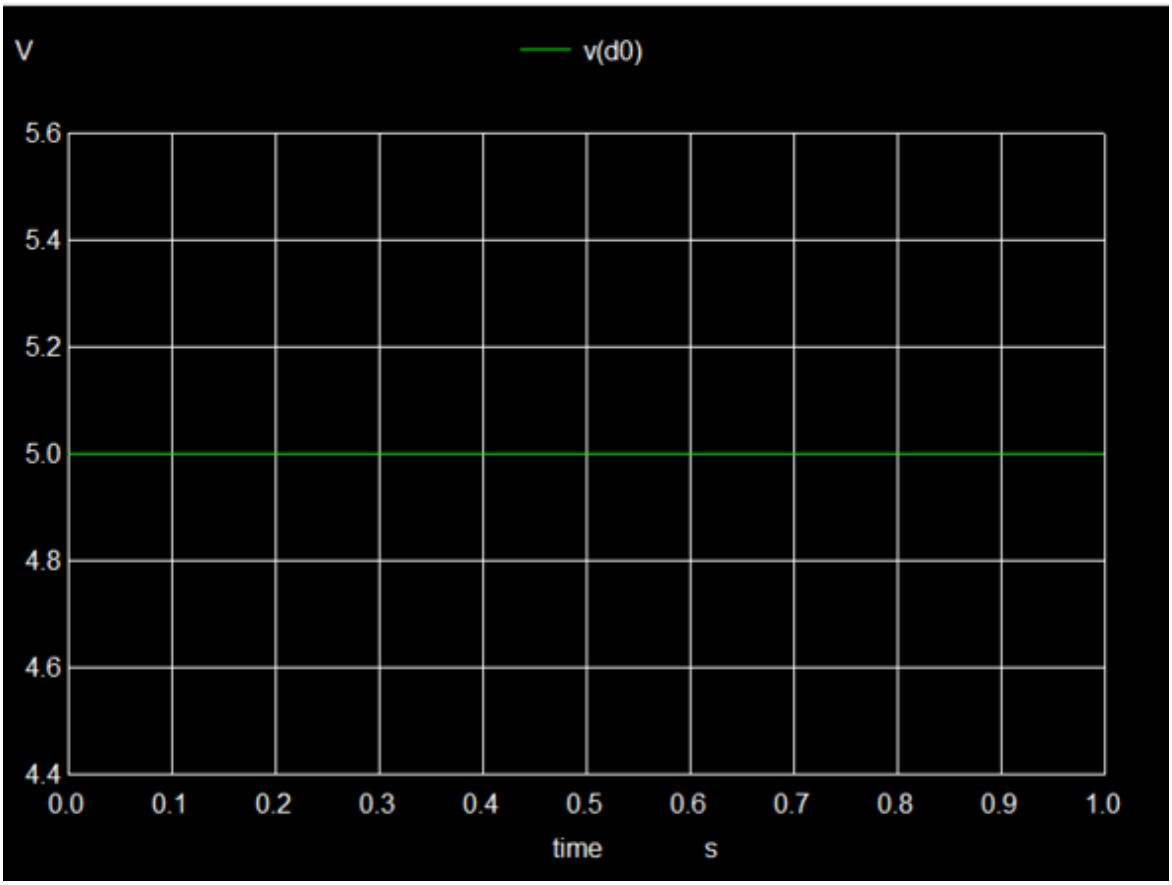


Figure 5.6.4.3: Input

5.6.5 Output Waveform

Shows the corresponding output signal behavior based on input and enable conditions, illustrating how the bus driver maintains signal integrity and responds to control signals.

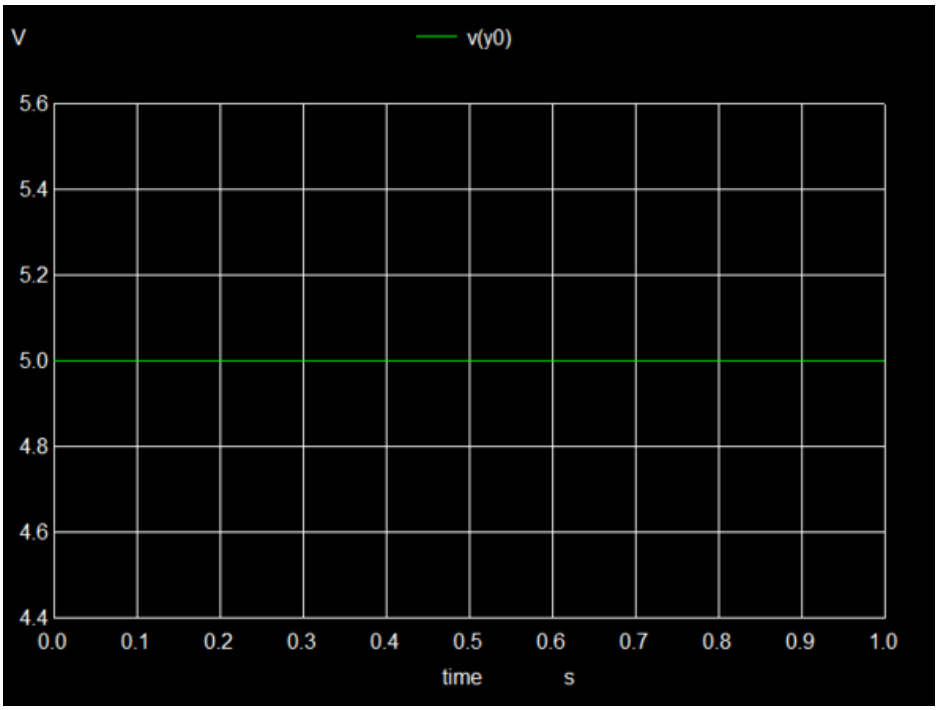


Figure 5.6.5.1: Output

5.7 SN74LS138

The SN74LS138 is a 3-to-8 line decoder/demultiplexer IC from Texas Instruments, commonly used in digital systems for decoding binary inputs into one of eight outputs. It features active-low outputs, meaning the selected output goes low (0) when the corresponding input is decoded, while all others remain high.

5.7.1 Pin Diagram

Describes the pin configuration of the SN74LS138 IC, showing the connections for the inputs, outputs, and control signals. This is essential for understanding how to interface with the IC.

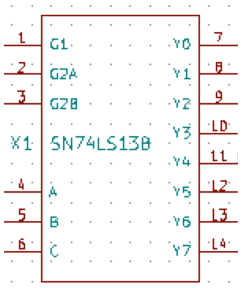


Figure 5.7.1.1: Pin Configuration of SN74LS138

5.7.2 Sub Circuit Layout

Represents the internal structure and functional blocks of the SN74LS138 IC, detailing how it decodes inputs and manages outputs. This layout helps in understanding the IC's internal workings.

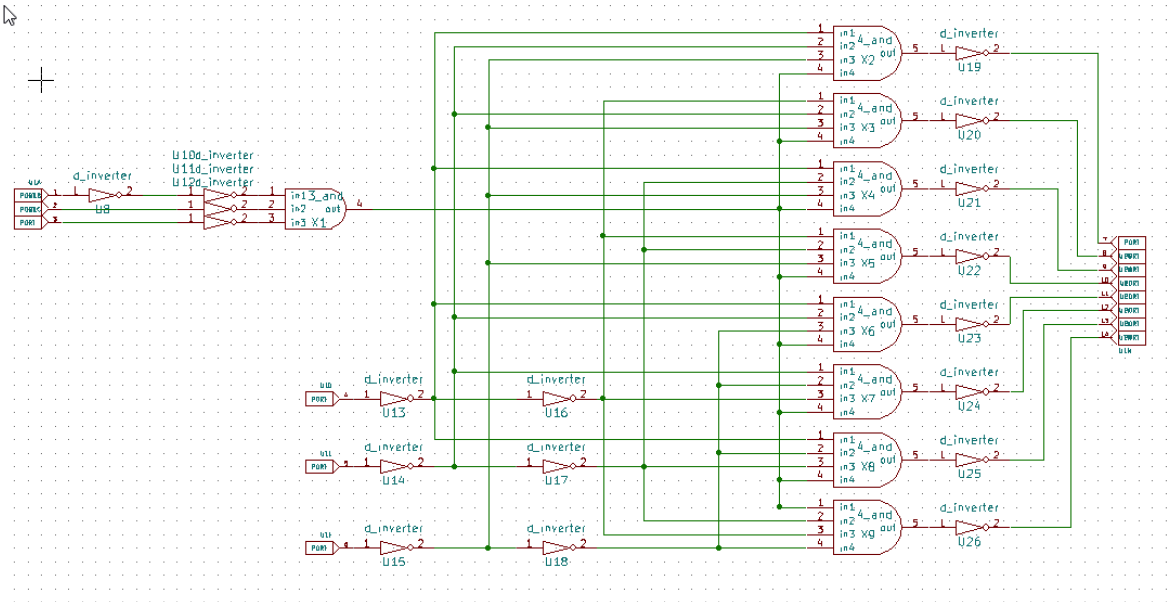


Figure 5.7.2.1: SUB circuit layout of the SN74LS138

5.7.3 Test Circuit

A schematic showing how the SN74LS138 can be tested in a practical circuit. This test circuit includes the connections for inputs, outputs, power, and control signals.

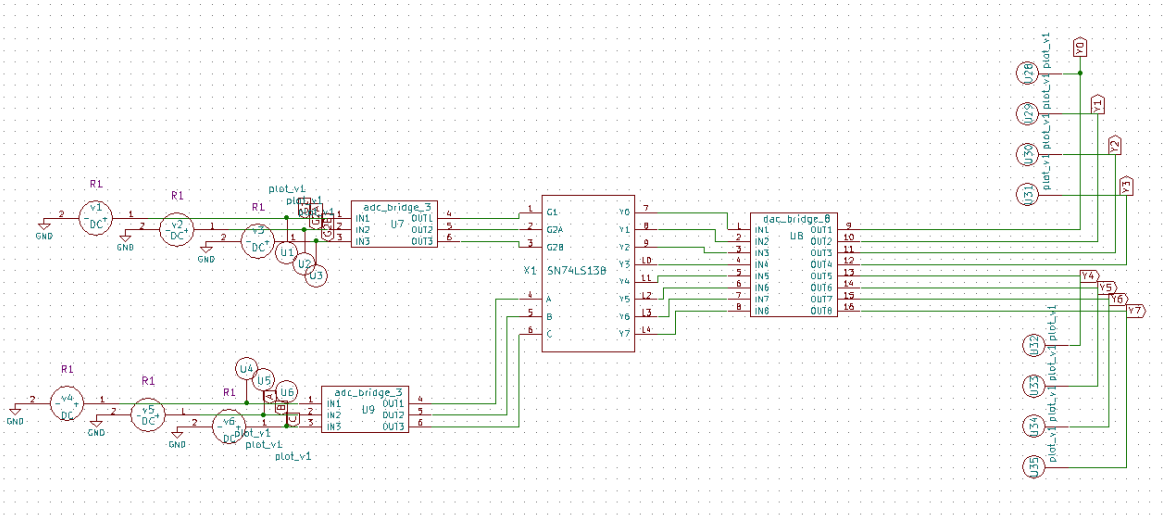


Figure 5.7.3.1: Test circuit layout of the SN74LS138

5.7.4 Input Waveform

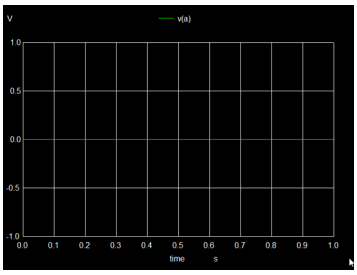
Illustrates the timing diagram of the input signals provided to the SN74LS138 IC. This helps in analyzing how different input combinations affect the outputs over time.

INPUTS					OUTPUTS							
ENABLE		SELECT										
G1	$\bar{G}2$*	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	H	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	H	H	H	H	H	L	H	H	H	H
H	L	H	L	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	H	L	H	H
H	L	H	H	L	H	H	H	H	H	H	L	H
H	L	H	H	H	H	H	H	H	H	H	H	L

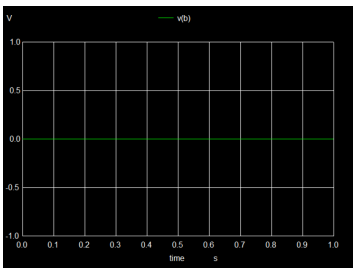
*$\bar{G}2 = \bar{G}2A + \bar{G}2B$

H = high level, L = low level, X = irrelevant

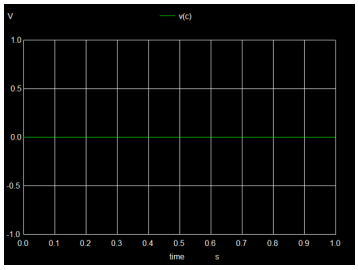
Figure 5.7.4.1: Input & Output Conditions



(a) V_A



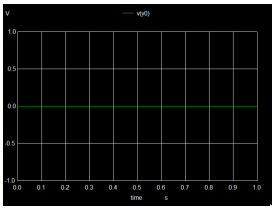
(b) V_B



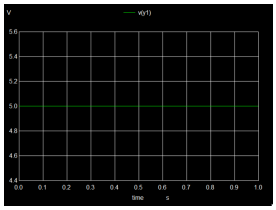
(c) V_C

Figure 5.7.4.2: SELECT INPUT

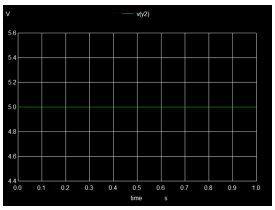
5.7.5 Output Waveform



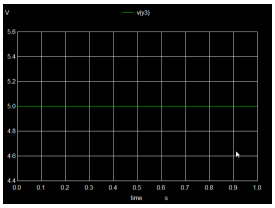
(a) Y0



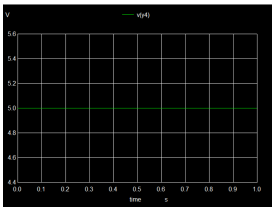
(b) Y1



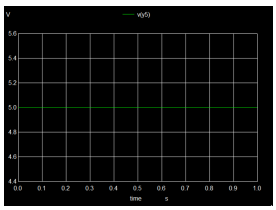
(c) Y2



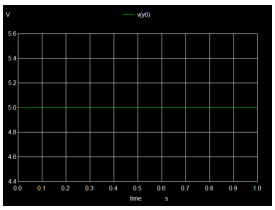
(d) Y3



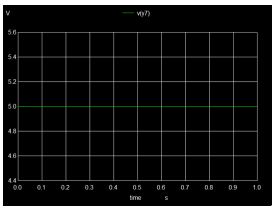
(e) Y4



(f) Y5



(g) Y6



(h) Y7

Figure 5.7.5.1: Output waveforms of the SN74LS138 circuit

Chapter 6

Conclusion and Future Scope

Developed a range of subcircuits for both Analog and Digital Integrated Circuits (ICs), strictly following the specifications from their official datasheets. These include essential components like Op-Amps, Voltage Regulators, and Comparators, as well as other foundational digital and analog ICs. Each IC model was thoroughly tested using appropriate test circuits to ensure accurate performance. These IC models are now ready for integration into eSim's subcircuit library, providing a comprehensive set of building blocks for developers and students to use in a wide array of circuit designs and simulations. With continued development, more such IC models are expected to enhance the library's offerings.

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