Summer Fellowship Report

On

Integrated Circuit Design using Subcircuit feature of eSim

Submitted by

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Under the guidance of

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Acknowledgment

I take this occasion to offer our heartfelt gratitude to the FOSSEE, IIT Bombay Team for offering me this wonderful opportunity to work on the design and integration of multiple sub-circuits in eSim. Working on eSim has prov ided myself with invaluable insights into various open-source EDA tools for circuit simulation and their applications in the practical world.

I extend our sincere regards to Prof. Kannan M. Moudgalya for his valuable guidance and motivation to throughout this fellowship program.

I would like to express our heartfelt appreciation to the entire FOSSEE team including our mentors Mr. Sumanto Kar, Mrs. Vineeta Gharvi, and Mrs. Usha Vishwanathan for constantly guiding and mentoring me throughout the duration of our internship.

It is with their support that I have been able to fulfill my project demands successfully. Whenever faced with an issue, my mentors were always accessible to help me assess and debug them. The learnings from them have been invaluable and shall be of paramount importance to me in the future.

Overall, it was a delightful experience interning at FOSSEE and contributing to its growth and I take away some great insights and knowledge from it. As enthusiastic beginners in the semiconductor industry, this internship is a milestone for me in my pursuit of a successful career.

Contents

Chapter 1

Introduction

FOSSEE which stands for Free/Libre and Open Source Software for Education is an organization, based at IIT Bombay, as a remarkable initiative aimed at promoting the use of open-source software in education and research. It was established with the mission to reduce the dependency on proprietary software and to encourage the adoption of open-source alternatives. FOSSEE offers a wide range of tools and resources that cater to various academic and professional needs.

It provides comprehensive documentation, tutorials, workshops, and hands-on training sessions, for empowering students, educators, and professionals to leverage open-source software for their projects and coursework. The organization's commitment to fostering a collaborative and inclusive environment has significantly contributed to the democratization of technology and has opened up new avenues for innovation and learning.

1.1 eSim

eSim, created by the FOSSEE project at IIT Bombay, is a versatile open-source software tool for circuit design and simulation. It combines various open-source software packages into one cohesive platform, making it easier to design, simulate, and analyze electronic circuits. This tool is particularly useful for students, educators, and professionals who need an affordable and accessible alternative to proprietary software.

eSim offers features for schematic creation, circuit simulation, PCB design, and includes an extensive library of components. The Subcircuit feature is a significant enhancement, enabling users to design complex circuits by integrating simpler subcircuits. Through eSim, FOSSEE promotes the use of open-source solutions in engineering education and professional fields, encouraging innovation and collaboration.

1.2 NgSpice

NgSpice is the open-source spice simulator for electric and electronic circuits. Such a circuit may comprise JFETs, bipolar and MOS transistors, passive elements like R, L, or C, diodes, transmission lines and other devices, all interconnected in a netlist.

Digital circuits are simulated as well, event-driven and fast, from single gates to complex circuits and the combination of both analog and digital as well as a mixed-signal circuits. NgSpice offers a wealth of device models for active, passive, analog, and digital elements. Model parameters are provided by our collections, by the semiconductor device manufacturers, or from semiconductor foundries. The user adds her circuits as a netlist, and the output is one or more graphs of currents, voltages and other electrical quantities or is saved in a data file.

1.3 Makerchip

Makerchip is a platform that offers convenient and accessible access to various tools for digital circuit design. It provides both browser-based and desktop-based environments for coding, compiling, simulating, and debugging Verilog designs. Makerchip supports a combination of open-source tools and proprietary ones, ensuring a comprehensive range of capabilities.

One can simulate Verilog/SystemVerilog/Transaction-Level Verilog code in Makerchip. eSim is interfaced with Makerchip using a Python based application called Makerchip-App which launches the Makerchip IDE. Makerchip aims to make circuit design easy and enjoyable for users of all skill levels. The platform provides a user-friendly interface, intuitive workflows, and a range of helpful features that simplify the design process and enhance the overall user experience.

The main drawback of these open source tools is that they are not comprehensive. Some of them are capable of PCB design (e.g. KiCad) while some of them are capable of performing simulations (e.g. gEDA). To the best of our knowledge, there is no open source software that can perform circuit design, simulation and layout design together. eSim is capable of doing all of the above.

Chapter 2

Feautures Of eSim

The objective behind the development of eSim is to provide an open source EDA solution for electronics and electrical engineers. The software should be capable of performing schematic creation, PCB design and circuit simulation (analog, digital and mixed-signal). It should provide facilities to create new models and components. Thus, eSim offers the following features -

1. Schematic Creation: eSim provides an easy-to-use graphical interface for drawing circuit schematics, making it accessible for users of all levels. Users can drag and drop components from the library onto the schematic, simplifying the design process. Comprehensive editing tools allow for easy modification of schematics, including moving, rotating, and labeling components.

2. Circuit Simulation: eSim supports SPICE (Simulation Program with Integrated Circuit Emphasis), a standard for simulating analog and digital circuits. Users can perform various types of analysis such as transient, AC, and DC, providing insights into circuit behavior over time and frequency.An integrated waveform viewer helps visualize simulation results, aiding in the analysis and debugging of circuit designs.

3. PCB Design: The PCB layout editor allows users to place components and route traces with precision. eSim includes DRC capabilities to ensure that the PCB design adheres to manufacturing constraints and electrical rules. Users can generate Gerber files, which are standard for PCB fabrication, directly from their designs.

4. Subcircuit Feature: This feature enables users to create complex circuits by integrating smaller, simpler subcircuits, promoting modular and hierarchical design approaches. Subcircuits can be reused in different projects, saving time and effort in redesigning common circuit elements.

5. Open Source Integration: eSim integrates several open-source tools like KiCad, Ngspice, and GHDL, providing a comprehensive suite for electronic design automation. Being open-source, eSim is free to use, making advanced circuit design tools accessible without the need for expensive licenses.

Chapter 3

Problem Statement

To design and develop various Analog and Digital Integrated Circuit Models in the form of sub-circuits using device model files already present in the eSim library. These IC models should be useful in the future for circuit designing purposes by developers and users, once they get successfully integrated into the eSim subcircuit Library.

3.1 Approach

The approach to implementing the problem statement began with examining datasheets from prominent Integrated Circuit (IC) manufacturers such as Texas Instruments, Analog Devices, and NXP Semiconductors. we selected ICs that offer a diverse range of functionalities, including precision amplifiers, comparators, encoders, and audio amplifiers. After building the subcircuits, we tested them to verify basic circuit configurations using NgSpice simulations. The step-by-step roadmap of this process is outlined below :

1. Analyzing Datasheets : The primary step is to browse through various analog and digital IC datasheets, and hence find suitable circuits to implement in eSim, that are not previously included into the eSim library. Check for the detailed schematic of the IC's and once the component values and the truth table is ascertained, then finalise the IC to be created.

2. Subcircuit Creation : After deciding the IC, we start modeling it as a subcircuit in eSim, using the model files present in the eSim device model library only. The design is strictly according to the information given in the official data-sheets of the ICs.This step also includes building the Symbol/Pin diagram of the IC according to the packaging and pin description given in the data-sheets only.

3. Test Circuit Design : Once the component of the IC is ready, now we can build the test circuits, according to the data-sheets. In this step we build the test cases and test circuits using the component IC.

4. Schematic Testing : Once the test circuits are ready, now it's time to simulate the test circuits so that the output can be obtained in the form of wave-forms and

plots. Here we take help of KiCad to NgSpice conversion and Simulation feature in eSim

If the output of the test circuit is not as per expectation, this implies that the test case has failed, and there is some error in the schematic. In such cases we go back to the design phase of the IC or the test circuits, to look for possible errors and then repeat the testing process again after making required changes.

Once the expected output of the test cases are correct and satisfy the expected results, then in such a case the IC is declared successfully working. The test case has been verified and the designing process is complete.

Chapter 4

Analog IC's

4.1 CA3240 - Dual Operational Amplifier

The CA3240 IC, made by Renesas, is a versatile dual operational amplifier that combines the best of bipolar and MOS transistor technologies. It's known for its high-speed performance, with a bandwidth of 4.5 MHz and a rapid slew rate of 9 V/µs, which is great for applications that need quick signal processing. The MOSFET inputs mean it has high input impedance and very low input bias currents, making it ideal for precision work.

It can handle a wide range of voltages, working well with both single-supply and dual-supply configurations, and it operates quietly, making it perfect for audio and precise instrumentation projects. The CA3240 is also reliable in different environmental conditions, making it a solid choice for a variety of commercial and industrial uses.

4.1.1 IC Layout

This figure represents the 8-Pin Package Diagram of the CA3240- Dual Op-Amp IC

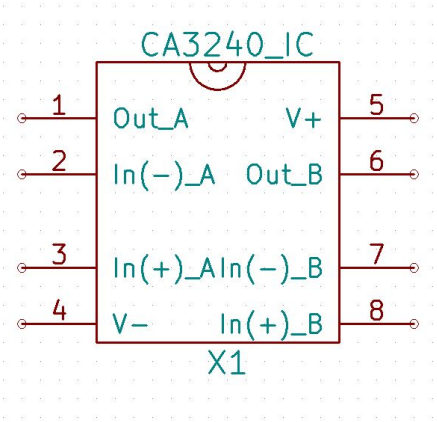


Figure 4.1: CA3240 - Dual Op Amp IC

4.1.2 Subcircuit Schematic Diagram

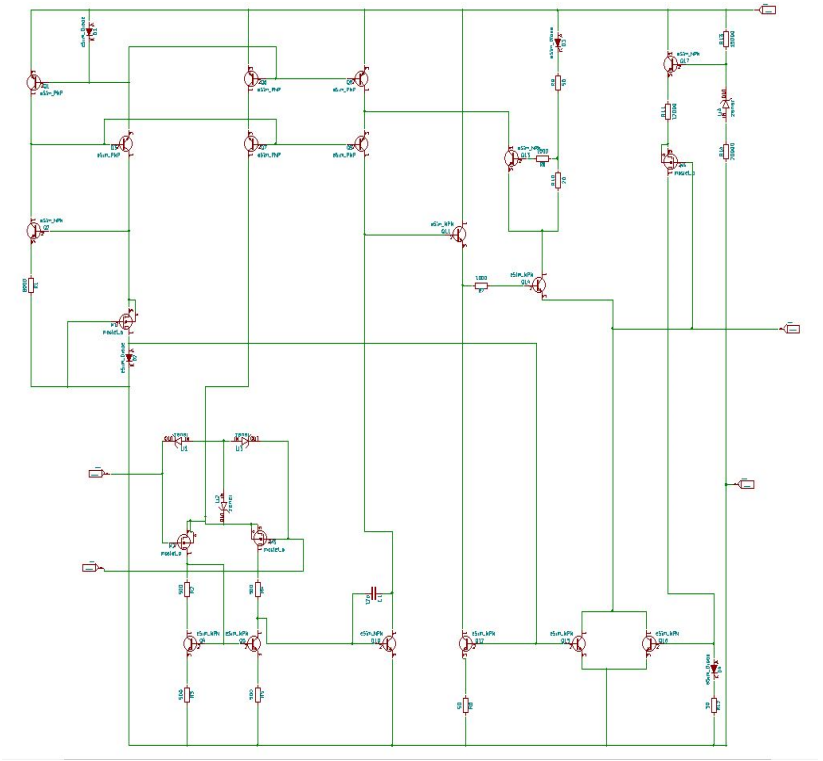


Figure 4.2: Subcircuit Schematic of CA3240

4.1.3 Test Circuit

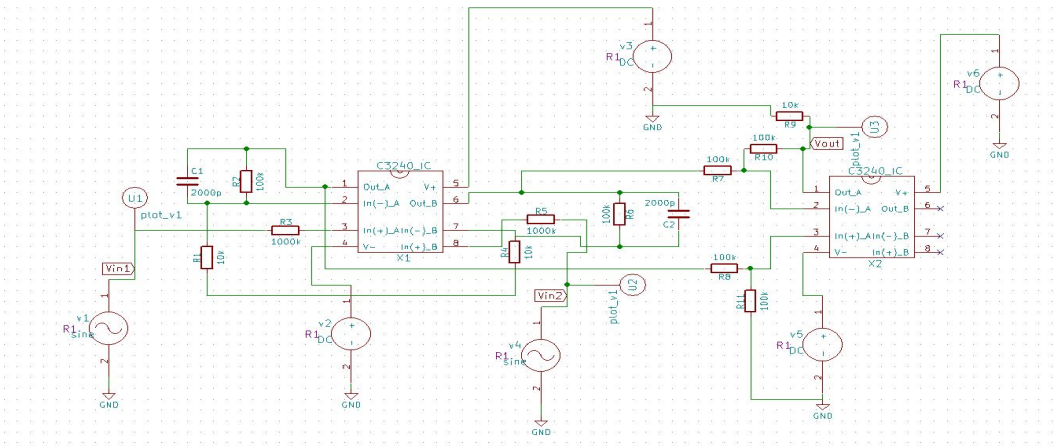


Figure 4.3: Differential Amplifier Test Circuit of CA3240

4.1.4 Input Plots

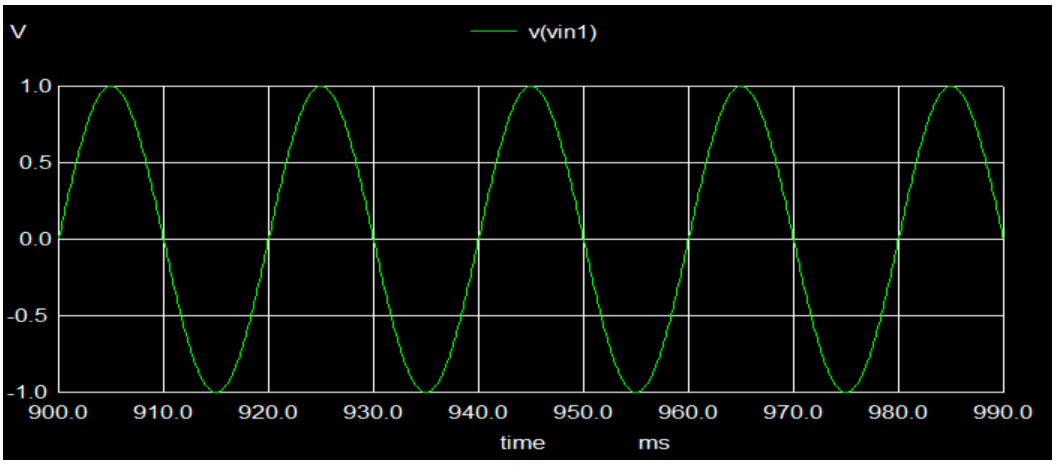


Figure 4.4: Vin1 = 1.1V

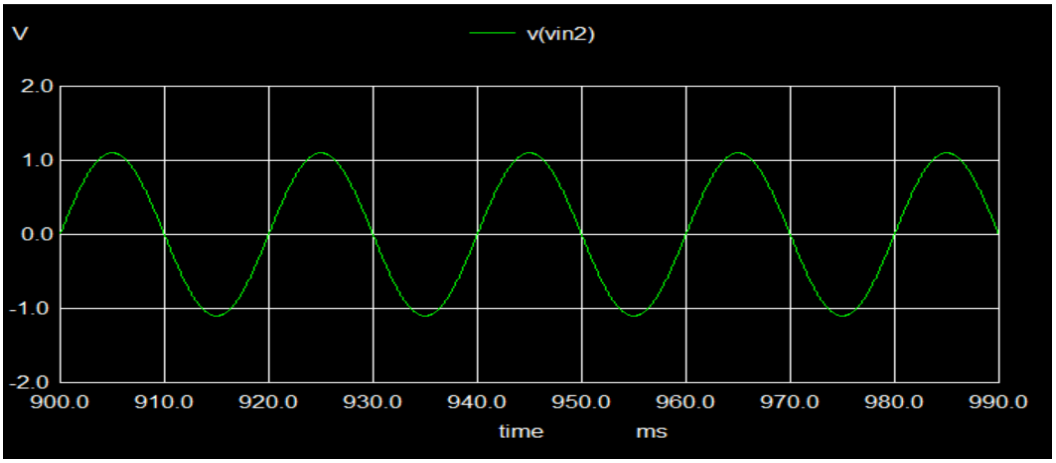


Figure 4.5: Vin2 = 1.0V

4.1.5 Output Plots

We know that the output voltage of an Op-Amp, Vout=Ad(Vin1-Vin2) Where,

Vin1 = The voltage applied at the inverting terminal of op-amp

Vin2= The voltage applied at the non-inverting terminal of op-amp

Ad= Differential Gain of the Op-Amp

Vout= The output voltage of the op-amp.

Hence, We can calculate the Differential Gain via the waveforms as -

Ad = Vout /(Vin1 - Vin2)

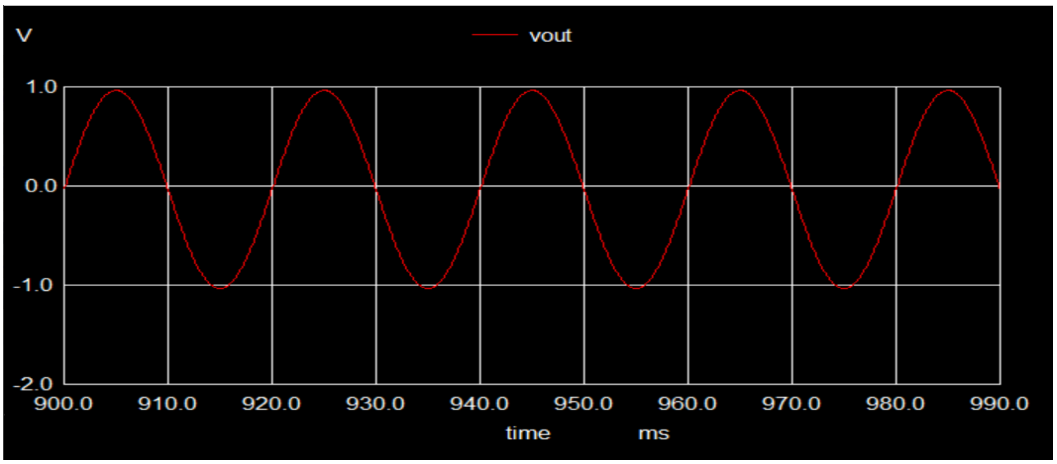


Figure 4.6: Output Plot with Differential Gain Ad=10

Vin1 = 1.0V

Vin2 = 1.1V

Vout = 1v

= 1.0/(0.1)

Hence Differential Gain, Ad = 10

4.2 MPY100 - Analog Multiplier

The MPY100 multiplier-divider is an affordable precision device designed for versatile applications. It supports four-quadrant multiplication as well as analog square root and division, eliminating the need for external amplifiers or potentiometers.

Its laser-trimmed, single-chip design ensures highly reliable operation with guaranteed accuracy. Thanks to its internal reference and pretrimmed accuracies, the MPY100 overcomes the limitations typically associated with other low-cost multipliers. It is available in TO-100 and DIP ceramic packages.

The MPY100 multiplier-divider can be used in a variety of applications, including:

1. Signal Processing: Performing analog computations like multiplication, division, and square root operations in real-time signal processing systems.

2. Instrumentation: Used in precision measurement instruments for tasks such as power measurement, RMS calculations, and other analog computations.

3. Modulation and Demodulation: Utilized in communication systems for amplitude modulation (AM) and demodulation processes.

4. Analog Filters: Creating variable-gain amplifiers and other analog filter designs that require precise gain control.

4.2.1 IC Layout

This figure represents the 8-Pin Package Diagram of the MPY100 Analog Multiplier IC

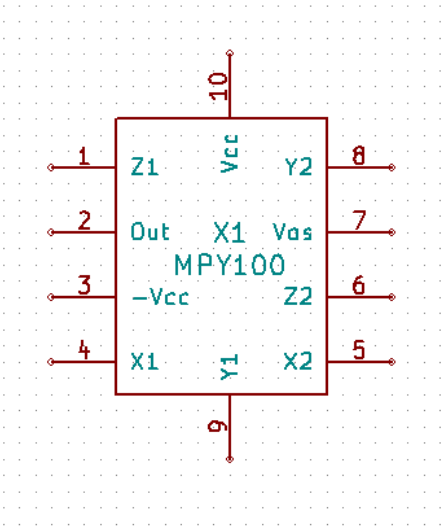


Figure 4.7: MPY100 Analog Multiplier IC

4.2.2 Subcircuit Schematic Diagram

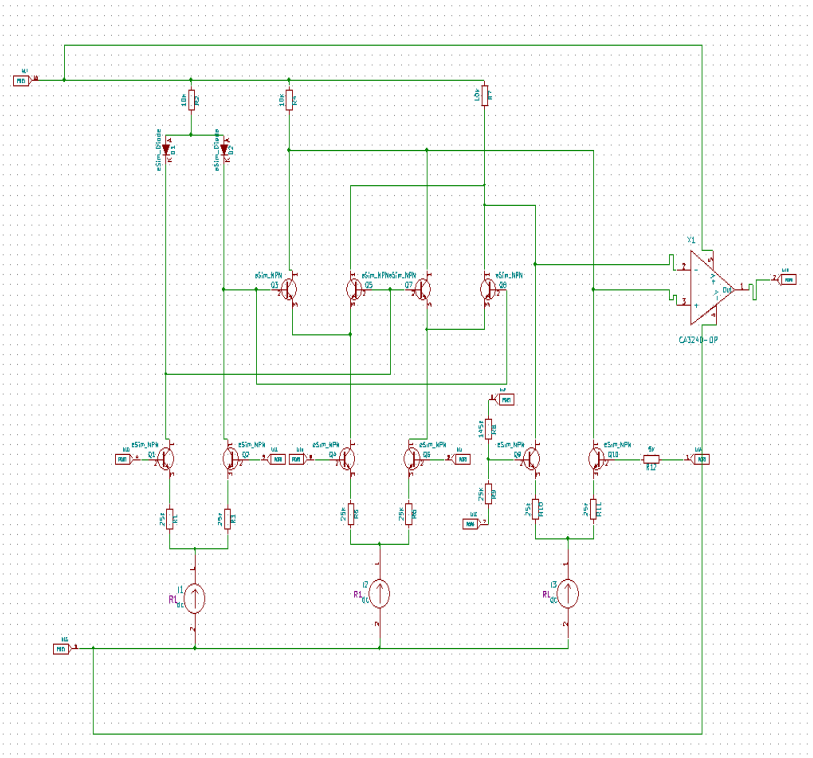


Figure 4.8: Subcircuit Schematic of MPY100

4.2.3 Test Circuit

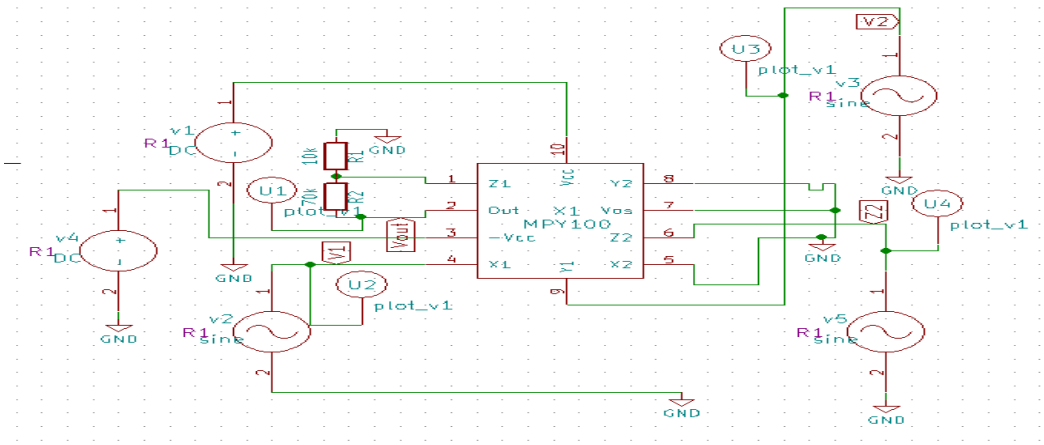


Figure 4.9: Test Circuit of MPY100

4.2.4 Input Plots

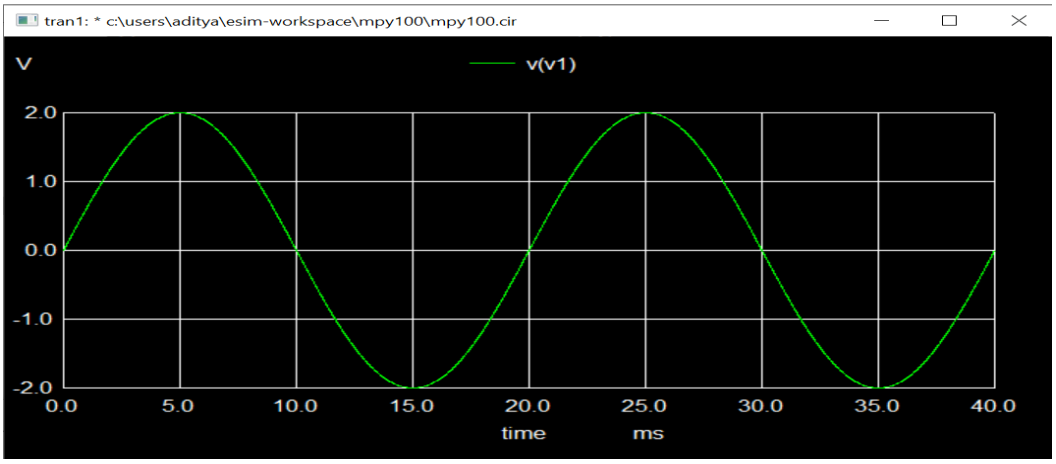


Figure 4.10: Vin1 = 2V

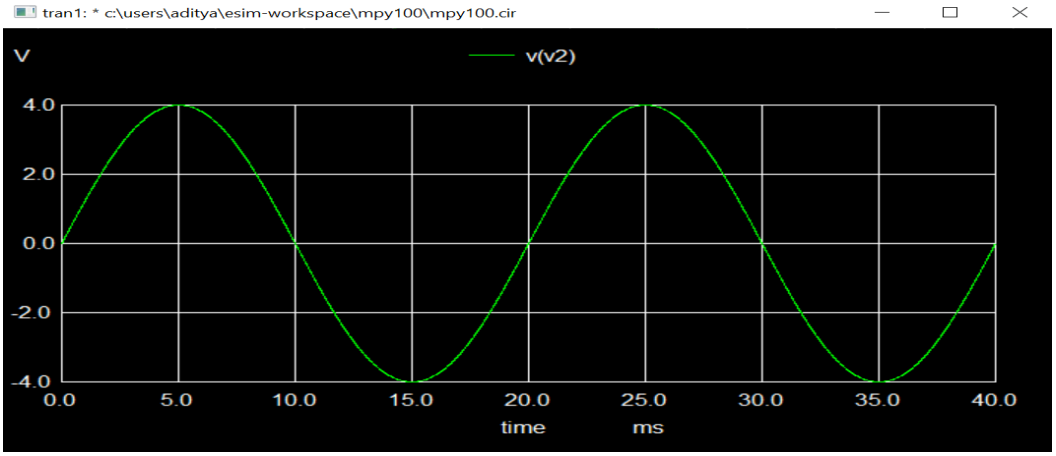


Figure 4.11: Vin2 = 4V

4.2.5 Output Plots

We know that the output voltage of the MPY100 multiplier,
Vout =(X1-X2)(Y1-Y2)+(Z2) Where,

X1-X2 = Vin1 = 2V (peak) sine wave

Y1-Y2 = Vin2 = 4V (peak) sine wave

Z2 = 0V

Vout=(X1-X2)(Y1-Y2)+(Z2) = (2x4V)+ 0V = 8V (peak) sine wave

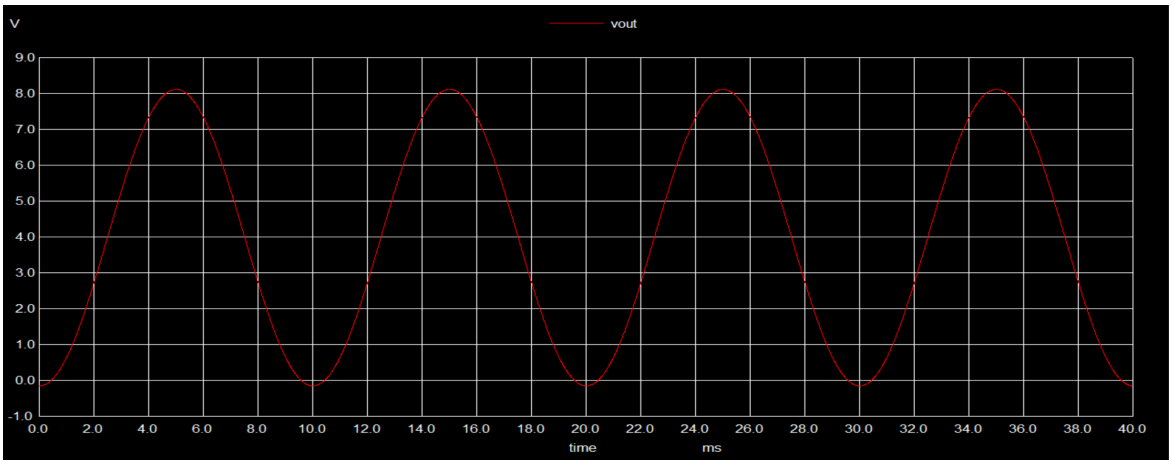


Figure 4.12: Vout = 8V sine-wave

4.3 LOG100 - Logarithmic Amplifier

The LOG100 amplifier is a highly versatile and precise electronic component designed for logarithmic amplification, effectively converting a wide range of input signals into a proportional logarithmic output. This capability makes it invaluable in fields requiring accurate signal processing across a broad dynamic range with minimal error and noise.

It boasts features like high input impedance, rapid response times, and temperature compensation, ensuring reliable performance under various conditions.

Its robust construction and availability as an integrated circuit enhance its suitability for compact and high-precision applications. The LOG100 finds application in several areas:

1. Scientific Instrumentation: Measures signals over a vast range of values, crucial for accurate data collection.

2. Communications: Processes RF and IF signals for amplitude modulation detection and signal strength indication.

3.Medical Equipment: Handles biological signals with significant magnitude variations, ensuring precise diagnostics.

4.Audio Processing: Compresses audio signal ranges to improve sound quality and manage dynamic audio content effectively.

4.3.1 IC Layout

This figure represents the 14-Pin Package Diagram of the LOG100 Amplifier IC

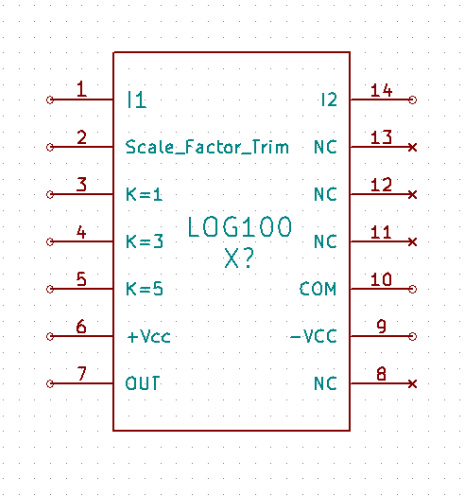


Figure 4.13: LOG100 Amplifier IC

4.3.2 Subcircuit Schematic Diagram

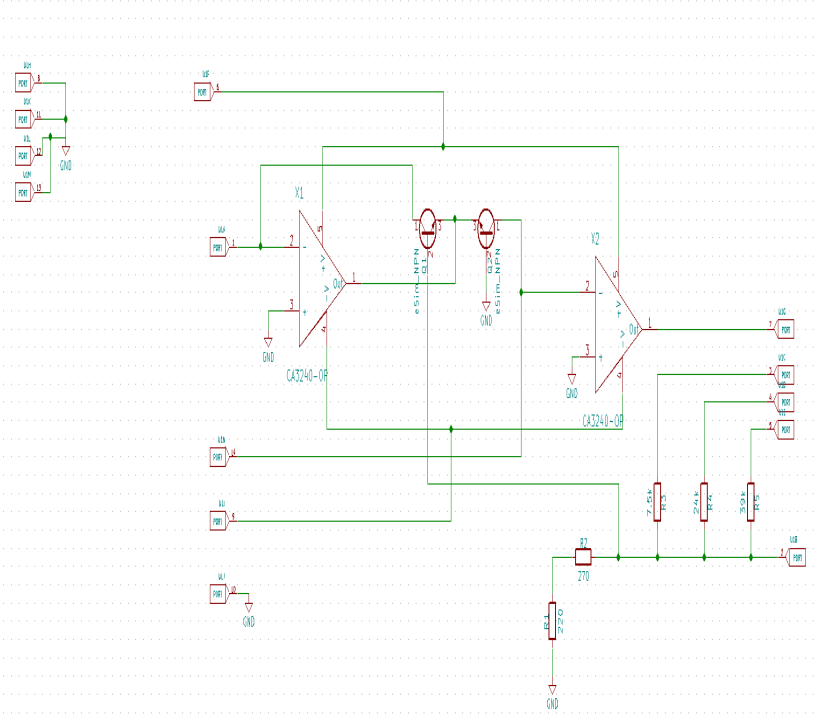
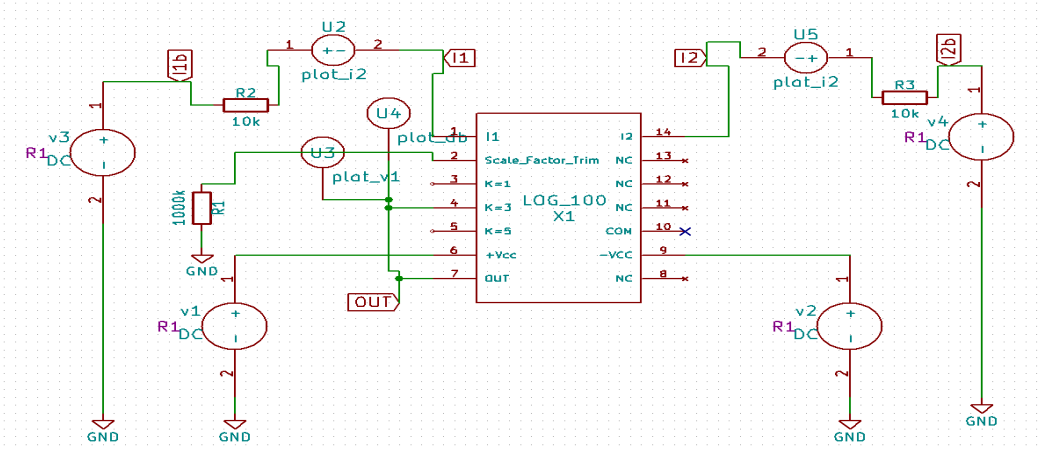


Figure 4.14: Subcircuit Schematic of LOG100

4.3.3 Test Circuit



4.3.4 Input Plots

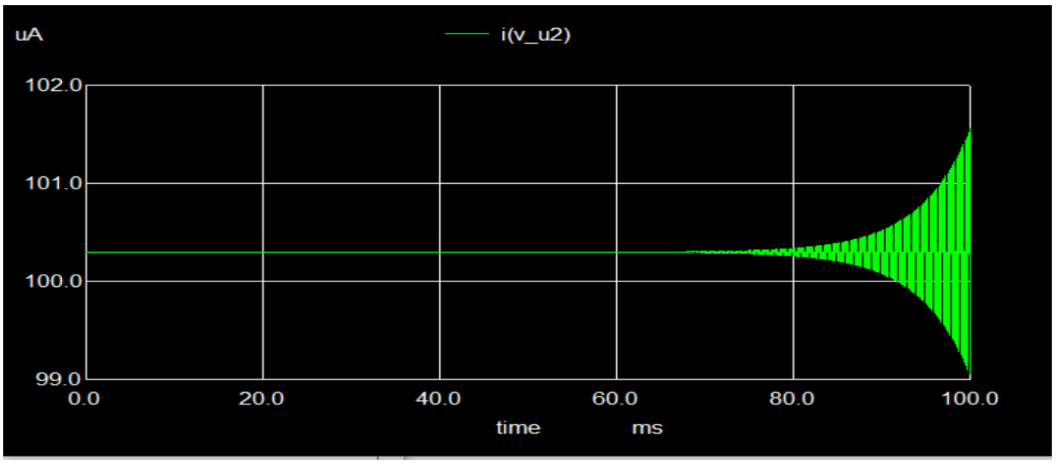


Figure 4.15: I1 = 102uA

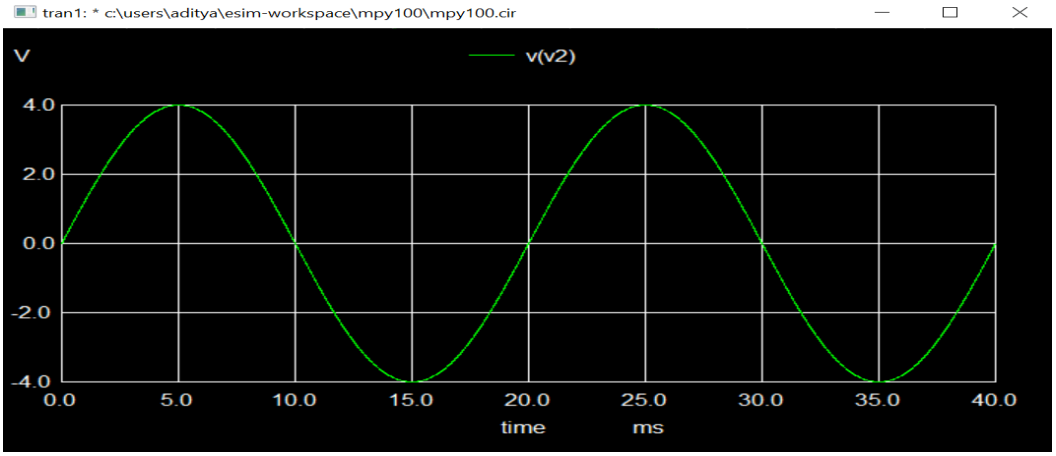


Figure 4.16: I2 = 10.33uA

4.3.5 Output Plots

The output voltage of the LOG100 amplifier is,
Vout = K LOG (I1/I2) Where, K = Scale Factor, you can select between 1,3 and 5

I1 = Input current 1

I2 = Input current 2

Hence, as per our inputs Vout = K LOG (I1/I2) = 3 Log (102 uA / 10.33 uA) Vout = 2.94, which is almost equal to the theoretical value of 2.96

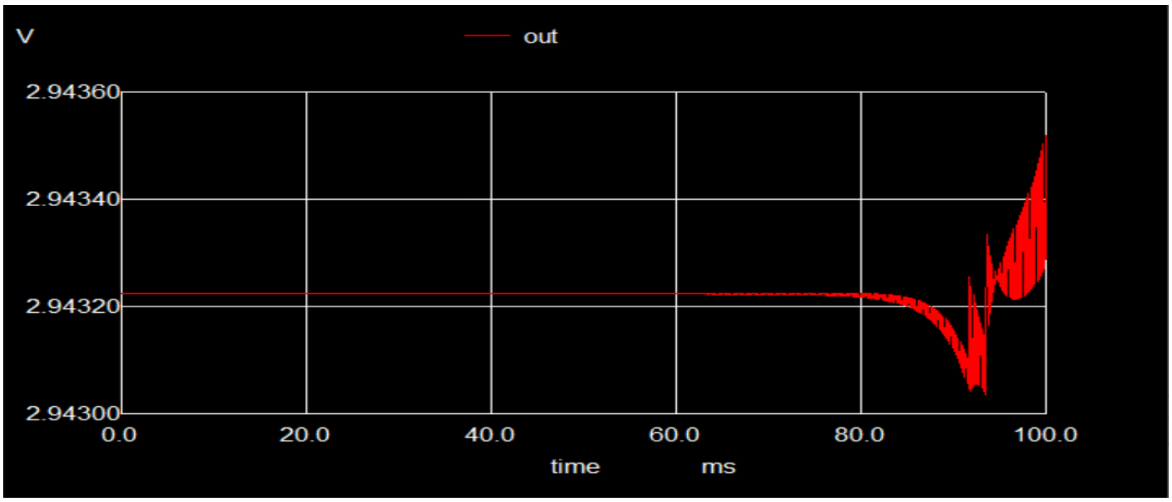
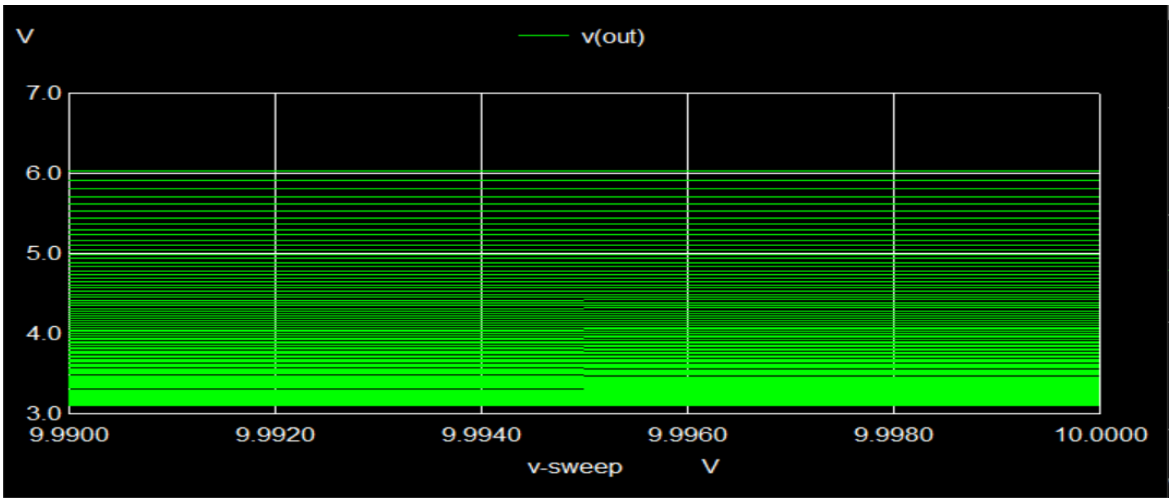


Figure 4.17: Vout = Log of the input currents = 2.94 V



4.4 MC1455B Timer

The MC1455 monolithic timing circuit is a highly stable device designed for generating precise time delays or oscillations. It includes additional terminals for optional triggering or resetting. In its time delay mode, the timing is accurately managed by one external resistor and capacitor.

For astable operation as an oscillator, both the free-running frequency and duty cycle are precisely controlled using two external resistors and one capacitor. The circuit can be triggered and reset by falling waveforms, and its output structure is capable of sourcing or sinking up to 200 mA, making it suitable for driving TTL circuits. The key features of the MC1455 monolithic timing circuit are-

1. High Stability: Ensures reliable and accurate time delays or oscillations in various applications

2.Versatile Triggering and Resetting: Includes additional terminals that allow for optional triggering or resetting as needed.

3. Precise Timing Control: Time delay mode is precisely managed using one external resistor and capacitor, while astable operation is controlled with two resistors and one capacitor.

4. Robust Output Structure: Capable of sourcing or sinking up to 200 mA, suitable for driving TTL circuits.

4.4.1 IC Layout

This figure represents the 8-Pin Package Diagram of the MC1455B Timer IC

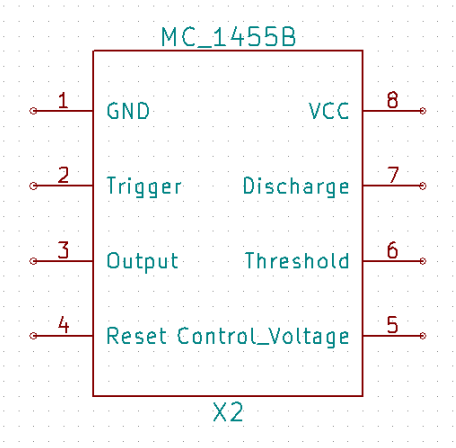


Figure 4.18: MC1455B Timer IC

4.4.2 Subcircuit Schematic Diagram

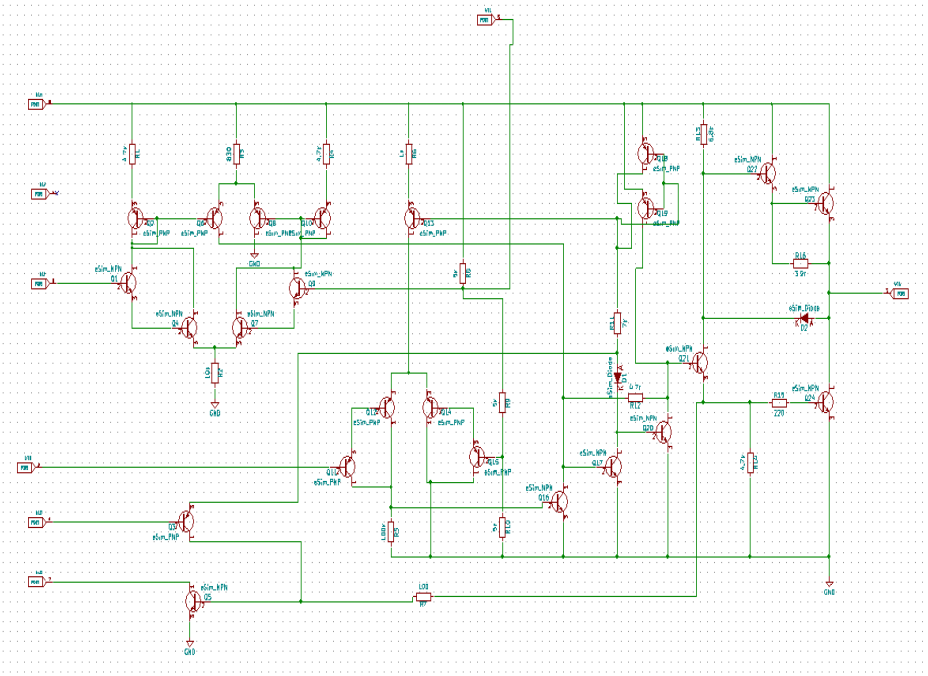


Figure 4.19: Subcircuit Schematic of MC1455B

4.4.3 Astable Multi-vibrator Test Circuit

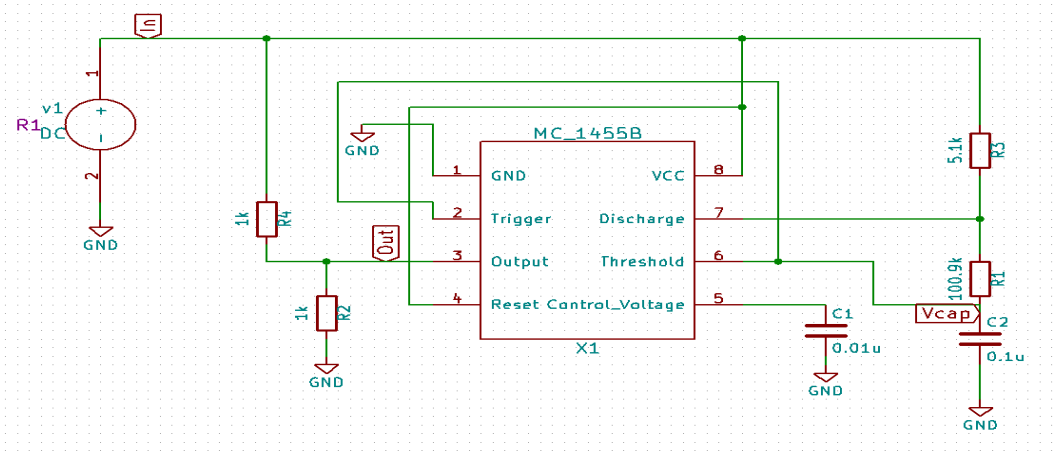


Figure 4.20: Astable Multi-vibrator Test Circuit of MC1455B

4.4.4 Input Plots

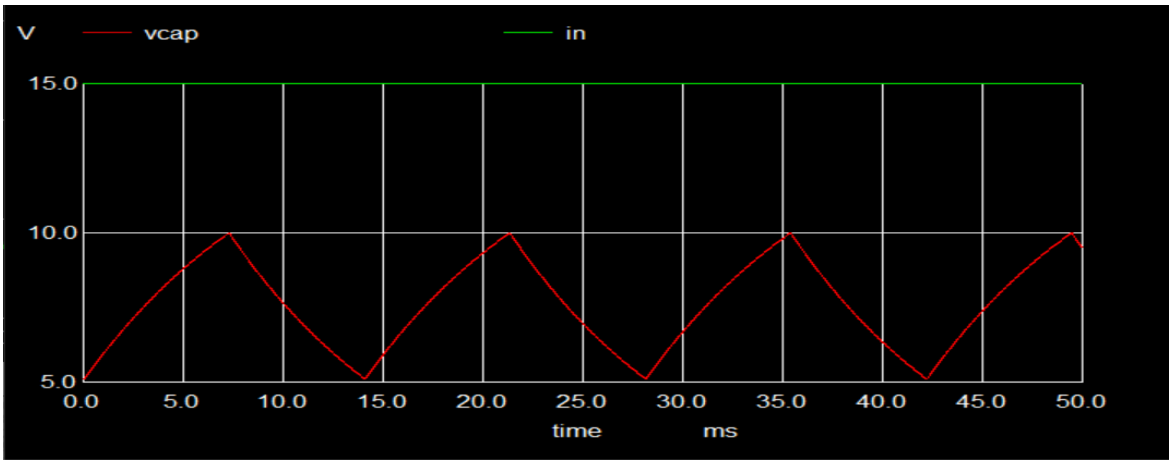


Figure 4.21: VCC=15V and Capacitor Voltage Waveform

4.4.5 Output Plots

For our Test Circuit, RA= 5.1k ohm , RB= 100.9 kohm, RL= 1k ohm and C= 0.1uF

The charge time (output high) is given by: t1 = 0.695(RA + RB)C = 7.367ms
The discharge time (output low) is given by: t2 = 0.695(RB)C = 7.0125ms
Thus the total period is given by: T = t1 + t2 = 0.695(RA + 2RB)C = 14.3795 ms
The frequency of oscillation is then: f = 1.44 / (RA + 2RB)C = 69.59 Hz
The duty cycle is given by: DC = (RA + RB)/(RA + 2RB) = 51.32 percent

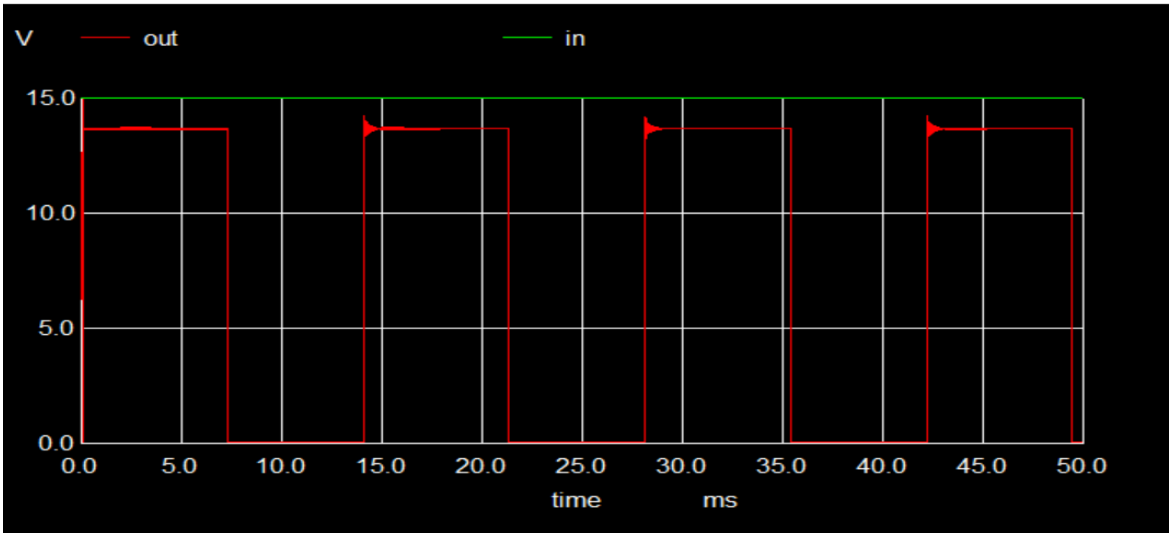


Figure 4.22: Output Voltage Waveform of MC1455B

4.5 MC1496 Balanced Modulator Demodulator

The MC1496 is a versatile balanced modulator and demodulator integrated circuit known for its high performance in various signal processing applications. It is designed to handle both analog and digital signals, making it a key component in communication systems.

The MC1496 excels in tasks such as amplitude modulation (AM), frequency modulation (FM), and phase modulation (PM), ensuring precise signal modulation and demodulation. Its balanced structure minimizes distortion and provides excellent carrier suppression, resulting in clear and accurate signal transmission. With a wide frequency range and the ability to operate at low power, the MC1496 is ideal for use in radio receivers, transmitters, and other RF communication devices. The key features of the MC1496 are -

1. Balanced Modulation and Demodulation: Provides high-performance signal modulation and demodulation with minimal distortion.

2. Wide Frequency Range: Capable of handling a broad spectrum of frequencies, making it suitable for various RF applications.

3. Excellent Carrier Suppression: Ensures clear and accurate signal transmission by minimizing unwanted carrier signals.

4. Low Power Operation: Designed to operate efficiently with low power consumption, ideal for battery-powered and portable devices.

4.5.1 IC Layout

This figure represents the 8-Pin Package Diagram of the MC1496 Balanced Modulator Demodulator

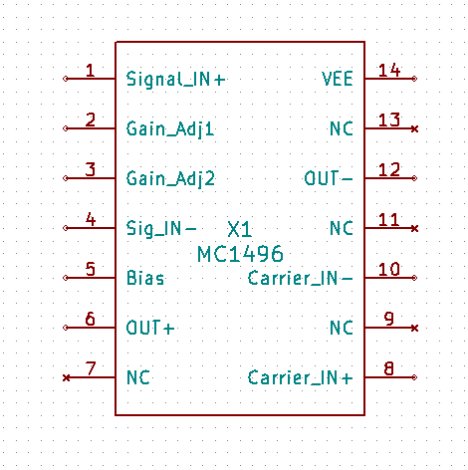


Figure 4.23: MC1496 Balanced Modulator Demodulator IC

4.5.2 Subcircuit Schematic Diagram

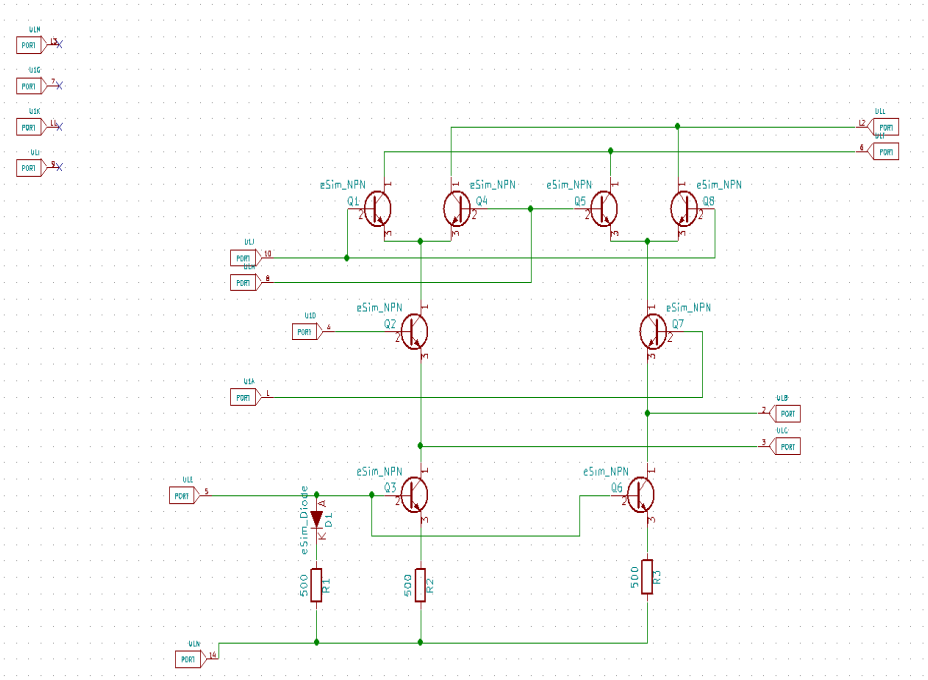


Figure 4.24: Subcircuit Schematic of MC1496

4.5.3 Balanced Modulator Demodulator

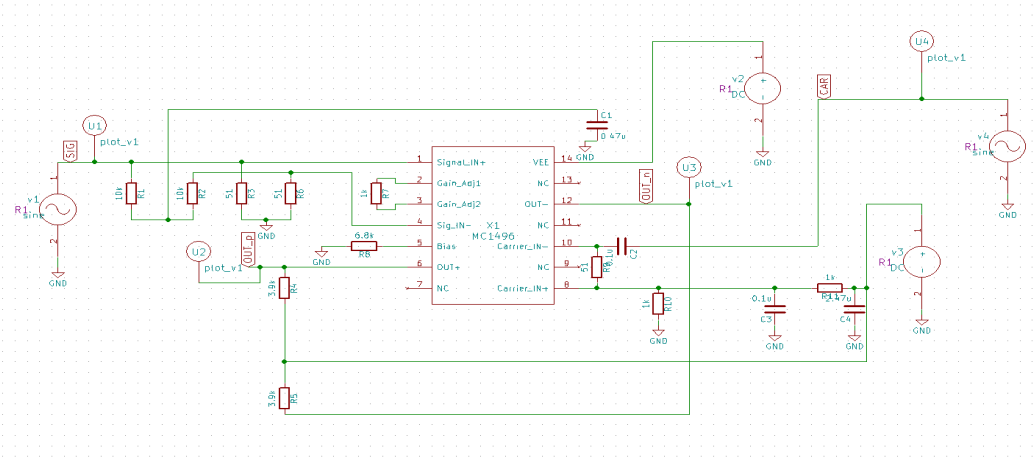


Figure 4.25: Balanced Modulator Demodulator Test Circuit of MC1496

4.5.4 Input Plots

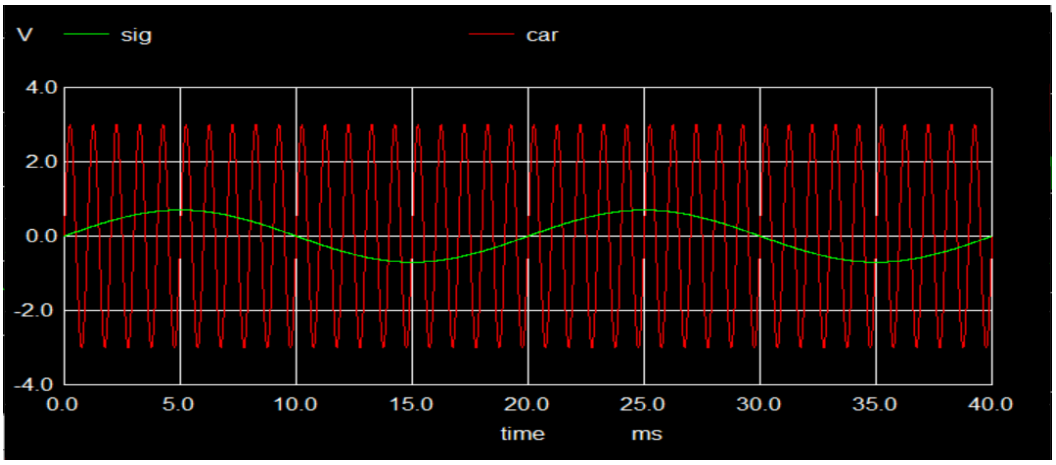


Figure 4.26: Vsig = 0.7V at 50 Hz and Vcar = 3V at 1 KHz

4.5.5 Output Plots

For our Test Circuit, RL= 3.9k ohm , RE= 1 kohm, re= 26 ohm
OUtput Voltage Gain is given by -
Vout = (0.637 * RL) / (RE + 2re) = 2.4
This multiplied with Vc is approximately equal to our Vout
Vout = Vc*2.4 = 3*1.414*2.4 =10.2V

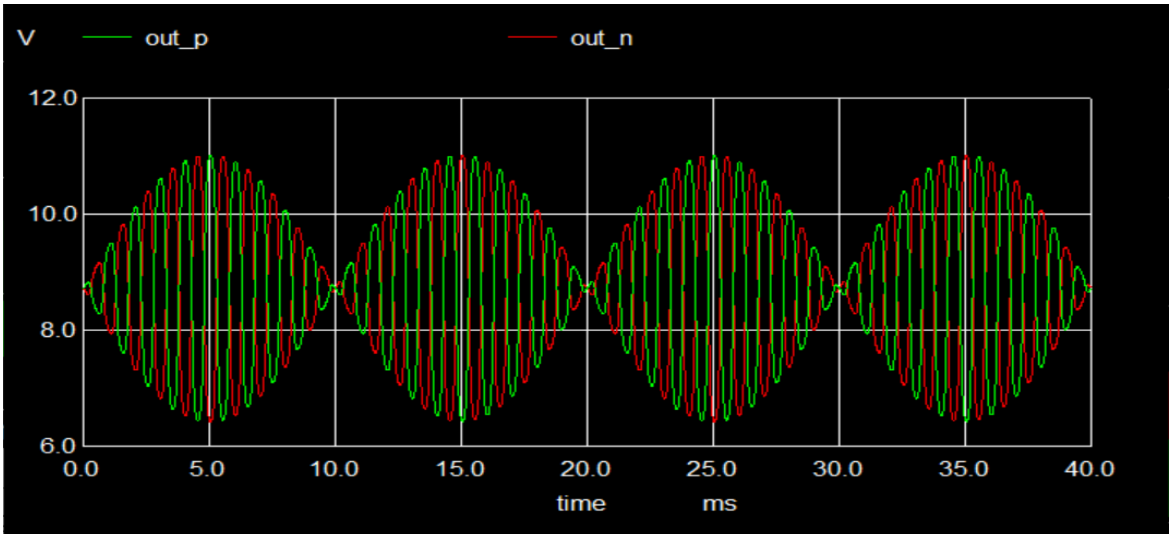


Figure 4.27: Balanced Output Voltage Waveform of MC1496

Chapter 5

Digital IC's

5.1 SN74LV3T97EP - Configurable Multiple-Function Gate

The SN74LV3T97-EP from Texas Instruments is a highly reliable, configurable multiple-function gate IC. The device offers configurable multiple functions with extended voltage operation, enabling level translation. The output state is determined by eight different patterns of 3-bit inputs, allowing users to select various logic functions such as MUX, AND, OR, NAND, NOR, inverter. The output level corresponds to the supply voltage (VCC) and supports CMOS levels of 1.2V, 1.8V, 2.5V, 3.3V, and 5V.

The input features a lower threshold circuit designed to facilitate up translation for lower voltage CMOS inputs, such as converting a 1.2V input to a 1.8V output or a 1.8V input to a 3.3V output. Additionally, the 5V tolerant input pins support down translation, like converting a 3.3V input to a 2.5V output.

5.1.1 IC Layout

This figure represents the 14-Pin Package Diagram of the SN74LV3T97-EP IC.

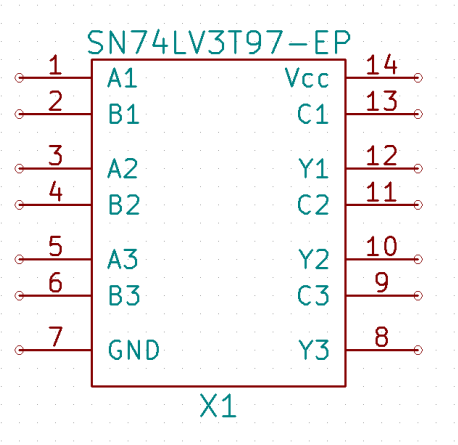


Figure 5.1: SN74LV3T97EP IC

5.1.2 Subcircuit Schematic Diagram

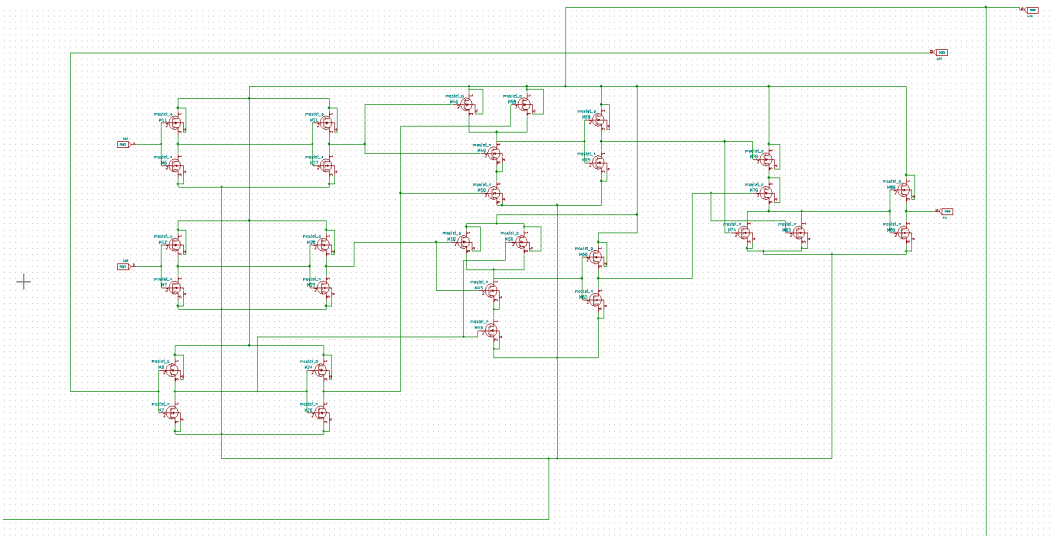


Figure 5.2: Subcircuit Schematic of SN74LV3T97EP IC (One of Three)

5.1.3 Test Circuit

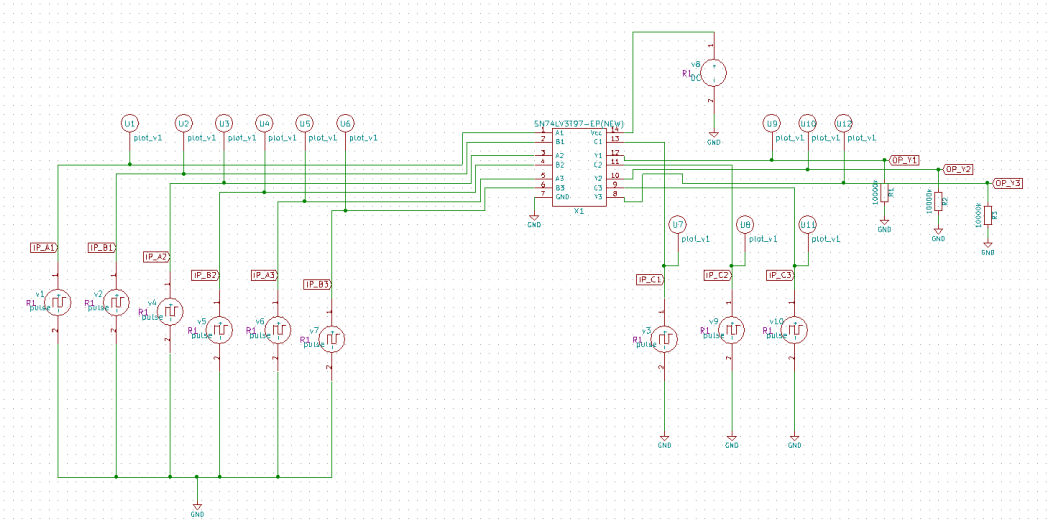


Figure 5.3: Test Circuit of SN74LV3T97EP IC

5.1.4 Input Plots

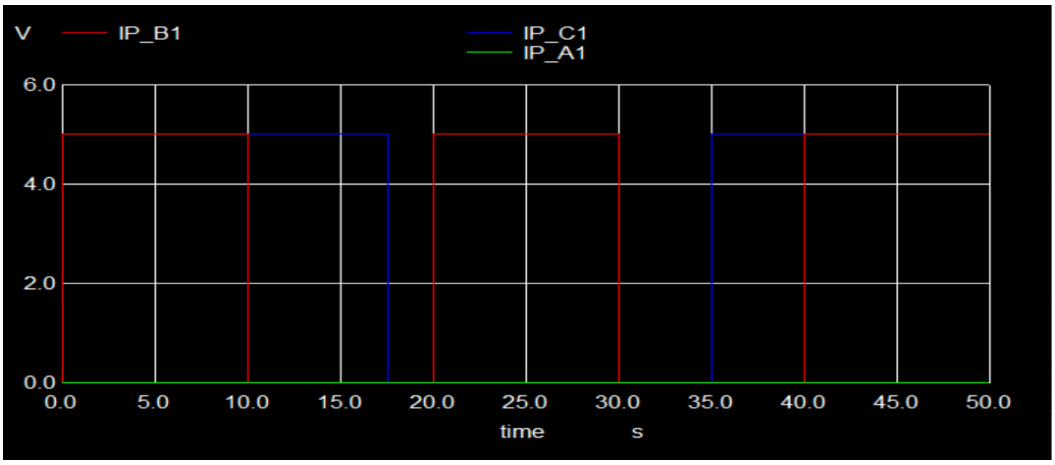


Figure 5.4: Case 1 - 2:1 Multiplexer Inputs

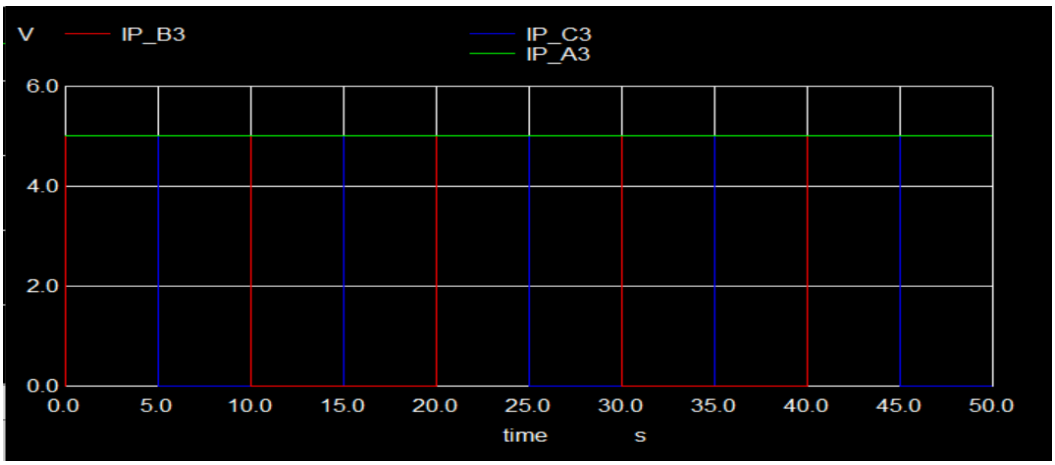


Figure 5.5: Case 2 - 2 Input OR gate Inputs

5.1.5 Output Plots

For Case 1-

We know that since it acts as Multiplexer, with A1 and B1 as inputs and C1 as the select signal. The output should be B1 when C1 is High, and output should be A1 when C1 is Low.

For Case 2-

The device acts as a 2-input OR gate when A3 is connected to VCC. The output is the logical OR between B3 and C3.

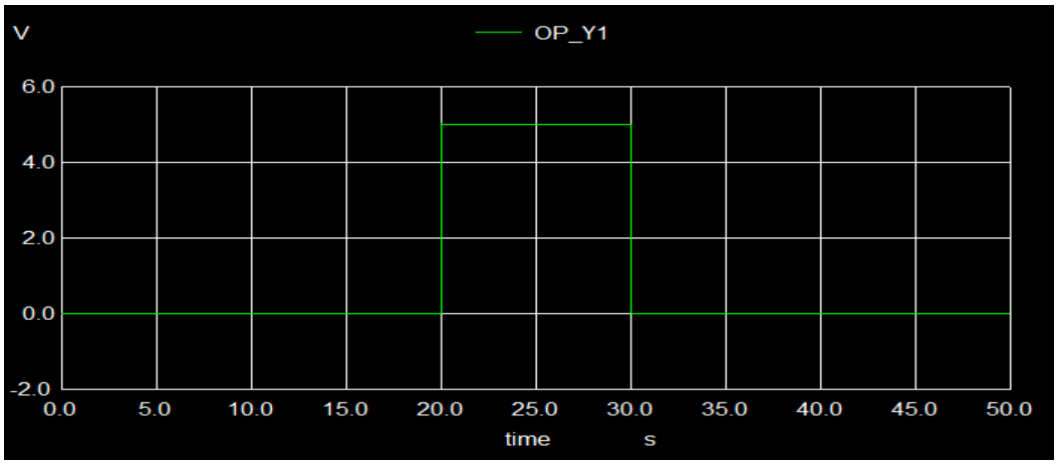


Figure 5.6: Output Plot of Case 1 - 2:1 Multiplexer

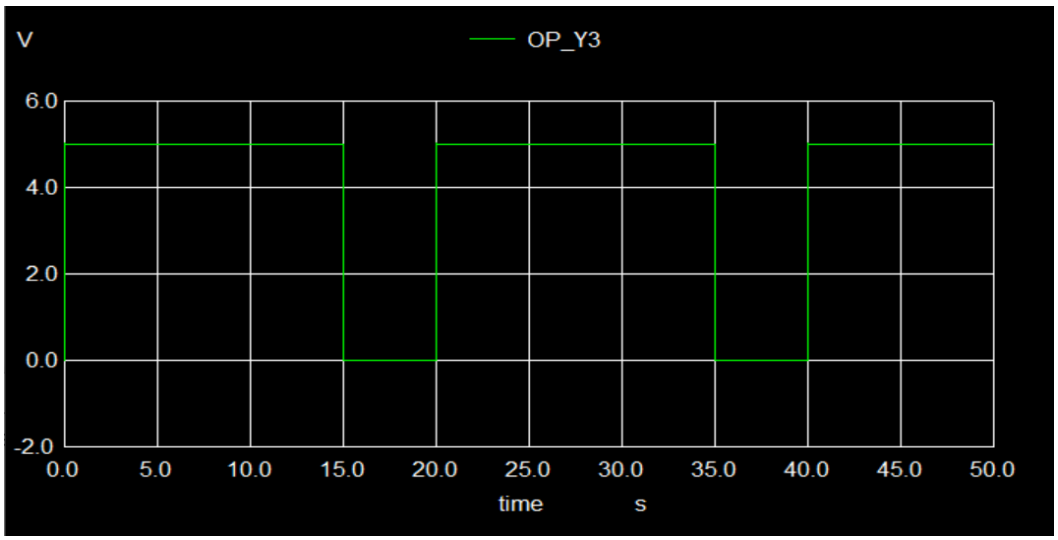


Figure 5.7: Output Plot of Case 2 - 2 Input OR gate

5.2 Static Memory - 6T SRAM Cell

A 6T SRAM cell, or six-transistor static random-access memory cell, is essential in high-speed and low-power memory systems. It consists of six transistors: two form cross-coupled inverters, and two serve as access transistors. These transistors create a bistable flip-flop that stores a single bit of data.

The inverters ensure data retention as long as the cell is powered, while the access transistors manage read and write operations when the word line is activated. Known for their stability, speed, and energy efficiency, 6T SRAM cells are ideal for cache memory and other applications requiring quick data access. Additionally, their design minimizes leakage currents, reducing power consumption during both active use and standby.

5.2.1 Cell Layout

This figure represents the 7-Pin Package Diagram of the 6T SRAM Cell

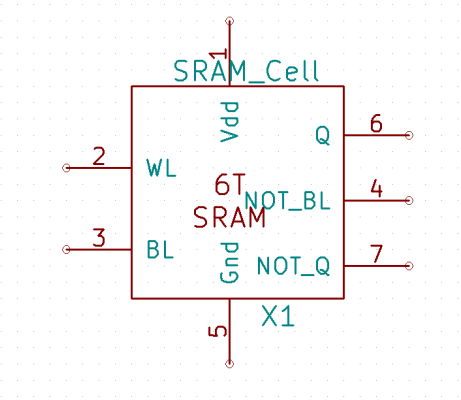


Figure 5.8: 6T SRAM Cell

5.2.2 Subcircuit Schematic Diagram

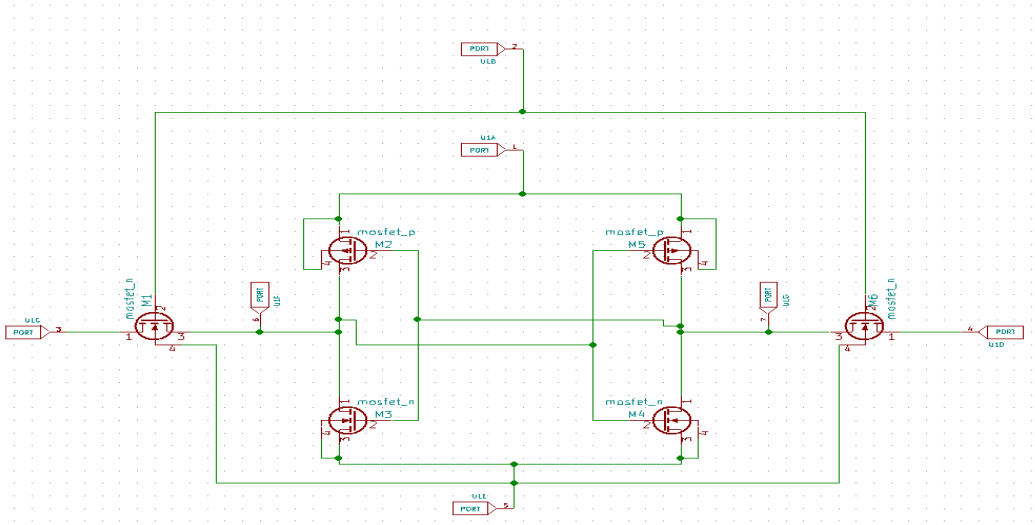


Figure 5.9: Subcircuit Schematic of the 6T SRAM Cell

5.2.3 Test Circuit

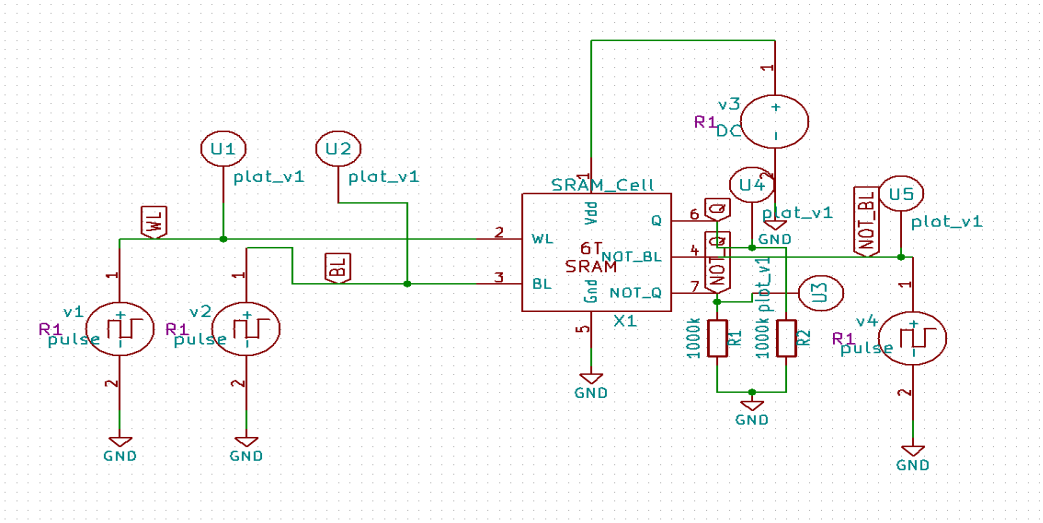


Figure 5.10: Test Circuit of 6T SRAM Cell

5.2.4 Input Plots

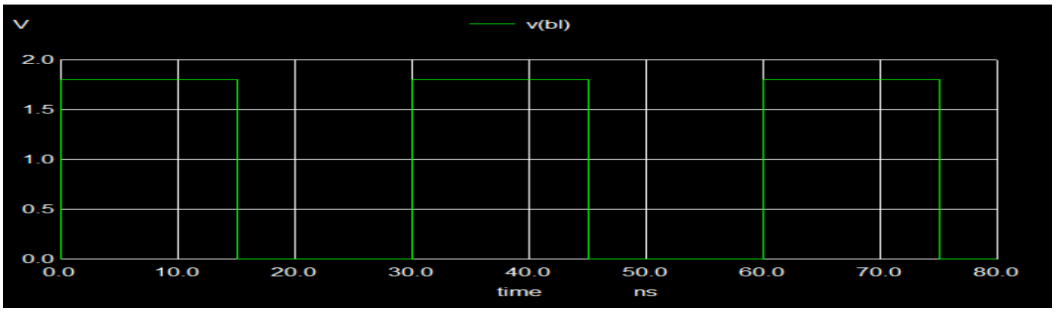


Figure 5.11: Bitline Voltage

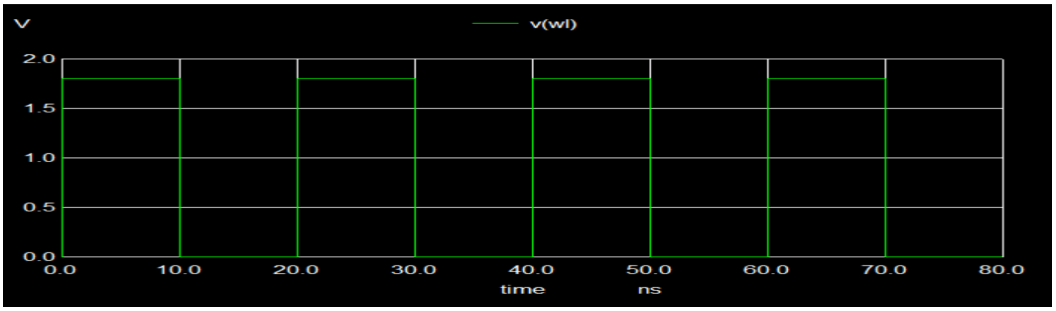


Figure 5.12: Wordline Voltage

5.2.5 Output Plots

Working Principle

A 6-transistor (6T) SRAM cell is a type of static random-access memory that uses six transistors to store a single bit of data. The cell consists of two cross-coupled inverters that form a bistable latch, which can hold either a '0' or '1'. The two bitlines (BL and BLB) are used to read from or write to the cell, while the wordline

(WL) controls the access to the cell. When the wordline is activated, the access transistors connect the storage nodes (formed by the inverters) to the bitlines. For a write operation, the bitlines are driven by external circuitry to the desired logic level, forcing the latch to the corresponding state. For a read operation, the precharged bitlines are allowed to discharge depending on the stored value, and the sense amplifiers detect the small voltage difference to determine the stored bit. The cell maintains its state as long as power is supplied, without requiring periodic refreshing like DRAM.

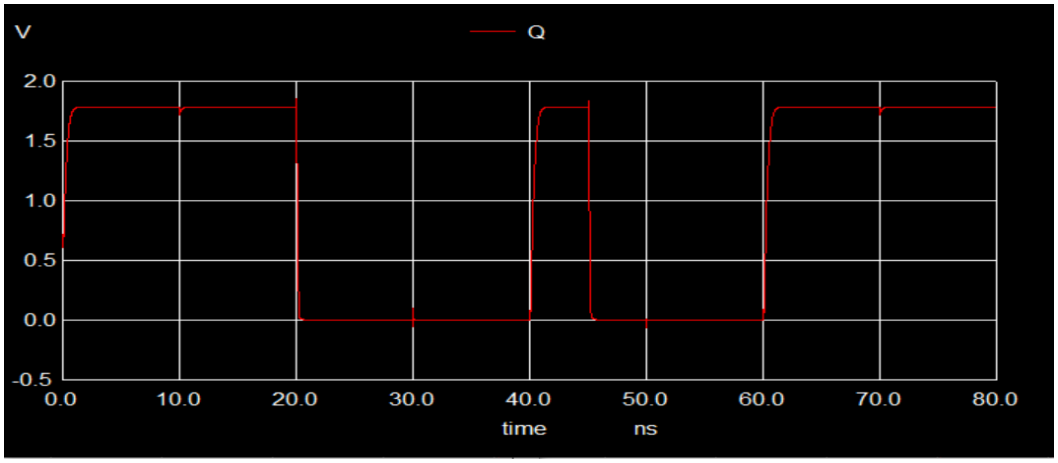


Figure 5.13: Output Plot of SRAM Cell - Q

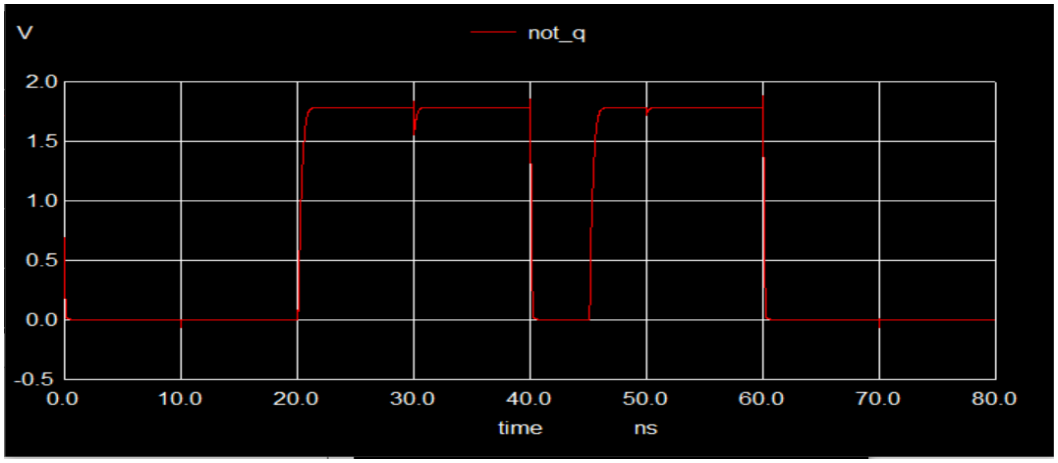


Figure 5.14: Output Plot of SRAM Cell - Q_Bar

5.3 IC 9348 - 12 Input Parity Generator/Checker

The 9348 is a 12-input parity checker/generator generating odd and even parity outputs. It can be used in high speed error detection applications.It provides odd and even parity for up to 12 data bits.

The Even Parity output (PE) will be HIGH if an even number of logic ones are present on the inputs. The Odd Parity output (PO) will be HIGH if an odd number of logic ones are present on the inputs. The key features of the IC 9348 are -

1. Error Detection in Data Transmission: It is used in communication systems to generate and check parity bits, ensuring that data transmitted over a network remains intact, by detecting errors in 12-bit data words.

2. Memory System Data Integrity: In memory systems, the IC 9348 can be used to monitor data integrity by generating parity bits during data write operations and checking them during read operations. This helps detect and correct single-bit errors in memory modules.

3. Digital Signal Processing (DSP) Systems: By generating and checking parity bits for 12-bit data blocks, it helps detect errors introduced during processing, ensuring reliable signal outputs in DSP Systems.

4. Peripheral Device Communication: Acts as an interface between a microcontroller and peripheral devices, where it ensures that data sent to or received from devices such as sensors, actuators, or other modules is error-free, enhancing the reliability of the overall system.

5.3.1 Cell Layout

This figure represents the 16-Pin Package Diagram of the IC 9348 - 12 Input Parity Generator/Checker

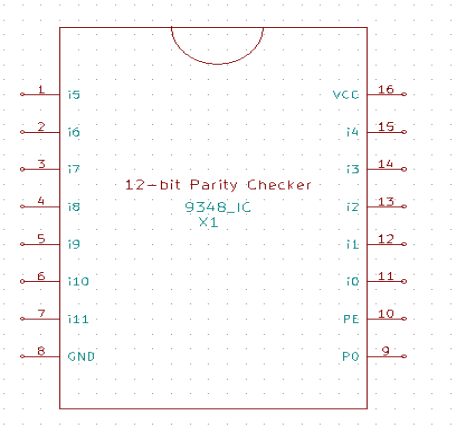


Figure 5.15: IC 9348 - 12 Input Parity Generator/Checker

5.3.2 Subcircuit Schematic Diagram

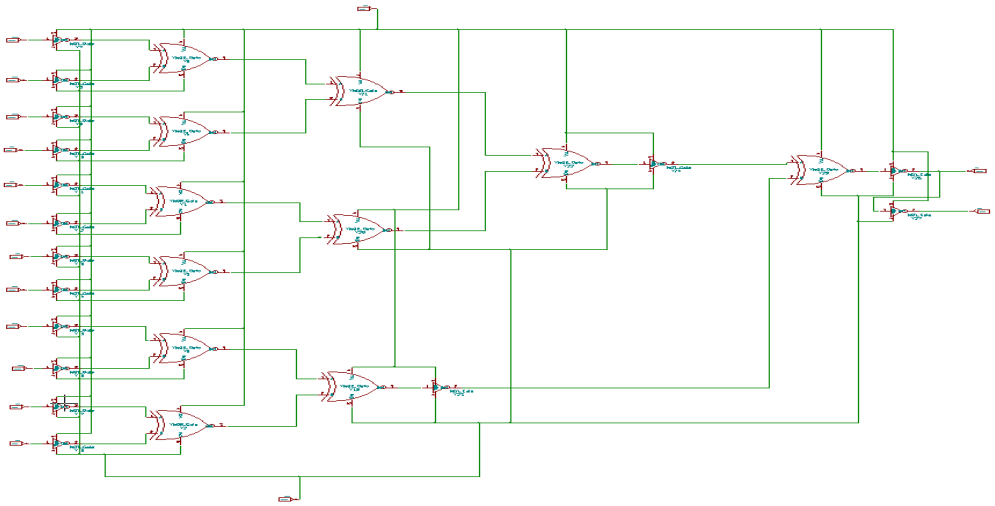


Figure 5.16: Subcircuit Schematic of the IC 9348

5.3.3 Test Circuit

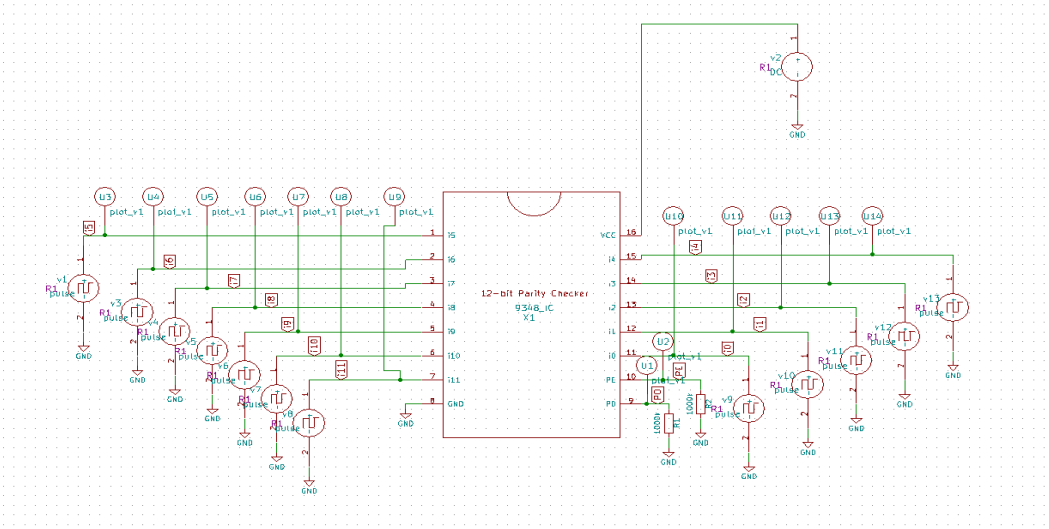


Figure 5.17: Test Circuit of IC 9348

5.3.4 Input Plots

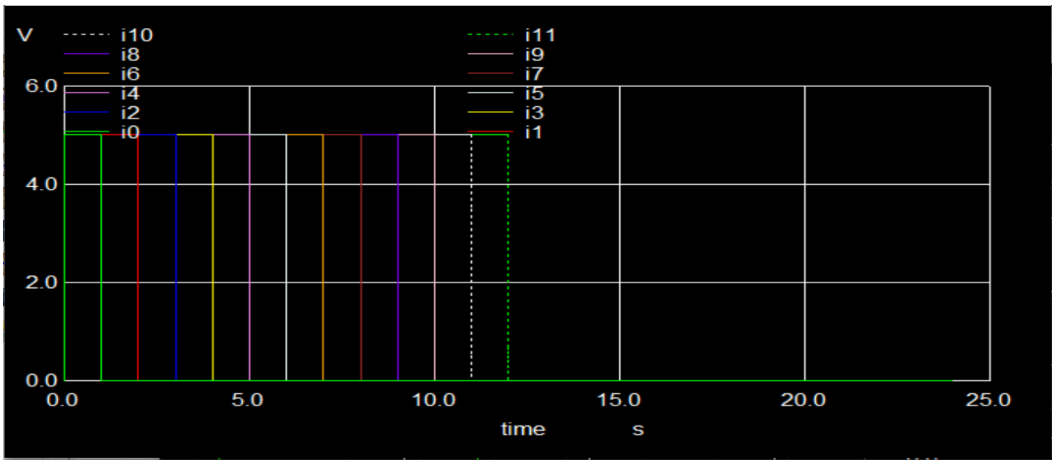


Figure 5.18: 12 Bit Inputs to IC 9348

5.3.5 Output Plots

The Odd Parity and Even Parity equations are given by -

PO = I0 XOR I1 XOR I2 XOR I3 XOR I4 XOR I5 XOR I6 XOR I7 XOR I8 XOR I9 XOR I10 XOR I11

PE = NOT(I0 XOR I1 XOR I2XOR I3 XOR I4 XOR I5 XOR I6 XOR I7 XOR I8 XOR I9 XOR I10 XOR I11)

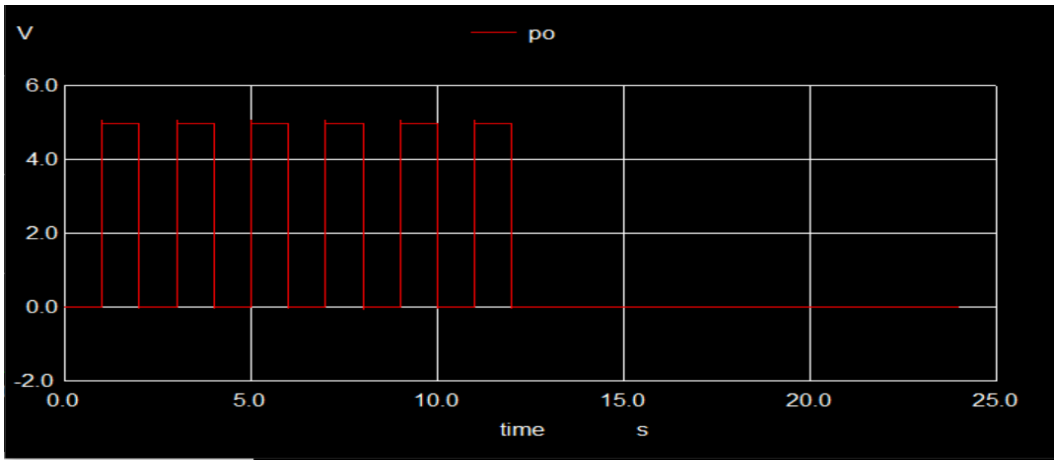


Figure 5.19: Output Plot of Odd Parity

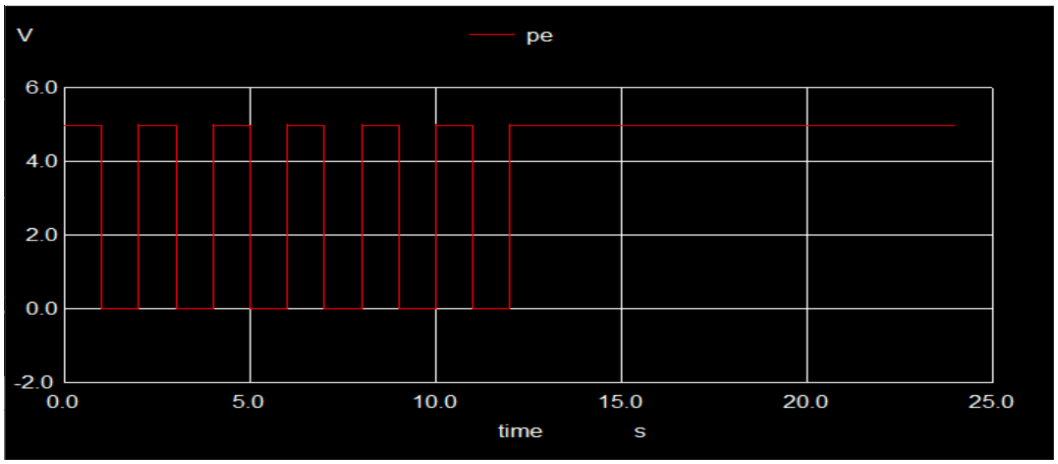


Figure 5.20: Output Plot of Even Parity

5.4 SN74F521 - 8 Bit Identity Comparator

The SN74F521 IC is an 8 Bit Identity Comparator. These identity comparators perform comparisons on two 8-bit binary or BCD words. It has open-collector outputs, allowing it to be used in wired-AND configurations with other open-collector devices. It is often used in data processing systems, address comparison in memory systems.

The SN54F521 is characterized for operation over the full temperature range of 55°C to 125°C. The SN74F521 is characterized for operation from 0°C to 70°C. This IC is widely used in systems where binary numbers need to be compared for equality. It features high-speed operation, with typical propagation delays around 5.5 nanoseconds.

1. 8-Bit Identity Comparison: The SN74F521 is designed to compare two 8-bit binary numbers. It outputs a low signal when the two numbers are identical, making it ideal for applications where precise equality checks between data streams or addresses are needed.

2. High-Speed Operation: With typical propagation delays of around 5.5 nanoseconds, the SN74F521 is well-suited for high-speed digital systems. This allows it to be used in time-sensitive applications, such as real-time data processing or fast decision-making circuits.

3. Open-Collector Outputs: The IC features open-collector outputs, which enable it to be used in wired-AND configurations with other devices. This is particularly useful in complex digital logic circuits where multiple comparison results need to be combined or controlled together.

4. Address Comparison in Memory Systems: The SN74F521 can be used in memory systems to compare addresses, ensuring that the correct data is accessed or written. By quickly verifying address equality, it helps improve the efficiency and accuracy of memory operations in computing systems.

5.4.1 Cell Layout

This figure represents the 20-Pin Package Diagram of the SN74HF521 - 8 Bit Comparator IC

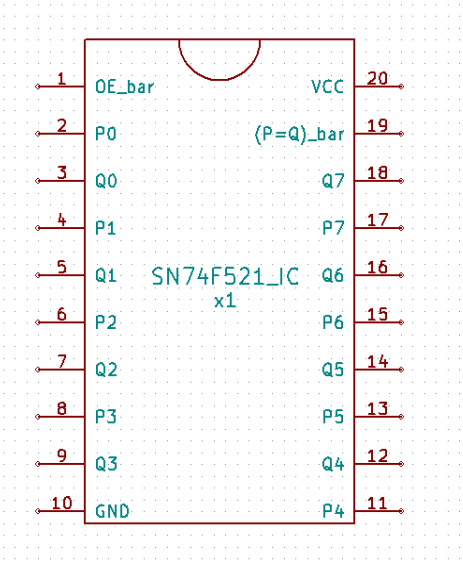


Figure 5.21: SN74HF521 - 8 Bit Comparator IC

5.4.2 Subcircuit Schematic Diagram

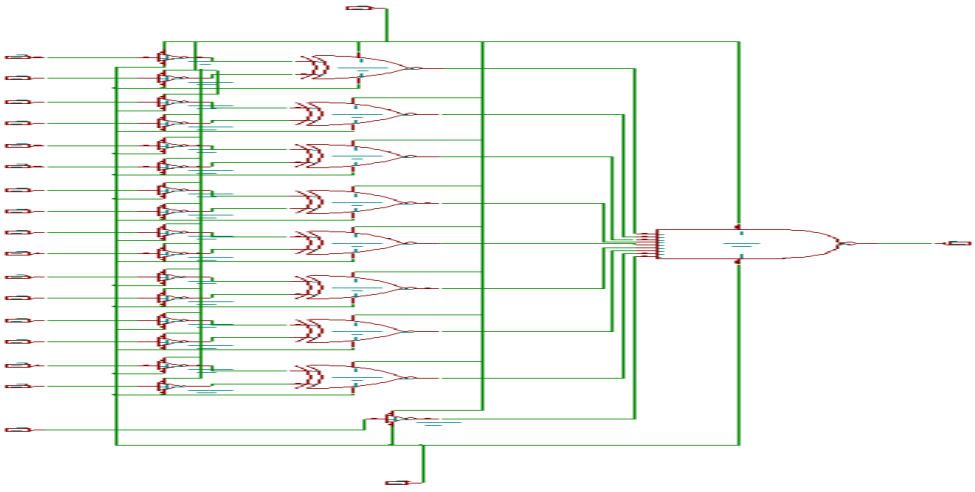


Figure 5.22: Subcircuit Schematic of the SN74HF521 IC

5.4.3 Test Circuit

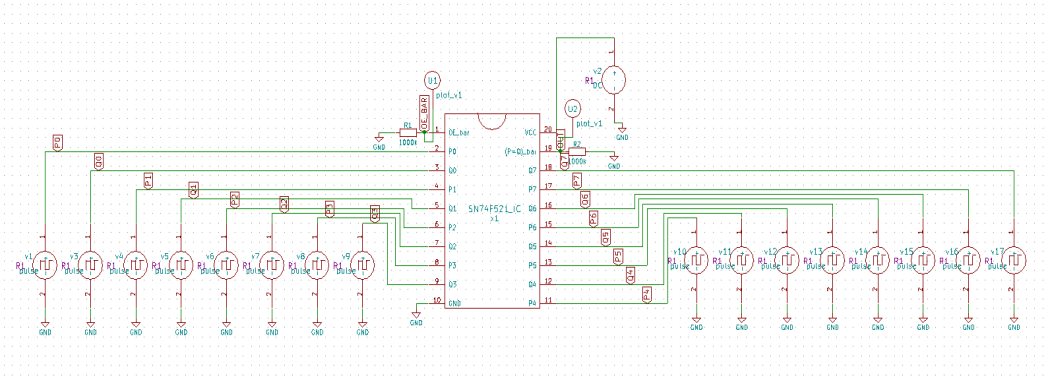


Figure 5.23: Test Circuit of SN74HF521

5.4.4 Input Plots

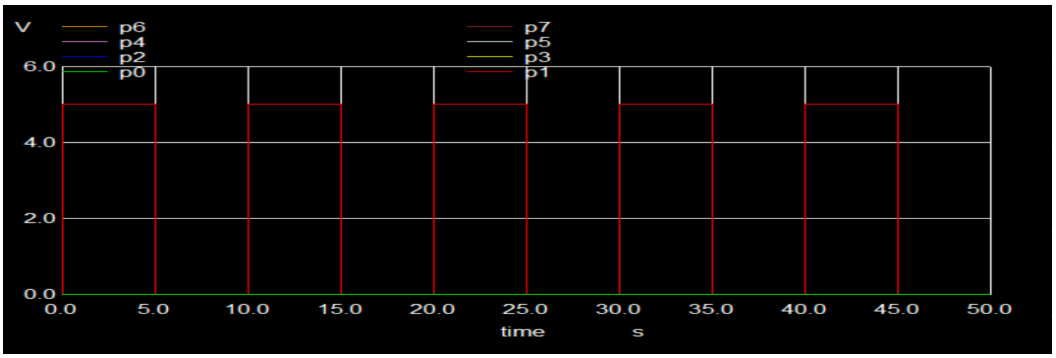


Figure 5.24: 8 Bit Input to SN74F521 IC , Represents one number P

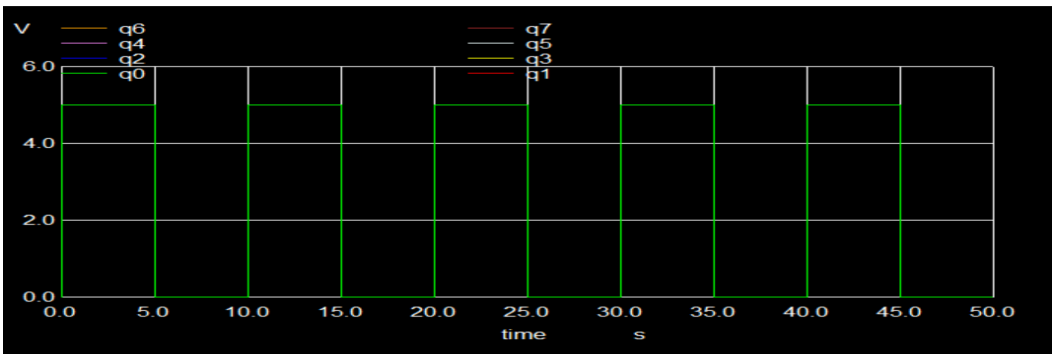


Figure 5.25: 8 Bit Input to SN74F521 IC, Represents one number Q

5.4.5 Output Plots

The IC evaluates each corresponding bit in the two numbers simultaneously. If all corresponding bits between the two inputs are identical, the IC outputs a low signal on its output pin, indicating equality. Conversely, if any bit differs between the two numbers, the output remains high, signaling that the numbers are not equal. The IC utilizes open-collector output, allowing it to be easily connected with other comparators in a wired-AND configuration. This feature makes it versatile in applications where multiple comparisons need to be logically combined. In our case, the all the bits of the Byte P and Q are same except P0 and Q0. P0 is always 0, whereas Q0 is a pulsates between high and low. This gives rise to our output voltage which is NOT(P = Q), hence is high when P and Q are unequal and low when P=Q. When Q0 is low, Output is low, when Q0 is high the Output is high.

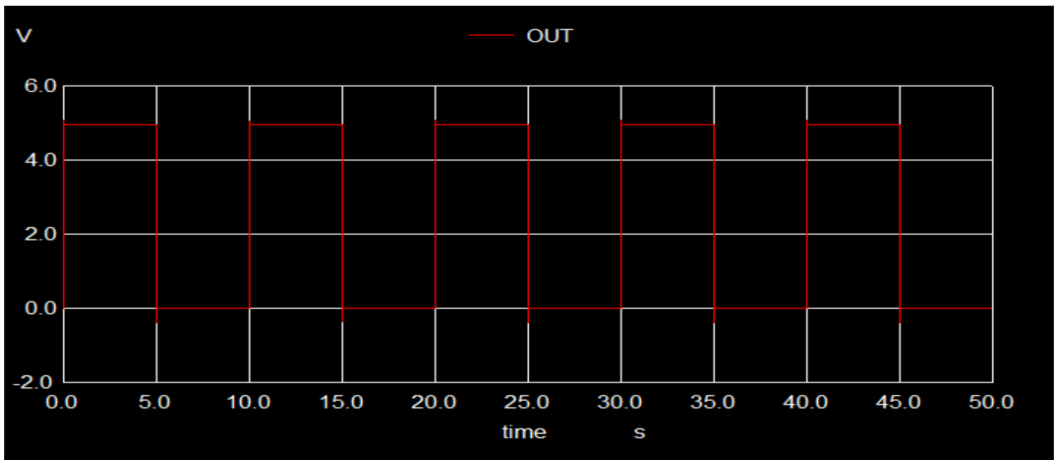


Figure 5.26: Output Plot of SN74F521 IC

5.5 SN54HC148 - 8:3 Priority Encoder IC

The SN54HC148 is a priority encoder IC from the 74HC logic family, which converts 8-input lines into a 3-bit binary output. It operates over a voltage range of 2V to 6V, making it adaptable for various uses.

The SN54HC148 offers high-speed performance, with typical propagation delays of around 16 ns at 5V, allowing for quick encoding in digital applications. The IC features active-low enable input (EI), active-low inputs (I0 to I7), and active-low outputs (Y0 to Y2), providing a 3-bit binary code representing the highest-priority active input. Some key applications of the encoder are-

1. Interrupt Management in Embedded Systems: It is widely used in embedded systems to manage multiple interrupt sources. It encodes the highest-priority interrupt request into a 3-bit binary output, enabling the microcontroller to quickly identify and service the most critical interrupt.

2. N-Bit Encoding in Digital Systems: It can be employed to encode multiple input lines into a smaller number of output lines. For example, it converts 8 input signals into a 3-bit binary code. In systems requiring more than 8 inputs, multiple SN54HC148 ICs can be cascaded to handle N-bit encoding

3. Code Converters and Generators: It can be used as part of a code conversion or generation process. For instance, in digital communication systems, the IC can convert a parallel input code into a different format or generate specific codes based on the priority of the inputs.

4. Input Signal Selection in Data Acquisition Systems: In data acquisition systems, the SN54HC148 prioritizes and encodes signals from multiple sensors or devices into a 3-bit code, ensuring that the most critical data is processed first.

5.5.1 Cell Layout

This figure represents the 16-Pin Package Diagram of the SN54HC148 - 8:3 Priority Encoder IC Generator/Checker

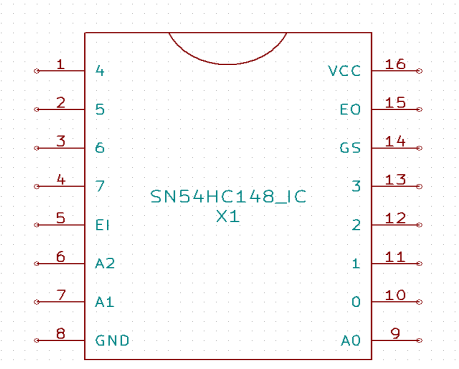


Figure 5.27: SN54HC148 - 8:3 Priority Encoder IC Generator/Checker

5.5.2 Subcircuit Schematic Diagram

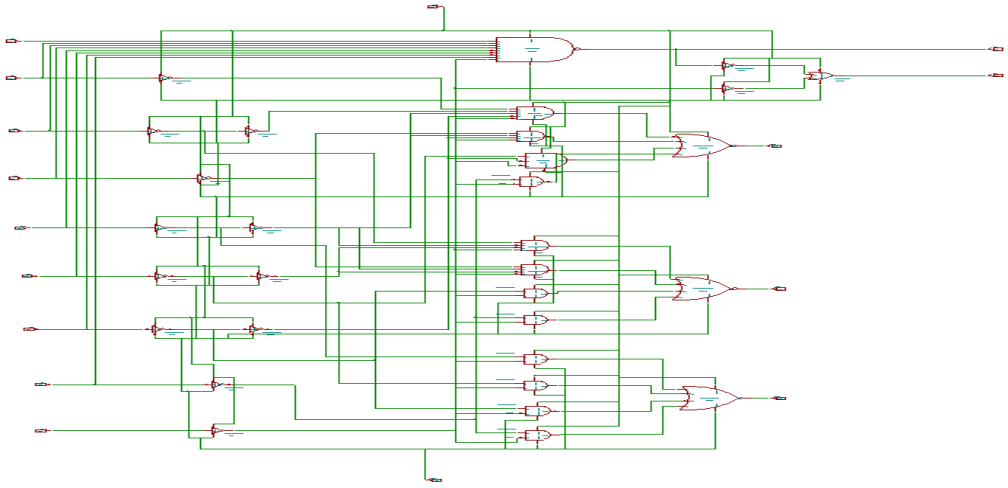


Figure 5.28: Subcircuit Schematic of the SN54HC148 IC

5.5.3 Test Circuit

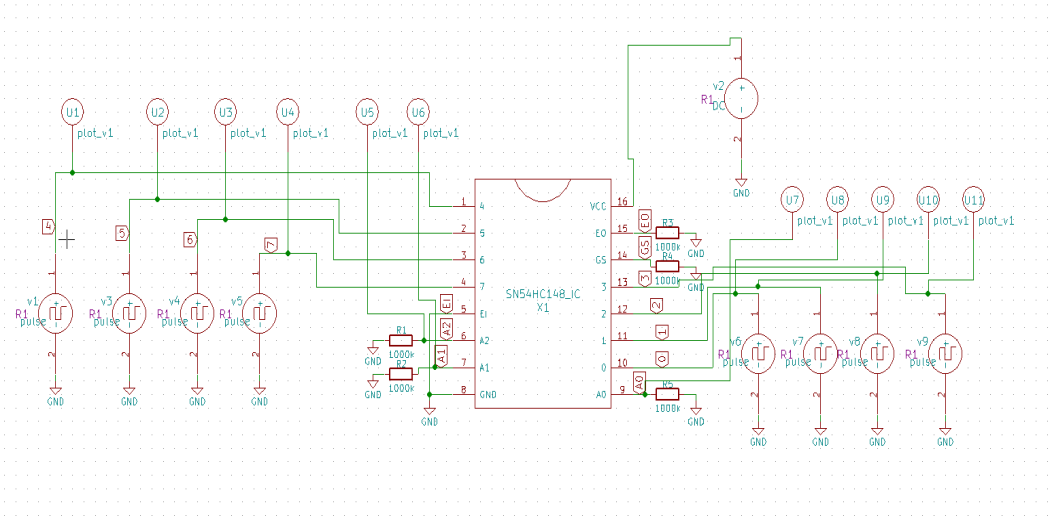


Figure 5.29: Test Circuit of SN54HC148 IC

5.5.4 Input Plots

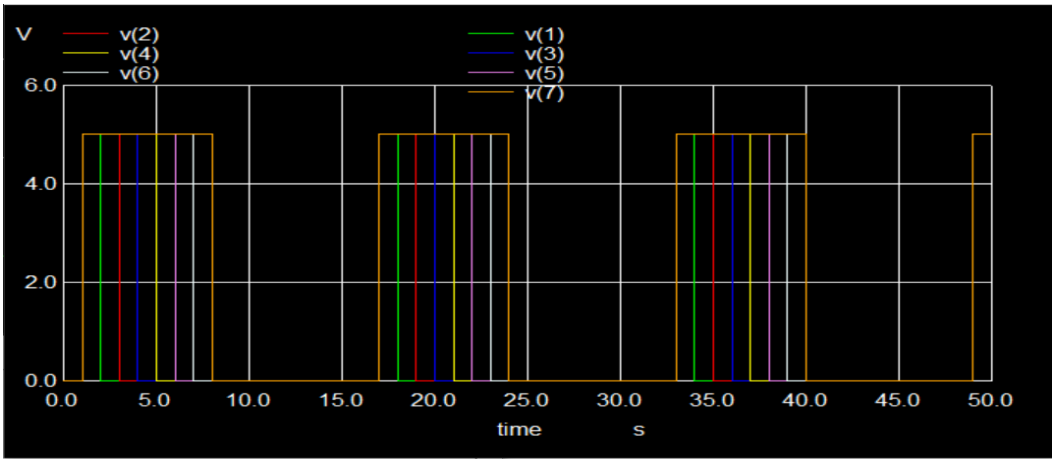


Figure 5.30: 8 Bit Inputs to SN54HC148 IC

5.5.5 Output Plots

The inputs (I0 to I7) are prioritized such that I7 has the highest priority, and I0 has the lowest. When multiple inputs are active (low), the IC outputs the binary code corresponding to the highest-priority active input. The IC also features an active-low Enable Input (EI) that, when low, enables the encoding process. Additionally, the SN54HC148 has a Group Select (GS) output, which indicates whether any input is active, and an Enable Output (EO), which is used for cascading multiple ICs to handle more inputs. The inputs are pulses are of time period 16s, and their duty cycle varies from 10 to 50 percent. The outputs are 3 bits, with each of a0, a1 and a2 representing the bits respectively from MSB to LSB

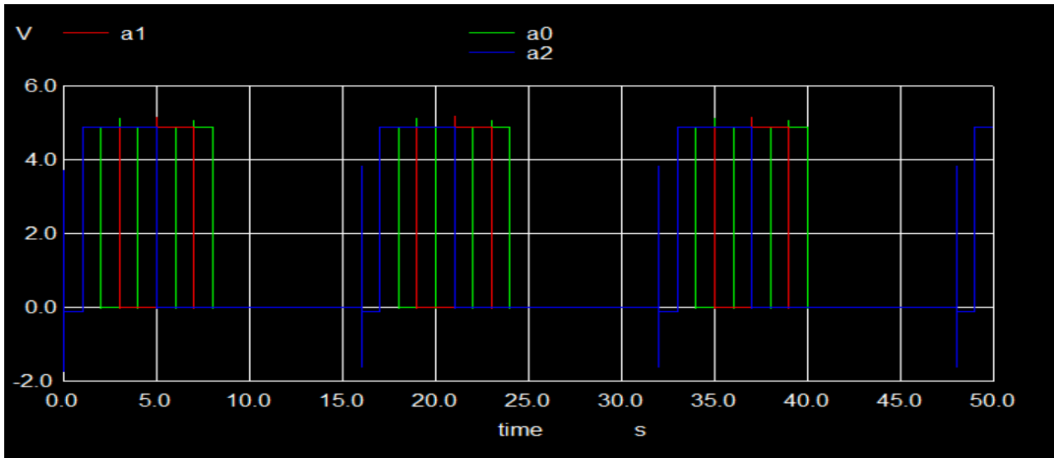


Figure 5.31: Output Plot of A0, A1,and A2

Chapter 6

Conclusion and Future Scope

Complementary metal oxide semiconductor (CMOS) digital integrated circuits are enabling technology for the modern information age. Because of their intrinsic features in low-power consumption, large noise margins, and ease of design, CMOS integrated circuits have been widely used to develop random access memory (RAM) chips, microprocessor chips, digital signal processor (DSP) chips, and application- specific integrated circuit (ASIC) chips. The popular use of CMOS circuits will grow with the increasing demands for low-power, low-noise integrated electronic systems in the development of portable computers, personal digital assistants (PDAs), portable phones, and multimedia agents.

VLSI Design has become a quite exquisite and necessary subject, which delves deep into the IC and semiconductor industry. Such designed schematics are of great importance as they form the stepping stones to the complicated schematics which we are used to today. This project focused on designing and developing a range of analog and digital integrated circuit models as sub-circuits using the existing device model files from the eSim library. The created IC models are intended to be added to the eSim subcircuit library, providing a valuable resource for developers and users engaged in circuit design. By successfully integrating these models into the library, the project enhances the capabilities of the eSim tool, making it easier for users to incorporate these circuits into their designs, thereby improving the overall efficiency and effectiveness of the design process.

Chapter 7

References

The following data sheets and references were used in developing the schematics of these IC's-

- CA3240A -https://www.renesas.com/us/en/document/dst/ca3240-ca3240a-datasheet
- LOG100 - https://www.digikey.at/htmldatasheets/production/4377/0/0/1/log100.html
- MC1455B - https://www.onsemi.com/pdf/datasheet/mc1455-d.pdf
- MC1496 - https://www.onsemi.com/download/data-sheet/pdf/mc1496-d.pdf
- MPY100 - https://www.ti.com/lit/gpn/MPY100
- IC 9348 -http://kazojc.com/elementy$_c$*zynne*/*IC*/9348.*pdf*
- SN54HC148 -https://www.ti.com/lit/ds/scls109h/scls109h.pdf
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